# EL7232

Dual Channel, High Speed, High Current Line Driver with 3-State

FN7283
Rev 4.00
November 12, 2015

The EL7232 3-state drivers are particularly well suited for ATE and microprocessor based applications. The low quiescent power dissipation makes this part attractive in battery applications. The 2A peak drive capability, makes the EL7232 an excellent choice when driving high speed capacitive lines, as well. The input circuitry provides level shifting from TTL levels to the supply rails. The EL7232 is available in 8 Ld PDIP and 8 Ld SO packages.

## Ordering Information

| PART NUMBER | PART MARKING | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| EL7232CN **No longer available or supported, recommended replacement: EL7232CNZ** | EL7232CN | 8 Ld PDIP | E8.3 |
| EL7232CNZ (Note) | EL7232CN Z | 8 Ld PDIP** | E8.3 |
| EL7232CSZ (Note) | 7232CSZ | 8 Ld SOIC (Pb-free) | M8.15E |
| EL7232CSZ-T7* (Note) | 7232CSZ | 8 Ld SOIC (Pb-free) Tape and Reel | M8.15E |
| EL7232CSZ-T13* (Note) | 7232CSZ | 8 Ld SOIC (Pb-free) Tape and Reel | M8.15E |

*-T7" suffix for 1k unit or "-T13" suffix for 2.5k unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

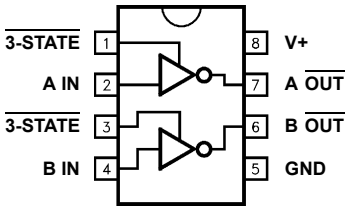
- 3-State output
- 3V and 5V input compatible
- Clocking speeds up to 10MHz
- 20ns Switching/delay time
- 2A Peak drive
- Low, matched output impedance 5Ω
- Low quiescent current 2.5mA
- Wide operating voltage 4.5V to 16V
- Pb-free available (RoHS compliant)

## Applications

- Parallel bus line drivers
- EPROM and PROM programming
- Motor controls
- Charge pumps
- Sampling circuits
- Pin drivers
- Bridge circuits

## Pinout

**EL7232**
**(8 LD PDIP, SO)**
TOP VIEW




Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

## Truth Table

| 3-STATE | INPUT | OUTPUT |
|---|---|---|
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 0 | Open |
| 0 | 1 | Open |

## Absolute Maximum Ratings ($T_A$ = +25°C)

Supply (V+ to Gnd) . . . . . 16.5V
Input Pins . . . . . -0.3V to +0.3V above V+
Combined Peak Output Current. . . . . .4A

## Thermal Information

Operating Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Power Dissipation
SOIC . . . . . .570mW
PDIP. . . . . .1050mW
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

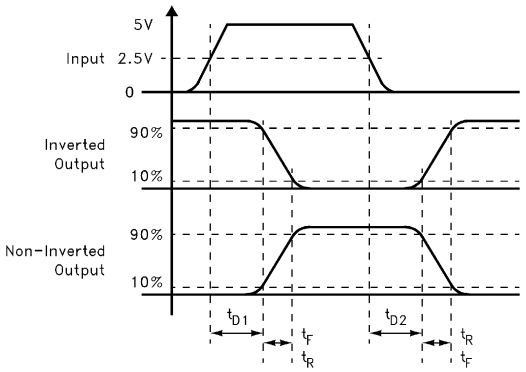
DC Electrical Specifications $T_A$ = +25°C, V = 15V unless otherwise specified.

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| $V_{IH}$ | Logic “1” Input Voltage | | 2.4 | | | V |
| $I_{IH}$ | Logic “1” Input Current | @V+ | | 0.1 | 10 | µA |
| $V_{IL}$ | Logic “0” Input Voltage | | | | 0.8 | V |
| $I_{IL}$ | Logic “0” Input Current | @0V | | 0.1 | 10 | µA |
| $V_{HVS}$ | Input Hysteresis | | | 0.3 | | V |
| **OUTPUT** | | | | | | |
| $R_{OH}$ | Pull-Up Resistance | $I_{OUT}$ = -100mA | | 3 | 6 | Ω |
| $R_{OL}$ | Pull-Down Resistance | $I_{OUT}$ = +100mA | | 4 | 6 | Ω |
| $I_{OFF}$ | 3-State Output Leakage | $V_{OUT}$ = V+<br>$V_{OUT}$ = 0V | 0.2 | | 10 | µA |
| $I_{PK}$ | Peak Output Current | Source<br>Sink | | 2.0<br>2.0 | | A |
| $I_{DC}$ | Continuous Output Current | Source/Sink | 100 | | | mA |
| **POWER SUPPLY** | | | | | | |
| $I_S$ | Power Supply Current | Inputs High | | 1 | 2.5 | mA |
| $V_S$ | Operating Voltage | | 4.5 | | 16 | V |

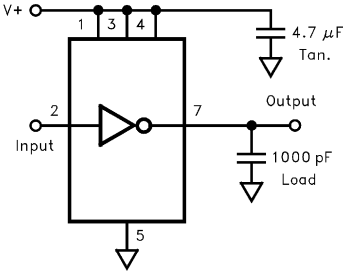
AC Electrical Specifications $T_A$ = +25°C, V = 15V unless otherwise specified.

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_R$ | Rise Time | $C_L$ = 500pF<br>$C_L$ = 1000pF | | 7.5<br>10 | | ns |
| $t_F$ | Fall Time | $C_L$ = 500pF<br>$C_L$ = 1000pF | | 10<br>13 | <br>20 | ns |
| $t_{D-ON}$ | Turn-On Delay Time | | | 18 | 25 | ns |
| $t_{D-OFF}$ | Turn-Off Delay Time | | | 20 | 25 | ns |
| $HIZ_{-ON}$ | Three-State Delay, Enable | | | 22 | | ns |
| $HIZ_{-OFF}$ | Three-State Delay, Disable | | | 22 | | ns |

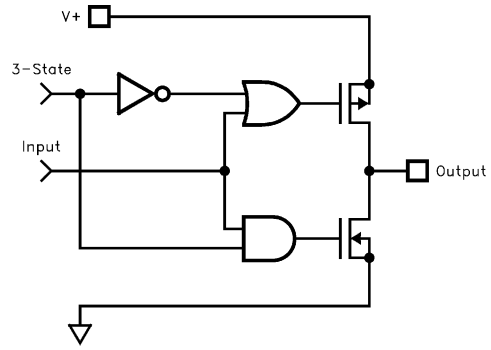
## Timing Table




## Standard Test Configuration




## Simplified Schematic




## Typical Performance Curves

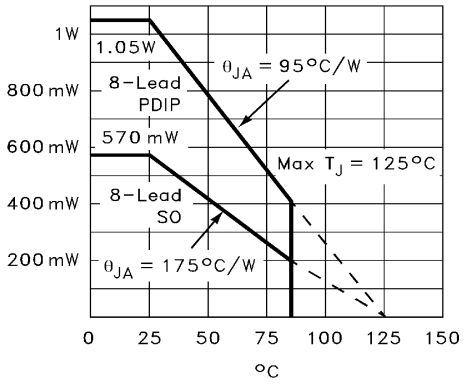



FIGURE 1. MAX POWER/DERATING CURVES

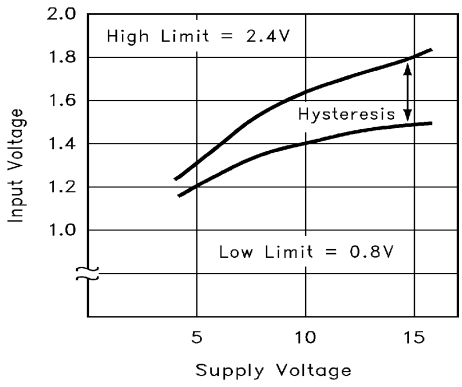



FIGURE 2. SWITCH THRESHOLD vs SUPPLY VOLTAGE

## *Typical Performance Curves* (Continued)

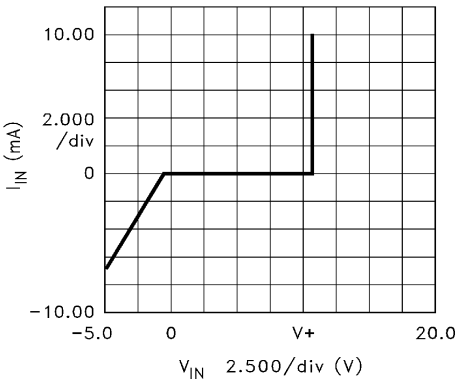



FIGURE 3. INPUT CURRENT vs VOLTAGE

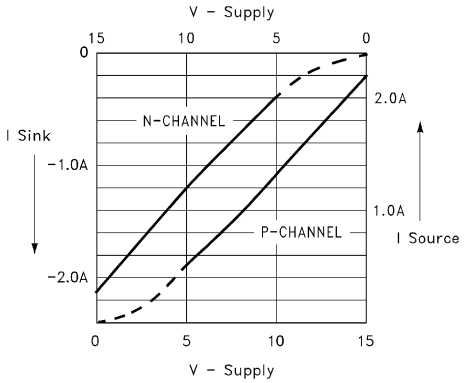



FIGURE 4. PEAK DRIVE vs SUPPLY VOLTAGE

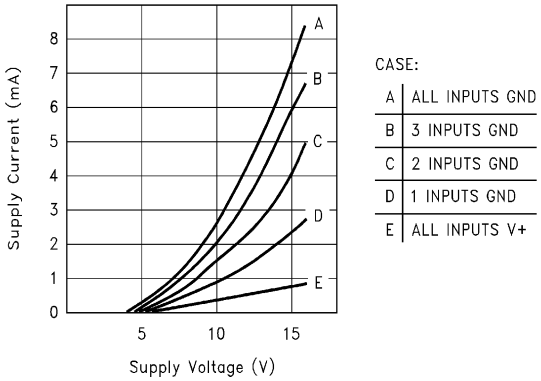



FIGURE 5. QUIESCENT SUPPLY CURRENT

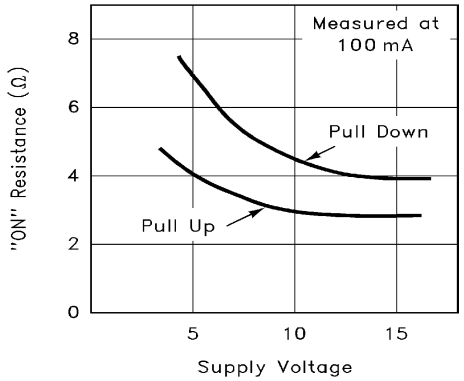



FIGURE 6. ON-RESISTANCE vs SUPPLY VOLTAGE

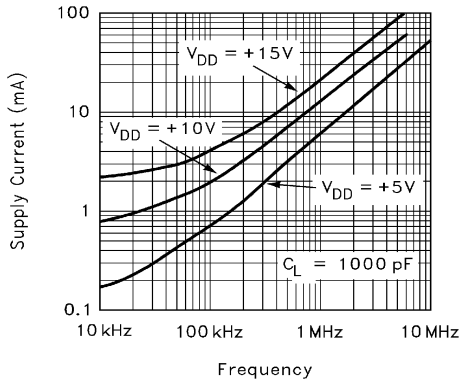



FIGURE 7. AVERAGE SUPPLY CURRENT vs VOLTAGE AND FREQUENCY

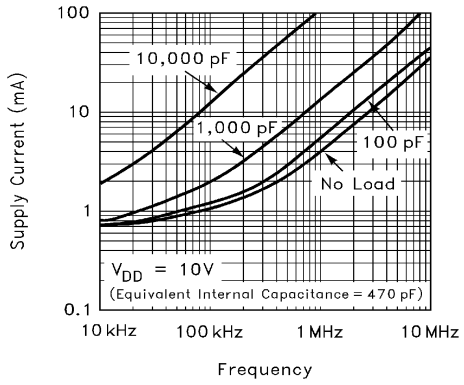



FIGURE 8. AVERAGE SUPPLY CURRENT vs CAPACITIVE LOAD

## *Typical Performance Curves* (Continued)

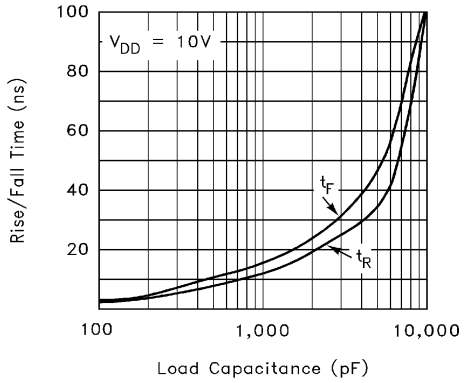



**FIGURE 9. RISE/FALL TIME vs LOAD**

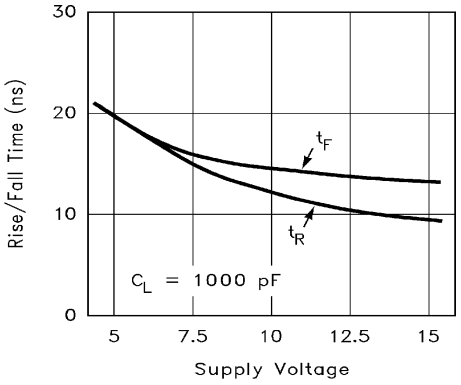



**FIGURE 10. RISE/FALL TIME vs SUPPLY VOLTAGE**

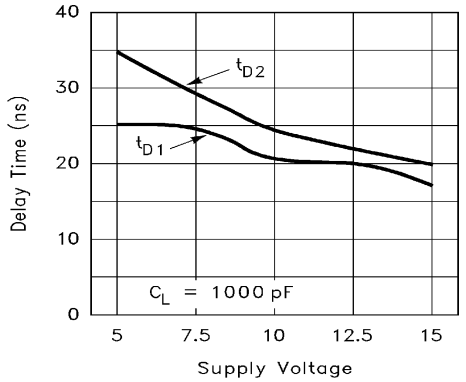



**FIGURE 11. PROPAGATION DELAY vs SUPPLY VOLTAGE**

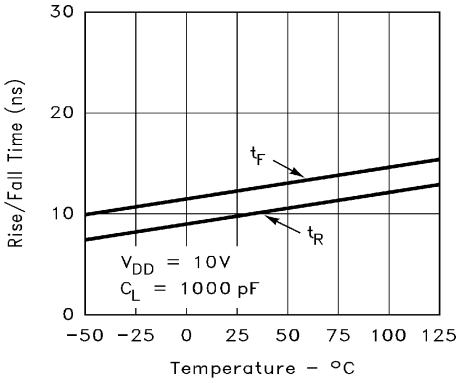



**FIGURE 12. RISE/FALL TIME vs TEMPERATURE**

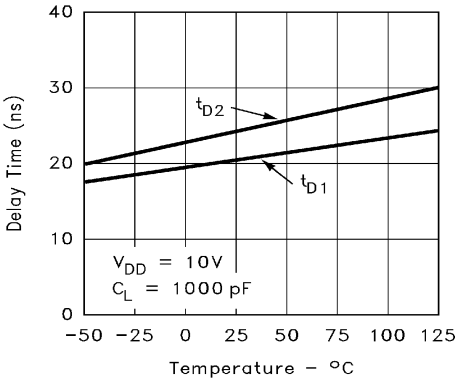



**FIGURE 13. PROPAGATION DELAY vs TEMPERATURE**

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| November 12, 2015 | FN7283.4 | Added Rev History and About Intersil Verbiage.<br>Updated Ordering Information on page 1<br>Updated POD MDP0031 to E8.3<br>Updated POD MDP0027 to M8.15E |

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

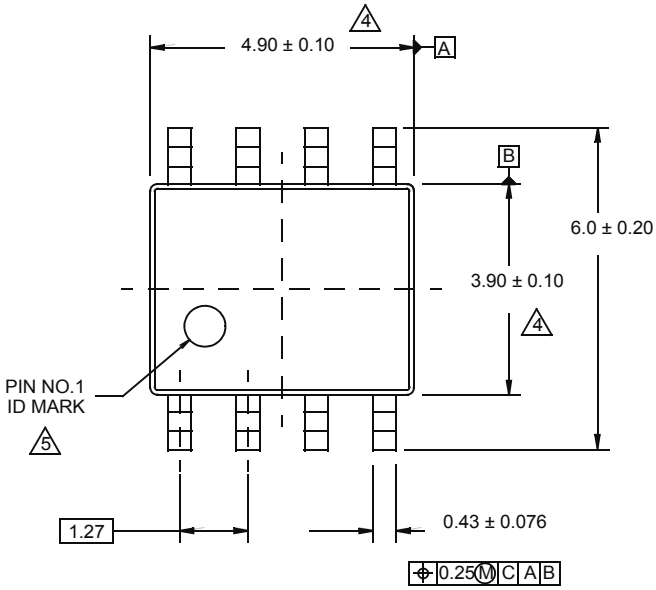
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

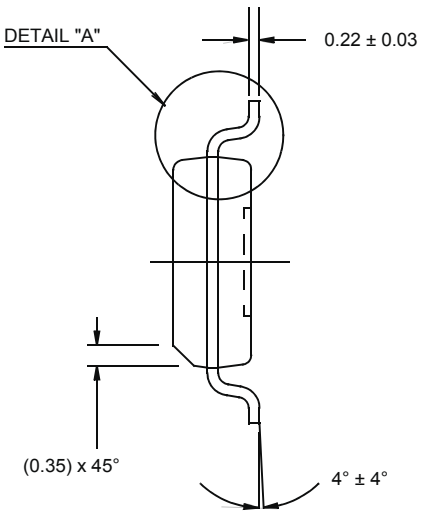
# Package Outline Drawing

## M8.15E

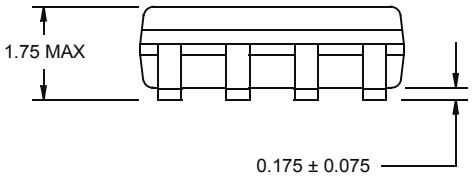
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**
**Rev 0, 08/09**



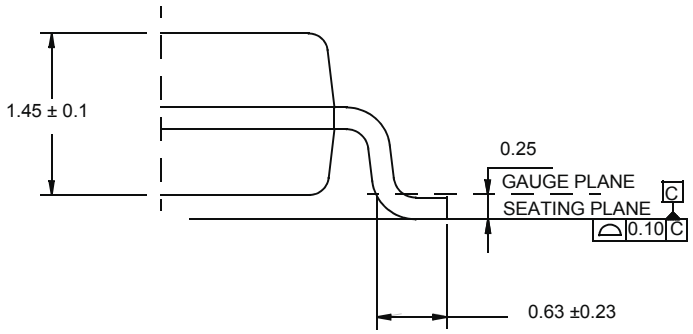

TOP VIEW



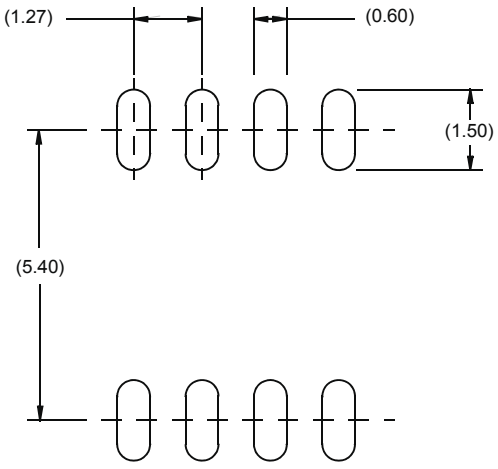

SIDE VIEW "B"




SIDE VIEW "A"




DETAIL "A"

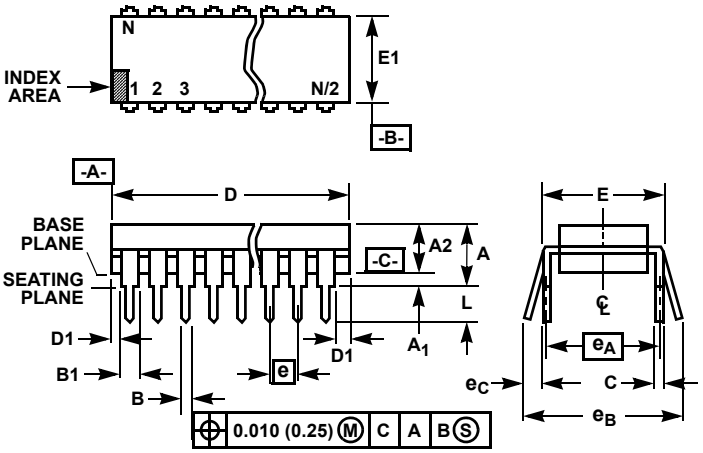



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

## *Dual-In-Line Plastic Packages (PDIP)*




**E8.3 (JEDEC MS-001-BA ISSUE D)**
**8 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8, 10 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.355 | 0.400 | 9.01 | 10.16 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| $e_A$ | 0.300 BSC | | 7.62 BSC | | 6 |
| $e_B$ | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 8 | | 8 | | 9 |

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $e_A$ are measured with the leads constrained to be perpendicular to datum -C-.
7. $e_B$ and $e_C$ are measured at the lead tips with the leads unconstrained. $e_C$ must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).