TQM879006A

1.4 – 2.7 GHz 1/4 W Digital Variable Amplifier

28 Pin 6X6 mm leadless SMT Package

General Description

The TQM879006A is a digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of a low noise amplifier gain block, a digital-step attenuator (DSA), along with a high linearity ¼W amplifier. The module has the added features of integrating all matching components with bias chokes and blocking capacitors. The internal DSA offers 0.5 dB step, 6-bit, and 31.5 dB range and is controlled with a serial periphery interface (SPI™).

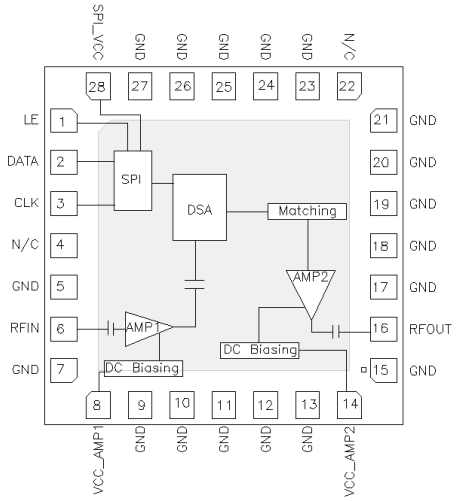
The TQM879006A features variable gain from 0 dB to 31.7 dB at 2 GHz, has +43 dBm Output IP3, and +24.5 dBm P1dB. The amplifier also has a very low 1.5 dB Noise Figure (at maximum gain) allowing it to be an ideal DVGA for both receiver and transmitter applications. The amplifier operates from a single +5V supply and is available in a compact 28-pin 6x6 mm leadless SMT package.

The TQM879006A is pin compatible with the TQM829007 (0.6-1GHz, 0.25W DVGA) and TQM879008 (1.5-2.7 GHz, 0.5W DVGA). This allows one to size the right type of device for specific system level requirements as well as making the DVGA family ideal for applications where a common PCB layout is used for different frequency bands.

Product Features

- 1.4-2.7 GHz Frequency Range
- 31.7 dB Maximum Gain at 2 GHz
- 31.5 dB Gain Range in 0.5 dB Steps
- +43 dBm Output IP3
- +24.5 dBm Output P1dB
- 1.5 dB Noise Figure at Max. Gain State
- Fully Internally Matched Module
- Integrated Blocking Capacitors, Bias Inductors
- 3-wire SPI Control Programming

Functional Block Diagram



Top View

Applications

- 3G / 4G Wireless Infrastructure
- CDMA, TD-CDMA, WCDMA, LTE
- Repeaters
- PTP Radio IF Chains

Ordering Information

Part No.	Description
TQM879006ATR13*	1.4−2.7 GHz Digital Variable Gain Amp
TQM879006A-PCB	Fully Assembled Evaluation Board Includes USB control board (EVH)

*Standard T/R size = 2500 pieces on a 13” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
RF Input Power,CW, 50Ω,T = 25°C	+23 dBm
Vcc (pins 8, 14, 28)	+5.5 V
Digital Input Voltage	V_{cc}+ 0.5V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Case Temperature	-40		+85	°C
Tj for >10^6 hours MTTF			+170	°C

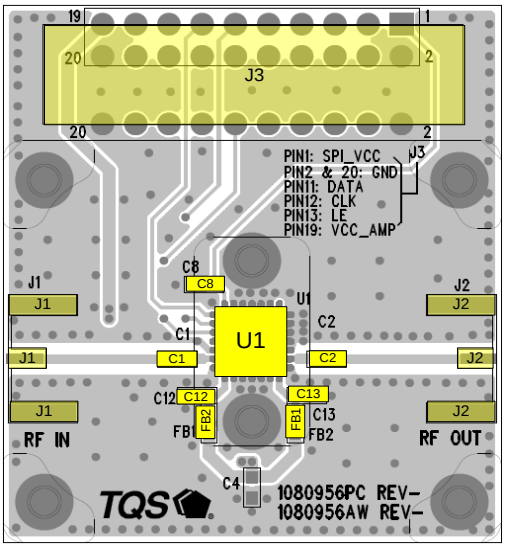
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

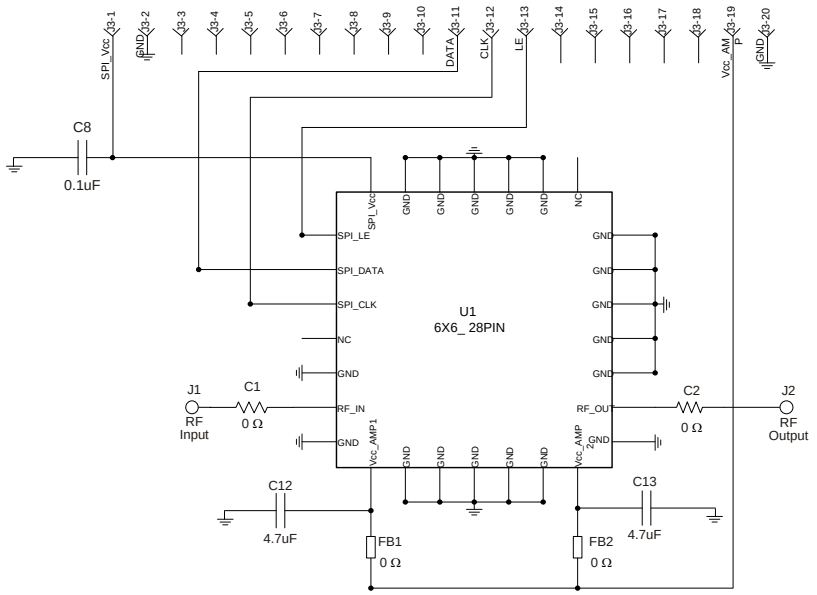
Electrical Specifications

Test conditions unless otherwise noted: V_{DD} =+5V, Temp=+25°C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1400		2700	MHz
Test Frequency			2000		MHz
Gain		27.5	31.7	34	dB
Gain Control Range	0.5 dB Step Size		31.5		dB
Attenuation Accuracy	3 wire SPI, Major State	±(0.3+5% of Attenuation setting) Max			dB
Control Interface	3-wire SPI		6		Bit
Input Return Loss			21		dB
Output Return Loss			20		dB
Output P1dB			+24.5		dBm
Output IP3	Pout=+11 dBm/tone, Δf=1 MHz	+38	+43.0		dBm
Noise Figure			1.5		dB
I/O Impedance			50		Ohm
Supply Voltage			+5		V
Supply Current			174	215	mA
Thermal Resistance, θ_{jc}	Module (junction to case)			36.7	°C/W

Application Circuit (TQM879006A-PCB)





Notes:

1. For PCB Board Layout, see page 9 for more information.
2. All Components are of 0603 size unless stated otherwise.
3. For SPI Timing Diagram, see page 6.
4. 0 Ω jumpers may be replaced with copper traces in the target application layout.
5. Different ground pins are used for SPI (digital) and analog supply voltages.
6. The primary RF microstrip characteristic line impedance is 50 Ω.
7. The single power supply is used to provide supply voltage to AMP1 and AMP2.

Bill of Material – TQM879006A-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	1.5-2.7 GHz ¼ W DVGA	Qorvo	TQM879006A
C8	0.1 uF	Cap, Chip, 0603, 16V, X7R, 10%	various	
C12, C13	4.7 uF	Cap, Chip, 0603, 6.3V, X5R, 20%	various	
C1, C2, FB1, FB2	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	
C4	DNP			

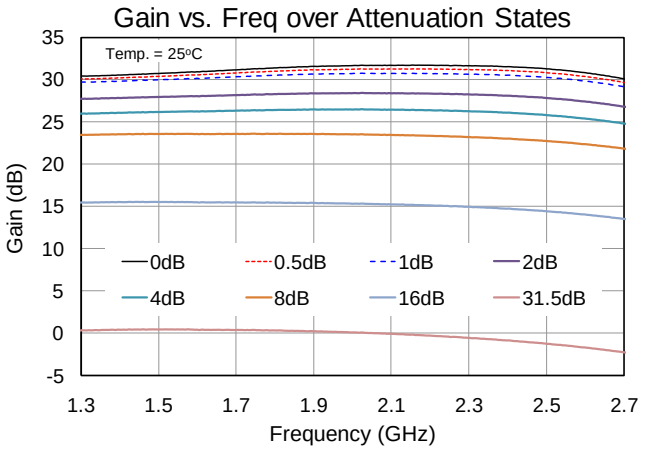
Typical Performance, Maximum Gain State

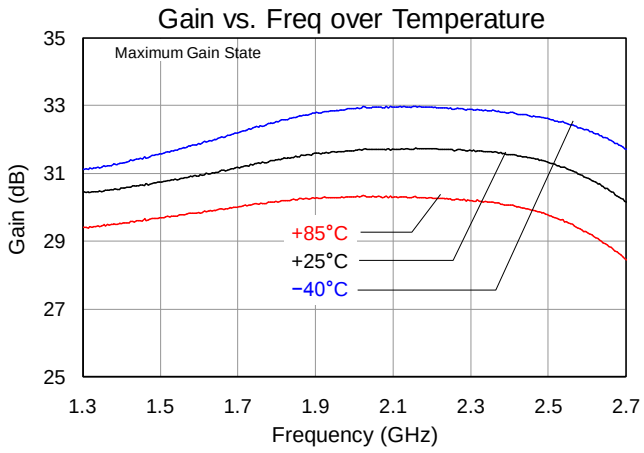
Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CC}=174 mA (typ), Temp=+25°C

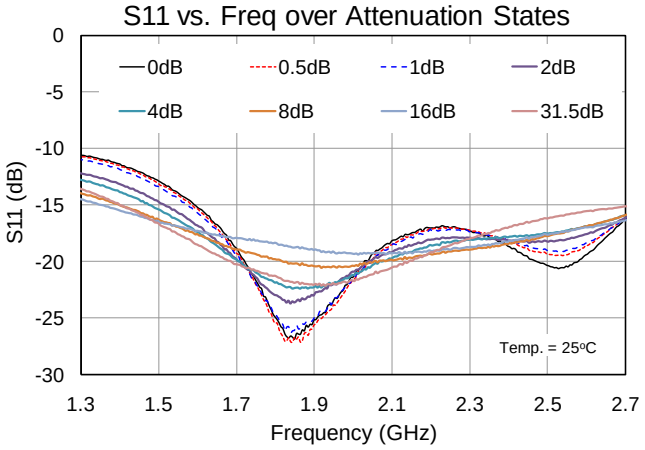
Parameter	Typical Value						Units
Frequency	1500	1800	2000	2140	2350	2600	MHz
Gain	30.8	31.4	31.7	31.7	31.6	30.8	dB
Input Return Loss	13	25	21	17	18	19	dB
Output Return Loss	10	15	20	19.5	15	11	dB
Output P1dB	+24.1	+24.5	+24.5	+24.5	+24.4	+24.3	dBm
Output IP3 (11 dBm/tone, Δf = 1 MHz)	+40.2	+42.0	+43.0	+43.0	+41.0	+40.5	dBm
Noise Figure	1.35	1.4	1.5	1.5	1.6	1.8	dB

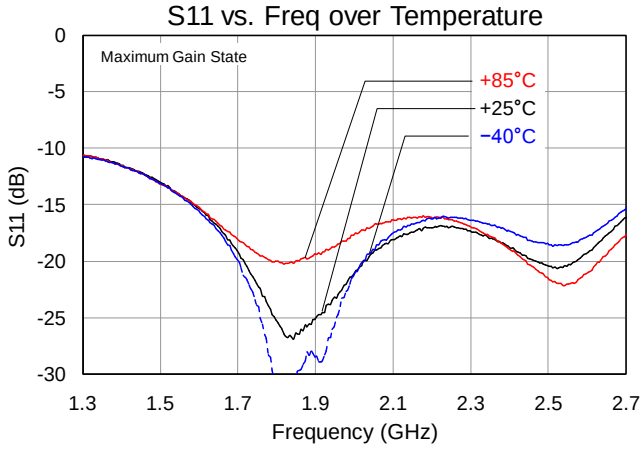
Notes:
1. The evaluation board can be used with Qorvo's USB interface board. Refer to Qorvo's website for more information.

Typical Performance Plots

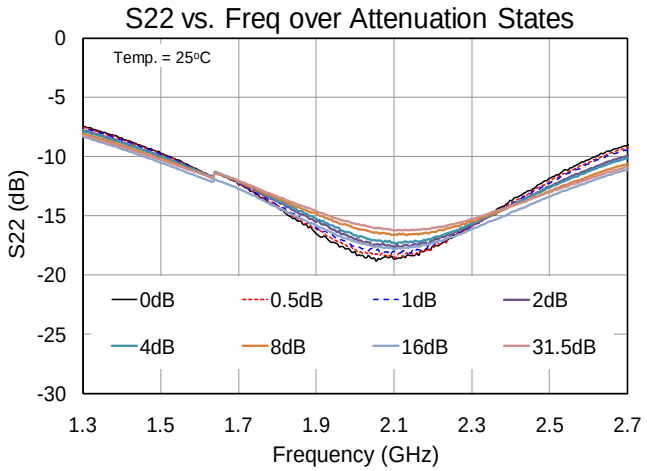


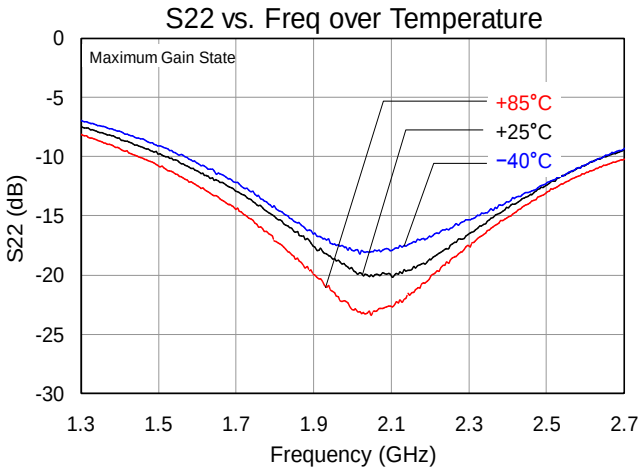


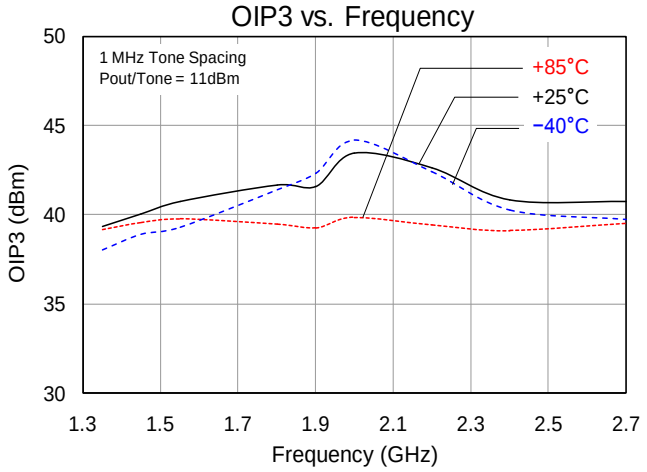


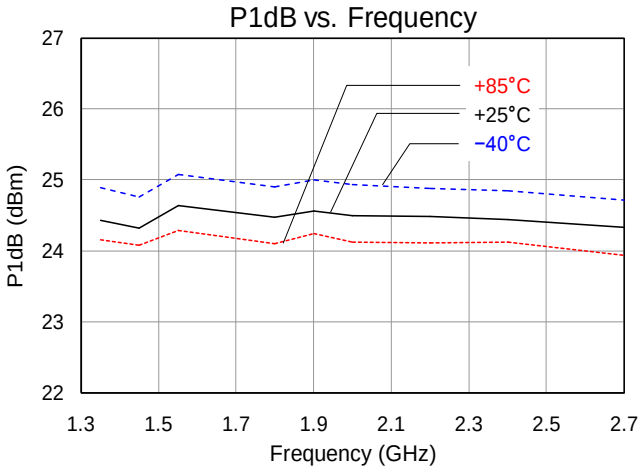


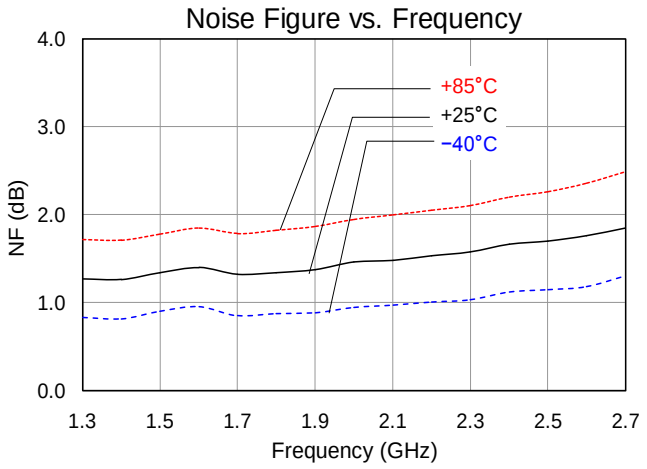
Typical Performance Plots

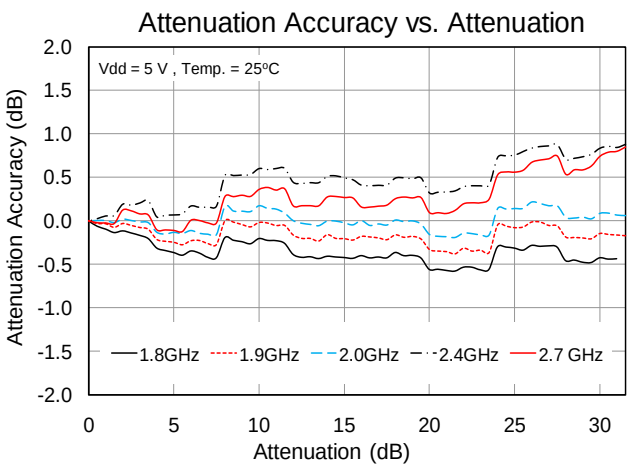












Serial Control Interface

Serial Control Timing Characteristics (Test conditions: V_{CC} = +5 V, T_{LEAD}=25°C)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
DATA set-up time, t_{SDSUP}	before CLK rising edge	10		ns
DATA hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing t_{LE}	LE to LE pulse spacing	630		ns
Propagation Delay t_{PLO}	LE to Parallel output valid		30	ns

Serial Control DC Logic Characteristics (Test conditions: V_{CC} = +5 V, T_{LEAD}=25°C)

Parameter	Condition	Min	Max	Units
Input Low Voltage, V_{IL}		0	0.8	V
Input High Voltage, V_{IH}		2.4	Vcc	V
Input Current, I_{IH} / I_{IL}	On DATA, LE and CLK	-10	+10	µA

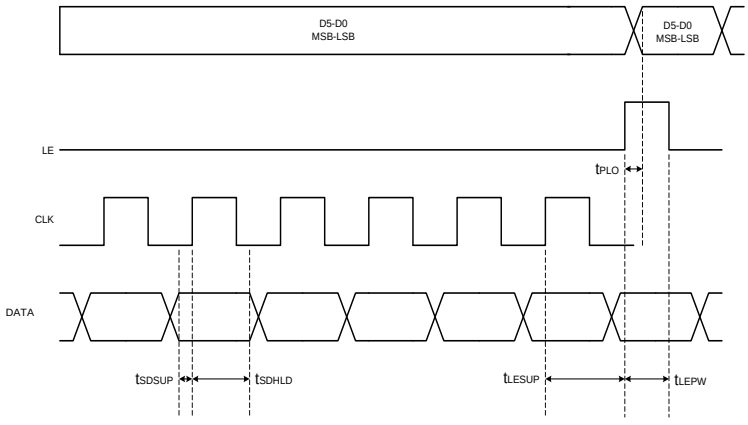
DATA (MSB in First 6-Bit Word) Control Logic Truth Table

MSB	6-Bit Control Word to DSA				LSB	Gain Relative to Maximum Gain
D5	D4	D3	D2	D1	D0	Reference : IL
1	1	1	1	1	1	0 dB
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB

Any combination of the possible 64 states will provide a reduction in gain of approximately the sum of the bits selected.

Serial Control Interface Timing Diagram

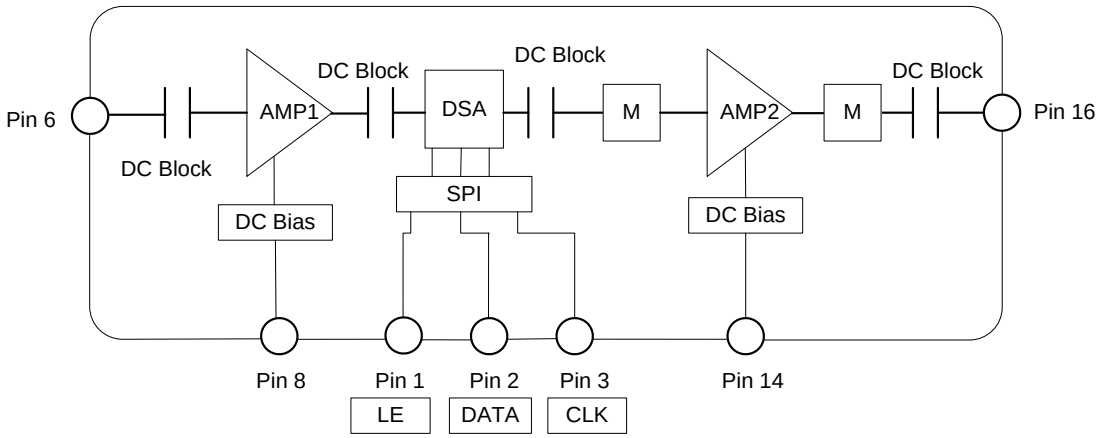
CLK is disabled when LE is high



Detailed Device Description

The TQM879006A is a 50 Ω internally matched digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of a low noise amplifier gain block, a digital step attenuator (DSA), along with a high linearity ¼W amplifier as shown in the functional diagram below. The module is unconditionally stable. Internal blocking capacitors and bias structures keep external parts count to a minimum. The DVGA has an operational frequency range from 1.4 - 2.7 GHz.

Functional Schematic Diagram



Where M = Matching Network.

Chain Analysis Table

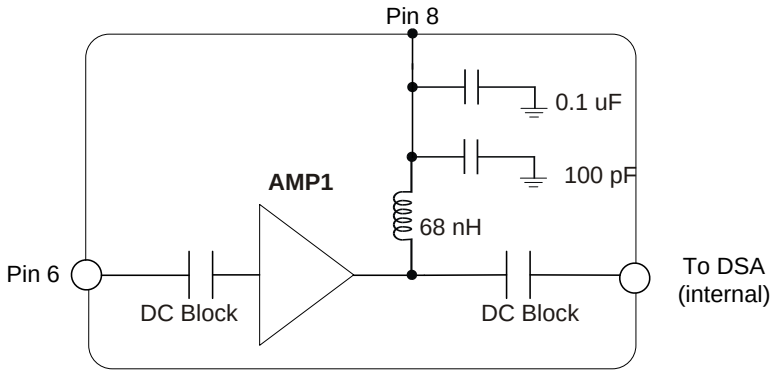
This table provides the typical performance of individual stages in the module as well as overall module performance.

Parameter	AMP1	DSA	AMP2	Overall Module	Units
Gain	19	-1.8	14.5	31.7	dB
NF	1.3	1.8	4.0	1.5	dB
OIP3	36	55	43	43	dBm
P1dB	20	28.5	24.5	24.5	dBm
Icc	85	2.0	87	174	mA

Device Detailed Description

AMP1

AMP1 is a wide band low noise amplifier gain block in DVGA module. The amplifier provides 19 dB gain, 1.3 dB noise figure, +36 dBm OIP3 at 2.0 GHz while only drawing 85 mA current. External DC blocks and biasing is not required. AMP1 is DC blocked internally and is connected internally to three bypass capacitors (22 pF, 100 pF, 0.01 uF) followed by 22 nH inductor inside the module as shown in the figure below.

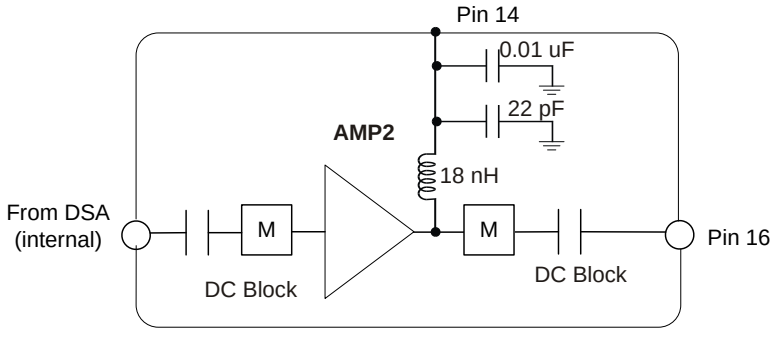


DSA (Digital Step Attenuator)

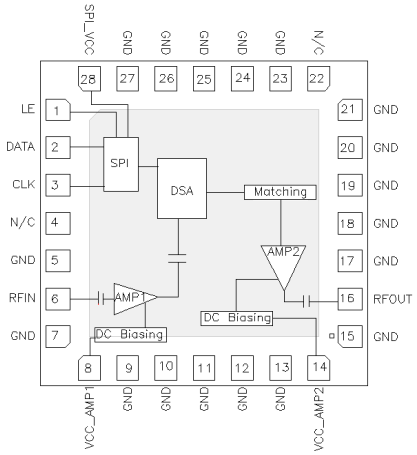
DVGA has a serial digital step attenuator that is controlled with 6-bit serial periphery interface (SPI™) and has 0.5 dB step size with 31.5 dB attenuation range. This 50-ohm RF DSA maintains high attenuation accuracy over frequency and temperature. "000000" represents maximum attenuation state. External bypass capacitors are needed to compensate the inductance effect associated with long transmission lines on the evaluation board.

AMP2

AMP2 is high linearity ¼-W amplifier in DVGA module. The amplifier provides 14.4 dB gain, +24.5 dBm P1dB, +43 dBm OIP3 at 2.0 GHz while only drawing 87 mA current. The amplifier is optimized over 1.4 – 2.7 GHz bandwidth using internal matching components. AMP2 is DC blocked internally and is connected internally to two bypass capacitors (22 pF, 0.01 uF) followed by an 18 nH inductor inside the module as shown in the figure below. External DC blocks and biasing is not required.



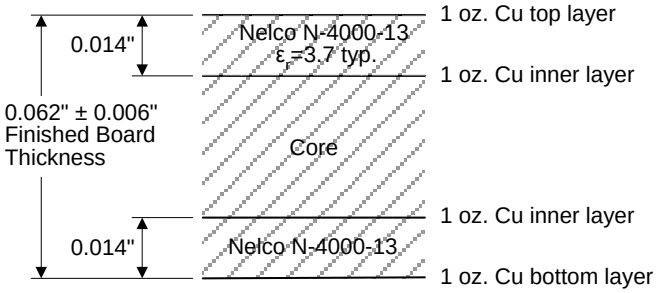
Pin Configuration and Description



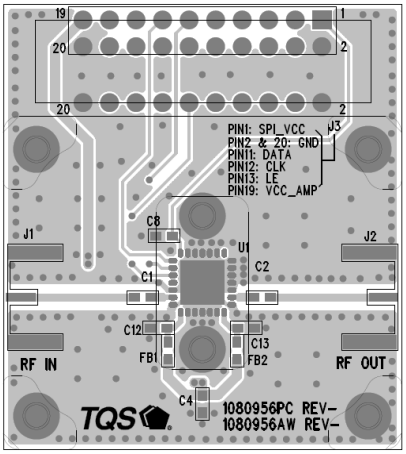
Pin No.	Symbol	Description
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial data input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial clock input.
4, 22	N/C	No internal connection. connect or open. This pin is not connected in this module
6	RFIN	Input, matched to 50 ohms between 1800 and 2700 MHz. Internally DC blocked.
8	VCC_AMP1	Supply Voltage to AMP1. This pin is connected internally to 3 bypass capacitors (22pF, 100 pF, 0.01uF) followed by a 22 nH inductor inside the module.
14	VCC_AMP2	Supply Voltage to AMP2. This pin is connected internally to 2 bypass capacitors (22pF, 0.01uF) followed by an 18 nH inductor inside the module.
16	RFOUT	Output, matched to 50 ohms between 1800 and 2700 MHz. Internally DC blocked.
28	VCC_SPI	Supply voltage for SPI and DSA chip. This pin is connected to 0.1uF bypass capacitor internally.
All other Pins	GND	RF/DC Ground Connection

Evaluation Board PCB Information

Qorvo PCB 1080956 Material and Stack-up

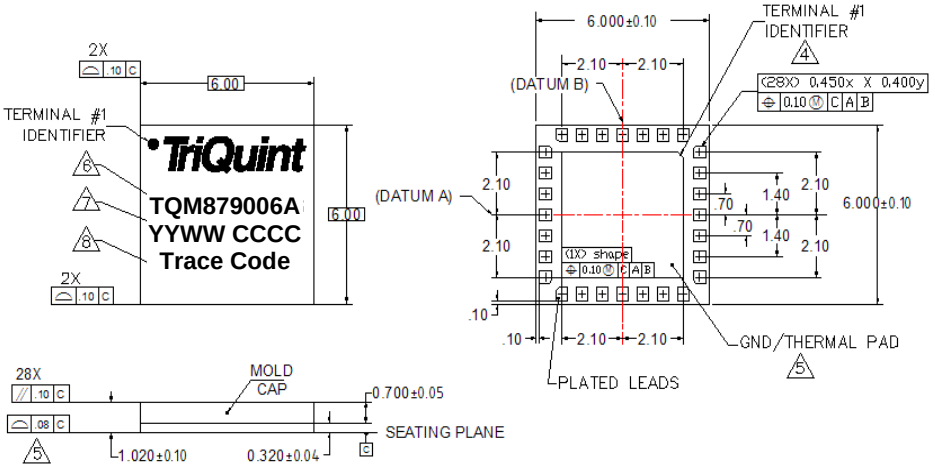


50 ohm line dimensions: width = .030”, spacing = .036”



Package Marking and Dimensions

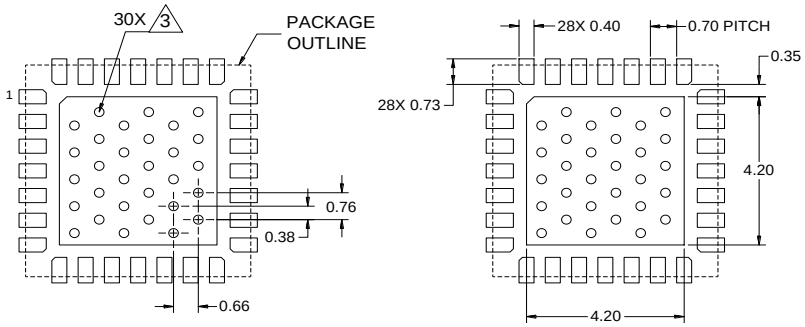
Marking: Part number – TQM879006A
Lot Code – YYWW CCCC
Trace Code – Up to 6 characters



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	Class C3	ESDA / JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.
Solder profiles available upon request.

Contact plating: Electrolytic Plated Au over Ni

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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