



QPB9324

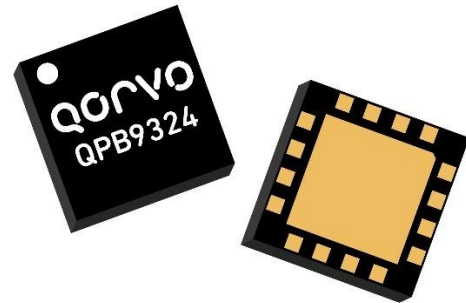
High Power Switch LNA Module

Product Overview

The Qorvo® QPB9324 is a highly integrated front-end module targeted for TDD macro or picocell base stations. The LNA switch module integrates RF functional blocks such as a pin-diode based high power switch capable of handling up to 52 W with an LTE signal (8 dB PAR) along with two LNA stages. Further integration is also implemented where the pin diode driver and dc-dc converter circuits are implemented inside the module to enable only the need for an external 5 V power supply. The control voltage for the switch and gain control. mode is with 3.3 V logic.

The QPB9324 can be utilized across the 3.4-3.6 GHz range to provide 1.2 dB noise figure for operation in the receive mode and 0.5 dB insertion loss in the transmit mode. The LNAs utilize Qorvo's high performance E-pHEMT process while the switch allows for power levels up to 330 W peak power to be routed to an external load termination.

The QPB9324 is packaged in a RoHS-compliant, compact 8x8 mm surface-mount leadless package. The switch LNA module is targeted for wireless infrastructure applications configured for TDD-based architectures.

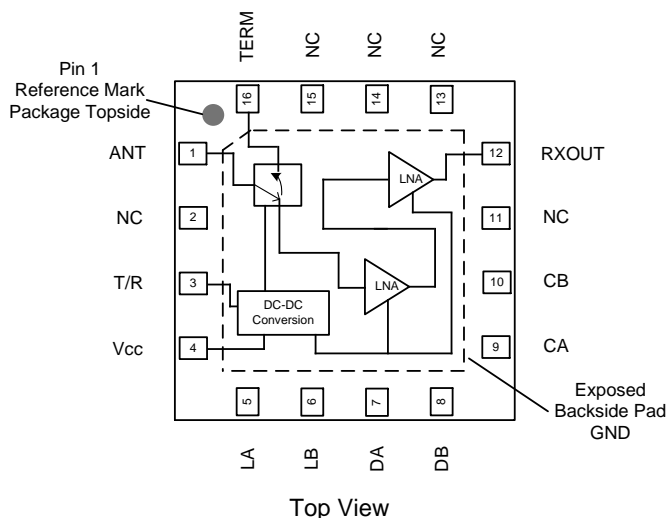


16 Pin 8 mm x 8 mm leadless SMT Package

Key Features

- 3.4-3.6 GHz frequency range
- Integrates a high-power switch, two LNA stages, pin diode driver circuits, and dc converter
- Ideal for TDD systems with an isolator
- Only requires a 5 V supply with 3.3 V logic control
- Max RF Input power: 52 W Pavg (8 dB PAR)
- 33.8 dB gain
- 1.2 dB noise figure
- -0.6 dBm IIP3 (Rx mode)
- 0.5 dB Insertion Loss (Tx mode)
- Compact package size, 8x8 mm

Functional Block Diagram



Applications

- Wireless Infrastructure
- Macro or picocell base stations
- TDD-based architectures

Ordering Information

Part No.	Description
QPB9324TR13	2500 pcs on a 13" reel
QPB9324EVB	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-50 to 150 °C
Operating Temperature	+115 °C
V _{CC}	+6 V
RF at ANT (Tx Mode), 10sec. ⁽¹⁾	+47.2 dBm
RF at ANT (Tx Mode), Indefinitely ⁽¹⁾	+44.2 dBm
RF at ANT (Rx Mode), Indefinitely ⁽¹⁾	+20 dBm
RF at ANT (Rx Mode), WCDMA PAR=10dB ⁽²⁾	+26 dBm
RF at ANT (Rx Mode), CW ⁽²⁾	+29 dBm
RF at ANT (Rx Mode), 1 μs pulse 1% duty cycle ⁽³⁾	+31.5 dBm

Notes:

1. LTE 1ch, 8 dB PAR, 88% duty cycle, 10.4 μs repetition time, T_{CASE} = +100 °C
2. 12 hours, T_{CASE} = +25 °C
3. 2 hour x 2 cycles, T_{CASE} = +60 °C & then 2 hour x 3 cycles, T_{CASE} = +75 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{CC}	+4.75	+5	+5.25	V
T/R Logic Low Voltage	0		0.8	V
T/R Logic High Voltage	2.0		3.6	V
T _{CASE}	-40		+105	°C
T _j for >10 ⁶ hours MTTF ⁽¹⁾			+190	°C

Notes:

1. For RX Mode operation

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

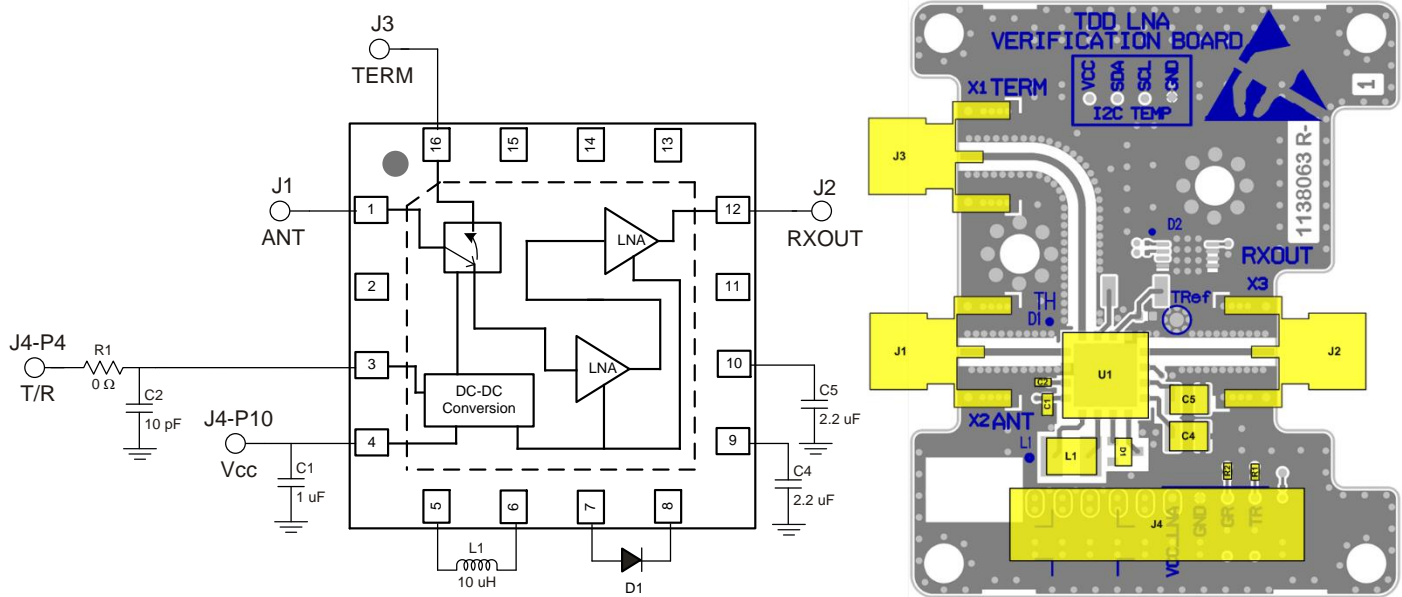
Test conditions unless otherwise noted: V_{CC} = +5.0 V, Temp. = +25 °C, 50 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		3400		3600	MHz
Gain	Rx mode		33.8		dB
Gain Flatness	Rx mode		0.5		dB
Noise Figure	Rx mode		1.2		dB
Input IP3	Rx mode, Pin/tone = -33dBm, Δf = 1MHz		-0.6		dBm
Input P1dB	Rx mode		-15.4		dBm
Input Return Loss (ANT)	Rx mode		26		dB
Output Return Loss (Rx Out)	Rx mode		23		dB
Reverse Isolation	Rx mode		58		dB
Insertion Loss	Tx mode		0.5		dB
Input P0.1dB	Tx mode		46.6		dBm
Return Loss (ANT, TERM)	Tx mode		27		dB
Operating Current	Rx mode		240		mA
Operating Current	Tx mode		145		mA
Switching Time (ANT to Rx Out)	Reaching RF full output less 0.1dB after T/R command		2		μs
Switching Time (ANT to Term)			1		μs
Wakeup Time (ANT to Rx Out/Term)	Reaching RF full output less 0.5dB after DC turn on		1		sec.
In Band Spurious Emission ⁽¹⁾	Rx Mode at Rx out with Pin = -49dBm ⁽²⁾		-85		dBc
Out of Band Emissions ⁽³⁾	Rx Mode at Rx out from DC to 12275MHz		-65		dBm
Thermal Resistance	Rx mode		22		°C/W
Thermal Resistance	Tx mode		22		°C/W

Notes:

1. Pin is a CW signal swept from 3.4 to 3.6GHz. Specification refers to any mixing product that occurs in 3.4 to 3.6GHz band.
2. Follow Qorvo EVB layout for lowest spur level, any deviation may increase spur level.
3. Measure Pout with IBW = 4.5MHz over frequency range with no input power applied.

Application Circuit Schematic and Layout



Note:
L1 placement for in band spur suppression - 5mm from bottom edge of U1 to top edge of L1

Bill of Material

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	High Power Switch LNA Module	Qorvo	QPB9324
R1, R2	0 Ω	Resistor, Chip, 0402, 5%	Various	
C1	1 μF	Capacitor, Chip, 0603, 20%, X7R	Various	
C2	10 pF	Capacitor, Chip, 0402, NPO/COG, 5%	Various	
C4, C5	2.2 μF	Capacitor, Chip, 1210, 100 V, 10%, X7R	Various	
D1	n/a	Diode, 200 V 200 mA SOT23	Various	
L1	10 μH	Inductor, Power, 10 μH , 20%, 0.84 A	Coilcraft	LPS4018-103ML

Logic Table

Parameter	High	Low
T/R Switch Control	Rx Mode	Tx Mode

Typical Performance – Rx Mode

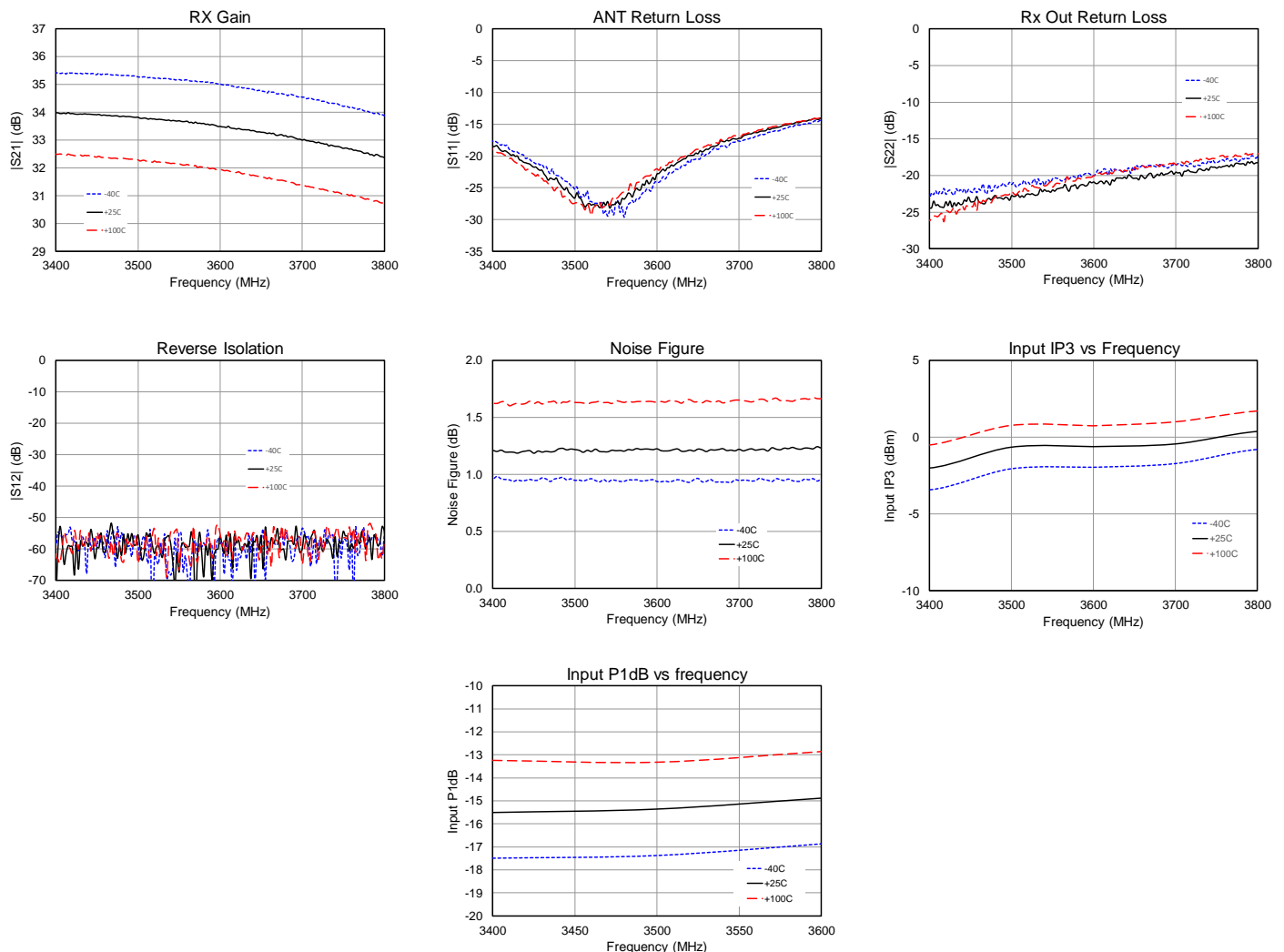
Parameter	Conditions ⁽¹⁾	Typical Value			Units
Frequency		3400	3500	3600	MHz
Gain		34.0	33.8	33.5	dB
Input IP3	Pin = -33 dBm/tone, $\Delta f = 1$ MHz	-2.0	-0.6	-0.6	dBm
Input P1dB		-15.5	-15.4	-14.9	dBm
Noise Figure	De-embedded from Evaluation board PCB	1.2	1.2	1.2	dB
Return Loss	ANT port	18	26	24	dB
Return Loss	Rx Out port	24	23	21	dB
Reverse Isolation	Rx Out to ANT port	58	58	58	dB

Notes:

1. Test conditions unless otherwise noted: $V_{CC} = +5.0$ V, $T/R = 3$ V, Temp. = +25 °C

Performance Plots – Rx Mode

Test conditions unless otherwise noted: $V_{CC} = +5.0$ V, $T/R = 3$ V; Temp. = +25 °C



Typical Performance – Tx Mode

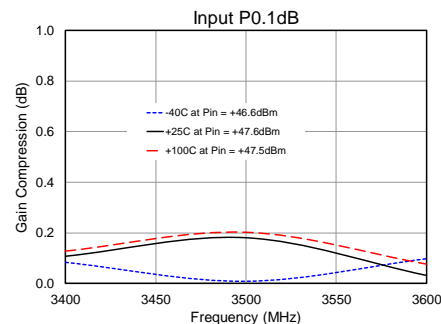
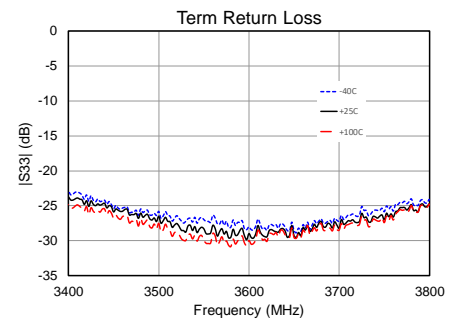
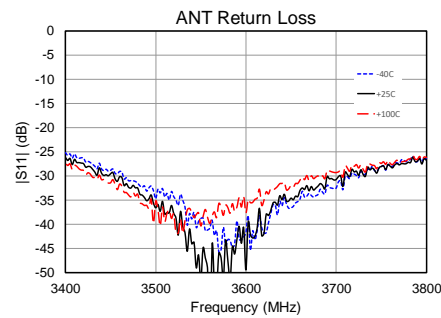
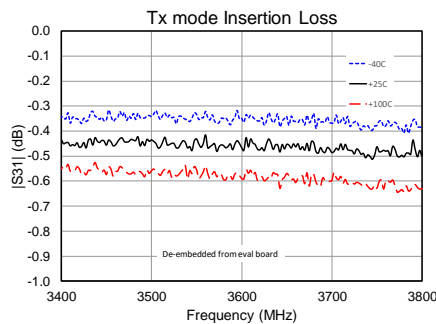
Parameter	Conditions ⁽¹⁾	Typical Value			Units
Frequency		3400	3500	3600	MHz
Insertion Loss	De-embedded from Evaluation board PCB	0.5	0.5	0.5	dB
Input Compression	Pin = +47.6 dBm	0.1	0.2	0.1	dB
Return Loss	ANT port	26	35	40	dB
Return Loss	TERM port	25	27	29	dB

Notes:

1. Test conditions unless otherwise noted: $V_{CC} = +5.0$ V, T/R = 0 V, Temp. = +25 °C

Performance Plots – Tx Mode

Test conditions unless otherwise noted: $V_{CC} = +5.0$ V, T/R = 0 V; Temp. = +25 °C

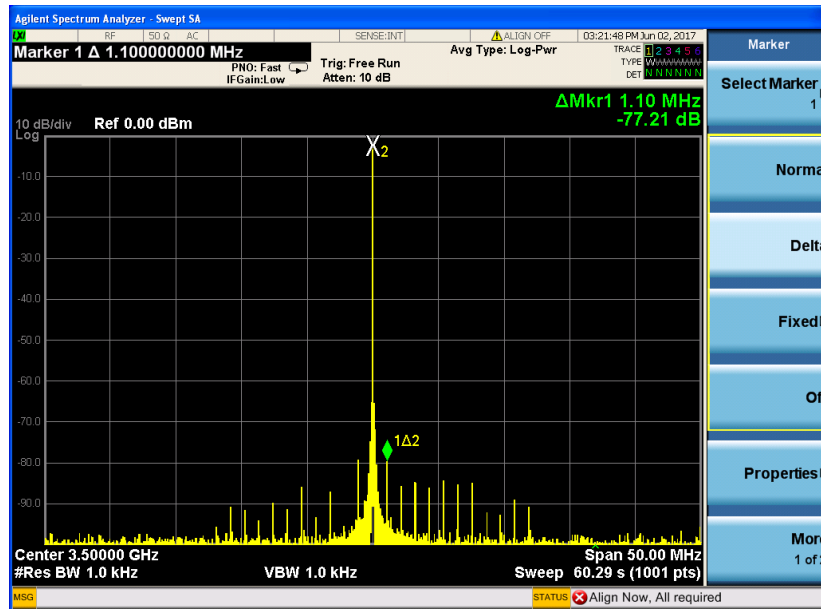


Application Circuit for Spurious Reduction

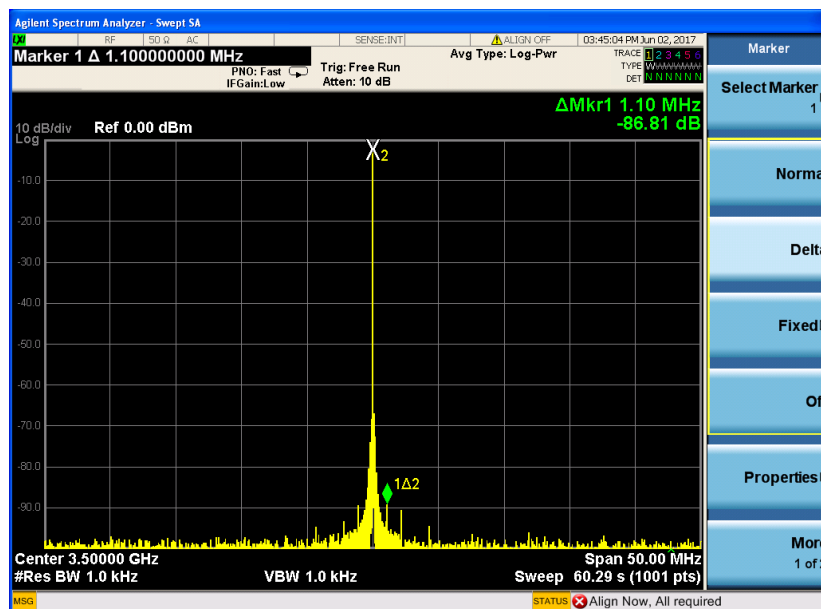
This section describes an alternative way to route the DC-DC converter signals for further improvement of in-band spurious emissions.

Spurious (Mixing Products) Plots – Rx Mode

Test conditions unless otherwise noted: $V_{CC} = +5.0$ V, $T/R = +3.0$ V, RF input at ANT = -35dBm CW; Temp. = +25 °C

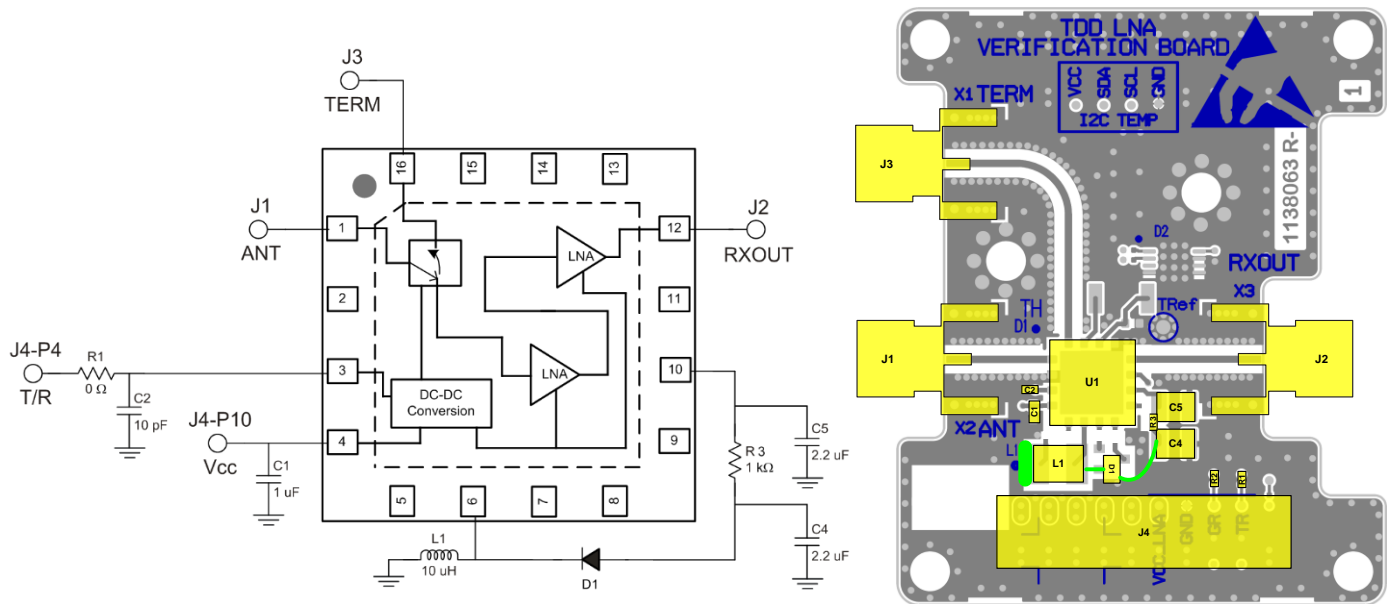


With Original EVB



With Modified Circuits and PCB

Application Circuit Schematic and Layout – Modified EVB



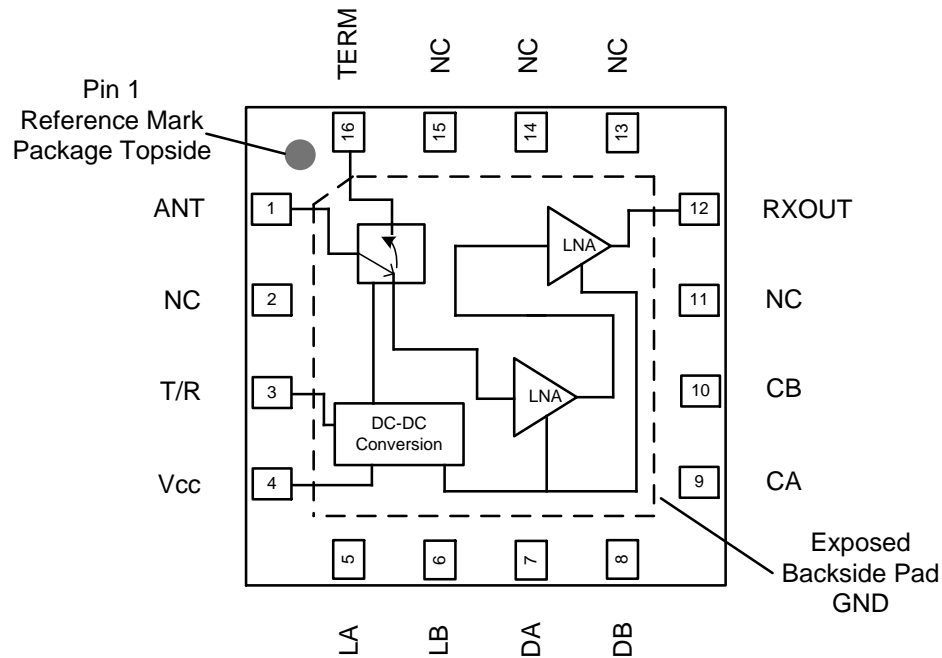
Note:

R3 is the additional component along with PCB trace modifications. All other parts are same as the Evaluation Board on page 3.

Bill of Material – Modified Circuits and PCB

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	High Power Switch LNA Module	Qorvo	QPB9324
R1, R2	0 Ω	Resistor, Chip, 0402, 5%	Various	
C1	1 μF	Capacitor, Chip, 0603, 20%, X7R	Various	
C2	10 pF	Capacitor, Chip, 0402, NPO/COG, 5%	Various	
C4, C5	2.2 μF	Capacitor, Chip, 1210, 100 V, 10%, X7R	Various	
D1	n/a	Diode 200 V 200 mA SOT23	Various	
L1	10 μH	Inductor, Power, 10 μH, 20%, 0.84 A	Coilcraft	LPS4018-103ML
R3	1 kΩ	Resistor, Chip, 0402, 5%	Various	

Pin Configuration and Description



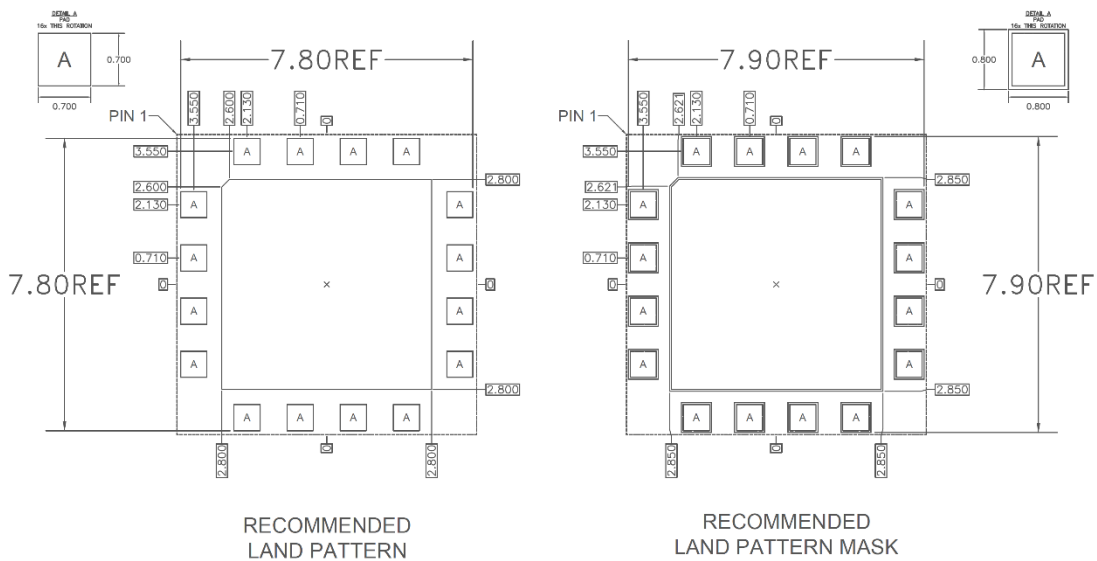
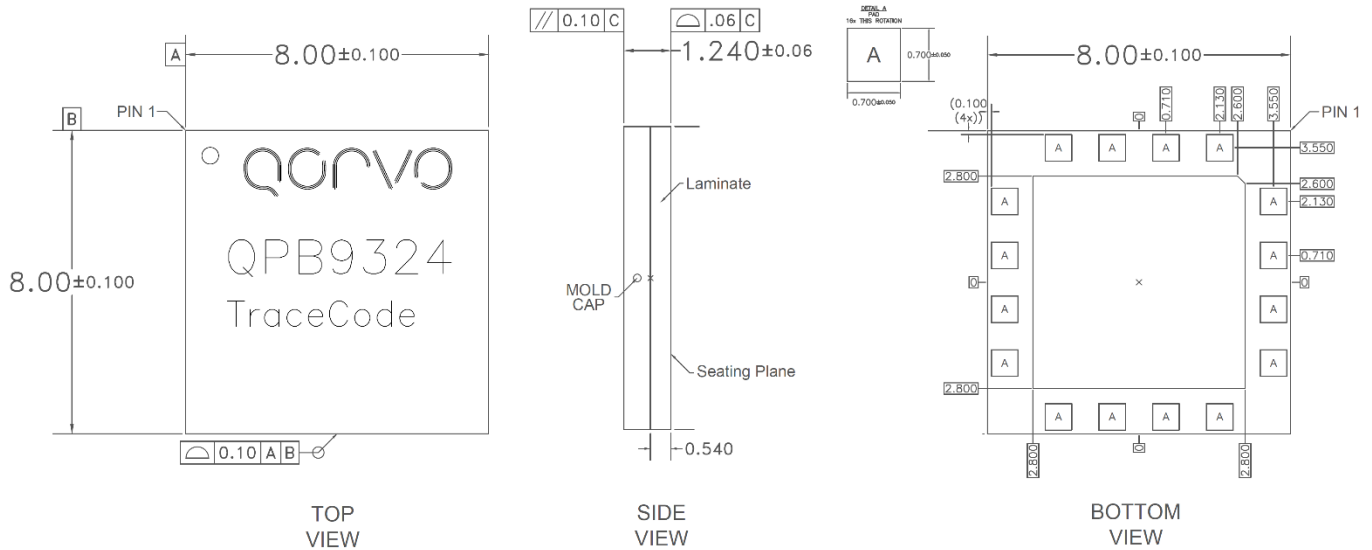
Top View

Pin No.	Label	Description
1	ANT	RF antenna input/output port, 50 Ω
2, 11, 13, 14, 15	NC	No Internal Connection.
3	T/R	Switch Control input, Tx mode Low state, Rx mode High state.
4	V _{CC}	DC Power Supply Voltage input.
5	LA	External inductor connection for DC-DC convertor.
6	LB	External inductor connection for DC-DC convertor.
7	DA	External diode anode connection for DC-DC convertor.
8	DB	External diode cathode connection for DC-DC convertor.
9	CA	External filtering capacitor connection for DC-DC convertor.
10	CB	External filtering capacitor connection for DC-DC convertor.
12	Rx OUT	RF LNA output port, 50 Ω
16	TERM	RF termination port, 50 Ω
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB via holes under the device are required.

Package Marking and Dimensions

Marking: Part number – QPB9324

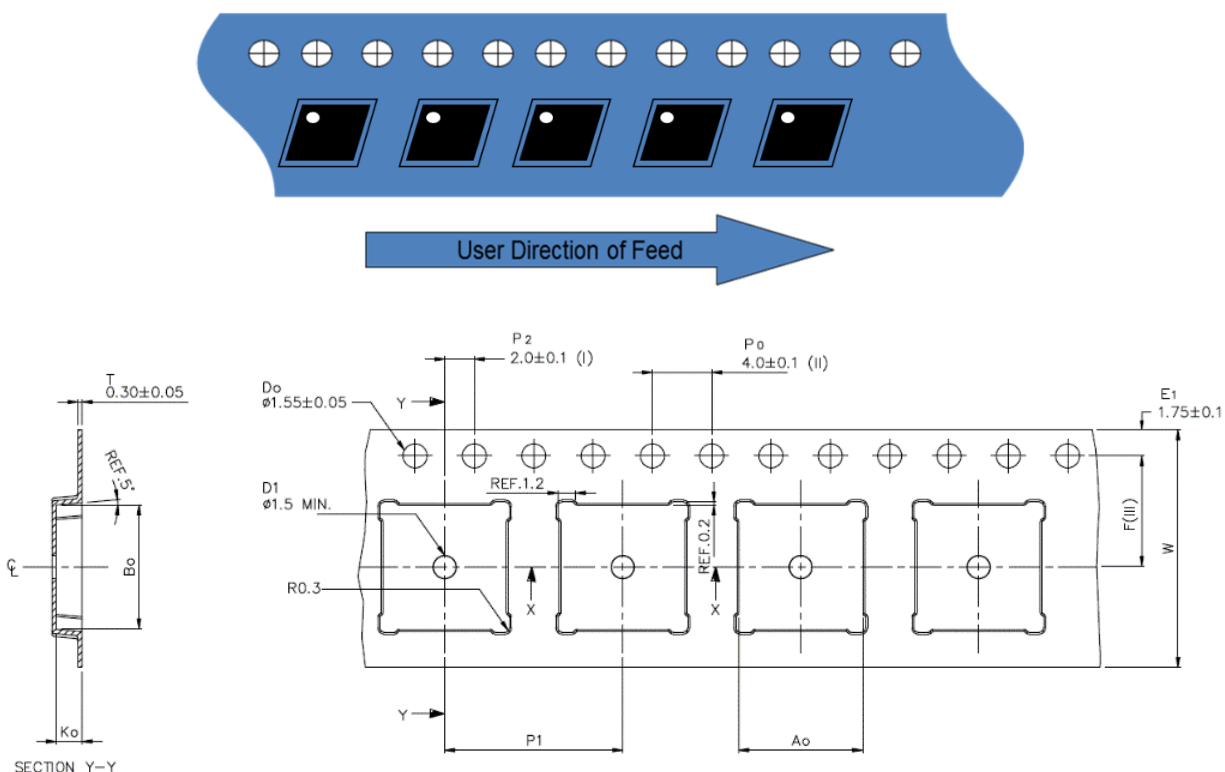
Trace Code – Assigned by assembly sub-contractor



Notes:

1. All dimensions are in microns. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

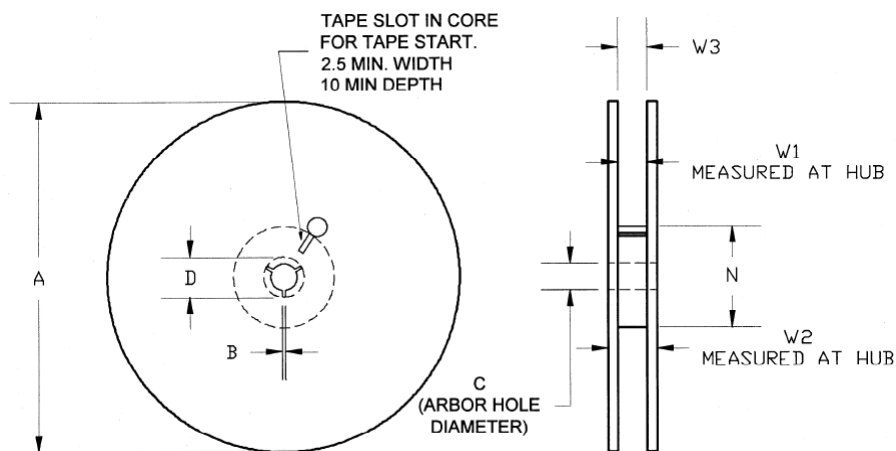
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.329	8.35
	Width	B0	0.329	8.35
	Depth	K0	0.069	1.76
	Pitch	P1	0.472	12.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.50
Cover Tape	Width	C	0.524	13.30
Carrier Tape	Width	W	0.630	16.0

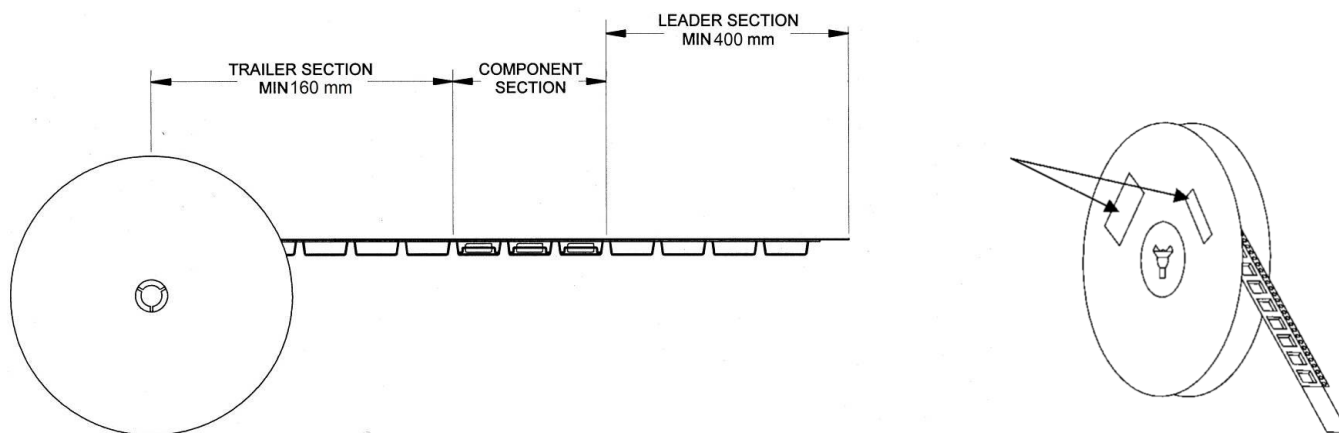
Tape and Reel Information – Reel Dimensions (13")

Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.874	22.2
	Space Between Flange	W1	0.661	16.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni (*Plating thickness: Ni = 5.0 ± 3.0 μm; Au ≥ 0.10 μm*)

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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