Intel Atom® Processor E3800 Product Family

Datasheet

October 2018

Revision 4.3

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Contents

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Table 142 LPC AC Specifications (with loop back from ILB_LPC_CLK[0] to ILB_LPC_CLK[1]) 197

Revision History

Revision Number	Description	Revision Date
1.0	Initial release.	October 2013
1.5	Chapter 2, “Physical Interfaces” • Updated the table details of the GPIO Signals for GPIO_S0_SC[046], GPIO_S0_SC[047], GPIO_S0_SC[048], GPIO_S5[15], GPIO_S5[16], GPIO_S5[17]. Chapter 5, “Integrated Clock” • Added table note (SoC Clock Outputs) that Intel recommends 25 MHz. 19.2 MHz is not validated. Chapter 6, “Power Management” • De-featured C6IS for all SKUs. • Updated the table details of the SoC Sx-States to SLPT_S*# for PMC_PLTRST# from 0 or 1 to High or Low to match platform understanding. • Remove VCC and VNN from Bay Trail-M/D SoC Power Rail DC Specs & Max Current table. Chapter 7, “Power Up and Reset Sequence” • Updated the figure and notes of the S0 to S3 to S4/S5 (Power Down) Sequence. • Updated the table of the S4/S5 to S0 (Power Up) Sequence for t3 parameter from 100 max to 95 min (no max). Chapter 9, “Electrical Specifications” • Updated the table details of the 25 MHz Platform Clock AC Specification. Chapter 11, “Processor Core” • Updated 11.1 note on Thermal management support. Chapter 12, “System Memory Controller” • Updated 12.2.2 table title and details for “Supported DDR3L Memory Size Per Rank” and “Supported DDR3L SO-DIMM Size”. Chapter 16, “Storage Control Cluster (eMMC, SDIO, SD Card)” • Updated the supported SDIO/SD card bandwidth is up to 400Mbits per seconds. Chapter 18, “USB Host Controller Interfaces (xHCI, EHCI)” • Added figure note of the xHCI and EHCI Port Mapping. • Updated USB configuration register to correctly reflect the power well. Chapter 22, “Intel® Trusted Execution Engine (TXE)” • Updated chapter title to Intel® Platform Trust Technology (PTT). Chapter 29, “Platform Controller Unit (PCU) Overview” • Added a note to Platform Clock Support section that Intel recommends 25 MHz as 19.2 MHz is not validated.	December 2013
2.0	Chapter 7, “Power Up and Reset Sequence” • Updated the 7.2.2 note 4 • OK to swap V1P0A and V1P8A • Measurement point for timing is 90% (10% on power down) Chapter 9, “Electrical Specifications” • Added S3 power spec per measurements • Added generic clock jitter specs	February 2014

Revision Number	Description	Revision Date
2.5	Chapter 2, "Physical Interfaces" • Updated 2.28 RTC_VCC detail Chapter 7, "Power Up and Reset Sequence" • Updated the 7.2.2 note 7 • Updated the 7.3.1 note 6 and note 7 • Measurement point for timing is 90% (10% on power down) Chapter 9, "Electrical Specifications" • Added 9.5.18 GPIO VIH max and VIL min • Added 9.5.19 I2C VIH max and VIL min	April 2014
3.0	Chapter 2, "Physical Interfaces" • Updated RTC_VCC detail Chapter 7, "Power Up and Reset Sequence" • Updated slew rate to 10ms. • Measurement point for timing is 10% on power down Chapter 9, "Electrical Specifications" • Added 9.5.18 GPIO VIH max and VIL min • Added 9.5.19 I2C VIH max and VIL min Chapter 11, "Processor Core" • Removed support on C1E and C6C Chapter 14, "Graphics, Video and Display" • Updated 14.10.11 MSR (MSR_READ) offset to 180000h Chapter 16, "Storage Control Cluster (eMMC, SDIO, SD Card)" • Updated the Preset value feature to not PoR. • Updated SDIO support SDR12/25. Chapter 22, "Intel® Trusted Execution Engine (TXE)" • Updated name of chapter to "Intel® Trusted Execution Engine (TXE)". • Clarified use of descriptor mode and other requirements for the boot SPI. • Added registers for Intel® TXE.	July 2014

Revision Number	Description	Revision Date
3.5	Chapter 2, "Physical Interfaces" • Changed Figure 3 USB_ULPI_REFCLK to output Chapter 5, "Integrated Clock" • Updated the MCSI clock to 80-500 MHz Chapter 7, "Power Up and Reset Sequence" • Updated Table 58, max tolerance time, to 2000us - to avoid in rush current • removed PMC_SUSPWRDNACK from figure 13 • updated PMC_SUSPWRDNACK in figure 14 Chapter 9, "Electrical Specifications" • Added SPI NOR AC Spec • Updated GPIO Vih/Vil min and max • changed the I2S max clock frequency to 12.288 MHz Chapter 11, "Processor Core" • Added Note: "L1 has parity protection and L2 has an ECC Protection." Chapter 12, "System Memory Controller" • Removed DECCSTAT OFFSET 61h register Chapter 13, "SoC Transaction Router" • Updated register TRR - OFFSET B1h Chapter 22, "Intel® Trusted Execution Engine (TXE)" • updated the SSP to support 24 bits data sample sizes Chapter 29, "Platform Controller Unit (PCU) Overview" • De-Featured Top Swap Mechanism	September 2014

Revision Number	Description	Revision Date
3.6	Chapter 1, "Introduction" • Changed Figure 1, "SoC Block Diagram" on page 34 • Changed Chapter 1, "Terminology" • Changed Chapter 1, "Display Controller" • Changed Chapter 1, "Graphics and Media Engine" • Changed Chapter 1, "SKU List" Chapter 2, "Physical Interfaces" • Changed Figure 3, "Signals (2 of 2)" on page 43 • Changed Chapter 2, "Pin States Through Reset" • Changed Table 9, "USB 2.0 Device Interface Signals" on page 49 • Changed Table 13, "Digital Display Interface Signals" on page 51 • Changed Chapter 2, "PCU – iLB – Low Pin Count (LPC) Bridge Interface Signals" • Changed Table 24, "PCU - Serial Peripheral Interface (SPI) Signals" on page 58 • Changed Table 30, "Power and Ground Pins" on page 66 Chapter 5, "Integrated Clock" • Updated Table 48, "SoC Clock Outputs" on page 88 Chapter 6, "Power Management" • Updated Table 50, "General Power States for System" on page 92 • Changed Chapter 6, "Package C-States" Chapter 7, "Power Up and Reset Sequence" • Updated Chapter 7, "G3 to S0" • Updated Table 63, "S3/S4/S5 to S0 Cause of Wake Events" on page 111 • Updated Chapter 7, "S0 to S3 and S4/S5/G3 Sequence" • Updated Chapter 7, "S0 to S3 to S4/S5 (Power Down) Sequence without S0ix" • Updated Table 63, "S3/S4/S5 to S0 Cause of Wake Events" on page 111 • Updated Chapter 7, "Reset Behavior" Chapter 8, "Thermal Management" • Updated Chapter 8, "Thermal Management" Chapter 9, "Electrical Specifications" • Updated Table 66, "Intel Atom® Processor E3800 Product Family Thermal Specifications" on page 118 • Updated Table 68, "Power Rail DC Specs and Max Current" on page 120 • Updated Table 69, "VCC and VNN Currents" on page 122 • Updated Table 75, "VGA_DDCCLK, VGA_DDCDATA Signal DC Specification" on page 133 • Updated Table 79, "DDI DDC Signal DC Specification (DDI[1:0]_DDCDATA, DDI[1:0]_DDCCLK)" on page 135 • Updated Table 83, "PCI Express* DC Clock Request Input Signal Characteristics" on page 137 • Updated Table 86, "SD Card DC Specification" on page 138 • Updated Table 87, "eMMC 4.5 Signal DC Electrical Specifications" on page 139 • Updated Table 88, "TAP Signal Group DC Specification (TAP_TCK, TAP_TRSRT#, TAP_TMS, TAP_TDI)" on page 140 • Updated Table 89, "TAP Signal Group DC Specification (TAP_TDO)" on page 140 • Updated Table 90, "TAP Signal Group DC Specification (TAP_PRDY#, TAP_PREQ#)" on page 141 • Updated Table 97, "Power Management 1.8V Suspend Well Signal Group DC Specification" on page 148 • Updated Table 100, "iLB RTC Well DC Specification (ILB_RTC_TEST#)" on page 149 • Added Table 105, "GPIO 3.3V Suspend Well Signal Group DC Specification (GPIO_S5[43:0])" on page 151 • Updated Table 106, "GPIO 1.8V Core Well Signal Group DC Specification (GPIO_S0_SC[101:0])" on page 152 • Updated Table 107, "GPIO 1.8V Suspend Well Signal Group DC Specification (GPIO_S5[43:0])" on page 152 • Updated Table 108, "I2C Signal Electrical Specifications" on page 153	January 2015

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3.6	• Updated Table 140, "PCU - SPI NOR AC Specification" on page 197 • Updated Table 140, "PCU - SPI NOR AC Specification" on page 197 Chapter 12, "System Memory Controller" • Updated Chapter 12, "Features" Chapter 14, "Graphics, Video and Display" • Updated Chapter 14, "Features" • Updated Chapter 14, "Video Engine" • Updated Table 170, "Hardware Accelerated Video Decode Codec Support" on page 423 Chapter 15, "MIPI-Camera Serial Interface (CSI) and ISP" • Updated Chapter 15, "Features" Updated Table 178, "Imaging Capabilities" on page 1048 Chapter 16, "Storage Control Cluster (eMMC, SDIO, SD Card)" • Updated Chapter 16, "SDIO/SD Card Interface Features" Chapter 21, "Low Power Engine (LPE) for Audio ($I^{2S)}$" • Updated Chapter 21, "External Timer" • Updated Table 227, "Clock Frequencies" on page 2817 Chapter 30, "PCU – Power Management Controller (PMC)" • Updated Table 292, "Transitions Due to Power Button" on page 4348 • Updated Chapter 30, "PMC_RSTBTN# Signal" • UpdatedTable 293, "System Power Planes" on page 4349 • Updated Table 294, "Causes of SMI and SCI" on page 4352 Chapter 31, "PCU – Serial Peripheral Interface (SPI)" • Updated Chapter 31, "Descriptor Mode" Chapter 32, "PCU – Universal Asynchronous Receiver/Transmitter (UART)" • Updated Chapter 32, "UART Enable/Disable" Chapter 33, "PCU – System Management Bus (SMBus)" • Added Chapter 33, "SPD Write Disable" Chapter 34, "PCU – Intel® Legacy Block (iLB) Overview" • Updated Chapter 34, "Non-Maskable Interrupt"	January 2015

Revision Number	Description	Revision Date
3.7	Chapter 1 • Remove eSATA capable from Section 1.2.8 Chapter 7.2.1 • Updated Table 60 • Updated Table 61 Chapter 9.3 • Updated Table 68, Added AC Voltage Tolerance for Platform Rail Chapter 9.6.1 • Removed Figure 19, Crystal Clock Timing • Removed Table 106, Crystal Clock Timings Chapter 9.5.8 • Updated Table 91 Chapter Note: • Updated Table 140 • Added Figure 68 Chapter 9.6.19 • Updated Table 142 • Updated Figure 69 Chapter 19.6.87 • Added Note to Bit Range 31 Section 23.6 • Removed Note from Bit Range 28 Chapter 39 • Added a note to Chapter 39, "Memory Mapped Use" • Updated Section 39.8.299 — Removed the VLV_GPIO_configuration_primer_presentation — Removed cross reverences from Bit Rages 30:24, 22:16, 14:8, and 6:0 • Updated Section 39.8.300 — Removed cross reverences from Bit Rages 30:24, 22:16, 14:8, and 6:0 • Updated Section 39.8.301 — Removed cross reverences from Bit Rages 30:24, 22:16, 14:8, and 6:0 • Updated Section 39.8.302 — Removed cross reverences from Bit Rages 30:24, 22:16, 14:8, and 6:0 • Updated Section 39.10.143 — Removed the VLV2_GPIO_configuration_primer_presentation — Removed cross reverences from Bit Rages 30:24, 22:16, 14:8, and 6:0 • Updated Section 39.10.144 • Removed cross reverences from Bit Rages 30:24, 22:16, 14:8, and 6:0 • Updated Section 39.10.145 — Removed cross reverences from Bit Rages 30:24, 22:16, 14:8, and 6:0 • Updated Section 39.10.146 — Removed cross reverences from Bit Rages 30:24, 22:16, 14:8, and 6:0	April 2015

Revision Number	Description	Revision Date
3.8	Chapter 4 • Updated Table 42 Section 7.2.2 • Updated Note page 106, Delay timing changed from 2000 μs to 10 ms Chapter 9.3 • Updated Table 68, Added AC Voltage Tolerance for Platform Rail	June 2015
3.9	Chapter 2.7 • Revised Table 29. Chapter 4.2 • Added New Table 44 • Revised Table 45 Chapter 4.2.2.1 • Added Table 44 • Revised Table 45 Chapter 9.5.6 • Revised Table 99 • Revised Table 100 and added Note 3. Chapter 9.5.18 • Revised Table 104 through Table 107 Chapter 9.6.4 • Revised Table 111 Chapter 9.6.10.1 • Revised Table 125 Chapter 12.3.9, DRFC (DRFC)—Offset 8h • Revised Bit Range 14:12 Chapter 17 • Added Note 1 Chapter 26.2.3 • Revised last bullet Chapter 26.2.3.3 • Master-Receiver and Slave-Transmitter paragraph revised. Chapter 26.3.1 Revised Step 6 bullets	October 2015

Revision Number	Description	Revision Date
4.0	Section 2.24 • Updated Table 26 Section 2.27 • Revised Table 29 Section 7.3 • Revised Note for Figure 12 Section 9.3 • Revised Table 70 Section 9.6.4 • Revised Table 113 Section 13.4 • Revised Table 162 • Added Table 13.4.8, "CUNIT_MSG_CTRL_REG_EXT—Offset D8h" on page 349 Section 16 • Added Second Note Section 30.1 • Revised Table 292 Section 30.7.15 Revised TCO Timer reload value	May 2016

Revision Number	Description	Revision Date
4.1	Section 1.2.1 • Updated Chapter 11 cross reference Section 1.2.2 • Updated Chapter 12 cross reference Section 1.2.3 • Updated Chapter 14 cross reference Section 1.2.4 • Updated Chapter 14 cross reference Section 1.2.5 • Updated Chapter 15 cross reference Section 1.2.6 • Updated Chapter 6 cross reference Section 1.2.7 • Updated Chapter 15 cross reference Section 1.2.8 • Updated Chapter 17 cross reference Section 1.2.9 • Updated Chapter 18 cross reference Section 1.2.10 • Updated Chapter 18 cross reference Section 1.2.11 • Updated Chapter 19 cross reference Section 1.2.12.1 • Updated Chapter 21 cross reference Section 1.2.12.2 • Updated Chapter 20 cross reference Section 1.2.13 • Updated Chapter 16 cross reference Section 1.2.14 • Updated Chapter 22 cross reference Section 1.2.15 • Updated Chapter 24 cross reference Section 1.2.16 • Updated Chapter 29 cross reference Section 1.2.17 • Updated Chapter 10 cross reference Section 6.1 • Revised second bullet statement and added new bullet Section 6.3.4.3 • Added new bullet Section 6.3.5 • Revised first paragraph • Added new and updated Table Notes • Removed Figure 11. Package C-state Entry and Exit Section 6.3.5.2, Package C1 removed	July 2016

Revision Number	Description	Revision Date
4.1 Cont.	Section 6.3.5.3 • Revised bullet Section 6.3.5.3, Package C7 State added	July 2016
4.2	Section 2.24 • Updated Table 26 Section 7.3.1 • Updated Section 63 Section 12.2.1 • Updated Section 157 Revised Section 26.7.1,"I2C Control Register (IC_CON)—Offset 0h" Revised Section 26.9.2, "I2C Target Address Register (IC_TAR)—Offset 4h" Revised Section 27.6.3, "Interrupt Identification Register and FIFO Control Register. (IIR_FCR)—Offset 8h" Section 30.1 • Updated Table 290	December 2016

Revision Number	Description	Revision Date
4.3	Section 4.1.2 • Updated Table 42 Section 7.3.1 • Updated Table 12 • Updated Table 61 Section 9.6.10.1 • Updated Table 127 Removed Chapter "PCU - SPI AC Specification" Removed Figure "SPI AC Timing" Section 17.1 • Updated Table 192 Section 18.9 • Updated Section 215 • Added Section 18.9.24,"USB Test Per Port Register 1 (USB2_TEST_PERPORT_REG1_LANE0/1/2/3) - Offset 4113h/4213h/4313h/4413h" • Added Section 18.9.25,"Per Port RCOMP High Speed Pull down Register (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_LANE0/1/2/3) - Offset 4123h/4223h/4323h/4423h" • Added Section 18.9.26,"USB Per Port (USB2_PER_PORT_2_LANE0/1/2/3) - Offset 4126h/4226h/4326h/4426h" Section 26.7.2 • Updated table Section 27.2.2 • Updated Table 280 Revised Section 34.2.1 Revised Section 35.2.2 Revised Section 35.3.2.2 Section 35.6 • Updated Table 325 • Added Section 35.6.25,"Manufacturer ID (PCIE_REG_MANUFACTURER_ID) - Offset F8h" Section 39.10.91 • Added Notes	October 2018

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1 Introduction

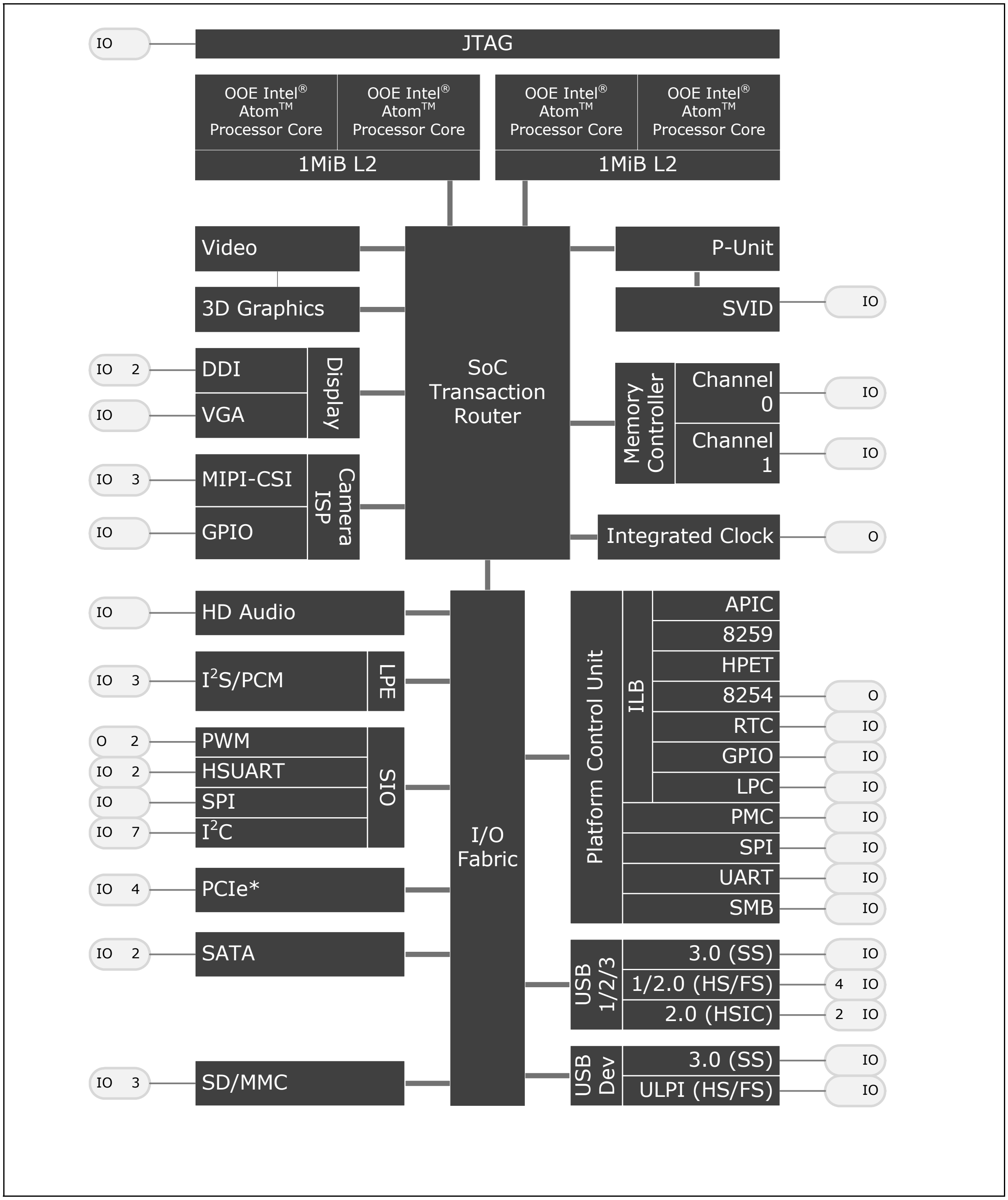
The Intel Atom ® Processor E3800 Product Family is the Intel Architecture (IA) SoC that integrates the next generation Intel® processor core, Graphics, Memory Controller, and I/O interfaces into a single system-on-chip solution.

The figures below show the system level block diagram of the SoC. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

Notes: Throughout this document Intel Atom ® Processor E3800 Product Family is referred to as the SoC or Processor.

This document details features of the silicon only. For platform support and software, contact your Intel representative.

Figure 1. SoC Block Diagram



1.1 Terminology

Term	Description
ACPI	Advanced Configuration and Power Interface
Cold Reset	A Host reset with Power Cycle. See Table 135
CRT	Cathode Ray Tube
CRU	Clock Reset Unit
DP	Display Port
DTS	Digital Thermal Sensor
EMI	Electro Magnetic Interference
eDP	embedded Display Port
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. HDMI transmits all Advanced Television Systems Committee (ATSC) HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available at http://www.hdmi.org/).
IGD	Internal Graphics Unit
Intel® TXE	Intel® Trusted Execution Engine
LCD	Liquid Crystal Display
LPE	Low Power Engine
MIPI CSI	MIPI Camera Interface Specification
MPEG	Moving Picture Experts Group
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
MSR	Model Specific Register, as the name implies, is model-specific and may change from processor model number (n) to processor model number (n+1). An MSR is accessed by setting ECX to the register number and executing either the RDMSR or WRMSR instruction. The RDMSR instruction will place the 64 bits of the MSR in the EDX: EAX register pair. The WRMSR writes the contents of the EDX: EAX register pair into the MSR.
PCIe*	PCI Express* (PCIe*) is a high-speed serial interface. The PCIe* configuration is software-compatible with the existing PCI specifications.
PWM	Pulse Width Modulation
Rank	A unit of DRAM corresponding to the set of SDRAM devices that are accessed in parallel for a given transaction. For a 64-bit wide data bus using 8-bit (x8) wide SDRAM devices, a rank would be eight devices. Multiple ranks can be added to increase capacity without widening the data bus, at the cost of additional electrical loading.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SDRAM	Synchronous Dynamic Random Access Memory
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.

Term	Description
SMI	System Management Interrupt is used to indicate any of several system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).
SIO	Serial I/O
TMDS	Transition-Minimized Differential Signaling. TMDS is a serial signaling interface used in DVI and HDMI to send visual data to a display. TMDS is based on low-voltage differential signaling with 8/10b encoding for DC balancing.
VCO	Voltage Controlled Oscillator
Warm Reset	Host Reset without Power Cycle. See Table 134

1.2 Feature Overview

All features subject to software availability.

1.2.1 Processor Core

See Chapter 11, "Processor Core" for more details.

- Up to four IA-compatible low power Intel® processor cores
  - One thread per core
- Two-wide instruction decode, out of order execution
- On-die, 32 KB 8-way L1 instruction cache and 24 KB 6-way L1 data cache per core
- On-die, 1 MB, 16-way L2 cache, shared per two cores
- L1 has parity protection and L2 has ECC protection
- 36-bit physical address, 48-bit linear address size support
- Supported C-states: C0, C1, C6
- Supports Intel® Virtualization Technology (Intel® VT-x)

1.2.2 System Memory Controller

See Chapter 12, "System Memory Controller" for more details.

- Supports up to two channels of DDR3L
- 64 bit data bus for each channel
- ECC supported in single channel mode only
- Supports x8 and x16 DDR3L SDRAM device data widths
- Supports DDR3L with 1066 or 1333 MT/s data rates
  - Total memory bandwidth supported is 8.5 GB/s (for 1066 MT/s single channel) scalable to 21.3GB/s(for 1333 MT/s dual channel)
- Supports different physical mappings of bank addresses to optimize performance

- Out-of-order request processing to increase performance
- Aggressive power management to reduce power consumption
- Proactive page closing policies to close unused pages

1.2.3 Display Controller

See Chapter 14, "Graphics, Video and Display" for more details.

- Support 2 DDI ports to enable eDP 1.3, DP 1.1a, DVI, or HDMI 1.4a
- Support 2 panel power sequence for 2 eDP ports
- Support Audio on DP and HDMI
- Supports Intel® Display Power Saving Technology (DPST) 6.0, Panel Self Refresh (PSR) and Display Refresh Rate Switching Technology (DRRS)
- Supports one VGA port

Note: These feature are not applicable to the E3805 SKU.

1.2.4 Graphics and Media Engine

See Chapter 14, "Graphics, Video and Display" for more details.

- Intel's 7th generation (Gen 7) graphics and media encode/decode engine
- VED video decoder in addition to Gen 7 Media decoder
- Supports DX*11, OpenGL 3.0 (OGL 3.0), OpenCL 1.2 (OCL 1.2), OpenGLES 2.0 (OGLES 2.0)
- GPU shader is capable of up to 8 gigaflops
- 4x anti-aliasing
- Full HW acceleration for decode of Up to 1080p@60fps and 3x 4kx2k @30fps (H.264/JPEG/MJPEG/MVC/MPEG-2 /WMV9/VC1)
- Full HW acceleration for encode of Up to 1080p@60fps and 1x 4kx2k @30fps (H.264)
- Supports 2.0 Stereoscopic 3D Stretch
- Polyphase 8 tap scaling
- HD HQV

Note: These feature are not applicable to the E3805 SKU.

1.2.5 Image Signal Processor

See Chapter 15, "MIPI-Camera Serial Interface (CSI) and ISP" for more details.

- Support up to three MIPI CSI ports
- Support for up to 24MP sensors

- Supports Stereoscopic Video

1.2.6 Power Management

See Chapter 6, "Power Management" for more details.

- ACPI 5.0 support
- Processor states: C0-C6
- Display device states: D0, D3
- Graphics device states: D0, D3
- System sleep states: S0, S3, S4, S5
- Dynamic I/O power reductions (disabling sense amps on input buffers, tristating output buffers)
- Active power-down of display links
- Downloadable power management firmware

1.2.7 PCI Express*

The SoC has four PCI Express* lanes and up to four PCI Express root ports, each supporting the PCI Express Base specification Rev 2.0 at a maximum of 5 Gbit/s data transfer rates.The root ports configurations are flexible and can be configured to be (4) x1, (2) x2's, (1) x2 plus (2) x1's, and (1) x4.

See Chapter 15, "MIPI-Camera Serial Interface (CSI) and ISP" for more details.

1.2.8 SATA

See Chapter 17, "Serial ATA (SATA)" for more details.

- Two (2) SATA Revision 2.0 ports
- Legacy IDE (including IRQ)/Native IDE/AHCI appearance to OS
- Partial/Slumber power management modes with wake
- Capable of 3 Gbit/s transfer rate

1.2.9 USB xHCI Controller

See Chapter 18, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

- Supports USB 3.0/2.0/1.1
- Implements xHCI software host controller interface
- One USB 3.0 Super Speed (SS) port
- Four ports multiplexed with EHCI controller that are High Speed/Full Speed (HS/FS)
- Two High Speed Inter Chip (HSIC) ports compliant with USB 2.0

1.2.10 USB 2.0 EHCI Controller

See Chapter 18, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

- Internal Rate Matching Hub to support USB 1.1 to 2.0 devices
- Four Ports multiplexed with xHCI controller
- Enhanced EHCI descriptor caching

1.2.11 USB 2.0 (ULPI) and 3.0 Device

See Chapter 19, "USB Device Controller Interfaces (3.0, ULPI)" for more details.

- Supports one USB 3.0 SS port with USB device compatibility
- Supports one ULPI port with HS/LS support

1.2.12 Audio Controllers

1.2.12.1 Low Power Engine (LPE) Audio

LPE is a complete audio solution based on an internal audio processing engine, which includes three I^2S output ports. See Chapter 21, "Low Power Engine (LPE) for Audio (I^2S)" for more details.

LPE supports:

- I^2S and DDI with dedicated DMA
- MP3, AAC, AC3/DD+, WMA9, PCM (WAV)

Note: Codecs supported depend on software and may be different.

1.2.12.2 Intel® High Definition Audio (Intel® HD Audio)

See Chapter 20, "Intel® High Definition Audio" for more details.

- Four in + four out streams (Only 3 used)
- One stream for each DDI, available for HDMI and DP
- No wake on audio (modem) support

1.2.13 Storage Control Cluster (eMMC, SDIO, SD)

See Chapter 16, "Storage Control Cluster (eMMC, SDIO, SD Card)" for more details.

- Supports one SDIO 3.0 controller
- Supports one eMMC 4.5 controller
- Supports one SDXC controller

1.2.14 Intel® Trusted Execution Engine (Intel® TXE)

Intel® TXE is a security co-processor used to enable security features.

See Chapter 22, "Intel® Trusted Execution Engine (TXE)" for more details.

Security features include:

- Isolated execution environment for crypto operations (SKU-enabled)
- Supports secure boot - with customer programmable keys to secure code

Note: The SoC requires TXE firmware in the PCU SPI flash image to function. Contact your Intel® representative for details.

1.2.15 Serial I/O (SIO)

See Chapter 24, "Serial IO (SIO) Overview" for links to more information about each interface.

- Controller for external devices via SPI, UART, I^2C or PWM
- Each port is multiplexed with general purpose I/O for configurations flexibility
- Supports up to 7 I^2C, 2 HSUART, 2 PWM, 1 SPI interface

1.2.16 Platform Control Unit (PCU)

The platform controller unit is a collection of HW blocks, including SMBus, UART, debug/boot SPI and Intel legacy block (iLB), that are critical to implement a Windows* compatible platform. See Chapter 29, "Platform Controller Unit (PCU) Overview" for links to more information about each interface.

Key PCU features include:

- SMBus Host controller - supports SMBus 2.0 specification
- Universal Asynchronous Receiver/Transmitter (UART) with COM1 interface
- A Serial Peripheral Interface (SPI) for Flash only - stores boot FW and system configuration data
- Intel Legacy Block (iLB) supports legacy PC platform features
  - RTC, Interrupts, Timers, General Purpose I/Os (GPIO) and Peripheral interface (LPC for TPM) blocks.

1.2.17 Package

This SoC is packaged in a Flip-Chip Ball Grid Array (FCBGA) package with 1170 solder balls with 0.593 mm (minimum) ball pitch. The package dimensions are 25mm x 27mm. See Chapter 10, "Ballout and Package Information" for more details.

1.2.18 SKU List

Table 1. Intel Atom ® Processor E3800 Product Family SKUs

SKU	Processor Number	CPU	TDP (W)	Core LFM (MHz)/ HFM (GHz)	Tj (°C)	GFX Normal / Burst (MHz)	DDR (MT/s)
Premium	E3845	4	10	500 / 1.91	-40 to 110	542 / 792	1333
Hi	E3827	2	8	500 / 1.75	-40 to 110	542 / 792	1333
Intermediate	E3826	2	7	533 / 1.46	-40 to 110	533 / 667	1066
Mid	E3825	2	6	533 / 1.33	-40 to 110	533 / NA	1066
Entry	E3815	1	5	533 / 1.46	-40 to 110	400 / NA	1066
Headless	E3805	2	3	533 / 1.33	-40 to 110	NA	1066

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2 Physical Interfaces

Many interfaces contain physical pins. These groups of pins make up the physical interfaces. Because of the large number of interfaces and the small size of the package, Some interfaces share their pins with GPIOs, while others use dedicated physical pins. This chapter summarizes the physical interfaces, including the diversity in GPIO multiplexing options.

Figure 2. Signals (1 of 2)

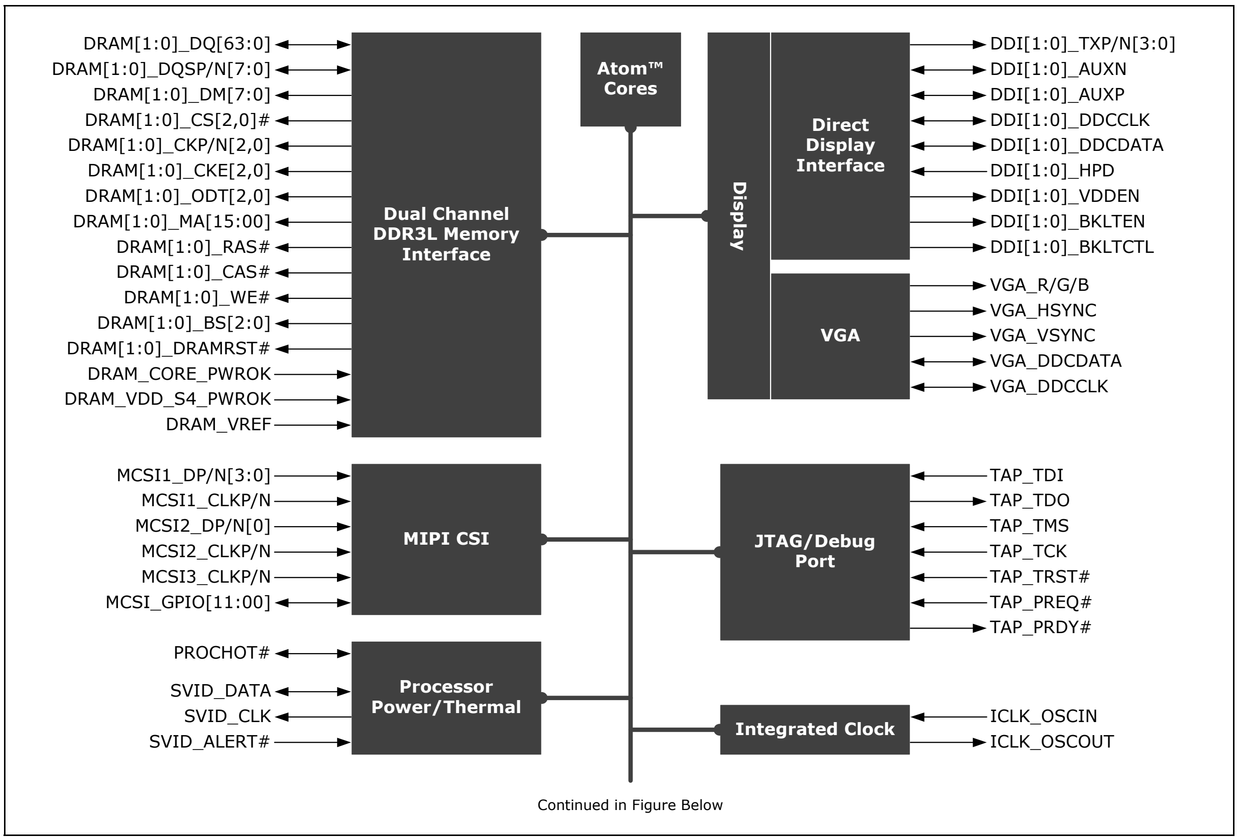
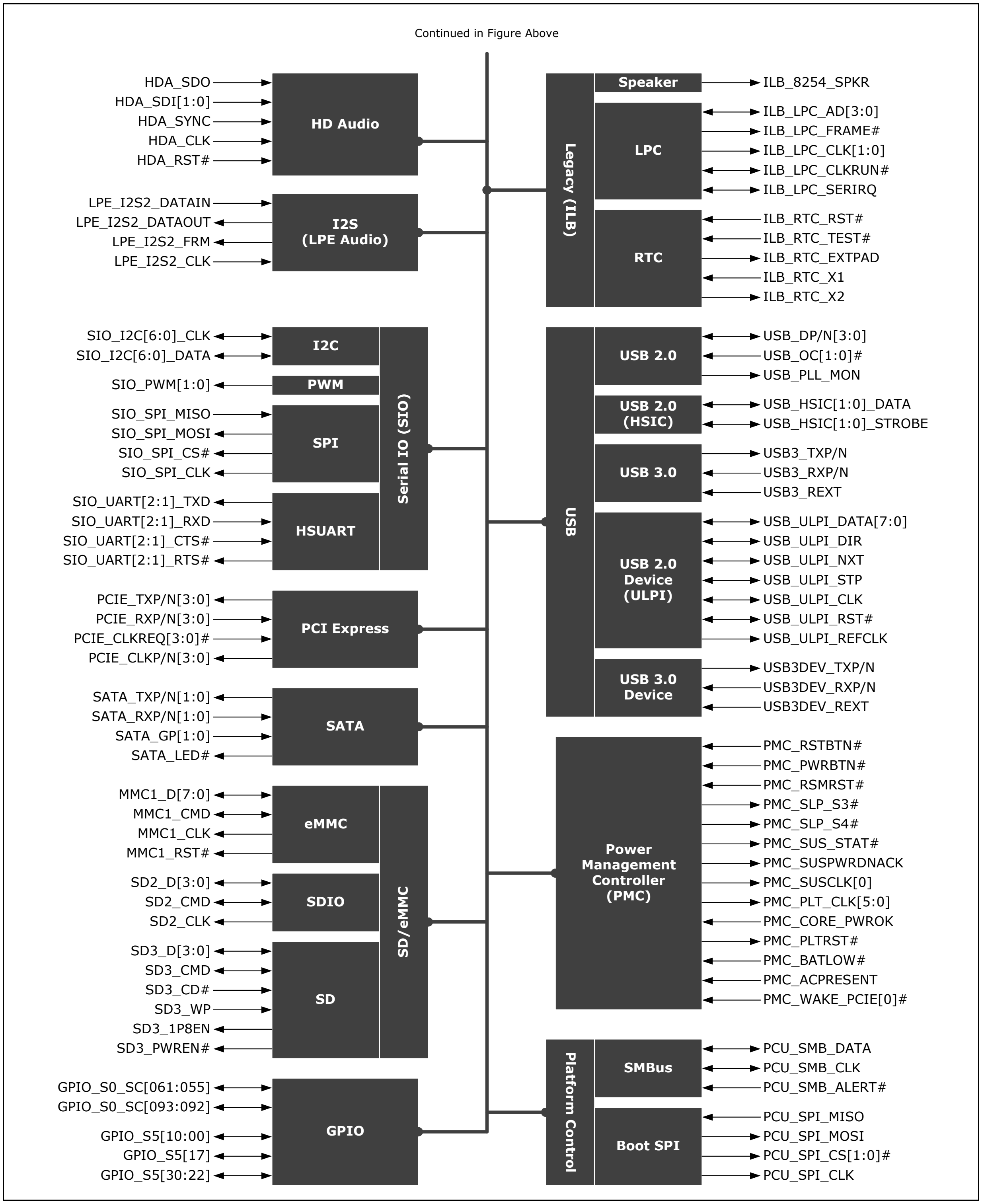


Figure 3. Signals (2 of 2)



2.1 Pin States Through Reset

This chapter describes the states of each signal before, during and directly after reset. Additionally, Some signals have internal pull-up/pull-down termination resistors, and their values are also provided (Term). Termination tolerances are +/- 50% unless otherwise specified by electrical specs (PCIe*, and other differential termination). All signals with the "†" symbol are muxed and may not be available without configuration. See Section 2.30, "Configurable IO: GPIO Muxing" on page 68.

Note: The internal termination resistor values & pull directions described in this chapter are the power-on defaults. Firmware & software may change the termination value, pull direction or disable the termination completely, on a pin-by-pin basis, using the _PCONF0 register corresponding to that pin.

Table 2. Platform Power Well Definitions

Power Type	Power Well Description
V1P05S	1.05 V rail. On in S0 only.
V1P0A	1.0 V rail. On in S0 through S4/5.
V1P0S	1.0 V rail. On in S0 only.
V1P24A	1.24 V rail. On in S0 through S4/5.
V1P24S	1.24 V rail. On in S0 only.
V1P35U	1.35 V rail. On in S0 through S3.
V1P8A	1.8 V rail. On in S0 through S4/5.
V1P35S	1.35 V rail. On in S0 only.
V1P8S	1.8 V rail. On in S0 only.
V3P3A	3.3 V rail. On in S0 through S4/5.
VAUD	1.5 V rail for HD Audio. 1.8 V rail for I^2S. On in S0 only.
VCC	Variable core rail. On in S0 only.
VLPC	1.8 or 3.3 V rail for LPC. On in S0 only.
VNN	Variable rail. On in S0 only.
VPCIESATA	1.0 V rail for PCIe* and SATA. On in S0 only.
VRTC	RTC voltage rail. On in S0 through G3.
VSDIO	1.8 or 3.3 V rail for SD3. On in S0 only.
VSFR	1.35 V rail for internal PLLs. On in S0 only.
VUSB2	3.3 V rail. On in S0 through S4/5.
VVGA_GPIO	3.3 V rail for VGA sideband. On in S0 only.

Table 3. Default Buffer State Definitions

Buffer State	Description
High-Z	The SoC places this output in a high-impedance state. For inputs, external drivers are not expected.
Do Not Care	The state of the input (driven or tristated) does not affect the SoC. For outputs, it is assumed that the output buffer is in a high-impedance state.
V_{OH}	The SoC drives this signal high with a termination of 50 Ω.
V_{OL}	The SoC drives this signal low with a termination of 50 Ω.
Unknown	The SoC drives or expects an indeterminate value.
V_{IH}	The SoC expects/requires the signal to be driven high.
V_{IL}	The SoC expects/requires the signal to be driven low.
Pull-up	This signal is pulled high by a pull-up resistor (internal value specified in "Term" column).
Pull-down	This signal is pulled low by a pull-down resistor (internal value specified in "Term" column).
Running/T	The clock is toggling, or the signal is transitioning.
Off	The power plane for this signal is powered down. The SoC does not drive outputs, and inputs should not be driven to the SoC. (VSS on output)

2.2 System Memory Controller Interface Signals

See Chapter 12, "System Memory Controller" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 4. DDR3L System Memory Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				Notes
				S4/S5	S3	Reset	Enter S0	
DRAM0_CKP[2,0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_CKN[2,0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_CS#[2,0]	O	-	V1P35U	Off	V_{OH}	V_{OH}	V_{OH}	
DRAM0_CKE[2,0]	O	-	V1P35U	Off	V_{OL}	V_{OL}	V_{OL}	
DRAM0_CAS#	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_RAS#	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_WE#	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_BS[2:0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_DRAMRST#	O	-	V1P35U	Off	-	-	-	
DRAM0_ODT[2,0]	O	-	V1P35U	Off	V_{OL}	V_{OL}	V_{OL}	
DRAM0_DQ[63:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_DM[7:0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_DQSP[7:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM0_DQSN[7:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_CKP[2,0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_CKN[2,0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_CKE[2,0]	O	-	V1P35U	Off	V_{OL}	V_{OL}	V_{OL}	
DRAM1_CS#[2,0]	O	-	V1P35U	Off	V_{OH}	V_{OH}	V_{OH}	
DRAM1_CAS#	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_RAS#	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_WE#	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_BS[2:0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_DRAMRST#	O	-	V1P35U	Off	-	-	-	
DRAM1_ODT[2,0]	O	-	V1P35U	Off	V_{OL}	V_{OL}	V_{OL}	
DRAM1_DQ[63:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_DM[7:0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_DQSP[7:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM1_DQSN[7:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z	
DRAM_VDD_S4_PWROK	I	-	V1P35U	V_{IL}	V_{IH}	Unknown	V_{IH}	
DRAM_CORE_PWROK	I	-	V1P35U	V_{IL}	V_{IL}	Unknown	V_{IH}	
DRAM_VREF	I	-	V1P35U					
DRAM_RCOMP[2:0]	-	-	V1P35U					

2.3 PCI Express* 2.0 Interface Signals

See Chapter 21, "PCI Express* 2.0" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 5. PCI Express* 2.0 Interface Signals

				Default Buffer State				
Signal Name	**Dir**	**Term**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**	**Notes**
PCIE_TXP[3:0]	O	50	VPCIESATA	Off	Off	V_{OL}	V_{OL}	
PCIE_TXN[3:0]	O	50	VPCIESATA	Off	Off	V_{OL}	V_{OL}	
PCIE_RXP[3:0]	I	50	VPCIESATA	Off	Off	High-Z	High-Z	
PCIE_RXN[3:0]	I	50	VPCIESATA	Off	Off	High-Z	High-Z	
PCIE_CLKP[3:0]	O	-	V1P0S	Off	Off	Running/ V_{IL}	Running/ V_{IL}	
PCIE_CLKN[3:0]	O	-	V1P0S	Off	Off	Running/ V_{IL}	Running/ V_{IL}	
PCIE_CLKREQ[3:0]#†	I	20k(H)	V1P8S	Off	Off	Pull_up	Pull_up	
PCIE_RCOMP_P/N	-	-						

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.4 USB 2.0 Host (EHCI/xHCI) Interface Signals

See Chapter 18, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 6. USB 2.0 Interface Signals

				Default Buffer State				
Signal Name	**Dir**	**Term**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**	**Notes**
USB_DN[3:0]	I/O	-	VUSB2					
USB_DP[3:0]	I/O	-	VUSB2					
USB_OC[1:0]#†	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
USB_RCOMPI	I	-	-					
USB_RCOMPO	O	-	-					

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.5 USB 2.0 HSIC Interface Signals

See Chapter 18, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 7. USB 2.0 HSIC Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State: S4/S5	S3	Reset	Enter S0	Notes
USB_HSIC0_DATA	I/O	-	V1P24A	Running	Running	V_{OH}	Running	
USB_HSIC0_STROBE	I/O	-	V1P24A	V_{OH}				
USB_HSIC1_DATA	I/O	-	V1P24A			V_{OH}		
USB_HSIC1_STROBE	I/O	-	V1P24A	V_{OH}				
USB_HSIC_RCOMP	I	-	V1P24A			V_{OH}		

2.6 USB 3.0 (xHCI) Host Interface Signals

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 8. USB 3.0 Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State: S4/S5	S3	Reset	Enter S0	Notes
USB3_TXN[0]	O	-	V1P0A					
USB3_TXP[0]	O	-	V1P0A					
USB3_RXN[0]	I	-	V1P0A					
USB3_RXP[0]	I	-	V1P0A					
USB3_REXT[0]	I	-	V1P0A	V_{OL}	V_{OL}	V_{OH}	V_{OH}	

2.7 USB 2.0 Device (ULPI) Interface Signals

See Chapter 19, "USB Device Controller Interfaces (3.0, ULPI)" for more details.

Note: S0ix is not supported for Bay Trail-I SKUs.

Table 9. USB 2.0 Device Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
USB_ULPI_CLK†	I	20k(L)	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down	Pull-down
USB_ULPI_DATA[0:7]†	I/O	20k(L)	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down	Pull-down
USB_ULPI_DIR†	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	Pull-up
USB_ULPI_NXT†	I	20k(L)	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down	Pull-down
USB_ULPI_STP†	O	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	Pull-up
USB_ULPI_REFCLK†	O	20k(L)	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down	Pull-down
USB_ULPI_RST#†	O	-	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down	Pull-down

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.8 USB 3.0 Device Interface Signals

See Chapter 19, "USB Device Controller Interfaces (3.0, ULPI)" for more details.

Note: S0ix is not supported for Bay Trail-I SKUs.

Table 10. USB 3.0 Device Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
USB3DEV_TXN[0]	O	-	V1P0S					
USB3DEV_TXP[0]	O	-	V1P0S					
USB3DEV_RXN[0]	I	-	V1P0S					
USB3DEV_RXP[0]	I	-	V1P0S					
USB3DEV_REXT[0]	I	-	V1P0S					

2.9 Serial ATA (SATA) 2.0 Interface Signals

See Chapter 17, “Serial ATA (SATA)” for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 11. SATA 2.0 Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
SATA_TXP[1:0]	O		VPCIESATA	Off	Off			
SATA_TXN[1:0]	O		VPCIESATA	Off	Off			
SATA_RXP[1:0]	I		VPCIESATA	Off	Off			
SATA_RXN[1:0]	I		VPCIESATA	Off	Off			
SATA_LED#†	O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	Pull-up
SATA_GP[1:0]†	I	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	Pull-down
SATA_RCOMP_P/N	-	-	1.0 V					

NOTE: All signals with the “†” symbol are muxed and may not be available without configuration.

2.10 Integrated Clock Interface Signals

See Chapter 5, “Integrated Clock” for more details..

Table 12. Integrated Clock Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
ICLK_OSCIN	I	-		Off	Off	Running	Running	
ICLK_OSCOUT	O	-		Off	Off	Running	Running	
ICLK_ICOMP	-	-		Off	Off			
ICLK_RCOMP	-	-		Off	Off			
ICLK_DRAM_TERM[1:0]	-	-	-	Pull-down	Pull-down	Pull-down	Pull-down	
ICLK_USB_TERM[1:0]	-	-	-	Pull-down	Pull-down	Pull-down	Pull-down	

2.11 Display - Digital Display Interface (DDI) Signals

See Chapter 14, "Graphics, Video and Display" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 13. Digital Display Interface Signals

				Default Buffer State				
Signal Name	**Dir**	**Term**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**	**Notes**
DDI0_TXP[3:0]	O		V1P0S	Off	Off			
DDI0_TXN[3:0]	O		V1P0S	Off	Off			
DDI0_AUXP	I/O		V1P0S	Off	Off			
DDI0_AUXN	I/O		V1P0S	Off	Off			
DDI0_BKLTCTL†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
DDI0_BKLTEN†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
DDI0_DDCCLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
DDI0_DDCDATA†	I/O	20k(L) 1	V1P8S	Off	Off	Pull-down[1]	Pull-up[2]	
DDI0_HPD†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
DDI0_VDDEN†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
DDI_RCOMP_P/N	-	-	V1P0S					
DDI1_TXP[3:0]	O		V1P0S	Off	Off			
DDI1_TXN[3:0]	O		V1P0S	Off	Off			
DDI1_AUXP	I/O		V1P0S	Off	Off			
DDI1_AUXN	I/O		V1P0S	Off	Off			
DDI1_BKLTCTL†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
DDI1_BKLTEN†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
DDI1_DDCCLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
DDI1_DDCDATA†	I/O	20k(L) 1	V1P8S	Off	Off	Pull-down[1]	Pull-up[2]	
DDI1_HPD†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
DDI1_VDDEN†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	

NOTE: 1. The internal pull-down resistor is disabled upon assertion of PMC_CORE_PWROK.
NOTE: 2. When the corresponding DDI port is used, an external pull-up resistor is required.
NOTE: 3. All signals with the "†" symbol are muxed and may not be available without configuration.

2.12 Display – VGA Interface Signals

See Chapter 14, "Graphics, Video and Display" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 14. VGA Interface Signals

Signal Name	Dir	Term	Plat. Power	Type	Default Buffer State				
					S4/S5	S3	Reset	Enter S0	Notes
VGA_RED	O		VVGA_GPIO		Off	Off	High-Z		
VGA_GREEN	O		VVGA_GPIO		Off	Off	High-Z		
VGA_BLUE	O		VVGA_GPIO		Off	Off	High-Z		
VGA_IREF					Off	Off	V_{OL}		
VGA_IRTN					Off	Off	High-Z		
VGA_HSYNC	O		VVGA_GPIO		Off	Off	V_{OL}		
VGA_VSYNC	O		VVGA_GPIO		Off	Off	V_{OL}		
VGA_DDCCLK	O		VVGA_GPIO		Off	Off	High-Z		
VGA_DDCDATA	I/O		VVGA_GPIO		Off	Off	High-Z		

2.13 MIPI Camera Serial Interface (CSI) and ISP Interface Signals

See Chapter 15, "MIPI-Camera Serial Interface (CSI) and ISP" for more details.

Note: S0ix is not supported for Bay Trail-I SKUs.

Table 15. MIPI CSI Interface Signals (Sheet 1 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
MCSI1_CLKN	I		V1P24S	Off				
MCSI1_CLKP	I		V1P24S	Off				
MCSI1_DN[0:3]	I		V1P24S	Off				
MCSI1_DP[0:3]	I		V1P24S	Off				
MCSI2_CLKN	I		V1P24S	Off				
MCSI2_CLKP	I		V1P24S	Off				
MCSI2_DN[0]	I		V1P24S	Off				
MCSI2_DP[0]	I		V1P24S	Off				

Table 15. MIPI CSI Interface Signals (Sheet 2 of 2)

				Default Buffer State				
Signal Name	**Dir**	**Term**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**	**Notes**
MCSI3_CLKN	I		V1P24S	Off				
MCSI3_CLKP	I		V1P24S	Off				
MCSI_RCOMP	-		V1P24S	Off	High-Z	High-Z	High-Z	

2.14 Intel® High Definition Audio Interface Signals

See Chapter 20, “Intel® High Definition Audio” for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 16. HD Audio Interface Signals

				Default Buffer State				
Signal Name	**Dir**	**Term**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**	**Notes**
HDA_SDO†	O	20k(L)	VAUD	Off	Off	Pull-down	Pull-down	
HDA_SDI[1:0]†	I	20k(L)	VAUD	Off	Off	Pull-down	Pull-down	
HDA_CLK†	O	20k(L)	VAUD	Off	Off	Pull-down	Pull-down	
HDA_RST#†	O	20k(L)	VAUD	Off	Off	Pull-down	Pull-down	
HDA_SYNC†	O	20k(L)	VAUD	Off	Off	Pull-down	Pull-down	
HDA_LPE_RCOMP	-							

NOTE: All signals with the “†” symbol are muxed and may not be available without configuration.

2.15 Low Power Engine (LPE) for Audio (I^2S) Interface Signals

See Chapter 21, “Low Power Engine (LPE) for Audio (I^2S)” for more details.

Note: S0ix is not supported for Bay Trail-I SKUs.

Table 17. LPE Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
LPE_I2S[2:0]_CLK	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
LPE_I2S[2:0]_FRM	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
LPE_I2S[2:0]_DATAOUT	O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
LPE_I2S[2:0]_DATAIN	I	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	

2.16 Storage Control Cluster (eMMC, SDIO, SD) Interface Signals

See Chapter 16, "Storage Control Cluster (eMMC, SDIO, SD Card)" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 18. Storage Control Cluster (eMMC, SDIO, SD) Interface Signals (Sheet 1 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
MMC1_D[7:0]†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
MMC1_CMD†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
MMC1_CLK†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
MMC1_RST#†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
MMC1_RCOMP	I/O	-	V1P8S					
SD2_D[3:0]†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SD2_CMD†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SD2_CLK†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
SD3_D[3:0]†	I/O	20k(H)	VSDIO	Off	Off	Pull-up	Pull-up	
SD3_CMD†	I/O	20k(H)	VSDIO	Off	Off	Pull-up	Pull-up	
SD3_CLK†	I/O	20k(L)	VSDIO	Off	Off	Pull-down	Pull-down	
SD3_PWREN#†	O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SD3_CD#†	I	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SD3_1P8EN†	O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	

Table 18. Storage Control Cluster (eMMC, SDIO, SD) Interface Signals (Sheet 2 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
SD3_WP†	I	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SD3_RCOMP	-	-	VSDIO					

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.
NOTE: VSDIO voltage selection is controlled by SD3_1P8EN. 3.3V is default due to pull-down. VSDIO can be either 1.8 or 3.3 V when these VSDIO referenced signals are configured to be GPIO's to meet different platform requirements.

2.17 SIO – High Speed UART Interface Signals

See Chapter 27, "SIO – High Speed UART" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 19. High Speed UART Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
SIO_UART1_RXD†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_UART1_TXD†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_UART1_RTS#†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_UART1_CTS#†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_UART2_RXD†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_UART2_TXD†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_UART2_RTS#†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_UART2_CTS#†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.18 SIO – I^{2}C Interface Signals

See Chapter 26, "SIO - I^{2}C Interface" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 20. SIO - I^{2}C Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				Notes
				S4/S5	S3	Reset	Enter S0	
SIO_I2C0_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C0_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C1_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C1_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C2_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C2_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C3_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C3_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C4_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C4_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C5_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C5_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C6_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_I2C6_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.19 SIO – Serial Peripheral Interface (SPI) Signals

See Chapter 25, "SIO - Serial Peripheral Interface (SPI)" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 21. SIO - Serial Peripheral Interface (SPI) Signals (Sheet 1 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State				Notes
				S4/S5	S3	Reset	Enter S0	
SIO_SPI_CLK†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down	
SIO_SPI_CS#†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	

Table 21. SIO - Serial Peripheral Interface (SPI) Signals (Sheet 2 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
SIO_SPI_MOSI†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
SIO_SPI_MISO†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.20 PCU – iLB – Real Time Clock (RTC) Interface Signals

See Chapter 36, "PCU – iLB – Real Time Clock (RTC)" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 22. PCU - iLB - Real Time Clock (RTC) Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
ILB_RTC_X1	I	-	VRTC	Running	Running	Running	Running	
ILB_RTC_X2	O	-	VRTC	Running	Running	Running	Running	
ILB_RTC_RST#	I	-	VRTC	V_{IH}	V_{IH}	V_{IH}	V_{IH}	
ILB_RTC_TEST#	I	-	VRTC	V_{IH}	V_{IH}	V_{IH}	V_{IH}	
ILB_RTC_EXTPAD	O	-	VRTC					

2.21 PCU – iLB – Low Pin Count (LPC) Bridge Interface Signals

See Chapter 35, "PCU – iLB – Low Pin Count (LPC) Bridge" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Note: If the VGA interface is used, VLPC must have a nominal voltage of 3.3V.

Table 23. PCU - iLB - LPC Bridge Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State: S4/S5	S3	Reset	Enter S0	Notes
ILB_LPC_AD[3:0]†	I/O	20k(H)	VLPC	Off	Off	Pull-up	Running	
ILB_LPC_FRAME#†	I/O	20k(H)	VLPC	Off	Off	V_{OH}	Running	
ILB_LPC_SERIRQ†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Running	
ILB_LPC_CLKRUN#†	I/O	20k(H)	VLPC	Off	Off	Pull-up	Running	
ILB_LPC_CLK[1:0]†	I/O	20k(L)	VLPC	Off	Off	V_{OL}	Running	
LPC_RCOMP	-		VLPC					

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.22 PCU – Serial Peripheral Interface (SPI) Signals

See Chapter 31, "PCU – Serial Peripheral Interface (SPI)" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 24. PCU - Serial Peripheral Interface (SPI) Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State: S4/S5	S3	Reset	Enter S0	Notes
PCU_SPI_CLK	O	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Running	
PCU_SPI_CS[0]#	O	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Running	
PCU_SPI_CS[1]#†	O	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Running	
PCU_SPI_MOSI	I/O	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
PCU_SPI_MISO	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.23 PCU – System Management Bus (SMBus) Interface Signals

See Chapter 33, "PCU – System Management Bus (SMBus)" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 25. PCU - System Management Bus (SMBus) Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	
PCU_SMB_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
PCU_SMB_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
PCU_SMB_ALERT#†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	

2.24 PCU – Power Management Controller (PMC) Interface Signals

See Chapter 30, "PCU – Power Management Controller (PMC)" for more details.

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 26. PCU - Power Management Controller (PMC) Interface Signals (Sheet 1 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
PMC_PLTRST#	O	-	V1P8A	V_{OL}	V_{OL}	V_{OL}->V_{OH}	V_{OH}	
PMC_PWRBTN#†	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
PMC_RSTBTN#	I	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up	
PMC_SUSPWRDNACK†	O	-	V1P8A	V_{OH}/V_{OL}	V_{OH}/V_{OL}	V_{OH}/V_{OL}	V_{OH}/V_{OL}	
PMC_SUS_STAT#†	O	-	V1P8A	V_{OL}	V_{OL}	V_{OL}	V_{OH}	
PMC_SUSCLK[0]†	O	-	V1P8A	Running	Running	Running	Running	
PMC_SUSCLK[3:1]†	O	-						
PMC_SLP_S3#	O	-	V1P8A	V_{OL}	V_{OL}	V_{OH}	V_{OH}	
PMC_SLP_S4#	O	-	V1P8A	V_{OL}	V_{OH}	V_{OH}	V_{OH}	
PMC_WAKE_PCIE[0]#	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
PMC_WAKE_PCIE[3:1]#†	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
PMC_ACPRESENT	I	20k(L)	V1P8A	High-Z	Pull-down	Pull-down	Pull-down	
PMC_BATLOW#	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	

Table 26. PCU - Power Management Controller (PMC) Interface Signals (Sheet 2 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
PMC_CORE_PWROK	I		VRTC	V_{IL}	V_{IL}	V_{IL}	V_{IH}	
PMC_RSMRST#	I		VRTC	V_{IH}	V_{IH}	V_{IH}	V_{IH}	

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.

2.25 JTAG and Debug Interface Signals

Note: S0ix is not supported for Bay Trail-M/D SKUs and Bay Trail-I SKUs.

Table 27. JTAG and Debug Interface Signals

Signal Name	Dir	Term	Plat. Power	Default Buffer State				
				S4/S5	S3	Reset	Enter S0	Notes
TAP_TCK	I	2k(L)	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down	
TAP_TDI	I	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
TAP_TDO	O	-	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
TAP_TMS	I	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
TAP_TRST#	I	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
TAP_PRDY#	O	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	
TAP_PREQ#	I	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up	

2.26 Miscellaneous Signals

Table 28. Miscellaneous Signals and Clocks (Sheet 1 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State			
				S4/S5	S3	Reset	Enter S0
SVID_DATA	I/O	2k(H)	V1P0S	Off	Off	Pull-up	Pull-up
SVID_CLK	O	2k(H)	V1P0S	Off	Off	Pull-up	Pull-up
SVID_ALERT#	I	2k(H)	V1P0S	Off	Off	Pull-up	Pull-up
PROCHOT#	I/O	2k(H)	V1P0S	Off	Off	Pull-up	Pull-up
ILB_8254_SPKR†	O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
ILB_NMI†	I	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up

Table 28. Miscellaneous Signals and Clocks (Sheet 2 of 2)

Signal Name	Dir	Term	Plat. Power	Default Buffer State			
				S4/S5	S3	Reset	Enter S0
PMC_PLT_CLK[5:0]†	O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_RCOMP	-	-	V1P8S	Off	Off	Active	Active

NOTE: All signals with the "†" symbol are muxed and may not be available without configuration.
NOTE:GPIO_RCOMP provides compensation for the following pins: GPIO_S5[10], PMC_SUSPWRDNACK PMC_SUSCLK[0], GPIO_S5[13], PMC_SLP_S4#, PMC_SLP_S3#, USB_ULPI_RST#, PMC_ACPRESENT, PMC_WAKE_PCIE[0]#, PMC_BATLOW#, PMC_PWRBTN#, PMC_PLTRST#, GPIO_S5[17], PMC_SUS_STAT#, USB_OC[1:0]#, GPIO_S5[09:00], GPIO_S5[30:22], TAP_TCK TAP_TRST#, TAP_TMS, TAP_TDI, TAP_TDO, TAP_PRDY#, TAP_PREQ#

2.27 GPIO Signals

Most GPIO's are configurable via multiplexors. See "Chapter 10, "Ballout and Package Information" for configuration options with the interfaces presented in this chapter.

Table 29. GPIO Signals (Sheet 1 of 5)

Signal Name	Dir	Term	Plat. Power	Default Buffer State			
				S4/S5	S3	Reset	Enter S0
GPIO_S0_SC[000]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[001]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[002]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[003]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[004]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[005]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[006]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[007]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[008]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[009]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[010]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[011]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[012]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[013]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[014]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[015]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[016]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[017]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up

Table 29. GPIO Signals (Sheet 2 of 5)

Signal Name	Dir	Term	Plat. Power	Default Buffer State			
				S4/S5	S3	Reset	Enter S0
GPIO_S0_SC[018]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[019]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[020]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[021]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[022]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[023]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[024]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[025]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[026]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[027]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[028]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[029]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[030]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[031]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[032]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[033]†	I/O	20k,L	VSDIO	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[034]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[035]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[036]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[037]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[038]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[039]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[040]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[041]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[042]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[043]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[044]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[045]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[046]†	I/O	20k,H	VLPC	Off	Off	1	1
GPIO_S0_SC[047]†	I/O	20k,L	VLPC	Off	Off	0	0
GPIO_S0_SC[048]†	I/O	20k,L	VLPC	Off	Off	0	0
GPIO_S0_SC[049]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[050]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[051]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[052]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up

Table 29. GPIO Signals (Sheet 3 of 5)

Signal Name	Dir	Term	Plat. Power	Default Buffer State			
				S4/S5	S3	Reset	Enter S0
GPIO_S0_SC[053]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[054]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[055]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[056]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[057]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[058]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[059]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[060]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[061]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[062]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[063]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[064]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[065]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[066]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[067]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[068]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[069]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[070]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[071]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[072]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[073]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[074]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[075]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[076]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[077]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[078]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[079]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[080]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[081]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[082]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[083]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[084]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[085]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[086]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[087]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up

Table 29. GPIO Signals (Sheet 4 of 5)

Signal Name	Dir	Term	Plat. Power	Default Buffer State			
				S4/S5	S3	Reset	Enter S0
GPIO_S0_SC[088]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[089]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[090]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[091]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[092]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[093]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[094]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[095]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[096]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[097]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[098]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[099]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[100]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[101]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S5[00]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[01]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[02]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[03]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[04]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[05]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[06]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[07]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[08]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[09]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[10]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[11]†	I/O	-	V1P8A	0/1	0/1	0	0/1
GPIO_S5[12]†	I/O	-	V1P8A	T	T	T	T
GPIO_S5[13]†	I/O	-	V1P8A	0	0	0	0/1
GPIO_S5[14]†	I/O	-	V1P8A	0	0	0	0/1
GPIO_S5[15]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[16]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[17]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[18]†	I/O	-	V1P8A	0	0	0	1
GPIO_S5[19]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[20]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up

Table 29. GPIO Signals (Sheet 5 of 5)

Signal Name	Dir	Term	Plat. Power	Default Buffer State S4/S5	S3	Reset	Enter S0
GPIO_S5[21]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[22]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[23]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[24]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[25]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[26]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[27]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[28]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[29]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[30]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[31]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[32]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[33]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[34]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[35]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[36]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[37]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[38]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[39]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[40]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[41]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[42]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[43]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down

2.28 Power And Ground Pins

Power Rail Ball Name Format: [Function]_[Voltage]_[S-State]{_[Filter]}:

- [Function]: The SoC function associated with the power rail.
  — E.g CORE, USB, …
- [Voltage]: The nominal voltage associated with the power rail.
  — E.g. 1P05, 3P3, VCC, …
- [S-State]: The ACPI system state, from S0 to G3, when the this rail is turned off.
- [Filter]: An optional indicator that one or more power rail balls have unique filtering requirements or requirement to be uniquely identified.

Note: The Resume power well is a set of supply rails (where [S-State] = G3) that must be powered even when S3/4/5 states aren't used. The "Resume Well" is also referred to as the "Suspend Power Well", "Always on/SUS", "SUS power", or "SUS well".

Table 30. Power and Ground Pins (Sheet 1 of 2)

Power Rails	Platform Power	Nominal Voltages	First Off State
CORE_V1P05_S3	V1P05S	1.05 V	S3
CORE_VCC_S3	VCC	Variable	S3
CORE_VCC_SENSE	See CORE_VCC_S3		
CORE_VSS_SENSE	-	-	-
DDI_V1P0_S3	V1P0S	1.0 V	S3
DRAM_V1P0_S3	V1P0S	1.0 V	S3
DRAM_V1P35_S3_F1	VSFR	1.35 V	S3
DRAM_VDD_S4	V1P35U	1.35 V	S4
GPIO_V1P0_S3	V1P0S	1.0 V	S3
HDA_LPE_V1P5V1P8_S3	VAUD	1.5/1.8 V	S3
ICLK_V1P35_S3_F1	VSFR	1.35 V	S3
ICLK_V1P35_S3_F2	VSFR	1.35 V	S3
LPC_V1P8V3P3_S3	VLPC	1.8/3.3 V	S3
MIPI_V1P24_S3	V1P24S	1.24 V	S3
MIPI_V1P8_S3	V1P8S	1.8 V	S3
PCIE_SATA_V1P0_S3	VPCIESATA	1.0 V	S3
PCIE_V1P0_S3	VPCIESATA	1.0 V	S3
PCU_V1P8_G3	V1P8A	1.8 V	G3
PCU_V3P3_G3	V3P3A	3.3 V	G3
PMC_V1P8_G3	V1P8A	1.8 V	G3
RTC_VCC	VRTC	2.0-3.0 at SoC V3P3A(pre diode drop)	(normally battery backed)
SATA_V1P0_S3	VPCIESATA	1.0 V	S3
SD3_V1P8V3P3_S3	VSDIO	1.8/3.3 V	S3
SVID_V1P0_S3	V1P0S	1.0 V	S3
UNCORE_V1P0_G3	V1P0A	1.0 V	G3
UNCORE_V1P0_S3	V1P0S	1.0 V	S3
UNCORE_V1P35_S3_F1	VSFR	1.35 V	S3
UNCORE_V1P35_S3_F2	VSFR	1.35 V	S3
UNCORE_V1P35_S3_F3	VSFR	1.35 V	S3

Table 30. Power and Ground Pins (Sheet 2 of 2)

Power Rails	Platform Power	Nominal Voltages	First Off State
UNCORE_V1P35_S3_F4	VSFR	1.35 V	S3
UNCORE_V1P35_S3_F5	VSFR	1.35 V	S3
UNCORE_V1P35_S3_F6	VSFR	1.35 V	S3
UNCORE_V1P8_G3	V1P8A	1.8 V	G3
UNCORE_V1P8_S3	V1P8S	1.8 V	S3
UNCORE_VNN_S3	VNN	Variable	S3
UNCORE_VNN_SENSE	See UNCORE_VNN_S3		
USB_HSIC_V1P24_G3	V1P24A	1.24 V	G3
USB_ULPI_V1P8_G3	V1P8A	1.8 V	G3
USB_V1P0_S3	V1P0S	1.0 V	S3
USB_V1P8_G3	V1P8A	1.8 V	G3
USB_V3P3_G3	VUSB2	3.3 V	G3
USB_VSSA	-	-	-
USB3_V1P0_G3	V1P0A	1.0 V	G3
USB3DEV_V1P0_S3	V1P0S	1.0 V	S3
VGA_V1P0_S3	V1P0S	1.0 V	S3
VGA_V1P35_S3_F1	VSFR	1.35 V	S3
VGA_V3P3_S3	VVGA_GPIO	3.3 V	S3
VSS	-	-	-
VSSA	-	-	-

Note: USB_HSIC_V1P24_G3 pin(s) can be connected to V1P0A platform rail if USB HSIC is not used. MIPI_V1P24_S3 can be grounded if MIPI interfaces (CSI) aren't used.

Note: If the VGA interface is used, LPC_V1P8V3P3_S3 must have a nominal voltage of 3.3V.

2.29 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK. Defaults are based on internal termination.

Table 31. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is inverted 1 = Top address bit is unchanged
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

2.30 Configurable IO: GPIO Muxing

Not all interfaces may be active at the same time. To provide flexibility, some interfaces are muxed with configurable IO balls. An interface's signal is selected by a function number. See Section 10.3, "Ball Name and Function by Location" on page 214 for details of which balls are muxed, and what functions are available by ball.

Note: Configurable IO defaults to function 0 at boot. All configurable IO with GPIO's for function 0 default to input at boot.

2.31 Reserved Pins

Reserved pins are non functional pins. Unless otherwise specified in this document or related collateral, reserved pins should not be connected to anything. RSVD_GND pins must be connect to the common ground plane (VSS), but don't provide a return path for currents.

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3 Register Access Methods

There are six different common register access methods:

- Fixed IO Register Access
- Fixed Memory Mapped Register Access
- IO Referenced Register Access
- Memory Referenced Register Access
- PCI Configuration Register Access (Indirect - via Memory or IO registers)
- Message Bus Register Access (Indirect - via PCI Configuration Registers)

3.1 Fixed IO Register Access

Fixed IO registers are accessed by specifying their 16-bit address in a PORT IN and/or PORT OUT transaction from the CPU core. This allows direct manipulation of the registers. Fixed IO registers are unmovable register in IO space.

Table 32. Fixed IO Register Access Method Example (P80 Register)

Type: I/O Register (Size: 32 bits)	**P80:** 80h

3.2 Fixed Memory Mapped Register Access

Fixed Memory Mapped IO (MMIO) registers are accessed by specifying their 32/36-bit address in a memory transaction from the CPU core. This allows direct manipulation of the registers. Fixed MMIO registers are unmovable registers in memory space.

Table 33. Fixed Memory Mapped Register Access Method Example (IDX Register)

Type: Memory Mapped I/O Register (Size: 32 bits)	**IDX:** FEC00000h

3.3 IO Referenced Register Access

IO referenced registers use programmable base address registers (BARs) to select a range of IO addresses that it will use to decode PORT IN and/or PORT OUT transactions from the CPU to directly access a register. Thus, the IO BARs act as pointers to blocks of actual IO registers. To access an IO referenced register for a specific IO base address, start with that base address and add the register's offset. Example pseudo code for an IO referenced register read is shown below:

```
Register_Snapshot = IOREAD([IO_BAR]+Register_Offset)
```

Base address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other base address register types may include fixed memory registers, fixed IO registers or message bus registers.

Table 34. Referenced IO Register Access Method Example (HSTS Register)

Type: I/O Register (Size: 8bits)	**HSTS:** [_IOBAR] + 0h **_IOBAR Type:** PCI Configuration Register (Size: 32 bits) **_IOBAR Reference:** [B:0, D:31, F:3] + 20h

3.4 Memory Referenced Register Access

The SoC uses programmable base address registers (BARs) to set a range of physical address (memory) locations that it will use to decode memory reads and writes from the CPU to directly access a register. These BARs act as pointers to blocks of actual memory mapped IO (MMIO) registers. To access a memory referenced register for a specific base address, start with that base address and add the register's offset. Example pseudo code for a read is shown below:

```
Register_Snapshot = MEMREAD([Mem_BAR]+Register_Offset)
```

Base address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other common base address register types include fixed memory registers and IO registers that point to MMIO register blocks.

Table 35. Memory Mapped Register Access Method Example (_MBAR Register)

Type: Memory Mapped I/O Register (Size: 8bits)	**HSTS:** [_MBAR] + 0h **_MBAR Type:** PCI Configuration Register (Size: 32 bits) **_MBAR Reference:** [B:0, D:31, F:3] + 10h

3.5 PCI Configuration Register Access

Access to PCI configuration space registers is performed through one of two different configuration access methods (CAMs):

- IO indexed - PCI CAM
- Memory mapped - PCI Enhanced CAM (ECAM)

Each PCI function has a standard PCI header consisting of 256 bytes for the IO access scheme (CAM), or 4096 bytes for the enhanced memory access method (ECAM). Invalid read accesses return binary strings of 1s.

Table 36. PCI Register Access Method Example (VID Register)

Type: PCI Configuration Register (Size: 16bits)	**VID:** [B:0, D:31, F:3] + 0h

3.5.1 PCI Configuration Access - CAM: IO Indexed Scheme

Accesses to configuration space using the IO method relies on two 32-bit IO registers:

- **CONFIG_ADDRESS** - IO Port CF8h
- **CONFIG_DATA** - IO Port CFCh

These two registers are both 32-bit registers in IO space. Using this indirect access mode, software uses CONFIG_ADDRESS (CF8h) as an index register, indicating which configuration space register to access, and CONFIG_DATA (CFCh) acts as a window to the register pointed to in CONFIG_ADDRESS. Accesses to CONFIG_ADDRESS (CF8h) are internally captured. Upon a read or write access to CONFIG_DATA (CFCh), configuration cycles will be generated to the PCI function specified by the address captured in CONFIG_ADDRESS. The format of the address is shown below.

Table 37. PCI CONFIG_ADDRESS Register (IO PORT CF8h) Mapping

Field	CONFIG_ADDRESS Bits
Enable PCI Config. Space Mapping	31
Reserved	30:24
Bus Number	23:16
Device Number	15:11
Function Number	10:08
Register/Offset Number	07:02

Note: Bit 31 of CONFIG_ADDRESS must be set for a configuration cycle to be generated.

Pseudo code for a PCI register read is shown below:

- MyCfgAddr[23:16] = bus; MyCfgAddr[15:11] = device; MyCfgAddr[10:8] = funct;
- MyCfgAddr[7:2] = dWordMask(offset); MyCfgAddr[31] = 1;
- IOWRITE(0xCF8, MyCfgAddr)
- Register_Snapshot = IOREAD(0xCFC)

3.5.2 PCI Configuration Access - ECAM: Memory Mapped Scheme

A flat, 256 MiB memory space may also be allocated to perform configuration transactions. This is enabled through the BUNIT.BECREG message bus register (Port: 3h, Register: 27h) found in the SoC Transaction Router. BUNIT.BECREG allows remapping this 256 MiB region anywhere in physical memory space. Memory accesses within the programmed MMIO range result in configuration cycles to the appropriate PCI devices specified by the memory address as shown below.

Table 38. PCI Configuration Memory Bar Mapping

ECAM Memory Address Field	ECAM Memory Address Bits
Use from BAR: BUNIT.BECREG[31:28]	31:28
Bus Number	27:20
Device Number	19:15
Function Number	14:12
Register Number	11:02

Note: ECAM accesses are only possible when BUNIT.BECREG.ECENABLE (bit 0) is set.

Pseudo code for an enhanced PCI configuration register read is shown below:

- MyCfgAddr[27:20] = bus; MyCfgAddr[19:15] = device; MyCfgAddr[14:12] = funct;
- MyCfgAddr[11:2] = dw_offset; MyCfgAddr[31:28] = BECREG[31:28];
- Register_Snapshot = MEMREAD(MyCfgAddr)

3.6 Message Bus Register Access

Accesses to the message bus space is through the SoC Transaction Router's PCI configuration registers. This unit relies on three 32-bit PCI configuration registers to generate messages:

- Message Bus Control Register (MCR) - PCI[B:0,D:0,F:0] + D0h
- Message Data Register (MDR) - PCI[B:0,D:0,F:0] + D4h
- Message Control Register eXtension (MCRX) - PCI[B:0,D:0,F:0] + D8h

This indirect access mode is similar to PCI CAM. Software uses the MCR/MCRX as an index register, indicating which message bus space register to access (MCRX only when required), and MDR as the data register. Writes to the MCR trigger message bus transactions.

Writes to MCRX and MDR will be captured. Writes to MCR will generate an internal 'message bus' transaction with the opcode and target (port, offset, bytes) specified in the MCR and the captured MCRX. When a write opcode is specified in MCR, the data that was captured by MDR is used for the write. When a data read opcode is specified in MCR, the data will be available in the MDR register after the MCR write completes (non-posted). The format of MCR and MCRX are shown below.

Table 39. MCR Description (Sheet 1 of 2)

Field	MBPR Bits
OpCode (typically 10h for read, 11h for write)	31:24

Table 39. MCR Description (Sheet 2 of 2)

Field	MBPR Bits
Port	23:16
Offset/Register	15:08
Byte Enable	07:04

Table 40. MCRX Description

Field	MBPER Bits
Offset/Register Extension. This is used for messages sent to end points that require more than 8 bits for the offset/register. These bits are a direct extension of MCR[15:8].	31:08

Most message bus registers are located in the SoC Transaction Router. The default opcode messages for those registers are as follows:

- Message 'Read Register' Opcode: 06h
- Message 'Write Register' Opcode: 07h

Registers with different opcodes will be specified as applicable. Pseudo code of a message bus register read is shown below (where ReadOp==0x06):

- MyMCR[31:24] = ReadOp; MyMCR[23:16] = port; MyMCR[15:8] = offset;
- MyMCR[7:4] = 0xf
- PCIWRITE(0, 0, 0, 0xD0, MyMCR)
- Register_Snapshot = PCIREAD(0, 0, 0, 0xD4)

3.7 Register Field Access Types

Table 41. Register Access Types and Definitions (Sheet 1 of 2)

Access Type	Meaning	Description
RO	Read Only	In some cases, if a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
WO	Write Only	In some cases, if a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
R/W	Read/Write	A register with this attribute can be read and written.

Table 41. Register Access Types and Definitions (Sheet 2 of 2)

Access Type	Meaning	Description
R/WC	Read/Write Clear	A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.
R/WO	Read/Write-Once	A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
R/WLO	Read/Write, Lock-Once	A register bit with this attribute can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.
Default	Default	When the processor is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the processor registers accordingly.

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4 Mapping Address Spaces

The SoC supports four different address spaces:

- Physical Address Space Mappings
- IO Address Space
- PCI Configuration Space
- Message Bus Space

The CPU core can only directly access *memory space* through memory reads and writes and *IO space* through the IN and OUT IO port instructions. *PCI configuration space* is indirectly accessed through IO or memory space, and the *Message Bus space* is accessed through PCI configuration space. See Chapter 3, "Register Access Methods" for details.

This chapter describes how the memory, IO, PCI and Message Bus spaces are mapped to interfaces in the SoC.

Note: See Chapter 13, "SoC Transaction Router" for registers specified in the chapter.

4.1 Physical Address Space Mappings

There are 64 GB (36-bits) of physical address space that can be used as:

- Memory Mapped IO (MMIO - IO fabric)
- Physical Memory (DRAM)

The CPU core can access the full physical address space, while downstream devices can only access SoC DRAM, and each CPU core's local APIC. Peer to peer transactions are not supported.

Most devices map their registers and memory to the physical address space. This chapter summarizes the possible mappings.

4.1.1 SoC Transaction Router Memory Map

The SoC Transaction Router maps the physical address space as follows:

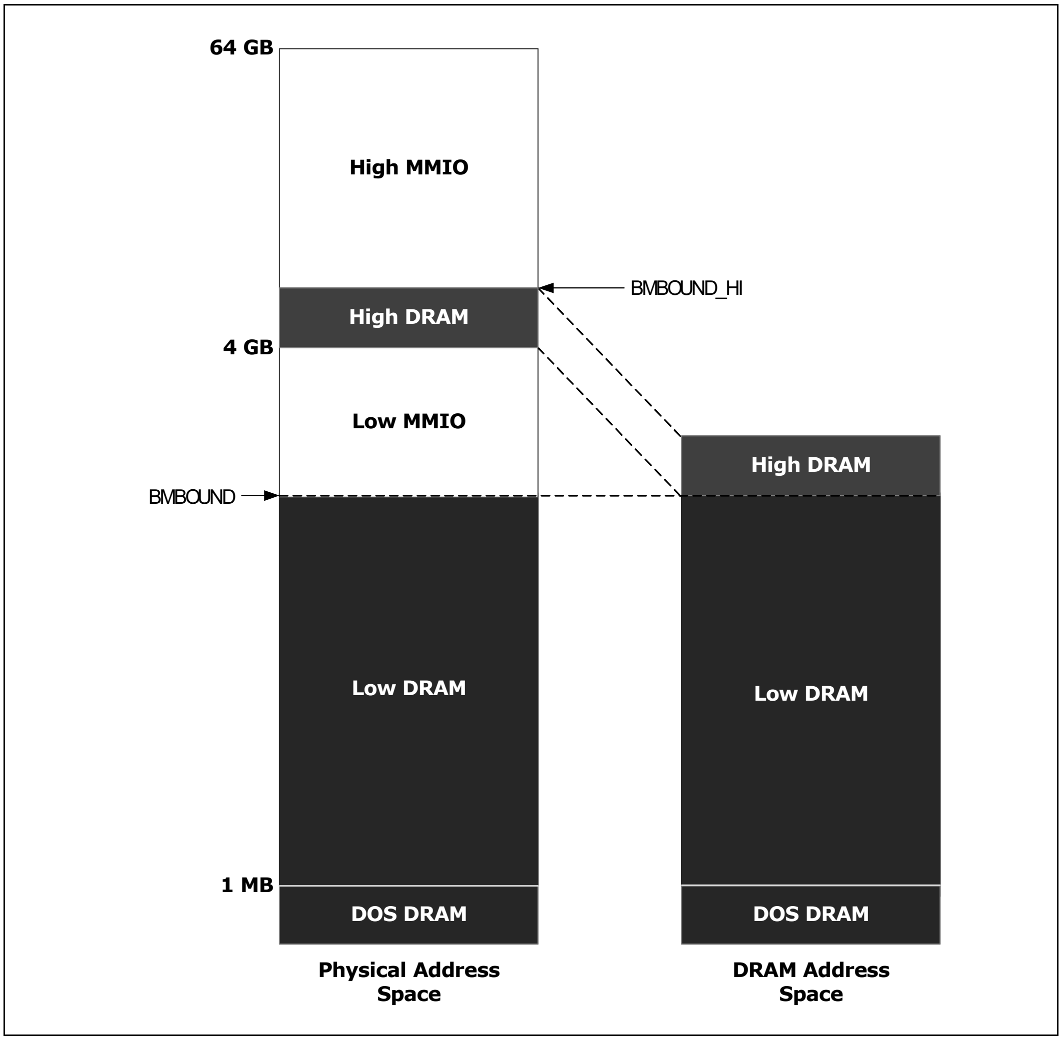
- CPU core to DRAM
- CPU core to IO fabric (MMIO)
- CPU core to extended PCI registers (ECAM accesses)
- IO fabric to CPU cores (local APIC interrupts)

Although 64 GB (36-bits) of physical address space is accessible, some MMIO must exist for devices and software with 32-bit limits. Further, all DRAM should remain accessible for devices and software with access to memory above 4 GB. These goals are accomplished by moving a section DRAM to start at the fixed 4 GB boundary, leaving a hole below 4 GB for MMIO. This creates the following distinct memory regions:

- DOS DRAM + Low DRAM
- Low MMIO
- High DRAM
- High MMIO

There are two registers used to create these regions, BMBOUND and BMBOUND_HI. Their use is shown in Figure 4.

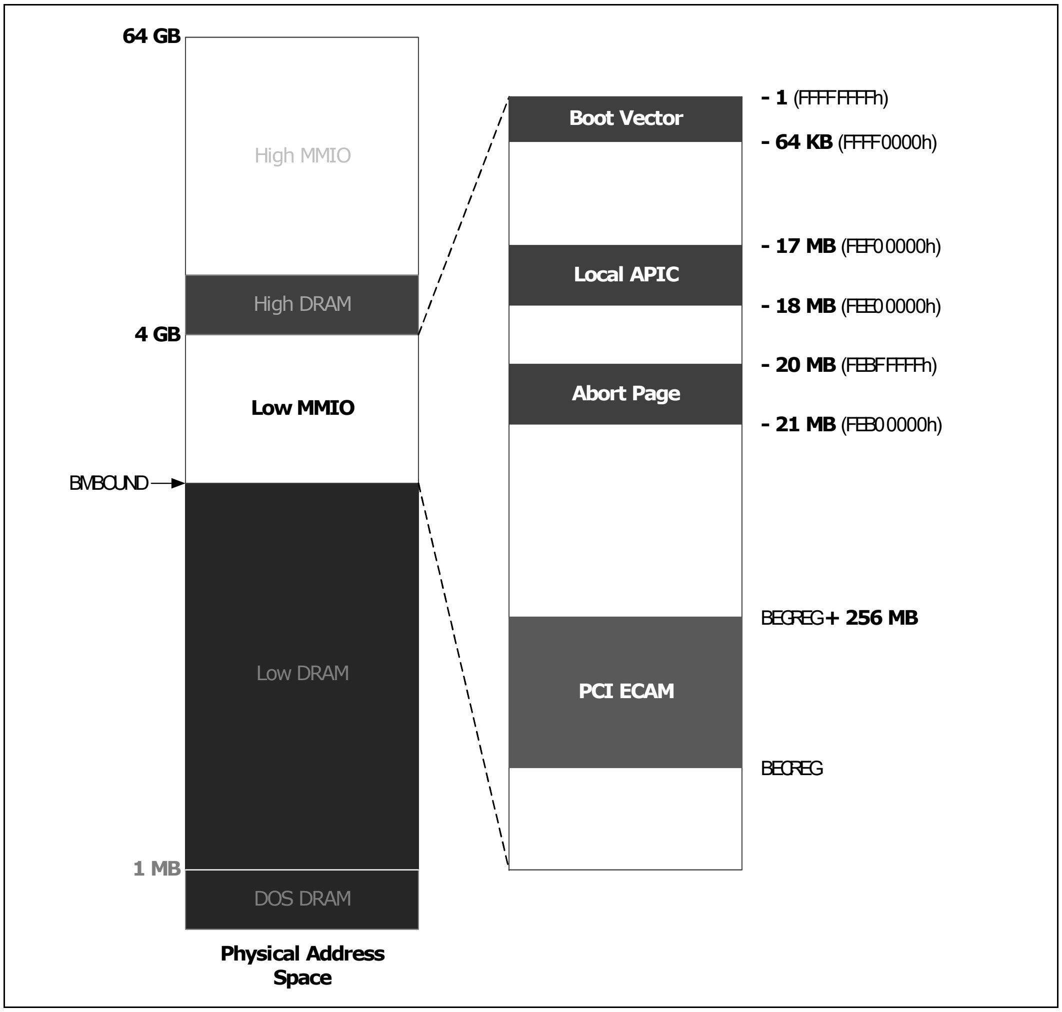
Figure 4. Physical Address Space - DRAM & MMIO



4.1.1.1 Low MMIO

The low MMIO mappings are shown in Figure 5.

Figure 5. Physical Address Space - Low MMIO



By default, CPU core reads targeting the **Boot Vector** range (FFFFFFFFh-FFFF0000h) are sent to the boot Flash connected to the Platform Controller Unit, and write accesses target DRAM. This allows the boot strap CPU core to fetch boot code from the boot Flash, and then shadow that code to DRAM.

Upstream writes from the IO fabric to the **Local APIC** range (FEE00000h-FEF00000h) are sent to the appropriate CPU core's APIC.

Write accesses from a CPU core to the **Abort Page** range (FEB00000h-FEBFFFFFh) will be dropped, and reads will always return all 1's in binary.

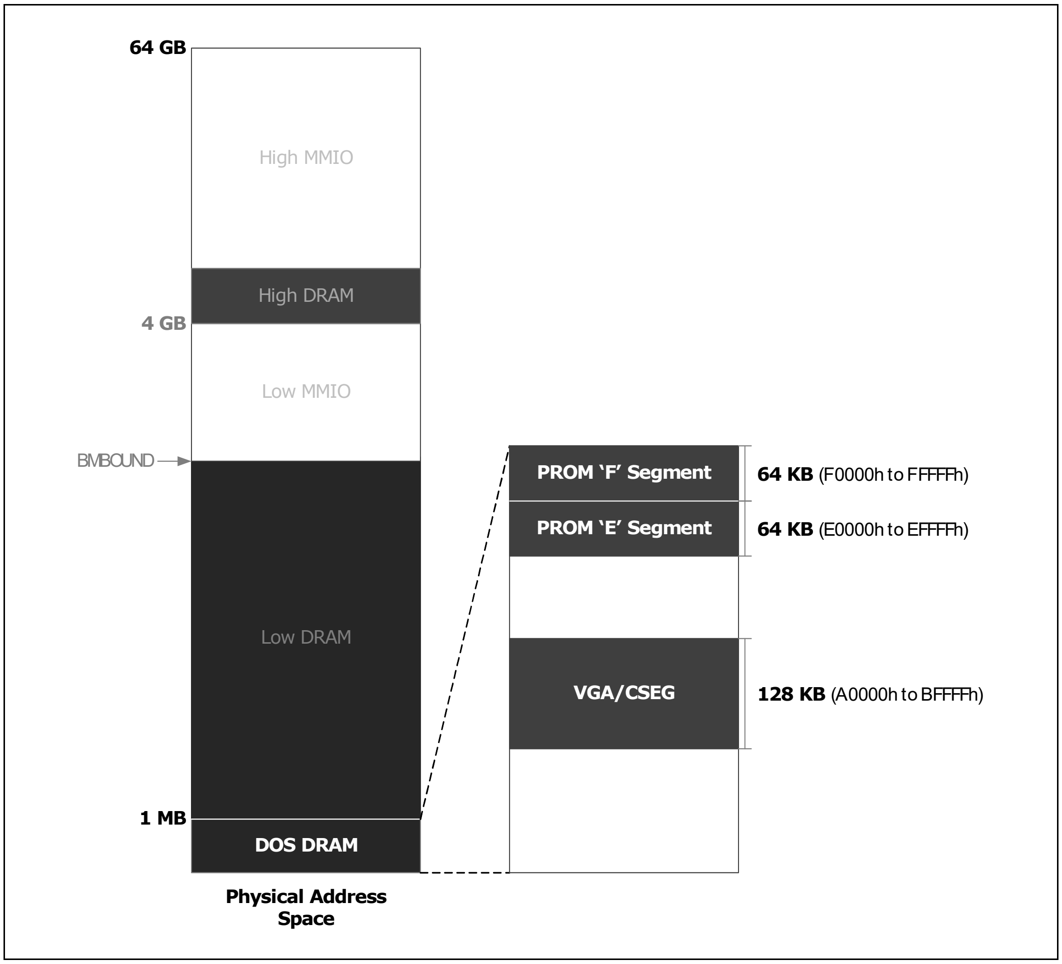
Accesses in the 256 MB **PCI ECAM** range starting at BECREG generate enhanced PCI configuration register accesses when enabled (BECREG.ECENABLE). Unlike traditional memory writes, writes to this range are non-posted when enabled. See Chapter 3, "Register Access Methods" for more details.

All other downstream accesses in the Low MMIO range are sent to the IO Fabric for further decode based on PCI resource allocations. The IO Fabric's subtractive agent (for unclaimed accesses) is the Platform Controller Hub.

4.1.1.2 DOS DRAM

The DOS DRAM is the memory space below 1 MB. In general, accesses from a processor targeting DOS DRAM target system DRAM. Exceptions are shown in the below figure.

Figure 6. Physical Address Space - DOS DRAM



Processor writes to the 64 KB (each) **PROM 'E'** and **'F'** segments (E0000h-EFFFFh and F0000h-FFFFFh) always target DRAM. The BMISC register is used to direct CPU core reads in these two segments to DRAM or the IO fabric (MMIO).

CPU core accesses to the 128 KB **VGA/CSEG** range (A0000h-BFFFFh) can target DRAM or the IO fabric (MMIO). The target is selected with the BMISC.ABSEGINDRAM register.

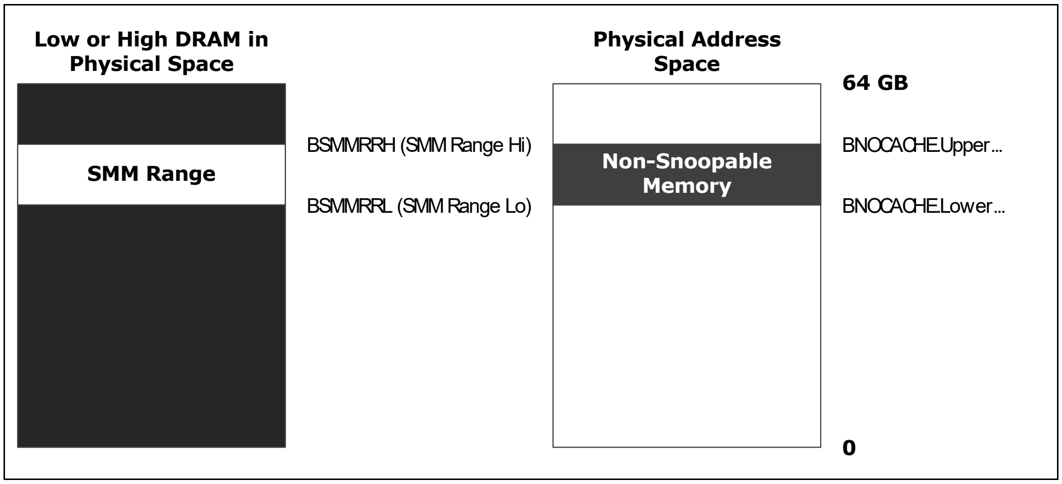
4.1.1.3 Additional Mappings

There are two additional mappings available in the SoC Transaction Router:

- SMM range
- Non-snoop range

Figure 7 shows these mappings.

Figure 7. Physical Address Space - SMM and Non-Snoop Mappings



SMI handlers running on a CPU core execute out of SMM memory. To protect this memory from non-CPU core access, the **SMM Range** (BSMMRRL-BSMMRRH) may be programmed anywhere in low or high DRAM space (1 MB aligned). This range will only allow accesses from the CPU cores.

To prevent snoops of the CPU cores when DMA devices access a specific memory region, the **Non-Snoopable Memory range** (BNOCACHE.Lower-BNOCACHE.Upper) can be programmed anywhere in physical address space. This range is enabled via the BNOCACHECTL register's enable bit (BNOCACHECTL.Enable).

4.1.2 IO Fabric (MMIO) Map

Memory accesses targeting MMIO are routed by the IO fabric to programmed PCI ranges, or routed to the PCU by default (subtractive agent). Programmed PCI ranges can be moved within low or high MMIO, and most can be disabled.

Note: Not all devices can be mapped to high MMIO.

Fixed MMIO is claimed by the Platform Controller Unit (PCU). The default regions are listed below. Movable ranges are not shown. See the register maps of all PCU devices for details.

Table 42. Fixed Memory Ranges in the Platform Controller Unit (PCU)

Device	Start Address	End Address	Comments
Low BIOS (Flash Boot)	000E0000h	000FFFFFh	Starts 128 KB below 1 MB; Firmware/ BIOS
IO APIC	FEC00000h	FEC00040h	Starts 20 MB below 4 GB
HPET	FED40000h	FED003FFh	Starts 19 MB below 4 GB
TPM (LPC)	FED40000h	FED40FFFh	Starts 16 KB above HPET range
High BIOS/Boot Vector	FFFF0000h	FFFFFFFFh	Starts 64 KB below 4 GB; Firmware/ BIOS

The following PCI devices may claim memory resources in MMIO space:

- Graphics/Display (High MMIO capable)
- PCI Express* (High MMIO capable)
- SATA
- SD/MMC/SDIO
- SIO
- HD Audio
- Platform Controller Unit (PCU) (Multiple BARs)
- xHCI USB
- EHCI USB
- USB Device
- LPE/I^{2}S
- ISP/MIPI-CSI

See each device's interface chapter for details.

Warning: Variable memory ranges should not be set to conflict with other memory ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

4.2 IO Address Space

There are 64 KB + 3 bytes of IO space (0h-10002h) for accessing IO registers. Most IO registers exists for legacy functions in the PCU or for PCI devices, while some are claimed by the SoC Transaction Router for graphics and for the PCI configuration space access registers.

4.2.1 SoC Transaction Router IO Map

The SoC claims IO transactions for VGA/Extended VGA found in the display/graphics interface. It also claims the two 32-bit registers at port CF8h and CFCh used to access PCI configuration space.

4.2.2 IO Fabric IO Map

4.2.2.1 PCU Fixed IO Address Ranges

Below table shows the fixed IO space ranges seen by a processor.

Table 43. Fixed IO Ranges in the Platform Controller Unit (PCU)

Device	IO Address	Comments
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39-, 3Ch-3Dh	
8254s	40h-43h, 50h-53h	
PS2 Control	60h, 64h	
NMI Controller	61h, 63h, 65h, 67h	
RTC	70h-77h	
Port 80h	80h-83h	
Init Register	92h	
8259 Slave	A0h-A1h, A4h-A5h, A8h-A9h, ACh-ADh, B0h-B1h, B4h-B5h, B8h-B9h, BCh-BDh, 4D0h-4D1h	
PCU UART	3F8h-3FFh	
Reset Control	CF9h	Overlaps PCI IO registers
Active Power Management	B2h-B3h	

Table 44. Fixed IO Ranges in the SoC Transaction Router, Serial ATA and PCIe* Blocks

Device	IO Address	Comments
SATA Legacy IDE Mode - Secondary Channel Legacy Taskfile Command Block	170h - 177h	
SATA Legacy IDE Mode - Primary Channel Legacy Taskfile Command Block	1F0h - 1F7h	
SATA Legacy IDE Mode - Secondary Channel Legacy Taskfile Control Block	374h - 377h	
SATA Legacy IDE Mode - Primary Channel Legacy Taskfile Control Block	3F4h - 3F7h	
PCI Express*: VGA Legacy Control & Status	3B0h - 3BBh, 3C0h - 3DFh	Only active if `INTR_BCTRL.VE=1b`
PCI Configuration Access Address	CF8h	
PCI Configuration Access Data	CFCh	

4.2.2.2 Variable IO Address Ranges

Table 45 shows the variable IO decode ranges. They are set using base address registers (BARs) or other similar means. Plug-and-play (PnP) software (PCI/ACPI) can use their configuration mechanisms to set and adjust these values.

Warning: The variable IO ranges should not be set to conflict with other IO ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

Table 45. Movable IO Ranges Decoded by PCI Devices on the IO Fabric (Sheet 1 of 2)

Device	Size (bytes)	Target
ACPI Power Management (PCU)	128	ACPI_BASE_ADDR (PM1BLK): PCI[B:0,D:31,F:0] + 40h
SMBus (PCU)	32	SMBA: PCI[B:0,D:31,F:3] + 20h
GPIO (PCU)	256	GBA: PCI[B:0,D:31,F:0] + 48h
RCBA (PCU)	1024	RCRB_BA: PCI[B:0,D:31,F:0] + F0h
Display Controller	8	IOBAR (PCI[B:0,D2,F:0] + 20h)
PCI Express: ISA Legacy	Variable[1]	IOBL_SSTS.IOBA (PCI[B:0,D28,F:0] + 1Ch)
SATA Native & AHCI Mode - Legacy IDE / AHCI Index Data Pair	32	LBAR (PCI[B:0,D19,F:0] + 20h)
SATA Native Mode - Serial ATA Index Data Pair	16	SIDPBA (PCI[B:0,D19,F:0] + 24h)
SATA Native Mode - Primary Command Block	8	PCMDBA (PCI[B:0,D19,F:0] + 10h)

Table 45. Movable IO Ranges Decoded by PCI Devices on the IO Fabric (Sheet 2 of 2)

Device	Size (bytes)	Target
SATA Native Mode - Secondary Command Block	8	SCMDBA (PCI[B:0,D19,F:0] + 18h)
SATA Native Mode - Primary Control Block	4	PCTLBA (PCI[B:0,D19,F:0] + 14h
SATA Native Mode - Secondary Control Block	4	SCTLBA (PCI[B:0,D19,F:0] + 1Ch)

NOTES 1: Size is defined by the configuration of `IOBL_SSTS.IOLA`

4.3 PCI Configuration Space

All PCI devices/functions are shown below. Table below will always take priority.

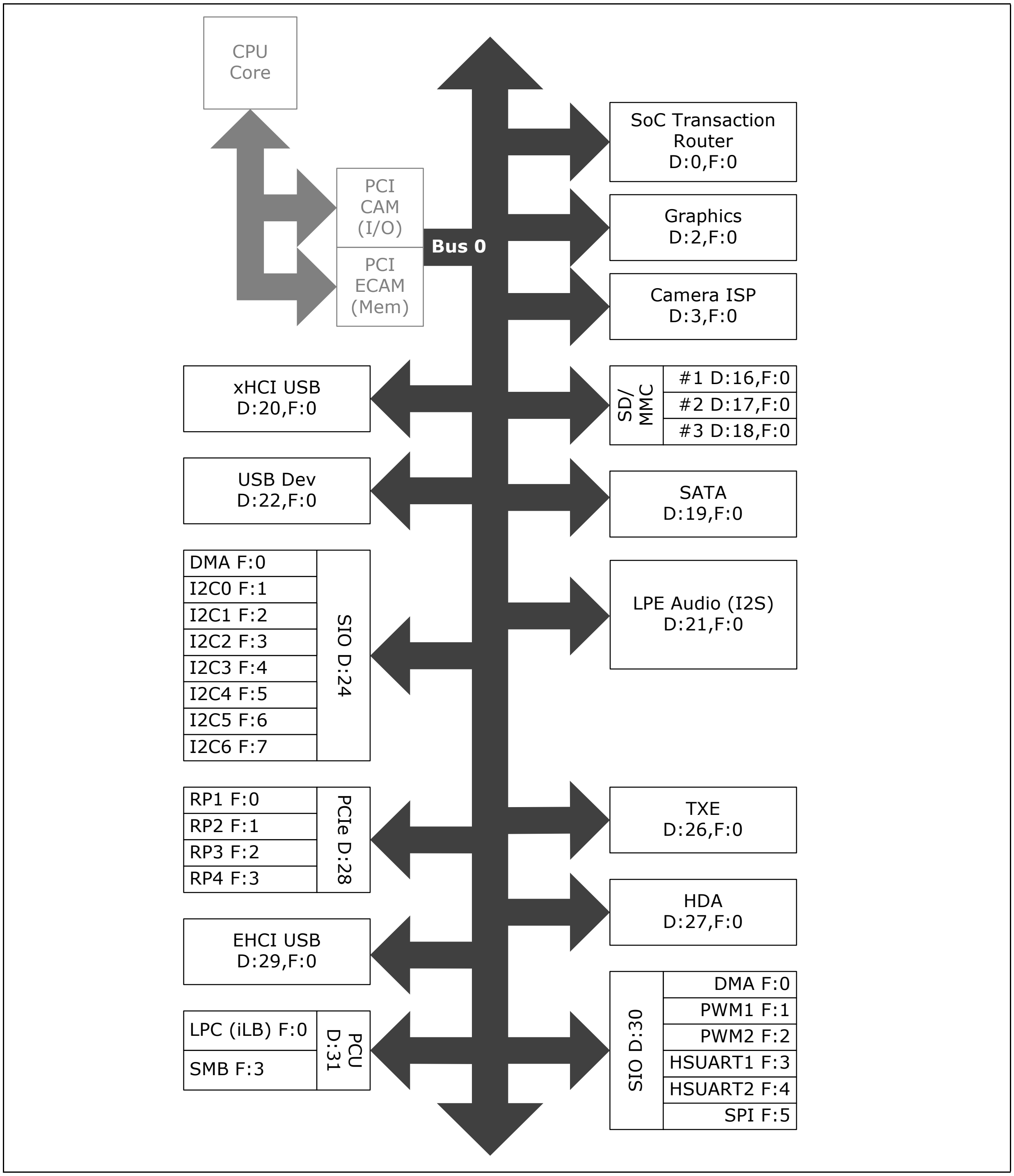
Table 46. PCI Devices and Functions (Sheet 1 of 2)

Bus	Device	Function	Device ID	Device Description	Function Description
0	0	0	0F00h	SoC Transaction Router	
0	2	0	0F31h	Graphics & Display	
0	3	0	0F38h	Camera Image Signal Processor	
0	16	0	0F14h	Storage Control Cluster (SCC)	eMMC Port (de-featured - use Device 23 instead)
0	17	0	0F15h		SDIO Port
0	18	0	0F16h		SD Port
0	19	0	0F20h (IDE) 0F21h (IDE) 0F22h (AHCI) 0F23h (AHCI)	SATA	
0	20	0	0F35h	xHCI USB	
0	21	0	0F28h	Low Power Engine Audio	Host Bridge + three I^2S Ports (0-2)
0	22	0	0F37h	USB Device	
0	23	0	0F50h	Storage Control Cluster (SCC)	eMMC 4.5 Port
0	24	0	0F40h	Serial IO (SIO)	DMA
		1	0F41h		I^2C Port 1
		2	0F42h		I^2C Port 2
		3	0F43h		I^2C Port 3
		4	0F44h		I^2C Port 4
		5	0F45h		I^2C Port 5
		6	0F46h		I^2C Port 6
		7	0F47h		I^2C Port 7
0	26	0	0F18h	Trusted Execution Engine	

Table 46. PCI Devices and Functions (Sheet 2 of 2)

Bus	Device	Function	Device ID	Device Description	Function Description
0	27	0	0F04h	HD Audio	
0	28	0	0F48h	PCI Express*	Root Port 1
		1	0F4Ah		Root Port 2
		2	0F4Ch		Root Port 3
		3	0F4Eh		Root Port 4
0	29	0	0F34h	EHCI USB	
0	30	0	0F06h	Serial IO (SIO)	DMA
		1	0F08h		PWM Port 1
		2	0F09h		PWM Port 2
		3	0F0Ah		HSUART Port 1
		4	0F0Ch		HSUART Port 2
		5	0F0Eh		SPI Port
0	31	0	0F1Ch	Platform Controller Unit	LPC: Bridge to Intel Legacy Block
0	31	3	0F12h	Platform Controller Unit	SMBus Port

Figure 8. Bus 0 PCI Devices and Functions



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5 Integrated Clock

Clocks are integrated, consisting of multiple variable frequency clock domains, across different voltage domains. This architecture achieves a low power clocking solution that supports the various clocking requirements of the SoC's many interfaces.

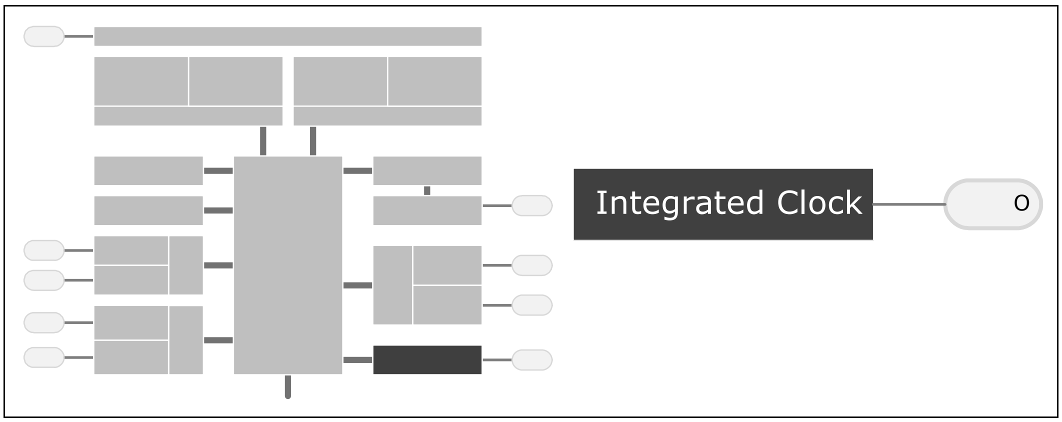
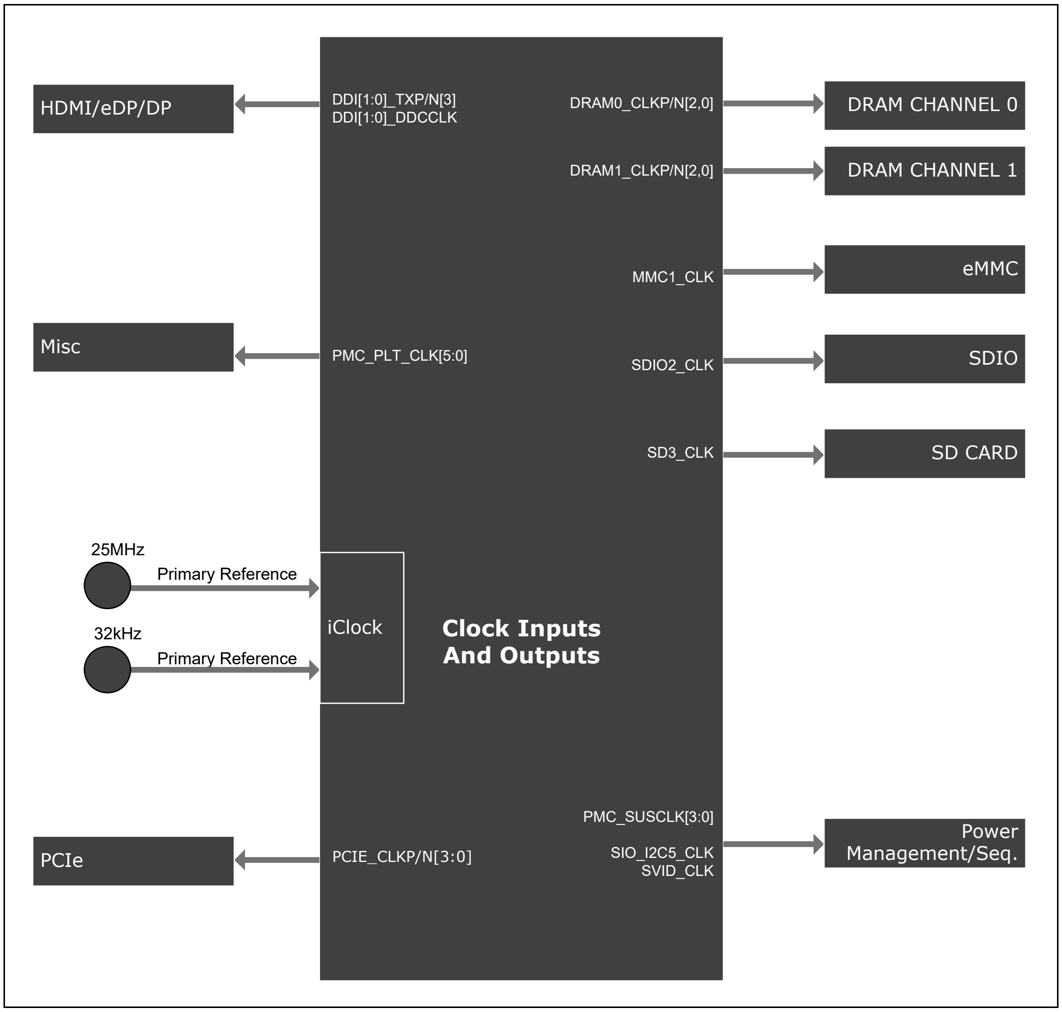


Figure 9. Clocking Example



5.1 Features

Platform clocking is provided internally by the Integrated Clock logic. No external clock chips are required for the SoC to function. All the required platform clocks are provided by two crystal inputs: a 25 MHz primary reference for the integrated clock block and a 32.768 kHz reference for the Real Time Clock (RTC) block.

The different inputs and outputs are listed below.

Table 47. SoC Clock Inputs

Clock Domain	Signal Name	Frequency	Usage/Description
Main	ICLK_OSCIN ICLK_OSCOUT	25 MHz	Reference crystal for the iCLK PLL
RTC	ILB_RTC_X1 ILB_RTC_X2	32.768 kHz	RTC crystal I/O for RTC block
MIPI CSI	MCSI1_CLKP/N MCSI2_CLKP/N MCSI3_CLKP/N	80-500 MHz	Clocks for cameras
LPC	ILB_LPC_CLK[1]	33 MHz	Can be configured as an input to compensate for board routing delays through Soft Strap.
USB PHY	USB_ULPI_CLK	60 MHz	Interface clock from ULPI PHY.

Table 48. SoC Clock Outputs (Sheet 1 of 2)

Clock Domain	Signal Name	Frequency	Usage/Description
Memory	DRAM0_CKP/N[2,0] DRAM1_CKP/N[2,0]	533/667 MHz	Drives the Memory ranks 0-1. Data rate (MT/s) is 2x the clock rate. Note: The frequency is fused in each SoC. It is not possible to support both frequencies on one SoC.
eMMC	MMC1_CLK MMC1_45_CLK	25-50 MHz 25-200 MHz	Clock for eMMC 4.41 devices Clock for eMMC 4.51 devices Actual clock can run as low as 400 kHz during initialization.
SDIO	SD2_CLK	25-50 MHz	Clock for SDIO devices
SD Card	SD3_CLK	25-50 MHz	Clock for SD card devices
SPI	PCU_SPI_CLK	20 MHz, 33 MHz, 50 MHz	Clock for SPI flash
PMIC/COMMS	PMC_SUSCLK[3:0]	32.768 kHz	Pass through clock from RTC oscillator
LPC	ILB_LPC_CLK[0:1]	33 MHz	Provided to devices requiring LPC clock
HDA	HDA_CLK	24 MHz	Serial clock for external HDA codec device
PCI Express	PCIE_CLKN[3:0] PCIE_CLKP[3:0]	100 MHz	Differential Clocks supplied to external PCI express devices based on assertion of PCIE_CLKREQ[3:0]# inputs
USB PHY	USB_ULPI_REFCLK	19.2 MHz	Clock for USB devices
HDMI	DDI[1:0]_TXP/N[3]	25-148.5 MHz	Differential clock for HDMI devices
HDMI DDC	DDI[1:0]_DDCCLK	100 kHz	Clock for HDMI DDC devices

Table 48. SoC Clock Outputs (Sheet 2 of 2)

Clock Domain	Signal Name	Frequency	Usage/Description
VGA DDC	VGA_DDCCLK	100 kHz	Clock for VGA DDC devices
SVID	SVID_CLK	25 MHz	Clock used by voltage regulator
I^2S	LPE_I2S[2:0]_CLK	12.5 MHz	Continuous serial clock for I^2S interfaces
Platform Clocks	PMC_PLT_CLK [5:0]	25 MHz	Platform clocks. For example: PLT_CLK [2:0] - Camera PLT_CLK [3] - Audio Codec PLT_CLK [4] - PLT_CLK [5] - COMMs
SIO SPI	SIO_SPI_CLK	15 MHz	SPI clock output
I^2C	SIO_I2C[6:0]_CLK	100 kHz, 400 kHz, 1 MHz, 3.4 MHz	I^2C clocks Note: In I2C Controller the parameter called IC_CAP_LOADING can be set to 400pf/100pf. As per specification 3.4MHz is supported in 100pf loading while 1.7MHz is the max frequency at 400pf load.
SMBus	PCU_SMB_CLK	10 kHz - 100 kHz	Drives SMBus device

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6 Power Management

This chapter provides information on the following power management topics:

- ACPI States
- Processor Core
- PCI Express
- Integrated Graphics Controller

6.1 Power Management Features

- ACPI System States support (S0, S3, S4, S5)
- Processor Core/ States support (C0 – C6)
- Processor Package States Support (C0-C7)
- SoC Graphics Adapter States support D0 – D3.
- Support Link Power Management (LPM)
- Thermal throttling
- Dynamic I/O power reductions (disabling sense amps on input buffers, tri-stating output buffers)
- Active power down of Display links

6.2 Power Management States Supported

The Power Management states supported by the processor are described in this section.

6.2.1 S-State Definition

6.2.1.1 S0 - Full On

This is the normal operating state of the processor. In S0, the core processor will transition in and out of the various processor C-States and P-States.

6.2.1.2 S3 - Suspend to RAM (Standby)

S3 is a suspend state in which the core power planes of the processor are turned off and the suspend wells remain powered.

- All power wells are disabled, except for the suspend and RTC wells.
- The core processor's macro-state is saved in memory.

- Memory is held in self-refresh and the memory interface is disabled, except the CKE pin as it is powered from the memory voltage rail. CKE is driven low.

6.2.1.3 S4 - Suspend to Disk (Hibernate)

S4 is a suspend state in which most power planes of the processor are turned off, except for the suspend and RTC well. In this ACPI state, system context is saved to the hard disk.

Key features:

- No activity is allowed.
- All power wells are disabled, except for the suspend and RTC well.

6.2.1.4 S5 - Soft Off

From a hardware perspective the S5 state is identical to the S4 state. The difference is purely software; software does not write system context to hard disk when entering S5.

The following table shows the differences in the sleeping states with regards to the processor’s output signals.

Table 49. SoC Sx-States to SLP_S*#

State	S0	S3	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle
CPU Executing	In C0	OFF	OFF	OFF	No	OFF
PMC_SLP_S3#	HIGH	LOW	LOW	LOW	HIGH	LOW
PMC_SLP_S4#	HIGH	HIGH	LOW	LOW	HIGH	LOW
S0 Power Rails	ON	OFF	OFF	OFF	ON	OFF
PMC_PLTRST#	HIGH	LOW	LOW	LOW	LOW	LOW
PMC_SUS_STAT#	HIGH	LOW	LOW	LOW	HIGH	LOW
PCIe Links	L0, L1	L3	L3	L3	L3 Ready	L3

NOTES: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S5#. PMC_SUS_STAT# is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT# also warns of upcoming reset.

6.2.2 System States

Table 50. General Power States for System

States/Sub-states	Legacy Name / Description
G0/S0/C0	**FULL ON:** CPU operating. Individual devices may be shut down to save power. The different CPU operating levels are defined by Cx states.
G0/S0/Cx	**Cx State:** CPU manages C-state itself.
G1/S3	**Suspend-To-RAM(STR):** The system context is maintained in system DRAM, but power is shut to non-critical circuits. Memory is retained, and refreshes continue. All external clocks are shut off; RTC clock and internal ring oscillator clocks are still toggling.
G1/S4	**Suspend-To-Disk (STD):** The context of the system is maintained on the disk. All of the power is shut down except power for the logic to resume. The S4 and S5 states are treated the same.
G2/S5	**Soft-Off:** System context is not maintained. All of the power is shut down except power for the logic to restart. A full boot is required to restart. A full boot is required when waking. The S4 and S5 states are treated the same.
SoC G3	**SoC Mechanical OFF.** System context is not maintained. All power to the SoC is shutdown except for the RTC. All of the power to the rest of the system is shut down except power for the logic to restart. No SoC "Wake" events are possible, because the SoC does not have any power. when SoC power returns, transition will depend on the state just prior to the entry to SoC G3.
G3	**Mechanical OFF.** System is not maintained. All power shutdown except for the RTC. No "Wake" events are possible, because the system does not have any power. This state occurs if the user removes the batteries, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3.

Table 51 shows the transitions rules among the various states. Note that transitions among the various states may appear to temporarily transition through intermediate states. These intermediate transitions and states are not listed in the table.

Table 51. ACPI PM State Transition Rules (Sheet 1 of 2)

Present State	Transition Trigger	Next State
G0/S0/C0	IA Code **MWAIT** or LVL Rd	C0/S0/Cx
	PM1_CNT.SLP_EN bit set	G1/Sx or G2/S5 state (specified by PM1_CNT.SLP_TYP)
	Power Button Override	G2/S5
	Mechanical Off/Power Failure	G3

Table 51. ACPI PM State Transition Rules (Sheet 2 of 2)

Present State	Transition Trigger	Next State
G0/S0/Cx	Cx break events which include: CPU snoop, MSI, Legacy Interrupt, AONT timer	G0/S0/C0
	Power Button Override	G2/S5
	System Power Failure	G3
G1/S3,G1/S4	Any Enabled Wake Event	G0/S0/C0
	Power button Override	G2/S5
	Resume Well Power Failure	G3
G2/S5	Any Enabled Wake Event	G0/S0/C0
	Resume Well Power Failure	G3
G3	Power Returns	Option to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other enabled wake event) or G1/S4 (if system state was S4 prior to the power failure). Some wake events are preserved through a power failure.

6.2.3 Processor States

Table 52. Processor Core/ States Support

State	Description
C0	Active mode, processor executing code
C1	AutoHALT state
C6	Deep Power Down. Prior to entering the Deep Power Down Technology (code named C6) State, The core process will flush its cache and save its core context to a special on die SRAM on a different power plane. Once Deep Power Down Technology (code named C6) sequence has completed. The core processor's voltage is completely shut off.

6.2.4 Integrated Graphics Display States

Table 53. SoC Graphics Adapter State Control

State	Description
D0	Full on, Display active
D3	Power off display

6.2.5 Integrated Memory Controller States

Table 54. Main Memory States

States	Description
Powerup	CKE asserted. Active mode.
Precharge Powerdown	CKE de-asserted (not self-refresh) with all banks closed.
Active Powerdown	CKE de-asserted (not self-refresh) with at least one bank active.
Self-Refresh	CKE de-asserted using device self-refresh

6.2.6 PCI Express* (PCIe*) States

Table 55. PCI Express* States

States	Description
L0	Full on – Active transfer state
L0s	First Active Power Management low power state – Low exit latency
L1	Lowest Active Power Management - Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

6.2.7 Interface State Combinations

Table 56. G, S and C State Combinations

Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1	Auto-Halt	On	Auto-Halt
G0	S0	C6	Deep Power Down	On	Deep Power Down
G1	S3	Power off		Off except RTC & internal ring OSC	Suspend to RAM
G1	S4	Power off		Off except RTC & internal ring OSC	Suspend to Disk
G2	S5	Power off		Off except RTC & internal ring OSC	Soft Off
G3	NA	Power Off		Power off	Hard Off

Table 57. D, S and C State Combinations

Graphics Adapter (D) State	Sleep (S) State	(C) State	Description
D0	S0	C0	Full On, Displaying
D0	S0	C1	Auto-Halt, Displaying
D0	S0	C6	Deep Sleep, Display Off
D3	S0	Any	Not Displaying
D3	S3		Not Displaying Graphics Core power off.
D3	S4		Not Displaying Suspend to disk Core power off

NOTE:S0ix is not supported for Bay Trail-M/D and Bay Trail-I.

6.3 Processor Core Power Management

While executing code, Enhanced Intel SpeedStep® Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

6.3.1 Enhanced Intel SpeedStep® Technology

The following are the key features of Enhanced Intel SpeedStep® Technology:

- Applicable to Processor Core Voltage and Graphic Core Voltage
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency:
  - If the target frequency is higher than the current frequency, Core_VCC_S3 is ramped up slowly to an optimized voltage. This voltage is signaled by the SVID signals to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the SVID signals.
- The processor controls voltage ramp rates by requesting appropriate ramp rates from an external SVID controller.
- Because there is low transition latency between P-states, a significant number of transitions per second are possible.

- Thermal Monitor mode.
  — Refer to Chapter 8, "Thermal Management"

6.3.2 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following condition:

- The C0 timer that tracks continuous residency in the Normal state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The predefined L2 shrink threshold is triggered.

The number of L2 cache ways disabled upon each Deeper Sleep entry is configured in the BBL_CR_CTL3 MSR. The C0 timer is referenced through the CLOCK_CORE_CST_CONTROL_STT MSR. The shrink threshold under which the L2 cache size is reduced is configured in the PMG_CST_CONFIG_CONTROL MSR. If the ratio is zero, then the ratio will not be taken into account for Dynamic Cache Sizing decisions. Refer to the BIOS Writer's Guide for more details.

6.3.3 Low-Power Idle States

When the processor core is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-state. However, higher C-states have longer exit and entry latencies. Resolution of C-state occur at the thread, processor core, and processor core level.

6.3.3.1 Clock Control and Low-Power States

The processor core supports low power states at core level. The central power management logic ensures the entire processor core enters the new common processor core power state. For processor core power states higher than C1, this would be done by initiating a P_LVLx (P_LVL6) I/O read to all of the cores. States that require external intervention and typically map back to processor core power states. States for processor core include Normal (C0, C1).

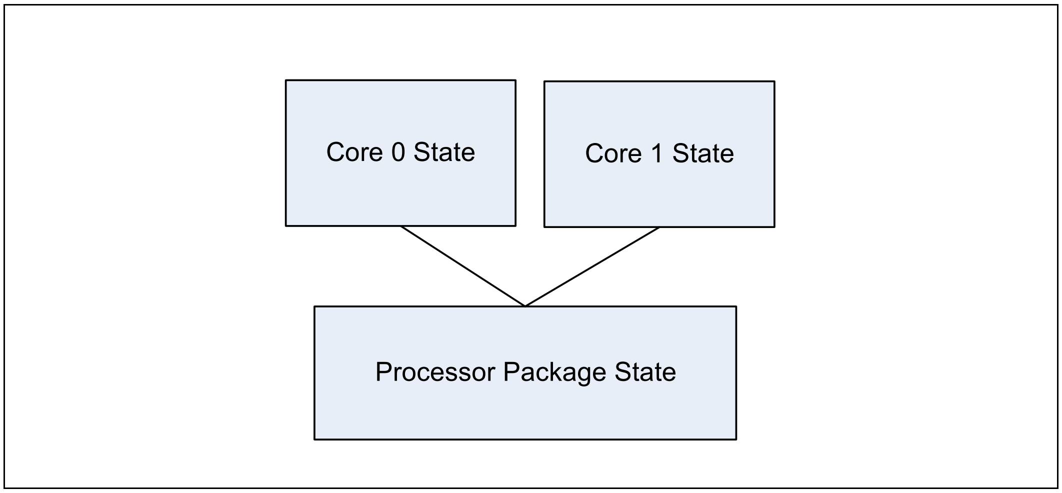
The processor core implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state specifies and P_LVLx reads to the ACPI P_BLK register block mapped in the processor core's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor core and do not directly result in I/O reads on the processor core bus. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state specifications used for each P_LVLx read can be configured in a software programmable MSR by BIOS.

The Cx state ends due to a break event. Based on the break event, the processor returns the system to C0. The following are examples of such break events:

- Any unmasked interrupt goes active

- Any internal event that will cause an NMI or SMI_B
- CPU Pending Break Event (PBE_B)
- MSI

Figure 10. Idle Power Management Breakdown of the Processor Cores



6.3.4 Processor Core C-States Description

The following state descriptions assume that both threads are in common low power state.

6.3.4.1 Core C0 State

The normal operating state of a core where code is being executed.

6.3.4.2 Core C1 State

C1 is a low power state entered when a core execute a HLT or MWAIT(C1) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1 state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide* for more information.

While a core is in C1 state, it processes bus snoops and snoops from other threads.

6.3.4.3 Core C6 State

Individual core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.

There are various types of C-state:

- C6NS implies only the core should be powergated, but the L2 cache contents should be retained.
- C6FS implies the core should be powergates, and the L2 cache can be fully flushed to get even more power savings.

6.3.5 Package C-States

The processor supports package C0, C6 and C7 power states. The following is a summary of the general rules for package C-state entry. These apply to all package Cstates unless specified otherwise:

- Package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
- Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
- The platform may allow additional power savings to be realized in the processor.
- For package C-states, the processor is not required to enter C0 before entering any other C-state.
- Entry in to a package C-state may be subject to auto-demotion - that is the processor may keep the package in a shallower package C-state then requested by the OS if the processor determines via heuristics that the shallower C-state results in better power/performance.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  - If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.
  - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

Table 58. Coordination of Module and Core Power States at the Package Level

Module C-State		Core/Module 1: C0	C1	C6NS	C6FS
Core 0	C0	C0	C0	C0	C0
	C1	C0	C0	C0	C0
	C6NS	C0	C0	C0	C6c
	C6FS	C0	C0	C6C	C6

Package C-State		Core/Module 1: C0	C6C	C6
Module 0	C0	C0	C0	C0
	C6C	C0	C6C	C6C
	C6	C0	C6C	C7

NOTE:

1. 2 Cores of the SoC will make up one module.

6.3.5.1 Package C0

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

6.3.5.2 Package C1

No additional power reduction actions are taken in the package C1 state.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

No notification to the system occurs upon entry to C1.

6.3.5.3 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.

- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.
- The platform has allowed a package C6 state.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts.

6.3.6 Graphics Power Management

6.3.6.1 Graphics and video decoder C-State

GFX C-State (GC6) and VED C-state (VC6) are designed to optimize the average power to the graphics and video decoder engines during times of idleness. GFX C-state is entered when the graphics engine, has no workload being currently worked on and no outstanding graphics memory transactions. VED S-state is entered when the video decoder engine has no workload being currently worked on and no outstanding video memory transactions. When the idleness condition is met, the processor will power gate the Graphics and video decoder engines.

6.3.6.2 Intel® Display Power Saving Technology (Intel® DPST)

The Intel DPST technique achieves backlight power savings while maintaining visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel® DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)
2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image. Intel DPST 5.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

6.3.6.3 Intel® Automatic Display Brightness

The Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the back light setting.

6.3.6.4 Intel® Seamless Display Refresh Rate Switching Technology (Intel® SDRRS Technology)

When a Local Flat Panel (LFP) supports multiple refresh rates, the Intel® Display Refresh Rate Switching power conservation feature can be enabled. The higher refresh rate will be used when on plugged in power or when the end user has not selected/enabled this feature. The graphics software will automatically switch to a lower refresh rate for maximum battery life when the design application is on battery power and when the user has selected/enabled this feature.

There are two distinct implementations of Intel SDRRS—static and seamless. The static Intel SDRRS method uses a mode change to assign the new refresh rate. The seamless Intel SDRRS method is able to accomplish the refresh rate assignment without a mode change and therefore does not experience some of the visual artifacts associated with the mode change (SetMode) method.

6.4 Memory Controller Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

6.4.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as DIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tristated with an SO-DIMM present, the DIMM is not guaranteed to maintain data integrity.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

6.4.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals, which the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

6.4.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that is recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power- up.

CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is guaranteed to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

6.4.2.2 Conditional Self-Refresh

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh in the package C3 and C6 low-power states. RMPM functionality depends on graphics/display state (relevant only when internal graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

When entering the Suspend-to-RAM (STR) state, the processor core flushes pending cycles and then places all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for the package C3 and C6 states as long as there are no memory requests to service.

6.4.2.3 Dynamic Power Down Operation

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power down state.The processor core controller can be configured to put the devices in active power down (CKE deassertion with open pages) or precharge power down (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

6.4.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks can be controlled on a per SO-DIMM basis. Exceptions are made for per SO-DIMM control signals such as CS#, CKE, and ODT for unpopulated SO-DIMM slots.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

6.5 PCI Express* (PCIe*) Power Management

- Active power management support using L0s, and L1 states.
- All inputs and outputs disabled in L3 Ready state.

§

7 Power Up and Reset Sequence

This chapter provides information on the following topics:

- "Power Up Sequences"
- "Power Down Sequences"
- "Reset Behavior"

7.1 SoC System States

7.1.1 System Sleeping States Control (S-states)

The SoC supports the S0, S3, S4, and S5 sleep states. S4 and S5 states are identical from a hardware and power perspective. The differentiation is software determined (S4 = Suspend to Disk).

The SoC platform architecture assumes the usage of an external power management controller e.g., CPLD or PMIC. Some flows in this section refer to the power management controller for support of the S-states transitions.

The SoC sleep states are described in Chapter 6, "Power Management".

7.2 Power Up Sequences

7.2.1 RTC Power Well Transition (G5 to G3 States Transition)

When RTC_VCC (Real Time Clock power) is applied via RTC battery, the following occurs (see Figure 11 for timing):

1. RTC_VCC ramps. ILB_RTC_TEST# should be low.
2. The system starts the real time clock oscillator.
3. A minimum of t1 units after RTC_VCC ramps, the external RTC RC circuit de-asserts ILB_RTC_TEST# and ILB_RTC_RTC#. The system is now in the G3 state. RTC oscillator is unlikely to be stable at this point.

Figure 11. RTC Power Well Timing Diagrams

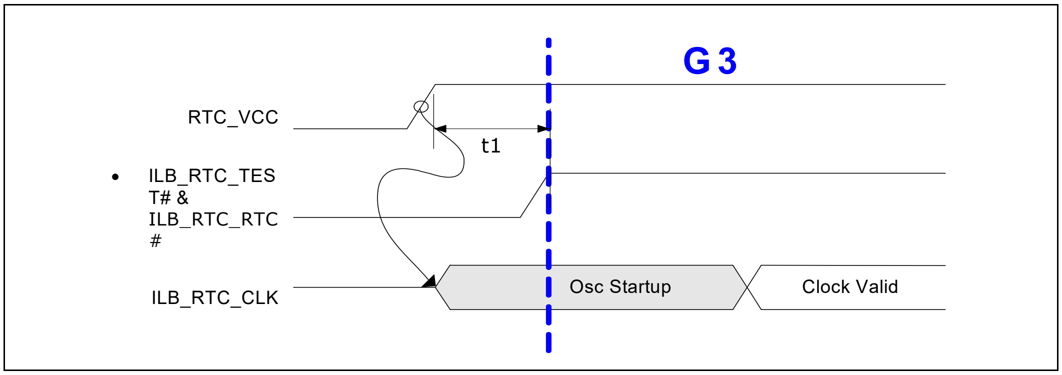


Table 60. RTC Power Well Timing Parameters

Parameter	Description	Min	Max	Units
t1	RTC_VCC to ILB_RTC_TEST# and ILB_RTC_RTC# de-assertion	18	-	ms

NOTES:
1. This delay is typically created from an RC circuit.
2. The oscillator startup times are component and design specific. A crystal oscillator can take several second to reach a large enough voltage swing. A silicon oscillator can have startups times <10 ms.

7.2.2 G3 to S0

The timings shown in Figure 12 occur when a board event such as AC power is applied or power management controller (PMIC) power button is pressed. The following occurs:

1. Suspend (SUS/Always On) wells ramp in the order shown.
2. The external power management controller de-asserts PMC_RSMRST# after the suspend rails become stable.
3. PMC_SUSCLK will begin toggling after the de-assertion of PMC_RSMRST#.
4. The system is now in S4/S5 state. Depending on policy bits (GEN_PMCON1.PWR_FLR & GEN_PMCON1.AG3E), the SoC either waits for a wake event to transition to S0 or continues to S0 state automatically.
5. The transition from S4/S5 to S0 is initiated.
6. The SoC de-asserts PMC_SLP_S4#, and the DRAM (VDD/Un-switched) well ramps.
7. After the DRAM power rail ramp, the external power management controller drives DRAM_VDD_S4_PWROK high.
8. The SoC de-asserts PMC_SLP_S3#, and the Core (S0/Switched On) wells ramp in the order shown.
9. After all of Core power rails are stable, external power management controller drives PMC_CORE_PWROK and DRAM_CORE_PWROK to HIGH, the SoC will then

fetch the descriptor region and soft straps data from the PCU located SPI interface, followed by the SoC de-asserting PMC_SUS_STAT#.

10. The SoC de-asserts PMC_PLTRST# after PMC_SUS_STAT# is stable. The PMC_PLTRST# is the main platform reset to other components.
11. The SoC will begin fetching data from the PCU-located SPI interface and proceed to finish initialization and start code execution (BIOS).

Note: There is no hard time requirement for transitions for the Always on/SUS rails (V1.0A, V1.2A, V1.8A, V3.3A). A 10 µs to 10 ms delay is required for two adjacent rails of them to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

Figure 12. G3/S5 to S0 Cold Boot Sequence

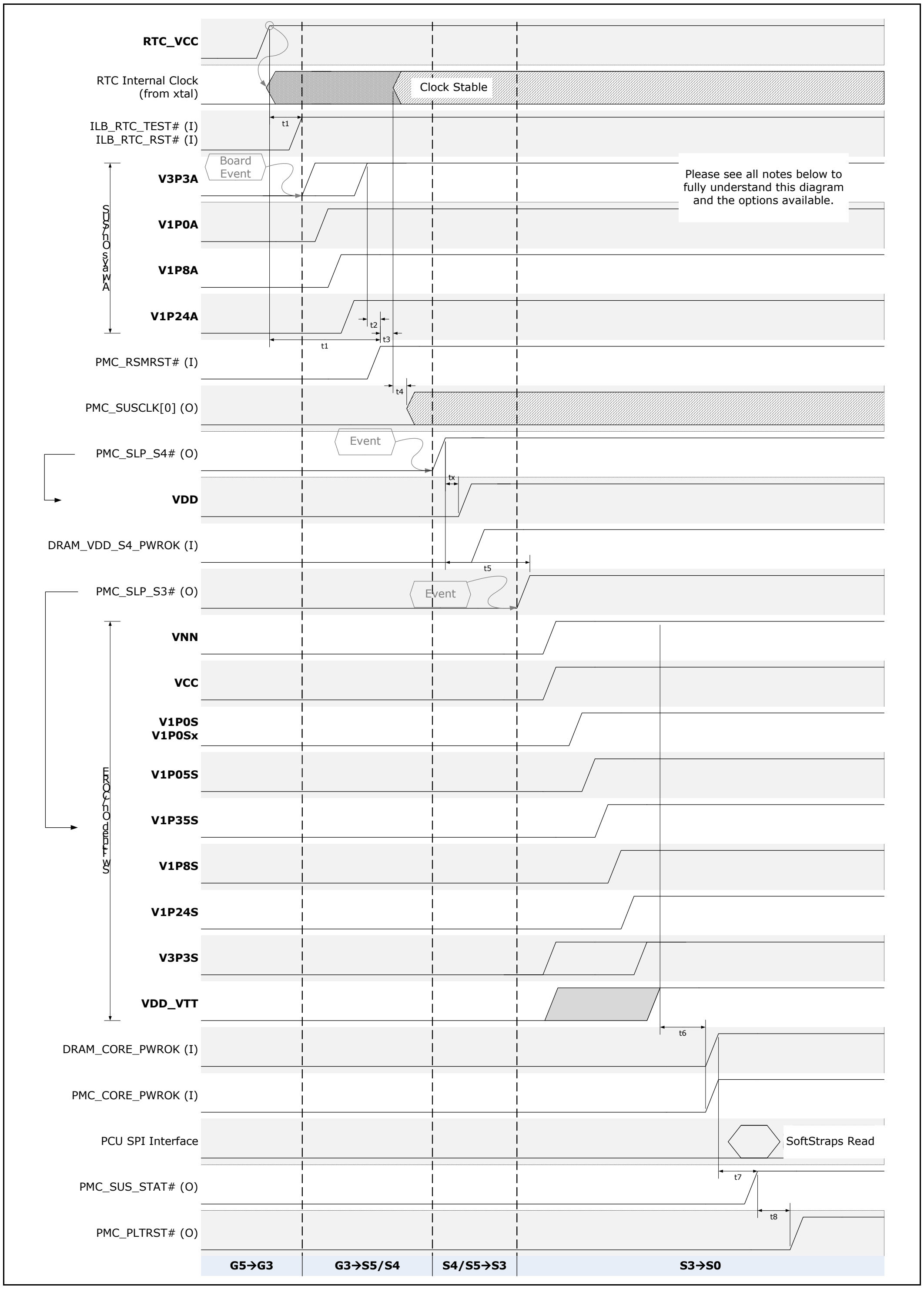


Table 61. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit
t1	RTC_VCC to ILB_RTC_TEST# and ILB_RTC_RTC# de-assertion RTC_VCC to PMC_RSMRST# de-assertion	18	-	ms
t2	V3P3A (SUS Rails) valid to PMC_RSMRST# de-assertion (t1 still applies in applications without RTC battery)	10	-	us
t3	PMC_RSMRST# to Internal RTC Clock assumed stable[2]	95		ms
t4	Internal RTC Clock assumed stable to PMC_SUSCLK[0] toggling[2]	5		ms
t5	PMC_SLP_S4# de-assertion to PMC_SLP_S3# de-assertion	30	-	us
t6a	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (No PCIe devices)	10	-	ms
t6b	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (for power rails needed by PCIe devices)	99	-	ms
t7	DRAM/PMC_CORE_PWROK to PMC_SUS_STAT#	1	-	ms
t8	PMS_SUS_STAT# de-assertion to PMC_PLTRST# de-assertion	60	-	us
tx	PMC_SLP_S4# de-assertion to VDDQ ramp start	0	-	ms

NOTES:.
1. RTC and SUS power rails may come up at the same time if no RTC battery is used.
2. Must ensure RTC clock is oscillating before these counts. SoC counts this time assuming a RTC clock of 32.768 KHz. Depending on how stable the oscillations are, however, this time can vary (+/-). This is effectively the *typical* amount of time the SoC waits to help ensure the clock is stable enough to proceed with power sequencing. It’s more likely a min since RTC clock will typically run slow until stable.
3. Wake events shown in figure depend on platform configuration.
4. In the SUS rail sequence, V3P3A can be first in sequence if required for designs, otherwise it can end the SUS sequence.
5. An alternate SUS rail sequence allows swapping V1P8A with V1P0A.
6. For power rail sequences, at least 10us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling. A maximum delay of 2 ms is allowed. Measurement of delay is at the 90% of full voltage mark of the prior rail to 10% later rail.
7. VCC can follow VNN in the CORE rail sequence or at the same time. Reference platform sequences both at the same time.
8. “Board Event” is platform specific. Most likely enabled by a platform power management controller or PMIC via a dedicated power button or when AC power is applied.
9. For exit from S4 and S3 Events, see “Cause of Wake Events” table in this chapter. S4 wake is required from PMC_PWRBTN# without prior configuration. S3 wake event is only used when the platform directly transitions to S3 (STR).
10. The V1P35S rail “VGA_V1P35_S3_F1” must be powered on as shown above. All other V1P35S/VSFR ([X]_V1P35_S3_F[x]) rails can either power on as shown, or power on after V3P3S.
11. PMC_SUSPWRDNACK is intended to be used at power-down and, since its state after a power-down is variable, it is recommended that a system treats PMC_SUSRWRDNACK as a Do Not Care during power-on. For systems that are unable to treat PMC_SUSPWRDNACK as a Do Not Care during power-on, the following power-on state is always valid: - 1) PMC_SUSPWRDNACK will always be low, until PMC_SLP_S3# de-asserts, if PMC_SUSPWRDNACK was low upon entry into S5. PMC_SUSPWRDNACK is always low when entering S5 from G3.
12. Where no maximum timing is specified, it is expected that the maximum timing should typically be within one unit of time of the minimum timing, under normal operating conditions. Due to potential variability in operating conditions, no maximum timing can be guaranteed however.
13. When HDA_LPE_V1P5V1P8_S3 is powered by a V1P5S rail, the V1P5S rail sequencing should meet the same sequencing requirements as the V1P8S rail.

7.3 Power Down Sequences

7.3.1 S0 to S3 and S4/S5/G3 Sequence

Entry to Sleep states (S3,S4, S5) is initiated by any of the following methods:

- Setting the desired sleep type in PM1_CNT.SLP_TYP and setting PM1_CNT.SLP_EN.
- Detection of an external catastrophic temperature event may cause a transition to S5, if the system is designed to do so.

The following sequence applies to S0-S3 and S0-S4/S5 transitions.

1. The Operating System Power Management (OSPM) will handle the enabling or disabling of interrupt generation after S3 resume. The Operating System Power Management (OSPM) will need to read and clear Wake status information and the processing of the clearing wake status which will include enabling interrupts (both at the core level and platform level).
2. All interrupts in the processor need to be disabled before the S3 sequence is started (and re-enabled on exit). The CPU APIC must be disabled.
3. When the desired sleep state is set in the PM1_CNT.TYP and PM1_CNT.SLP_EN registers, a sleep state request is sent to the PMC.
4. The PMC flushes all the internal buffers to main memory.
5. The PMC places the PCI Express* devices into the L2/L3 state. The PMC will wait until the PCI Express* devices are in the L2/L3 state before preceding. A timeout will occur in 1 ms if there is a non-functional PCI Express* device.

The Power Down Sequence is shown in Figure 13 below.

Additional assumptions:

- Entry to a Cx state is mutually exclusive with software-initiated entry to a Sleep state. This is because the processor(s) can only perform one register access at a time. This requirement is enforced by the CPU as well as the OS. The system may hang if it attempts to do a C-state and S-state at the same time.
- The G3 system state cannot be entered via any software mechanism. The G3 state indicates a complete loss of power. In this state, the RTC well may or may not be powered by an external coin cell battery.
- An external Power Management Controller (PMIC/EC) can be used to put the SoC in G3 when the S4/S5 state is requested by the SoC. This is done to save power in S4/S5 state. This G3 like state, known as SoC G3, is enabled by removing SUS rails via when the SUSPWRDNACK pin is asserted on power down. Doing so prevents the use of any of SUS wake events including USB, RTC, and GPIOs including the power button. The external Power Management Controller (or re-application of power) is required to return to S0.

Figure 13. S0 to S3 to S4/S5 (Power Down) Sequence without S0ix

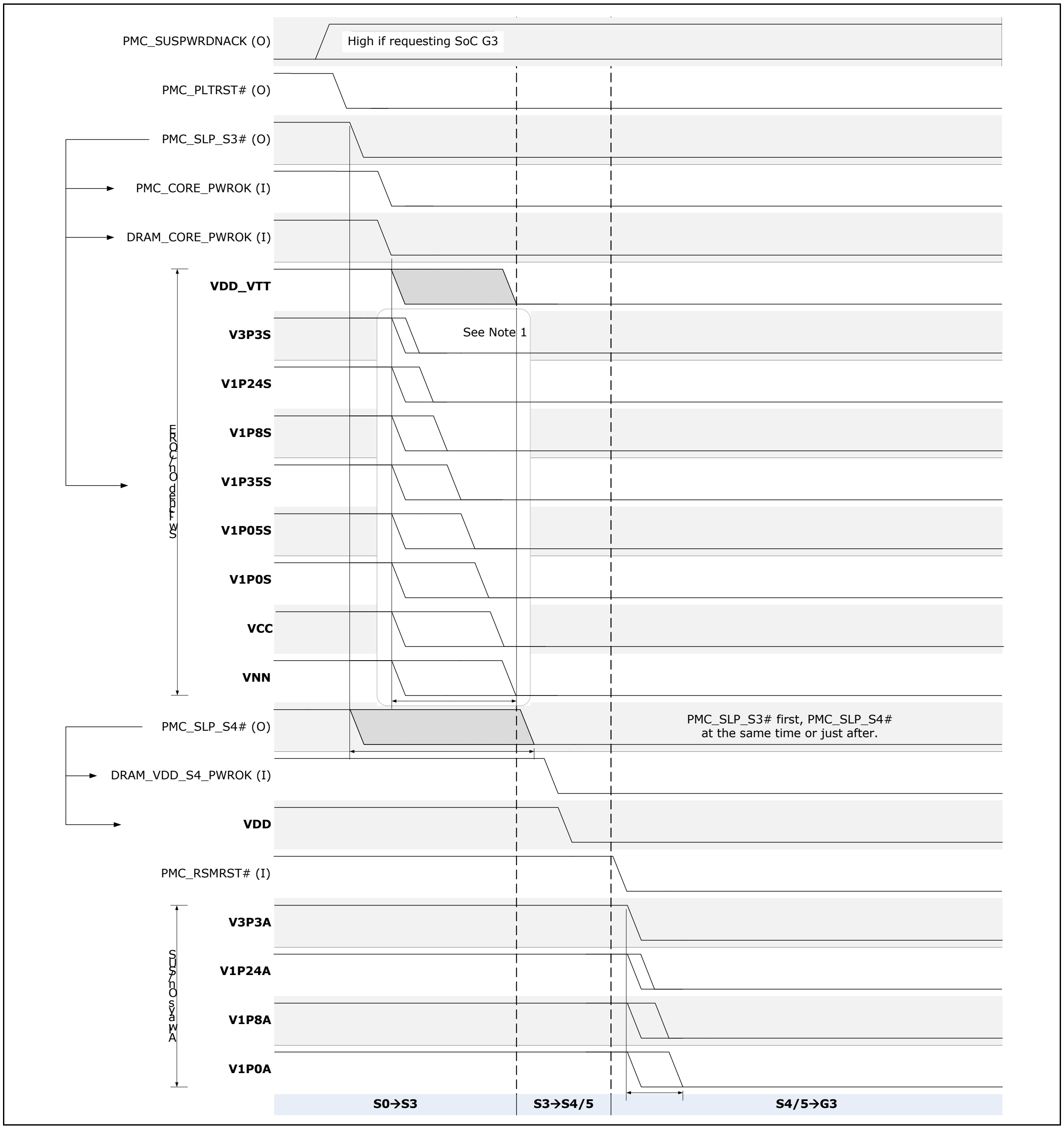


Table 62. S0 to G3 (Power Down) Sequence

Parameter	Description	Min	Max	Unit
t1	Power rail slew rate: From 90% to 10% of voltage typical	0.1	10	ms
t2	Tail to rail kick off delay[1]	0	3	ms

NOTES:.
1. The rail to rail kick off delay min is 0 ms and max 3 ms.
2. The Power Down Slew rate min is 0.1 ms and max is 10 ms.
3. Switched/CORE rails should be turned off at the same time. Alternately, it's ok to turn off all Switch/CORE rails in the reverse order of power up paying attention to t2 timing if so. Both sequences are shown.
4. An alternate SUS rail sequence allows swapping V1P8A with V1P0A.
5. SUS rails are turned off only if entering SoC G3 state (SoC lets the board/PMIC power management system know if this is ok - that there are no wake up events expected by the SoC). They can turn off at the same time, or in reverse power up order, just like the Switched/CORE rails.
6. VDD_VTT shows a range of times at which it can turn off. Any time within this range is fine.
7. SLP_S3# can be active before or after DRAM_CORE_PWROK and PMC_CORE_PWROK, but DRAM_CORE_PWROK should go low before memory power rails go low and PMC_CORE_PWROK should go low before Switched/CORE rails go low.
8. Measurement of delays is at the 10% voltage mark. Contact your Intel representative for additional details.
9. The V1P35S rail "VGA_V1P35_S3_F1" must be powered down as shown above. All other V1P35S/VSFR ([X]_V1P35_S3_F[x]) rails can either power down as shown, or power down before V3P3S.

7.3.2 S3/S4/S5 to S0 (Exit Sleep States)

Sleep states (S3-S5) are exited based on Wake events. The Wake events will force the system to a full on state (S0), although some non-critical subsystems might still be powered down and have to be brought back manually. For example, the hard disk may be powered down during a sleep state, and have to be enabled via an I/O pin before it can be used. Upon exit from software-entered Sleep states (i.e., those initiated via the PM1_CNT.SLP_EN bit), the PM1_STS_EN.WAK_STS bit will be set.

To enable Wake Events, the possible causes of wake events (and their restrictions) are shown in Table 63.

Table 63. S3/S4/S5 to S0 Cause of Wake Events (Sheet 1 of 2)

Cause	Type	How Enabled
RTC Alarm[1]	Internal	Set PM1_STS_EN.RTC_EN register bit
PMC_PWRBTN# (Power Button)	External	Default enabled as Wake event
GPIO_S5[7:0][1]	External	GPE0a_EN register (after having gone to S5 via PM1_CNT.SLP_EN, but not after a power failure.) Note: GPIOs that are in the core well are not capable of waking the system from sleep states where the core well is not powered.

Table 63. S3/S4/S5 to S0 Cause of Wake Events (Sheet 2 of 2)

Cause	Type	How Enabled
PMC_WAKE_PCIE[0:3]#[1] (PCI Express WAKE#)	External	PM1_STS_EN.PCIEXP_WAKE_DIS register bit Note: When the PMC_WAKE_PCIE# pin is active and the PM1_STS_EN.PCIEXP_WAKE_DIS register bit is clear, CPU will wake the platform.
Primary PME#[1]	Internal	GPEOa_EN.PME_B0_EN register bit. This wake status bit includes multiple internal agents: HD Audio EHCI (USB2) xHCI SATA Note: SATA can only trigger a wake event if it had asserted its PME prior to S3/S4/S5 entry and software doesn't clear GPE0a_STS.PME_B0_STS, a wake event would still result. PME_B0_S5_DIS bit is used to prevent these devices from waking from S5. Does not apply to wake from S3.
PMC - Initiated[1]	Internal	No enable bits. The PMC can wake the host independent of other wake events listed, if desired. A bit is provided in PRSTS for reporting this wake event to BIOS. Note that this wake event may be used as a wake trigger on behalf of some other wake source.

Note: 1. It is not possible to wake the SoC using this event after a Global Reset, Go-to-S5 type reset.

2. When the HDA_LPE_V1P5V1P8_S3 is powered by a V1P5S rail, the V1P5S rail sequencing should meet the same sequencing requirements as the V1P8S rail.

7.3.3 Handling Power Failures

The power failures can occur if the AC power or battery is removed. In this case, when the system was originally in a S0 state, power failure bit (GEN_PMCON1.PWR_FLR) is set after a power failure. Software can clear the bit.Chapter 7, "Handling Power Failures"

7.4 Reset Behavior

There are several ways to reset the processor.

Table 64. Types of Resets (Sheet 1 of 2)

Trigger	Description	Note
Write of 0Eh to Reset Control Register (RST_CNT)	Write of 0Eh to the Reset Control register	Host Reset with Power Cycle
Write of 06h to Reset Control Register (RST_CNT)	Write of 06h to the Reset Control register	Host Reset without Power Cycle with PMC_PLTRST# assertion
PMC_RSTBTN# & RST_CNT.full_rst = 0	User presses the reset button, causing the PMC_RSTBTN# signal to go active (after the debounce logic)	Host Reset without Power Cycle PMC_PLTRST# assertion enabled/ disabled by RST_CNT.sys_rst
Write of 4h to Reset Control Register (RST_CNT)	Write of 4h to Reset Control Register (RST_CNT)	Host Reset without Power Cycle without PMC_PLTRST# assertion
PMC_RSTBTN# & RST_CNT.full_rst = 1	User presses the reset button, causing the PMC_RSTBTN# signal to go active (after the debounce logic)	Host Reset with Power Cycle
Power Failure	PMC_CORE_PWROK signal goes inactive in S0/S1	Global Reset with Power Cycle
S3/S4/S5	The processor is reset when going to S3, S4 or S5 state	Sx Entry
Processor Thermal Trip	The internal thermal sensor signals a catastrophic temperature condition – transition to S5 and reset asserts	Global Reset, Go-to-S5
PMC_PWRBTN# Power Button Override	4-second press causes transition to S5 (and reset asserts)	Global Reset, Go-to-S5
CPU Shutdown with Policy to assert PMC_PLTRST#	Shutdown special cycle from CPU can cause either INIT or Reset Control-style PMC_PLTRST#	Global Reset with Power Cycle (if ETR.CF9GR = 1b) Host Reset with Power Cycle (if RST_CNT.full_rst= 1b), Host Reset without Power Cycle (others setting)
Write of 06h or 0Eh to Reset Control Register (RST_CNT)	ETR.CF9GR = 1b	Global Reset with Power Cycle
Host Partition Reset Entry Timeout	Host partition reset entry sequence took longer than the allowed timeout value (presumably due to a failure to receive one of the internal or external handshakes)	Global Reset with Power Cycle
S3/S4/S5 Entry Timeout	S3, S4, or S5 entry sequence took longer than the allowed timeout value (presumably due to a failure to receive one of the internal or external handshakes)	Global Reset, Go-to-S5

Table 64. Types of Resets (Sheet 2 of 2)

Trigger	Description	Note
PMC Watchdog Timer	PMC firmware watchdog time expires twice	Global Reset, Go-to-S5
TCO Watchdog Timer	TCO timer	RST_CNT.full_rst = 0: Host Reset without Power Cycle RST_CNT.full_rst = 1: Host Reset with Power Cycle
Host Reset promoted to Global Reset	During boot, TXE FW may promote a Host Reset to a Global Reset in order to apply new TXE or PMC firmware	Global Reset with Power Cycle

Note: - Host Reset without Power Cycle: All processor functionality not required for correct operation during & after reset, excluding the PMC, is reset and the SoC remain in S0.

- Host Reset with Power Cycle: All processor functionality not required for correct operation during & after reset, excluding the PMC, is reset and the SoC transitions to S5 and then to S0.

- Global Reset with Power Cycle: All processor functionality not required for correct operation during & after reset, including the PMC, is reset and the SoC transitions to S5 and then S0.

- Global Reset, Go-to-S5: All processor functionality not required for correct operation upon wake, including the PMC, are reset and the SoC transitions to S5.

8 Thermal Management

The SoC's thermal management system helps in managing the overall thermal profile of the system to prevent overheating and system breakdown. The architecture implements various proven methods of maintaining maximum performance while remaining within the thermal spec. Throttling mechanisms are used to reduce power consumption when thermal limits of the device are exceeded and the system is notified of critical conditions via interrupts or thermal signalling pins. SoC thermal management differs from legacy implementations primarily by replacing dedicated thermal management hardware with firmware.

The thermal management features are:

- Eight digital thermal sensors (DTS)
- Supports a hardware trip point and four programmable trip points based on the temperature indicated by thermal sensors.
- Supports different thermal throttling mechanisms.

8.1 CPU Thermal Management Registers

The description of the control and status registers can be found in the *Bay Trail SoC BIOS Writer's Guide*.

8.2 Thermal Sensors

SoC provides thermal sensors that use ring oscillator based DTS (Digital Thermal Sensor) to provide more accurate measure of system thermals.

The SoC instantiates multiple digital thermal sensors (one DTS for each processor core, one for each BIU-Bus Interface Unit, and two for non-core SoC) and sensor grouping configurations are provided to optionally select the maximum of all sensors for thermal readout and interrupt generation.

DTS output are adjusted for silicon variations. For a given temperature the output from DTS is always the same irrespective of silicon.

Table 65. Temperature Reading Based on DTS (If $T_{J\text{-}MAX}$ =90°C) (Sheet 1 of 2)

DTS Counter Value	Temperature Reading
127	90°C
137	80°C
147	70°C
157	60°C
167	50°C

Table 65. Temperature Reading Based on DTS (If $T_{J\text{-}MAX}$ =90°C) (Sheet 2 of 2)

DTS Counter Value	Temperature Reading
177	40°C
187	30°C
197	20°C
207	10°C

Note: DTS encoding of 127 always represents $T_{J\text{-}MAX}$.If $T_{J\text{-}MAX}$ is at 110°C instead of 90°C then the encoding 127 from DTS indicates 110°C, 137 indicates 90°C and so forth.

Thermal trip points are of two types:

- **Hard Trip**: The Catastrophic trip points generated by DTS's based on predefined temperature setting defined in fuses.
- **Programmable Trips**: four programmable trip settings (Hot, Aux2, Aux1, Aux0) that can be set by firmware/software. Default value for Hot Trip is from Fuses.

Note: DTS accuracy is around 8°C under 60°C and around 6°C above 60°C.

8.3 SoC Programmable Trips

Programmable trips can be programmed to cause different actions when triggered to reduce temperature of the die.

8.3.1 Aux3 Trip

By default, the Aux 3 (Hot Trip) point is set by fuses but the software/firmware has an option to set these to a different value.

This trip point is enabled by firmware to monitor and control the system temperature while the rest of the system is being set up.

8.3.2 Aux2, Aux1, Aux0 Trip

These are fully programmable trip points for general hardware protection mechanisms. The programmable trips are only active after software/firmware enables the trip.

Note: Unlike Aux3, the Aux[2:0] trip registers are defaulted to zero. To prevent spurious results, software/firmware should program the trip values prior to enabling the trip point.

8.4 Platform Trips

8.4.1 PROCHOT#

The platform components use the signal PROCHOT# to indicate thermal events to SoC.

The processor core HOT trip as well as the processor AUX 3 trip are individually sent to firmware, which internally combines them and drives the appropriate PROCHOT back. Assertion of the PROCHOT# input will trigger Thermal Monitor 1 or Thermal Monitor 2 throttling mechanisms if they are enabled.

8.5 Thermal Throttling Mechanisms

Thermal throttling mechanisms are implemented to try to reduce temperature by reducing power consumption in response to a HOT condition. Actions taken as a result of Thermal Trip indication can be as simple as throttling bandwidth and frequency to as drastic as shutting down the PLL's and the entire system. Actions are primarily taken in to prevent system breakdown and are dependent on the severity of the trips.

8.6 Thermal Status

The firmware captures Thermal Trip events (other than THERMTRIP) in status registers to trigger thermal actions. Associated with each event is a set of programmable actions. For a complete list of refer to the *Bay Trail SoC BIOS Writer's Guide.*

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9 Electrical Specifications

This chapter is split into the following sections:

- "Thermal Specifications"
- "Storage Conditions"
- "Voltage and Current Specifications"
- "Crystal Specifications"
- "DC Specifications"
- "AC Specifications"

9.1 Thermal Specifications

These specifications define the operating thermal limits of the SoC. Thermal solutions not designed to provide the following level of thermal capability may affect the long-term reliability of the processor and system, but more likely result in performance throttling to ensure silicon junction temperatures within spec. For more details on thermal solution design, refer to this product's Thermal/Mechanical Design Guide.

This section specifies the thermal specifications for all SKUs. Some definitions are needed, however. "Tj Max" defines the maximum operating silicon junction temperature. Unless otherwise specified, all specifications in this document assume Tj Max as the worse case junction temperature. This is the temperature needed to ensure TDP specifications when running at guaranteed CPU and graphics frequencies. "TDP" defines the thermal dissipated power for a worse case estimated real world thermal scenario.

Table 66. Intel Atom® Processor E3800 Product Family Thermal Specifications

SKU	T_j Min/Max	TDP
E3845	-40 to 110 °C	10 W @ Tj Max
E3827	-40 to 110 °C	8 W @ Tj Max
E3826	-40 to 110 °C	7 W @ Tj Max
E3825	-40 to 110 °C	6 W @ Tj Max
E3815	-40 to 110 °C	5 W @ Tj Max
E3805	-40 to 110 °C	3 W @ Tj Max

9.2 Storage Conditions

This section specifies absolute maximum and minimum storage temperature and humidity limits for given time durations. Failure to adhere to the specified limits could result in physical damage to the component. If this is suspected, Intel recommends a visual inspection to determine possible physical damage to the silicon or surface components.

Table 67. Storage Conditions Prior to Board Attach

Symbol	Parameter	Min	Max
Tabsolute storage	Device storage temperature when exceeded for any length of time.	-25 °C	125 °C
Tshort term storage	The ambient storage temperature and time for up to 72 hours.	-25 °C	85 °C
Tsustained storage	The ambient storage temperature and time for up to 30 months.	-5 °C	40 °C
RHsustained storage	The maximum device storage relative humidity for up to 30 months.		60% @ 24 °C

Note:

- Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount re-flow are specified by the applicable JEDEC standard. Non-adherence may affect processor reliability.
- Component product device storage temperature qualification methods may follow JESD22-A119 (low temperature) and JESD22-A103 (high temperature) standards when applicable for volatile memory.
- Component stress testing is conducted in conformance with JESD22-A104.
- The JEDEC J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.

9.2.1 Post Board-Attach

The storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component-level certification assessments post board-attach given the multitude of attach methods, socket types, and board types used by customers.

Provided as general guidance only, board-level Intel-branded products are specified and certified to meet the following temperature and humidity limits:

- Non-Operating Temperature Limit: -40 °C to 70 °C
- Humidity: 50% to 90%, non-condensing with a maximum wet-bulb of 28 °C

9.3 Voltage and Current Specifications

The I/O buffer supply voltages are specified at the SoC package balls. The tolerances shown in Table 86 are inclusive of all noise from DC up to 20 MHz. The voltage rails should be measured with a bandwidth limited oscilloscope with a roll-off of 3 dB/decade above 20 MHz under all operating conditions. Table 94 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltage rails that are connected to a filter, they should be measured at the input of the filter. If the recommended platform decoupling guidelines cannot be met, the system designer will have to make trade-offs between the voltage regulator out DC tolerance and the decoupling performances of the capacitor network to stay within the voltage tolerances listed below.

Table 68. Power Rail DC Specs and Max Current

Platform Rail	Voltage Tolerances	Max Icc
V1P0A - UNCORE_V1P0_G3 - USB3_V1P0_G3	1.0 V DC: ±2% AC: ±3%	375 mA
V1P24A - USB_HSIC_V1P24_G3 (Can connect to V1P0A when USB HSIC isn't used)	1.24 V DC: ±3% AC: ±2%	35 mA
V1P8A - PCU_V1P8_G3 - PMC_V1P8_G3 - UNCORE_V1P8_G3 - USB_V1P8_G3 - USB_ULPI_V1P8_G3	1.8 V DC: ±3% AC: ±2%	65 mA
V3P3A - PCU_V3P3_G3 - USB_V3P3_G3	3.3 V DC: ±2% AC: ±3%	55 mA
V1P0S - GPIO_V1P0_S3 - PCIE_SATA_V1P0_S3 - PCIE_V1P0_S3 - SATA_V1P0_S3 - SVID_V1P0_S3 - USB3DEV_V1P0_S3 - USB_V1P0_S3 - VGA_V1P0_S3	1.0 V DC: ±2% AC: ±3%	1.1 A
V1P0S - DRAM_V1P0_S3 - DDI_V1P0_S3 - UNCORE_V1P0_S3	1.0 V DC: ±2% AC: ±3%	2.5 A

Table 68. Power Rail DC Specs and Max Current

Platform Rail	Voltage Tolerances	Max Icc
V1P05S - CORE_V1P05_S3	1.05 V DC: ±2% AC: ±3%	1.3 A
V1P24S - MIPI_V1P24_S3 (can be grounded if MIPI CSI not used)	1.24 V DC: ±2% AC: ±3%	45 mA
V1P35S (VSFR) - ICLK_V1P35_S3_F[2:1] - VGA_V1P35_S3_F1(grounded if VGA not used) - DRAM_V1P35_S3_F1 - UNCORE_V1P35_S3_F[6:1]	1.35 V DC: ±3% AC: ±2%	400 mA
V1P5V1P8S (VAUD) - HDA_LPE_V1P5V1P8_S3	1.5 V (LV HDA) 1.8 V (LPE)	In V1P8S
V1P8S - UNCORE_V1P8_S3 - MIPI_V1P8_S3	1.8 V DC: ±3% AC: ±2%	10 mA
V1P8V3P3S (VSDIO,VLPC) - LPC_V1P8V3P3_S3 - SD3_V1P8V3P3_S3	1.8 V 3.3 V DC: ±2% AC: ±3%	8 mA
V3P3S - VGA_V3P3_S3	3.3 V DC: ±2% AC: ±3%	35 mA
VCC - CORE_VCC_S3	See Table 70	See Table 69
VNN - UNCORE_VNN_S3	See Table 70	See Table 69
VDD - DRAM_VDD_S4	1.35 V DC: ±2% AC: ±3%	1.3 A
VRTC - RTC_VCC	G3: 2-3.3 V at SoC Otherwise: V3P3A (pre diode drop)	100 uA (6 uA Avg.) (see note)

Note: RTC_VCC average current draw (G3) is specified at 27°C under battery conditions.

Note: S3/S4/S5 power is 20 mW max. S3/S4/S5 power is measured during S3/S4/S5 idle as a long term average over worst case silicon at room temperature (27°C). It is intended to define a limit of the power consumed by the SoC during the S3/S4/S5 state for battery life estimates and power budgeting. Breakdown is as follows: < 4 mA on V1P8A, < 15 mA on V1P0A, < 1 mW on V1P35U/V3P3A/V1P24A.

Table 69. VCC and VNN Currents

SKU	VCC Icc Max	VNN Icc Max
E3845	9 A	10 A
E3827	4 A	10 A
E3826	4 A	10 A
E3825	4 A	9 A
E3815	2 A	8 A
E3805	4 A	7 A

9.3.1 VCC and VNN Voltage Specifications

Table 70 and Table 86 list the DC specifications for the SoC power rails. They are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 70. VCC and VNN DC Voltage Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
CORE_VCC_S3 VID	Core VID (voltage) Target Range	0.40		1.0	V	1
UNCORE_VNN_S3 VID	Uncore VID (voltage) Target Range	0.50		1.05	V	1
CORE_VCC/ UNCORE_VNN V_{BOOT}	Default target V_{CC}/V_{NN} voltage for initial power up.		1.0 or 1.1		V	2
VCC/VNN Tolerance	Tolerance of VCC/VNN voltage at VID target.	-5		5	%	

NOTES:
1. Each SoC is programmed with voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual VID values are calibrated during manufacturing such that two SoCs at the same frequency may have different settings within the VID range above. VID targets employed by the SoC during a power management event are selected within the range uniquely hard-coded into each SoC.
2. See the VR12/IMVP7 Pulse Width Modulation specification for additional details. Either value is ok.

9.3.2 Voltage Identification (VID)

The VID specifications for the SoC CORE_VCC_S3 and UNCORE_VNN_S 3are defined by the IMVP7 Pulse Width Modulation (PWM) Specification. Table 71 specifies the voltage level corresponding to the eight bit VID value transmitted over serial VID (SVID) interface per IMVP7 specification. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to a low voltage level. If the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself.

The SVID signals are CMOS push/pull drivers. Refer to Table 103 for the DC specifications for these signals. The VID codes will change due to performance, temperature and/or current load changes in order to minimize the power of the part. A voltage range is provided in Table 70. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual SoC VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Table 70. The SoC provides the ability to operate while transitioning to an adjacent VID and its associated voltage. This will represent a DC shift in the loadline.

Note: Table below lists all voltages possible per IMVP7 specification. Not all voltages are valid on actual SKUs.

Table 71. IMVP7.0 Voltage Identification Reference (Sheet 1 of 8)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.25000
0	0	0	0	0	0	1	0	0	2	0.25500
0	0	0	0	0	0	1	1	0	3	0.26000
0	0	0	0	0	1	0	0	0	4	0.26500
0	0	0	0	0	1	0	1	0	5	0.27000
0	0	0	0	0	1	1	0	0	6	0.27500
0	0	0	0	0	1	1	1	0	7	0.28000
0	0	0	0	1	0	0	0	0	8	0.28500
0	0	0	0	1	0	0	1	0	9	0.29000
0	0	0	0	1	0	1	0	0	A	0.29500
0	0	0	0	1	0	1	1	0	B	0.30000
0	0	0	0	1	1	0	0	0	C	0.30500
0	0	0	0	1	1	0	1	0	D	0.31000
0	0	0	0	1	1	1	0	0	E	0.31500
0	0	0	0	1	1	1	1	0	F	0.32000
0	0	0	1	0	0	0	0	1	0	0.32500
0	0	0	1	0	0	0	1	1	1	0.33000
0	0	0	1	0	0	1	0	1	2	0.33500
0	0	0	1	0	0	1	1	1	3	0.34000

Table 71. IMVP7.0 Voltage Identification Reference (Sheet 2 of 8)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
0	0	0	1	0	1	0	0	1	4	0.34500
0	0	0	1	0	1	0	1	1	5	0.35000
0	0	0	1	0	1	1	0	1	6	0.35500
0	0	0	1	0	1	1	1	1	7	0.36000
0	0	0	1	1	0	0	0	1	8	0.36500
0	0	0	1	1	0	0	1	1	9	0.37000
0	0	0	1	1	0	1	0	1	A	0.37500
0	0	0	1	1	0	1	1	1	B	0.38000
0	0	0	1	1	1	0	0	1	C	0.38500
0	0	0	1	1	1	0	1	1	D	0.39000
0	0	0	1	1	1	1	0	1	E	0.39500
0	0	0	1	1	1	1	1	1	F	0.40000
0	0	1	0	0	0	0	0	2	0	0.40500
0	0	1	0	0	0	0	1	2	1	0.41000
0	0	1	0	0	0	1	0	2	2	0.41500
0	0	1	0	0	0	1	1	2	3	0.42000
0	0	1	0	0	1	0	0	2	4	0.42500
0	0	1	0	0	1	0	1	2	5	0.43000
0	0	1	0	0	1	1	0	2	6	0.43500
0	0	1	0	0	1	1	1	2	7	0.44000
0	0	1	0	1	0	0	0	2	8	0.44500
0	0	1	0	1	0	0	1	2	9	0.45000
0	0	1	0	1	0	1	0	2	A	0.45500
0	0	1	0	1	0	1	1	2	B	0.46000
0	0	1	0	1	1	0	0	2	C	0.46500
0	0	1	0	1	1	0	1	2	D	0.47000
0	0	1	0	1	1	1	0	2	E	0.47500
0	0	1	0	1	1	1	1	2	F	0.48000
0	0	1	1	0	0	0	0	3	0	0.48500
0	0	1	1	0	0	0	1	3	1	0.49000
0	0	1	1	0	0	1	0	3	2	0.49500
0	0	1	1	0	0	1	1	3	3	0.50000
0	0	1	1	0	1	0	0	3	4	0.50500
0	0	1	1	0	1	0	1	3	5	0.51000
0	0	1	1	0	1	1	0	3	6	0.51500
0	0	1	1	0	1	1	1	3	7	0.52000

Table 71. IMVP7.0 Voltage Identification Reference (Sheet 3 of 8)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
0	0	1	1	1	0	0	0	3	8	0.52500
0	0	1	1	1	0	0	1	3	9	0.53000
0	0	1	1	1	0	1	0	3	A	0.53500
0	0	1	1	1	0	1	1	3	B	0.54000
0	0	1	1	1	1	0	0	3	C	0.54500
0	0	1	1	1	1	0	1	3	D	0.55000
0	0	1	1	1	1	1	0	3	E	0.55500
0	0	1	1	1	1	1	1	3	F	0.56000
0	1	0	0	0	0	0	0	4	0	0.56500
0	1	0	0	0	0	0	1	4	1	0.57000
0	1	0	0	0	0	1	0	4	2	0.57500
0	1	0	0	0	0	1	1	4	3	0.58000
0	1	0	0	0	1	0	0	4	4	0.58500
0	1	0	0	0	1	0	1	4	5	0.59000
0	1	0	0	0	1	1	0	4	6	0.59500
0	1	0	0	0	1	1	1	4	7	0.60000
0	1	0	0	1	0	0	0	4	8	0.60500
0	1	0	0	1	0	0	1	4	9	0.61000
0	1	0	0	1	0	1	0	4	A	0.61500
0	1	0	0	1	0	1	1	4	B	0.62000
0	1	0	0	1	1	0	0	4	C	0.62500
0	1	0	0	1	1	0	1	4	D	0.63000
0	1	0	0	1	1	1	0	4	E	0.63500
0	1	0	0	1	1	1	1	4	F	0.64000
0	1	0	1	0	0	0	0	5	0	0.64500
0	1	0	1	0	0	0	1	5	1	0.65000
0	1	0	1	0	0	1	0	5	2	0.65500
0	1	0	1	0	0	1	1	5	3	0.66000
0	1	0	1	0	1	0	0	5	4	0.66500
0	1	0	1	0	1	0	1	5	5	0.67000
0	1	0	1	0	1	1	0	5	6	0.67500
0	1	0	1	0	1	1	1	5	7	0.68000
0	1	0	1	1	0	0	0	5	8	0.68500
0	1	0	1	1	0	0	1	5	9	0.69000
0	1	0	1	1	0	1	0	5	A	0.69500
0	1	0	1	1	0	1	1	5	B	0.70000

Table 71. IMVP7.0 Voltage Identification Reference (Sheet 4 of 8)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
0	1	0	1	1	1	0	0	5	C	0.70500
0	1	0	1	1	1	0	1	5	D	0.71000
0	1	0	1	1	1	1	0	5	E	0.71500
0	1	0	1	1	1	1	1	5	F	0.72000
0	1	1	0	0	0	0	0	6	0	0.72500
0	1	1	0	0	0	0	1	6	1	0.73000
0	1	1	0	0	0	1	0	6	2	0.73500
0	1	1	0	0	0	1	1	6	3	0.74000
0	1	1	0	0	1	0	0	6	4	0.74500
0	1	1	0	0	1	0	1	6	5	0.75000
0	1	1	0	0	1	1	0	6	6	0.75500
0	1	1	0	0	1	1	1	6	7	0.76000
0	1	1	0	1	0	0	0	6	8	0.76500
0	1	1	0	1	0	0	1	6	9	0.77000
0	1	1	0	1	0	1	0	6	A	0.77500
0	1	1	0	1	0	1	1	6	B	0.78000
0	1	1	0	1	1	0	0	6	C	0.78500
0	1	1	0	1	1	0	1	6	D	0.79000
0	1	1	0	1	1	1	0	6	E	0.79500
0	1	1	0	1	1	1	1	6	F	0.80000
0	1	1	1	0	0	0	0	7	0	0.80500
0	1	1	1	0	0	0	1	7	1	0.81000
0	1	1	1	0	0	1	0	7	2	0.81500
0	1	1	1	0	0	1	1	7	3	0.82000
0	1	1	1	0	1	0	0	7	4	0.82500
0	1	1	1	0	1	0	1	7	5	0.83000
0	1	1	1	0	1	1	0	7	6	0.83500
0	1	1	1	0	1	1	1	7	7	0.84000
0	1	1	1	1	0	0	0	7	8	0.84500
0	1	1	1	1	0	0	1	7	9	0.85000
0	1	1	1	1	0	1	0	7	A	0.85500
0	1	1	1	1	0	1	1	7	B	0.86000
0	1	1	1	1	1	0	0	7	C	0.86500
0	1	1	1	1	1	0	1	7	D	0.87000
0	1	1	1	1	1	1	0	7	E	0.87500
0	1	1	1	1	1	1	1	7	F	0.88000

Table 71. IMVP7.0 Voltage Identification Reference (Sheet 5 of 8)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
1	0	0	1	0	0	0	0	8	0	0.88500
1	0	0	1	0	0	0	1	8	1	0.89000
1	0	0	1	0	0	1	0	8	2	0.89500
1	0	0	0	0	0	1	1	8	3	0.90000
1	0	0	0	0	1	0	0	8	4	0.90500
1	0	0	0	0	1	0	1	8	5	0.91000
1	0	0	0	0	1	1	0	8	6	0.91500
1	0	0	0	0	1	1	1	8	7	0.92000
1	0	0	0	1	0	0	0	8	8	0.92500
1	0	0	0	1	0	0	1	8	9	0.93000
1	0	0	0	1	0	1	0	8	A	0.93500
1	0	0	0	1	0	1	1	8	B	0.94000
1	0	0	0	1	1	0	0	8	C	0.94500
1	0	0	0	1	1	0	1	8	D	0.95000
1	0	0	0	1	1	1	0	8	E	0.95500
1	0	0	0	1	1	1	1	8	F	0.96000
1	0	0	0	0	0	0	0	9	0	0.96500
1	0	0	0	0	0	0	1	9	1	0.97000
1	0	0	0	0	0	1	0	9	2	0.97500
1	0	0	1	0	0	1	1	9	3	0.98000
1	0	0	1	0	1	0	0	9	4	0.98500
1	0	0	1	0	1	0	1	9	5	0.99000
1	0	0	1	0	1	1	0	9	6	0.99500
1	0	0	1	0	1	1	1	9	7	1.00000
1	0	0	1	1	0	0	0	9	8	1.00500
1	0	0	1	1	0	0	1	9	9	1.01000
1	0	0	1	1	0	1	0	9	A	1.01500
1	0	0	1	1	0	1	1	9	B	1.02000
1	0	0	1	1	1	0	0	9	C	1.02500
1	0	0	1	1	1	0	1	9	D	1.03000
1	0	0	1	1	1	1	0	9	E	1.03500
1	0	0	1	1	1	1	1	9	F	1.04000
1	0	1	1	0	0	0	0	A	0	1.04500
1	0	1	1	0	0	0	1	A	1	1.05000
1	0	1	1	0	0	1	0	A	2	1.05500
1	0	1	0	0	0	1	1	A	3	1.06000

Table 71. IMVP7.0 Voltage Identification Reference (Sheet 6 of 8)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
1	0	1	0	0	1	0	0	A	4	1.06500
1	0	1	0	0	1	0	1	A	5	1.07000
1	0	1	0	0	1	1	0	A	6	1.07500
1	0	1	0	0	1	1	1	A	7	1.08000
1	0	1	0	1	0	0	0	A	8	1.08500
1	0	1	0	1	0	0	1	A	9	1.09000
1	0	1	0	1	0	1	0	A	A	1.09500
1	0	1	0	1	0	1	1	A	B	1.10000
1	0	1	0	1	1	0	0	A	C	1.10500
1	0	1	0	1	1	0	1	A	D	1.11000
1	0	1	0	1	1	1	0	A	E	1.11500
1	0	1	0	1	1	1	1	A	F	1.12000
1	0	1	0	0	0	0	0	B	0	1.12500
1	0	1	0	0	0	0	1	B	1	1.13000
1	0	1	0	0	0	1	0	B	2	1.13500
1	0	1	1	0	0	1	1	B	3	1.14000
1	0	1	1	0	1	0	0	B	4	1.14500
1	0	1	1	0	1	0	1	B	5	1.15000
1	0	1	1	0	1	1	0	B	6	1.15500
1	0	1	1	0	1	1	1	B	7	1.16000
1	0	1	1	1	0	0	0	B	8	1.16500
1	0	1	1	1	0	0	1	B	9	1.17000
1	0	1	1	1	0	1	0	B	A	1.17500
1	0	1	1	1	0	1	1	B	B	1.18000
1	0	1	1	1	1	0	0	B	C	1.18500
1	0	1	1	1	1	0	1	B	D	1.19000
1	0	1	1	1	1	1	0	B	E	1.19500
1	0	1	1	1	1	1	1	B	F	1.20000
1	1	0	0	0	0	0	0	C	0	1.20500
1	1	0	0	0	0	0	1	C	1	1.21000
1	1	0	0	0	0	1	0	C	2	1.21500
1	1	0	0	0	0	1	1	C	3	1.22000
1	1	0	0	0	1	0	0	C	4	1.22500
1	1	0	0	0	1	0	1	C	5	1.23000
1	1	0	0	0	1	1	0	C	6	1.23500
1	1	0	0	0	1	1	1	C	7	1.24000

Table 71. IMVP7.0 Voltage Identification Reference (Sheet 7 of 8)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
1	1	0	0	1	1	0	0	C	8	1.24500
1	1	0	0	1	0	0	1	C	9	1.25000
1	1	0	0	1	0	1	0	C	A	1.25500
1	1	0	0	1	0	1	1	C	B	1.26000
1	1	0	0	1	0	0	0	C	C	1.26500
1	1	0	0	1	1	0	1	C	D	1.27000
1	1	0	0	1	1	1	0	C	E	1.27500
1	1	0	0	1	1	1	1	C	F	1.28000
1	1	0	1	0	1	0	0	D	0	1.28500
1	1	0	1	0	1	0	1	D	1	1.29000
1	1	0	1	0	0	1	0	D	2	1.29500
1	1	0	1	0	0	1	1	D	3	1.30000
1	1	0	1	0	1	0	0	D	4	1.30500
1	1	0	1	0	1	0	1	D	5	1.31000
1	1	0	1	0	1	1	0	D	6	1.31500
1	1	0	1	0	1	1	1	D	7	1.32000
1	1	0	1	1	0	0	0	D	8	1.32500
1	1	0	1	1	0	0	1	D	9	1.33000
1	1	0	1	1	0	1	0	D	A	1.33500
1	1	0	1	1	0	1	1	D	B	1.34000
1	1	0	1	1	1	0	0	D	C	1.34500
1	1	0	1	1	1	0	1	D	D	1.35000
1	1	0	1	1	1	1	0	D	E	1.35500
1	1	0	1	1	1	1	1	D	F	1.36000
1	1	1	0	0	0	0	0	E	0	1.36500
1	1	1	0	0	0	0	1	E	1	1.37000
1	1	1	0	0	0	1	0	E	2	1.37500
1	1	1	0	0	0	1	1	E	3	1.38000
1	1	1	0	0	1	0	0	E	4	1.38500
1	1	1	0	0	1	0	1	E	5	1.39000
1	1	1	0	0	1	1	0	E	6	1.39500
1	1	1	0	0	1	1	1	E	7	1.40000
1	1	1	0	1	0	0	0	E	8	1.40500
1	1	1	0	1	0	0	1	E	9	1.41000
1	1	1	0	1	0	1	0	E	A	1.41500
1	1	1	0	1	0	1	1	E	B	1.42000

Table 71. IMVP7.0 Voltage Identification Reference (Sheet 8 of 8)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
1	1	1	0	1	1	0	0	E	C	1.42500
1	1	1	0	1	1	0	1	E	D	1.43000
1	1	1	0	1	1	1	0	E	E	1.43500
1	1	1	0	1	1	1	1	E	F	1.44000
1	1	1	1	0	0	0	0	F	0	1.44500
1	1	1	1	0	0	0	1	F	1	1.45000
1	1	1	1	0	0	1	0	F	2	1.45500
1	1	1	1	0	0	1	1	F	3	1.46000
1	1	1	1	0	1	0	0	F	4	1.46500
1	1	1	1	0	1	0	1	F	5	1.47000
1	1	1	1	0	1	1	0	F	6	1.47500
1	1	1	1	0	1	1	1	F	7	1.48000
1	1	1	1	1	0	0	0	F	8	1.48500
1	1	1	1	1	0	0	1	F	9	1.49000
1	1	1	1	1	0	1	0	F	A	1.49500
1	1	1	1	1	0	1	1	F	B	1.50000
1	1	1	1	1	1	0	0	F	C	1.49500
1	1	1	1	1	1	0	1	F	D	1.50000
1	1	1	1	1	1	1	0	F	E	1.49500
1	1	1	1	1	1	1	1	F	F	1.50000

9.4 Crystal Specifications

There are two crystal. One for RTC which maintains time and provides initial timing reference for power sequencing. The other is for the Integrated Clock, which covers clocking for the entire SoC.

Table 72. ILB RTC Crystal Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{RTC}	Frequency	-	32.768	-	kHz	1
T_{PPM}	Crystal frequency tolerance (see notes)	-	-	+/-50	ppm	1
R_{ESR}	ESR	-	-	50	kOhm	1
$C_{X1,2}$	Capacitance of X1, X2 pins				pF	1

NOTES:
1. These are the specifications needed to select a crystal oscillator for the RTC circuit.

2. Crystal tolerance impacts RTC time. A 10 ppm crystal is recommended for 1.7 s tolerance per day, RTC circuit itself contributes addition 10 ppm for a total of 20 ppm in this example.

Table 73. Integrated Clock Crystal Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{ICLK}	Frequency	-	25	-	MHz	1
T_{PPM}	Crystal frequency tolerance & stability	-	-	+/-100	ppm	1
P_{DRIVE}	Crystal drive load	-	-	100	uW	1
R_{ESR}	ESR	-	-	100	Ohm	1
C_{LOAD}	Crystal load capacitance		18		pF	
C_{SHUNT}	Crystal shunt capacitance	-	-	6	pF	1
$C_{IN/OUT}$	Capacitance of oscillator pins				pF	1

NOTES:
1. These are the specifications needed to select a crystal oscillator for the Integrated Clock circuit. Crystal must be AT cut, fundamental, parallel resonance.

9.5 DC Specifications

Platform reference voltages are specified at DC only. V_{REF} measurements should be made with respect to the supply voltages specified in "Voltage and Current Specifications".

See the following DC Specifications in this section:

- "Display DC Specification"
- "PCI Express* DC Specification"
- "MIPI-Camera Serial Interface (CSI) DC Specification"
- "SCC - SDIO DC Specification"
- "SCC - SD Card DC Specification"
- "SCC - eMMC 4.5 DC Specification"
- "SATA DC Specification"
- "JTAG (TAP) DC Specification"
- "DDR3L Memory Controller DC Specification"
- "USB 2.0 Host DC Specification"
- "USB 3.0 DC Specification"
- "PCU - iLB - LPC DC Specification"
- "PCU - SPI (Platform Control Unit) DC Specification"
- "PCU - Power Management/Thermal (PMC) & iLB RTC DC Specification"
- "SVID DC Specification"
- "GPIO DC Specification"

- "SIO - I2C DC Specification"
- "SIO - UART DC Specification"
- "I2S (Audio) DC Specification"

Note: Care should be taken to read all notes associated with each parameter.

9.5.1 Display DC Specification

DC specifications for display interfaces:

- "Analog VGA Video DC Specification"
- "Digital Display Interface (DDI) Signals DC Specification"

9.5.1.1 Analog VGA Video DC Specification

Interface DC Specifications are referred to the VESA Video Signal Standard, version 1 revision 2.

Table 74. R,G,B/VGA DAC Display DC specification (Functional Operating Range)

Parameter	Min	Typ	Max	Units	Notes
Resolution		8		bits	1
Max Luminance (full-scale)	0.665	0.700	0.770	V	1,2,4 (white video level voltage)
Min Luminance		0.0		V	1,3,4 (black video level voltage)
LSB Current		73.2	8	µA	4,5
Integral Non Linearity (INL)	-1.0		+1.0	LSB	1,6
Differential Non-Linearity (DNL)	-1.0		+1.0	LSB	1,6
Video Channel-to-Channel Voltage amplitude mismatch			6	%	7
Monotonicity		Guaranteed			

NOTES:
1. Measured at each R,G,B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude
4. Defined for a double 75 Ω termination
5. Set by external reference resistor value
6. INL & DNL measured and calculated according to VESA Video Signal Standards
7. Max fill-scale voltage difference among R,G,B outputs (percentage of steady-state full-scale voltage).

Table 75. VGA_DDCCLK, VGA_DDCDATA Signal DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	VGA_V3P3_S3				
V_{IH}	Input High Voltage	2		Vref	V	1
V_{IL}	Input Low Voltage	0		0.8	V	2
V_{OL}	Output Low Voltage	0		0.4	V	3
Ii	Input Pin Leakage	-45		45	µA	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. 3 mA sink current.
4. For VIN between 0V and VGA_V3P3_S3. Measured when driver is tri-stated.

Table 76. VGA_HSYNC and VGA_VSYNC DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	VGA_V3P3_S3				
V_{OH}	Output High Voltage	2.4		V_{REF}	V	
V_{OL}	Output Low Voltage	0		0.5	V	
I_{OH}	Output High Current			8	mA	
I_{OL}	Output Low Current			8	mA	
I_i	Input Pin Leakage	-35		35	µA	1

NOTE:
1. For V_{IN} between 0-V and VGA_V3P3_S3. Measured when driver is tri-stated.

9.5.1.2 Digital Display Interface (DDI) Signals DC Specification

Table 77. DDI Main Transmitter DC specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level0}$	Differential Peak-to-peak Output Voltage Level 0	0.34	0.4	0.46	V	1
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	Differential Peak-to-peak Output Voltage Level 1	0.51	0.6	0.68	V	1
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	Differential Peak-to-peak Output Voltage Level 2	0.69	0.8	0.92	V	1
$VT_{X\text{-}DIFFp\text{-}p\text{-}Level3}$	Differential Peak-to-peak Output Voltage Level 3	0.85	1.2	1.38	V	1
$V_{TX\text{-}PREEMP\text{-}RATIO}$	No Pre-emphasis	0.0	0.0	0.0	dB	1
	3.5 dB Pre-emphasis	2.8	3.5	4.2	dB	1

Table 77. DDI Main Transmitter DC specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
	6.0 dB Pre-emphasis	4.8	6.0	7.2	dB	1
	9.5 dB Pre-emphasis	7.5	9.5	11.4	dB	1
$V_{TX\text{-}DC\text{-}CM}$	Tx DC Common Mode Voltage	0		2.0	V	1
RLTX-DIFF	Differential Return Loss at 0.675GHz at Tx Package pins	12			dB	4
	Differential Return Loss at 1.35 GHz at Tx Package pins	9			dB	4
C_{TX}	AC Coupling Capacitor	75		200	nF	5
Voff	Single Ended Standby (off), output voltage	-10		10	mV	6 @ AVcc
Vswing	Single Ended output swing voltage	400		600	mV	
V_{OH} (<=165 MHz)	Single Ended high level, output voltage	-10		10	mv	6 @ AVcc
V_{OH}(>165 MHz)	Single Ended high level, output voltage	-200		10	mV	6 @ AVcc
V_{OL}(<=165 MHz)	Single Ended low level, output voltage	-600		-400	mV	6 @ AVcc
V_{OL}(>165MHz)	Single Ended low level, output voltage	-700		-400	mV	6 @ AVcc

NOTES:
1. For embedded connection, support of programmable voltage swing levels is optional.
2. Total drive current of the transmitter when it is shorted to its ground.
3. Common mode voltage is equal to Vbias_Tx voltage shown in Figure 14.
4. Straight loss line between 0.675 GHz and 1.35 GHz.
5. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.
6. AVcc =Analog Voltage level

Table 78. DDI AUX Channel DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{AUX\text{-}DIFFp\text{-}p}$	AUX Peak-to-peak Voltage at a transmitting Device	0.29		1.38	V	1
$V_{AUX\text{-}\_TERM\_R}$	AUX CH termination DC resistance		100		Ω	
$V_{AUX\text{-}DC\text{-}CM}$	AUX DC Common Mode Voltage	0		2.0	V	2

Table 78. DDI AUX Channel DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{AUX\text{-}TURN\text{-}CM}$	AUX turn around common mode voltage			0.3	V	3
I_{AUX_SHORT}	AUX Short Circuit Current Limit			90	mA	4
C_{AUX}	AC Coupling Capacitor	75		200	nF	5

NOTES:
1. $V_{AUX\text{-}DIFFp\text{-}p} = 2*|V_{AUXP} - V_{AUXM}|$
2. Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage.
3. Steady state common mode voltage shift between transmit and receive modes of operation.
4. Total drive current of the transmitter when it is shorted to its ground.
5. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.

NOTES:

Table 79. DDI DDC Signal DC Specification (DDI[1:0]_DDCDATA, DDI[1:0]_DDCCLK)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	MIPI_V1P8_S3			V	
V_{IH}	Input High Voltage	$0.65*V_{REF}$		V_{REF}	V	1
V_{IL}	Input Low Voltage	0		$0.35*V_{REF}$	V	2
V_{OL}	Output Low Voltage	0		0.4	V	3
I_i	Input Pin Leakage	-30		30	µA	4

1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. 3mA sink current.
4. For VIN between 0V and CORE_VCC_S3. Measured when driver is tri-stated.

Table 80. DDI DDC Misc Signal DC Specification (DDI[1:0]_HPD, DDI[1:0]_BKLTCTL, DDI[1:0]_VDDEN, DDI[1:0]_BKLTEN)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	MIPI_V1P8_S3			V	
V_{IH}	Input High Voltage	$0.65*V_{REF}$		V_{REF}	V	1
V_{IL}	Input Low Voltage	0		$0.35*V_{REF}$	V	2
Z_{pu}	Pull up Impedance	40	50	60	Ω	3
Z_{pd}	Pull down Impedance	40	50	60	Ω	3
I_i	Input Pin Leakage	-20		20	µA	4

1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at CORE_VCC_S3.
4. For VIN between 0V and CORE_VCC_S3. Measured when driver is tri-stated.

Figure 14. Definition of Differential Voltage and Differential Voltage Peak-to-Peak

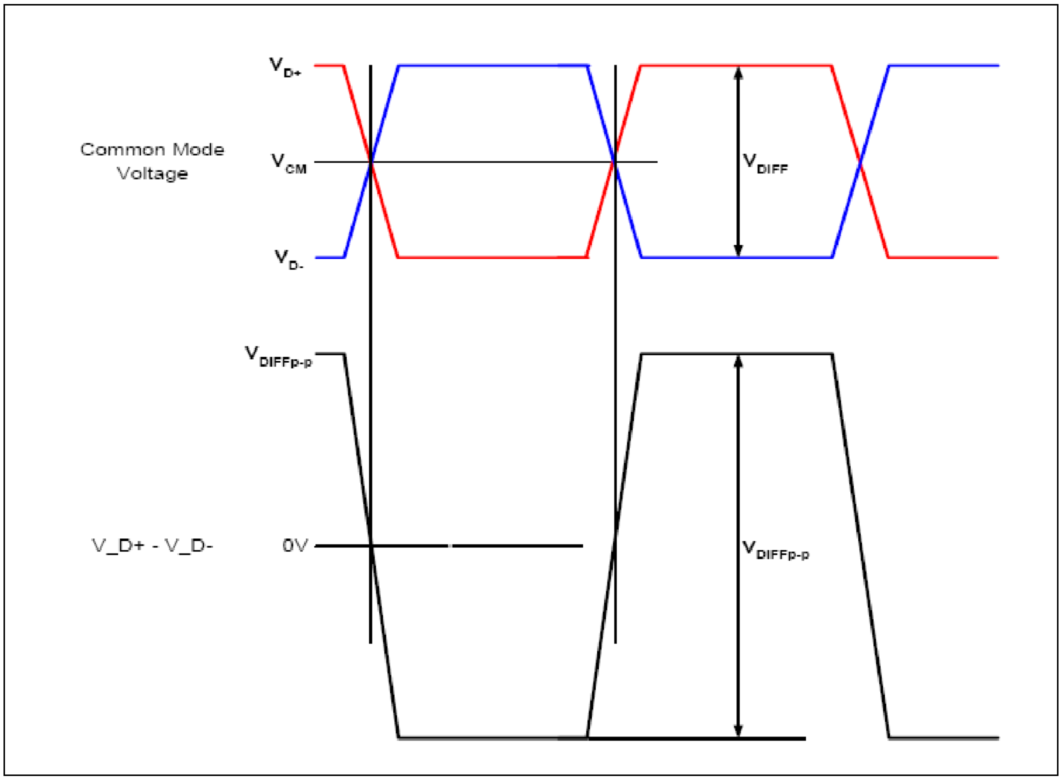
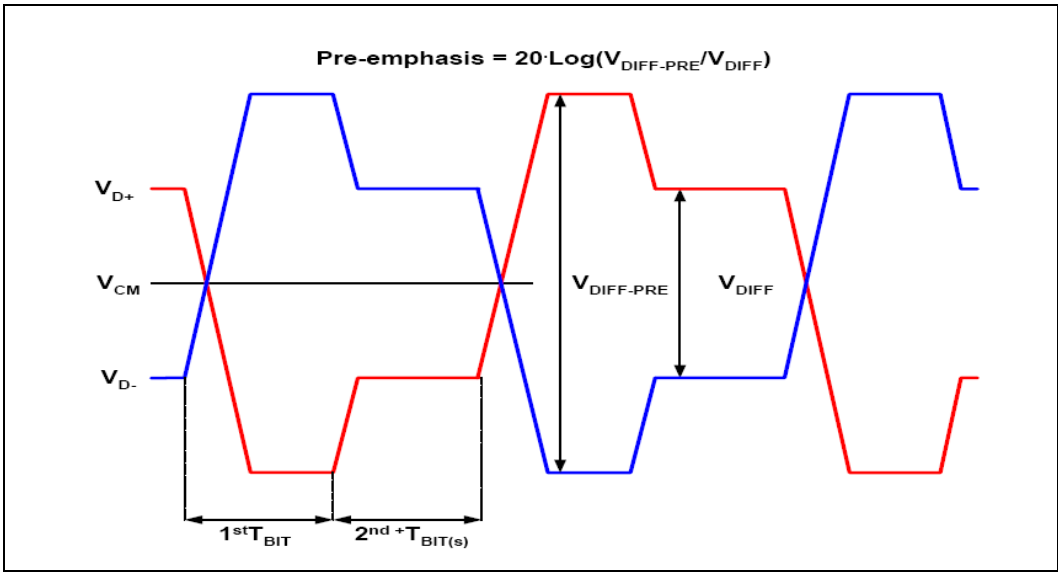


Figure 15. Definition of Pre-emphasis



9.5.2 PCI Express* DC Specification

Table 81. PCI Express* DC Receive Signal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{RXDIFF\ Gen1}$	Differential RX Peak to Peak	175		1200	mV	1
$V_{RXDIFF\ Gen2}$	Differential RX Peak to Peak	100		1200	mV	1

NOTE:
1. PCI Express differential peak to peak = 2*|RXp[x] – RXn[x]|

Table 82. PCI Express* DC Transmit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{TXDIFF}	Differential TX Peak to Peak	800		1200	mV	1
$V_{TXDIFF-LP}$	Differential TX Peak to Peak (low power mode)	400		1200	mV	1

NOTE:
1. PCI Express differential peak to peak = 2*|TXp[x] – TXn[x]|

Table 83. PCI Express* DC Clock Request Input Signal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{REF}	I/O Voltage	UNCORE_V1P8_S3				
V_{IL}	Input Low Voltage	0		$0.3*V_{REF}$	V	1
V_{IH}	Input High Voltage	$0.65*V_{REF}$		V_{REF}	V	1

9.5.3 MIPI-Camera Serial Interface (CSI) DC Specification

Table 84. MIPI HS-RX/MIPI LP-RX Minimum, Nominal, and Maximum Voltage Parameters (Sheet 1 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
I_{LEAK}	Pin Leakage current	-10	–	10	µA	
MIPI-CSI HS-RX Mode						
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	–	330	mV	
V_{IDTH}	Differential input high threshold	–	–	70	mV	
V_{IDTL}	Differential input low threshold	-70	–	–	mV	
V_{IHHS}	Single-ended input high voltage	–	–	460	mV	
V_{ILHS}	Single-ended input low voltage	-40	–	–	mV	
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	–	–	450	mV	
Z_{ID}	Differential input impedance	80	100	125	Ω	

Table 84. MIPI HS-RX/MIPI LP-RX Minimum, Nominal, and Maximum Voltage Parameters (Sheet 2 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
MIPI-CSI LP-RX Mode						
V_{IH}	Logic 1 input voltage	880	–	–	mV	
V_{IL}	Logic 0 input voltage, not in ULP state	–	–	550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	–	–	300	mV	
V_{HYST}	Input hysteresis	25	–	–	mV	

9.5.4 SCC - SDIO DC Specification

Table 85 provides the SDIO DC Specification, for all other DC Specifications not listed in Table 85, refer to Table 106, "GPIO 1.8V Core Well Signal Group DC Specification (GPIO_S0_SC[101:0]).

Table 85. SDIO DC Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output High Voltage	1.4	–	–	V	Measured at I_{OH} maximum.
I_{OH}/I_{OL}	Current at VoL/Voh	-2	–	–	mA	

9.5.5 SCC - SD Card DC Specification

Table 86 provides the SD Card DC Specification, for all other DC Specifications not listed in Table 86, refer to Table 106, "GPIO 1.8V Core Well Signal Group DC Specification (GPIO_S0_SC[101:0]).

Table 86. SD Card DC Specification

Symbol	Parameter	Min.	Max.	Unit
V_{REF}	I/O Voltage	SD3_V1P8V3P3_S3		
V_{OH}	Output High Voltage	$0.75*V_{REF}$	V_{REF}	V
V_{OL}	Output Low Voltage	0	$0.125*V_{REF}$	V
$V_{IH\ (3.3)}$	Input High Voltage (3.3 V)	$0.625*V_{REF}$	V_{REF}	V
$V_{IL\ (3.3)}$	Input Low Voltage (3.3 V)	0	$0.25*V_{REF}$	V
$V_{PEAK\ (3.3)}$	Peak Voltage on All lines	-0.3	$V_{REF}+0.3$	V
$V_{IH\ (1.8)}$	Input High Voltage (1.8 V)	1.28	V_{REF}	V

Table 86. SD Card DC Specification

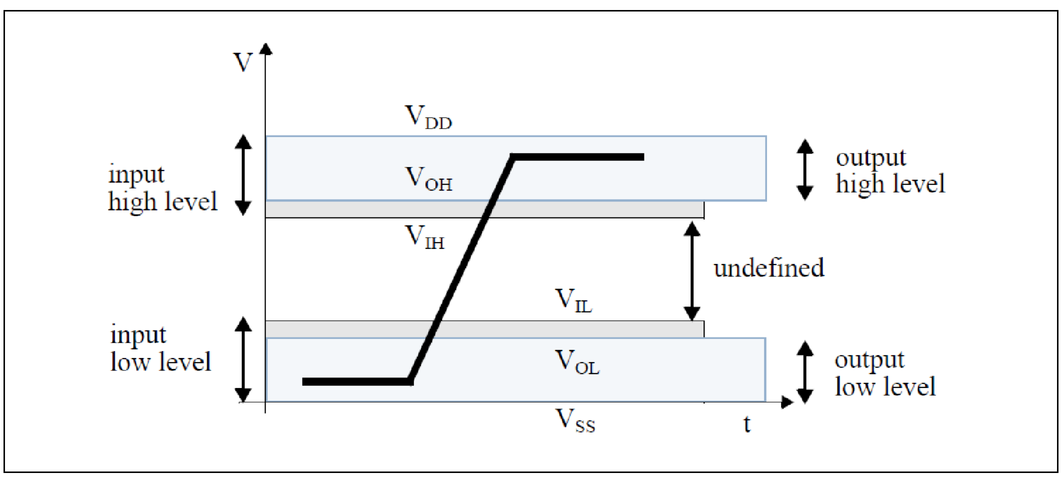
Symbol	Parameter	Min.	Max.	Unit
$V_{IL\ (1.8)}$	Input Low Voltage (1.8 V)	0	0.58	V
$V_{PEAK\ (1.8)}$	Peak Voltage on All lines	-0.3	V_{REF}+0.3	V
I_{OH}/I_{OL}	Current at VoL/Voh	-45	45	µA
$V_{hysteresis}$	Input Hysteresis	None		V
C_{LOAD}	Input Load Capacitance	4	9	pF

9.5.6 SCC - eMMC 4.5 DC Specification

Table 87. eMMC 4.5 Signal DC Electrical Specifications

Symbol	Parameter	Min	Max	Units
V_{REF}	I/O Voltage	UNCORE_V1P8_S3		
V_{OH}	Output HIGH voltage	V_{REF} - 0.45	V_{REF}	V
V_{OI}	Output LOW voltage	0	0.45	V
V_{IH}	Input HIGH voltage	0.65 * V_{REF}	V_{REF} + 0.3	V
V_{IL}	Input LOW voltage	-0.3	0.35 * V_{REF}	V
C_L	Bus Signal Line capacitance	-	30	pF
I_{LI}	Input Leakage Current	-2	2	µA
I_{LO}	Output Leakage Current	-2	2	µA

Figure 16. eMMC DC Bus signal level



9.5.7 JTAG (TAP) DC Specification

Table 88. TAP Signal Group DC Specification (TAP_TCK, TAP_TRSRT#, TAP_TMS, TAP_TDI)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V1P8_G3				
V_{IH}	Input High Voltage	$0.8*V_{REF}$		V_{REF}	V	1
V_{IL}	Input Low Voltage	0		$0.4*V_{REF}$	V	2
Z_{pu}	Pull up Impedance			60	Ω	3
Z_{pd}	Pull down Impedance			60	Ω	3
R_{wpu}	Weak Pull Impedance	1		4	kΩ	3
R_{wpd}	Weak Pull Down Impedance	1		4	kΩ	3
$R_{wpu\text{-}40K}$	Weak Pull Up Impedance 40K	20		70	kΩ	4
$R_{wpd\text{-}40K}$	Weak Pull Down Impedance 40K	20		70	kΩ	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at PMC_V1P8_G3/2.
4. Rwpu_40k and Rwpd_40k are only used for TAP_TRST#

Table 89. TAP Signal Group DC Specification (TAP_TDO)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V1P8_G3				
V_{IH}	Input High Voltage	$0.8*V_{REF}$		V_{REF}	V	1
V_{IL}	Input Low Voltage	0		$0.5*V_{REF}$	V	2
Z_{pd}	Pull down Impedance			30	Ω	3
R_{wpu}	Weak Pull Impedance	1		4	kΩ	3
R_{wpd}	Weak Pull Down Impedance	1		4	kΩ	3

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at PMC_V1P8_G3/2.

Table 90. TAP Signal Group DC Specification (TAP_PRDY#, TAP_PREQ#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V1P8_G3				
V_{IH}	Input High Voltage	0.64*V_{REF}		V_{REF}	V	1
V_{IL}	Input Low Voltage	0		0.4*V_{REF}	V	2
Z_{pd}	Pull down Impedance			30	Ω	3
R_{wpu}	Weak Pull Impedance	1		4	kΩ	3

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at PMC_V1P8_G3/2.

9.5.8 DDR3L Memory Controller DC Specification

Table 91. DDR3L Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Type	Max	Units	Notes
V_{IL}	Input Low Voltage			DRAM_VREF - 200mV	V	1
V_{IH}	Input High Voltage	DRAM_VREF + 200mV			V	2, 3
V_{OL}	Output Low Voltage		(DRAM_VDD_S4 / 2)* (RON / (RON+RVTT_TERM))			3,4
V_{OH}	Output High Voltage		DRAM_VDD_S4 - ((DRAM_VDD_S4 /2)* (RON/(RON+RVTT_TERM))		V	3,4
I_{IL}	Input Leakage Current			5	μA	For all DRAM Signals
R_{ON}	DDR3L-RS Clock Buffer strength	26		40	Ω	5
C_{IO}	DQ/DQS/DQS# DDR3L-RS IO Pin Capacitance		3.0		pF	
VIH	Input High Voltage	1.1			V	DRAM_VDD_S4_PWROK DRAM_CORE_PWROK

Table 91. DDR3L Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Type	Max	Units	Notes
VIL	Input Low Voltage			0.3	V	DRAM_VDD_S4_PWROK DRAM_CORE_PWROK
Pin Leakage				100	µA	
VIH	Input High Voltage	0.83			V	CMD/CTL
VIL	Input Low Voltage			0.55	V	CMD/CTL
Pin Leakage				50	µA	

NOTES:
1. V_{IL} is defined as the maximum voltage level at the receiving agent that will be received as a logical low value. DRAM_VREF is normally DRAM_VDD_S4/2
2. V_{IH} is defined as the minimum voltage level at the receiving agent that will be received as a logical high value. DRAM_VREF is normally DRAM_VDD_S4/2
3. V_{IH} and V_{OH} may experience excursions above DRAM_VDD_S4. However, input signal drivers must comply with the signal quality specifications.
4. RON is DRAM driver resistance whereas RTT_TERM is DRAM ODT resistance which is controlled by DRAM.
5.
6. DDR3L-1333 CLK buffer Ron is 26ohm and SR target is 4V/ns; DQ-DQS buffer Ron is 30ohms and SR target is 4V/ns; CMD/CTL buffer Ron is 20ohms and SR target is 1.8V/ns.

9.5.9 Intel® HD Audio DC Specification

Table 92. HDA Signal Group DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit	Notes
VCC_{HDA}	HDA Supply Voltage		HDA_LPE_V1P5V1P8_S3			
V_{IH_HDA}	Input High Voltage		$0.6*VCC_{HDA}$		V	
V_{IL_HDA}	Input Low Voltage			$0.4*VCC_{HDA}$	V	
V_{OH_HDA}	Output High Voltage	Iout = -500µA	$0.9*VCC_{HDA}$		V	
V_{OL_HDA}	Output Low Voltage	Iout = 1500µA		$0.1*VCC_{HDA}$	V	
IIL_HDA	Input Leakage Current	$0<Vin<VCC_{HDA}$		±175	µA	1
C_{IN_HDA}	Input Pin Capacitance			7.5	pF	
L_{PIN_HDA}	Pin Inductance			20	nH	2

NOTES:
1. For HDA_SDI[x] buffers (or in general any bidirectional buffer with tri-state output), input leakage current also include hi-Z output leakage.
2. This is a recommendation, not an absolute requirement.

9.5.10 USB 2.0 Host DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
Supply Voltage:						
VBUS	High-power Port	4.75		5.25	V	2
VBUS	Low-power Port					
Supply Current:						
ICCPRT	High-power Hub Port (out)	500			mA	
ICCUPT	Low-power Hub Port (out)	100			mA	
ICCHPF	High-power Function (in)			500	mA	
ICCLPF	Low-power Function (in)			100	mA	
ICCINIT	Unconfigured Function/Hub (in)			100	mA	
ICCSH	Suspended High-power Device			2.5	mA	15
ICCSL	Suspended Low-power Device			500	µA	
Input Levels for Low-/full-speed:						
VIH	High (driven)	2.0			V	4
VIHZ	High (floating)	2.7		3.6	V	4
VIL	Low			0.8	V	4
VDI	Differential Input Sensitivity	0.2			V	|(D+)-(D-)|;Figure; Note 4
VCM	Differential Common Mode Range	0.8		2.5	V	Includes VDI range; Figure; Note 4
Input Levels for High-speed:						
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	100		150	mV	
VHSDSC	High speed disconnect detection threshold (differential signal amplitude)	525		625	mV	
	High-speed differential input signaling levels					
VHSCM	High-speed data signaling common mode voltage range (guideline for receiver)	-50		500	mV	
Output Levels for Low-/full-speed:						
VOL	Low	0.0		0.3	V	4,5

Symbol	Parameter	Min	Typ	Max	Units	Notes
VOH	High (Driven)	2.8		3.6	V	4,6
VOSE1	SE1	0.8			V	
VCRS	Output Signal Crossover Voltage	1.3		2.0	V	10
Output Levels for High-speed:						
VHSOI	High-speed idle level	-10		10	mV	
VHSOH	High-speed data signaling high	360		440	mV	
VHSOL	High-speed data signaling low	-10		10	mV	
VCHIRPJ	Chirp J level (differential voltage)	700		1100	mV	
VCHIRPK	Chirp K level (differential voltage)	-900		-500	mV	
Decoupling Capacitance:						
CHPB	Downstream Facing Port Bypass Capacitance (per hub)	120			μF	
CRPB	Upstream Facing Port Bypass Capacitance	1.0		10.0	μF	9
Input Capacitance for Low-/full-speed:						
CIND	Downstream Facing Port			150	pF	2
CINUB	Upstream Facing Port (w/o cable)			100	pF	3
CEDGE	Transceiver edge rate control capacitance			75	pF	
Input Impedance for High-speed:						
	TDR spec for high-speed termination					
Terminations:						
RPU	Bus Pull-up Resistor on Upstream Facing Port	1.425		1.575	kΩ	1.5 kΩ ±5%
RPD	Bus Pull-down Resistor on Downstream Facing Port	14.25		15.75	kΩ	1.5 kΩ ±5%
ZINP	Input impedance exclusive of pull-up/pull-down (for low-/full speed)	300			kΩ	
VTERM	Termination voltage for upstream facing port pull-up (RPU)	3.0		3.6	V	
Terminations in High-speed:						
VHSTERM	Termination voltage in high speed	-10		10	mV	

NOTES:
1. Measured at A plug.
2. Measured at A receptacle.
3. Measured at B receptacle.

4. Measured at A or B connector.
5. Measured with RL of 1.425 kΩ to 3.6 V.
6. Measured with RL of 14.25 kΩ to GND.
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target VBUS drop of 330 mV.
10. Excluding the first transition from the Idle state.
11. The two transitions should be a (nominal) bit time apart.
12. For both transitions of differential signaling.
13. Must accept as valid EOP.
14. Single-ended capacitance of D+ or D- is the capacitance of D+/D- to all other conductors and, if present, shield in the cable. That is, to measure the single-ended capacitance of D+, short D-, VBUS, GND, and the shield line together and measure the capacitance of D+ to the other conductors.
15. For high power devices (non-hubs) when enabled for remote wakeup.

9.5.11 USB 3.0 DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	199.94		200.06	ps	1
$V_{TX\text{-}DIFF\text{-}PP}$	Differential peak-peak Tx voltage swing	0.9	1	1.05	V	
$V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$	Low-Power Differential peak-peak Tx voltage swing	0.4		1.2	V	2
$V_{TX\text{-}DE\text{-}RATIO}$	Tx De-Emphasis	3.45	3.5	3.65	dB	
$R_{TX\text{-}DIFF\text{-}DC}$	DC differential impedance	88		92	Ω	
$V_{TX\text{-}RCV\text{-}DETECT}$	The amount of voltage change allowed during Receiver Detection			0.6	V	3
$C_{AC\text{-}COUPLING}$	AC Coupling Capacitor	75		200	nF	4
$t_{CDR\_SLEW\_MAX}$	Maximum slew rate			10	ms/s	

NOTES:
1. The specified UI is equivalent to a tolerance of 300ppm for each device. Period does not account for SSC induced variations.
2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
3. Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an “off” receiver's input goes below output.
4. All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

9.5.12 SATA DC Specification

Table 93. SATA TX/RX Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IMIN_Gen1i}	Minimum Input Voltage for 1.5 Gb/s	325	-	mVdiffp-p	1
V_{IMAX_Gen1i}	Maximum Input Voltage for 1.5 Gb/s	-	600	mVdiffp-p	1
V_{IMIN_Gen2i}	Minimum Input Voltage for 3 Gb/s	275	-	mVdiffp-p	2
V_{IMAX_Gen2i}	Maximum Input Voltage for 3 Gb/s	-	750	mVdiffp-p	2
$V_{OMIN\_Gen1i,m}$	Minimum Output Voltage for 1.5 Gb/s	400	-	mVdiffp-p	3
$V_{OMAX\_Gen1i,m}$	Maximum Output Voltage for 1.5 Gb/s	-	600	mVdiffp-p	3
$V_{OMIN\_Gen2i,m}$	Minimum Output Voltage for 3 Gb/s	400	-	mVdiffp-p	3
$V_{OMAX\_Gen2i,m}$	Maximum Output Voltage for 3 Gb/s	-	700	mVdiffp-p	3

1. Applicable only when SATA port signaling rate is 1.5 Gb/s: SATA Vdiff, rx is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA_RXP[x] – SATA_RXN[x]|
2. Applicable only when SATA port signaling rate is 3 Gb/s: SATA Vdiff, rx is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA_RXP[x] – SATA_RXN[x]|
3. SATA Vdiff, tx is measured at the SATA connector on the transmit side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA_TXP[x] – SATA_TXN[x]|

For SATA_GP[x] and SATA_LED#, Please refer to the GPIO Buffer (1.8V) DC Specification in section "GPIO DC Specification".

9.5.13 PCU - SMBUS DC Specification

For SMBUS, Please refer to the GPIO Buffer (1.8V) DC Specification in section "GPIO DC Specification".

9.5.14 PCU - iLB - LPC DC Specification

Table 94. LPC Signal Group DC Specification (LPC_V1P8V3P3_S = 1.8V (ILB_LPC_AD][3:0], ILB_LPC_FRAME#, ILB_LPC_SERIRQ, ILB_LPC_CLKRUN#))

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	1.27	1.8	1.8 +0.1	V	
V_{IL}	Input Low Voltage	-0.1	0	0.58	V	
V_{OH}	Output High Voltage	0.9 x 1.8			V	
V_{OL}	Output Low Voltage			0.1 x 1.8	V	
I_{OH}	Output High Current		1.5		mA	

Table 94. LPC Signal Group DC Specification (LPC_V1P8V3P3_S = 1.8V (ILB_LPC_AD][3:0], ILB_LPC_FRAME#, ILB_LPC_SERIRQ, ILB_LPC_CLKRUN#))

Symbol	Parameter	Min	Typ	Max	Units	Notes
I_{OL}	Output Low Current		-0.5		mA	
I_{LEAK}	Input Leakage Current			30	µA	
C_{IN}	Input Capacitance	1		9	pF	

Table 95. LPC Signal Group DC Specification LPC_V1P8V3P3_S = 3.3V (ILB_LPC_AD[3:0], ILB_LPC_FRAME#, ILB_LPC_CLKRUN#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	0.5 x 3.3+ 0.7	3.3	3.3 +0.1	V	1
V_{IL}	Input Low Voltage	-0.1	0	0.5 x 3.3 - 0.7	V	2
V_{OH}	Output High Voltage	0.9 x 3.3			V	3
V_{OL}	Output Low Voltage			0.1 x 3.3	V	3
I_{OH}	Output High Current		1.5		mA	3
I_{OL}	Output Low Current		-0.5		mA	3
I_{LEAK}	Input Leakage Current			30	µA	
C_{IN}	Input Capacitance	1		9	pF	

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value, Applies to ILB_LPC_AD[3:0], ILB_LPC_CLKRUN#
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value. Applies to ILB_LPC_AD[3:0], ILB_LPC_CLKRUN#
3. V_{OH} is tested with Iout=500uA, V_{OL} is tested with Iout=1500uA
4. Applies to ILB_LPC_AD[3:0],ILB_LPC_CLKRUN# and ILB_LPC_FRAME#
5. ILB_LPC_SERIRQ is always a 1.8V I/O irrespective of the value of LPC_V1P8V3P3_S.

9.5.15 PCU - SPI (Platform Control Unit) DC Specification

Table 96. SPI Signal Group DC Specification (PCU_SPI_MISO, PCU_SPI_CS[1:0]#, PCU_SPI_MOSI, PCU_SPI_CLK)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage		PCU_1P8_G3		V	3
V_{IH}	Input High Voltage	0.5 *V_{REF}		V_{REF} + 0.5	V	2
V_{IL}	Input Low Voltage	-0.5		0.3 * V_{REF}	V	2
V_{OH}	Output High Voltage	0.9 * V_{REF}		1.8V	V	1
V_{OL}	Output Low Voltage			0.1 * V_{REF}	V	1
I_{OH}	Output High Current			1.5	mA	1
I_{OL}	Output Low Current	-0.5			mA	1

NOTES:
1. Applies to PCU_SPI_CS[1:0], PCU_SPI_CLK, PCU_SPI_MOSI
2. Applies to PCU_SPI_MISO and PCU_SPI_MOSI
3. The I/O buffer supply voltage is measured at the SoC package pins. The tolerances shown are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a rolloff of 3 dB/decade above 20 MHz.

9.5.16 PCU - Power Management/Thermal (PMC) & iLB RTC DC Specification

Table 97. Power Management 1.8V Suspend Well Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PCU_1P8_G3			V	
V_{IH}	Input High Voltage	0.8*V_{REF}			V	1
V_{IL}	Input Low Voltage			0.5*V_{REF}	V	2
V_{OH}	Output High Voltage	0.9*V_{REF}		V_{REF}	V	1
V_{OL}	Output Low Voltage			0.1*V_{REF}	V	1

NOTES:
1. The data in this table apply to signals - PMC_ACPRESENT, PMC_BATLOW#, PMC_PLTRST#, PMC_PWRBTN#, PMC_SLP_S4#, PMC_SUS_STAT#, PMC_SUSCLK[3:0], PMC_SUSPWRDNACK
2. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
3. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 98. PMC_RSTBTN# 1.8V Core Well Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
VREF	I/O Voltage	UNCORE_V1P8_S3			V	
V_{IH}	Input High Voltage	0.8* VREF			V	1
V_{IL}	Input Low Voltage			0.5* VREF	V	2

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 99. Power Management & RTC Well Signal Group DC Specification (PMC_RSMRST#, PMC_CORE_PWROK, ILB_RTC_RST#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
VREF	I/O Voltage	RTC_VCC				
V_{IH}	Input High Voltage	2.0	-	VREF +0.5	V	1
V_{IL}	Input Low Voltage	- 0.5	-	0.78	V	2
I_I	Input leakage Current	0.1	1	100	µA	3

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. I_I (Tyical) is specified at 30°C. V_{IL} (Maximum) is specified at Tj_{MAX}.

Table 100. iLB RTC Well DC Specification (ILB_RTC_TEST#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	2.0	-	VREF + 0.5	V	1
V_{IL}	Input Low Voltage	- 0.5	-	0.78	V	1

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 101. ILB RTC Oscillator Optional DC Specification (ILB_RTC_X1)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	0.65	0.8	1.2	V	1
V_{IL}	Input Low Voltage			0.25	V	1

NOTES:
1. ILB_RTC_X1 DC specification is **only** used for applications with an active external clock source instead of a crystal. When a crystal is used (typical case) between ILB_RTC_X2 and ILB_RTC_X1, this spec is not used.

Table 102. PROCHOT# Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	CORE_V1P0_S3				
V_{IH}	Input High Voltage	$0.8*V_{REF}$		V_{REF}	V	1
V_{IL}	Input Low Voltage			$0.4*V_{REF}$	V	2
V_{OH}	Output High Voltage	$0.9*V_{REF}$		V_{REF}	V	
V_{OL}	Output Low Voltage			$0.1*V_{REF}$	V	

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

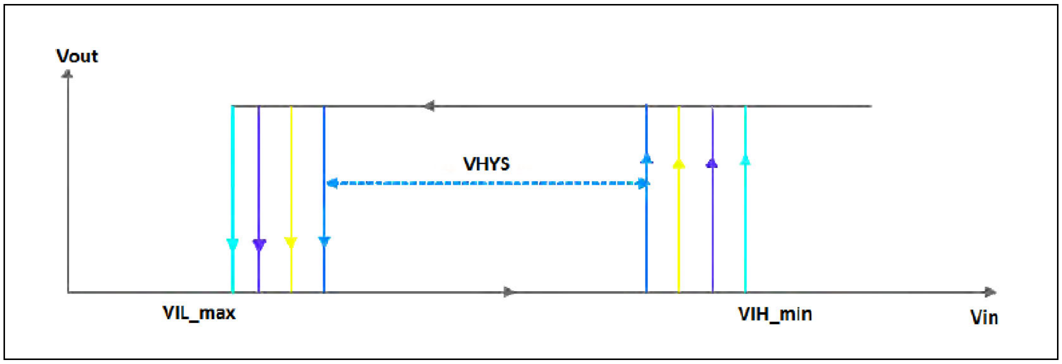
9.5.17 SVID DC Specification

Table 103. SVID Signal Group DC Specification (SVID_DATA, SVID_CLK, SVID_ALERT#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	SVID_V1P0_S3				
V_{IH}	Input High Voltage	$0.65*V_{REF}$			V	1
V_{IL}	Input Low Voltage			$0.44*V_{REF}$	V	1
V_{OH}	Output High Voltage				V	1
V_{OL}	Output Low Voltage			$0.1*V_{REF}$	V	4
V_{HYS}	Hysteresis Voltage	0.05			V	
R_{ON}	BUffer on Resistance	10		20	Ω	2
I_L	Leakage Current	-100		100	μA	3
C_{PAD}	Pad Capacitance			4.0	pF	4
V_{PIN}	Pin Capacitance			5.0	pF	

NOTES:
1. SVID_V1P0_S3 refers to instantaneous voltage VSS_SENSE
2. Measured at 0.31 * SVID_V1P0_S3
3. V_{IN} between 0V and SVID_V1P0_S3
4. CPAD includes die capacitance only. No package parasitic included.

Figure 17. Definition of VHYS in Table 169



9.5.18 GPIO DC Specification

GPIO Buffer is used across various interfaces on the SoC such as, GPIOs, I^2C, I2S, SPI, SDIO, SVID, UART, JTAG and ULPI

Note: I_{OX}# -> Spec is used for those GPIO which does not have industrial spec. Those GPIO interfaces that have its own industrial spec shouldn't refer to this spec.

Table 104. GPIO 3.3V Core Well Signal Group DC Specification(GPIO_S0_SC[101:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	UNCORE_V3P3_S3				
V_{IH}	Input High Voltage	0.61* V_{REF}		1.24*V_{REF}	V	
V_{IL}	Input Low Voltage	-0.21*V_{REF}		0.24*V_{REF}	V	
V_{OH}	Output High Voltage	0.95* V_{REF}		V_{REF}	V	
V_{OL}	Output Low Voltage	0		0.1* V_{REF}	V	
V_{Hys}	Input Hysteresis	0.1			V	
I_L	Leakage Current			5	µA	
I_{OH}#	Output High Current			3	mA	
I_{OL}#	Output Low Current			-3	mA	
C_{LOAD}	Load Capacitance	2		75	pF	

Table 105. GPIO 3.3V Suspend Well Signal Group DC Specification (GPIO_S5[43:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V3P3_G3			V	
V_{IH}	Input High Voltage	0.61* V_{REF}		1.24*V_{REF}	V	
V_{IL}	Input Low Voltage	-0.21*V_{REF}		0.24*V_{REF}	V	
V_{OH}	Output High Voltage	0.95* V_{REF}		V_{REF}	V	
V_{OL}	Output Low Voltage	0		0.1* V_{REF}	V	

Table 105. GPIO 3.3V Suspend Well Signal Group DC Specification (GPIO_S5[43:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{Hys}	Input Hysteresis	0.1			V	
I_L	Leakage Current			5	µA	
I_{OH}#	Output High Current			3	mA	
I_{OL}#	Output Low Current			-3	mA	
C_{LOAD}	Load Capacitance	2		75	pF	

Table 106. GPIO 1.8V Core Well Signal Group DC Specification (GPIO_S0_SC[101:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	UNCORE_V1P8_S3				
V_{IH}	Input High Voltage	$0.65*V_{REF}$		$1.24*V_{REF}$	V	
V_{IL}	Input Low Voltage	$-0.21*V_{REF}$		$0.35 * V_{REF}$	V	
V_{OH}	Output High Voltage	V_{REF} -0.45		V_{REF}	V	
V_{OL}	Output Low Voltage	0		0.45	V	
V_{Hys}	Input Hysteresis	0.1			V	
I_L	Leakage Current			5	µA	
I_{OH}#	Output High Current			3	mA	
I_{OL}#	Output Low Current			-3	mA	
C_{LOAD}	Load Capacitance	2		75	pF	

Table 107. GPIO 1.8V Suspend Well Signal Group DC Specification (GPIO_S5[43:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V1P8_G3			V	
V_{IH}	Input High Voltage	$0.65*V_{REF}$		$1.24*V_{REF}$	V	
V_{IL}	Input Low Voltage	$-0.21*V_{REF}$		$0.35*V_{REF}$	V	
V_{OH}	Output High Voltage	V_{REF} - 0.45		V_{REF}	V	
V_{OL}	Output Low Voltage	0		0.45	V	
V_{Hys}	Input Hysteresis	0.1			V	
I_L	Leakage Current			5	µA	
I_{OH}#	Output High Current			3	mA	
I_{OL}#	Output Low Current			-3	mA	
C_{LOAD}	Load Capacitance	2		75	pF	

9.5.19 SIO - I^2C DC Specification

Table 108. I^2C Signal Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	UNCORE_V1P8_S3			V	
V_{IH}	Input High Voltage	0.7 * V_{REF}		1.24*V_{REF}	V	
V_{IL}	Input Low Voltage	0.21*V_{REF}		0.3 * V_{REF}	V	
V_{OL}	Output Low Voltage	0		0.2 * V_{REF}	V	
V_{Hys}	Input Hysteresis	0.1			V	
C_{PIN}	Pin Capacitance	2		5	pF	

9.5.20 SIO - UART DC Specification

Refer to the GPIO Buffer (1.8V) DC Specification, mentioned Section 106, "GPIO 1.8V Core Well Signal Group DC Specification (GPIO_S0_SC[101:0])" on page 152

9.5.21 I^2S (Audio) DC Specification

Refer to the GPIO Buffer (1.8V) DC Specification, mentioned Section 107, "GPIO 1.8V Suspend Well Signal Group DC Specification (GPIO_S5[43:0])" on page 152

9.6 AC Specifications

The timings specified in this section are defined at the SoC pads. Therefore, proper simulation of the signals is the only means to verify proper timing and signal quality.

See Chapter 2, "Physical Interfaces" for signal definitions and Chapter 10, "Ballout and Package Information" for the ball map. Generic timing diagrams can be found in "General AC Timing Diagrams".

The timings specified in this section should be used in conjunction with the SoC signal integrity models provided by Intel.

See the following DC Specifications in this section:

- "Integrated Clock 25 MHz Crystal AC Specification"
- "Platform Clocks AC Specification"
- "SVID AC Specification"
- "DDR3L Memory Controller AC Specification"
- "Display AC Specifications"
- "MIPI-Camera Serial Interface (CSI) AC Specification"
- "SCC - SD Card AC Specification"
- "SSC - SDIO AC specification"

- "SCC - eMMC 4.5 AC Specification"
- "SATA AC Specification"
- "USB 3.0 AC Specification"
- "ULPI USB 2.0 Device AC Specification"
- "Intel® HD Audio AC Specification"
- "I^2S (Audio) AC Specification"
- "PCI Express* AC Specification"
- "PCU - PMC - Suspended Clock AC Specification"
- "1. SUSCLK duty cycle can range from 30% minimum to 70% maximum."
- "PCU - SPI NOR AC Specification"
- "PCU - iLB - LPC AC Specification"
- "SIO - I^2C AC Specifications"
- "SIO - UART AC Specification"
- "JTAG AC Specification"

Note: Care should be taken to read all notes associated with a particular timing parameter.

9.6.1 Integrated Clock 25 MHz Crystal AC Specification

See"Crystal Specifications" for crystal selection.

9.6.2 Generic Clock Jitter AC Specification

Applies to the following clocks unless overridden below: SIO_I2C[0:6]_CLK, PMC+PLT_CLK[0:6], SIO_SPI_CLK, LPE_I2S[0:2]_CLK, TAP_CLK, PCU_SPI_CLK, ILB_LPC_CLK[0:1], SD3_CLK, SD2_CLK, MMC1_CLK, HDA_CLK, SVID_CLK, DDI[0:1]_DDCCLK, VGA_DDCLK.

Table 109. Generic Clock Jitter AC Specification

Symbol	Parameter	Min.	Typ	Max.	Unit	Notes
$T_{RISE/FALL}$	Minimum and Maximum Rise/Fall Time	1.5		20	ns	1, 3
T_{DC}	Duty Cycle	45		55	%	2
$T_{PEAKJIT}$	Peak Jitter (cycle to cycle)			300	ps	2
T_{PERJIT}	Period Jitter (peak to peak)			500	ps	4
T_{TIE}	Time Interval Error (peak to peak)			400	ps	5
T_{LONG}	Long Term Accuracy	-100		100	ps	

NOTES:
1. Edge Rate is measured from 10%-90% of supply voltage.
2. Cycle to cycle jitter measure for 100K samples.

3. Based on trace length of 25–200 mm, total maximum far end capacitance of 5 pF, EDS of 10 pF and board impedance of 30–75 Ω.
4. Period jitter value is measured by adjusting an oscilloscope to display a little more than one complete clock cycle with the display set to infinite persistence. Scope trigger is set on the first edge, and the period jitter is captured by measuring spread/peak-peak value of the second edge. 100K samples.
5. The TIE is estimated by measuring how far each active edge of the clock varies from its ideal position. 100K samples.

9.6.3 Platform Clocks AC Specification

Table 110. 25 MHz Platform Clock AC Specification

Symbol	Parameter	Min.	Typ	Max.	Unit	Notes
F_{PLT}	Frequency		25		MHz	
T_{DC}	Duty Cycle	45		55	%	
$T_{RISE/FALL}$	Minimum and Maximum Rise/Fall Time	5		20	ns	
V_{SWING}	Voltage Swing		1.8		V	
$T_{PEAKJIT}$	Peak Jitter (c-c)	-300		300	ps	
T_{PERJIT}	Period Jitter			500	ps	

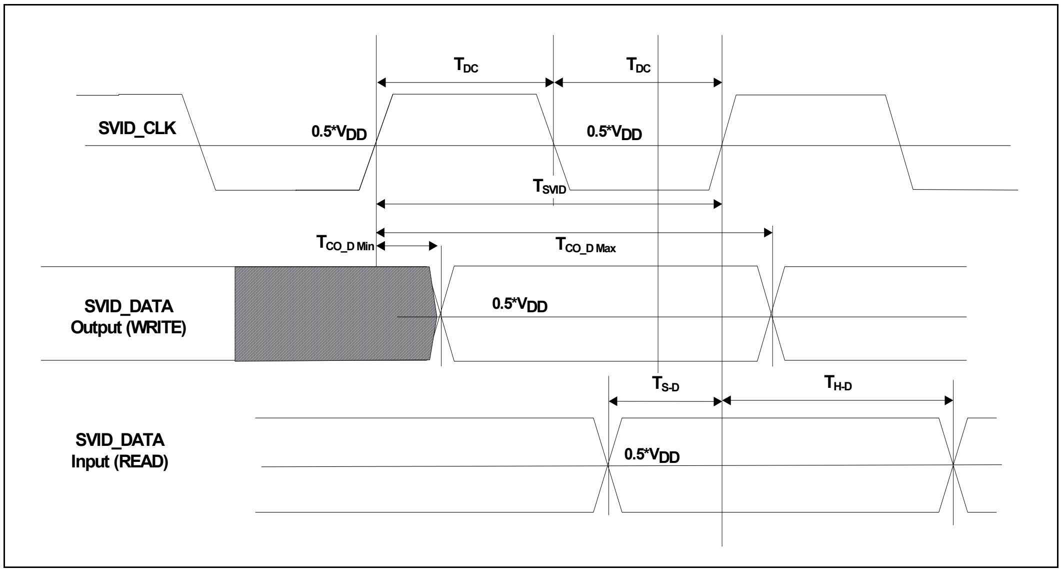
9.6.4 SVID AC Specification

Table 111. SVID AC Specification

Symbol	Parameter	Min.	Max.	Unit	Figure	Notes
F_{SVID}	SVID_CLK Frequency		25	MHz	18	
T_{DC}	SVID_CLK Duty Cycle	45	55	%		
T_{S_D}	SVID_DATA Input Setup Time	-2		ns	18	
T_{H_D}	SVID_DATA Input Hold Time	9		ns	18	
T_{CO_D}	Rising edge SVID_CLK to SVID_DATA Output	0	5	ns	18	
TRISE/ FALL	Minimum and Maximum Rise/Fall Time	0	5	ns		1, 2

NOTES:
1. Based on trace length of 0.2–4 inches, total maximum far end capacitance of 5 pF and board impedance of 25–75 Ω.
2. Measured from 30–70%

Figure 18. SVID Timing Diagram



9.6.5 DDR3L Memory Controller AC Specification

Note: The contents of this section are only valid for DRAM_VDD_S4 = 1.35V

Table 112. DDR3L Interface Timing Specification (Sheet 1 of 3)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
DDR3L Electrical Characteristic and AC timings at 1066 MT/s						
T_{SLR_D}	DQ, DQSP, DQSN Input Slew Rate	3	5.5	V/ns		
System Memory Clock Timings						
$T_{CK(AVG)}$	Average CK Period		1.875	ns		
T_{CH}	Average CK High Time	0.45		tCKAVG		
T_{CL}	Average CK Low Time	0.45		tCKAVG		
T_{SKEW}	Skew between any System Memory Differential Clock Pair (CKP/CKN)		30	ps		
System Memory Command Signal Timings						
T_{CMD} (tCMDVB+tCMDVA)	Total CMD Buffer window available for command buffers (RAS#, CAS#, WE#, BS[2:0], MA)	1380		ps		1
System Memory Control Signal Timings						

Table 112. DDR3L Interface Timing Specification (Sheet 2 of 3)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T_{CTL} (tCTLVB + tCTLVA)	Total Control buffer Window available for Control buffers (CS#, CKE)	1400		ps		2
System Memory Data and Strobe Signal Timings						
$T_{DVB}+T_{VDA}$	Data, DQ and DM timing window available at the interface output for write commands. tDVB is data available before strobe and tDVA is data available after corresponding slope.	645		ps		3
$T_{SU} + T_{HD}$	Data, DQ Input Setup Plus Hold Time requirement for successful Read operation. These Setup and Hold numbers are measured w.r.t. corresponding strobe or Falling Edge	310		ps		4
T_{DQSS}	Strobe to rising clock edge during write.	-120		120	ps	
T_{WPRE}	DQSP/N Preamble duration (one dummy cycle)	0.9		tCKAVG		
T_{WPST}	DQSP/N Postamble Duration	0.4		tCKAVG		
DDR3L Electrical Characteristic and AC timings at 1333 MT/s. DRAM_VDD_S4 = 1.35 V						
T_{SLR_D}	DQ, DQSP, DQSN Input Slew Rate	3	5.5	V/ns		
System Memory Clock Timings						
$T_{CK(AVG)}$	Average CK Period		1.5	ns		
T_{CH}	Average CK High Time	0.45		tCKAVG		
T_{CL}	Average CK Low Time	0.45		tCKAVG		
T_{SKEW}	Skew between any System Memory Differential Clock Pair (CKP/CKN)		30	ps		
System Memory Command Signal Timings						
T_{CMD} (tCMDVB+tCMDVA)	Total CMD Buffer window available for command buffers (RAS#, CAS#, WE#, BS[2:0], MA)	1075		ps		1
System Memory Control Signal Timings						
T_{CTL} (tCTLVB + tCTLVA)	Total Control buffer Window available for Control buffers (CS#, CKE)	1125		ps		2
System Memory Data and Strobe Signal Timings						

Table 112. DDR3L Interface Timing Specification (Sheet 3 of 3)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
$T_{DVB}+T_{VDA}$	Data, DQ and DM timing window available at the interface output for write commands. tDVB is data available before strobe and tDVA is data available after corresponding slope.	495		ps		3
$T_{SU} + T_{HD}$	Data, DQ Input Setup Plus Hold Time requirement for successful Read operation. These Setup and Hold numbers are measured w.r.t. corresponding strobe or Falling Edge	255		ps		4
T_{DQSS}		-120		120	ps	
T_{WPRE}	DQSP/N Preamble duration (one dummy cycle)	0.9		tCKAVG		
T_{WPST}	DQSP/N Postamble Duration	0.4		tCKAVG		

NOTES:
1. The CMD time is measured w.r.t. differential crossing of DRAM_CKP and DRAM_CKN. The tCMDVB and tCMDVA will be adjusted for proper CMD Setup and Hold time requirement at DRAM. The command timing assumes CMD-1N Mode.
2. The CTL time is measured w.r.t. differential crossing of DRAM_CKP and DRAM_CKN. The tCTLVB and tCTLVA will be adjusted for proper CTL Setup and Hold time requirement at DRAM.
3. The accurate strobe placement using write training algorithm will be performed which will guarantee the required Data setup/hold time w.r.t. strobe differential crossing at the DRAM input.
4. The Read training algorithm will center the DQS internally inside DRAM interface in order to have equal tSU and tHD timings.
5. All the timing windows are measured at 50% of the respective DRAM signal swing.

Figure 19. DDR3L DQ Setup/Hold Relationship to/from DQSP/DQSN (Read Operation)

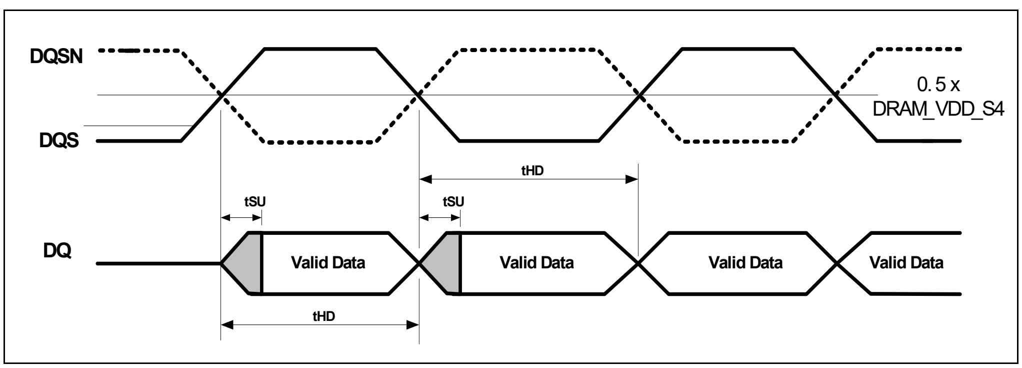


Figure 20. DDR3L DQ and DM Valid before and after DQSP/DQSN (Write Operation)

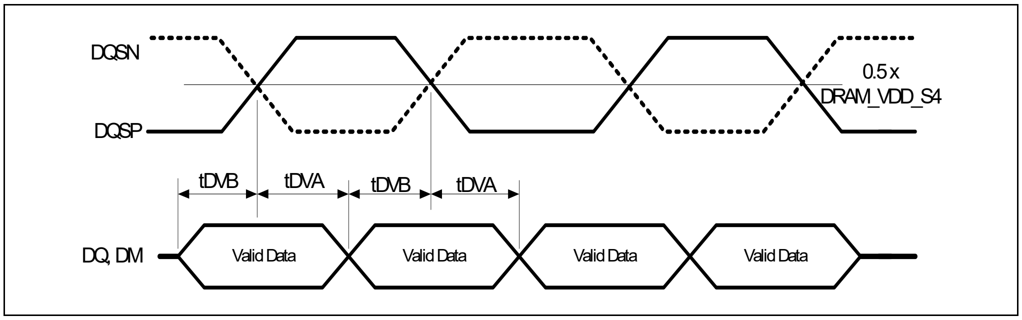


Figure 21. DDR3L Write Pre-amble Duration

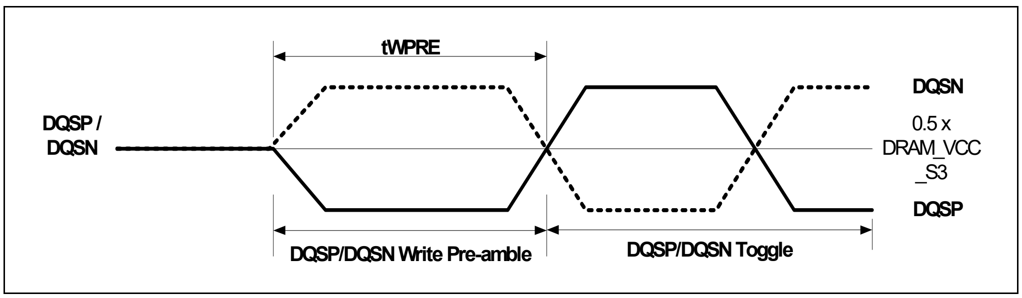


Figure 22. DDR3L Write Post-amble Duration

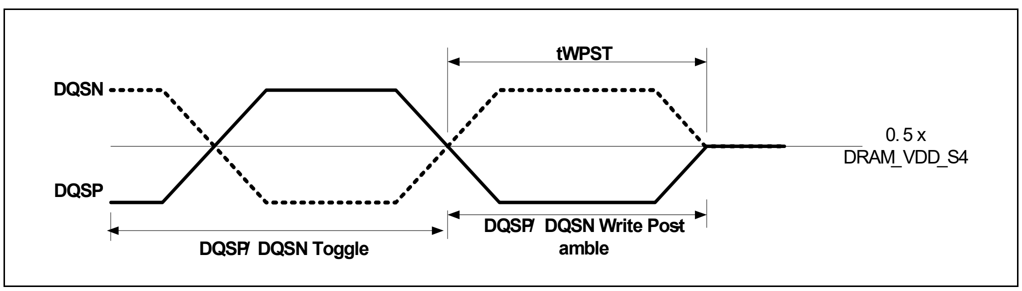


Figure 23. DDR3L Command Signals Valid before and after CK Rising Edge

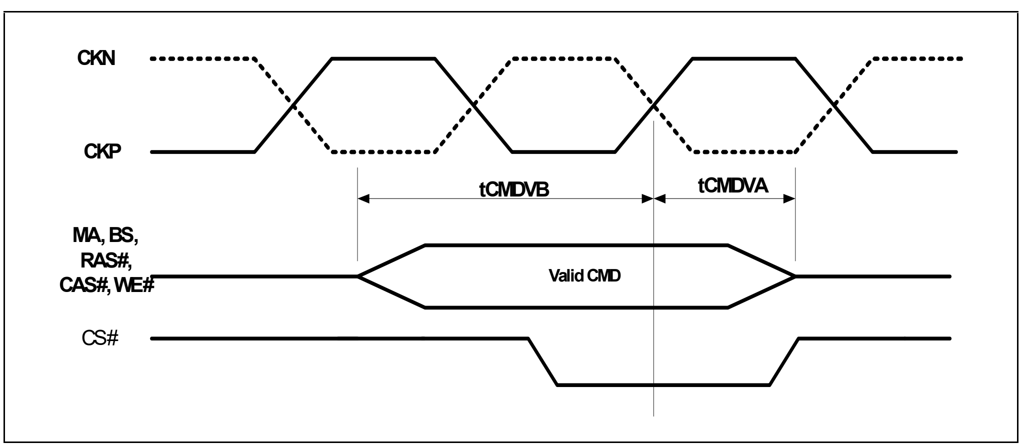


Figure 24. DDR3L CKE Valid before and after CK Rising Edge

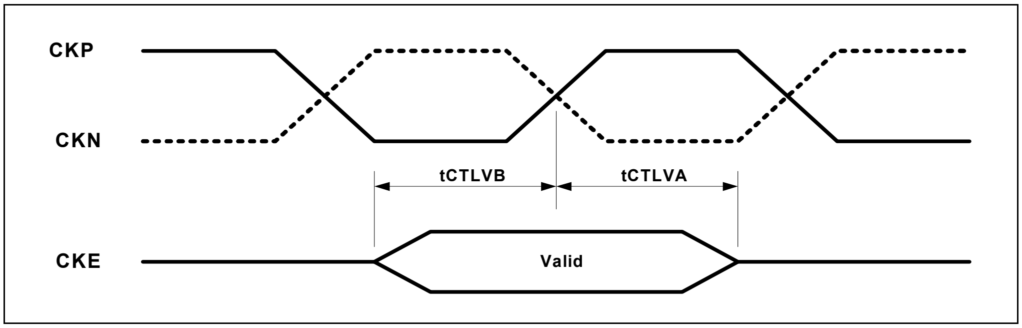


Figure 25. DDR3L CS# Valid before and after CK Rising Edge

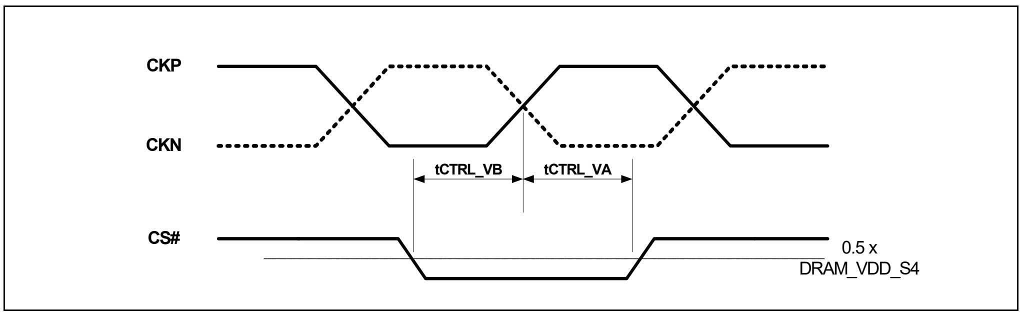


Figure 26. DDR3L ODT Valid before CK Rising Edge

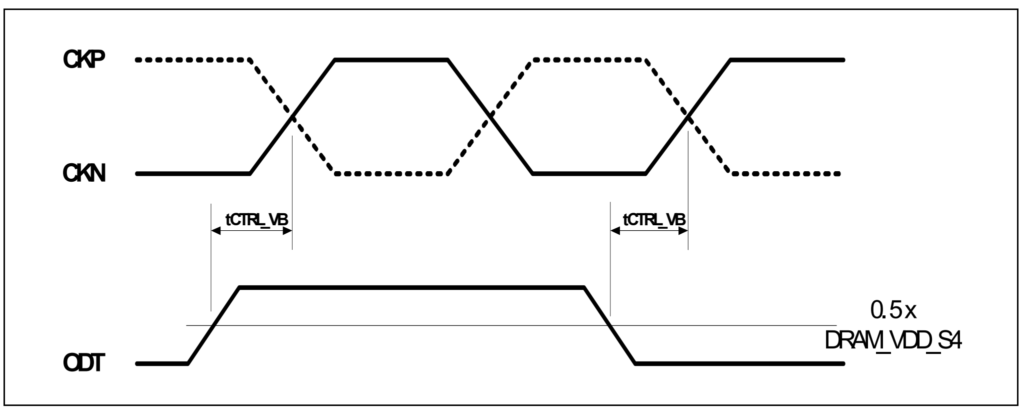


Figure 27. DDR3L Clock Cycle Time

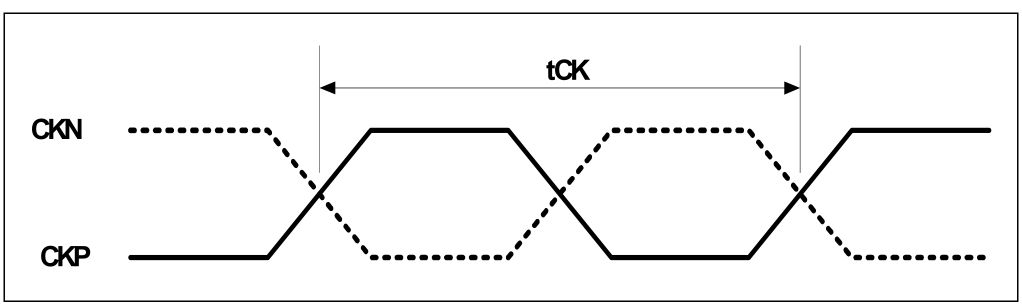
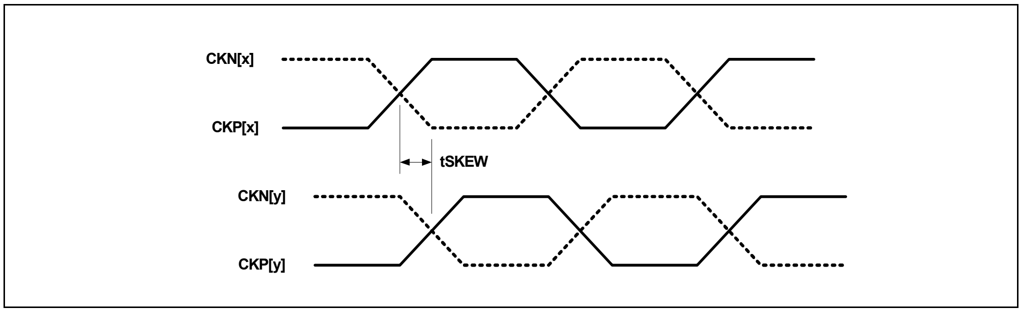


Figure 28. DDR3L Skew between System Memory Differential Clock Pairs (CKP/CKN)



NOTE: x represents one differential clock pair, and y represents another differential clock pair within same channel.

Figure 29. DDR3L CK High Time

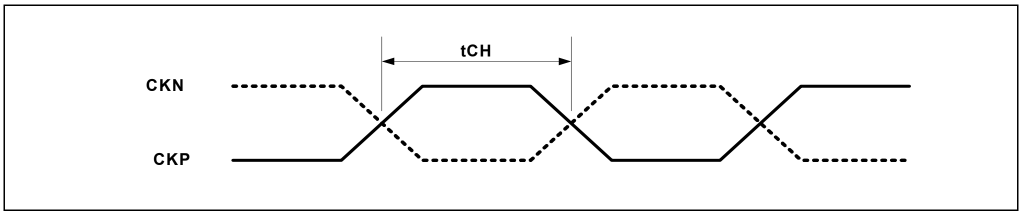


Figure 30. DDR3L CK Low Time

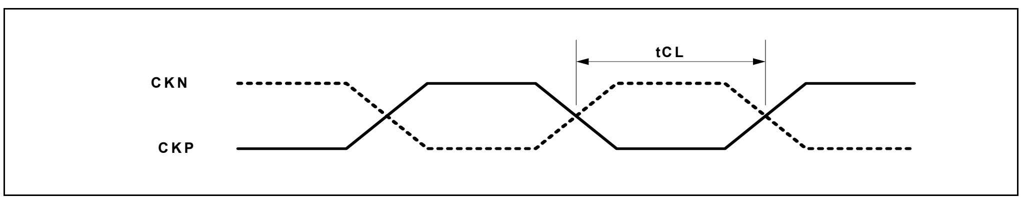


Figure 31. DDR3L DQS Falling Edge Output Access Time to CK Rising Edge

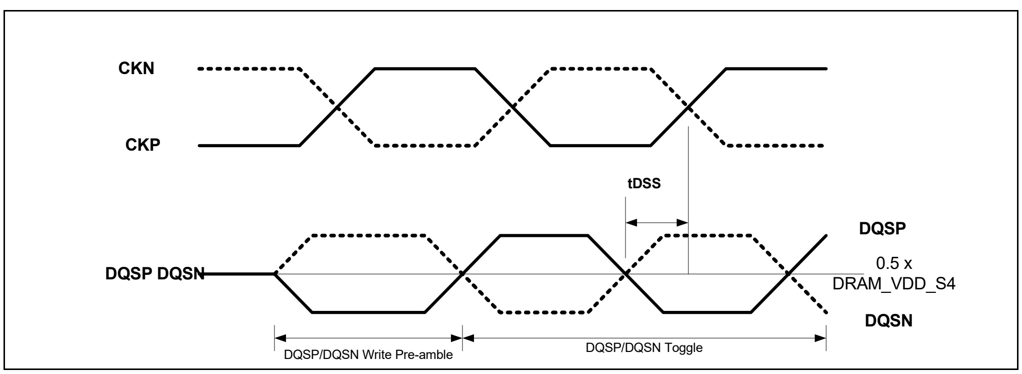


Figure 32. DDR3L DQS Falling Edge Output Access Time From CK Rising Edge

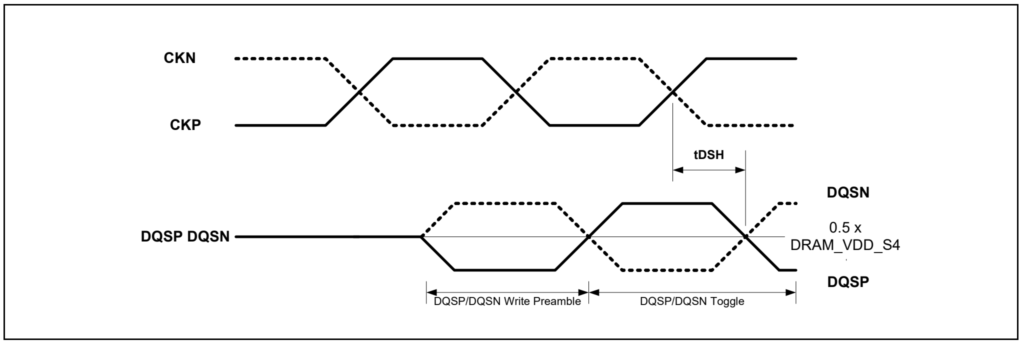
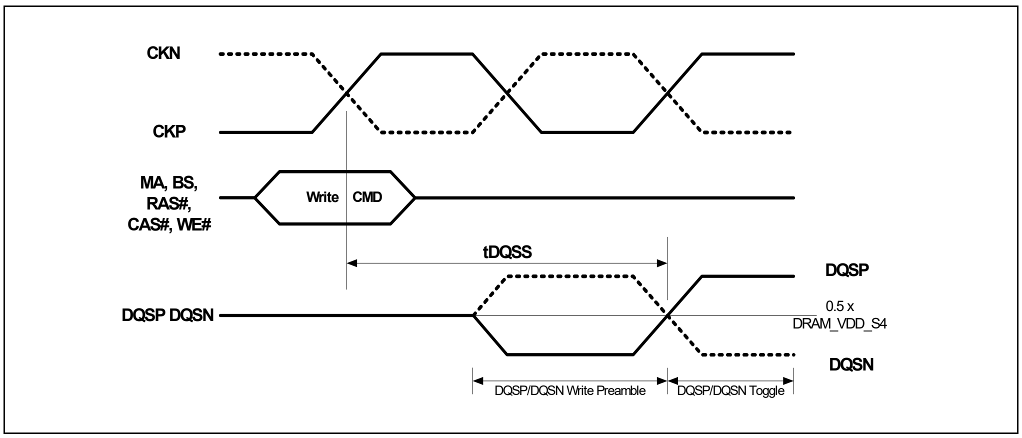


Figure 33. DDR3L CK Rising Edge Output Access Time to the 1st DQS Rising Edge



9.6.6 Display AC Specifications

9.6.6.1 DDI Main Transmitter AC specification

Table 113. DDI Main Transmitter AC specification (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	1
f_{RBR}	Frequency for Reduced Bit Rate	1.61141	1.62	1.620048	Gbps	1
UI_High_Rate	Unit Interval for high bit rate (2.7 Gbps / lane)		370		ps	1
UI_Low_Rate	Unit Interval for high bit rate (1.62 Gbps / lane)		617		ps	1
Down_Spread_Amplitude	Link clock down Spreading	0		0.5	%	2
Down_Spread_Frequency	Link Clock down Spreading Frequency	30		33	kHz	3

Table 113. DDI Main Transmitter AC specification (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
$T_{TX\text{-}EYE\_CHIP\_High\_Rate}$	Minimum TX Eye Width at Tx package pins	0.72			UI	4
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER\_CHIP\_\_High\_Rate}$	Maximum time between the jitter median and maximum deviation from the median at Tx package pins			0.147	UI	4
$T_{TX\text{-}EYE\_CHIP\_Low\_Rate}$	Minimum TX Eye Width at Tx package pins	0.82			UI	5
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER\ CHIP\ Low\_Rate}$	Maximum time between the jitter median and maximum deviation from the median at Tx package pins			0.09	UI	5
$T_{TX\text{-}RISE\_CHIP}$, $T_{TX\text{-}FALL\_CHIP}$	D+/D- TX Output Rise/Fall Time at Tx package pins	50		130	ps	6
ITX-SHORT	TX Short Circuit Current Limit			50	mA	7
$L_{TX\text{-}SKEWINTER\_PAIR}$	Lane-to-Lane Output Skew at Tx package pins			2	UI	
$L_{TX\text{-}SKEWINTRA\_PAIR}$	Lane Intra-pair Output Skew at Tx package pins			20	ps	
$T_{TX\text{-}RISE\_FALL\_MISMATCH\_CHIPDIFF}$	Lane Intra-pair Rise-fall Time Mismatch at Tx package pins.			5	%	8
$F_{TX\text{-}REJECTION\text{-}BW}$	Clock Jitter Rejection Bandwidth			4	MHz	9
$V_{TX\text{-}AC\text{-}CM}$	TX AC Common Mode Voltage			20	mV	2
C_{TX}	AC Coupling Capacitor	75		200	nF	11
T_{RISE}/T_{FALL}	Rise time/ Fall time (20%-80%)	75		-	ps	
$V_{UNDERSHOOT}$	Undershoot, max			0.25 of full differential amplitude		
$L_{TX\text{-}SKEWINTER\_PAIR}$	Intra-Pair skew at source connector			0.15 UI	ps	
$L_{TX\text{-}SKEWINTRA\_PAIR}$	Intra-Pair skew at source connector			1.212	ns	12
	Clock duty cycle, min/average/max	40	50	60	%	
	TMDS differential Clock Jitter			0.25	UI	

NOTES:
1. Frequency High limit = +300ppm; Low limit = -5300ppm
2. Range: 0% ~ 0.5% when downspread enabled
3. Range: 30 kHz ~33 kHz when downspread enabled.
4. For High Bit Rate.
5. For Reduced Bit Rate.
6. At 20 to 80
7. Total drive current of the transmitter when it is shorted to its ground.
8. Informative. D+ rise to D- fall mismatch and D+ fall to D- rise mismatch.

9. Informative. Transmitter jitter must be measured at source connector pins using a signal analyzer that has a 2nd order PLL with tracking bandwidth of 20MHz (for D10.2 pattern) and damping factor of 1.428.
10. Measured at 1.62 GHz and 2.7 GHz (if supported), within the frequency tolerance range. Time-domain measurement using a spectrum analyzer.
11. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.
12. 0.20* Tcharacter @165MHz

Table 114. DDI AUX Channel AC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
UI	AUX Unit Interval	0.4	0.5	0.6	µs	1
$T_{AUX-BUS-PARK}$	AUX CH bus park time	10			ns	2
$T_{CYCLE-to-CYCLE}$ Jitter	Maximum allowable UI variation within a single transaction at connector pins of a transmitting Device			0.08	UI	3
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a transmitting Device			0.04	UI	4
I_{AUX_SHORT}	AUX Short Circuit Current Limit			90	mA	5
C_{AUX}	AC Coupling Capacitor	75		200	nF	6

NOTES:
1. Results in the bit rate of 1Mbps including the overhead of ManchesterII coding.
2. Period after the AUX CH STOP condition for which the bus is parked
3. Equal to 48 ns maximum. The transmitting Device is a Source Device for a Request transaction and a Sink Device for a Reply Transaction
4. Equal to 24 ns maximum. The transmitting Device is a Source Device for a Request transaction and a Sink Device for a Reply Transaction.
5. Total drive current of the transmitter when it is shorted to its ground.
6. The AUX CH AC-coupling capacitor placed on both the DP upstream and downstream devices.

9.6.6.2 Analog VGA Display AC Specification

The VGA DAC (digital-to-analog converter) consists of three identical 8-bit DACs to provide red, green, and blue color components. Each DAC can output a current from 0 to 255 units of current, where one unit of current (LSB) is defined based on the VESA video signal standard.

Table 115. R,G,B / VGA DAC Display AC Specification (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
Pixel Clock Frequency = 300 MHz						
T_{RISE}	R,G,B Video Rise TIme	0.33		1.67	ns	1,2,8 (10-90% of “black”-to-”white” video transition)
T_{FALL}	R,G,B Video Fall TIme	0.33		1.67	ns	1,3,8 (90-10% of “black”-to-”white” video transition)
$T_{SETTLING}$	Settling time		1.0		ns	1,4,8
VO	Video Channel-to-Channel output skew		0.833		ns	1,5,8
	Overshoot/ Undershoot	-0.084		+0.084	V	1,6,8 (0.7V full-scale voltage step)

Table 115. R,G,B / VGA DAC Display AC Specification (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
	Noise Injection Ratio		2.5		%	
Pixel Clock Frequency = 350 MHz						
T_{RISE}	R,G,B Video Rise TIme	0.286		1.43	ns	1,2,8 (10-90% of "black"-to-"white" video transition)
T_{FALL}	R,G,B Video Fall TIme	0.286		1.43	ns	1,3,8 (90-10% of "black"-to-"white" video transition)
$T_{SETTLING}$	Settling time		0.857		ns	1,4,8
VO	Video Channel-to-Channel output skew		0.714		ns	1,5,8
	Overshoot/ Undershoot	-0.084		+0.084	V	1,6,8 (0.7V full-scale voltage step)
	Noise Injection Ratio		2.5		%	

NOTES:
1. Measured at each R,G,B termination according to the VESA Test Procedure - Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. R,G,B Max Video Rise/Fall Time: 50% of minimum pixel clock period
3. R,G,B Min Video Rise./Fall Time: 10% of minimum pixel clock period
4. Max settling time: 30% of minimum pixel clock period
5. Video channel-to-channel output skew: 25% of minimum pixel clock period
6. Overshoot/Undershoot: ±12% of "black"-to-"white" video step function
7. Noise Injection Ratio: 2.5% of maximum luminance voltage (dc to max pixel clock frequency)
8. R,G,B AC parameters are strongly dependent on the board design & implementation: actual performance may differ from values noted above depending on board implementation.

Table 116. VGA_HSYNC and VGA_VSYNC AC Specification

Symbol	Parameter	Min	Max	Units	Notes[1]
T_F	Fall Time	--	80% of minimum pixel clock period	ns	
T_R	Rise Time	--	80% of minimum pixel clock period	ns	
--	Overshoot/Undershoot	--	30% of high level signal voltage range	mA	1
--	Jitter (measured between Hsync pulses)	--	One half of the difference between max and min interval <15% of the pixel clock, DC to max.	V	2

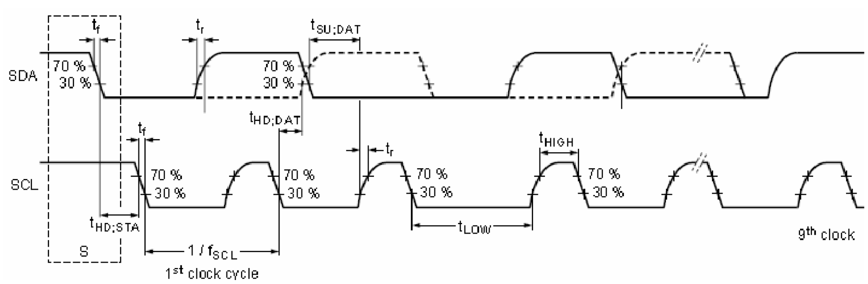
NOTES:
1. No signal non-monotonicity / excursions allowed in the 0.5 to 2.4V range
2. Measured over 100,000 intervals. Horizontal refresh rate at all image format, worse-case screen patterns.

Table 117. VGA_DDCDATA, and VGA_DDCCLK Timing Specification

Symbol	Parameter	Standard mode 100kbits/s		Units	Figures
		Min	Max		
f_{SCL}	SCL Clock Frequency	0	100	kHz	34
t_{LOW}	Low Period of SCL Clock	4.7	--	µs	
t_{HIGH}	High Period of SCL Clock	4	--	µs	
t_R	Rise Time[1] of Both SDA and SCL Signals	--	1000	ns	
t_F	Fall Time[1] of Both SDA and SCL Signals	--	300	ns	
$t_{HD:DAT}$	Data Hold Time[3]	0	--	µs	
$t_{SU:DAT}$	Data Setup Time	250	--	ns	

NOTES:
1. Measurement point for rise and fall time: V_{IL}(min) - V_{IL}(max)
2. $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.

Figure 34. VGA_DDCDATA, and VGA_DDCCLK Timing Diagram



9.6.7 MIPI-Camera Serial Interface (CSI) AC Specification

Based on version 2 of the MIPI-CSI specification.

Table 118. MIPI-CSI-2 Receiver Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
MIPI HS-Receiver Mode						
$\Delta V_{CMRX(HF)}$	Common-mode interference above 450 MHz	–	–	100	mV	2, 9
$\Delta V_{CMTX(LF)}$	Common-mode interference between 50–450 MHz	-50	–	50	mV	1, 4
C_{CM}	Common-mode termination	–	–	60	pF	3

Table 118. MIPI-CSI-2 Receiver Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
S_{CDRX}	differential to common-mode	–	–	-26	dB	From 0 to fMAX (1.33Ghz)
MIPI LP-Receiver Mode						
e_{spike}	Input pulse rejection	–	–	300	V*ps	5, 6, 7
T_{MIN-RX}	Minimum pulse width response	20	–	–	ns	8
V_{INT}	Peak interference amplitude	–	–	200	mV	
f_{INT}	Interference frequency	450	–	–	MHz	

NOTES:

1. Excluding static ground shift of 50 mV.
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. For higher bit rates a 14 pF capacitor is needed to meet the common-mode return loss specification.
4. Voltage difference compared to the DC average common-mode potential.
5. Time-voltage integration of a spike above V_{IL} when in the LP-0 state or below V_{IH} when in the LP-1 state.
6. An impulse spike less than this will not change the receiver state.
7. In addition to the required glitch rejection, designers shall ensure rejection of known RF-interference.
8. An input pulse greater than this will toggle the output
9. Improves on DPHY specification, which requires 100 mV maximum.

Figure 35. Input Glitch Rejection of Low-Power Receivers

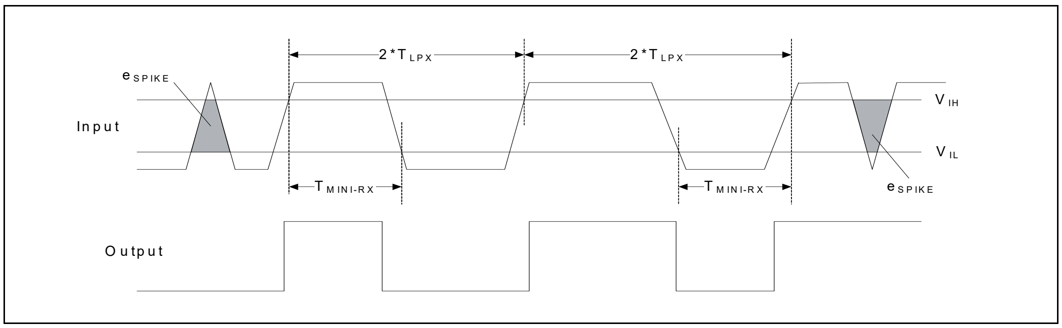


Table 119. MIPI-CSI-2 Clock Signal Specification

Symbol	Clock Parameter	Min.	Typ.	Max.	Unit	Notes
UI_{INST}	UI Instantaneous (In 1 or 2 or 3 or 4 Lane configuration)	1 (1Gbps/ 500Mhz)		2.77 (163 Mbps/ 80Mhz)	ns	1

NOTE: [1]The minimum UI shall not be violated for any single bit period, that is, any DDR half cycle within a data burst.

Figure 36. MIPI-CSI-2 Clock Definition

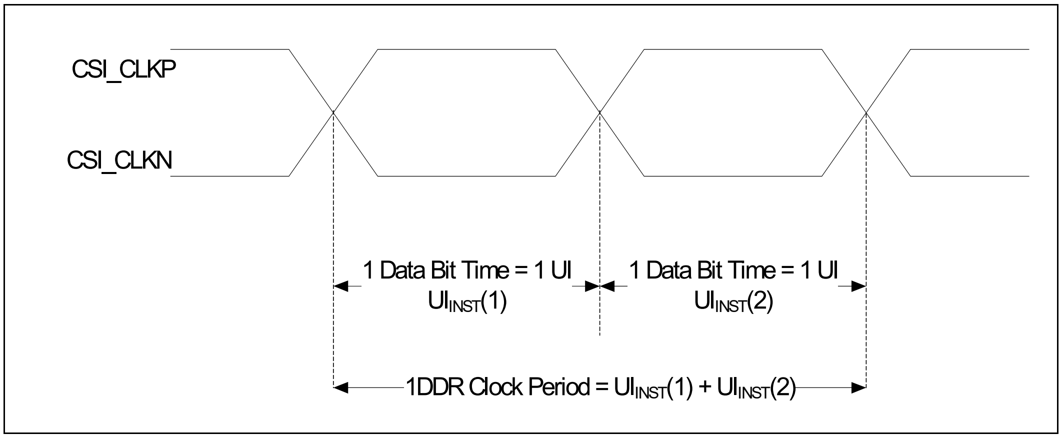
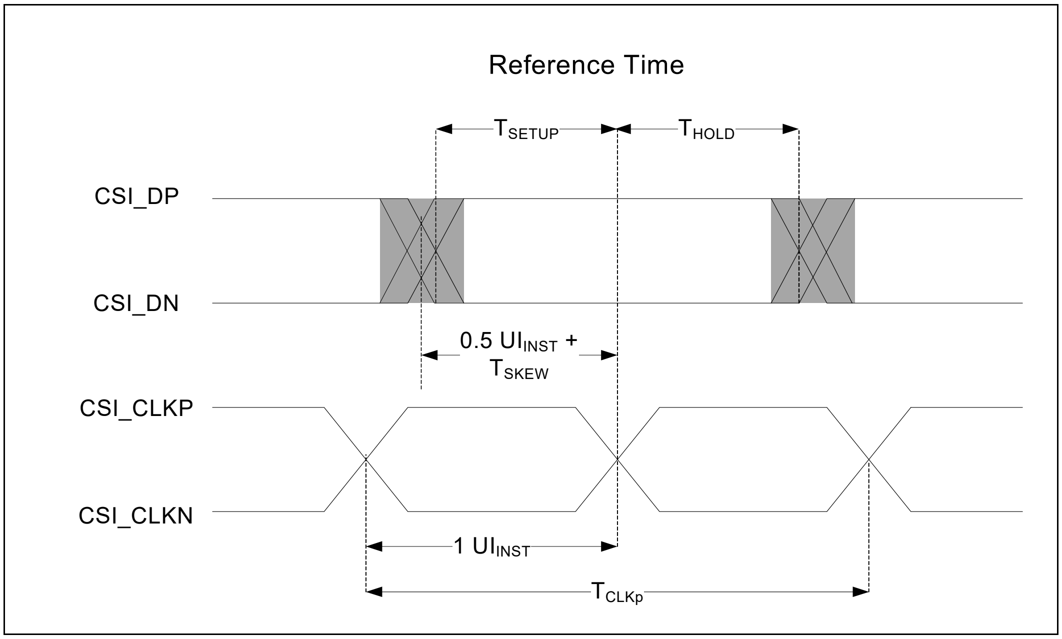


Table 120. MIPI CSI 2 Data Clock Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
TSETUP[RX]	Data to Clock Setup Time [receiver]	0.15	–	–	UI_{INST}	1, 2
THOLD[RX]	Clock to Data Hold Time [receiver]	0.15	–	–	UI_{INST}	1, 2

NOTES:
1. Total silicon and package delay budget of $0.3*UI_{INST}$
2. Total setup and hold window for receiver of $0.3*UI_{INST}$

Figure 37. MIPI-CSI-2 Data to Clock Timing Definitions



9.6.8 SCC - SD Card AC Specification

Table 121. SD Card AC Specification

Symbol	Parameter	Min.	Max.	Unit	Figure	Notes
$T_{wc(DDR50)}$	CLK cycle time for DDR50 Mode	19	–	ns	41	
$T_{wc(SDR25)}$	CLK cycle time for SDR25 Mode	19	–	ns	42	
$T_{wc(SDR12)}$	CLK cycle time for SDR12 Mode	39	–	ns	45	
$T_{ODLY(DDR50)}$	SD_CLK Transitioning Edge to SDIO_D	2	6	ns	41	
$T_{ODLY(SDR25)}$	SD_CLK Rising Edge to SDIO_D	2	12	ns	42	
$T_{ODLY(SDR12)}$	SD_CLK Falling Edge to SDIO_D	0	12	ns	45	
T_{SU_SOC} (DDR)	SoC setup time (data valid before clock launched)	3	–	ns	41 (For DDR50 Mode)	
T_{SU_SOC} (SDR)	SoC setup time (data valid before clock launched)	5	–	ns	40 (For SDR12/25 Mode)	
T_{HD_SOC} (DDR)	SoC hold time (data valid after clock launched)	2	–	ns	41 (For DDR50 Mode)	
T_{HD_SOC} (SDR)	SoC hold time (data valid after clock launched)	2	–	ns	40 (For SDR12/25 Mode)	
$T_{RISE\ CLK}$/ $T_{FALL\ CLK}$ (1.8V)	Clock Rise and Fall Time (1.8V operation)	1	4	ns		1, 2, 3, 4
$T_{RISE\ CLK}$/ $T_{FALL\ CLK}$ (3.3V)	Clock Rise and Fall Time (3.3V operation)	1	4	ns		1, 2, 3, 4

1. Based on trace length of 0.25”–4”, 2–5 pF Far End Load for Port 0 AND 2–10 pF Far End Load (for Port 1 and Board impedance of 25–75 Ω.
2. Minimum time deviates from SDIO Specification 2.0, minimum time is not defined in specification.
3. Measured from 0.58–1.27V.

4. Takes into consideration EMI filter of 10 pF - 40 Ω -10 pF.

Figure 38. SD Card Timing Diagram (DDR50)

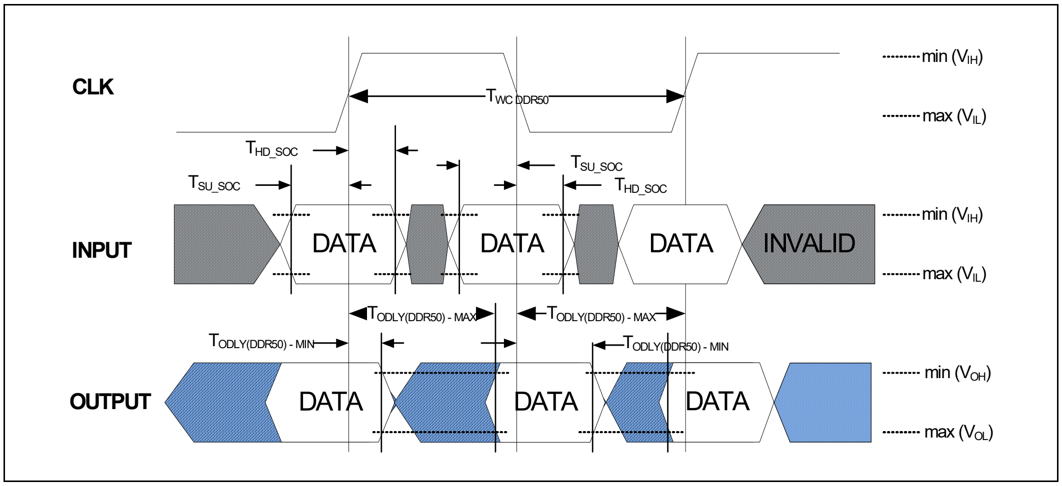


Figure 39. SD card Output Timing Diagram (SDR25)

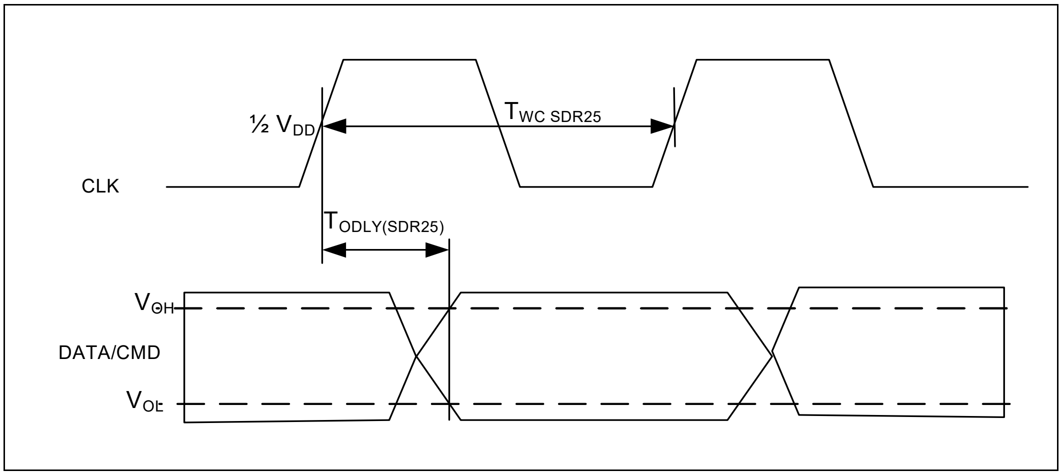
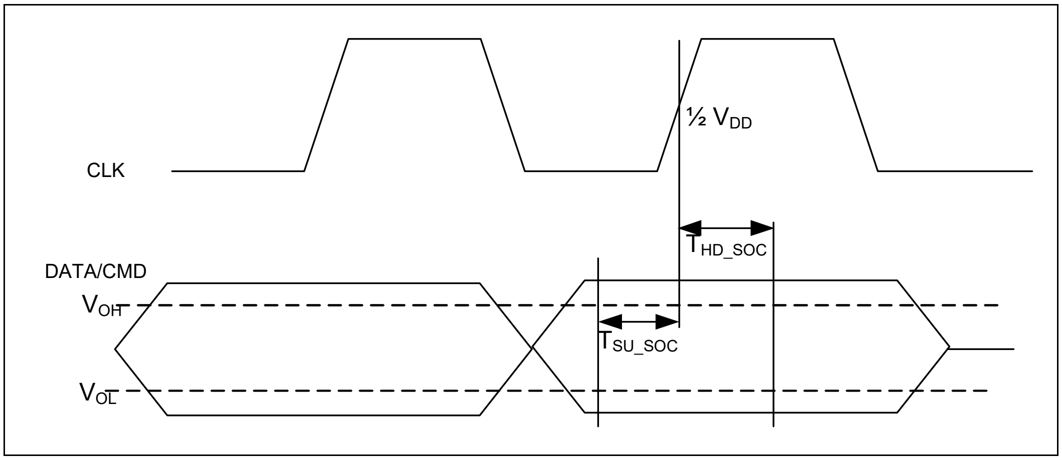


Figure 40. SD Card Input Timing Diagram (SDR12)



9.6.8.1 SD Card Default Speed Specification

Table 122. SD Card Default Speed AC Specification

Symbol	Parameter	Min.	Max.	Unit	Figure	Notes
f_{PP}	Clock Frequency Data transfer mode	0	25	MHz		
f_{OD}	Clock Frequency identification mode	0	400	kHz		1
t_{FL}	Clock low time	10	-	ns	Figure 54, 55	
t_{WH}	Clock High time	10	-	ns	Figure 54, 55	
t_{TLH}	Clock Rise time	-	10	ns	Figure 54, 55	
t_{THL}	Clock Fall time	-	10	ns	Figure 54, 55	
	Clock Overshoot	-	4.5	V		
	Clock undershoot	-1.5	-	V		
Outputs CMD,DAT (referenced to CLK)						
t_{ODLY}	Output Delay time during Data Transfer Mode	0	14	ns	Figure 55	
t_{ODLY}	Output Delay time during Identification Mode	0	50	ns	Figure 55	
Inputs CMD, DAT (referenced to CLK)						
t_{ISU}	Input Set-up time	5	-	ns	Figure 54	
t_{IH}	Input hold time	5	-	ns	Figure 54	

NOTES:
1. 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

Figure 41. SD Card Input Timing Diagram (Default)

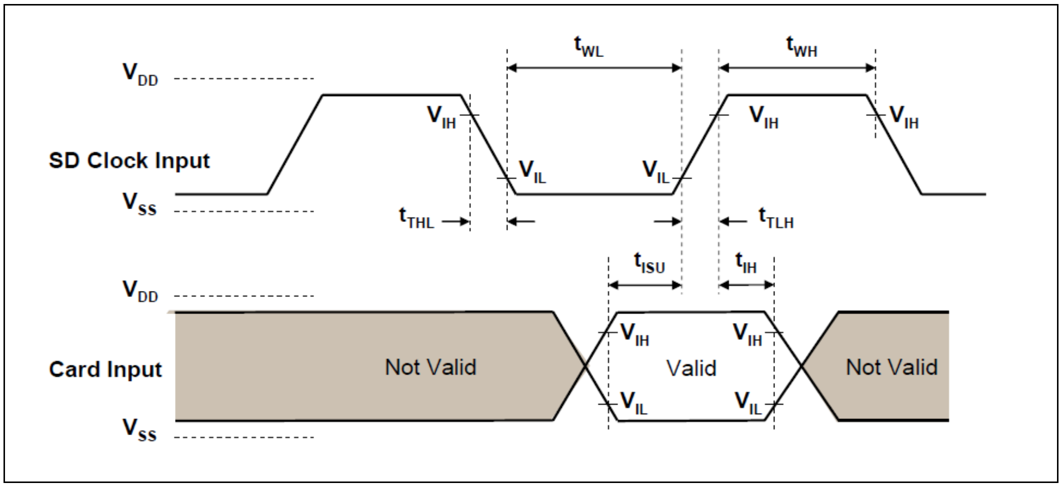
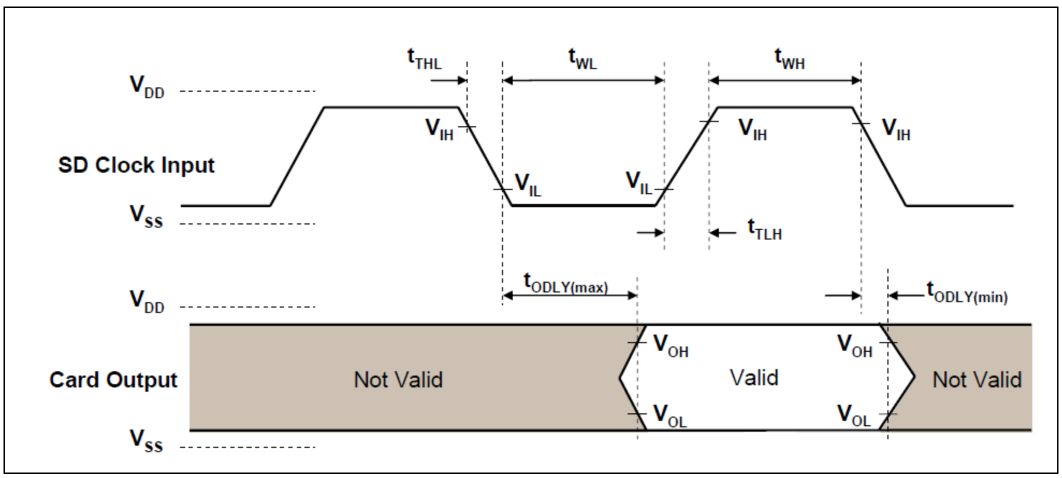


Figure 42. SD card Output Timing Diagram (Default)



9.6.8.2 SD Card High Speed Specification

Table 123. SD Card High Speed AC Specification (Sheet 1 of 2)

Symbol	Parameter	Min.	Max.	Unit	Figure	Notes
f_{PP}	Clock Frequency Data transfer mode	0	50	MHz		
t_{FL}	Clock low time	7	-	ns	Figure 56, 57	
t_{WH}	Clock High time	7	-	ns	Figure 56, 57	
t_{TLH}	Clock Rise time	-	3	ns	Figure 56, 57	
t_{THL}	Clock Fall time	-	3	ns	Figure 56, 57	
	Clock Overshoot	-	4.5	V		

Table 123. SD Card High Speed AC Specification (Sheet 2 of 2)

Symbol	Parameter	Min.	Max.	Unit	Figure	Notes
	Clock undershoot	-1.5	-	V		
Outputs CMD,DAT (referenced to CLK)						
t_{ODLY}	Output Delay time during Data Transfer Mode	-	14	ns	Figure 57	
t_{ODLY}	Output Delay time during Identification Mode	2.5	-	ns	Figure 57	
Inputs CMD, DAT (referenced to CLK)						
t_{ISU}	Input Set-up time	6	-	ns	Figure 56	
t_{IH}	Input hold time	2	-	ns	Figure 56	
C_L	Total Capacitance for each line	-	40	pF		

NOTES:
1. 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

Figure 43. SD Card Input Timing Diagram (High Speed)

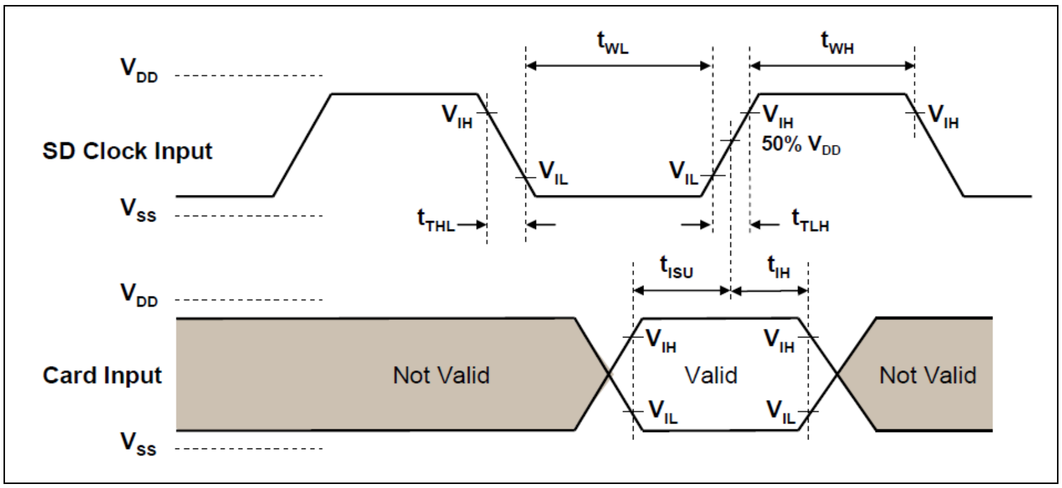
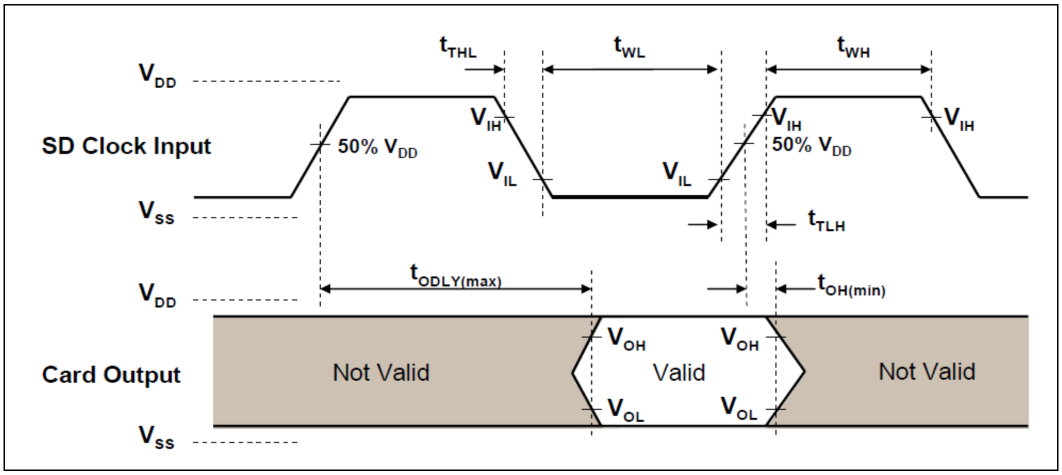


Figure 44. SD card Output Timing Diagram (High Speed)



9.6.9 SSC - SDIO AC specification

Table 124. SDIO AC Specification

Symbol	Parameter	Min.	Max.	Unit	Figure	Notes
$T_{wc(DDR50)}$	CLK cycle time for DDR50 Mode	19	–	ns	45	
$T_{wc(SDR25)}$	CLK cycle time for SDR25 Mode	19	–	ns	46	
$T_{wc(SDR12)}$	CLK cycle time for SDR12 Mode	39	–	ns	47	
$T_{ODLY(DDR50)}$	SD_CLK Transitioning Edge to SDIO_D	1.5	6	ns	45	
$T_{ODLY(SDR25)}$	SD_CLK Rising Edge to SDIO_D	3	11.9	ns	46	
$T_{ODLY(SDR12)}$	SD_CLK Falling Edge to SDIO_D	0	11.9	ns	47	
T_{SU_SOC} (DDR)	SoC setup time (data valid before clock launched)	1	–	ns	45 (For DDR50 Mode)	
T_{SU_SOC} (SDR)	SoC setup time (data valid before clock launched)	4	–	ns	48 (For SDR12/25 Mode)	
T_{HD_SOC} (DDR)	SoC hold time (data valid after clock launched)	2	–	ns	45 (For DDR50 Mode)	

Table 124. SDIO AC Specification

Symbol	Parameter	Min.	Max.	Unit	Figure	Notes
T_{HD_SOC} (SDR)	SoC hold time (data valid after clock launched)	2	–	ns	48 (For SDR12/25 Mode)	
$T_{RISE\ CLK}$/ $T_{FALL\ CLK}$ (1.8V)	Clock Rise and Fall Time (1.8V operation)	1	3	ns		1, 2, 3, 4
$T_{RISE\ CLK}$/ $T_{FALL\ CLK}$ (3.3V)	Clock Rise and Fall Time (3.3V operation)	1	3	ns		1, 2, 3, 4

NOTES:
1. Based on trace length of 0.25”–4”, 2–5 pF Far End Load for Port 0 AND 2–10 pF Far End Load (for Port 1 and Board impedance of 25–75 Ω.
2. Minimum time deviates from SDIO Specification 2.0, minimum time is not defined in specification.
3. Measured from 0.58–1.27V.
4. Takes into consideration EMI filter of 10 pF - 40 Ω -10 pF.

Figure 45. SDIO Timing Diagram (DDR50)

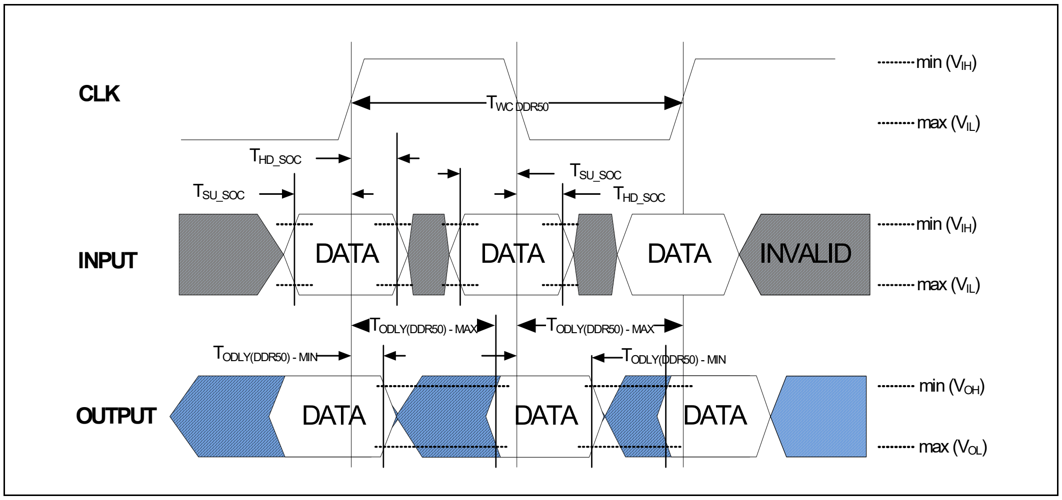


Figure 46. SDIO Output Timing Diagram (SDR25)

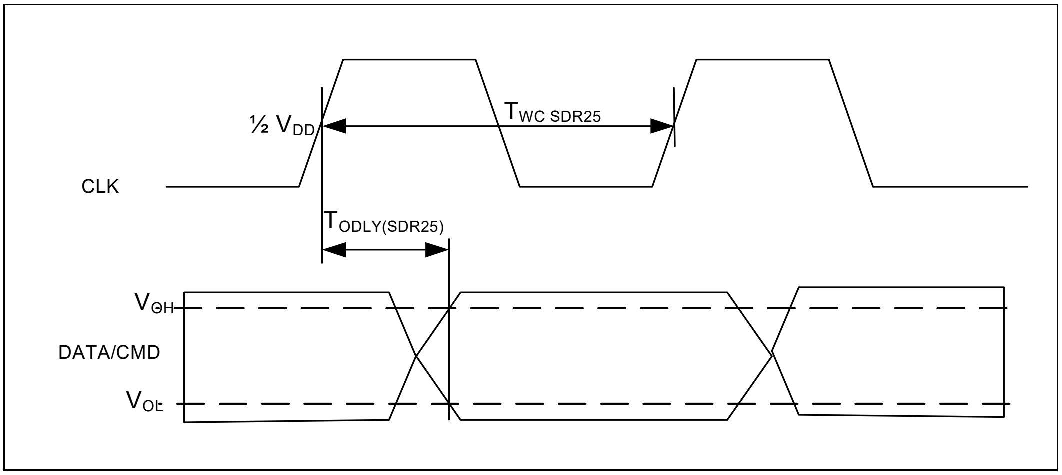


Figure 47. SDIO Output Timing Diagram (SDR12)

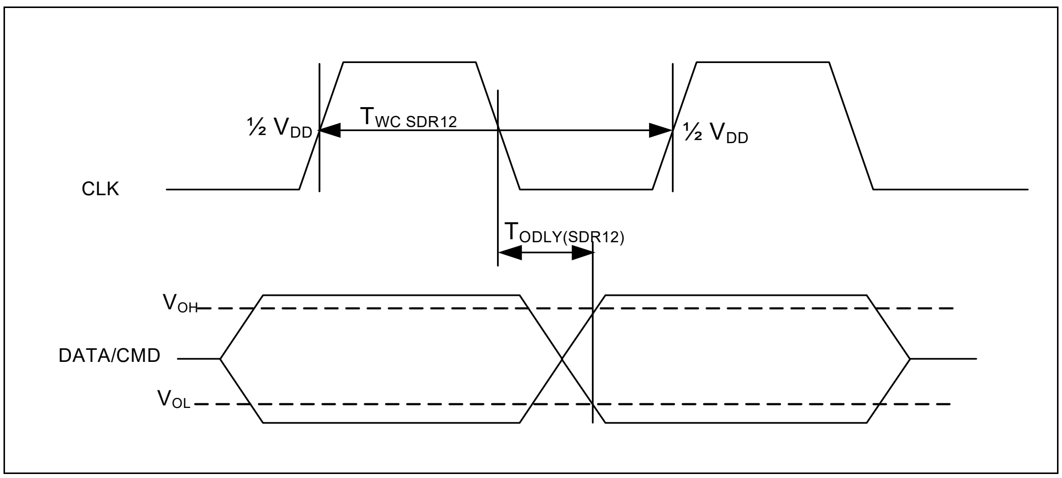
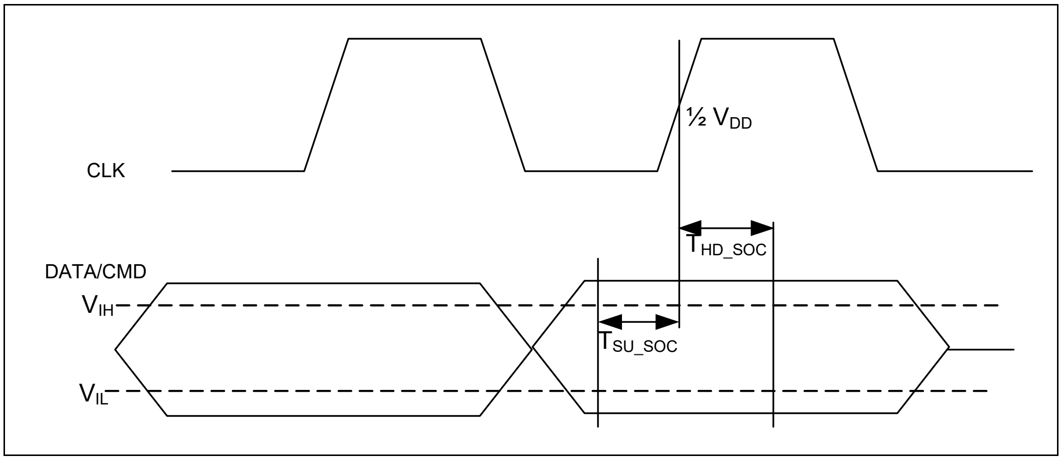


Figure 48. SDIO Input Timing Diagram (SDR12/25)



9.6.10 SCC - eMMC 4.5 AC Specification

9.6.10.1 HS/DDR Mode AC Characteristics

Table 125. eMMC 4.5 AC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min.	Max.	Units	Figures	Notes
F_{pp}	Clock Frequency Data transfer Mode		200	MHZ		
$T_{wc(HS/DDR)}$	CLK Cycle Time (High Speed Mode and DDR Modes)	20	–	ns	49	
T_{DC}	CLK Duty Cycle	40	55	%		
$T_{ODLY(HS)}$	EMMC_CLK Rising Edge to EMMC_D (High Speed Mode)	-	13.7	ns	49	
$T_{ODLY(DDR)}$	EMMC_CLK Rising Edge to EMMC_D (DDR Mode)	1.5	7	ns	50	
$T_{OH(HS)}$	Output hold time (HS mode)	2.5	–	ns		
$T_{SU(HS)}$	EMMC_D Input Setup Time to EMMC_CLK Rising Edge (data read - HS mode)	1.5	–	ns	50	
$T_{H(HS)}$	EMMC_D Input Hold Time to EMMC_CLK Rising Edge (data read - HS mode)	3	–	ns	51	
$T_{SU(DDR)}$	EMMC_D Input Setup Time to EMMC_CLK Rising Edge (data read - DDR Mode)	2.5	–	ns	50	
$T_{H(DDR)}$	EMMC_D Input Setup Time to EMMC_CLK Rising Edge (data read–DDR Mode)	2.5	–	ns	50	
$T_{RISE(HS)}$	Rise Time (Output - HS mode)	-	3	ns		1, 2, 3
$T_{FALL(HS)}$	Fall Time (Output -HS mode)	-	3	ns		1, 2, 3

Table 125. eMMC 4.5 AC Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min.	Max.	Units	Figures	Notes
$T_{RISE(DDR)}$	Rise Time (Output - DDR mode)	-	2	ns		1, 2, 3
$T_{FALL(DDR)}$	Fall Time (Output - DDR mode)	-	2	ns		1, 2, 3
T_{RSTW}	eMMC_RST# Pulse Width	1	–	µs		
T_{RSTCA}	eMMC_RST# to Command Time	200	–	µs		4
T_{RSTH}	eMMC_RST# High Period (interval time)	1	–	µs		

NOTES:
1. Based on trace length of 0.25 –2”, 2–12 pF Far End Load and Board impedance of 25–75 Ω.
2. Measured from 35–65%.
3. Minimum time deviates from e-MMC* Specification 4.41, minimum time is not defined in the specification.
4. Seventy-four (74) clock cycles are required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA.

Figure 49. eMMC* Output Timing Diagram (High Speed Mode)

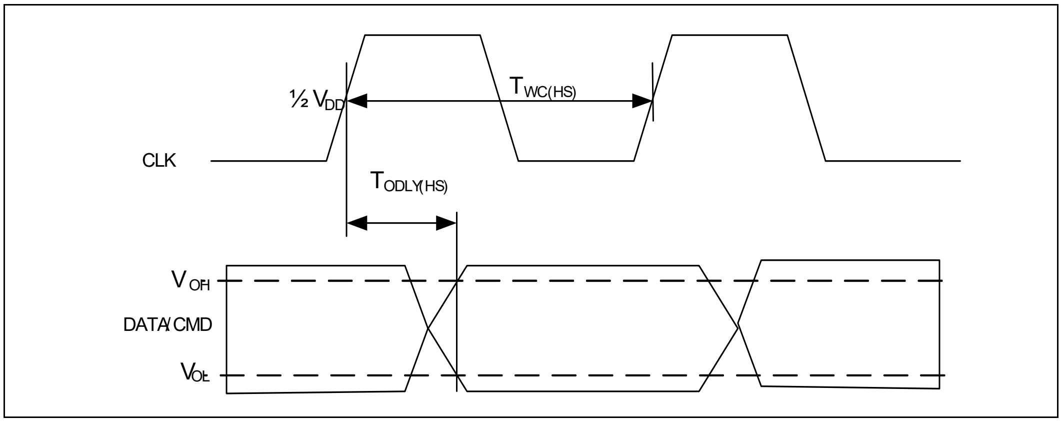


Figure 50. eMMC* DDR Timings

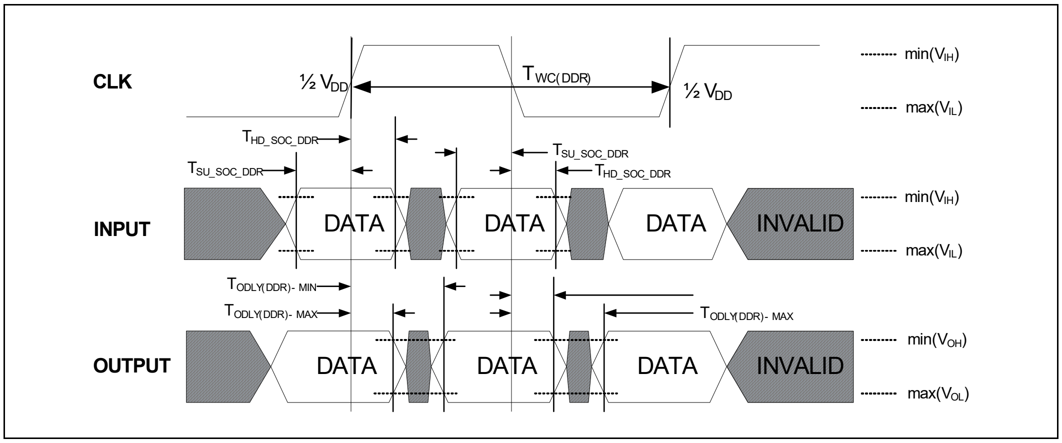
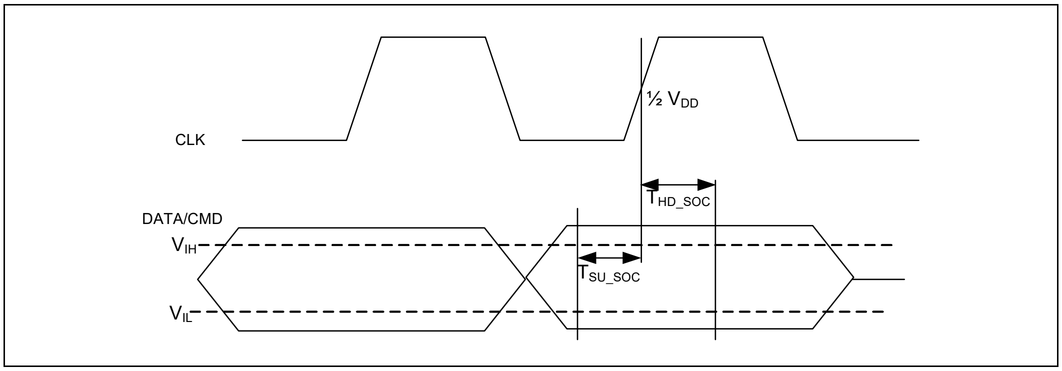


Figure 51. eMMC* Input Timing Diagram (High Speed Mode)



9.6.10.2 HS200 Mode AC Characteristics

Table 126. eMMC 4.5 AC Characteristics

Symbol	Parameter	Min.	Max.	Units	Figures	Notes
F_{pp}	Clock Frequency Data transfer Mode		200	MHZ		
T_{wc}	CLK Cycle Time	5	–	ns		
T_{DC}	CLK Duty Cycle	30	70	%		
T_{VW}	Output Valid Data Window	3.24	-	ns	70	
T_{ISU}	Input Setup Time	1.40	–	ns	70	
T_{IH}	Input Hold Time	0.8	–	ns	70	
T_{TLH}	Rise Time	-	1	ns	69	
T_{THL}	Fall Time	-	1	ns	69	

Figure 52. eMMC Clock Signal Timing Diagram (HS200 Mode)

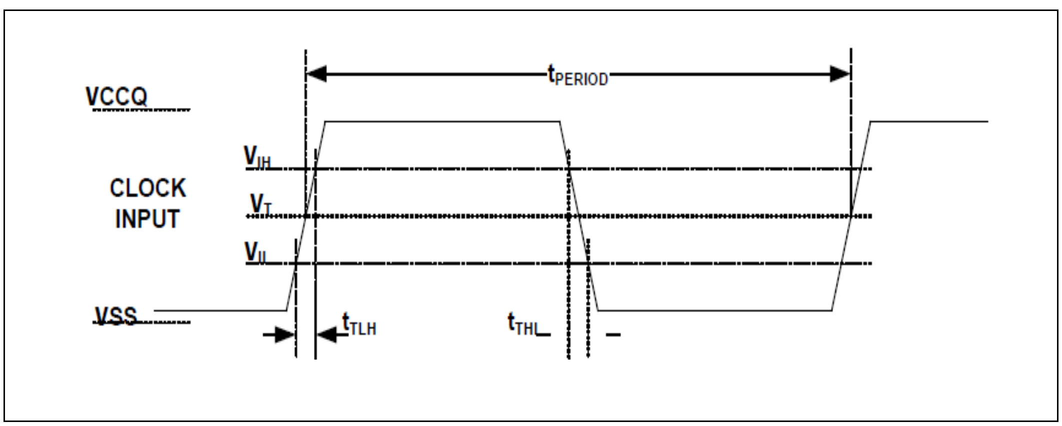
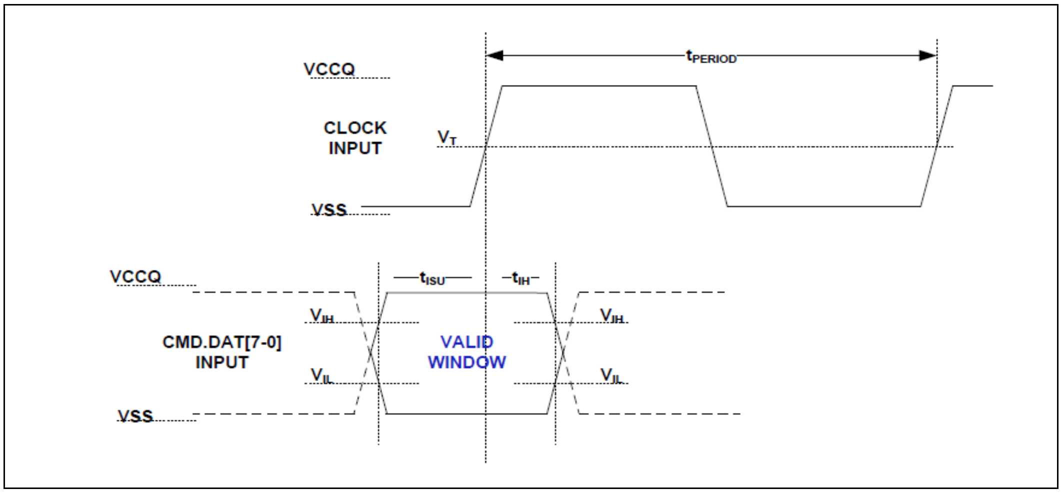


Figure 53. eMMC Input Timing Diagram (HS200 Mode)



9.6.11 SATA AC Specification

Table 127. SATA Specification and Interface Timings (Sheet 1 of 3)

Symbol	Parameter	Gen1		Gen2		Units	Notes
		Min	Max	Min	Max		
UI	Unit Interval	666.43	670.23	333.21	335.11	ps	
Receiver Parameter							
Z_{diffRX}	RX Pair Differential Impedance	85	115	85	115	Ω	
$V_{RX\text{-}DIFF\text{-}PP}$	VdiffRX, RX Differential Input Voltage	325	600	275	750	mvPP	
$T_{RX\text{-}RISE}$	RX Rise Time	100	273	67	136	ps	
$T_{RX\text{-}FALL}$	RX Fall Time	100	273	67	136	ps	
$T_{RX\text{-}SKEW}$	RX Differential Skew		100	50	100	ps	
$V_{RX\text{-}CM\text{-}AC}$	Vcm,acRX,RX AC Common Mode Voltage		100	100	150	mvPP	
$F_{RX\text{-}CM\text{-}AC}$	AC Common Mode Frequency	3	200	2	200	MHz	
$T_{J\text{-}Con\text{-}DD\text{-}5}$	TJ at Connector, Data-Data, 5		0.43			UI	
$D_{J\text{-}Con\text{-}DD\text{-}5}$	DJ at Connector, Data-Data, 5		0.35			UI	
$T_{J\text{-}Con\text{-}DD\text{-}250}$	TJ at Connector, Data-Data, 250		0.60			UI	
$D_{J\text{-}Con\text{-}DD\text{-}250}$	DJ at Connector, Data-Data, 250		0.42			UI	
$T_{TJ\text{-}Con\text{-}CD\text{-}10}$	TJ at Connector, Clk-Data, fBAUD/10				0.46	UI	

Table 127. SATA Specification and Interface Timings (Sheet 2 of 3)

Symbol	Parameter	Gen1		Gen2		Units	Notes
$T_{DJ-Con-CD-10}$	DJ at Connector, Clk-Data, fBAUD/10				0.35	UI	
$T_{TJ-Con-CD-500}$	TJ at Connector, Clk-Data, fBAUD/500				0.60	UI	
$T_{DJ-Con-CD-500}$	DJ at Connector, Clk-Data, fBAUD/500				0.42	UI	
$T_{jcon\ CD-1667}$	Tj at Connector Clk-Data, fbaud/1667		.65		.65	UI	
$D_{j\ con\ CD-1667}$	Dj at Connector Clk-Data, fbaud/1667		.35		.35	UI	
$RL_{DD11,RX}$	Min Differential Mode return loss (limits 150 - 300 MHz)			18		dB	
	Min Differential Mode return loss (limits 1.2 - 2.4 GHz)			8		dB	
	Min Differential Mode return loss (limits 2.4 - 3.0 GHz)			3		dB	
$RL_{CC11,RX}$	RX Common Mode Return Loss (limits 150 - 600 MHz)			5		dB	
	RX Common Mode Return Loss (limits 1.2 - 2.4 GHz)			2		dB	
	RX Common Mode Return Loss (limits 3.0 - 5.0 GHz)			1		dB	
V_{diffRX}	RX Differential Input Voltage	240	600	240	750	mV	
Transmitter Parameter							
Z_{diffTX}	TX Pair Differential Impedance	85	115	85	115	Ω	
$V_{TX-DIFF-PP}$	VdiffTX, TX Differential Input Voltage	400	600	400	700	mvPP	
$T_{TX-RISE}$	TX Rise Time	100	273	67	136	ps	1
$T_{TX-FALL}$	TX Fall Time	100	273	67	136	ps	1
$T_{TX-SKEW}$	TX Differential Skew	-	20	-	20	ps	
V_{CM-AC}	TX AC Common Mode				50	mv	
$T_{TJ-Con-DD-5}$	TJ at Connector, Data-Data, 5 UI		0.355			UI	
$T_{DJ-Con-DD-5}$	DJ at Connector, Data-Data, 5 UI		0.175			UI	
$T_{TJ-Con-DD-250}$	TJ at Connector, Data-Data, 250 UI		0.470			UI	
$D_{J-Con-DD-250}$	DJ at Connector, Data-Data, 250		0.220			UI	
$T_{TJ-Con-CD-10}$	TJ at Connector, Clk-Data, fBAUD/10				0.30	UI	
$T_{DJ-Con-CD-10}$	DJ at Connector, Clk-Data, fBAUD/10				0.17	UI	

Table 127. SATA Specification and Interface Timings (Sheet 3 of 3)

Symbol	Parameter	Gen1		Gen2		Units	Notes
$T_{TJ\text{-}Con\text{-}CD\text{-}500}$	TJ at Connector, Clk-Data, fBAUD/ 500				0.37	UI	
$T_{DJ\text{-}Con\text{-}CD\text{-}500}$	DJ at Connector, Clk-Data, fBAUD/ 500				0.19	UI	
$T_{jcon\ CD\text{-}1667}$	Tj at Connector Clk-Data, fbaud/ 1667		.65		.65	UI	
$D_{j\ con\ CD\text{-}1667}$	Dj at Connector Clk-Data, fbaud/ 1667		.35		.35	UI	
$RL_{DD11,TX}$	Min Differential Mode return loss (limits 150 - 300 MHz)			14		dB	
	Min Differential Mode return loss (limits 1.2 - 2.4 GHz)			6		dB	
	Min Differential Mode return loss (limits 2.4 - 3.0 GHz)			3		dB	
$RL_{CC11,TX}$	RX Common Mode Return Loss (limits 150 - 600 MHz)			5 - 8		dB	
	RX Common Mode Return Loss (limits 1.2 - 2.4 GHz)			2		dB	
	RX Common Mode Return Loss (limits 3.0 - 5.0 GHz)			1		dB	
$V_{RX\text{-}DIFF\text{-}PP}$	VdiffRX, RX Differential Input Voltage	325	600	275	750	mvPP	
$T_{RX\text{-}RISE}$	RX Rise Time	100	273	67	136	ps	
$T_{RX\text{-}FALL}$	RX Fall Time	100	273	67	136	ps	
$T_{RX\text{-}SKEW}$	RX Differential Skew		100	50	100	ps	
$V_{RX\text{-}CM\text{-}AC}$	Vcm,acRX,RX AC Common Mode Voltage		100	100	150	mvPP	

NOTES:
1. 20% - 80%
2. All parameters measured at Rload = 100Ω ±10% load.
3. For a detailed description of the symbols, see the *IEEE1596.3-1996* Standard.

9.6.12 USB 2.0 Host AC Specification

Table 128. USB 2.0 AC specification (HIGH SPEED)

Symbol	Parameter	Min	Max	Units	Notes	Fig
DRIVER CHARCTERTICS:						
THSR	Rise Time (10% - 90%)	100		ps		
THSF	Fall Time (10% - 90%)	100		ps		
ZHSDRV	Driver Output Resistance (which also serves as high- speed termination)	40.5	49.5			

Table 128. USB 2.0 AC specification (HIGH SPEED)

Symbol	Parameter	Min	Max	Units	Notes	Fig
CLOCK TIMINGS:						
THSDRAT	High-speed Data Rate	479.760	480.240	Mb/s		
THSFRAM	Microframe Interval	124.9375	125.0625	us		

Table 129. USB 2.0 AC specification (FULL SPEED)

Symbol	Parameter	Min	Max	Units	Notes	Fig
DRIVER CHARCTERTICS:						
TFR	Rise Time	4	20	ns		44,45
TFF	Fall Time	4	20	ns		44,45
TFRFM	Differential Rise and Fall Time Matching	90	111.11	%	10	
ZDRV	Driver Output Resistance for driver which is not high-speed capable	28	44			
CLOCK TIMINGS:						
TFDRATHS	Full-speed Data Rate for hubs and devices which are high-speed capable	11.99	12.0060	Mb/s		
TFDRATE	Full-speed Data Rate for hubs and devices which are not high-speed capable	11.97	12.0300	MB/s		
TFRAME	Frame Interval	0.9995	1.0005	ms		
FULL-SPEED DATA TIMINGS						
TDJ1 TDJ2	Source Jitter Total (including frequency tolerance): To Next Transition For Paired Transitions	-3.5 -4	3.5 4	ns ns	7,8,12,10	46
TFDEOP	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns	8,11	47
TFEOPT	Source SE0 interval of EOP	160	175	ns		47

Table 130. USB 2.0 AC specification (LOW SPEED)

Symbol	Parameter	Min	Max	Units	Notes	Fig
DRIVER CHARCTERTICS:						
TLR	Rise Time	75	300	ns		44
TFF	Fall Time	75	300	ns		44
TLRFM	Differential Rise and Fall Time Matching	80	125	%	10	

Table 130. USB 2.0 AC specification (LOW SPEED)

Symbol	Parameter	Min	Max	Units	Notes	Fig
CLOCK TIMINGS:						
TLDRATHS	Low-speed Data Rate for hubs and devices which are high-speed capable	1.49925	1.50075	Mb/s		
TLDRATE	Low-speed Data Rate for hubs and devices which are not high-speed capable	1.4775	1.5225	MB/s		
FULL-SPEED DATA TIMINGS						
TUDJ1 TUDJ2	Upstream facing port source Jitter Total (including frequency tolerance): To Next Transition For Paired Transitions	-95 -150	95 150	ns ns	7,8	46
TDDJ1 TDDJ2	Downstream facing port source Jitter Total (including frequency tolerance): To Next Transition For Paired Transitions	-25 -14	25 14	ns ns	7,8	46
TLDEOP	Source Jitter for Differential Transition to SE0 Transition	-40	100	ns	8,11	47
TLEOPT	Source SE0 interval of EOP	1.25	1.50	us		47

NOTES:
1. Measured at A plug.
2. Measured at A receptacle.
3. Measured at B receptacle.
4. Measured at A or B connector.
5. Measured with RL of 1.425 kΩ to 3.6 V.
6. Measured with RL of 14.25 kΩ to GND.
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target VBUS drop of 330 mV.
10. Excluding the first transition from the Idle state.
11. The two transitions should be a (nominal) bit time apart.
12. For both transitions of differential signaling.
13. Must accept as valid EOP.
14. Single-ended capacitance of D+ or D- is the capacitance of D+/D- to all other conductors and, if present, shield in the cable. That is, to measure the single-ended capacitance of D+, short D-, VBUS, GND, and the shield line together and measure the capacitance of D+ to the other conductors.
15. For high power devices (non-hubs) when enabled for remote wakeup.

Figure 54. USB Rise and Fall Times

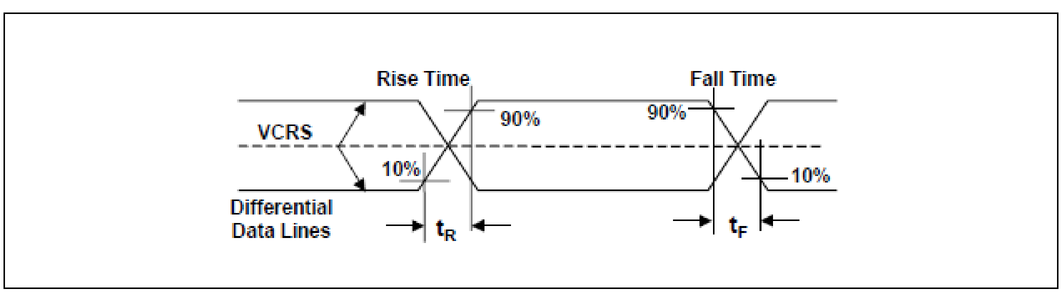


Figure 55. USB Full Speed Load

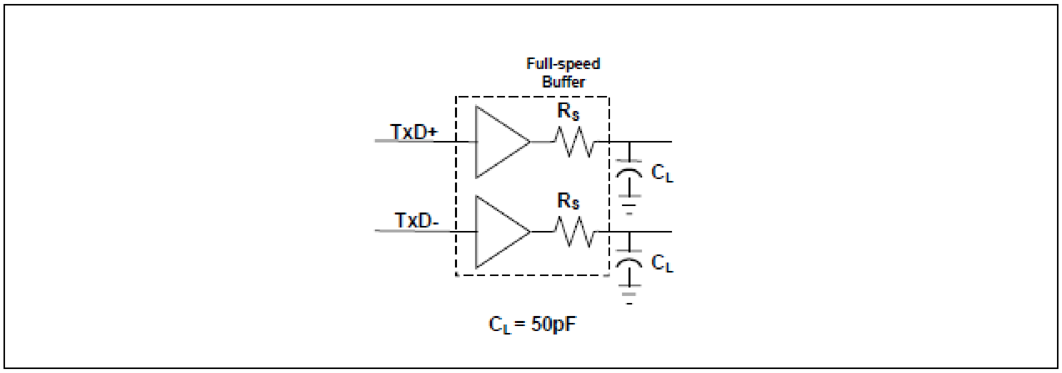


Figure 56. USB Differential Data Jitter for Low/Full- Speed

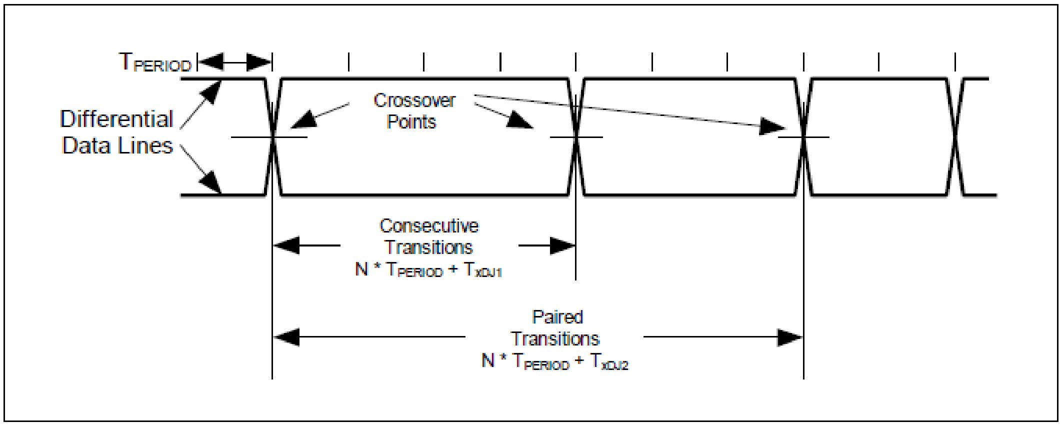
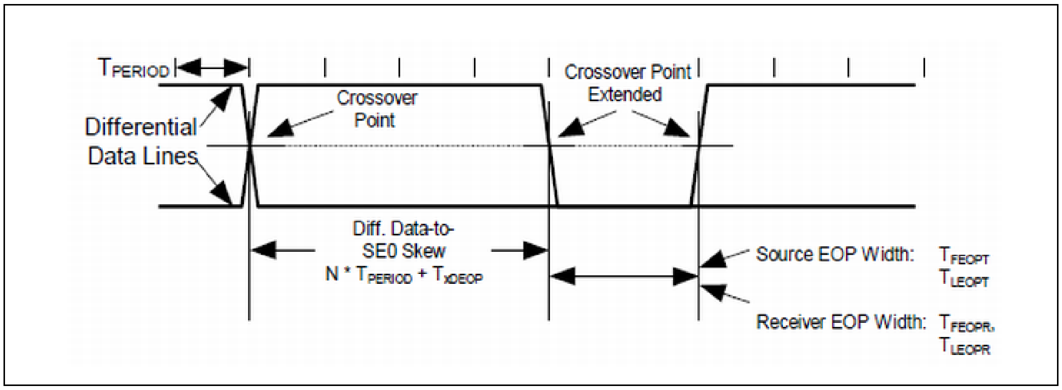


Figure 57. USB Differential-to-EOP Transition Skew and EOP Width for Low/Full-Speed



9.6.13 USB 3.0 AC Specification

Figure 58. USB 3.0 Signals AC Specification

Symbol	Parameter	Min	Max	Units	Notes
TMIN-PULSE-DJ	Deterministic min Pulse	-	0.96	UI	1
TMIN-PULSE-TJ	Tx min Pulse	-	0.90	UI	2
TTX-EYE	Transmitter Eye	0.625	-	UI	3
TTx-DJ-DD	Tx deterministic jitter	-	.205	UI	4

NOTES:
1. Tx pulse width variation that is deterministic.
2. Min Tx Pulse at 10^{-12} including Dj and Rj.
3. Includes all jitter sources.
4. Deterministic jitter only assuming the Dual Dirac distribution

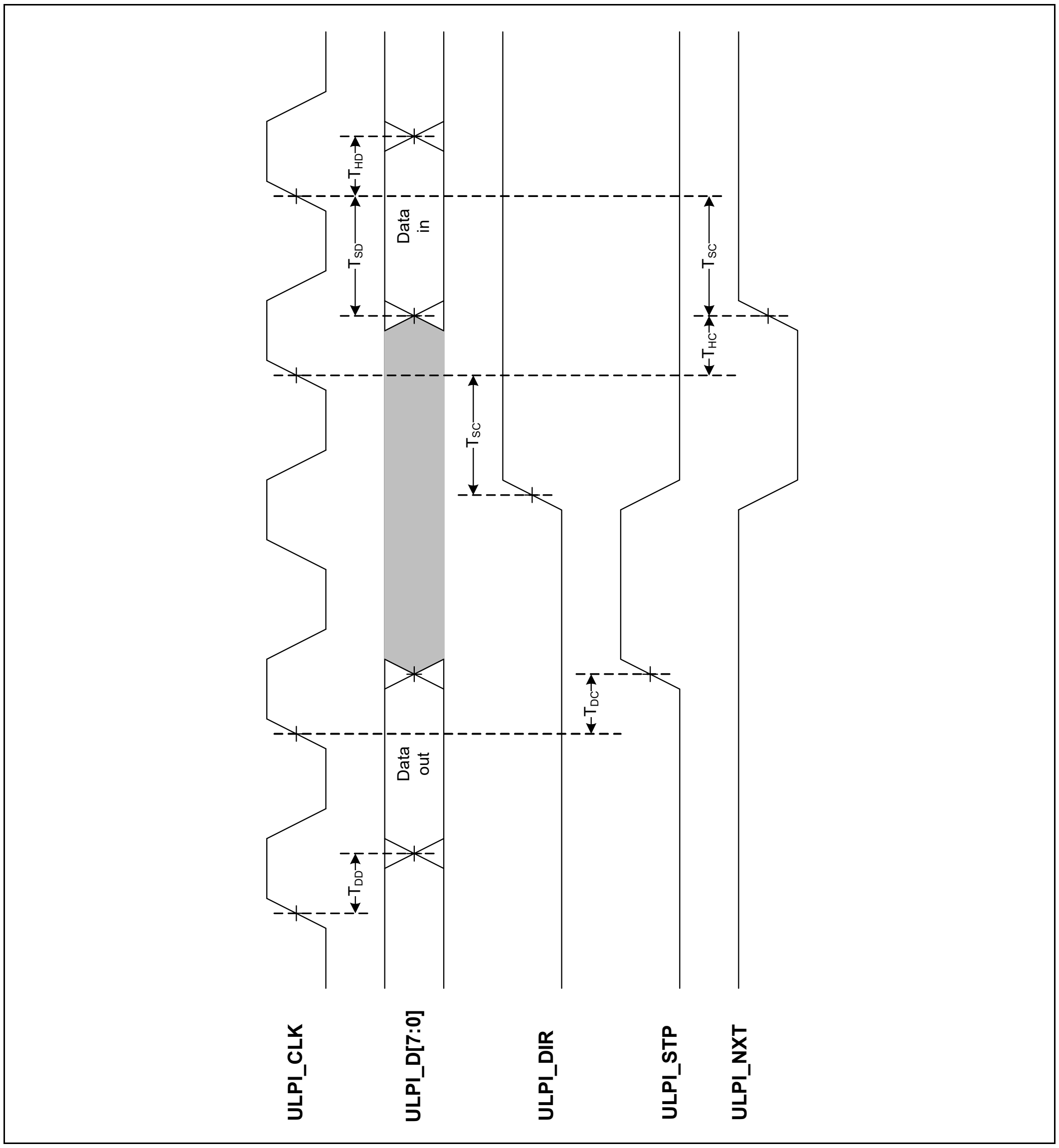
9.6.14 ULPI USB 2.0 Device AC Specification

Table 131. ULPI Signals AC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{STEADY}	Clock frequency steady state	59.97	60	60.03	MHz	
TRISE/ FALL	Input clock rise/fall time	2		7	ns	1,2
TSC,TSD	Setup time (control in, 8-bit data in) relative to rising clock edge at host	6		-	ns	
THC,THD	Hold time (control in, 8-bit data in) relative to rising clock edge at host	0			ns	
TDC,TDD	Output delay (control in, 8-bit data in) relative to rising clock edge at host	0		-	ns	3
TRISE/ FALL	Rise/Fall time (control out, 8-bit data out)	2		7	ns	1,2,4

NOTES:
1. Based on trace length of 1–4”, Far End Load of 1–5 pF and board impedance of 30–75 ohms.
2. Measured from 10–90%.
3. Minimum time deviates from ULPI Specification, minimum time is not defined in ULPI Specification.
4. Minimum time and Maximum time not mentioned in the ULPI Specification.

Figure 59. ULPI Timing Diagram



9.6.15 Intel® HD Audio AC Specification

9.6.15.1 1.5-V AC specification

The output driver on the Intel HD Audio electrical link must be able to deliver an initial voltage of at least V_{IL_HDA} or V_{IH_HDA} respectively at the receiver through the bus with known characteristic impedance and at the same time meeting signal quality requirements.

The minimum and maximum drive characteristics of Intel HD Audio output buffers are defined by the V/I curves. Table 132 and Figure 60 describe the SDO buffer AC drive specification where as the Table 133 and Figure 61 describe the AC drive specification of the HDA_SDI[x] buffers. The AC drive specification for HDA_SYNC, HDA_RST# and HDA_CLK buffers is same as that of HDA_SDO.

These curves should be interpreted as traditional 'DC' transistor curves with the following exceptions: 'DC drive point' is the only position on the curves at which steady state operation is intended, while the higher currents are only reached momentarily during bus switching transients. The 'AC drive point' (real definition of buffer strength) defines the minimum instantaneous current required to switch the bus.

Adherence to these curves should be evaluated at worst case conditions. Minimum pull up curve is evaluated at minimum VCC_{HDA} and high temperature. Minimum pull down curve is evaluated at minimum VCC_{HDA} and high temperature. The maximum curve test points are evaluated at maximum VCC_{HDA} and low temperature.

Inputs must be clamped to both ground and power rails. The clamp diode characteristics are also listed here for reference.

Figure 60. V/I Curves for HDA_SDO buffers

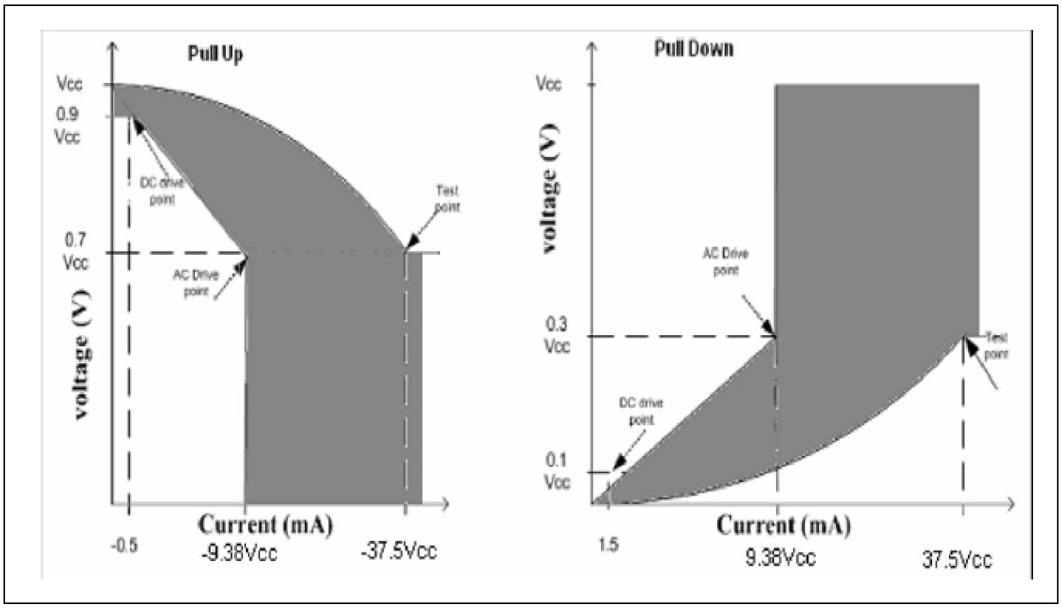


Table 132. HDA_SDO 1.5V Buffer AC Specification (Sheet 1 of 2)

Symbol	Parameter	Condition	Min	Max	Unit
I_{OH}	switching Current High	$0 < V_{O\_HDA} < 0.7VCC_{HDA}$	$-16.67VCC_{HDA}$		mA
		$0.7VCC_{HDA} < V_{O\_HDA} < 0.9VCC_{HDA}$	$-55.57(VCC_{HDA}\text{-Vout})$		mA

Table 132. HDA_SDO 1.5V Buffer AC Specification (Sheet 2 of 2)

Symbol	Parameter	Condition	Min	Max	Unit
		$0.7VCC_{HDA} < V_{O\_HDA} < VCC_{HDA}$		$(151.52/VCC_{HDA}) * (V_{O\_HDA} - VCC_{HDA}) * (V_{O\_HDA} + 0.4VCC_{HDA})$	mA
	(Test Point)	$V_{O\_HDA} = 0.7VCC_{HDA}$		$-50VCC_{HDA}$	mA
I_{OL}	Low Period of SCL Clock	$VCC_{HDA} > V_{O\_HDA} > 0.3VCC_{HDA}$	$16.67VCC_{HDA}$		mA
		$0.3VCC_{HDA} > V_{O\_HDA} > 0.1VCC_{HDA}$	57.57Vout		mA
		$0.3VCC_{HDA} > V_{O\_HDA} > 0$		$(238.1/VCC_{HDA}) * V_{O\_HDA} * (VCC_{HDA} - V_{O\_HDA})$	mA
	(Test Point)	$V_{O\_HDA} = 0.3VCC_{HDA}$		$50VCC_{HDA}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{I\_HDA} < -1$	$-25 + (V_{I\_HDA}+1)/0.015$		
I_{CH}	High Clamp Current	$VCC_{HDA}+4 > Vin > VCC_{HDA}+1$	$25+(V_{I\_HDA} - VCC_{HDA}-1)/0.015$		
Slew_r	Output rise Slew rate	$0.25VCC_{HDA}$ to $0.75VCC_{HDA}$	0.5	1.5	V/ns Slew rate (note1)
Slew_f	Output rise Slew rate	$0.75VCC_{HDA}$ to $0.25VCC_{HDA}$	0.5	1.5	V/ns Slew rate (note1)

NOTE:

1. Slew rate is to be interpreted as the cumulative edge rate across the specified range, ($0.25VCC_{HDA}$ to $0.75VCC_{HDA}$ load for rise and $0.75VCC_{HDA}$ to $0.25VCC_{HDA}$ load for fall), rather than instantaneous rate at any point within the transition range.

Table 133. HDA_SDI[x] 1.5V Buffer AC Specification (Sheet 1 of 2)

Symbol	Parameter	Condition	Min	Max	Unit
I_{OH}	switching Current High	$0 < V_{O\_HDA} < 0.7VCC_{HDA}$	$-9.38VCC_{HDA}$		mA
		$0.7VCC_{HDA} < V_{O\_HDA} < 0.9VCC_{HDA}$	$-31.27(VCC_{HDA} - V_{O\_HDA})$		mA

Table 133. HDA_SDI[x] 1.5V Buffer AC Specification (Sheet 2 of 2)

Symbol	Parameter	Condition	Min	Max	Unit
		$0.7VCC_{HDA} < V_{O\_HDA} < VCC_{HDA}$		$(113.64/VCC_{HDA}) * (V_{O\_HDA} - VCC_{HDA}) * (V_{O\_HDA} + 0.4VCC_{HDA})$	mA
	(Test Point)	$V_{O\_HDA} = 0.7VCC_{HDA}$		$-37.5VCC_{HDA}$	mA
I_{OL}	Low Period of SCL Clock	$VCC_{HDA} > V_{O\_HDA} > 0.3VCC_{HDA}$	$9.38VCC_{HDA}$		mA
		$0.3VCC_{HDA} > V_{O\_HDA} > 0.1VCC_{HDA}$	$31.27V_{O\_HDA}$		mA
		$0.3VCC_{HDA} > V_{O\_HDA} > 0$		$(178.57/VCC_{HDA}) * V_{O\_HDA} * (VCC_{HDA} - V_{O\_HDA})$	mA
	(Test Point)	$V_{O\_HDA} = 0.3VCC_{HDA}$		$37.55VCC_{HDA}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{I\_HDA} < -1$	$-25 + (V_{I\_HDA} + 1)/0.015$		
I_{CH}	High Clamp Current	$VCC_{HDA} + 4 > V_{I\_HDA} > VCC_{HDA} + 1$	$25 + (V_{I\_HDA} - VCC_{HDA} - 1)/0.015$		
Slew_r	Output rise Slew rate	$0.25VCC_{HDA}$ to $0.75VCC_{HDA}$	0.5	1.5	V/ns Slew rate (note1)
Slew_f	Output rise Slew rate	$0.75VCC_{HDA}$ to $0.25VCC_{HDA}$	0.5	1.5	V/ns Slew rate (note1)

NOTE:

1. Slew rate is to be interpreted as the cumulative edge rate across the specified range, ($0.25VCC_{HDA}$ to $0.75VCC_{HDA}$ load for rise and $0.75VCC_{HDA}$ to $0.25VCC_{HDA}$ load for fall), rather than instantaneous rate at any point within the transition range.

9.6.15.2 Maximum AC Ratings and Device Protection

All Intel HD Audio buffers should be capable of withstanding continuous exposure to the waveform shown in Figure 61. It is recommended that these waveforms be used as qualification criteria against which the long term reliability of each device is evaluated. Table 134 and Table 135 list the parameters of the waveform. This level of robustness should be guaranteed by design; it is not intended that this waveform should be used as a production test.

These waveforms are applied with the equivalent of a zero impedance voltage source, driving through a series resistor directly into each input or tri-stated output pin. The open-circuit voltage of the voltage source is shown in Figure 61, which is based on the worst case overshoot and undershoot expected in actual Intel HD Audio buses. The resistor values are calculated to produce the worst case current into an effective internal clamp diode.

Figure 61. Maximum AC Waveforms for 1.5 V Signaling

NOTE:
1. The voltage waveform is supplied at the resistor shown in the evaluation setup, not the package pin.
2. Any internal clamping in the device being tested will greatly reduce the voltage levels seen at the package pin.

Table 134. 1.5V Parameters for Maximum AC Signalling Waveforms

Symbol	Parameter	Min	Max	Unit
V_1	Overshoot Voltage		3.25	V
V_2	Undershoot Initial Voltage		1.65	V
V_3	Undershoot Voltage	-1.6		V
V_{pu}	Waveform peak-to-peak		3.25	V
V_{po}	Waveform peak-to-peak		3.25	V
t_{rf}	Rise/fall time	0.5	1.5	V/ns
f_{SDI}	Frequency of AC rating waveform as applied to SDI input buffers		24	MHz
f_{SDO}	Frequency of AC rating waveform as applied to SDO input buffers		24	MHz

Table 135. Resistance value for the AC rating Waveform

Condition	Value
Overshoot waveform at the codec	65 Ohms
Undershoot waveform ar the codec	101 Ohms
Overshoot waveform at the controller	108 Ohms

Table 135. Resistance value for the AC rating Waveform

Condition	Value
Undershoot waveform ar the controller	133 Ohms

NOTE:
1. The voltage waveform is supplied at the resistor shown in the evaluation setup, not the package pin.
2. Any internal clamping in the device being tested will greatly reduce the voltage levels seen at the package pin.

9.6.16 I²S (Audio) AC Specification

9.6.16.1 I²S Slave Mode AC Specification

Table 136. I²S AC Timings

Symbol	Parameter	Min.	Max.	Units	Figure	Notes
T_{DC}	Clock Duty Cycle	45	55	%	62, 63, 64	
T_{I2S}	Clock Frequency		12.25	MHz	62, 63, 64	
$T_{S\text{-}RXD}$	Setup for DATAIN with respect to the CLK active edge.	6	–	ns	62, 63, 64	1, 2, 3
T_{H_RXD}	Hold for DATAIN with respect to the CLK active edge.	6	–	ns	62, 63, 64	1, 2, 3
$T_{S\text{-}FS}$	Setup for FRM with respect to the CLK active edge.	6	–	ns	62, 63, 64	1, 2, 3
T_{H_FS}	Hold for FRM with respect to CLK active edge.	20	–	ns	62, 63, 64	1, 2, 3
T_{CO_TXD}	Tco of DATAOUT with respect to CLK active edge at the host	–	18	ns	62, 63, 64	1, 2,3

NOTE:
1. Active edge refers to the mode selected.
2. For I²S mode, data launches at falling edge and is being captured at rising edge.
3. For PCM mode data launches at rising edge and is being captured at falling edge. PCM Mode has two different modes, Short Frame Mode and Long Frame Mode.
   a. Short Frame Mode—FS is asserted one clock cycle earlier than data is launched by the Master.
   b. Long Frame Mode—FS and Data are launched on the same clock edge by the Master.

Figure 62. I^{2}S Slave Port Timings in I^{2}S Mode

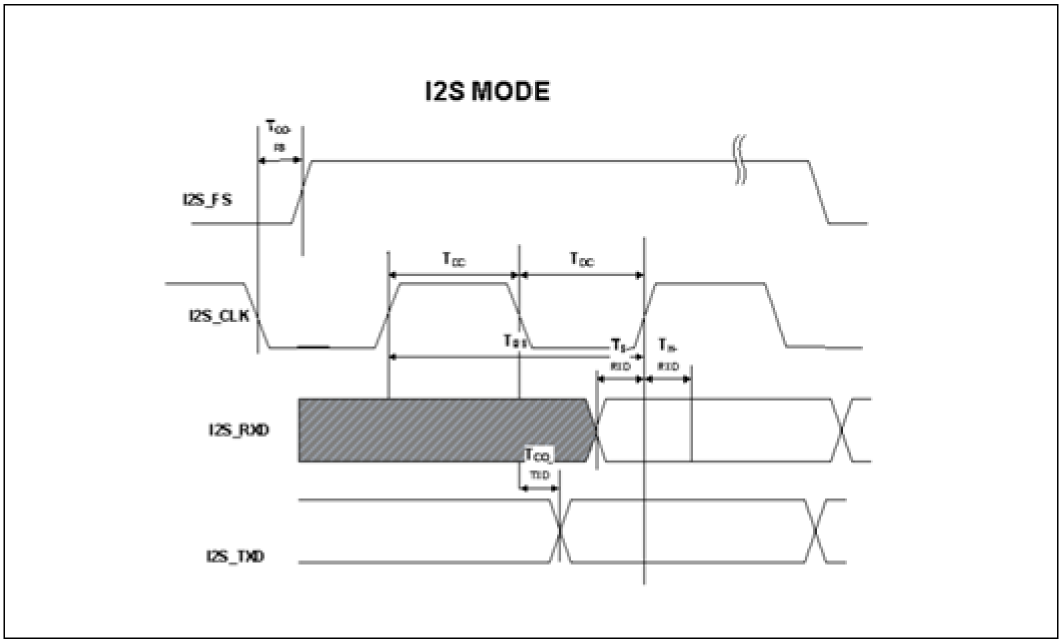


Figure 63. I^{2}S Slave Port Timings in PCM Short Frame Mode

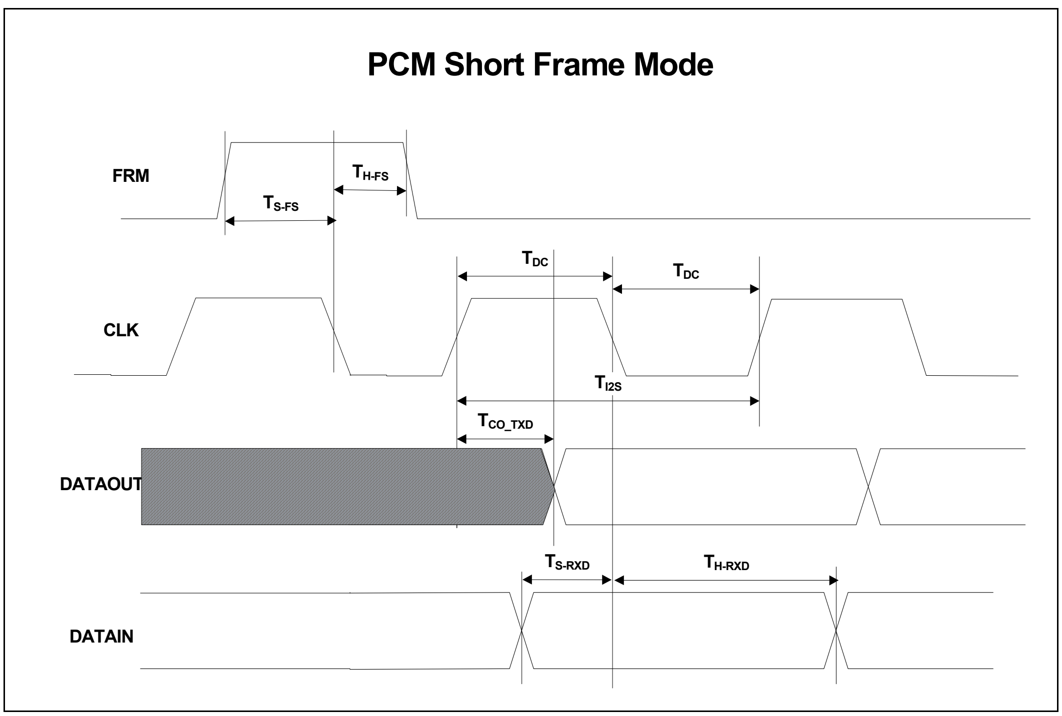
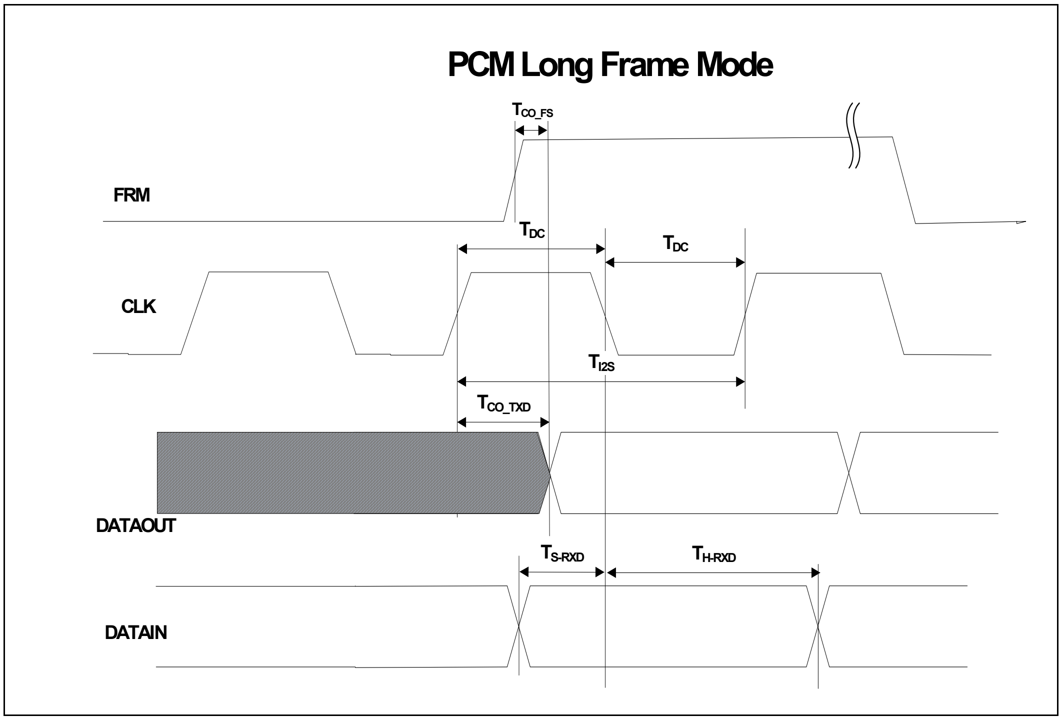


Figure 64. I^2S Slave Port Timings in PCM Long Frame Mode



9.6.16.2 I^2S Master Mode AC Specification

Table 137. I^2S Master Mode AC Timing

Symbol	Parameter	Min.	Max.	Units	Figure
T_{DC}	Clock Duty Cycle	45	55	%	
T_{I2S}	Clock Frequency		12.5	MHz	
$T_{S\text{-}RXD}$	Setup for DATAIN with respect to the CLK active edge	10	–	ns	
$T_{H\text{-}RXD}$	Hold for DATAIN with respect to the CLK active edge	10	–	ns	
T_{CO_TXD}	T_{CO} of DATAOUT with respect to CLK active edge at the SoC	–	10	ns	
$T_{CO\text{-}FS}$	T_{CO} of FRM with respect to CLK at the SoC		10	ns	

9.6.17 PCI Express* AC Specification

Table 138. PCI Express* Interface Timings

Symbol	Parameter	Min	Typ	Max	Unit	Figures	Notes
Transmitter and Receiver Timings							
UI	Unit Interval – PCI Express* Gen 1 (2.5 GT/s)	399.88		400.12	ps		5
UI	Unit Interval – PCI Express* Gen 2 (5.0 GT/s)	199.9		200.1	ps		5
$T_{TX\text{-}EYE}$	Minimum Transmission Eye Width	0.7		—	UI	65	1,2
$T_{TX\text{-}RISE/Fall}$ (Gen1)	TXP/TXN Rise/Fall time	0.125			UI		1,2
$T_{TX\text{-}RISE/Fall}$ (Gen2)	TXP/TXN Rise/Fall time	0.15			UI		1,2
$T_{RX\text{-}EYE}$	Minimum Receiver Eye Width	0.40		—	UI	66	3,4

NOTES:

1. Specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter compliance eye diagram)
2. A $T_{TX\text{-}EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TXJITTER\text{-}MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TXEYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load documented in the PCI Express* specification 2.0 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
4. A $T_{RX\text{-}EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.6 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
5. Nominal Unit Interval is 400 ps for 2.5 GT/s and 200 ps for 5 GT/s.
6. PCIe Reference clocks follow PCI Express* specification with the exception of edge rate: Max = 8.0 V/ns instead of 4.0 V/ns. There should be no DC termination of the clocks.

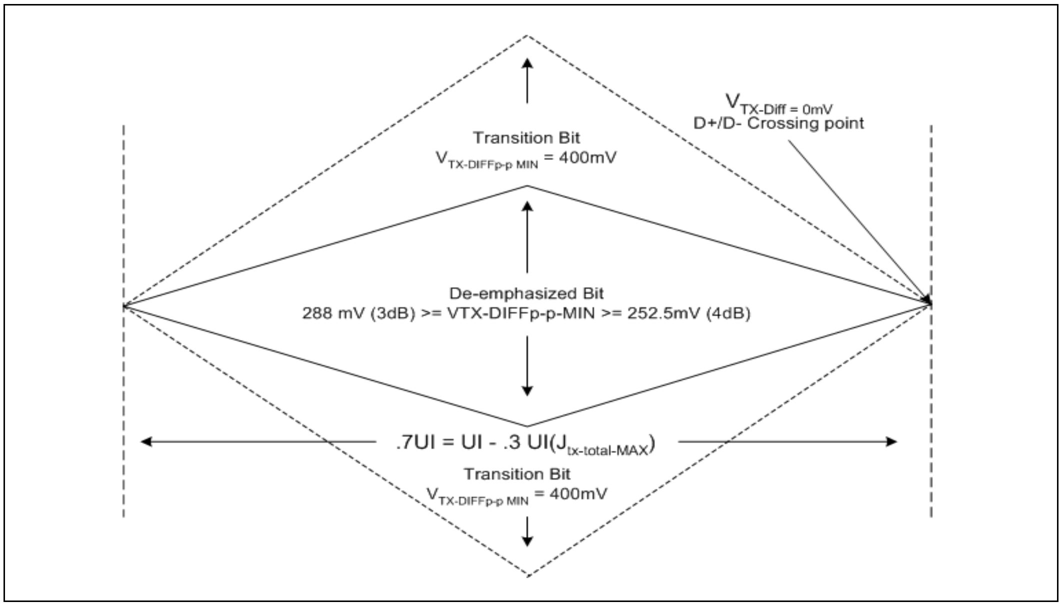


Figure 65. PCI Express* Transmitter Eye

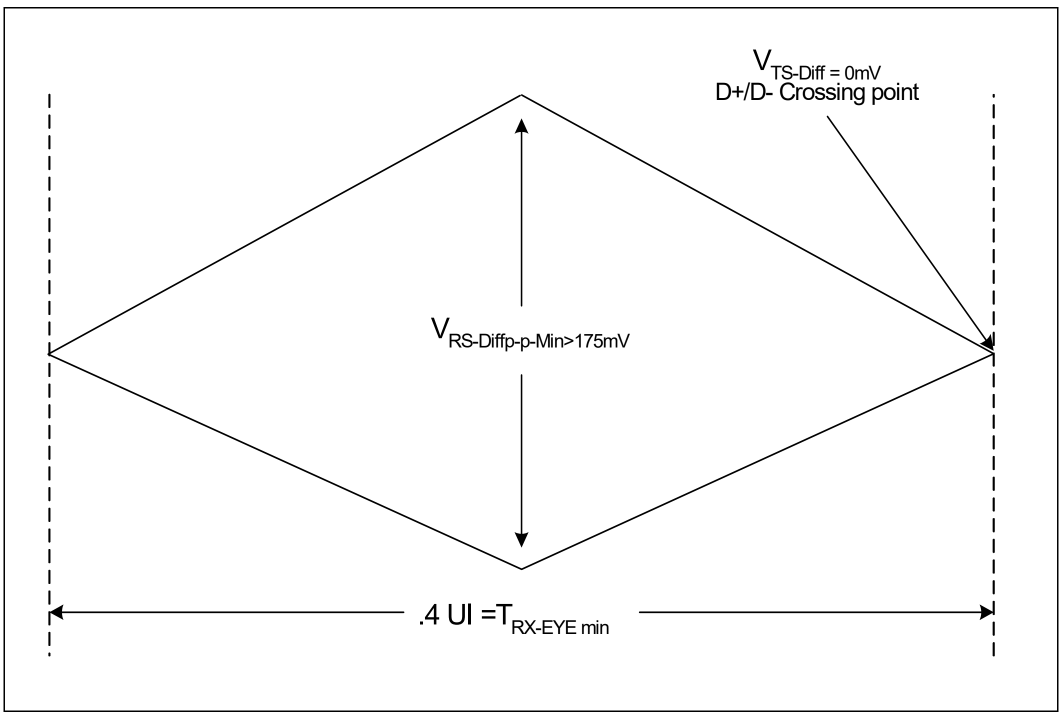


Figure 66. PCI Express* Receiver Eye

9.6.18 PCU - PMC - Suspended Clock AC Specification

Table 139. SUS Clock Timings

Symbol	Parameter	Min	Max	Units	Notes	Figure
f_{susclk}	Operating Frequency	32		kHz	1	
t39	High time	9.5	-	µs	1	
t39a	Low Time	9.5	-	µs	1	

Note: 1. SUSCLK duty cycle can range from 30% minimum to 70% maximum.

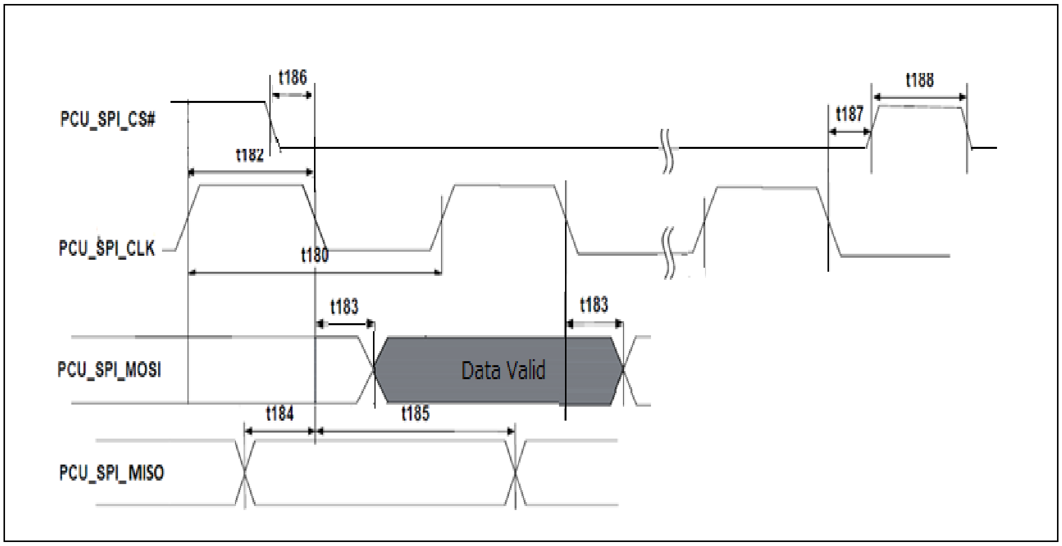
9.6.19 PCU - SPI NOR AC Specification

Table 140. PCU - SPI NOR AC Specification

Sym	Parameter	Min	Max	Units	Notes
t180	Serial Clock Frequency	20, 33, 50		MHz	
t182	SPI Clock duty cycle at Host	45	55	%	
t183	Tco of PCU_SPI_MOSI with respect to serial clock falling edge at the host	0	5	ns	
t184	Setup of PCU_SPI_MISO with respect to serial clock falling edge at the host	11	-	ns	
t185	Hold of PCU_SPI_MISO with respect to serial clock falling edge at the host	0	-	ns	1, 2, 3
t186	Setup of PCU_SPI_CS[1:0]# with respect to serial clock falling edge at the host	12	-	ns	
t187	Hold of PCU_SPI_CS[1:0]# with respect to serial clock falling edge at the host	5	-	ns	
t188/t189	Min Idle (de-assertion) time for PCU_SPI_CLK signals	32	-	ns	
Trise/Tfall	Rise / Fall time	-	2	ns	1,2

NOTES:
1. Based on trace length of up to 4” and board impedance of 30–75 Ω Measured from 30–70%.
2. Total maximum, capacitance of 25 pF

Figure 67. SPI NOR Timing



9.6.20 PCU - SMBUS AC Specification

Table 141. SMBUS Clock Signal Timings

Symbol	Parameter	Min	Max	Unit	Notes	Figure
f_{smb}	Operating Frequency	10	100	kHz		
t_{HIGH}	High time	4.0	50	us	1	68
t_{Low}	Low time	4.7		us		68
t_{RISE}	Rise time		1000	ns		68
t_{FALL}	Fall time		300	ns		68

1. The maximum high time (t_{HIGH} Max) provides a simple method for devices to detect bus idle conditions.

Table 142. SMBus Timing

Sym	Parameter	Min	Max	Units	Notes	Figure
t_{STOP_START}	Bus Tree Time Between Stop and Start Condition	4.7	—	μs		69
t_{START_HOLD}	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	4.0	—	μs		69
t_{START_SET}	Repeated Start Condition Setup Time	4.7	—	μs		69
t_{STOP_SET}	Stop Condition Setup Time	4.0	—	μs		69
t_{DATA_HOLD}	Data Hold Time	0	—	ns	1	69
t_{DATA_SET}	Data Setup Time	250	—	ns		69

Table 142. SMBus Timing

Sym	Parameter	Min	Max	Units	Notes	Figure
t_{DEV_TO}	Device Time Out	25	35	ms	2	
t_{SLVCLK_LOWEXT}	Cumulative Clock Low Extend Time (slave device)	—	25	ms	3	69
t_{MSTCLK_LOWEXT}	Cumulative Clock Low Extend Time (master device)	—	10	ms	4	69

1. tDATA_HOLD has a minimum timing for I2C of 0 ns, while the minimum timing for SMBus is 300 ns.
2. A device will timeout when any clock low exceeds this value.
3. tSLVCLK_LOWEXT is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
4. tMSTCLK_LOWEXT is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack or ack-to-stop.

Figure 68. SMBus Transaction

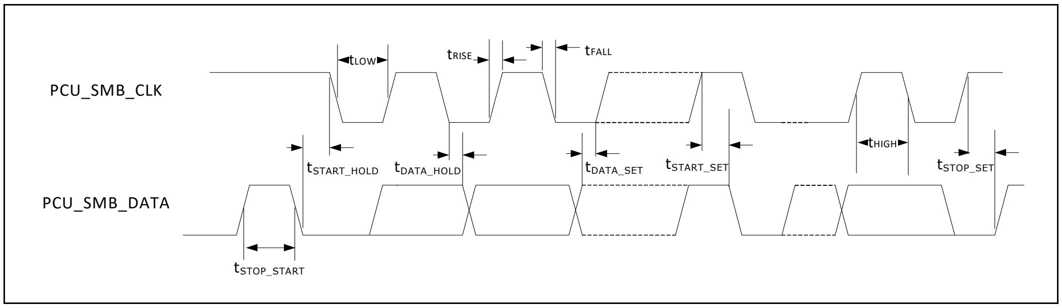
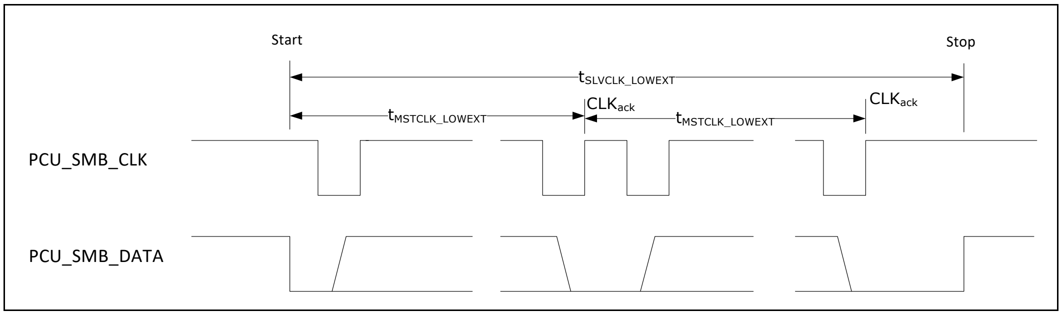


Figure 69. SMBus Timeout



9.6.21 PCU - iLB - LPC AC Specification

Table 143. LPC AC Specifications (with loop back from ILB_LPC_CLK[0] to ILB_LPC_CLK[1])

Sym	Parameter	Min	Max	Units	Notes	Fig
T_{CO}	ILB_LPC_AD[3:0], ILB_LPC_FRAME#, ILB_LPC_SERIRQ Valid Delay from ILB_LPC_CLK[1] Rising	2	14	ns		73
T_{EN_AD}	ILB_LPC_AD[3:0], ILB_LPC_FRAME#, ILB_LPC_SERIRQ Output Enable Delay from ILB_LPC_CLK[1] Rising	2		ns		74
T_{FD_AD}	ILB_LPC_AD[3:0] Float Delay from ILB_LPC_CLK[1] Rising		28	ns		75
T_{SU_AD}	ILB_LPC_AD[3:0] Setup Time to ILB_LPC_CLK[1] Rising	7		ns		76
T_{HD_AD}	ILB_LPC_AD[3:0] Hold Time from ILB_LPC_CLK[1] Rising	0		ns		76
T_{lpc}	ILB_LPC_CLK[1:0] Duty Cycle	35	65	%	1	

NOTE:
1. High time is measured from 0.75 x PCU_1P8_G3. Low time is measured from 0.35 x PCU_1P8_G3
2. The load capacitance used for the LPC timing parameters is 30 pF
3. VT is 1/2 of LPC IO voltage

Figure 70. Valid Delay from Rising Clock Edge

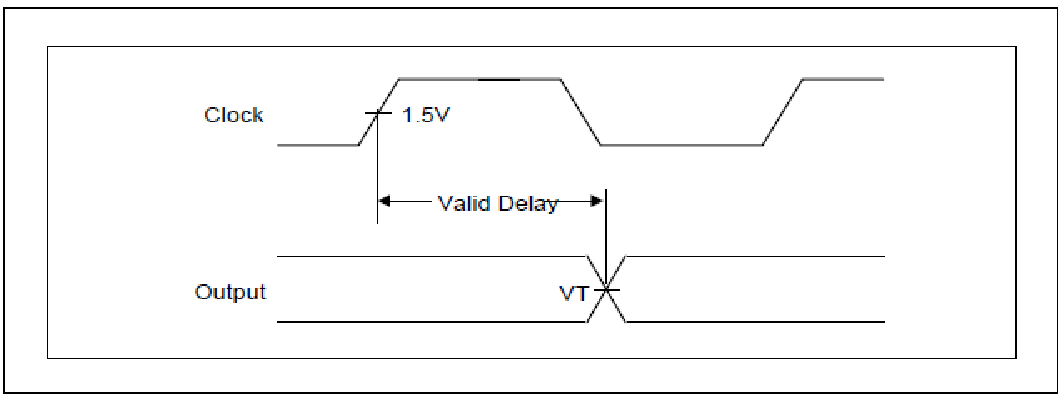


Figure 71. Output Enable Delay

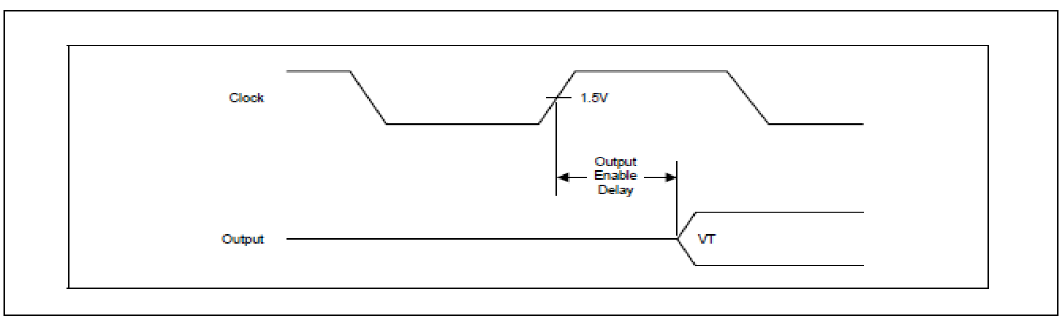


Figure 72. Float Delay

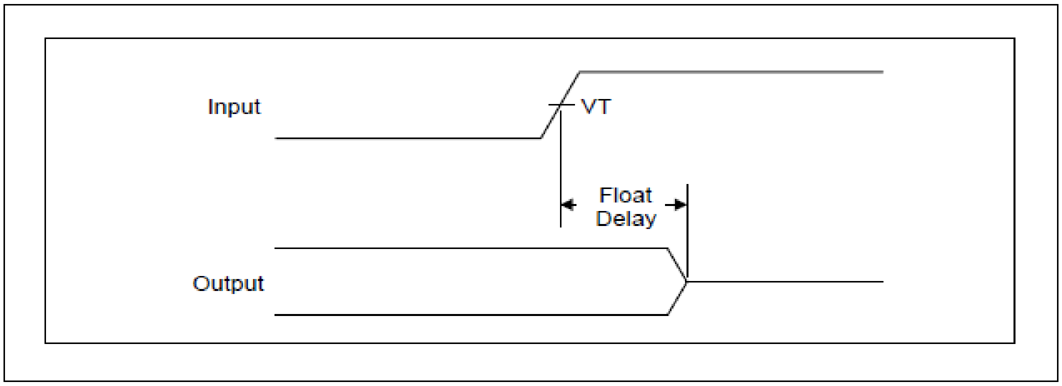
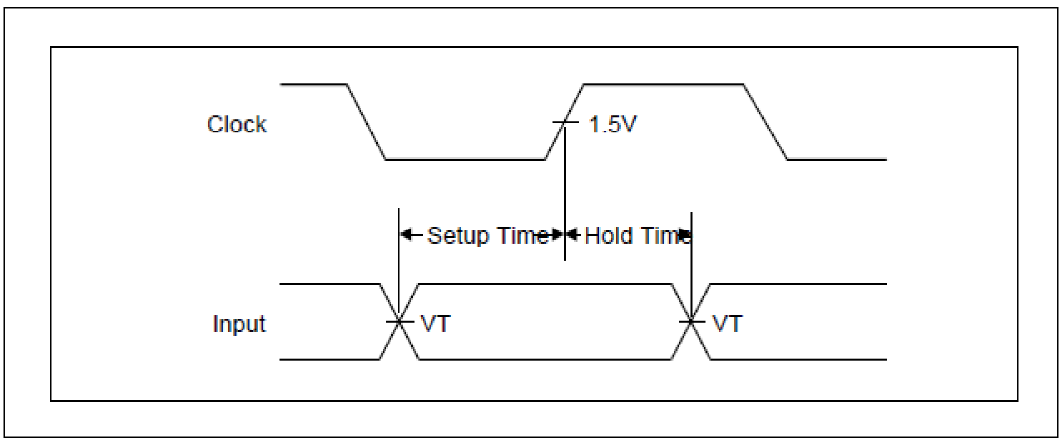


Figure 73. Setup and Hold Times



9.6.22 SIO - I²C AC Specifications

9.6.22.1 I²C Fast/Standard Mode Electrical Specification

Table 144. I²C Fast/Standard Mode AC Specifications (Sheet 1 of 2)

Symbol	Parameter	Standard-Mode		Fast-Mode		Fast-Mode Plus		Units	Notes	Figure
		Min.	Max.	Min.	Max.	Min.	Max.			
f_{SCL}	I^2C_CLK clock frequency	0	100	0	400	0	1000	kHz		
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	0.26	–	µs		74
t_{LOW}	LOW period of the I^2C_CLK clock	4.7	–	1.3	–	0.5	–	µs		74
t_{HIGH}	HIGH period of the I^2C_CLK clock	4.0	–	0.6	–	0.26	–	µs		74

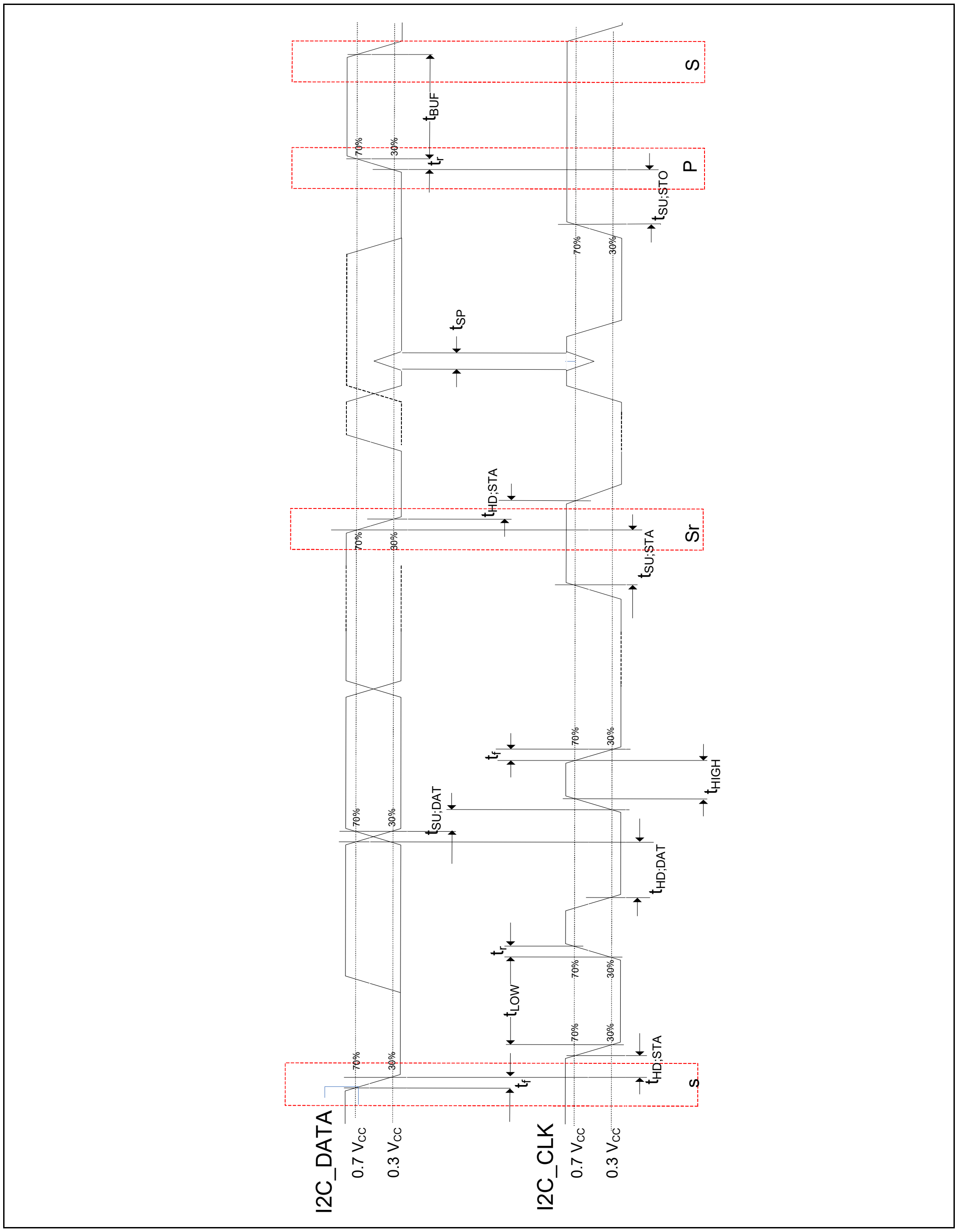
Table 144. I^2C Fast/Standard Mode AC Specifications (Sheet 2 of 2)

Symbol	Parameter	Standard-Mode		Fast-Mode		Fast-Mode Plus		Units	Notes	Figure
		Min.	Max.	Min.	Max.	Min.	Max.			
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	–	0.6	–	0.26	–	µs		74
$t_{HD:DAT}$	Data hold time: I^2C-bus devices	0	–	0	–	0	–	ns		74
$t_{SU:DAT}$	Data set-up time	250	–	100	–	50	–	ns	1	74
t_r	Rise time of both I^2C_DATA and I^2C_CLK signals	–	1000	20 + $0.1C_b$(5)	300	–	120	ns	2, 3	74
t_f	Fall time of both I^2C_DATA and I^2C_CLK signals	1	300	1	300	1	120	ns	5	74
$t_{SU:STO}$	Set-up time for STOP condition	4.0	–	0.6	–	0.26	-	µs		74
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	0.5	–	µs		
C_b	Capacitive load for each bus line	–	130	–	130	-	-	pF		
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	0.1 V_{DD}	–	0.1 V_{DD}	–	0.1 V_{DD}	–	V		
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2 V_{DD}	–	0.2 V_{DD}	–	0.2 V_{DD}	–	V		

NOTES:

1. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU; DAT ³ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2C_CLK signal. If such a device does stretch the LOW period of the I2C_CLK signal, it must output the next data bit to the I2C_DATA line tr max + tSU; DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2C_CLK line is released
2. Cb = total capacitance of one bus line in pF.
3. No Active current source PU on I2C_CLK signals. Rise time is based upon the Pull-up resistor mentioned in the Platform Design Guide.
4. The maximum tHD;DAT could be 3.45 ms and 0.9 ms for Standard-mode and Fast-mode, but must be less than the maximum of tVD;DAT or tVD;ACK by a transition time. This maximum must only be met if the device does not stretch the LOW period (tLOW) of the I2C_CLK signal. If the clock stretches the I2C_CLK, the data must be valid by the set-up time before it releases the clock.
5. Specification deviates from the minimum time compared to Industrial specification.

Figure 74. Definition of Timing for F/S-Mode Devices on I^2C Bus

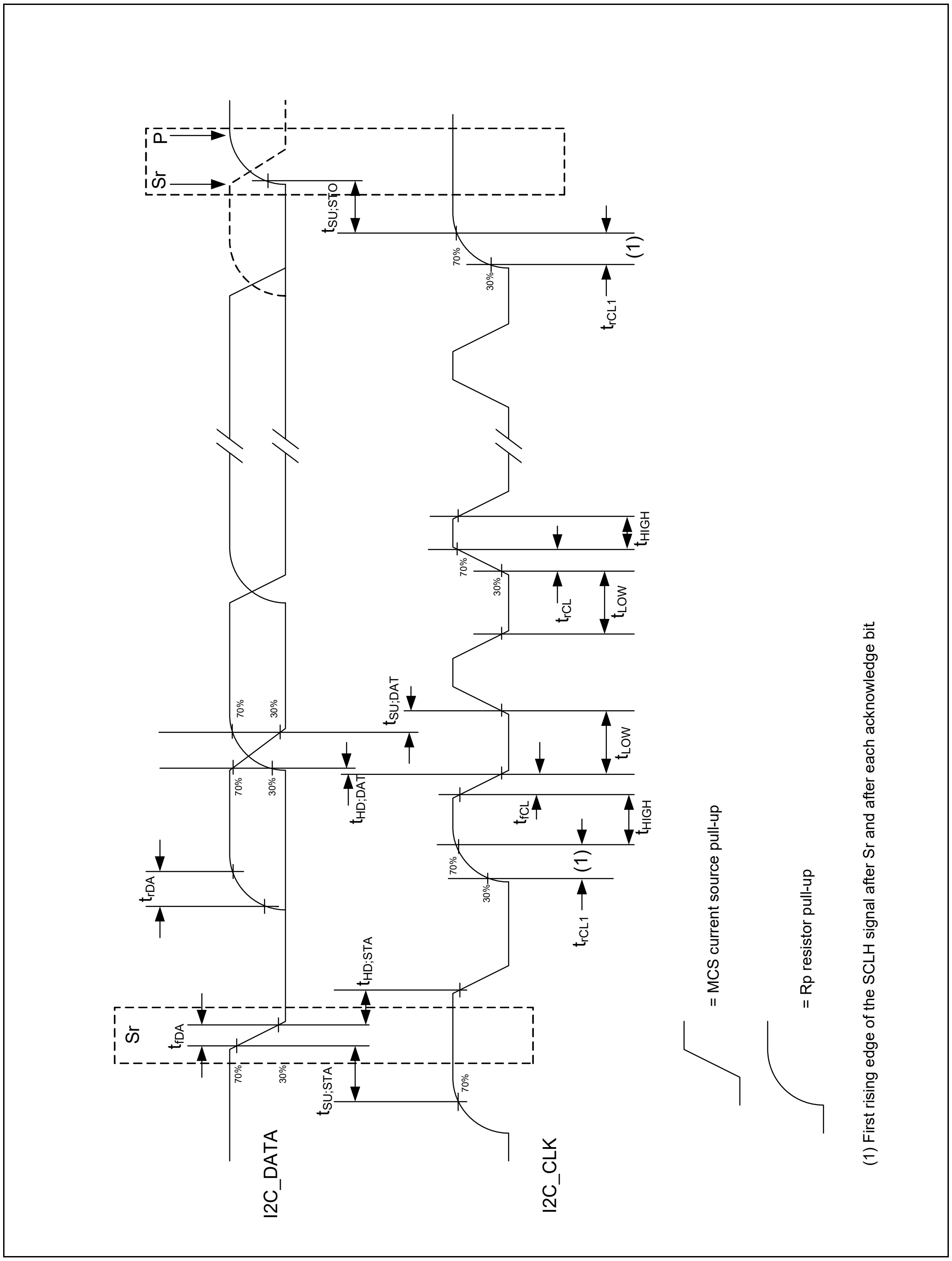


9.6.22.2 I^2C High Speed Mode Electrical Specification

Table 145. AC Specification for High Speed Mode I^2C—Bus Devices

Symbol	Parameter	C_b = 100 pF (max)		Units	Figure
		Min.	Max.		
f_{SCL}	I^2C_CLK clock frequency	0	1.7	MHz	
t_{SU}:STA	Set-Up time for a repeated START condition	160	–	ns	
t_{HD}:STA	Hold time (repeated) START condition.	160	–	ns	
t_{LOW}	LOW period of the I^2C_CLK clock	160	–	ns	
t_{HIGH}	HIGH period of the I^2C_CLK clock	60	–	ns	
t_{HD}:DAT	Data hold time: I^2C-bus devices	0	–	ns	
t_{SU}:DAT	Data set-up time	10	–	ns	
t_r CL	Rise time of I^2C_CLK signals	10	40	ns	
t_f CL	Fall time of I^2C_CLK signals	1	40	ns	
t_rCL1	Rise time of I^2C_CLK signal after a repeated START condition and after an acknowledge bit	10	40	ns	
t_r DA	Rise time of I^2C_DATA signals	10	80	ns	
t_f DA	Fall time of I^2C_DATA signals	1	80	ns	
$t_{SU:}$STO	Set-up time for STOP condition	160	–	ns	
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	0.1 V_{DD}	–	V	
V_{NH}	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2 V_{DD}	–	V	

Figure 75. Definition of Timing for High Speed-Mode Devices on I²C Bus



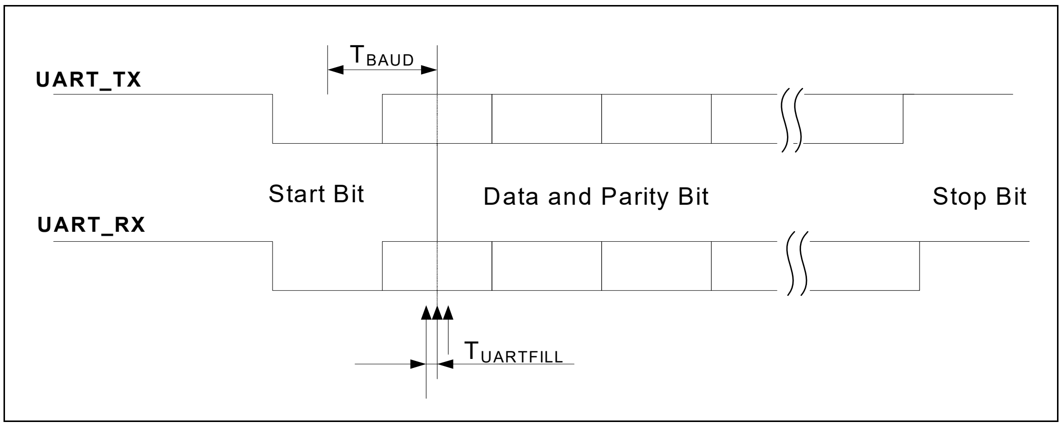
9.6.23 SIO - UART AC Specification

Table 146. UART AC Specification

Symbol	Parameter	Min.	Max.	Unit	Notes
T_{RISE}	Maximum Rise Time	2.5	5	ns	1, 2
T_{FALL}	Maximum Fall Time	2.5	5	ns	1, 2
$T_{UARTFIL}$	UART Sampling Filter Period	20		ns	3

NOTES:
1. Based on total trace length of 1-4”, Total maximum, capacitance of 27 pF and board impedance of 30–75Ω.
2. Measured from 10–90%.
3. Each bit including start and stop bit is sampled three times at center of a bit at an interval of 20 ns (minimum). If three sampled values do not agree, then UART noise error is generated.

Figure 76. UART Timing Diagram



9.6.24 JTAG AC Specification

Table 147. JTAG AC Specification

T# Parameter	Min	Max	Unit	Figure	Notes
T_P:TAP_TCK Period	15		ns		66 MHz
T_{CL}:TAP_TCK Clock Low Time	0.4 * T_{JC}		ns		
T_{CH}:TAP_TCK Clock High Time	0.4 * T_{JC}		ns		
T_{SU}:TAP_TDI, TAP_TMS Setup Time	11		ns	78	
T_H: TAP_TDI, TAP_TMS Hold Time	5		ns	78	
T_{CO}: TAP_TCK falling to TAP_TDO output valid		11	ns	78	
T_{CO}: TAP_TCK falling to TAP_TDO output high impedance		11	ns		
T_{18}: TAP_TRST# assert time	2		ns	79	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all SoC frequencies.
2. Not 100% tested. Specified by design characterization.
3. It is recommended that TAP_TMS be asserted while TAP_TRST# is being deasserted.
4. Board JTAG signal skew max = ±500 ps.

Figure 77. JTAG Timing Diagram

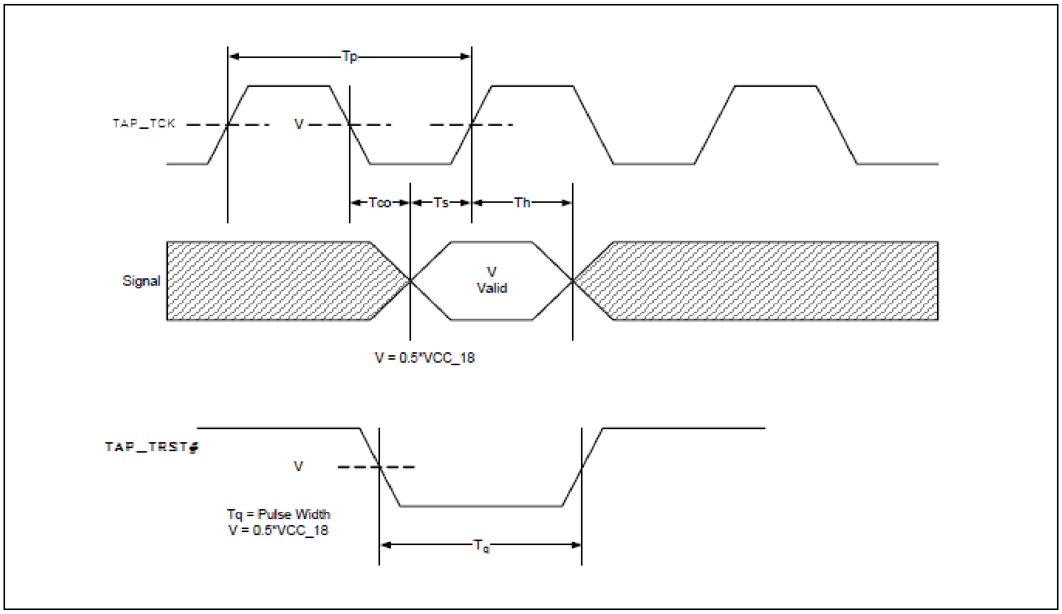
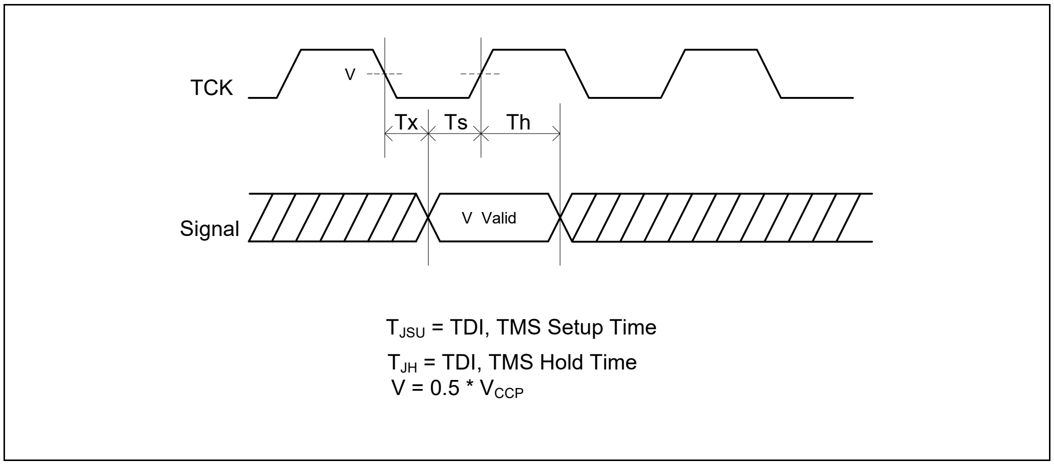


Table 148. Boundary Scan AC Specification

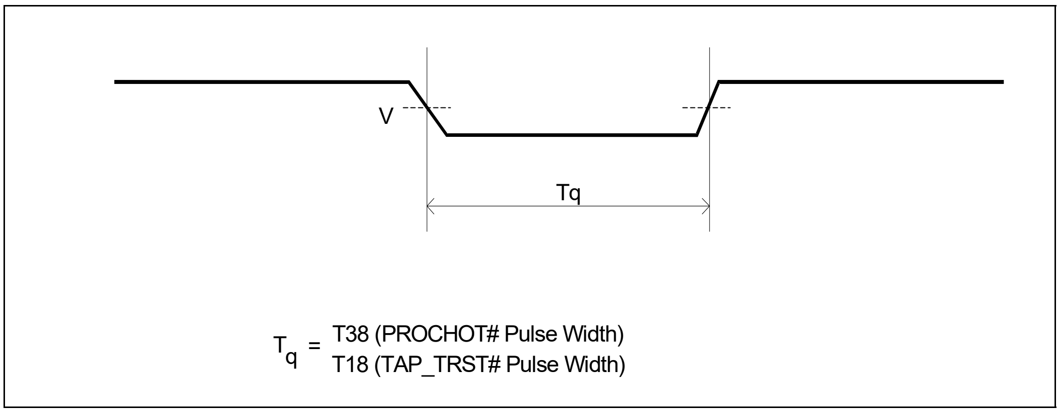
T# Parameter	Min	Max	Unit	Notes
Boundary scan all non test output/float delay	0.5	15	ns	Referenced to the falling edge of T_{CK}
Boundary scan all non test input setup	10		ns	Referenced to the falling edge of T_{CK}
Boundary scan all non test input hold	13		µs	Referenced to the falling edge of T_{CK}

Figure 78. TAP Valid Delay Timing Waveform



Refer to Table 88, Table 89, Table 90 for TAP Signal Group DC specifications and Table 147 for TAP Signal Group AC specifications.

Figure 79. Test Reset (TAP_TRST#), Async GTL Input and PROCHOT# Timing Waveform



9.6.25 General AC Timing Diagrams

Note that the measurement of the differential waveform according to these diagrams would have to be made directly at the load at the end of the line. In a real system, this is not possible because the end of the line is at the input pad of the SoC silicon.

Figure 80. Clock Cycle Time

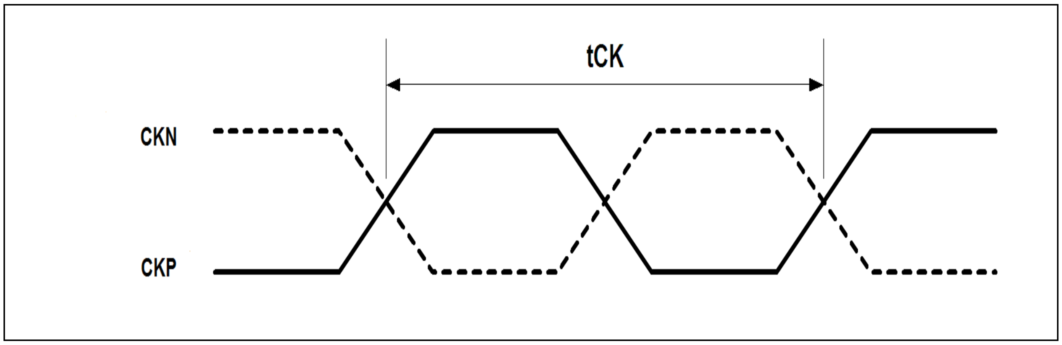


Figure 81. Clock Timing

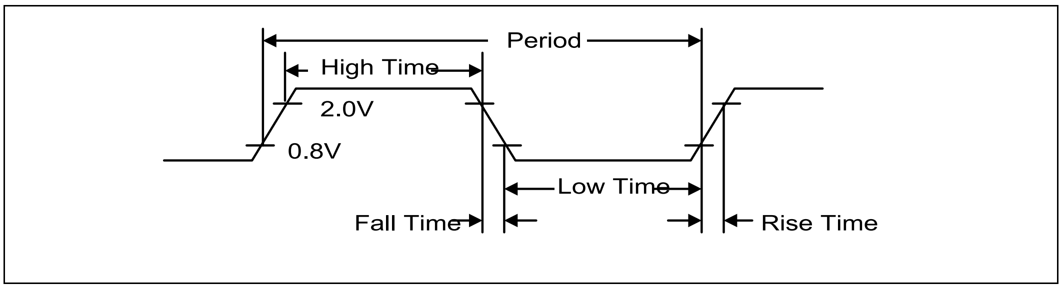


Figure 82. Valid Delay from Rising Clock Edge

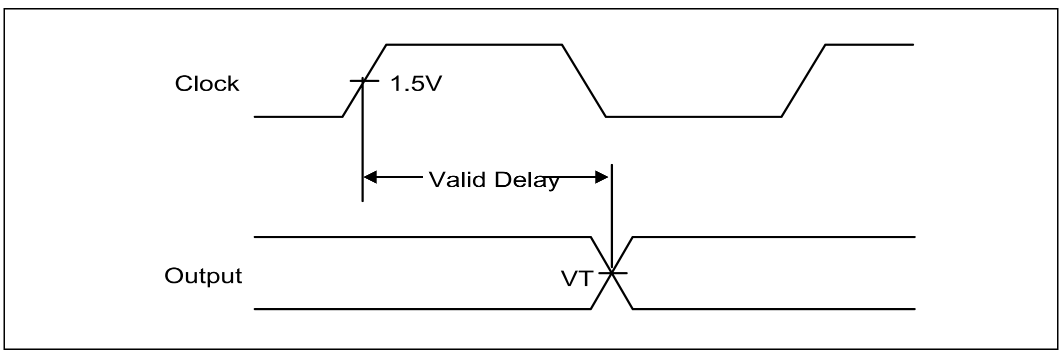


Figure 83. Setup and Hold Times

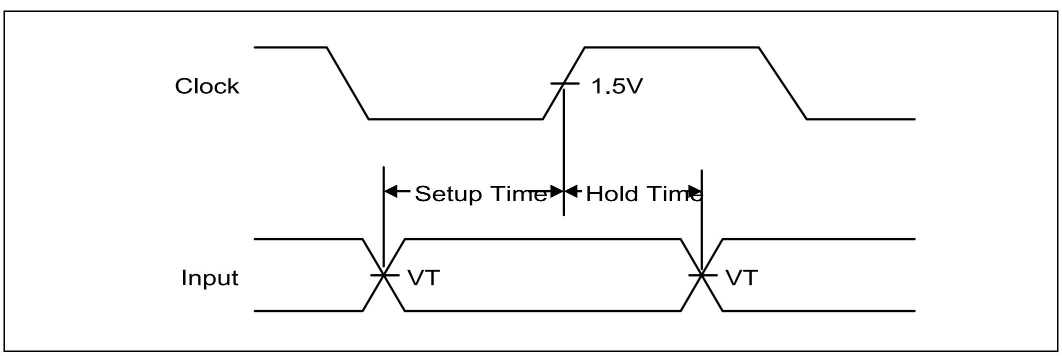


Figure 84. Float Delay

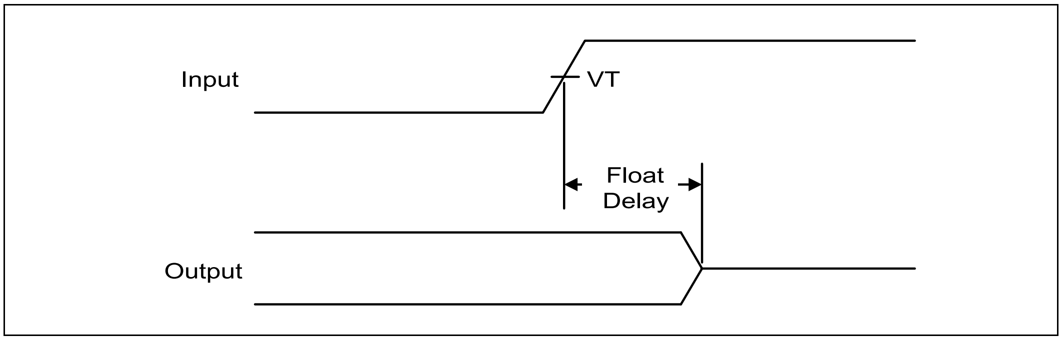


Figure 85. Pulse Width

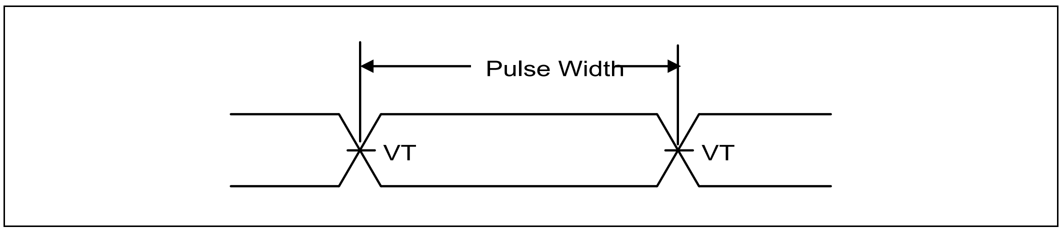


Figure 86. Output Enable Delay

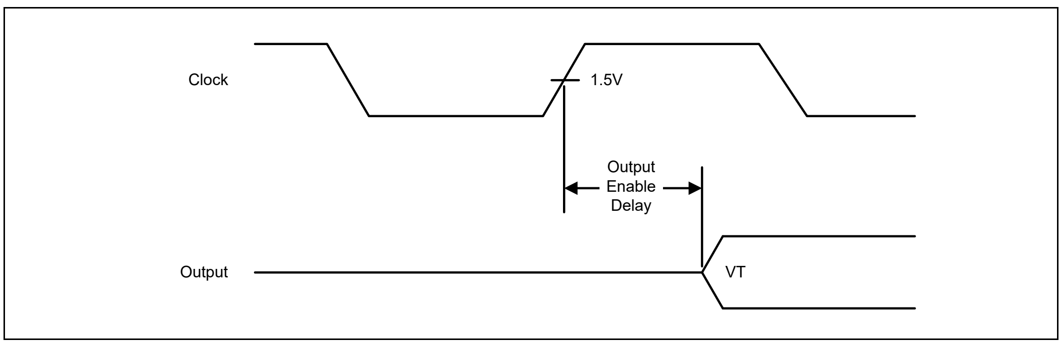


Figure 87. Differential Clock Waveform (Measured Single-ended)

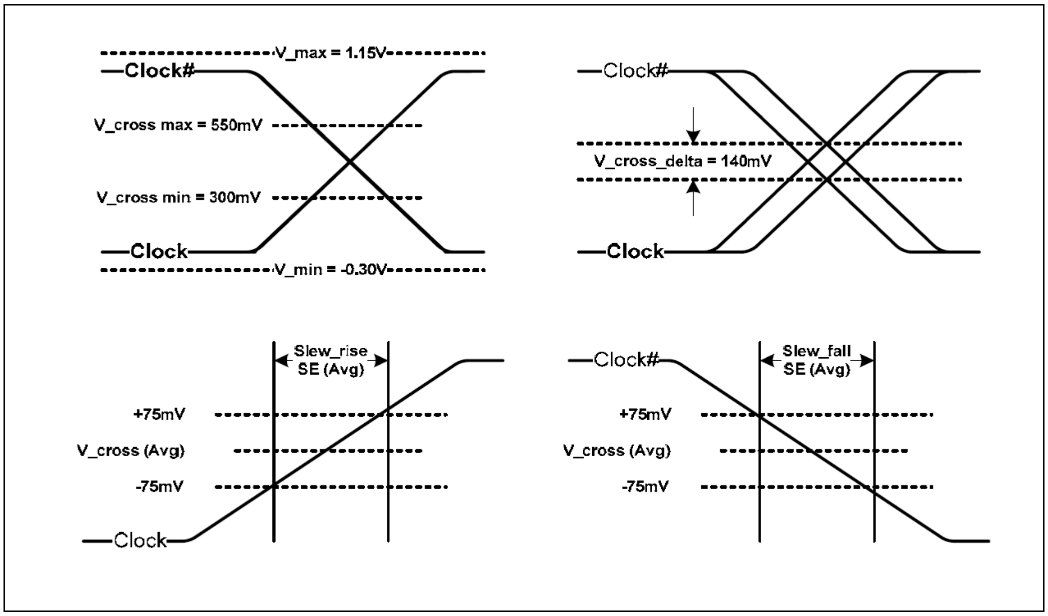
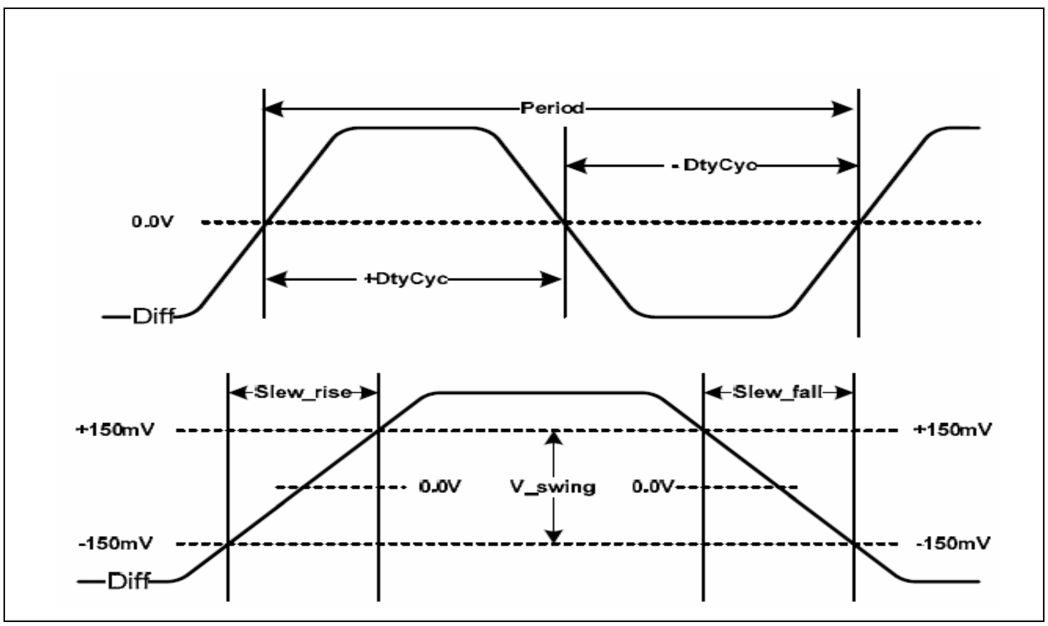


Figure 88. Differential Clock Waveform (Using Differential Probe for Measurement)



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10 Ballout and Package Information

The SoC comes in a **25 mm X 27 mm** Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 1170 solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out zone, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Refer to the *Bay Trail SoC Thermal and Mechanical Design Guide* for details on package mechanical dimensions and tolerance, as well as other key package attributes.

10.1 SoC Attributes

- Package parameters: 25 mm X 27 mm
- Ball Count:1170

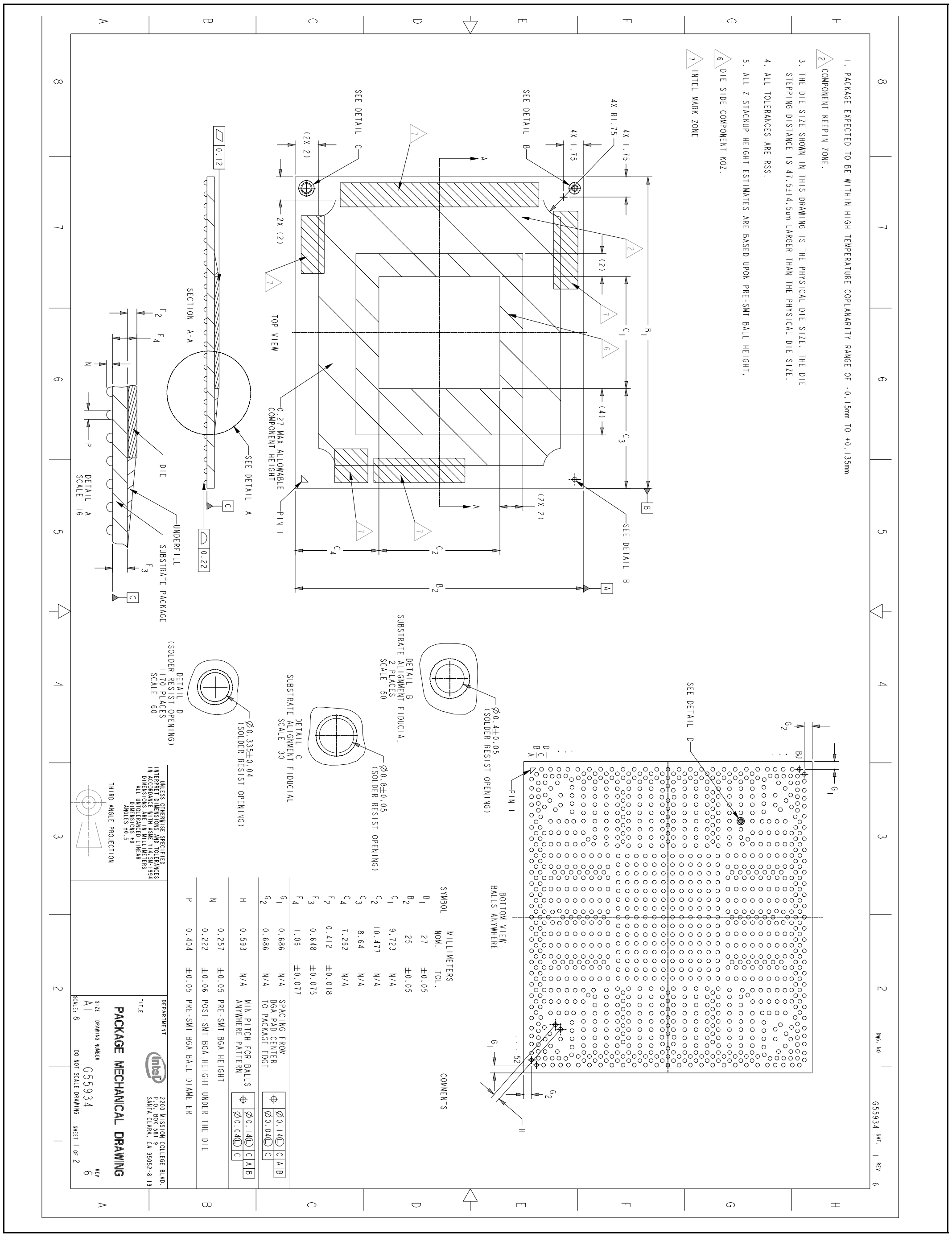
All Units: mm

Tolerances if not specified:

- .X: ± 0.1
- .XX: ± 0.05
- Angles: ± 1.0 degrees

10.2 Package Diagrams

Figure 89. Package Mechanical Drawing



10.3 Ball Name and Function by Location

Many I/O's are configurable GPIO's. These I/O's are multiplexed with other signals in the ball list. This table matches names and locations of every ball with all possible multiplexed signals (denoted as GPIO Functions). Configurable GPIO's default to function 0 during power on and may not match the ball name. BIOS (platform firmware) is responsible for enabling the platform specific configuration. Please see your BIOS vendor for details.

Note: The X & Y locations in Table 146 are measured in microns from the center of the package.

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 1 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
A3	**VSS**	11951.46	-11814.05	-	-	-	-	-
A5	**VSS**	11170.41	-11814.05	-	-	-	-	-
A6	**VSS**	10446.51	-11814.05	-	-	-	-	-
A7	**USB_HSIC_RCOMP**	9748.01	-11814.05	-	-	-	-	-
A9	**ILB_RTC_X2**	8835.9	-11814.05	-	-	-	-	-
A11	**VSS**	7774.43	-11814.05	-	-	-	-	-
A13	**GPIO_S5[09]**	6802.63	-11814.05	GPIO_S5[09]	RESERVED	RESERVED	RESERVED	RESERVED
A15	**VSS**	5830.82	-11814.05	-	-	-	-	-
A17	**GPIO_S5[03]**	4859.02	-11814.05	GPIO_S5[03]	RESERVED	RESERVED	RESERVED	PMC_WAKE_PCIE[3]#
A19	**VSS**	3887.22	-11814.05	-	-	-	-	-
A21	**PCU_SPI_MOSI**	2915.41	-11814.05	PCU_SPI_MOSI	-	-	-	-
A23	**VSS**	1943.61	-11814.05	-	-	-	-	-
A25	**SVID_DATA**	971.8	-11814.05	SVID_DATA	-	-	-	-
A27	**VSS**	0	-11814.05	-	-	-	-	-
A29	**RESERVED**	-971.8	-11814.05	RESERVED	RESERVED	-	-	-
A31	**VSS**	-1943.61	-11814.05	-	-	-	-	-
A33	**DRAM0_DQ[13]**	-2915.41	-11814.05	-	-	-	-	-
A35	**VSS**	-3887.22	-11814.05	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 2 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
A37	**DRAM0_DQ[11]**	-4859.02	-11814.05	-	-	-	-	-
A39	**VSS**	-5830.82	-11814.05	-	-	-	-	-
A41	**DRAM0_DQ[24]**	-6802.63	-11814.05	-	-	-	-	-
A43	**VSS**	-7774.43	-11814.05	-	-	-	-	-
A45	**DRAM0_DQ[26]**	-8746.24	-11814.05	-	-	-	-	-
A47	**VSS**	-9620.5	-11814.05	-	-	-	-	-
A48	**DRAM_VDD_S4**	-10293.6	-11814.05	-	-	-	-	-
A49	**VSS**	-10992.1	-11814.05	-	-	-	-	-
A51	**VSS**	-11773.15	-11814.05	-	-	-	-	-
A52	**VSS**	-12382.75	-11814.05	-	-	-	-	-
B2	**VSS**	12382.75	-11382.76	-	-	-	-	-
B4	**USB_HSIC0_DATA**	11631.68	-11237.72	-	-	-	-	-
B5	**USB_HSIC0_STROBE**	11038.33	-11222.48	-	-	-	-	-
B6	**UNCORE_V1P0_G3**	10444.99	-11220.7	-	-	-	-	-
B7	**PMC_CORE_PWROK**	9851.64	-11229.59	-	-	-	-	-
B8	**ILB_RTC_EXTPAD**	9258.3	-11224.26	-	-	-	-	-
B10	**PMC_RSMRST#**	8260.33	-11428.98	-	-	-	-	-
B12	**USB_ULPI_REFCLK**	7288.53	-11428.98	GPIO_S5[43]	USB_ULPI_REFCLK	RESERVED	RESERVED	-
B14	**GPIO_S5[06]**	6316.73	-11428.98	GPIO_S5[06]	PMC_SUSCLK[2]	RESERVED	RESERVED	RESERVED
B16	**GPIO_S5[01]**	5344.92	-11428.98	GPIO_S5[01]	RESERVED	RESERVED	RESERVED	PMC_WAKE_PCIE[1]#
B18	**GPIO_S5[00]**	4373.12	-11428.98	GPIO_S5[00]	RESERVED	-	-	-
B20	**USB_OC[1]#**	3401.31	-11428.98	USB_OC[1]#	GPIO_S5[20]	-	-	-
B22	**PCU_SPI_MISO**	2429.51	-11428.98	PCU_SPI_MISO	-	-	-	-
B24	**SVID_ALERT#**	1457.71	-11428.98	SVID_ALERT#	-	-	-	-
B26	**DDI0_BKLTCTL**	485.9	-11428.98	RESERVED	RESERVED	DDI0_BKLTCTL	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 3 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
B28	**DDI0_VDDEN**	-485.9	-11428.98	RESERVED	RESERVED	DDI0_VDDEN	-	-
B30	**RESERVED**	-1457.71	-11428.98	RESERVED	RESERVED	-	-	-
B32	**DRAM0_DQ[08]**	-2429.51	-11428.98	-	-	-	-	-
B34	**DRAM0_DQSN[1]**	-3401.31	-11428.98	-	-	-	-	-
B36	**DRAM0_DM[1]**	-4373.12	-11428.98	-	-	-	-	-
B38	**DRAM0_DQ[15]**	-5344.92	-11428.98	-	-	-	-	-
B40	**DRAM0_DQ[29]**	-6316.73	-11428.98	-	-	-	-	-
B42	**DRAM0_DM[3]**	-7288.53	-11428.98	-	-	-	-	-
B44	**DRAM0_DQSP[3]**	-8260.33	-11428.98	-	-	-	-	-
B46	**DRAM0_DQ[27]**	-9258.3	-11224.26	-	-	-	-	-
B47	**DRAM0_DQ[31]**	-9851.64	-11229.59	-	-	-	-	-
B48	**DRAM0_DQ[30]**	-10444.99	-11220.7	-	-	-	-	-
B49	**DRAM0_MA[14]**	-11038.33	-11222.48	-	-	-	-	-
B50	**DRAM0_MA[15]**	-11631.68	-11237.72	-	-	-	-	-
B52	**VSS**	-12225.02	-11225.02	-	-	-	-	-
B53	**VSS**	-12814.05	-11382.76	-	-	-	-	-
C1	**VSS**	12814.05	-10951.46	-	-	-	-	-
C3	**USB3_V1P0_G3**	11644.38	-10644.38	-	-	-	-	-
C5	**UNCORE_V1P0_G3**	10579.86	-10642.85	-	-	-	-	-
C7	**USB_RCOMPI**	9553.19	-10709.15	-	-	-	-	-
C9	**ILB_RTC_X1**	8697.98	-11028.17	-	-	-	-	-
C11	**ILB_RTC_TEST#**	7774.43	-11070.59	-	-	-	-	-
C12	**ILB_RTC_RST#**	7288.53	-10729.98	-	-	-	-	-
C13	**GPIO_S5[08]**	6802.63	-11070.59	GPIO_S5[08]	RESERVED	RESERVED	RESERVED	RESERVED
C14	**VSS**	6316.73	-10729.98	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 4 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
C15	**GPIO_S5[07]**	5830.82	-11070.59	GPIO_S5[07]	PMC_SUSCLK[3]	RESERVED	RESERVED	RESERVED
C16	**GPIO_S5[05]**	5344.92	-10729.98	GPIO_S5[05]	PMC_SUSCLK[1]	RESERVED	RESERVED	RESERVED
C17	**GPIO_S5[04]**	4859.02	-11070.59	GPIO_S5[04]	RESERVED	RESERVED	RESERVED	RESERVED
C18	**GPIO_S5[02]**	4373.12	-10729.98	GPIO_S5[02]	RESERVED	RESERVED	RESERVED	PMC_WAKE_PCIE[2]#
C19	**GPIO_S5[10]**	3887.22	-11070.59	GPIO_S5[10]	RESERVED	RESERVED	RESERVED	-
C20	**USB_OC[0]#**	3401.31	-10729.98	USB_OC[0]#	GPIO_S5[19]	-	-	-
C21	**PCU_SPI_CS[1]#**	2915.41	-11070.59	PCU_SPI_CS[1]#	GPIO_S5[21]	-	-	-
C22	**PCU_SPI_CLK**	2429.51	-10729.98	PCU_SPI_CLK	-	-	-	-
C23	**PCU_SPI_CS[0]#**	1943.61	-11070.59	PCU_SPI_CS[0]#	-	-	-	-
C24	**PROCHOT#**	1457.71	-10729.98	PROCHOT#	-	-	-	-
C25	**SVID_CLK**	971.8	-11070.59	SVID_CLK	-	-	-	-
C26	**DDI0_DDCDATA**	479.81	-10715.24	RESERVED	RESERVED	DDI0_DDCDATA	-	-
C27	**DDI0_BKLTEN**	0	-11070.59	RESERVED	RESERVED	DDI0_BKLTEN	-	-
C28	**DDI0_DDCCLK**	-479.81	-10715.24	RESERVED	RESERVED	DDI0_DDCCLK	-	-
C29	**RESERVED**	-971.8	-11070.59	RESERVED	RESERVED	-	-	-
C30	**RESERVED**	-1457.71	-10729.98	MDSI_C_TE	-	-	-	-
C31	**VSS**	-1943.61	-11070.59	-	-	-	-	-
C32	**DRAM0_DQ[09]**	-2429.51	-10729.98	-	-	-	-	-
C33	**DRAM0_DQ[12]**	-2915.41	-11070.59	-	-	-	-	-
C34	**VSS**	-3401.31	-10729.98	-	-	-	-	-
C35	**DRAM0_DQSP[1]**	-3887.22	-11070.59	-	-	-	-	-
C36	**DRAM0_DQ[10]**	-4373.12	-10729.98	-	-	-	-	-
C37	**DRAM0_DQ[14]**	-4859.02	-11070.59	-	-	-	-	-
C38	**DRAM0_DQ[21]**	-5344.92	-10729.98	-	-	-	-	-
C39	**VSS**	-5830.82	-11070.59	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 5 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
C40	**DRAM0_DQ[28]**	-6316.73	-10729.98	-	-	-	-	-
C41	**DRAM0_DQ[25]**	-6802.63	-11070.59	-	-	-	-	-
C42	**VSS**	-7288.53	-10729.98	-	-	-	-	-
C43	**DRAM0_DQSN[3]**	-7774.43	-11070.59	-	-	-	-	-
C45	**VSS**	-8697.98	-11028.17	-	-	-	-	-
C47	**DRAM0_CKE[0]**	-9553.19	-10709.15	-	-	-	-	-
C49	**VSS**	-10579.86	-10642.85	-	-	-	-	-
C51	**DRAM_VDD_S4**	-11644.38	-10644.38	-	-	-	-	-
C53	**VSS**	-12814.05	-10773.16	-	-	-	-	-
D2	**USB_HSIC1_STROBE**	12237.72	-10631.68	-	-	-	-	-
D4	**USB3_RXP[0]**	11162.79	-10162.79	-	-	-	-	-
D6	**USB_RCOMPO**	10112.76	-10238.49	-	-	-	-	-
D10	**ICLK_USB_TERM[1]**	8307.32	-10168.38	-	-	-	-	-
D12	**VSS**	7316.72	-10137.14	-	-	-	-	-
D14	**TAP_TCK**	6326.12	-10136.63	TAP_TCK	-	-	-	-
D16	**VSS**	5335.52	-10136.63	-	-	-	-	-
D18	**TAP_PRDY#**	4388.36	-10136.63	TAP_PRDY#	-	-	-	-
D20	**PMC_ACPRESENT**	3386.07	-10136.63	PMC_ACPRESENT	-	-	-	-
D22	**PMC_SLP_S3#**	2438.91	-10136.63	PMC_SLP_S3#	-	-	-	-
D24	**VSS**	1448.31	-10136.63	-	-	-	-	-
D26	**PMC_SUSPWRDNACK**	462.79	-9994.65	PMC_SUSPWRDNACK	GPIO_S5[11]	-	-	-
D27	**DDI0_HPD**	0	-10365.99	RESERVED	RESERVED	DDI0_HPD	-	-
D28	**MCSI_GPIO[02]**	-462.79	-9994.65	RESERVED	MCSI_GPIO[02]	RESERVED	-	-
D30	**VSS**	-1448.31	-10136.63	-	-	-	-	-
D32	**MCSI_GPIO[11]**	-2438.91	-10136.63	RESERVED	MCSI_GPIO[11]	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 6 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
D34	**MCSI_GPIO[05]**	-3386.07	-10136.63	RESERVED	MCSI_GPIO[05]	RESERVED	-	-
D36	**VSS**	-4388.36	-10136.63	-	-	-	-	-
D38	**VSS**	-5335.52	-10136.63	-	-	-	-	-
D40	**DRAM0_DQSP[2]**	-6326.12	-10136.63	-	-	-	-	-
D42	**DRAM0_DQ[23]**	-7316.72	-10137.14	-	-	-	-	-
D44	**DRAM_VDD_S4**	-8307.32	-10168.38	-	-	-	-	-
D48	**RESERVED**	-10112.76	-10238.49	-	-	-	-	-
D50	**DRAM0_MA[07]**	-11162.79	-10162.79	-	-	-	-	-
D52	**DRAM0_BS[2]**	-12237.72	-10631.68	-	-	-	-	-
E1	**VSS**	12814.05	-10170.41	-	-	-	-	-
E2	**USB_HSIC1_DATA**	12222.48	-10038.33	-	-	-	-	-
E3	**USB3_RXN[0]**	11642.85	-9579.86	-	-	-	-	-
E8	**VSS**	9320.02	-9747	-	-	-	-	-
E19	**VSS**	3887.22	-9818.88	-	-	-	-	-
E35	**VSS**	-3887.22	-9818.88	-	-	-	-	-
E46	**RESERVED**	-9320.02	-9747	-	-	-	-	-
E51	**DRAM0_MA[11]**	-11642.85	-9579.86	-	-	-	-	-
E52	**DRAM0_MA[09]**	-12222.48	-10038.33	-	-	-	-	-
E53	**VSS**	-12814.05	-9992.11	-	-	-	-	-
F1	**RESERVED**	12814.05	-9446.51	-	-	-	-	-
F2	**VSS**	12220.7	-9444.99	-	-	-	-	-
F5	**VSS**	10565.13	-9301.73	-	-	-	-	-
F7	**VSS**	9712.2	-9301.73	-	-	-	-	-
F10	**ICLK_USB_TERM[0]**	8307.32	-9457.18	-	-	-	-	-
F12	**TAP_TDI**	7316.72	-9463.28	TAP_TDI	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 7 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
F14	**TAP_TMS**	6326.12	-9463.28	TAP_TMS	-	-	-	-
F16	**TAP_PREQ#**	5335.52	-9463.28	TAP_PREQ#	-	-	-	-
F18	**GPIO_S5[13]**	4362.2	-9463.28	RESERVED	GPIO_S5[13]	-	-	-
F19	**VSS**	3887.22	-9107.68	-	-	-	-	-
F20	**PMC_PLTRST#**	3412.24	-9463.28	PMC_PLTRST#	-	-	-	-
F22	**PMC_SLP_S4#**	2438.91	-9463.28	PMC_SLP_S4#	-	-	-	-
F24	**VSS**	1448.31	-9463.28	-	-	-	-	-
F26	**PMC_WAKE_PCIE[0]#**	525.02	-9404.35	PMC_WAKE_PCIE[0]#	GPIO_S5[15]	-	-	-
F27	**VSS**	0	-9107.68	-	-	-	-	-
F28	**MCSI_GPIO[07]**	-525.02	-9404.35	RESERVED	MCSI_GPIO[07]	RESERVED	-	-
F30	**VSS**	-1448.31	-9463.28	-	-	-	-	-
F32	**MCSI_GPIO[06]**	-2438.91	-9463.28	RESERVED	MCSI_GPIO[06]	RESERVED	-	-
F34	**MCSI_GPIO[00]**	-3412.24	-9463.28	RESERVED	MCSI_GPIO[00]	RESERVED	-	-
F35	**VSS**	-3887.22	-9107.68	-	-	-	-	-
F36	**DRAM0_DQ[16]**	-4362.2	-9463.28	-	-	-	-	-
F38	**DRAM0_DM[2]**	-5335.52	-9463.28	-	-	-	-	-
F40	**DRAM0_DQSN[2]**	-6326.12	-9463.28	-	-	-	-	-
F42	**DRAM0_DQ[18]**	-7316.72	-9463.28	-	-	-	-	-
F44	**DRAM0_CKE[2]**	-8307.32	-9457.18	-	-	-	-	-
F47	**DRAM0_MA[12]**	-9712.2	-9301.73	-	-	-	-	-
F49	**DRAM_VDD_S4**	-10565.13	-9301.73	-	-	-	-	-
F52	**DRAM_VDD_S4**	-12220.7	-9444.99	-	-	-	-	-
F53	**DRAM_VDD_S4**	-12814.05	-9293.61	-	-	-	-	-
G1	**USB3DEV_V1P0_S3**	12814.05	-8679.18	-	-	-	-	-
G2	**USB_ULPI_CLK**	12246.36	-8852.15	GPIO_S5[31]	USB_ULPI_CLK	RESERVED	RESERVED	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 8 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
G10	**VSS**	8307.32	-8763.76	-	-	-	-	-
G12	**TAP_TRST#**	7316.72	-8752.08	TAP_TRST#	-	-	-	-
G14	**USB_DN[1]**	6326.12	-8752.08	-	-	-	-	-
G16	**TAP_TDO**	5335.52	-8752.08	TAP_TDO	-	-	-	-
G18	**PMC_SUS_STAT#**	4362.2	-8752.08	PMC_SUS_STAT#	GPIO_S5[18]	-	-	-
G20	**VSS**	3412.24	-8752.08	-	-	-	-	-
G22	**VSS**	2438.91	-8752.08	-	-	-	-	-
G24	**PMC_SUSCLK[0]**	1448.31	-8752.08	PMC_SUSCLK[0]	GPIO_S5[12]	-	-	-
G26	**VSS**	474.98	-8752.08	-	-	-	-	-
G28	**VSS**	-474.98	-8752.08	-	-	-	-	-
G30	**DDI1_DDCCLK**	-1448.31	-8752.08	RESERVED	RESERVED	DDI1_DDCCLK	-	-
G32	**VSS**	-2438.91	-8752.08	-	-	-	-	-
G34	**VSS**	-3412.24	-8752.08	-	-	-	-	-
G36	**DRAM0_DM[0]**	-4362.2	-8752.08	-	-	-	-	-
G38	**DRAM0_DQ[17]**	-5335.52	-8752.08	-	-	-	-	-
G40	**DRAM0_DQ[20]**	-6326.12	-8752.08	-	-	-	-	-
G42	**VSS**	-7316.72	-8752.08	-	-	-	-	-
G44	**DRAM0_DQ[22]**	-8307.32	-8763.76	-	-	-	-	-
G52	**DRAM0_MA[08]**	-12246.36	-8852.15	-	-	-	-	-
G53	**DRAM0_MA[05]**	-12814.05	-8620.51	-	-	-	-	-
H3	**USB_ULPI_STP**	11928.86	-8350.76	GPIO_S5[42]	USB_ULPI_STP	RESERVED	RESERVED	-
H4	**RESERVED**	11257.79	-8307.32	-	-	-	-	-
H5	**RESERVED**	10546.59	-8307.32	-	-	-	-	-
H7	**RESERVED**	9835.39	-8307.32	-	-	-	-	-
H8	**RESERVED**	9124.19	-8307.32	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 9 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
H10	**USB_DN[3]**	8307.32	-8170.42	-	-	-	-	-
H19	**VSS**	3887.22	-8396.48	-	-	-	-	-
H27	**VSS**	0	-8396.48	-	-	-	-	-
H35	**VSS**	-3887.22	-8396.48	-	-	-	-	-
H44	**DRAM0_MA[03]**	-8307.32	-8170.42	-	-	-	-	-
H46	**DRAM_VDD_S4**	-9124.19	-8307.32	-	-	-	-	-
H47	**DRAM0_MA[01]**	-9835.39	-8307.32	-	-	-	-	-
H49	**DRAM0_MA[06]**	-10546.59	-8307.32	-	-	-	-	-
H50	**DRAM0_MA[04]**	-11257.79	-8307.32	-	-	-	-	-
H51	**DRAM0_WE#**	-11928.86	-8350.76	-	-	-	-	-
J1	**VSS**	12814.05	-7815.58	-	-	-	-	-
J3	**USB_ULPI_DIR**	12070.59	-7774.43	GPIO_S5[40]	USB_ULPI_DIR	RESERVED	RESERVED	-
J12	**USB_DN[2]**	7316.72	-8040.88	-	-	-	-	-
J14	**USB_DP[1]**	6326.12	-8040.88	-	-	-	-	-
J16	**VSS**	5335.52	-8040.88	-	-	-	-	-
J18	**GPIO_S5[25]**	4362.2	-8040.88	GPIO_S5[25]	RESERVED	RESERVED	RESERVED	RESERVED
J19	**VSS**	3887.22	-7685.28	-	-	-	-	-
J20	**USB_ULPI_RST#**	3412.24	-8040.88	RESERVED	GPIO_S5[14]	USB_ULPI_RST#	-	-
J22	**VSS**	2438.91	-8040.88	-	-	-	-	-
J24	**GPIO_S5[17]**	1448.31	-8040.88	RESERVED	GPIO_S5[17]	-	-	-
J26	**PMC_PWRBTN#**	474.98	-8040.88	PMC_PWRBTN#	GPIO_S5[16]	-	-	-
J27	**VSS**	0	-7685.28	-	-	-	-	-
J28	**MCSI_GPIO[03]**	-474.98	-8040.88	RESERVED	MCSI_GPIO[03]	RESERVED	-	-
J30	**DDI1_BKLTEN**	-1448.31	-8040.88	RESERVED	RESERVED	DDI1_BKLTEN	-	-
J32	**VSS**	-2438.91	-8040.88	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 10 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
J34	**MCSI_GPIO[09]**	-3412.24	-8040.88	RESERVED	MCSI_GPIO[09]	-	-	-
J35	**VSS**	-3887.22	-7685.28	-	-	-	-	-
J36	**DRAM0_DQ[01]**	-4362.2	-8040.88	-	-	-	-	-
J38	**DRAM0_DQSP[0]**	-5335.52	-8040.88	-	-	-	-	-
J40	**VSS**	-6326.12	-8040.88	-	-	-	-	-
J42	**DRAM0_DQ[19]**	-7316.72	-8040.88	-	-	-	-	-
J51	**DRAM0_MA[13]**	-12070.59	-7774.43	-	-	-	-	-
J53	**VSS**	-12814.05	-7774.43	-	-	-	-	-
K2	**USB_ULPI_DATA[2]**	12428.98	-7288.53	GPIO_S5[34]	USB_ULPI_DATA[2]	RESERVED	RESERVED	-
K3	**USB_ULPI_DATA[3]**	11729.97	-7288.53	GPIO_S5[35]	USB_ULPI_DATA[3]	RESERVED	RESERVED	-
K4	**VSS**	11137.14	-7316.72	-	-	-	-	-
K6	**USB3_TXP[0]**	10463.28	-7316.72	-	-	-	-	-
K7	**USB3_TXN[0]**	9752.08	-7316.72	-	-	-	-	-
K9	**VSS**	9040.88	-7316.72	-	-	-	-	-
K10	**USB_DP[3]**	8329.68	-7316.72	-	-	-	-	-
K12	**USB_DP[2]**	7316.72	-7339.58	-	-	-	-	-
K14	**VSS**	6326.12	-7329.68	-	-	-	-	-
K16	**USB_DN[0]**	5335.52	-7329.68	-	-	-	-	-
K18	**GPIO_S5[27]**	4362.2	-7329.68	GPIO_S5[27]	RESERVED	RESERVED	RESERVED	RESERVED
K20	**GPIO_S5[28]**	3412.24	-7329.68	GPIO_S5[28]	RESERVED	RESERVED	RESERVED	RESERVED
K22	**VSS**	2438.91	-7329.68	-	-	-	-	-
K24	**GPIO_S5[22]**	1448.31	-7329.68	GPIO_S5[22]	RESERVED	RESERVED	RESERVED	RESERVED
K26	**PMC_BATLOW#**	474.98	-7329.68	PMC_BATLOW#	-	-	-	-
K28	**MCSI_GPIO[08]**	-474.98	-7329.68	RESERVED	MCSI_GPIO[08]	RESERVED	-	-
K30	**DDI1_HPD**	-1448.31	-7329.68	RESERVED	RESERVED	DDI1_HPD	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 11 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
K32	**VSS**	-2438.91	-7329.68	-	-	-	-	-
K34	**MCSI_GPIO[04]**	-3412.24	-7329.68	RESERVED	MCSI_GPIO[04]	RESERVED	-	-
K36	**VSS**	-4362.2	-7329.68	-	-	-	-	-
K38	**DRAM0_DQSN[0]**	-5335.52	-7329.68	-	-	-	-	-
K40	**DRAM0_DQ[06]**	-6326.12	-7329.68	-	-	-	-	-
K42	**DRAM0_DQ[07]**	-7316.72	-7339.58	-	-	-	-	-
K44	**DRAM0_BS[1]**	-8329.68	-7316.72	-	-	-	-	-
K45	**DRAM0_MA[00]**	-9040.88	-7316.72	-	-	-	-	-
K47	**DRAM0_BS[0]**	-9752.08	-7316.72	-	-	-	-	-
K48	**DRAM0_MA[10]**	-10463.28	-7316.72	-	-	-	-	-
K50	**VSS**	-11137.14	-7316.72	-	-	-	-	-
K51	**DRAM0_DQ[33]**	-11729.97	-7288.53	-	-	-	-	-
K52	**DRAM0_DQ[32]**	-12428.98	-7288.53	-	-	-	-	-
L1	**USB_ULPI_DATA[1]**	12814.05	-6802.63	GPIO_S5[33]	USB_ULPI_DATA[1]	RESERVED	RESERVED	-
L3	**USB_ULPI_DATA[7]**	12070.59	-6802.63	GPIO_S5[39]	USB_ULPI_DATA[7]	RESERVED	RESERVED	-
L13	**VSS**	6750.56	-6914.9	-	-	-	-	-
L19	**VSS**	3887.22	-6974.08	-	-	-	-	-
L27	**VSS**	0	-6974.08	-	-	-	-	-
L35	**VSS**	-3887.22	-6974.08	-	-	-	-	-
L41	**DRAM0_MA[02]**	-6750.56	-6914.9	-	-	-	-	-
L51	**DRAM0_DQ[36]**	-12070.59	-6802.63	-	-	-	-	-
L53	**DRAM0_DQ[37]**	-12814.05	-6802.63	-	-	-	-	-
M2	**USB_ULPI_DATA[4]**	12428.98	-6316.73	GPIO_S5[36]	USB_ULPI_DATA[4]	RESERVED	RESERVED	-
M3	**USB_ULPI_DATA[0]**	11729.97	-6316.73	GPIO_S5[32]	USB_ULPI_DATA[0]	RESERVED	RESERVED	-
M4	**USB3DEV_TXP[0]**	11136.63	-6326.12	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 12 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
M6	**USB3DEV_TXN[0]**	10463.28	-6326.12	-	-	-	-	-
M7	**USB3DEV_REXT[0]**	9752.08	-6326.12	-	-	-	-	-
M9	**RESERVED**	9040.88	-6326.12	-	-	-	-	-
M10	**RESERVED**	8329.68	-6326.12	-	-	-	-	-
M12	**USB3_REXT[0]**	7618.48	-6326.12	-	-	-	-	-
M13	**USB_PLL_MON**	6907.28	-6326.12	-	-	-	-	-
M14	**USB_V1P0_S3**	6326.12	-6446.01	-	-	-	-	-
M16	**USB_DP[0]**	5335.52	-6618.48	-	-	-	-	-
M18	**GPIO_S5[26]**	4362.2	-6618.48	GPIO_S5[26]	RESERVED	RESERVED	RESERVED	RESERVED
M19	**VSS**	3887.22	-6262.88	-	-	-	-	-
M20	**GPIO_S5[24]**	3412.24	-6618.48	GPIO_S5[24]	RESERVED	RESERVED	RESERVED	RESERVED
M22	**GPIO_S5[29]**	2438.91	-6618.48	GPIO_S5[29]	RESERVED	RESERVED	RESERVED	RESERVED
M24	**GPIO_S5[30]**	1448.31	-6618.48	GPIO_S5[30]	RESERVED	RESERVED	RESERVED	RESERVED
M26	**VSS**	474.98	-6618.48	-	-	-	-	-
M27	**VSS**	0	-6262.88	-	-	-	-	-
M28	**VSS**	-474.98	-6618.48	-	-	-	-	-
M30	**DDI1_BKLTCTL**	-1448.31	-6618.48	RESERVED	RESERVED	DDI1_BKLTCTL	-	-
M32	**MCSI_GPIO[01]**	-2438.91	-6618.48	RESERVED	MCSI_GPIO[01]	RESERVED	-	-
M34	**VSS**	-3412.24	-6618.48	-	-	-	-	-
M35	**VSS**	-3887.22	-6262.88	-	-	-	-	-
M36	**DRAM0_DQ[00]**	-4362.2	-6618.48	-	-	-	-	-
M38	**VSS**	-5335.52	-6618.48	-	-	-	-	-
M40	**DRAM0_DQ[03]**	-6326.12	-6446.01	-	-	-	-	-
M41	**DRAM_VDD_S4**	-6907.28	-6326.12	-	-	-	-	-
M42	**DRAM_VDD_S4**	-7618.48	-6326.12	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 13 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
M44	**DRAM0_CAS#**	-8329.68	-6326.12	-	-	-	-	-
M45	**DRAM0_RAS#**	-9040.88	-6326.12	-	-	-	-	-
M47	**VSS**	-9752.08	-6326.12	-	-	-	-	-
M48	**DRAM0_CKN[0]**	-10463.28	-6326.12	-	-	-	-	-
M50	**DRAM0_CKP[0]**	-11136.63	-6326.12	-	-	-	-	-
M51	**VSS**	-11729.97	-6316.73	-	-	-	-	-
M52	**DRAM0_DQSN[4]**	-12428.98	-6316.73	-	-	-	-	-
N1	**VSS**	12814.05	-5830.82	-	-	-	-	-
N3	**USB_ULPI_DATA[5]**	12070.59	-5830.82	GPIO_S5[37]	USB_ULPI_DATA[5]	RESERVED	RESERVED	-
N16	**VSS**	5335.52	-5907.28	-	-	-	-	-
N18	**USB_V3P3_G3**	4362.2	-5907.28	-	-	-	-	-
N20	**USB_V1P8_G3**	3412.24	-5907.28	-	-	-	-	-
N22	**PCU_V3P3_G3**	2438.91	-5907.28	-	-	-	-	-
N24	**GPIO_S5[23]**	1448.31	-5907.28	GPIO_S5[23]	RESERVED	RESERVED	RESERVED	RESERVED
N26	**GPIO_RCOMP**	474.98	-5907.28	-	-	-	-	-
N28	**CORE_VSS_SENSE**	-474.98	-5907.28	-	-	-	-	-
N30	**DDI1_VDDEN**	-1448.31	-5907.28	RESERVED	RESERVED	DDI1_VDDEN	-	-
N32	**MCSI_GPIO[10]**	-2438.91	-5907.28	RESERVED	MCSI_GPIO[10]	-	-	-
N34	**RESERVED**	-3412.24	-5907.28	-	-	-	-	-
N36	**DRAM0_DQ[05]**	-4362.2	-5907.28	-	-	-	-	-
N38	**VSS**	-5335.52	-5907.28	-	-	-	-	-
N51	**VSS**	-12070.59	-5830.82	-	-	-	-	-
N53	**DRAM0_DQSP[4]**	-12814.05	-5830.82	-	-	-	-	-
P2	**USB_ULPI_DATA[6]**	12428.98	-5344.92	GPIO_S5[38]	USB_ULPI_DATA[6]	RESERVED	RESERVED	-
P3	**USB_ULPI_NXT**	11729.97	-5344.92	GPIO_S5[41]	USB_ULPI_NXT	RESERVED	RESERVED	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 14 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
P4	**VSS**	11136.63	-5335.52	-	-	-	-	-
P6	**RESERVED**	10463.28	-5335.52	-	-	-	-	-
P7	**RESERVED**	9752.08	-5335.52	-	-	-	-	-
P9	**VSS**	9040.88	-5335.52	-	-	-	-	-
P10	**USB3DEV_RXP[0]**	8329.68	-5335.52	-	-	-	-	-
P12	**USB3DEV_RXN[0]**	7618.48	-5335.52	-	-	-	-	-
P13	**VSS**	6907.28	-5335.52	-	-	-	-	-
P14	**MCSI_RCOMP**	6304.79	-5335.52	-	-	-	-	-
P16	**VSS**	5335.52	-5196.08	-	-	-	-	-
P18	**USB_V3P3_G3**	4362.2	-5196.08	-	-	-	-	-
P19	**VSS**	3887.22	-5551.68	-	-	-	-	-
P20	**VSS**	3412.24	-5196.08	-	-	-	-	-
P22	**RTC_VCC**	2438.91	-5196.08	-	-	-	-	-
P24	**VSS**	1448.31	-5196.08	-	-	-	-	-
P26	**CORE_VCC_S3**	474.98	-5196.08	-	-	-	-	-
P27	**CORE_VCC_S3**	0	-5551.68	-	-	-	-	-
P28	**CORE_VCC_SENSE**	-474.98	-5196.08	-	-	-	-	-
P30	**DDI1_DDCDATA**	-1448.31	-5196.08	RESERVED	RESERVED	DDI1_DDCDATA	-	-
P32	**VSS**	-2438.91	-5196.08	-	-	-	-	-
P34	**RESERVED**	-3412.24	-5196.08	-	-	-	-	-
P35	**VSS**	-3887.22	-5551.68	-	-	-	-	-
P36	**DRAM0_DQ[04]**	-4362.2	-5196.08	-	-	-	-	-
P38	**VSS**	-5335.52	-5196.08	-	-	-	-	-
P40	**DRAM0_DQ[02]**	-6304.79	-5335.52	-	-	-	-	-
P41	**DRAM0_DRAMRST#**	-6907.28	-5335.52	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 15 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
P42	**DRAM0_ODT[2]**	-7618.48	-5335.52	-	-	-	-	-
P44	**DRAM0_CS[0]#**	-8329.68	-5335.52	-	-	-	-	-
P45	**DRAM0_CS[2]#**	-9040.88	-5335.52	-	-	-	-	-
P47	**VSS**	-9752.08	-5335.52	-	-	-	-	-
P48	**DRAM0_CKN[2]**	-10463.28	-5335.52	-	-	-	-	-
P50	**DRAM0_CKP[2]**	-11136.63	-5335.52	-	-	-	-	-
P51	**DRAM0_DM[4]**	-11729.97	-5344.92	-	-	-	-	-
P52	**VSS**	-12428.98	-5344.92	-	-	-	-	-
R1	**RESERVED**	12814.05	-4859.02	-	-	-	-	-
R3	**RESERVED**	12070.59	-4859.02	-	-	-	-	-
R51	**DRAM0_DQ[38]**	-12070.59	-4859.02	-	-	-	-	-
R53	**DRAM0_DQ[39]**	-12814.05	-4859.02	-	-	-	-	-
T2	**RESERVED**	12428.98	-4373.12	-	-	-	-	-
T3	**RESERVED**	11729.97	-4373.12	-	-	-	-	-
T4	**MCSI3_CLKP**	11136.63	-4388.36	-	-	-	-	-
T6	**MCSI3_CLKN**	10463.28	-4362.2	-	-	-	-	-
T7	**MCSI1_CLKN**	9752.08	-4362.2	-	-	-	-	-
T9	**MCSI1_CLKP**	9040.88	-4362.2	-	-	-	-	-
T10	**MCSI1_DP[3]**	8329.68	-4362.2	-	-	-	-	-
T12	**MCSI1_DN[3]**	7618.48	-4362.2	-	-	-	-	-
T13	**MCSI2_DP[0]**	6907.28	-4362.2	-	-	-	-	-
T14	**MCSI2_DN[0]**	6196.08	-4362.2	-	-	-	-	-
T40	**VSS**	-6196.08	-4362.2	-	-	-	-	-
T41	**DRAM0_ODT[0]**	-6907.28	-4362.2	-	-	-	-	-
T42	**DRAM0_DQSP[5]**	-7618.48	-4362.2	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 16 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
T44	**DRAM0_DQSN[5]**	-8329.68	-4362.2	-	-	-	-	-
T45	**DRAM0_DQ[41]**	-9040.88	-4362.2	-	-	-	-	-
T47	**DRAM0_DQ[40]**	-9752.08	-4362.2	-	-	-	-	-
T48	**DRAM0_DQ[44]**	-10463.28	-4362.2	-	-	-	-	-
T50	**DRAM0_DQ[45]**	-11136.63	-4388.36	-	-	-	-	-
T51	**DRAM0_DQ[35]**	-11729.97	-4373.12	-	-	-	-	-
T52	**DRAM0_DQ[34]**	-12428.98	-4373.12	-	-	-	-	-
U1	**VSS**	12814.05	-3887.22	-	-	-	-	-
U3	**VSS**	12070.59	-3887.22	-	-	-	-	-
U5	**VSS**	10818.88	-3887.22	-	-	-	-	-
U6	**VSS**	10107.68	-3887.22	-	-	-	-	-
U8	**VSS**	9396.48	-3887.22	-	-	-	-	-
U9	**VSS**	8685.28	-3887.22	-	-	-	-	-
U11	**VSS**	7974.08	-3887.22	-	-	-	-	-
U12	**VSS**	7262.88	-3887.22	-	-	-	-	-
U14	**VSS**	6551.68	-3887.22	-	-	-	-	-
U16	**USB_VSSA**	5307.33	-4313.94	-	-	-	-	-
U18	**USB_V1P0_S3**	4549.14	-4313.94	-	-	-	-	-
U19	**USB_V1P0_S3**	3790.95	-4313.94	-	-	-	-	-
U21	**VSS**	3032.76	-4313.94	-	-	-	-	-
U22	**UNCORE_V1P0_G3**	2274.57	-4313.94	-	-	-	-	-
U24	**UNCORE_V1P8_G3**	1516.38	-4313.94	-	-	-	-	-
U25	**PMC_V1P8_G3**	758.19	-4313.94	-	-	-	-	-
U27	**CORE_VCC_S3**	0	-4313.94	-	-	-	-	-
U29	**CORE_VCC_S3**	-758.19	-4313.94	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 17 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
U30	**VSS**	-1516.38	-4313.94	-	-	-	-	-
U32	**VSS**	-2274.57	-4313.94	-	-	-	-	-
U33	**CORE_V1P05_S3**	-3032.76	-4313.94	-	-	-	-	-
U35	**CORE_V1P05_S3**	-3790.95	-4313.94	-	-	-	-	-
U36	**UNCORE_V1P35_S3_F4**	-4549.14	-4313.94	-	-	-	-	-
U38	**MIPI_V1P8_S3**	-5307.33	-4313.94	-	-	-	-	-
U40	**VSS**	-6551.68	-3887.22	-	-	-	-	-
U42	**VSS**	-7262.88	-3887.22	-	-	-	-	-
U43	**VSS**	-7974.08	-3887.22	-	-	-	-	-
U45	**VSS**	-8685.28	-3887.22	-	-	-	-	-
U46	**VSS**	-9396.48	-3887.22	-	-	-	-	-
U48	**VSS**	-10107.68	-3887.22	-	-	-	-	-
U49	**VSS**	-10818.88	-3887.22	-	-	-	-	-
U51	**VSS**	-12070.59	-3887.22	-	-	-	-	-
U53	**VSS**	-12814.05	-3887.22	-	-	-	-	-
V2	**RESERVED**	12428.98	-3401.31	-	-	-	-	-
V3	**RESERVED**	11729.97	-3401.31	-	-	-	-	-
V4	**RESERVED**	11136.63	-3386.07	-	-	-	-	-
V6	**RESERVED**	10463.28	-3412.24	-	-	-	-	-
V7	**VSS**	9752.08	-3412.24	-	-	-	-	-
V9	**MCSI1_DP[2]**	9040.88	-3412.24	-	-	-	-	-
V10	**MCSI1_DN[2]**	8329.68	-3412.24	-	-	-	-	-
V12	**VSS**	7618.48	-3412.24	-	-	-	-	-
V13	**MCSI2_CLKP**	6907.28	-3412.24	-	-	-	-	-
V14	**MCSI2_CLKN**	6196.08	-3412.24	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 18 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
V16	**VSS**	5307.33	-3529.58	-	-	-	-	-
V18	**USB_HSIC_V1P24_G3**	4549.14	-3529.58	-	-	-	-	-
V19	**VSS**	3790.95	-3529.58	-	-	-	-	-
V21	**VSS**	3032.76	-3529.58	-	-	-	-	-
V22	**UNCORE_V1P0_G3**	2274.57	-3529.58	-	-	-	-	-
V24	**UNCORE_V1P0_S3**	1516.38	-3529.58	-	-	-	-	-
V25	**PCU_V1P8_G3**	758.19	-3529.58	-	-	-	-	-
V27	**CORE_VCC_S3**	0	-3529.58	-	-	-	-	-
V29	**CORE_VCC_S3**	-758.19	-3529.58	-	-	-	-	-
V30	**CORE_VCC_S3**	-1516.38	-3529.58	-	-	-	-	-
V32	**SVID_V1P0_S3**	-2274.57	-3529.58	-	-	-	-	-
V33	**CORE_V1P05_S3**	-3032.76	-3529.58	-	-	-	-	-
V35	**VSS**	-3790.95	-3529.58	-	-	-	-	-
V36	**UNCORE_V1P35_S3_F3**	-4549.14	-3529.58	-	-	-	-	-
V38	**DRAM_VDD_S4**	-5307.33	-3529.58	-	-	-	-	-
V40	**VSS**	-6196.08	-3412.24	-	-	-	-	-
V41	**DRAM0_DQ[43]**	-6907.28	-3412.24	-	-	-	-	-
V42	**DRAM0_DM[5]**	-7618.48	-3412.24	-	-	-	-	-
V44	**VSS**	-8329.68	-3412.24	-	-	-	-	-
V45	**DRAM0_DQ[48]**	-9040.88	-3412.24	-	-	-	-	-
V47	**DRAM0_DQ[49]**	-9752.08	-3412.24	-	-	-	-	-
V48	**DRAM0_DQ[52]**	-10463.28	-3412.24	-	-	-	-	-
V50	**DRAM0_DQ[53]**	-11136.63	-3386.07	-	-	-	-	-
V51	**VSS**	-11729.97	-3401.31	-	-	-	-	-
V52	**DRAM0_DQ[56]**	-12428.98	-3401.31	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 19 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
W1	**RESERVED**	12814.05	-2915.41	-	-	-	-	-
W3	**RESERVED**	12070.59	-2915.41	-	-	-	-	-
W51	**DRAM0_DQ[57]**	-12070.59	-2915.41	-	-	-	-	-
W53	**DRAM0_DQ[60]**	-12814.05	-2915.41	-	-	-	-	-
Y2	**RESERVED**	12428.98	-2429.51	-	-	-	-	-
Y3	**RESERVED**	11729.97	-2429.51	-	-	-	-	-
Y4	**RESERVED**	11136.63	-2438.91	-	-	-	-	-
Y6	**RESERVED**	10463.28	-2438.91	-	-	-	-	-
Y7	**VSS**	9752.08	-2438.91	-	-	-	-	-
Y9	**VSS**	9040.88	-2438.91	-	-	-	-	-
Y10	**VSS**	8329.68	-2438.91	-	-	-	-	-
Y12	**MCSI1_DN[1]**	7618.48	-2438.91	-	-	-	-	-
Y13	**MCSI1_DP[1]**	6907.28	-2438.91	-	-	-	-	-
Y14	**VSS**	6196.08	-2438.91	-	-	-	-	-
Y16	**VSS**	5307.33	-2745.23	-	-	-	-	-
Y18	**USB3DEV_V1P0_S3**	4549.14	-2745.23	-	-	-	-	-
Y19	**USB3_V1P0_G3**	3790.95	-2745.23	-	-	-	-	-
Y21	**VSS**	3032.76	-2745.23	-	-	-	-	-
Y22	**UNCORE_V1P0_S3**	2274.57	-2745.23	-	-	-	-	-
Y24	**UNCORE_V1P0_S3**	1516.38	-2745.23	-	-	-	-	-
Y25	**VSS**	758.19	-2745.23	-	-	-	-	-
Y27	**CORE_VCC_S3**	0	-2745.23	-	-	-	-	-
Y29	**CORE_VCC_S3**	-758.19	-2745.23	-	-	-	-	-
Y30	**CORE_VCC_S3**	-1516.38	-2745.23	-	-	-	-	-
Y32	**CORE_V1P05_S3**	-2274.57	-2745.23	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 20 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
Y33	**VSS**	-3032.76	-2745.23	-	-	-	-	-
Y35	**DRAM_V1P0_S3**	-3790.95	-2745.23	-	-	-	-	-
Y36	**DRAM_V1P0_S3**	-4549.14	-2745.23	-	-	-	-	-
Y38	**DRAM_VDD_S4**	-5307.33	-2745.23	-	-	-	-	-
Y40	**DRAM0_DQ[42]**	-6196.08	-2438.91	-	-	-	-	-
Y41	**VSS**	-6907.28	-2438.91	-	-	-	-	-
Y42	**DRAM0_DQ[46]**	-7618.48	-2438.91	-	-	-	-	-
Y44	**VSS**	-8329.68	-2438.91	-	-	-	-	-
Y45	**DRAM0_DQ[55]**	-9040.88	-2438.91	-	-	-	-	-
Y47	**DRAM0_DQSP[6]**	-9752.08	-2438.91	-	-	-	-	-
Y48	**DRAM0_DQSN[6]**	-10463.28	-2438.91	-	-	-	-	-
Y50	**DRAM0_DM[6]**	-11136.63	-2438.91	-	-	-	-	-
Y51	**DRAM0_DQ[61]**	-11729.97	-2429.51	-	-	-	-	-
Y52	**DRAM0_DM[7]**	-12428.98	-2429.51	-	-	-	-	-
AA1	**VSS**	12814.05	-1943.61	-	-	-	-	-
AA3	**VSS**	12070.59	-1943.61	-	-	-	-	-
AA16	**VSS**	5307.33	-1960.88	-	-	-	-	-
AA18	**USB_ULPI_V1P8_G3**	4549.14	-1960.88	-	-	-	-	-
AA19	**VSS**	3790.95	-1960.88	-	-	-	-	-
AA21	**VSS**	3032.76	-1960.88	-	-	-	-	-
AA22	**TP2_CORE_VCC_S3**	2274.57	-1960.88	-	-	-	-	-
AA24	**UNCORE_VNN_S3**	1516.38	-1960.88	-	-	-	-	-
AA25	**UNCORE_V1P35_S3_F5**	758.19	-1960.88	-	-	-	-	-
AA27	**CORE_VCC_S3**	0	-1960.88	-	-	-	-	-
AA29	**CORE_VCC_S3**	-758.19	-1960.88	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 21 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AA30	**CORE_VCC_S3**	-1516.38	-1960.88	-	-	-	-	-
AA32	**VSS**	-2274.57	-1960.88	-	-	-	-	-
AA33	**CORE_V1P05_S3**	-3032.76	-1960.88	-	-	-	-	-
AA35	**VSS**	-3790.95	-1960.88	-	-	-	-	-
AA36	**DRAM_V1P0_S3**	-4549.14	-1960.88	-	-	-	-	-
AA38	**VSS**	-5307.33	-1960.88	-	-	-	-	-
AA51	**DRAM0_DQSN[7]**	-12070.59	-1943.61	-	-	-	-	-
AA53	**VSS**	-12814.05	-1943.61	-	-	-	-	-
AB2	**RESERVED**	12428.98	-1457.71	-	-	-	-	-
AB3	**RESERVED**	11729.97	-1457.71	-	-	-	-	-
AB4	**VSS**	11136.63	-1448.31	-	-	-	-	-
AB6	**VSS**	10463.28	-1448.31	-	-	-	-	-
AB7	**RESERVED**	9752.08	-1448.31	-	-	-	-	-
AB9	**RESERVED**	9040.88	-1448.31	-	-	-	-	-
AB10	**VSS**	8329.68	-1448.31	-	-	-	-	-
AB12	**MCSI1_DP[0]**	7618.48	-1448.31	-	-	-	-	-
AB13	**MCSI1_DN[0]**	6907.28	-1448.31	-	-	-	-	-
AB14	**RESERVED**	6196.08	-1448.31	-	-	-	-	-
AB40	**DRAM0_DQ[47]**	-6196.08	-1448.31	-	-	-	-	-
AB41	**VSS**	-6907.28	-1448.31	-	-	-	-	-
AB42	**DRAM_CORE_PWROK**	-7618.48	-1448.31	-	-	-	-	-
AB44	**DRAM0_DQ[54]**	-8329.68	-1448.31	-	-	-	-	-
AB45	**VSS**	-9040.88	-1448.31	-	-	-	-	-
AB47	**VSS**	-9752.08	-1448.31	-	-	-	-	-
AB48	**VSS**	-10463.28	-1448.31	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 22 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AB50	**VSS**	-11136.63	-1448.31	-	-	-	-	-
AB51	**VSS**	-11729.97	-1457.71	-	-	-	-	-
AB52	**DRAM0_DQSP[7]**	-12428.98	-1457.71	-	-	-	-	-
AC1	**DDI1_TXN[3]**	12814.05	-971.8	-	-	-	-	-
AC3	**DDI1_TXP[3]**	12070.59	-971.8	-	-	-	-	-
AC16	**VSS**	5307.33	-1176.53	-	-	-	-	-
AC18	**VSS**	4549.14	-1176.53	-	-	-	-	-
AC19	**VSS**	3790.95	-1176.53	-	-	-	-	-
AC21	**VSS**	3032.76	-1176.53	-	-	-	-	-
AC22	**UNCORE_VNN_S3**	2274.57	-1176.53	-	-	-	-	-
AC24	**UNCORE_VNN_S3**	1516.38	-1176.53	-	-	-	-	-
AC25	**VSS**	758.19	-1176.53	-	-	-	-	-
AC27	**CORE_VCC_S3**	0	-1176.53	-	-	-	-	-
AC29	**CORE_VCC_S3**	-758.19	-1176.53	-	-	-	-	-
AC30	**CORE_VCC_S3**	-1516.38	-1176.53	-	-	-	-	-
AC32	**CORE_V1P05_S3**	-2274.57	-1176.53	-	-	-	-	-
AC33	**VSS**	-3032.76	-1176.53	-	-	-	-	-
AC35	**VSS**	-3790.95	-1176.53	-	-	-	-	-
AC36	**VSS**	-4549.14	-1176.53	-	-	-	-	-
AC38	**VSS**	-5307.33	-1176.53	-	-	-	-	-
AC51	**DRAM0_DQ[59]**	-12070.59	-971.8	-	-	-	-	-
AC53	**DRAM0_DQ[58]**	-12814.05	-971.8	-	-	-	-	-
AD2	**DDI1_TXN[2]**	12428.98	-485.9	-	-	-	-	-
AD3	**DDI1_TXP[2]**	11715.24	-479.81	-	-	-	-	-
AD4	**RESERVED**	10994.64	-462.79	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 23 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AD6	**RESERVED**	10404.35	-525.02	-	-	-	-	-
AD7	**VSS**	9752.08	-474.98	-	-	-	-	-
AD9	**RESERVED**	9040.88	-474.98	-	-	-	-	-
AD10	**RESERVED**	8329.68	-474.98	-	-	-	-	-
AD12	**RESERVED**	7618.48	-474.98	-	-	-	-	-
AD13	**ICLK_RCOMP**	6907.28	-474.98	-	-	-	-	-
AD14	**ICLK_ICOMP**	6196.08	-474.98	-	-	-	-	-
AD16	**MIPI_V1P24_S3**	5307.33	-392.18	-	-	-	-	-
AD18	**MIPI_V1P24_S3**	4549.14	-392.18	-	-	-	-	-
AD19	**VSS**	3790.95	-392.18	-	-	-	-	-
AD21	**VSS**	3032.76	-392.18	-	-	-	-	-
AD22	**UNCORE_VNN_S3**	2274.57	-392.18	-	-	-	-	-
AD24	**UNCORE_VNN_S3**	1516.38	-392.18	-	-	-	-	-
AD25	**VSS**	758.19	-392.18	-	-	-	-	-
AD27	**CORE_VCC_S3**	0	-392.18	-	-	-	-	-
AD29	**CORE_VCC_S3**	-758.19	-392.18	-	-	-	-	-
AD30	**CORE_VCC_S3**	-1516.38	-392.18	-	-	-	-	-
AD32	**VSS**	-2274.57	-392.18	-	-	-	-	-
AD33	**VSS**	-3032.76	-392.18	-	-	-	-	-
AD35	**DRAM_V1P0_S3**	-3790.95	-392.18	-	-	-	-	-
AD36	**DRAM_V1P35_S3_F1**	-4549.14	-392.18	-	-	-	-	-
AD38	**DRAM_VDD_S4**	-5307.33	-392.18	-	-	-	-	-
AD40	**RESERVED**	-6196.08	-474.98	-	-	-	-	-
AD41	**RESERVED**	-6907.28	-474.98	-	-	-	-	-
AD42	**DRAM_VDD_S4_PWROK**	-7618.48	-474.98	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 24 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AD44	**DRAM_RCOMP[0]**	-8329.68	-474.98	-	-	-	-	-
AD45	**DRAM_RCOMP[2]**	-9040.88	-474.98	-	-	-	-	-
AD47	**VSS**	-9752.08	-474.98	-	-	-	-	-
AD48	**DRAM0_DQ[50]**	-10404.35	-525.02	-	-	-	-	-
AD50	**DRAM0_DQ[51]**	-10994.64	-462.79	-	-	-	-	-
AD51	**DRAM0_DQ[63]**	-11715.24	-479.81	-	-	-	-	-
AD52	**DRAM0_DQ[62]**	-12428.98	-485.9	-	-	-	-	-
AE1	**VSS**	12814.05	0	-	-	-	-	-
AE3	**VSS**	12070.59	0	-	-	-	-	-
AE4	**VSS**	11365.99	0	-	-	-	-	-
AE6	**VSS**	10107.68	0	-	-	-	-	-
AE8	**VSS**	9396.48	0	-	-	-	-	-
AE9	**VSS**	8685.28	0	-	-	-	-	-
AE11	**VSS**	7974.08	0	-	-	-	-	-
AE12	**VSS**	7262.88	0	-	-	-	-	-
AE14	**VSS**	6551.68	0	-	-	-	-	-
AE40	**VSS**	-6551.68	0	-	-	-	-	-
AE42	**VSS**	-7262.88	0	-	-	-	-	-
AE43	**VSS**	-7974.08	0	-	-	-	-	-
AE45	**VSS**	-8685.28	0	-	-	-	-	-
AE46	**VSS**	-9396.48	0	-	-	-	-	-
AE48	**VSS**	-10107.68	0	-	-	-	-	-
AE50	**VSS**	-11365.99	0	-	-	-	-	-
AE51	**VSS**	-12070.59	0	-	-	-	-	-
AE53	**VSS**	-12814.05	0	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 25 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AF2	**DDI1_TXN[1]**	12428.98	485.9	-	-	-	-	-
AF3	**DDI1_TXP[1]**	11715.24	479.81	-	-	-	-	-
AF4	**PCIE_CLKP[0]**	10994.64	462.79	-	-	-	-	-
AF6	**PCIE_CLKN[0]**	10404.35	525.02	-	-	-	-	-
AF7	**PCIE_CLKP[1]**	9752.08	474.98	-	-	-	-	-
AF9	**PCIE_CLKN[1]**	9040.88	474.98	-	-	-	-	-
AF10	**VSS**	8329.68	474.98	-	-	-	-	-
AF12	**VSS**	7618.48	474.98	-	-	-	-	-
AF13	**RESERVED**	6907.28	474.98	-	-	-	-	-
AF14	**RESERVED**	6196.08	474.98	-	-	-	-	-
AF16	**UNCORE_V1P0_S3**	5307.33	392.18	-	-	-	-	-
AF18	**UNCORE_V1P0_S3**	4549.14	392.18	-	-	-	-	-
AF19	**UNCORE_V1P35_S3_F6**	3790.95	392.18	-	-	-	-	-
AF21	**UNCORE_V1P0_S3**	3032.76	392.18	-	-	-	-	-
AF22	**UNCORE_VNN_S3**	2274.57	392.18	-	-	-	-	-
AF24	**UNCORE_VNN_S3**	1516.38	392.18	-	-	-	-	-
AF25	**VSS**	758.19	392.18	-	-	-	-	-
AF27	**CORE_VCC_S3**	0	392.18	-	-	-	-	-
AF29	**CORE_VCC_S3**	-758.19	392.18	-	-	-	-	-
AF30	**TP_CORE_V1P05_S4**	-1516.38	392.18	-	-	-	-	-
AF32	**VSS**	-2274.57	392.18	-	-	-	-	-
AF33	**CORE_V1P05_S3**	-3032.76	392.18	-	-	-	-	-
AF35	**DRAM_V1P0_S3**	-3790.95	392.18	-	-	-	-	-
AF36	**DRAM_V1P0_S3**	-4549.14	392.18	-	-	-	-	-
AF38	**DRAM_VDD_S4**	-5307.33	392.18	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 26 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AF40	**RESERVED**	-6196.08	474.98	-	-	-	-	-
AF41	**RESERVED**	-6907.28	474.98	-	-	-	-	-
AF42	**ICLK_DRAM_TERM[0]**	-7618.48	474.98	-	-	-	-	-
AF44	**DRAM_VREF**	-8329.68	474.98	-	-	-	-	-
AF45	**DRAM_RCOMP[1]**	-9040.88	474.98	-	-	-	-	-
AF47	**VSS**	-9752.08	474.98	-	-	-	-	-
AF48	**DRAM1_DQ[50]**	-10404.35	525.02	-	-	-	-	-
AF50	**DRAM1_DQ[51]**	-10994.64	462.79	-	-	-	-	-
AF51	**DRAM1_DQ[63]**	-11715.24	479.81	-	-	-	-	-
AF52	**DRAM1_DQ[62]**	-12428.98	485.9	-	-	-	-	-
AG1	**DDI1_TXN[0]**	12814.05	971.8	-	-	-	-	-
AG3	**DDI1_TXP[0]**	12070.59	971.8	-	-	-	-	-
AG16	**VSS**	5307.33	1176.53	-	-	-	-	-
AG18	**ICLK_V1P35_S3_F2**	4549.14	1176.53	-	-	-	-	-
AG19	**UNCORE_V1P35_S3_F1**	3790.95	1176.53	-	-	-	-	-
AG21	**UNCORE_V1P0_S3**	3032.76	1176.53	-	-	-	-	-
AG22	**UNCORE_VNN_S3**	2274.57	1176.53	-	-	-	-	-
AG24	**UNCORE_VNN_S3**	1516.38	1176.53	-	-	-	-	-
AG25	**VSS**	758.19	1176.53	-	-	-	-	-
AG27	**CORE_VCC_S3**	0	1176.53	-	-	-	-	-
AG29	**CORE_VCC_S3**	-758.19	1176.53	-	-	-	-	-
AG30	**CORE_VCC_S3**	-1516.38	1176.53	-	-	-	-	-
AG32	**UNCORE_V1P35_S3_F2**	-2274.57	1176.53	-	-	-	-	-
AG33	**CORE_V1P05_S3**	-3032.76	1176.53	-	-	-	-	-
AG35	**CORE_V1P05_S3**	-3790.95	1176.53	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 27 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AG36	**VSS**	-4549.14	1176.53	-	-	-	-	-
AG38	**VSS**	-5307.33	1176.53	-	-	-	-	-
AG51	**DRAM1_DQ[59]**	-12070.59	971.8	-	-	-	-	-
AG53	**DRAM1_DQ[58]**	-12814.05	971.8	-	-	-	-	-
AH2	**RSVD_GND[3]**	12428.98	1457.71	-	-	-	-	-
AH3	**RSVD_GND[2]**	11729.97	1457.71	-	-	-	-	-
AH4	**VSS**	11136.63	1448.31	-	-	-	-	-
AH6	**VSS**	10463.28	1448.31	-	-	-	-	-
AH7	**VSS**	9752.08	1448.31	-	-	-	-	-
AH9	**VSS**	9040.88	1448.31	-	-	-	-	-
AH10	**ICLK_OSCOUT**	8329.68	1448.31	-	-	-	-	-
AH12	**ICLK_OSCIN**	7618.48	1448.31	-	-	-	-	-
AH13	**RESERVED**	6907.28	1448.31	-	-	-	-	-
AH14	**RESERVED**	6196.08	1448.31	-	-	-	-	-
AH40	**DRAM1_DQ[47]**	-6196.08	1448.31	-	-	-	-	-
AH41	**VSS**	-6907.28	1448.31	-	-	-	-	-
AH42	**ICLK_DRAM_TERM[1]**	-7618.48	1448.31	-	-	-	-	-
AH44	**DRAM1_DQ[54]**	-8329.68	1448.31	-	-	-	-	-
AH45	**VSS**	-9040.88	1448.31	-	-	-	-	-
AH47	**VSS**	-9752.08	1448.31	-	-	-	-	-
AH48	**VSS**	-10463.28	1448.31	-	-	-	-	-
AH50	**VSS**	-11136.63	1448.31	-	-	-	-	-
AH51	**VSS**	-11729.97	1457.71	-	-	-	-	-
AH52	**DRAM1_DQSP[7]**	-12428.98	1457.71	-	-	-	-	-
AJ1	**VSS**	12814.05	1943.61	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 28 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AJ3	**VSS**	12070.59	1943.61	-	-	-	-	-
AJ16	**VSS**	5307.33	1960.88	-	-	-	-	-
AJ18	**DDI_V1P0_S3**	4549.14	1960.88	-	-	-	-	-
AJ19	**ICLK_V1P35_S3_F1**	3790.95	1960.88	-	-	-	-	-
AJ21	**VSS**	3032.76	1960.88	-	-	-	-	-
AJ22	**UNCORE_VNN_S3**	2274.57	1960.88	-	-	-	-	-
AJ24	**UNCORE_VNN_S3**	1516.38	1960.88	-	-	-	-	-
AJ25	**VSS**	758.19	1960.88	-	-	-	-	-
AJ27	**VSS**	0	1960.88	-	-	-	-	-
AJ29	**VSS**	-758.19	1960.88	-	-	-	-	-
AJ30	**VSS**	-1516.38	1960.88	-	-	-	-	-
AJ32	**VSS**	-2274.57	1960.88	-	-	-	-	-
AJ33	**VSS**	-3032.76	1960.88	-	-	-	-	-
AJ35	**VSS**	-3790.95	1960.88	-	-	-	-	-
AJ36	**DRAM_V1P0_S3**	-4549.14	1960.88	-	-	-	-	-
AJ38	**VSS**	-5307.33	1960.88	-	-	-	-	-
AJ51	**DRAM1_DQSN[7]**	-12070.59	1943.61	-	-	-	-	-
AJ53	**VSS**	-12814.05	1943.61	-	-	-	-	-
AK2	**DDI1_AUXN**	12428.98	2429.51	-	-	-	-	-
AK3	**DDI1_AUXP**	11729.97	2429.51	-	-	-	-	-
AK4	**PCIE_CLKN[2]**	11136.63	2438.91	-	-	-	-	-
AK6	**PCIE_CLKP[2]**	10463.28	2438.91	-	-	-	-	-
AK7	**RESERVED**	9752.08	2438.91	-	-	-	-	-
AK9	**RESERVED**	9040.88	2438.91	-	-	-	-	-
AK10	**VSS**	8329.68	2438.91	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 29 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AK12	**DDI_RCOMP_P**	7618.48	2438.91	-	-	-	-	-
AK13	**DDI_RCOMP_N**	6907.28	2438.91	-	-	-	-	-
AK14	**VSS**	6196.08	2438.91	-	-	-	-	-
AK16	**VSS**	5307.33	2745.23	-	-	-	-	-
AK18	**PCIE_V1P0_S3**	4549.14	2745.23	-	-	-	-	-
AK19	**DDI_V1P0_S3**	3790.95	2745.23	-	-	-	-	-
AK21	**DDI_V1P0_S3**	3032.76	2745.23	-	-	-	-	-
AK22	**UNCORE_VNN_S3**	2274.57	2745.23	-	-	-	-	-
AK24	**UNCORE_VNN_S3**	1516.38	2745.23	-	-	-	-	-
AK25	**UNCORE_VNN_S3**	758.19	2745.23	-	-	-	-	-
AK27	**UNCORE_VNN_S3**	0	2745.23	-	-	-	-	-
AK29	**UNCORE_VNN_S3**	-758.19	2745.23	-	-	-	-	-
AK30	**UNCORE_VNN_S3**	-1516.38	2745.23	-	-	-	-	-
AK32	**UNCORE_VNN_S3**	-2274.57	2745.23	-	-	-	-	-
AK33	**VSS**	-3032.76	2745.23	-	-	-	-	-
AK35	**DRAM_V1P0_S3**	-3790.95	2745.23	-	-	-	-	-
AK36	**DRAM_V1P0_S3**	-4549.14	2745.23	-	-	-	-	-
AK38	**DRAM_VDD_S4**	-5307.33	2745.23	-	-	-	-	-
AK40	**DRAM1_DQ[42]**	-6196.08	2438.91	-	-	-	-	-
AK41	**VSS**	-6907.28	2438.91	-	-	-	-	-
AK42	**DRAM1_DQ[46]**	-7618.48	2438.91	-	-	-	-	-
AK44	**VSS**	-8329.68	2438.91	-	-	-	-	-
AK45	**DRAM1_DQ[55]**	-9040.88	2438.91	-	-	-	-	-
AK47	**DRAM1_DQSP[6]**	-9752.08	2438.91	-	-	-	-	-
AK48	**DRAM1_DQSN[6]**	-10463.28	2438.91	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 30 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AK50	**DRAM1_DM[6]**	-11136.63	2438.91	-	-	-	-	-
AK51	**DRAM1_DQ[61]**	-11729.97	2429.51	-	-	-	-	-
AK52	**DRAM1_DM[7]**	-12428.98	2429.51	-	-	-	-	-
AL1	**DDI0_AUXN**	12814.05	2915.41	-	-	-	-	-
AL3	**DDI0_AUXP**	12070.59	2915.41	-	-	-	-	-
AL51	**DRAM1_DQ[57]**	-12070.59	2915.41	-	-	-	-	-
AL53	**DRAM1_DQ[60]**	-12814.05	2915.41	-	-	-	-	-
AM2	**RSVD_GND[1]**	12428.98	3401.31	-	-	-	-	-
AM3	**RSVD_GND[0]**	11729.97	3401.31	-	-	-	-	-
AM4	**PCIE_CLKN[3]**	11136.63	3386.07	-	-	-	-	-
AM6	**PCIE_CLKP[3]**	10463.28	3412.24	-	-	-	-	-
AM7	**VSS**	9752.08	3412.24	-	-	-	-	-
AM9	**RESERVED**	9040.88	3412.24	-	-	-	-	-
AM10	**RESERVED**	8329.68	3412.24	-	-	-	-	-
AM12	**VSS**	7618.48	3412.24	-	-	-	-	-
AM13	**RESERVED**	6907.28	3412.24	-	-	-	-	-
AM14	**RESERVED**	6196.08	3412.24	-	-	-	-	-
AM16	**DDI_V1P0_S3**	5307.33	3529.58	-	-	-	-	-
AM18	**PCIE_V1P0_S3**	4549.14	3529.58	-	-	-	-	-
AM19	**VSS**	3790.95	3529.58	-	-	-	-	-
AM21	**PCIE_V1P0_S3**	3032.76	3529.58	-	-	-	-	-
AM22	**UNCORE_VNN_S3**	2274.57	3529.58	-	-	-	-	-
AM24	**VSS**	1516.38	3529.58	-	-	-	-	-
AM25	**VSS**	758.19	3529.58	-	-	-	-	-
AM27	**LPC_V1P8V3P3_S3**	0	3529.58	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 31 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AM29	**VSS**	-758.19	3529.58	-	-	-	-	-
AM30	**UNCORE_V1P8_S3**	-1516.38	3529.58	-	-	-	-	-
AM32	**HDA_LPE_V1P5V1P8_S3**	-2274.57	3529.58	-	-	-	-	-
AM33	**VSS**	-3032.76	3529.58	-	-	-	-	-
AM35	**VSS**	-3790.95	3529.58	-	-	-	-	-
AM36	**VSS**	-4549.14	3529.58	-	-	-	-	-
AM38	**DRAM_VDD_S4**	-5307.33	3529.58	-	-	-	-	-
AM40	**VSS**	-6196.08	3412.24	-	-	-	-	-
AM41	**DRAM1_DQ[43]**	-6907.28	3412.24	-	-	-	-	-
AM42	**DRAM1_DM[5]**	-7618.48	3412.24	-	-	-	-	-
AM44	**VSS**	-8329.68	3412.24	-	-	-	-	-
AM45	**DRAM1_DQ[48]**	-9040.88	3412.24	-	-	-	-	-
AM47	**DRAM1_DQ[49]**	-9752.08	3412.24	-	-	-	-	-
AM48	**DRAM1_DQ[52]**	-10463.28	3412.24	-	-	-	-	-
AM50	**DRAM1_DQ[53]**	-11136.63	3386.07	-	-	-	-	-
AM51	**VSS**	-11729.97	3401.31	-	-	-	-	-
AM52	**DRAM1_DQ[56]**	-12428.98	3401.31	-	-	-	-	-
AN1	**VSS**	12814.05	3887.22	-	-	-	-	-
AN3	**VSS**	12070.59	3887.22	-	-	-	-	-
AN5	**VSS**	10818.88	3887.22	-	-	-	-	-
AN6	**VSS**	10107.68	3887.22	-	-	-	-	-
AN8	**VSS**	9396.48	3887.22	-	-	-	-	-
AN9	**VSS**	8685.28	3887.22	-	-	-	-	-
AN11	**VSS**	7974.08	3887.22	-	-	-	-	-
AN12	**VSS**	7262.88	3887.22	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 32 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AN14	**VSS**	6551.68	3887.22	-	-	-	-	-
AN16	**VSSA**	5307.33	4313.94	-	-	-	-	-
AN18	**PCIE_SATA_V1P0_S3**	4549.14	4313.94	-	-	-	-	-
AN19	**SATA_V1P0_S3**	3790.95	4313.94	-	-	-	-	-
AN21	**PCIE_V1P0_S3**	3032.76	4313.94	-	-	-	-	-
AN22	**VSS**	2274.57	4313.94	-	-	-	-	-
AN24	**VGA_V3P3_S3**	1516.38	4313.94	-	-	-	-	-
AN25	**GPIO_V1P0_S3**	758.19	4313.94	-	-	-	-	-
AN27	**SD3_V1P8V3P3_S3**	0	4313.94	-	-	-	-	-
AN29	**UNCORE_V1P0_S3**	-758.19	4313.94	-	-	-	-	-
AN30	**UNCORE_V1P0_S3**	-1516.38	4313.94	-	-	-	-	-
AN32	**UNCORE_V1P8_S3**	-2274.57	4313.94	-	-	-	-	-
AN33	**VSS**	-3032.76	4313.94	-	-	-	-	-
AN35	**VSS**	-3790.95	4313.94	-	-	-	-	-
AN36	**VSS**	-4549.14	4313.94	-	-	-	-	-
AN38	**VSS**	-5307.33	4313.94	-	-	-	-	-
AN40	**VSS**	-6551.68	3887.22	-	-	-	-	-
AN42	**VSS**	-7262.88	3887.22	-	-	-	-	-
AN43	**VSS**	-7974.08	3887.22	-	-	-	-	-
AN45	**VSS**	-8685.28	3887.22	-	-	-	-	-
AN46	**VSS**	-9396.48	3887.22	-	-	-	-	-
AN48	**VSS**	-10107.68	3887.22	-	-	-	-	-
AN49	**VSS**	-10818.88	3887.22	-	-	-	-	-
AN51	**VSS**	-12070.59	3887.22	-	-	-	-	-
AN53	**VSS**	-12814.05	3887.22	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 33 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AP2	**DDI0_TXN[3]**	12428.98	4373.12	-	-	-	-	-
AP3	**DDI0_TXP[3]**	11729.97	4373.12	-	-	-	-	-
AP4	**PCIE_TXN[3]**	11136.63	4388.36	-	-	-	-	-
AP6	**PCIE_TXP[3]**	10463.28	4362.2	-	-	-	-	-
AP7	**PCIE_RXN[3]**	9752.08	4362.2	-	-	-	-	-
AP9	**PCIE_RXP[3]**	9040.88	4362.2	-	-	-	-	-
AP10	**PCIE_RXN[2]**	8329.68	4362.2	-	-	-	-	-
AP12	**PCIE_RXP[2]**	7618.48	4362.2	-	-	-	-	-
AP13	**PCIE_RCOMP_N**	6907.28	4362.2	-	-	-	-	-
AP14	**PCIE_RCOMP_P**	6196.08	4362.2	-	-	-	-	-
AP40	**VSS**	-6196.08	4362.2	-	-	-	-	-
AP41	**DRAM1_ODT[0]**	-6907.28	4362.2	-	-	-	-	-
AP42	**DRAM1_DQSP[5]**	-7618.48	4362.2	-	-	-	-	-
AP44	**DRAM1_DQSN[5]**	-8329.68	4362.2	-	-	-	-	-
AP45	**DRAM1_DQ[41]**	-9040.88	4362.2	-	-	-	-	-
AP47	**DRAM1_DQ[40]**	-9752.08	4362.2	-	-	-	-	-
AP48	**DRAM1_DQ[44]**	-10463.28	4362.2	-	-	-	-	-
AP50	**DRAM1_DQ[45]**	-11136.63	4388.36	-	-	-	-	-
AP51	**DRAM1_DQ[35]**	-11729.97	4373.12	-	-	-	-	-
AP52	**DRAM1_DQ[34]**	-12428.98	4373.12	-	-	-	-	-
AR1	**DDI0_TXN[2]**	12814.05	4859.02	-	-	-	-	-
AR3	**DDI0_TXP[2]**	12070.59	4859.02	-	-	-	-	-
AR51	**DRAM1_DQ[38]**	-12070.59	4859.02	-	-	-	-	-
AR53	**DRAM1_DQ[39]**	-12814.05	4859.02	-	-	-	-	-
AT2	**DDI0_TXP[1]**	12428.98	5344.92	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 34 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AT3	**DDI0_TXN[1]**	11729.97	5344.92	-	-	-	-	-
AT4	**VSS**	11136.63	5335.52	-	-	-	-	-
AT6	**PCIE_TXN[2]**	10463.28	5335.52	-	-	-	-	-
AT7	**PCIE_TXP[2]**	9752.08	5335.52	-	-	-	-	-
AT9	**PCIE_RXN[1]**	9040.88	5335.52	-	-	-	-	-
AT10	**PCIE_RXP[1]**	8329.68	5335.52	-	-	-	-	-
AT12	**VSS**	7618.48	5335.52	-	-	-	-	-
AT13	**PCIE_RXN[0]**	6907.28	5335.52	-	-	-	-	-
AT14	**PCIE_RXP[0]**	6304.79	5335.52	-	-	-	-	-
AT16	**VSS**	5335.52	5196.08	-	-	-	-	-
AT18	**SATA_RCOMP_N**	4362.2	5196.08	-	-	-	-	-
AT19	**VSS**	3887.22	5551.68	-	-	-	-	-
AT20	**MMC1_D[3]**	3412.24	5196.08	GPIO_S0_SC[020]	MMC1_D[3]	-	MMC1_45_D[3]	-
AT22	**MMC1_CLK**	2438.91	5196.08	GPIO_S0_SC[016]	MMC1_CLK	-	MMC1_45_CLK	-
AT24	**VSS**	1448.31	5196.08	-	-	-	-	-
AT26	**MMC1_D[6]**	474.98	5196.08	GPIO_S0_SC[023]	MMC1_D[6]	-	MMC1_45_D[6]	-
AT27	**VSS**	0	5551.68	-	-	-	-	-
AT28	**SD3_D[0]**	-474.98	5196.08	GPIO_S0_SC[034]	SD3_D[0]	-	-	-
AT30	**VSS**	-1448.31	5196.08	-	-	-	-	-
AT32	**SIO_PWM[1]**	-2438.91	5196.08	GPIO_S0_SC[095]	SIO_PWM[1]	-	-	-
AT34	**RESERVED**	-3412.24	5196.08	RESERVED	-	-	-	-
AT35	**VSS**	-3887.22	5551.68	-	-	-	-	-
AT36	**DRAM1_DQ[17]**	-4362.2	5196.08	-	-	-	-	-
AT38	**VSS**	-5335.52	5196.08	-	-	-	-	-
AT40	**DRAM1_DQ[19]**	-6304.79	5335.52	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 35 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AT41	**DRAM1_DRAMRST#**	-6907.28	5335.52	-	-	-	-	-
AT42	**DRAM1_ODT[2]**	-7618.48	5335.52	-	-	-	-	-
AT44	**DRAM1_CS[0]#**	-8329.68	5335.52	-	-	-	-	-
AT45	**DRAM1_CS[2]#**	-9040.88	5335.52	-	-	-	-	-
AT47	**VSS**	-9752.08	5335.52	-	-	-	-	-
AT48	**DRAM1_CKN[2]**	-10463.28	5335.52	-	-	-	-	-
AT50	**DRAM1_CKP[2]**	-11136.63	5335.52	-	-	-	-	-
AT51	**DRAM1_DM[4]**	-11729.97	5344.92	-	-	-	-	-
AT52	**VSS**	-12428.98	5344.92	-	-	-	-	-
AU1	**VSS**	12814.05	5830.82	-	-	-	-	-
AU3	**VSS**	12070.59	5830.82	-	-	-	-	-
AU16	**SATA_RXP[0]**	5335.52	5907.28	-	-	-	-	-
AU18	**SATA_RCOMP_P**	4362.2	5907.28	-	-	-	-	-
AU20	**MMC1_D[7]**	3412.24	5907.28	GPIO_S0_SC[024]	MMC1_D[7]	-	MMC1_45_D[7]	-
AU22	**MMC1_D[1]**	2438.91	5907.28	GPIO_S0_SC[018]	MMC1_D[1]	-	MMC1_45_D[1]	-
AU24	**VSS**	1448.31	5907.28	-	-	-	-	-
AU26	**MMC1_D[5]**	474.98	5907.28	GPIO_S0_SC[022]	MMC1_D[5]	-	MMC1_45_D[5]	-
AU28	**SD3_D[2]**	-474.98	5907.28	GPIO_S0_SC[036]	SD3_D[2]	-	-	-
AU30	**VSS**	-1448.31	5907.28	-	-	-	-	-
AU32	**SIO_PWM[0]**	-2438.91	5907.28	GPIO_S0_SC[094]	SIO_PWM[0]	-	-	-
AU34	**SIO_UART1_RXD**	-3412.24	5907.28	GPIO_S0_SC[070]	SIO_UART1_RXD	RESERVED	-	-
AU36	**DRAM1_DQ[16]**	-4362.2	5907.28	-	-	-	-	-
AU38	**VSS**	-5335.52	5907.28	-	-	-	-	-
AU51	**VSS**	-12070.59	5830.82	-	-	-	-	-
AU53	**DRAM1_DQSP[4]**	-12814.05	5830.82	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 36 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AV2	**DDI0_TXN[0]**	12428.98	6316.73	-	-	-	-	-
AV3	**DDI0_TXP[0]**	11729.97	6316.73	-	-	-	-	-
AV4	**PCIE_TXN[1]**	11136.63	6326.12	-	-	-	-	-
AV6	**PCIE_TXP[1]**	10463.28	6326.12	-	-	-	-	-
AV7	**VSS**	9752.08	6326.12	-	-	-	-	-
AV9	**RESERVED**	9040.88	6326.12	-	-	-	-	-
AV10	**RESERVED**	8329.68	6326.12	-	-	-	-	-
AV12	**VSS**	7618.48	6326.12	-	-	-	-	-
AV13	**VSS**	6907.28	6326.12	-	-	-	-	-
AV14	**VSS**	6326.12	6446.01	-	-	-	-	-
AV16	**SATA_RXN[0]**	5335.52	6618.48	-	-	-	-	-
AV18	**VSS**	4362.2	6618.48	-	-	-	-	-
AV19	**VSS**	3887.22	6262.88	-	-	-	-	-
AV20	**MMC1_D[0]**	3412.24	6618.48	GPIO_S0_SC[017]	MMC1_D[0]	-	MMC1_45_D[0]	-
AV22	**MMC1_D[2]**	2438.91	6618.48	GPIO_S0_SC[019]	MMC1_D[2]	-	MMC1_45_D[2]	-
AV24	**VSS**	1448.31	6618.48	-	-	-	-	-
AV26	**MMC1_CMD**	474.98	6618.48	GPIO_S0_SC[025]	MMC1_CMD	-	MMC1_45_CMD	-
AV27	**VSS**	0	6262.88	-	-	-	-	-
AV28	**SD3_CMD**	-474.98	6618.48	GPIO_S0_SC[039]	SD3_CMD	-	-	-
AV30	**VSS**	-1448.31	6618.48	-	-	-	-	-
AV32	**SIO_SPI_CS#**	-2438.91	6618.48	GPIO_S0_SC[066]	SIO_SPI_CS#	-	-	-
AV34	**SIO_UART1_TXD**	-3412.24	6618.48	GPIO_S0_SC[071]	SIO_UART1_TXD	RESERVED	-	-
AV35	**VSS**	-3887.22	6262.88	-	-	-	-	-
AV36	**DRAM1_DQ[21]**	-4362.2	6618.48	-	-	-	-	-
AV38	**VSS**	-5335.52	6618.48	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 37 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AV40	**DRAM1_DQ[18]**	-6326.12	6446.01	-	-	-	-	-
AV41	**DRAM_VDD_S4**	-6907.28	6326.12	-	-	-	-	-
AV42	**DRAM_VDD_S4**	-7618.48	6326.12	-	-	-	-	-
AV44	**DRAM1_CAS#**	-8329.68	6326.12	-	-	-	-	-
AV45	**DRAM1_RAS#**	-9040.88	6326.12	-	-	-	-	-
AV47	**VSS**	-9752.08	6326.12	-	-	-	-	-
AV48	**DRAM1_CKN[0]**	-10463.28	6326.12	-	-	-	-	-
AV50	**DRAM1_CKP[0]**	-11136.63	6326.12	-	-	-	-	-
AV51	**VSS**	-11729.97	6316.73	-	-	-	-	-
AV52	**DRAM1_DQSN[4]**	-12428.98	6316.73	-	-	-	-	-
AW1	**VGA_IREF**	12814.05	6802.63	-	-	-	-	-
AW3	**VSS**	12070.59	6802.63	-	-	-	-	-
AW13	**VSS**	6750.56	6914.9	-	-	-	-	-
AW19	**VSS**	3887.22	6974.08	-	-	-	-	-
AW27	**VSS**	0	6974.08	-	-	-	-	-
AW35	**VSS**	-3887.22	6974.08	-	-	-	-	-
AW41	**DRAM1_MA[02]**	-6750.56	6914.9	-	-	-	-	-
AW51	**DRAM1_DQ[36]**	-12070.59	6802.63	-	-	-	-	-
AW53	**DRAM1_DQ[37]**	-12814.05	6802.63	-	-	-	-	-
AY2	**VGA_BLUE**	12428.98	7288.53	-	-	-	-	-
AY3	**VGA_IRTN**	11729.97	7288.53	-	-	-	-	-
AY4	**VSS**	11137.14	7316.72	-	-	-	-	-
AY6	**PCIE_TXN[0]**	10463.28	7316.72	-	-	-	-	-
AY7	**PCIE_TXP[0]**	9752.08	7316.72	-	-	-	-	-
AY9	**VSS**	9040.88	7316.72	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 38 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
AY10	**VSS**	8329.68	7316.72	-	-	-	-	-
AY12	**SATA_LED#**	7316.72	7339.58	GPIO_S0_SC[002]	SATA_LED#	-	-	-
AY14	**SATA_GP[1]**	6326.12	7329.68	GPIO_S0_SC[001]	SATA_GP[1]	SATA_DEVSLP[0]	-	-
AY16	**SATA_RXP[1]**	5335.52	7329.68	-	-	-	-	-
AY18	**MMC1_RCOMP**	4362.2	7329.68	-	-	-	-	-
AY20	**SD2_D[0]**	3412.24	7329.68	GPIO_S0_SC[028]	SD2_D[0]	-	-	-
AY22	**VSS**	2438.91	7329.68	-	-	-	-	-
AY24	**MMC1_D[4]**	1448.31	7329.68	GPIO_S0_SC[021]	MMC1_D[4]	-	MMC1_45_D[4]	-
AY26	**SD3_CLK**	474.98	7329.68	GPIO_S0_SC[033]	SD3_CLK	-	-	-
AY28	**SIO_SPI_MOSI**	-474.98	7329.68	GPIO_S0_SC[068]	SIO_SPI_MOSI	-	-	-
AY30	**SIO_SPI_CLK**	-1448.31	7329.68	GPIO_S0_SC[069]	SIO_SPI_CLK	-	-	-
AY32	**VSS**	-2438.91	7329.68	-	-	-	-	-
AY34	**SIO_UART1_CTS#**	-3412.24	7329.68	GPIO_S0_SC[073]	SIO_UART1_CTS#	-	-	-
AY36	**VSS**	-4362.2	7329.68	-	-	-	-	-
AY38	**DRAM1_DQSN[2]**	-5335.52	7329.68	-	-	-	-	-
AY40	**DRAM1_DQ[23]**	-6326.12	7329.68	-	-	-	-	-
AY42	**DRAM1_DQ[22]**	-7316.72	7339.58	-	-	-	-	-
AY44	**DRAM1_BS[1]**	-8329.68	7316.72	-	-	-	-	-
AY45	**DRAM1_MA[00]**	-9040.88	7316.72	-	-	-	-	-
AY47	**DRAM1_BS[0]**	-9752.08	7316.72	-	-	-	-	-
AY48	**DRAM1_MA[10]**	-10463.28	7316.72	-	-	-	-	-
AY50	**VSS**	-11137.14	7316.72	-	-	-	-	-
AY51	**DRAM1_DQ[33]**	-11729.97	7288.53	-	-	-	-	-
AY52	**DRAM1_DQ[32]**	-12428.98	7288.53	-	-	-	-	-
BA1	**VGA_GREEN**	12814.05	7774.43	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 39 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BA3	**VGA_RED**	12070.59	7774.43	-	-	-	-	-
BA12	**SATA_GP[0]**	7316.72	8040.88	GPIO_S0_SC[000]	SATA_GP[0]	-	-	-
BA14	**VSS**	6326.12	8040.88	-	-	-	-	-
BA16	**SATA_RXN[1]**	5335.52	8040.88	-	-	-	-	-
BA18	**SD2_CLK**	4362.2	8040.88	GPIO_S0_SC[027]	SD2_CLK	-	-	-
BA19	**VSS**	3887.22	7685.28	-	-	-	-	-
BA20	**SD2_D[2]**	3412.24	8040.88	GPIO_S0_SC[030]	SD2_D[2]	-	-	-
BA22	**VSS**	2438.91	8040.88	-	-	-	-	-
BA24	**MMC1_RST#**	1448.31	8040.88	GPIO_S0_SC[026]	MMC1_RST#	SATA_DEVSLP[0]	MMC1_45_RST#	-
BA26	**SD3_D[3]**	474.98	8040.88	GPIO_S0_SC[037]	SD3_D[3]	-	-	-
BA27	**VSS**	0	7685.28	-	-	-	-	-
BA28	**SIO_SPI_MISO**	-474.98	8040.88	GPIO_S0_SC[067]	SIO_SPI_MISO	-	-	-
BA30	**LPE_I2S2_FRM**	-1448.31	8040.88	GPIO_S0_SC[063]	LPE_I2S2_FRM	RESERVED	-	-
BA32	**VSS**	-2438.91	8040.88	-	-	-	-	-
BA34	**SIO_UART1_RTS#**	-3412.24	8040.88	GPIO_S0_SC[072]	SIO_UART1_RTS#	-	-	-
BA35	**VSS**	-3887.22	7685.28	-	-	-	-	-
BA36	**DRAM1_DQ[20]**	-4362.2	8040.88	-	-	-	-	-
BA38	**DRAM1_DQSP[2]**	-5335.52	8040.88	-	-	-	-	-
BA40	**VSS**	-6326.12	8040.88	-	-	-	-	-
BA42	**DRAM1_DQ[02]**	-7316.72	8040.88	-	-	-	-	-
BA51	**DRAM1_MA[13]**	-12070.59	7774.43	-	-	-	-	-
BA53	**VSS**	-12814.05	7774.43	-	-	-	-	-
BB3	**RESERVED**	11928.86	8350.76	-	-	-	-	-
BB4	**RESERVED**	11257.79	8307.32	-	-	-	-	-
BB5	**RSVD_GND[6]**	10546.59	8307.32	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 40 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BB7	**RSVD_GND[7]**	9835.39	8307.32	-	-	-	-	-
BB8	**UNCORE_VNN_SENSE**	9124.19	8307.32	-	-	-	-	-
BB10	**RSVD_GND[4]**	8307.32	8170.42	-	-	-	-	-
BB19	**VSS**	3887.22	8396.48	-	-	-	-	-
BB27	**VSS**	0	8396.48	-	-	-	-	-
BB35	**VSS**	-3887.22	8396.48	-	-	-	-	-
BB44	**DRAM1_MA[03]**	-8307.32	8170.42	-	-	-	-	-
BB46	**DRAM_VDD_S4**	-9124.19	8307.32	-	-	-	-	-
BB47	**DRAM1_MA[01]**	-9835.39	8307.32	-	-	-	-	-
BB49	**DRAM1_MA[06]**	-10546.59	8307.32	-	-	-	-	-
BB50	**DRAM1_MA[04]**	-11257.79	8307.32	-	-	-	-	-
BB51	**DRAM1_WE#**	-11928.86	8350.76	-	-	-	-	-
BC1	**VGA_DDCCLK**	12814.05	8620.51	VGA_DDCCLK	-	-	-	-
BC2	**VGA_DDCDATA**	12246.36	8852.15	VGA_DDCDATA	-	-	-	-
BC10	**RSVD_GND[5]**	8307.32	8763.76	-	-	-	-	-
BC12	**GPIO_S0_SC[056]**	7316.72	8752.08	GPIO_S0_SC[056]	RESERVED	-	-	-
BC14	**GPIO_S0_SC[058]**	6326.12	8752.08	GPIO_S0_SC[058]	RESERVED	-	-	-
BC16	**GPIO_S0_SC[061]**	5335.52	8752.08	GPIO_S0_SC[061]	PCU_UART_RXD	-	-	-
BC18	**SD2_CMD**	4362.2	8752.08	GPIO_S0_SC[032]	SD2_CMD	-	-	-
BC20	**VSS**	3412.24	8752.08	-	-	-	-	-
BC22	**VSS**	2438.91	8752.08	-	-	-	-	-
BC24	**SD3_CD#**	1448.31	8752.08	GPIO_S0_SC[038]	SD3_CD#	-	-	-
BC26	**VSS**	474.98	8752.08	-	-	-	-	-
BC28	**VSS**	-474.98	8752.08	-	-	-	-	-
BC30	**LPE_I2S2_DATAOUT**	-1448.31	8752.08	GPIO_S0_SC[065]	LPE_I2S2_DATAOUT	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 41 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BC32	**VSS**	-2438.91	8752.08	-	-	-	-	-
BC34	**VSS**	-3412.24	8752.08	-	-	-	-	-
BC36	**DRAM1_DM[2]**	-4362.2	8752.08	-	-	-	-	-
BC38	**DRAM1_DQ[04]**	-5335.52	8752.08	-	-	-	-	-
BC40	**DRAM1_DQ[01]**	-6326.12	8752.08	-	-	-	-	-
BC42	**VSS**	-7316.72	8752.08	-	-	-	-	-
BC44	**DRAM1_DQ[07]**	-8307.32	8763.76	-	-	-	-	-
BC52	**DRAM1_MA[08]**	-12246.36	8852.15	-	-	-	-	-
BC53	**DRAM1_MA[05]**	-12814.05	8620.51	-	-	-	-	-
BD1	**VGA_V1P35_S3_F1**	12814.05	9293.61	-	-	-	-	-
BD2	**VGA_HSYNC**	12220.7	9444.99	VGA_HSYNC	-	-	-	-
BD5	**SD3_WP**	10565.13	9301.73	GPIO_S0_SC[007]	RESERVED	SD3_WP	-	-
BD7	**PCIE_CLKREQ[1]#**	9712.2	9301.73	GPIO_S0_SC[004]	PCIE_CLKREQ[1]#	-	-	-
BD10	**SATA_TXP[1]**	8307.32	9457.18	-	-	-	-	-
BD12	**GPIO_S0_SC[055]**	7316.72	9463.28	GPIO_S0_SC[055]	RESERVED	-	-	-
BD14	**GPIO_S0_SC[057]**	6326.12	9463.28	GPIO_S0_SC[057]	PCU_UART_TXD	-	-	-
BD16	**GPIO_S0_SC[060]**	5335.52	9463.28	GPIO_S0_SC[060]	RESERVED	-	-	-
BD18	**SD2_D[3]_CD#**	4362.2	9463.28	GPIO_S0_SC[031]	SD2_D[3]_CD#	-	-	-
BD19	**VSS**	3887.22	9107.68	-	-	-	-	-
BD20	**SD2_D[1]**	3412.24	9463.28	GPIO_S0_SC[029]	SD2_D[1]	-	-	-
BD22	**SD3_PWREN#**	2438.91	9463.28	GPIO_S0_SC[041]	SD3_PWREN#	-	-	-
BD24	**VSS**	1448.31	9463.28	-	-	-	-	-
BD26	**SD3_D[1]**	525.02	9404.35	GPIO_S0_SC[035]	SD3_D[1]	-	-	-
BD27	**VSS**	0	9107.68	-	-	-	-	-
BD28	**LPE_I2S2_DATAIN**	-525.02	9404.35	GPIO_S0_SC[064]	LPE_I2S2_DATAIN	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 42 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BD30	**VSS**	-1448.31	9463.28	-	-	-	-	-
BD32	**SIO_UART2_RTS#**	-2438.91	9463.28	GPIO_S0_SC[076]	SIO_UART2_RTS#	-	-	-
BD34	**SIO_UART2_TXD**	-3412.24	9463.28	GPIO_S0_SC[075]	SIO_UART2_TXD	-	-	-
BD35	**VSS**	-3887.22	9107.68	-	-	-	-	-
BD36	**DRAM1_DQ[05]**	-4362.2	9463.28	-	-	-	-	-
BD38	**DRAM1_DM[0]**	-5335.52	9463.28	-	-	-	-	-
BD40	**DRAM1_DQSN[0]**	-6326.12	9463.28	-	-	-	-	-
BD42	**DRAM1_DQ[03]**	-7316.72	9463.28	-	-	-	-	-
BD44	**DRAM1_CKE[2]**	-8307.32	9457.18	-	-	-	-	-
BD47	**DRAM1_MA[12]**	-9712.2	9301.73	-	-	-	-	-
BD49	**DRAM_VDD_S4**	-10565.13	9301.73	-	-	-	-	-
BD52	**DRAM_VDD_S4**	-12220.7	9444.99	-	-	-	-	-
BD53	**DRAM_VDD_S4**	-12814.05	9293.61	-	-	-	-	-
BE1	**VSS**	12814.05	9992.11	-	-	-	-	-
BE2	**VSS**	12222.48	10038.33	-	-	-	-	-
BE3	**PCIE_CLKREQ[3]#**	11642.85	9579.86	GPIO_S0_SC[006]	PCIE_CLKREQ[3]#	-	-	-
BE8	**VSS**	9320.02	9747	-	-	-	-	-
BE19	**VSS**	3887.22	9818.88	-	-	-	-	-
BE35	**VSS**	-3887.22	9818.88	-	-	-	-	-
BE46	**RESERVED**	-9320.02	9747	-	-	-	-	-
BE51	**DRAM1_MA[11]**	-11642.85	9579.86	-	-	-	-	-
BE52	**DRAM1_MA[09]**	-12222.48	10038.33	-	-	-	-	-
BE53	**VSS**	-12814.05	9992.11	-	-	-	-	-
BF2	**VGA_VSYNC**	12237.72	10631.68	VGA_VSYNC	-	-	-	-
BF4	**VSS**	11162.79	10162.79	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 43 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BF6	**SATA_TXP[0]**	10112.76	10238.49	-	-	-	-	-
BF10	**SATA_TXN[1]**	8307.32	10168.38	-	-	-	-	-
BF12	**VSS**	7316.72	10137.14	-	-	-	-	-
BF14	**GPIO_S0_SC[059]**	6326.12	10136.63	GPIO_S0_SC[059]	RESERVED	-	-	-
BF16	**VSS**	5335.52	10136.63	-	-	-	-	-
BF18	**LPC_RCOMP**	4388.36	10136.63	LPC_RCOMP	-	-	-	-
BF20	**HDA_LPE_RCOMP**	3386.07	10136.63	-	-	-	-	-
BF22	**SD3_1P8EN**	2438.91	10136.63	GPIO_S0_SC[040]	SD3_1P8EN	-	-	-
BF24	**VSS**	1448.31	10136.63	-	-	-	-	-
BF26	**SD3_RCOMP**	462.79	9994.65	-	-	-	-	-
BF27	**SIO_I2C4_DATA**	0	10365.99	GPIO_S0_SC[086]	SIO_I2C4_DATA	-	-	-
BF28	**LPE_I2S2_CLK**	-462.79	9994.65	GPIO_S0_SC[062]	LPE_I2S2_CLK	SATA_DEVSLP[1]	RESERVED	-
BF30	**VSS**	-1448.31	10136.63	-	-	-	-	-
BF32	**SIO_UART2_CTS#**	-2438.91	10136.63	GPIO_S0_SC[077]	SIO_UART2_CTS#	-	-	-
BF34	**SIO_UART2_RXD**	-3386.07	10136.63	GPIO_S0_SC[074]	SIO_UART2_RXD	-	-	-
BF36	**VSS**	-4388.36	10136.63	-	-	-	-	-
BF38	**VSS**	-5335.52	10136.63	-	-	-	-	-
BF40	**DRAM1_DQSP[0]**	-6326.12	10136.63	-	-	-	-	-
BF42	**DRAM1_DQ[06]**	-7316.72	10137.14	-	-	-	-	-
BF44	**DRAM_VDD_S4**	-8307.32	10168.38	-	-	-	-	-
BF48	**RESERVED**	-10112.76	10238.49	-	-	-	-	-
BF50	**DRAM1_MA[07]**	-11162.79	10162.79	-	-	-	-	-
BF52	**DRAM1_BS[2]**	-12237.72	10631.68	-	-	-	-	-
BG1	**VSS**	12814.05	10773.16	-	-	-	-	-
BG3	**PCIE_CLKREQ[0]#**	11644.38	10644.38	GPIO_S0_SC[003]	PCIE_CLKREQ[0]#	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 44 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BG5	**PCIE_CLKREQ[2]#**	10579.86	10642.85	GPIO_S0_SC[005]	PCIE_CLKREQ[2]#	-	-	-
BG7	**SATA_TXN[0]**	9553.19	10709.15	-	-	-	-	-
BG9	**PMC_RSTBTN#**	8697.98	11028.17	PMC_RSTBTN#	-	-	-	-
BG11	**PCU_SMB_ALERT#**	7774.43	11070.59	GPIO_S0_SC[053]	PCU_SMB_ALERT#	-	-	-
BG12	**PCU_SMB_DATA**	7288.53	10729.98	GPIO_S0_SC[051]	PCU_SMB_DATA	-	-	-
BG13	**ILB_LPC_SERIRQ**	6802.63	11070.59	GPIO_S0_SC[050]	ILB_LPC_SERIRQ	-	-	-
BG14	**ILB_LPC_AD[3]**	6316.73	10729.98	GPIO_S0_SC[045]	ILB_LPC_AD[3]	-	-	-
BG15	**ILB_LPC_CLK[0]**	5830.82	11070.59	GPIO_S0_SC[047]	ILB_LPC_CLK[0]	-	-	-
BG16	**ILB_LPC_CLKRUN#**	5344.92	10729.98	GPIO_S0_SC[049]	ILB_LPC_CLKRUN#	-	-	-
BG17	**ILB_LPC_FRAME#**	4859.02	11070.59	GPIO_S0_SC[046]	ILB_LPC_FRAME#	-	-	-
BG18	**GPIO_S0_SC[015]**	4373.12	10729.98	GPIO_S0_SC[015]	I2S1_DATAIN	RESERVED	-	-
BG19	**HDA_SDI[0]**	3887.22	11070.59	GPIO_S0_SC[012]	I2S1_CLK	HDA_SDI[0]	-	-
BG20	**HDA_SDO**	3401.31	10729.98	GPIO_S0_SC[011]	I2S0_DATAIN	HDA_SDO	-	-
BG21	**HDA_SDI[1]**	2915.41	11070.59	GPIO_S0_SC[013]	I2S1_FRM	HDA_SDI[1]	-	-
BG22	**HDA_RST#**	2429.51	10729.98	GPIO_S0_SC[008]	I2S0_CLK	HDA_RST#	-	-
BG23	**SIO_I2C0_CLK**	1943.61	11070.59	GPIO_S0_SC[079]	SIO_I2C0_CLK	-	-	-
BG24	**SIO_I2C1_DATA**	1457.71	10729.98	GPIO_S0_SC[080]	SIO_I2C1_DATA	-	-	-
BG25	**SIO_I2C2_DATA**	971.8	11070.59	GPIO_S0_SC[082]	SIO_I2C2_DATA	-	-	-
BG26	**SIO_I2C3_DATA**	479.81	10715.24	GPIO_S0_SC[084]	SIO_I2C3_DATA	-	-	-
BG27	**SIO_I2C4_CLK**	0	11070.59	GPIO_S0_SC[087]	SIO_I2C4_CLK	-	-	-
BG28	**SIO_I2C5_CLK**	-479.81	10715.24	GPIO_S0_SC[089]	SIO_I2C5_CLK	-	-	-
BG29	**SIO_I2C6_CLK**	-971.8	11070.59	GPIO_S0_SC[091]	SIO_I2C6_CLK	SD3_WP	-	-
BG30	**GPIO_S0_SC[093]**	-1457.71	10729.98	RESERVED	GPIO_S0_SC[093]	-	-	-
BG31	**VSS**	-1943.61	11070.59	-	-	-	-	-
BG32	**DRAM1_DQ[09]**	-2429.51	10729.98	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 45 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BG33	**DRAM1_DQ[12]**	-2915.41	11070.59	-	-	-	-	-
BG34	**VSS**	-3401.31	10729.98	-	-	-	-	-
BG35	**DRAM1_DQSP[1]**	-3887.22	11070.59	-	-	-	-	-
BG36	**DRAM1_DQ[10]**	-4373.12	10729.98	-	-	-	-	-
BG37	**DRAM1_DQ[14]**	-4859.02	11070.59	-	-	-	-	-
BG38	**DRAM1_DQ[00]**	-5344.92	10729.98	-	-	-	-	-
BG39	**VSS**	-5830.82	11070.59	-	-	-	-	-
BG40	**DRAM1_DQ[28]**	-6316.73	10729.98	-	-	-	-	-
BG41	**DRAM1_DQ[25]**	-6802.63	11070.59	-	-	-	-	-
BG42	**VSS**	-7288.53	10729.98	-	-	-	-	-
BG43	**DRAM1_DQSN[3]**	-7774.43	11070.59	-	-	-	-	-
BG45	**VSS**	-8697.98	11028.17	-	-	-	-	-
BG47	**DRAM1_CKE[0]**	-9553.19	10709.15	-	-	-	-	-
BG49	**VSS**	-10579.86	10642.85	-	-	-	-	-
BG51	**DRAM_VDD_S4**	-11644.38	10644.38	-	-	-	-	-
BG53	**VSS**	-12814.05	10773.16	-	-	-	-	-
BH1	**VSS**	12814.05	11382.76	-	-	-	-	-
BH2	**VSS**	12225.02	11225.02	-	-	-	-	-
BH4	**PMC_PLT_CLK[2]**	11631.68	11237.72	GPIO_S0_SC[098]	PMC_PLT_CLK[2]	-	-	-
BH5	**PMC_PLT_CLK[1]**	11038.33	11222.48	GPIO_S0_SC[097]	PMC_PLT_CLK[1]	-	-	-
BH6	**PMC_PLT_CLK[4]**	10444.99	11220.7	GPIO_S0_SC[100]	PMC_PLT_CLK[4]	-	-	-
BH7	**PMC_PLT_CLK[0]**	9851.64	11229.59	GPIO_S0_SC[096]	PMC_PLT_CLK[0]	-	-	-
BH8	**PMC_PLT_CLK[3]**	9258.3	11224.26	GPIO_S0_SC[099]	PMC_PLT_CLK[3]	-	-	-
BH10	**PCU_SMB_CLK**	8260.33	11428.98	GPIO_S0_SC[052]	PCU_SMB_CLK	-	-	-
BH12	**ILB_8254_SPKR**	7288.53	11428.98	GPIO_S0_SC[054]	ILB_8254_SPKR	RESERVED	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 46 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BH14	**ILB_LPC_CLK[1]**	6316.73	11428.98	GPIO_S0_SC[048]	ILB_LPC_CLK[1]	-	-	-
BH16	**ILB_LPC_AD[0]**	5344.92	11428.98	GPIO_S0_SC[042]	ILB_LPC_AD[0]	-	-	-
BH18	**GPIO_S0_SC[014]**	4373.12	11428.98	GPIO_S0_SC[014]	I2S1_DATAOUT	RESERVED	-	-
BH20	**HDA_SYNC**	3401.31	11428.98	GPIO_S0_SC[009]	I2S0_FRM	HDA_SYNC	-	-
BH22	**SIO_I2C0_DATA**	2429.51	11428.98	GPIO_S0_SC[078]	SIO_I2C0_DATA	-	-	-
BH24	**SIO_I2C1_CLK**	1457.71	11428.98	GPIO_S0_SC[081]	SIO_I2C1_CLK	RESERVED	-	-
BH26	**SIO_I2C3_CLK**	485.9	11428.98	GPIO_S0_SC[085]	SIO_I2C3_CLK	-	-	-
BH28	**SIO_I2C5_DATA**	-485.9	11428.98	GPIO_S0_SC[088]	SIO_I2C5_DATA	-	-	-
BH30	**GPIO_S0_SC[092]**	-1457.71	11428.98	RESERVED	GPIO_S0_SC[092]	-	-	-
BH32	**DRAM1_DQ[08]**	-2429.51	11428.98	-	-	-	-	-
BH34	**DRAM1_DQSN[1]**	-3401.31	11428.98	-	-	-	-	-
BH36	**DRAM1_DM[1]**	-4373.12	11428.98	-	-	-	-	-
BH38	**DRAM1_DQ[15]**	-5344.92	11428.98	-	-	-	-	-
BH40	**DRAM1_DQ[29]**	-6316.73	11428.98	-	-	-	-	-
BH42	**DRAM1_DM[3]**	-7288.53	11428.98	-	-	-	-	-
BH44	**DRAM1_DQSP[3]**	-8260.33	11428.98	-	-	-	-	-
BH46	**DRAM1_DQ[27]**	-9258.3	11224.26	-	-	-	-	-
BH47	**DRAM1_DQ[31]**	-9851.64	11229.59	-	-	-	-	-
BH48	**DRAM1_DQ[30]**	-10444.99	11220.7	-	-	-	-	-
BH49	**DRAM1_MA[14]**	-11038.33	11222.48	-	-	-	-	-
BH50	**DRAM1_MA[15]**	-11631.68	11237.72	-	-	-	-	-
BH52	**VSS**	-12225.02	11225.02	-	-	-	-	-
BH53	**VSS**	-12814.05	11382.76	-	-	-	-	-
BJ2	**VSS**	12382.75	11814.05	-	-	-	-	-
BJ3	**VSS**	11773.15	11814.05	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 47 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BJ5	**VSS**	10992.1	11814.05	-	-	-	-	-
BJ6	**VGA_V1P0_S3**	10293.6	11814.05	-	-	-	-	-
BJ7	**VSS**	9620.5	11814.05	-	-	-	-	-
BJ9	**PMC_PLT_CLK[5]**	8746.24	11814.05	GPIO_S0_SC[101]	PMC_PLT_CLK[5]	-	-	-
BJ11	**VSS**	7774.43	11814.05	-	-	-	-	-
BJ13	**ILB_LPC_AD[2]**	6802.63	11814.05	GPIO_S0_SC[044]	ILB_LPC_AD[2]	-	-	-
BJ15	**VSS**	5830.82	11814.05	-	-	-	-	-
BJ17	**ILB_LPC_AD[1]**	4859.02	11814.05	GPIO_S0_SC[043]	ILB_LPC_AD[1]	-	-	-
BJ19	**VSS**	3887.22	11814.05	-	-	-	-	-
BJ21	**HDA_CLK**	2915.41	11814.05	GPIO_S0_SC[010]	I2S0_DATAOUT	HDA_CLK	-	-
BJ23	**VSS**	1943.61	11814.05	-	-	-	-	-
BJ25	**SIO_I2C2_CLK**	971.8	11814.05	GPIO_S0_SC[083]	SIO_I2C2_CLK	-	-	-
BJ27	**VSS**	0	11814.05	-	-	-	-	-
BJ29	**SIO_I2C6_DATA**	-971.8	11814.05	GPIO_S0_SC[090]	SIO_I2C6_DATA	ILB_NMI	-	-
BJ31	**VSS**	-1943.61	11814.05	-	-	-	-	-
BJ33	**DRAM1_DQ[13]**	-2915.41	11814.05	-	-	-	-	-
BJ35	**VSS**	-3887.22	11814.05	-	-	-	-	-
BJ37	**DRAM1_DQ[11]**	-4859.02	11814.05	-	-	-	-	-
BJ39	**VSS**	-5830.82	11814.05	-	-	-	-	-
BJ41	**DRAM1_DQ[24]**	-6802.63	11814.05	-	-	-	-	-
BJ43	**VSS**	-7774.43	11814.05	-	-	-	-	-
BJ45	**DRAM1_DQ[26]**	-8746.24	11814.05	-	-	-	-	-
BJ47	**VSS**	-9620.5	11814.05	-	-	-	-	-
BJ48	**DRAM_VDD_S4**	-10293.6	11814.05	-	-	-	-	-

Table 149. Ball Listing by Location with GPIO Muxed Functions (Sheet 48 of 48)

Location	Ball Name	X-Location	Y-Location	GPIO F0	GPIO F1	GPIO F2	GPIO F3	GPIO F6
BJ49	**VSS**	-10992.1	11814.05	-	-	-	-	-
BJ51	**VSS**	-11773.15	11814.05	-	-	-	-	-
BJ52	**VSS**	-12382.75	11814.05	-	-	-	-	-

10.4 Alphabetical Ball Name List

Ball Name	Location
CORE_V1P05_S3	U33
CORE_V1P05_S3	U35
CORE_V1P05_S3	V33
CORE_V1P05_S3	Y32
CORE_V1P05_S3	AA33
CORE_V1P05_S3	AC32
CORE_V1P05_S3	AF33
CORE_V1P05_S3	AG33
CORE_V1P05_S3	AG35
CORE_VCC_S3	P26
CORE_VCC_S3	P27
CORE_VCC_S3	U27
CORE_VCC_S3	U29
CORE_VCC_S3	V27
CORE_VCC_S3	V29
CORE_VCC_S3	V30
CORE_VCC_S3	Y27
CORE_VCC_S3	Y29
CORE_VCC_S3	Y30
CORE_VCC_S3	AA27
CORE_VCC_S3	AA29
CORE_VCC_S3	AA30
CORE_VCC_S3	AC27
CORE_VCC_S3	AC29
CORE_VCC_S3	AC30
CORE_VCC_S3	AD27
CORE_VCC_S3	AD29
CORE_VCC_S3	AD30
CORE_VCC_S3	AF27
CORE_VCC_S3	AF29
CORE_VCC_S3	AG27
CORE_VCC_S3	AG29
CORE_VCC_S3	AG30
CORE_VCC_SENSE	P28
CORE_VSS_SENSE	N28
DDI0_AUXN	AL1
DDI0_AUXP	AL3
DDI0_BKLTCTL	B26
DDI0_BKLTEN	C27
DDI0_DDCCLK	C28
DDI0_DDCDATA	C26
DDI0_HPD	D27

Ball Name	Location
DDI0_TXN[0]	AV2
DDI0_TXN[1]	AT3
DDI0_TXN[2]	AR1
DDI0_TXN[3]	AP2
DDI0_TXP[0]	AV3
DDI0_TXP[1]	AT2
DDI0_TXP[2]	AR3
DDI0_TXP[3]	AP3
DDI0_VDDEN	B28
DDI1_AUXN	AK2
DDI1_AUXP	AK3
DDI1_BKLTCTL	M30
DDI1_BKLTEN	J30
DDI1_DDCCLK	G30
DDI1_DDCDATA	P30
DDI1_HPD	K30
DDI1_TXN[0]	AG1
DDI1_TXN[1]	AF2
DDI1_TXN[2]	AD2
DDI1_TXN[3]	AC1
DDI1_TXP[0]	AG3
DDI1_TXP[1]	AF3
DDI1_TXP[2]	AD3
DDI1_TXP[3]	AC3
DDI1_VDDEN	N30
DDI_RCOMP_N	AK13
DDI_RCOMP_P	AK12
DDI_V1P0_S3	AJ18
DDI_V1P0_S3	AK19
DDI_V1P0_S3	AK21
DDI_V1P0_S3	AM16
DRAM0_BS[0]	K47
DRAM0_BS[1]	K44
DRAM0_BS[2]	D52
DRAM0_CAS#	M44
DRAM0_CKE[0]	C47
DRAM0_CKE[2]	F44
DRAM0_CKN[0]	M48
DRAM0_CKN[2]	P48
DRAM0_CKP[0]	M50
DRAM0_CKP[2]	P50
DRAM0_CS[0]#	P44

Ball Name	Location
DRAM0_CS[2]#	P45
DRAM0_DM[0]	G36
DRAM0_DM[1]	B36
DRAM0_DM[2]	F38
DRAM0_DM[3]	B42
DRAM0_DM[4]	P51
DRAM0_DM[5]	V42
DRAM0_DM[6]	Y50
DRAM0_DM[7]	Y52
DRAM0_DQ[00]	M36
DRAM0_DQ[01]	J36
DRAM0_DQ[02]	P40
DRAM0_DQ[03]	M40
DRAM0_DQ[04]	P36
DRAM0_DQ[05]	N36
DRAM0_DQ[06]	K40
DRAM0_DQ[07]	K42
DRAM0_DQ[08]	B32
DRAM0_DQ[09]	C32
DRAM0_DQ[10]	C36
DRAM0_DQ[11]	A37
DRAM0_DQ[12]	C33
DRAM0_DQ[13]	A33
DRAM0_DQ[14]	C37
DRAM0_DQ[15]	B38
DRAM0_DQ[16]	F36
DRAM0_DQ[17]	G38
DRAM0_DQ[18]	F42
DRAM0_DQ[19]	J42
DRAM0_DQ[20]	G40
DRAM0_DQ[21]	C38
DRAM0_DQ[22]	G44
DRAM0_DQ[23]	D42
DRAM0_DQ[24]	A41
DRAM0_DQ[25]	C41
DRAM0_DQ[26]	A45
DRAM0_DQ[27]	B46
DRAM0_DQ[28]	C40
DRAM0_DQ[29]	B40
DRAM0_DQ[30]	B48
DRAM0_DQ[31]	B47
DRAM0_DQ[32]	K52

Ball Name	Location
DRAM0_DQ[33]	K51
DRAM0_DQ[34]	T52
DRAM0_DQ[35]	T51
DRAM0_DQ[36]	L51
DRAM0_DQ[37]	L53
DRAM0_DQ[38]	R51
DRAM0_DQ[39]	R53
DRAM0_DQ[40]	T47
DRAM0_DQ[41]	T45
DRAM0_DQ[42]	Y40
DRAM0_DQ[43]	V41
DRAM0_DQ[44]	T48
DRAM0_DQ[45]	T50
DRAM0_DQ[46]	Y42
DRAM0_DQ[47]	AB40
DRAM0_DQ[48]	V45
DRAM0_DQ[49]	V47
DRAM0_DQ[50]	AD48
DRAM0_DQ[51]	AD50
DRAM0_DQ[52]	V48
DRAM0_DQ[53]	V50
DRAM0_DQ[54]	AB44
DRAM0_DQ[55]	Y45
DRAM0_DQ[56]	V52
DRAM0_DQ[57]	W51
DRAM0_DQ[58]	AC53
DRAM0_DQ[59]	AC51
DRAM0_DQ[60]	W53
DRAM0_DQ[61]	Y51
DRAM0_DQ[62]	AD52
DRAM0_DQ[63]	AD51
DRAM0_DQSN[0]	K38
DRAM0_DQSN[1]	B34
DRAM0_DQSN[2]	F40
DRAM0_DQSN[3]	C43
DRAM0_DQSN[4]	M52
DRAM0_DQSN[5]	T44
DRAM0_DQSN[6]	Y48
DRAM0_DQSN[7]	AA51
DRAM0_DQSP[0]	J38
DRAM0_DQSP[1]	C35
DRAM0_DQSP[2]	D40
DRAM0_DQSP[3]	B44
DRAM0_DQSP[4]	N53

Ball Name	Location
DRAM0_DQSP[5]	T42
DRAM0_DQSP[6]	Y47
DRAM0_DQSP[7]	AB52
DRAM0_DRAMRST#	P41
DRAM0_MA[00]	K45
DRAM0_MA[01]	H47
DRAM0_MA[02]	L41
DRAM0_MA[03]	H44
DRAM0_MA[04]	H50
DRAM0_MA[05]	G53
DRAM0_MA[06]	H49
DRAM0_MA[07]	D50
DRAM0_MA[08]	G52
DRAM0_MA[09]	E52
DRAM0_MA[10]	K48
DRAM0_MA[11]	E51
DRAM0_MA[12]	F47
DRAM0_MA[13]	J51
DRAM0_MA[14]	B49
DRAM0_MA[15]	B50
DRAM0_ODT[0]	T41
DRAM0_ODT[2]	P42
DRAM0_RAS#	M45
DRAM0_WE#	H51
DRAM1_BS[0]	AY47
DRAM1_BS[1]	AY44
DRAM1_BS[2]	BF52
DRAM1_CAS#	AV44
DRAM1_CKE[0]	BG47
DRAM1_CKE[2]	BD44
DRAM1_CKN[0]	AV48
DRAM1_CKN[2]	AT48
DRAM1_CKP[0]	AV50
DRAM1_CKP[2]	AT50
DRAM1_CS[0]#	AT44
DRAM1_CS[2]#	AT45
DRAM1_DM[0]	BD38
DRAM1_DM[1]	BH36
DRAM1_DM[2]	BC36
DRAM1_DM[3]	BH42
DRAM1_DM[4]	AT51
DRAM1_DM[5]	AM42
DRAM1_DM[6]	AK50
DRAM1_DM[7]	AK52

Ball Name	Location
DRAM1_DQ[00]	BG38
DRAM1_DQ[01]	BC40
DRAM1_DQ[02]	BA42
DRAM1_DQ[03]	BD42
DRAM1_DQ[04]	BC38
DRAM1_DQ[05]	BD36
DRAM1_DQ[06]	BF42
DRAM1_DQ[07]	BC44
DRAM1_DQ[08]	BH32
DRAM1_DQ[09]	BG32
DRAM1_DQ[10]	BG36
DRAM1_DQ[11]	BJ37
DRAM1_DQ[12]	BG33
DRAM1_DQ[13]	BJ33
DRAM1_DQ[14]	BG37
DRAM1_DQ[15]	BH38
DRAM1_DQ[16]	AU36
DRAM1_DQ[17]	AT36
DRAM1_DQ[18]	AV40
DRAM1_DQ[19]	AT40
DRAM1_DQ[20]	BA36
DRAM1_DQ[21]	AV36
DRAM1_DQ[22]	AY42
DRAM1_DQ[23]	AY40
DRAM1_DQ[24]	BJ41
DRAM1_DQ[25]	BG41
DRAM1_DQ[26]	BJ45
DRAM1_DQ[27]	BH46
DRAM1_DQ[28]	BG40
DRAM1_DQ[29]	BH40
DRAM1_DQ[30]	BH48
DRAM1_DQ[31]	BH47
DRAM1_DQ[32]	AY52
DRAM1_DQ[33]	AY51
DRAM1_DQ[34]	AP52
DRAM1_DQ[35]	AP51
DRAM1_DQ[36]	AW51
DRAM1_DQ[37]	AW53
DRAM1_DQ[38]	AR51
DRAM1_DQ[39]	AR53
DRAM1_DQ[40]	AP47
DRAM1_DQ[41]	AP45
DRAM1_DQ[42]	AK40
DRAM1_DQ[43]	AM41

Ball Name	Location
DRAM1_DQ[44]	AP48
DRAM1_DQ[45]	AP50
DRAM1_DQ[46]	AK42
DRAM1_DQ[47]	AH40
DRAM1_DQ[48]	AM45
DRAM1_DQ[49]	AM47
DRAM1_DQ[50]	AF48
DRAM1_DQ[51]	AF50
DRAM1_DQ[52]	AM48
DRAM1_DQ[53]	AM50
DRAM1_DQ[54]	AH44
DRAM1_DQ[55]	AK45
DRAM1_DQ[56]	AM52
DRAM1_DQ[57]	AL51
DRAM1_DQ[58]	AG53
DRAM1_DQ[59]	AG51
DRAM1_DQ[60]	AL53
DRAM1_DQ[61]	AK51
DRAM1_DQ[62]	AF52
DRAM1_DQ[63]	AF51
DRAM1_DQSN[0]	BD40
DRAM1_DQSN[1]	BH34
DRAM1_DQSN[2]	AY38
DRAM1_DQSN[3]	BG43
DRAM1_DQSN[4]	AV52
DRAM1_DQSN[5]	AP44
DRAM1_DQSN[6]	AK48
DRAM1_DQSN[7]	AJ51
DRAM1_DQSP[0]	BF40
DRAM1_DQSP[1]	BG35
DRAM1_DQSP[2]	BA38
DRAM1_DQSP[3]	BH44
DRAM1_DQSP[4]	AU53
DRAM1_DQSP[5]	AP42
DRAM1_DQSP[6]	AK47
DRAM1_DQSP[7]	AH52
DRAM1_DRAMRST#	AT41
DRAM1_MA[00]	AY45
DRAM1_MA[01]	BB47
DRAM1_MA[02]	AW41
DRAM1_MA[03]	BB44
DRAM1_MA[04]	BB50
DRAM1_MA[05]	BC53
DRAM1_MA[06]	BB49

Ball Name	Location
DRAM1_MA[07]	BF50
DRAM1_MA[08]	BC52
DRAM1_MA[09]	BE52
DRAM1_MA[10]	AY48
DRAM1_MA[11]	BE51
DRAM1_MA[12]	BD47
DRAM1_MA[13]	BA51
DRAM1_MA[14]	BH49
DRAM1_MA[15]	BH50
DRAM1_ODT[0]	AP41
DRAM1_ODT[2]	AT42
DRAM1_RAS#	AV45
DRAM1_WE#	BB51
DRAM_CORE_PWROK	AB42
DRAM_RCOMP[0]	AD44
DRAM_RCOMP[1]	AF45
DRAM_RCOMP[2]	AD45
DRAM_V1P0_S3	Y35
DRAM_V1P0_S3	Y36
DRAM_V1P0_S3	AA36
DRAM_V1P0_S3	AD35
DRAM_V1P0_S3	AF35
DRAM_V1P0_S3	AF36
DRAM_V1P0_S3	AJ36
DRAM_V1P0_S3	AK35
DRAM_V1P0_S3	AK36
DRAM_V1P35_S3_F1	AD36
DRAM_VDD_S4	A48
DRAM_VDD_S4	C51
DRAM_VDD_S4	D44
DRAM_VDD_S4	F49
DRAM_VDD_S4	F52
DRAM_VDD_S4	F53
DRAM_VDD_S4	H46
DRAM_VDD_S4	M41
DRAM_VDD_S4	M42
DRAM_VDD_S4	V38
DRAM_VDD_S4	Y38
DRAM_VDD_S4	AD38
DRAM_VDD_S4	AF38
DRAM_VDD_S4	AK38
DRAM_VDD_S4	AM38
DRAM_VDD_S4	AV41
DRAM_VDD_S4	AV42

Ball Name	Location
DRAM_VDD_S4	BB46
DRAM_VDD_S4	BD49
DRAM_VDD_S4	BD52
DRAM_VDD_S4	BD53
DRAM_VDD_S4	BF44
DRAM_VDD_S4	BG51
DRAM_VDD_S4	BJ48
DRAM_VDD_S4_PWROK	AD42
DRAM_VREF	AF44
GPIO_RCOMP	N26
RESERVED	B30
GPIO_S0_SC[014]	BH18
GPIO_S0_SC[015]	BG18
GPIO_S0_SC[055]	BD12
GPIO_S0_SC[056]	BC12
GPIO_S0_SC[057]	BD14
GPIO_S0_SC[058]	BC14
GPIO_S0_SC[059]	BF14
GPIO_S0_SC[060]	BD16
GPIO_S0_SC[061]	BC16
GPIO_S0_SC[092]	BH30
GPIO_S0_SC[093]	BG30
GPIO_S5[00]	B18
GPIO_S5[01]	B16
GPIO_S5[02]	C18
GPIO_S5[03]	A17
GPIO_S5[04]	C17
GPIO_S5[05]	C16
GPIO_S5[06]	B14
GPIO_S5[07]	C15
GPIO_S5[08]	C13
GPIO_S5[09]	A13
GPIO_S5[10]	C19
GPIO_S5[13]	F18
GPIO_S5[17]	J24
GPIO_S5[22]	K24
GPIO_S5[23]	N24
GPIO_S5[24]	M20
GPIO_S5[25]	J18
GPIO_S5[26]	M18
GPIO_S5[27]	K18
GPIO_S5[28]	K20
GPIO_S5[29]	M22
GPIO_S5[30]	M24

Ball Name	Location
GPIO_V1P0_S3	AN25
HDA_CLK	BJ21
HDA_LPE_RCOMP	BF20
HDA_LPE_V1P5V1P8_S3	AM32
HDA_RST#	BG22
HDA_SDI[0]	BG19
HDA_SDI[1]	BG21
HDA_SDO	BG20
HDA_SYNC	BH20
ICLK_DRAM_TERM[0]	AF42
ICLK_DRAM_TERM[1]	AH42
ICLK_ICOMP	AD14
ICLK_OSCIN	AH12
ICLK_OSCOUT	AH10
ICLK_RCOMP	AD13
ICLK_USB_TERM[0]	F10
ICLK_USB_TERM[1]	D10
ICLK_V1P35_S3_F1	AJ19
ICLK_V1P35_S3_F2	AG18
ILB_8254_SPKR	BH12
ILB_LPC_AD[0]	BH16
ILB_LPC_AD[1]	BJ17
ILB_LPC_AD[2]	BJ13
ILB_LPC_AD[3]	BG14
ILB_LPC_CLK[0]	BG15
ILB_LPC_CLK[1]	BH14
ILB_LPC_CLKRUN#	BG16
ILB_LPC_FRAME#	BG17
ILB_LPC_SERIRQ	BG13
ILB_RTC_EXTPAD	B8
ILB_RTC_RST#	C12
ILB_RTC_TEST#	C11
ILB_RTC_X1	C9
ILB_RTC_X2	A9
LPC_RCOMP	BF18
LPC_V1P8V3P3_S3	AM27
LPE_I2S2_CLK	BF28
LPE_I2S2_DATAIN	BD28
LPE_I2S2_DATAOUT	BC30
LPE_I2S2_FRM	BA30
MCSI1_CLKN	T7
MCSI1_CLKP	T9
MCSI1_DN[0]	AB13
MCSI1_DN[1]	Y12

Ball Name	Location
MCSI1_DN[2]	V10
MCSI1_DN[3]	T12
MCSI1_DP[0]	AB12
MCSI1_DP[1]	Y13
MCSI1_DP[2]	V9
MCSI1_DP[3]	T10
MCSI2_CLKN	V14
MCSI2_CLKP	V13
MCSI2_DN[0]	T14
MCSI2_DP[0]	T13
MCSI3_CLKN	T6
MCSI3_CLKP	T4
MCSI_GPIO[00]	F34
MCSI_GPIO[01]	M32
MCSI_GPIO[02]	D28
MCSI_GPIO[03]	J28
MCSI_GPIO[04]	K34
MCSI_GPIO[05]	D34
MCSI_GPIO[06]	F32
MCSI_GPIO[07]	F28
MCSI_GPIO[08]	K28
MCSI_GPIO[09]	J34
MCSI_GPIO[10]	N32
MCSI_GPIO[11]	D32
MCSI_RCOMP	P14
MIPI_V1P8_S3	U38
MIPI_V1P24_S3	AD16
MIPI_V1P24_S3	AD18
MMC1_CLK	AT22
MMC1_CMD	AV26
MMC1_D[0]	AV20
MMC1_D[1]	AU22
MMC1_D[2]	AV22
MMC1_D[3]	AT20
MMC1_D[4]	AY24
MMC1_D[5]	AU26
MMC1_D[6]	AT26
MMC1_D[7]	AU20
MMC1_RCOMP	AY18
MMC1_RST#	BA24
PCIE_CLKN[0]	AF6
PCIE_CLKN[1]	AF9
PCIE_CLKN[2]	AK4
PCIE_CLKN[3]	AM4

Ball Name	Location
PCIE_CLKP[0]	AF4
PCIE_CLKP[1]	AF7
PCIE_CLKP[2]	AK6
PCIE_CLKP[3]	AM6
PCIE_CLKREQ[0]#	BG3
PCIE_CLKREQ[1]#	BD7
PCIE_CLKREQ[2]#	BG5
PCIE_CLKREQ[3]#	BE3
PCIE_RCOMP_N	AP13
PCIE_RCOMP_P	AP14
PCIE_RXN[0]	AT13
PCIE_RXN[1]	AT9
PCIE_RXN[2]	AP10
PCIE_RXN[3]	AP7
PCIE_RXP[0]	AT14
PCIE_RXP[1]	AT10
PCIE_RXP[2]	AP12
PCIE_RXP[3]	AP9
PCIE_SATA_V1P0_S3	AN18
PCIE_TXN[0]	AY6
PCIE_TXN[1]	AV4
PCIE_TXN[2]	AT6
PCIE_TXN[3]	AP4
PCIE_TXP[0]	AY7
PCIE_TXP[1]	AV6
PCIE_TXP[2]	AT7
PCIE_TXP[3]	AP6
PCIE_V1P0_S3	AK18
PCIE_V1P0_S3	AM18
PCIE_V1P0_S3	AM21
PCIE_V1P0_S3	AN21
PCU_SMB_ALERT#	BG11
PCU_SMB_CLK	BH10
PCU_SMB_DATA	BG12
PCU_SPI_CLK	C22
PCU_SPI_CS[0]#	C23
PCU_SPI_CS[1]#	C21
PCU_SPI_MISO	B22
PCU_SPI_MOSI	A21
PCU_V1P8_G3	V25
PCU_V3P3_G3	N22
PMC_ACPRESENT	D20
PMC_BATLOW#	K26
PMC_CORE_PWROK	B7

Ball Name	Location
PMC_PLT_CLK[0]	BH7
PMC_PLT_CLK[1]	BH5
PMC_PLT_CLK[2]	BH4
PMC_PLT_CLK[3]	BH8
PMC_PLT_CLK[4]	BH6
PMC_PLT_CLK[5]	BJ9
PMC_PLTRST#	F20
PMC_PWRBTN#	J26
PMC_RSMRST#	B10
PMC_RSTBTN#	BG9
PMC_SLP_S3#	D22
PMC_SLP_S4#	F22
PMC_SUS_STAT#	G18
PMC_SUSCLK[0]	G24
PMC_SUSPWRDNACK	D26
PMC_V1P8_G3	U25
PMC_WAKE_PCIE[0]#	F26
PROCHOT#	C24
RESERVED	A29
RESERVED	C29
RESERVED	C30
RESERVED	D48
RESERVED	E46
RESERVED	F1
RESERVED	H4
RESERVED	H5
RESERVED	H7
RESERVED	H8
RESERVED	M9
RESERVED	M10
RESERVED	N34
RESERVED	P6
RESERVED	P7
RESERVED	P34
RESERVED	R1
RESERVED	R3
RESERVED	T2
RESERVED	T3
RESERVED	V2
RESERVED	V3
RESERVED	V4
RESERVED	V6
RESERVED	W1
RESERVED	W3
RESERVED	Y2
RESERVED	Y3
RESERVED	Y4
RESERVED	Y6
RESERVED	AB2
RESERVED	AB3
RESERVED	AB7
RESERVED	AB9
RESERVED	AB14
RESERVED	AD4
RESERVED	AD6
RESERVED	AD9
RESERVED	AD10
RESERVED	AD12
RESERVED	AD40
RESERVED	AD41
RESERVED	AF13
RESERVED	AF14
RESERVED	AF40
RESERVED	AF41
RESERVED	AH13
RESERVED	AH14
RESERVED	AK7
RESERVED	AK9
RESERVED	AM9
RESERVED	AM10
RESERVED	AM13
RESERVED	AM14
RESERVED	AT34
RESERVED	AV9
RESERVED	AV10
RESERVED	BB3
RESERVED	BB4
RESERVED	BE46
RESERVED	BF48
RSVD_GND[0]	AM3
RSVD_GND[1]	AM2
RSVD_GND[2]	AH3
RSVD_GND[3]	AH2
RSVD_GND[4]	BB10
RSVD_GND[5]	BC10
RSVD_GND[6]	BB5
RSVD_GND[7]	BB7
RTC_VCC	P22
SATA_GP[0]	BA12
SATA_GP[1]	AY14
SATA_LED#	AY12
SATA_RCOMP_N	AT18
SATA_RCOMP_P	AU18
SATA_RXN[0]	AV16
SATA_RXN[1]	BA16
SATA_RXP[0]	AU16
SATA_RXP[1]	AY16
SATA_TXN[0]	BG7
SATA_TXN[1]	BF10
SATA_TXP[0]	BF6
SATA_TXP[1]	BD10
SATA_V1P0_S3	AN19
SD2_CLK	BA18
SD2_CMD	BC18
SD2_D[0]	AY20
SD2_D[1]	BD20
SD2_D[2]	BA20
SD2_D[3]_CD#	BD18
SD3_1P8EN	BF22
SD3_CD#	BC24
SD3_CLK	AY26
SD3_CMD	AV28
SD3_D[0]	AT28
SD3_D[1]	BD26
SD3_D[2]	AU28
SD3_D[3]	BA26
SD3_PWREN#	BD22
SD3_RCOMP	BF26
SD3_V1P8V3P3_S3	AN27
SD3_WP	BD5
SIO_I2C0_CLK	BG23
SIO_I2C0_DATA	BH22
SIO_I2C1_CLK	BH24
SIO_I2C1_DATA	BG24
SIO_I2C2_CLK	BJ25
SIO_I2C2_DATA	BG25
SIO_I2C3_CLK	BH26
SIO_I2C3_DATA	BG26
SIO_I2C4_CLK	BG27
SIO_I2C4_DATA	BF27
SIO_I2C5_CLK	BG28
SIO_I2C5_DATA	BH28

Ball Name	Location
SIO_I2C6_CLK	BG29
SIO_I2C6_DATA	BJ29
SIO_PWM[0]	AU32
SIO_PWM[1]	AT32
SIO_SPI_CLK	AY30
SIO_SPI_CS#	AV32
SIO_SPI_MISO	BA28
SIO_SPI_MOSI	AY28
SIO_UART1_CTS#	AY34
SIO_UART1_RTS#	BA34
SIO_UART1_RXD	AU34
SIO_UART1_TXD	AV34
SIO_UART2_CTS#	BF32
SIO_UART2_RTS#	BD32
SIO_UART2_RXD	BF34
SIO_UART2_TXD	BD34
SVID_ALERT#	B24
SVID_CLK	C25
SVID_DATA	A25
SVID_V1P0_S3	V32
TAP_PRDY#	D18
TAP_PREQ#	F16
TAP_TCK	D14
TAP_TDI	F12
TAP_TDO	G16
TAP_TMS	F14
TAP_TRST#	G12
TP2_CORE_VCC_S3	AA22
TP_CORE_V1P05_S4	AF30
UNCORE_V1P0_G3	B6
UNCORE_V1P0_G3	C5
UNCORE_V1P0_G3	U22
UNCORE_V1P0_G3	V22
UNCORE_V1P0_S3	V24
UNCORE_V1P0_S3	Y22
UNCORE_V1P0_S3	Y24
UNCORE_V1P0_S3	AF16
UNCORE_V1P0_S3	AF18
UNCORE_V1P0_S3	AF21
UNCORE_V1P0_S3	AG21
UNCORE_V1P0_S3	AN29
UNCORE_V1P0_S3	AN30
UNCORE_V1P8_G3	U24
UNCORE_V1P8_S3	AM30

Ball Name	Location
UNCORE_V1P8_S3	AN32
UNCORE_V1P35_S3_F1	AG19
UNCORE_V1P35_S3_F2	AG32
UNCORE_V1P35_S3_F3	V36
UNCORE_V1P35_S3_F4	U36
UNCORE_V1P35_S3_F5	AA25
UNCORE_V1P35_S3_F6	AF19
UNCORE_VNN_S3	AA24
UNCORE_VNN_S3	AC22
UNCORE_VNN_S3	AC24
UNCORE_VNN_S3	AD22
UNCORE_VNN_S3	AD24
UNCORE_VNN_S3	AF22
UNCORE_VNN_S3	AF24
UNCORE_VNN_S3	AG22
UNCORE_VNN_S3	AG24
UNCORE_VNN_S3	AJ22
UNCORE_VNN_S3	AJ24
UNCORE_VNN_S3	AK22
UNCORE_VNN_S3	AK24
UNCORE_VNN_S3	AK25
UNCORE_VNN_S3	AK27
UNCORE_VNN_S3	AK29
UNCORE_VNN_S3	AK30
UNCORE_VNN_S3	AK32
UNCORE_VNN_S3	AM22
UNCORE_VNN_SENSE	BB8
USB3_REXT[0]	M12
USB3_RXN[0]	E3
USB3_RXP[0]	D4
USB3_TXN[0]	K7
USB3_TXP[0]	K6
USB3_V1P0_G3	C3
USB3_V1P0_G3	Y19
USB_DN[0]	K16
USB_DN[1]	G14
USB_DN[2]	J12
USB_DN[3]	H10
USB_DP[0]	M16
USB_DP[1]	J14
USB_DP[2]	K12
USB_DP[3]	K10
USB_HSIC0_DATA	B4
USB_HSIC0_STROBE	B5

Ball Name	Location
USB_HSIC1_DATA	E2
USB_HSIC1_STROBE	D2
USB_HSIC_RCOMP	A7
USB_HSIC_V1P24_G3	V18
USB_OC[0]#	C20
USB_OC[1]#	B20
USB_PLL_MON	M13
USB_RCOMPI	C7
USB_RCOMPO	D6
USB_ULPI_CLK	G2
USB_ULPI_DATA[0]	M3
USB_ULPI_DATA[1]	L1
USB_ULPI_DATA[2]	K2
USB_ULPI_DATA[3]	K3
USB_ULPI_DATA[4]	M2
USB_ULPI_DATA[5]	N3
USB_ULPI_DATA[6]	P2
USB_ULPI_DATA[7]	L3
USB_ULPI_DIR	J3
USB_ULPI_NXT	P3
USB_ULPI_REFCLK	B12
USB_ULPI_RST#	J20
USB_ULPI_STP	H3
USB_ULPI_V1P8_G3	AA18
USB_V1P0_S3	M14
USB_V1P0_S3	U18
USB_V1P0_S3	U19
USB_V1P8_G3	N20
USB_V3P3_G3	N18
USB_V3P3_G3	P18
USB_VSSA	U16
USB3DEV_REXT[0]	M7
USB3DEV_RXN[0]	P12
USB3DEV_RXP[0]	P10
USB3DEV_TXN[0]	M6
USB3DEV_TXP[0]	M4
USB3DEV_V1P0_S3	G1
USB3DEV_V1P0_S3	Y18
VGA_BLUE	AY2
VGA_DDCCLK	BC1
VGA_DDCDATA	BC2
VGA_GREEN	BA1
VGA_HSYNC	BD2
VGA_IREF	AW1

Ball Name	Location
VGA_IRTN	AY3
VGA_RED	BA3
VGA_V1P0_S3	BJ6
VGA_V1P35_S3_F1	BD1
VGA_V3P3_S3	AN24
VGA_VSYNC	BF2
VSS	A3
VSS	A5
VSS	A6
VSS	A11
VSS	A15
VSS	A19
VSS	A23
VSS	A27
VSS	A31
VSS	A35
VSS	A39
VSS	A43
VSS	A47
VSS	A49
VSS	A51
VSS	A52
VSS	B2
VSS	B52
VSS	B53
VSS	C1
VSS	C14
VSS	C31
VSS	C34
VSS	C39
VSS	C42
VSS	C45
VSS	C49
VSS	C53
VSS	D12
VSS	D16
VSS	D24
VSS	D30
VSS	D36
VSS	D38
VSS	E1
VSS	E8
VSS	E19
VSS	E35

Ball Name	Location
VSS	E53
VSS	F2
VSS	F5
VSS	F7
VSS	F19
VSS	F24
VSS	F27
VSS	F30
VSS	F35
VSS	G10
VSS	G20
VSS	G22
VSS	G26
VSS	G28
VSS	G32
VSS	G34
VSS	G42
VSS	H19
VSS	H27
VSS	H35
VSS	J1
VSS	J16
VSS	J19
VSS	J22
VSS	J27
VSS	J32
VSS	J35
VSS	J40
VSS	J53
VSS	K4
VSS	K9
VSS	K14
VSS	K22
VSS	K32
VSS	K36
VSS	K50
VSS	L13
VSS	L19
VSS	L27
VSS	L35
VSS	M19
VSS	M26
VSS	M27
VSS	M28

Ball Name	Location
VSS	M34
VSS	M35
VSS	M38
VSS	M47
VSS	M51
VSS	N1
VSS	N16
VSS	N38
VSS	N51
VSS	P4
VSS	P9
VSS	P13
VSS	P16
VSS	P19
VSS	P20
VSS	P24
VSS	P32
VSS	P35
VSS	P38
VSS	P47
VSS	P52
VSS	T40
VSS	U1
VSS	U3
VSS	U5
VSS	U6
VSS	U8
VSS	U9
VSS	U11
VSS	U12
VSS	U14
VSS	U21
VSS	U30
VSS	U32
VSS	U40
VSS	U42
VSS	U43
VSS	U45
VSS	U46
VSS	U48
VSS	U49
VSS	U51
VSS	U53
VSS	V7

Ball Name	Location	Ball Name	Location	Ball Name	Location
VSS	V12	VSS	AC38	VSS	AH51
VSS	V16	VSS	AD7	VSS	AJ1
VSS	V19	VSS	AD19	VSS	AJ3
VSS	V21	VSS	AD21	VSS	AJ16
VSS	V35	VSS	AD25	VSS	AJ21
VSS	V40	VSS	AD32	VSS	AJ25
VSS	V44	VSS	AD33	VSS	AJ27
VSS	V51	VSS	AD47	VSS	AJ29
VSS	Y7	VSS	AE1	VSS	AJ30
VSS	Y9	VSS	AE3	VSS	AJ32
VSS	Y10	VSS	AE4	VSS	AJ33
VSS	Y14	VSS	AE6	VSS	AJ35
VSS	Y16	VSS	AE8	VSS	AJ38
VSS	Y21	VSS	AE9	VSS	AJ53
VSS	Y25	VSS	AE11	VSS	AK10
VSS	Y33	VSS	AE12	VSS	AK14
VSS	Y41	VSS	AE14	VSS	AK16
VSS	Y44	VSS	AE40	VSS	AK33
VSS	AA1	VSS	AE42	VSS	AK41
VSS	AA3	VSS	AE43	VSS	AK44
VSS	AA16	VSS	AE45	VSS	AM7
VSS	AA19	VSS	AE46	VSS	AM12
VSS	AA21	VSS	AE48	VSS	AM19
VSS	AA32	VSS	AE50	VSS	AM24
VSS	AA35	VSS	AE51	VSS	AM25
VSS	AA38	VSS	AE53	VSS	AM29
VSS	AA53	VSS	AF10	VSS	AM33
VSS	AB4	VSS	AF12	VSS	AM35
VSS	AB6	VSS	AF25	VSS	AM36
VSS	AB10	VSS	AF32	VSS	AM40
VSS	AB41	VSS	AF47	VSS	AM44
VSS	AB45	VSS	AG16	VSS	AM51
VSS	AB47	VSS	AG25	VSS	AN1
VSS	AB48	VSS	AG36	VSS	AN3
VSS	AB50	VSS	AG38	VSS	AN5
VSS	AB51	VSS	AH4	VSS	AN6
VSS	AC16	VSS	AH6	VSS	AN8
VSS	AC18	VSS	AH7	VSS	AN9
VSS	AC19	VSS	AH9	VSS	AN11
VSS	AC21	VSS	AH41	VSS	AN12
VSS	AC25	VSS	AH45	VSS	AN14
VSS	AC33	VSS	AH47	VSS	AN22
VSS	AC35	VSS	AH48	VSS	AN33
VSS	AC36	VSS	AH50	VSS	AN35

Ball Name	Location
VSS	AN36
VSS	AN38
VSS	AN40
VSS	AN42
VSS	AN43
VSS	AN45
VSS	AN46
VSS	AN48
VSS	AN49
VSS	AN51
VSS	AN53
VSS	AP40
VSS	AT4
VSS	AT12
VSS	AT16
VSS	AT19
VSS	AT24
VSS	AT27
VSS	AT30
VSS	AT35
VSS	AT38
VSS	AT47
VSS	AT52
VSS	AU1
VSS	AU3
VSS	AU24
VSS	AU30
VSS	AU38
VSS	AU51
VSS	AV7
VSS	AV12
VSS	AV13
VSS	AV14
VSS	AV18
VSS	AV19
VSS	AV24
VSS	AV27
VSS	AV30
VSS	AV35
VSS	AV38
VSS	AV47
VSS	AV51
VSS	AW3
VSS	AW13

Ball Name	Location
VSS	AW19
VSS	AW27
VSS	AW35
VSS	AY4
VSS	AY9
VSS	AY10
VSS	AY22
VSS	AY32
VSS	AY36
VSS	AY50
VSS	BA14
VSS	BA19
VSS	BA22
VSS	BA27
VSS	BA32
VSS	BA35
VSS	BA40
VSS	BA53
VSS	BB19
VSS	BB27
VSS	BB35
VSS	BC20
VSS	BC22
VSS	BC26
VSS	BC28
VSS	BC32
VSS	BC34
VSS	BC42
VSS	BD19
VSS	BD24
VSS	BD27
VSS	BD30
VSS	BD35
VSS	BE1
VSS	BE2
VSS	BE8
VSS	BE19
VSS	BE35
VSS	BE53
VSS	BF4
VSS	BF12
VSS	BF16
VSS	BF24
VSS	BF30

Ball Name	Location
VSS	BF36
VSS	BF38
VSS	BG1
VSS	BG31
VSS	BG34
VSS	BG39
VSS	BG42
VSS	BG45
VSS	BG49
VSS	BG53
VSS	BH1
VSS	BH2
VSS	BH52
VSS	BH53
VSS	BJ2
VSS	BJ3
VSS	BJ5
VSS	BJ7
VSS	BJ11
VSS	BJ15
VSS	BJ19
VSS	BJ23
VSS	BJ27
VSS	BJ31
VSS	BJ35
VSS	BJ39
VSS	BJ43
VSS	BJ47
VSS	BJ49
VSS	BJ51
VSS	BJ52
VSSA	AN16

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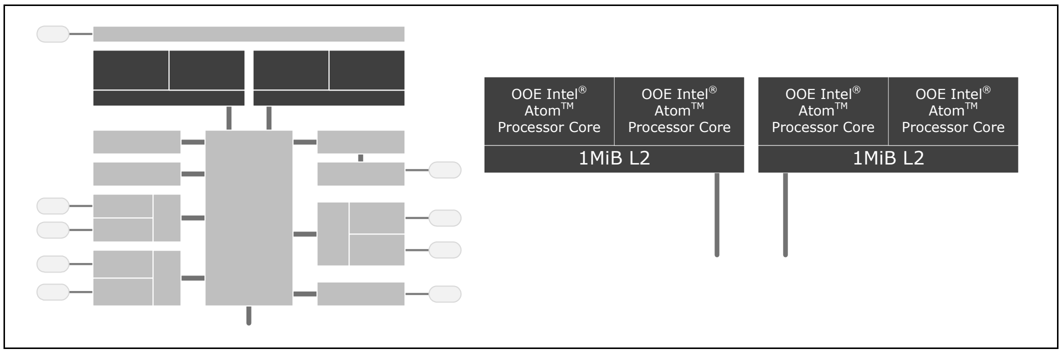
11 Processor Core

Up to four out-of-order execution processor cores are supported, each dual core module supports up to 1 MiB of L2 cache.



11.1 Features

- Single, Dual or Quad Out-of-Order Execution (OOE) processor cores
- Primary 32 KiB, 8-way L1 instruction cache and 24 KiB, 6-way L1 write-back data cache
- Cores are grouped into dual-core modules: modules share a 1 MiB, 16-way L2 cache (2 MiB total for Quad Core)
    — Dual core SKU's use 512 KiB per core. Each core has a dedicated link to memory.
- L1 caches has Parity Protection and L2 cache has ECC Protection
- Intel® Streaming SIMD Extensions 4.1 and 4.2 (SSE4.1 and SSE4.2), which include new instructions for media and for fast XML parsing
- Intel® 64 architecture
- Support for IA 32-bit
- Support for Intel® VT-x
- Support for Intel® Carry-Less Multiplication Instruction (PCLMULQDQ)
- Support for a Digital Random Number Generator (via RDRAND instruction)
- Supports C0, C1, C6
- Thermal management support via Intel® Thermal Monitor (TM1 and TM2)
- Uses Power Aware Interrupt Routing (PAIR)
- Uses 22 nm process technology
- Real Time Instruction Trace for debug

- Supports RTIT

Note: Intel® Hyper-Threading Technology is not supported.

11.1.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

Intel® VT-x specifications and functional descriptions are included in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B* and is available at: http://www.intel.com/products/processor/manuals/index.htm

Other Intel® VT documents can be referenced at: http://www.intel.com/technology/virtualization/index.htm

11.1.1.1 Intel® VT-x Objectives

- Robust: VMMs no longer need to use paravirtualization or binary translation. This means that they will be able to run off-the-shelf OSs and applications without any special steps.
- Enhanced: Intel® VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- More reliable: Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- More secure: The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system. Intel® VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel® VT-x features to provide improved reliable virtualized platform.

11.1.1.1.1 Intel® VT-x Features

- Extended Page Tables (EPT)
  - — EPT is hardware assisted page table physical memory virtualization
  - — Support guest VM execution in unpaged protected mode or in real-address mode
  - — It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)

  — A VM Virtual Processor ID is used to tag processor core hardware structures (such as TLBs) to allow a logic processor to cache information (such as TLBs) for multiple linear address spaces
  — This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead
- Guest Preemption Timer
  — Mechanism for a VMM to preempt the execution of a guest OS VM after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest.
  — The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees flexibility in guest VM scheduling and building Quality of Service (QoS) schemes
- Descriptor-Table Exiting
  — Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector)
  — A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software
- VM Functions
  — A VM function is an operation provided by the processor that can be invoked using the VMFUNC instruction from guest VM without a VM exit
  — A VM function to perform EPTP switching is supported and allows guest VM to load a new value for the EPT pointer, thereby establishing a different EPT paging structure hierarchy

11.1.2 Security and Cryptography Technologies

11.1.2.1 Advanced Encryption Standard New Instructions (AES-NI)

The processor supports Advanced Encryption Standard New Instructions (AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). AES-NI are valuable for a wide range of cryptographic applications, for example: applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

AES-NI consists of six Intel® SSE instructions. Four instructions, namely AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide a full hardware for support AES, offering security, high performance, and a great deal of flexibility.

11.1.2.2 PCLMULQDQ Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two, 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

11.1.2.3 Digital Random Number Generator

The processor introduces a software visible digital random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the new RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards (ANSI X9.82 and NIST SP 800-90).

Some possible uses of the new RDRAND instruction include cryptographic key generation as used in a variety of applications including communication, digital signatures, secure storage, etc.

11.1.3 Power Aware Interrupt Routing

PAIR is an improvement in H/W routing of “redirectable” interrupts. Each core power-state is considered in the routing selection to reduce the power or performance impact of interrupts. System BIOS configures the routing algorithm, e.g. fixed-priority, rotating, hash, or PAIR, during setup via non-architectural register. The PAIR algorithm can be biased to optimize for power or performance and the largest gains will be seen in systems with high interrupt rates.

11.2 Platform Identification and CPUID

In addition to verifying the processor signature, the intended processor platform type must be determined to properly target the microcode update. The intended processor platform type is determined by reading bits [52:50] of the IA32_PLATFORM_ID register, (MSR 17h) within the processor. This is a 64-bit register that must be read using the RDMSR instruction. The 3 Platform Id bits, when read as a binary coded decimal (BCD) number, indicate the bit position in the microcode update header’s Processor Flags field that is asSoCiated with the installed processor.

Executing the CPUID instruction with EAX=1 will provide the following information.

EAX	Field description
[31:28]	Reserved
[27:20]	Extended Family value
[19:16]	Extended Model value
[15:13]	Reserved
[12]	Processor Type Bit
[11:8]	Family value
[7:4]	Model value
[3:0]	Stepping ID Value

11.3 References

For further details of Intel® 64 and IA-32 architectures refer to Intel® 64 and IA-32 Architectures Software Developer's Manual Combined Volumes:1, 2A, 2B, 2C, 3A, 3B, and 3C:

- http://www.intel.com/content/www/µs/en/processors/architectures-software-developer-manuals.html

For more details on AES-NI refer to:

- Intel ® Performance Primitives (IPP) web page - http://software.intel.com/en-us/intel-ipp/
- White Paper on AES-NI - http://software.intel.com/en-us/articles/intel-advanced-encryption-standard-aes-instructions-set/

For more details on using the RDRAND instruction refer to Intel® Advanced Vector Extensions Programming Reference.

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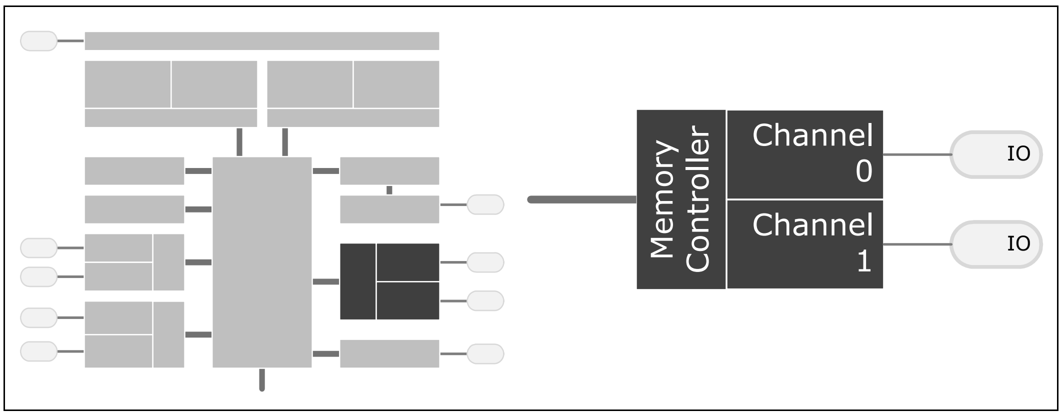
12 System Memory Controller

The system memory controller supports DDR3L protocol with up to two 64-bit wide dual rank channels at data rates up to 1333 MT/s. ECC is also available on a single channel.

Note: The memory data rate is fixed for each SKU. For example, a SKU that supports 1333 MT/s will only run at 1333 MT/s, nothing lower. For single channel use cases, Channel 0 must be used.



12.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 150. Memory Channel 0 DDR3L Signals (Sheet 1 of 2)

Signal Name	Direction Type	Description
DRAM0_CKP[2,0] **DRAM0_CKN[2,0]**	O DDR3	**SDRAM and inverted Differential Clock:** (1 pair per Rank) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to one rank on DRAM side.
DRAM0_CS[2,0]#	O DDR3	**Chip Select:** (1 per Rank). Used to qualify the command on the command bus for a particular rank.
DRAM0_CKE[2,0]	O DDR3	**Clock Enable:** (power management) It is used during DRAM power up/power down and Self refresh. *Note: DDR3L uses only DRAM0_CKE[2,0]. DRAM0_CKE[1,3] are not being used for DDR3L.*
DRAM0_MA[15:0]	O DDR3	**Memory Address:** Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol w.r.t. DRAM0_CKN, DRAM0_CKP pairs
DRAM0_BS[2:0]	O DDR3	**Bank Select:** These signals define which banks are selected within each DRAM rank
DRAM0_RAS#	O DDR3	**Row Address Select:** Used with DRAM0_CAS# and DRAM0_WE# (along with DRAM0_CS#) to define the DRAM Commands
DRAM0_CAS#	O DDR3	**Column Address Select:** Used with DRAM0_RAS# and DRAM0_WE# (along with DRAM0_CS#) to define the DRAM Commands
DRAM0_WE#	O DDR3	**Write Enable Control Signal:** Used with DRAM0_WE# and DRAM0_CAS# (along with control signal, DRAM0_CS#) to define the DRAM Commands.
DRAM0_DQ[63:0]	I/O DDR3	**Data Lines:** Data signal interface to the DRAM data bus
DRAM0_DM[7:0]	O DDR3	**Data Mask:** DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
DRAM0_DQSP[7:0] **DRAM0_DQSN[7:0]**	I/O DDR3	**Data Strobes:** The data is captured at the crossing point of each 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
DRAM0_ODT[2,0]	O DDR3	**On Die Termination:** ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.

Table 150. Memory Channel 0 DDR3L Signals (Sheet 2 of 2)

Signal Name	Direction Type	Description
DRAM_RCOMP[2]	O Analog	**Resistor Compensation:** This signal needs to be terminated to VSS on board (refer to platform design guide for resistor value). This external resistor termination scheme is used for Resistor compensation of DRAM ODT strength.
DRAM_RCOMP[1]	O Analog	**Resistor Compensation:** This signal needs to be terminated to VSS on board (refer to platform design guide for resistor value). This external resistor termination scheme is used for Resistor compensation of DQ buffers
DRAM_RCOMP[0]	O Analog	**Resistor Compensation:** This signal needs to be terminated to VSS on board (refer to platform design guide for resistor value). This external resistor termination scheme is used for Resistor compensation of CMD buffers.
DRAM_VREF	I Analog	**Reference Voltage:** DRAM interface Reference Voltage
DRAM_CORE_PWROK	I Asynchronous CMOS	**Core Power OK:** This signal indicates the status of the DRAM Core power supply (power on in S0).
DRAM_VDD_S4_PWROK	I Asynchronous CMOS	**VDD Power OK:** Asserted once the VRM is settled. Used primarily in the DRAM PHY to determine S3 state.
DRAM0_DRAMRST#	O	**DRAM Reset:** This signal is used to reset DRAM devices.
ICLK_DRAM_TERM [1:0]	I/O	Pull-down to VSS through an 100kOhm 1% resistor.

Table 151. Memory Channel 1 DDR3L Signals (Sheet 1 of 2)

Signal Name	Direction Type	Description
DRAM1_CKP[2,0] **DRAM1_CKN[2,0]**	O DDR3	**SDRAM and inverted Differential Clock:** (1 pair per Rank) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to one rank on DRAM side.
DRAM1_CS[2,0]#	O DDR3	**Chip Select:** (1 per Rank). Used to qualify the command on the command bus for a particular rank.
DRAM1_CKE[2,0]	O DDR3	**Clock Enable:** (power management) It is used during DRAM power up/power down and Self refresh. *Note: DDR3L uses only DRAM1_CKE[0,2]. DRAM1_CKE[1,3] are not being used for DDR3L.*

Table 151. Memory Channel 1 DDR3L Signals (Sheet 2 of 2)

Signal Name	Direction Type	Description
DRAM1_MA[15:0]	O DDR3	**Memory Address:** Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol relative to DRAM1_CKN, DRAM1_CKP pairs
DRAM1_BS[2:0]	O DDR3	**Bank Select:** These signals define which banks are selected within each DRAM rank
DRAM1_RAS#	O DDR3	**Row Address Select:** Used with DRAM1_CAS# and DRAM1_WE# (along with DRAM1_CS#) to define the DRAM Commands
DRAM1_CAS#	O DDR3	**Column Address Select:** Used with DRAM1_RAS# and DRAM1_WE# (along with DRAM1_CS#) to define the DRAM Commands
DRAM1_WE#	O DDR3	**Write Enable Control Signal:** Used with DRAM1_WE# and DRAM1_CAS# (along with control signal, DRAM1_CS#) to define the DRAM Commands.
DRAM1_DQ[63:0]	I/O DDR3	**Data Lines:** Data signal interface to the DRAM data bus.
DRAM1_DM[7:0]	O DDR3	**Data Mask:** DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
DRAM1_DQSP[7:0] **DRAM1_DQSN[7:0]**	I/O DDR3	**Data Strobes:** The data is captured at the crossing point of DRAM1_DQSP[7:0] and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
DRAM1_ODT[2,0]	O DDR3	**On Die Termination:** ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.
DRAM1_DRAMRST#	O	**Reset DRAM:** This signal can be used to reset DRAM devices.

12.1.1 ECC Support

The system memory controller supports ECC. When ECC is enabled, only Memory Channel 0 will be active. Memory Channel 1 will be disabled and used for the ECC data signals. Signals on Memory Channel 1 not used for ECC will be tri-stated. The table below shows the details on the muxing relationship between the ECC signals and the Memory Channel 1 signals.

Note: Although ECC and non-ECC SO-DIMM's share the same socket, ECC SO-DIMMs are not pinout compatible with standard, non-ECC SO-DIMMs.

Table 152. ECC Signals and Memory Channel 1 Signal Muxing

Memory Channel 1 Signal Names	Ball #	Signal Names when ECC is Enabled
DRAM1_DQ[56]	AM52	DRAM0_ECC_DQ[0]
DRAM1_DQ[57]	AL51	DRAM0_ECC_DQ[1]
DRAM1_DQ[58]	AG53	DRAM0_ECC_DQ[2]
DRAM1_DQ[59]	AG51	DRAM0_ECC_DQ[3]
DRAM1_DQ[60]	AL53	DRAM0_ECC_DQ[4]
DRAM1_DQ[61]	AK51	DRAM0_ECC_DQ[5]
DRAM1_DQ[62]	AF52	DRAM0_ECC_DQ[6]
DRAM1_DQ[63]	AF51	DRAM0_ECC_DQ[7]
DRAM1_DM[7]	AK52	DRAM0_ECC_DM
DRAM1_DQSP[7]	AH52	DRAM0_ECC_DQSP
DRAM1_DQSN[7]	AJ51	DRAM0_ECC_DQSN

Table 153. ECC Signals

Signal Name	Direction Type	Description
DRAM0_ECC_DQ[7:0]	I/O DDR3	**ECC Check Data Bits** *These are muxed with channel 1.*
DRAM0_ECC_DM	O DDR3	**ECC Data Mask:** DM is an optional output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of ECC_DQS. *This signal is muxed with channel 1 and may not be needed.*
DRAM0_ECC_DQSP **DRAM0_ECC_DQSN**	I/O DDR3	**ECC Data Strobes:** The data is captured at the crossing point the 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window. *These are muxed with channel 1.*

12.2 Features

The system memory controller supports the following DDR3L DRAM technologies, Data Transfer Rates, SO-DIMM Modules and other features:

- DDR3L Data Transfer Rates (Fixed per SKU): 1066MT/s (Theoretical Maximum Bandwidth: 8.5 GB/s per channel) or 1333MT/s (Theoretical Maximum Bandwidth: 10.6 GB/s per channel)
- DDR3L SDRAM's (1.35 V DRAM interface I/Os, including DDR3L-RS)
- DDR3L DRAM Device Technology

- Standard 1Gb, 2Gb and 4Gb technologies and addressing
- Read latency 5, 6, 7, 8, 9, 10, 11
- Write latency 5, 6, 7, 8

- DDR3L SO-DIMM Modules (unbuffered)
  - Raw Card B = 1 rank of x8 SDRAM
  - Raw Card C = 1 rank of x16 SDRAM
  - Raw Card F = 2 ranks of x8 SDRAM
  - ECC Raw Card C = 1 rank of x8 SDRAM
  - ECC Raw Card D = 2 ranks of x8 SDRAM
  - No mixed Raw Card support
  - Contact your Intel representative for platform supportable memory configurations and limitations based on layout and firmware initialization (MRC) requirements
- Support Trunk Clock Gating
- Supports up to two 64-bit channels
  - Channel 0 only for single channel configuration
- ECC support for 64-bit data bus
- Support early SR exit
- Support slow power down

12.2.1 System Memory Technology Support

Table 154. Supported DDR3L DRAM Devices

DRAM Density	Data Width	Banks	Bank Address	Row Address	Column Address	Page Size
1Gb	x8	8	BA[2:0]	A[13:0]	A[9:0]	1KB
2Gb	x8	8	BA[2:0]	A[14:0]	A[9:0]	1KB
4Gb	x8	8	BA[2:0]	A[15:0]	A[9:0]	1KB
2Gb	x16	8	BA[2:0]	A[13:0]	A[9:0]	2KB

Table 155. Supported DDR3L Memory Size Per Rank

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
1GB	8	1Gb	x8	8KB = 1KB * 8 chips

Table 155. Supported DDR3L Memory Size Per Rank

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
2GB	8	2Gb	x8	8KB = 1KB * 8 chips
4GB	8	4Gb	x8	8KB = 1KB * 8 chips
1GB	4	2Gb	x16	8KB = 2KB * 4 chips

Table 156. Supported DDR3L ECC Memory Size Per Rank

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
2GB	8	2Gb	x8	8KB = 1KB * 8 chips
4GB	8	4Gb	x8	8KB = 1KB * 8 chips

Table 157. Supported DDR3L SO-DIMM Size

DRAM Chip Density	Module Size	# of chips needed	DRAM Chip Data Width	Data Bus Width	# of Ranks needed	# of chips /rank
1Gbit	2GB	16	x8	x64	2	8
2Gbit	1GB	4	x16	x64	1	4
2Gbit	2GB	8 (9 w/ECC)	x8	x64	1	8
2Gbit	4GB	16 (18 w/ECC)	x8	x64	2	8
4Gbit	4GB	8 (9 w/ECC)	x8	x64	1	8
4Gbit	8GB	16 (18 w/ECC)	x8	x64	2	8

The frequency of system memory is fixed based on SKU. Timing parameters (CAS latency or CL + AL for DDR3, tRAS, tRCD, tRP) must be programmed to match within a channel (Contact your Intel field representative for more information on memory reference code (MRC)). The controller supports these configurations:

— Supports 1 SO-DIMM per channel.

— Each SO-DIMM can have 1 or 2 ranks.

— If a SO-DIMM has two ranks, then both ranks must be symmetrical (same chip width, same chip density, and same total memory size per rank).

— For dual channel population, the two channels must be populated symmetrically (chip width, density, ranks).

— The maximum total memory supported by the SoC is 8GB. Contact your Intel representative for guidelines on the specific SO-DIMM Raw cards supported.

12.3 System Memory Controller (D-Unit) Message Registers

Table 158. Summary of Memory Controller Message Bus Registers—Port 0x01

Offset	Register Name (Register Symbol)	Default Value
0–0h	"DRP—Offset 0h" on page 288	00000000h
1–1h	"DTR0—Offset 1h" on page 289	43001110h
2–2h	"DTR1 (DTR1)—Offset 2h" on page 291	02690320h
3–3h	"DTR2—Offset 3h" on page 293	00845544h
4–4h	"DTR3 (DTR3)—Offset 4h" on page 294	06406255h
5–5h	"DTR4 (DTR4)—Offset 5h" on page 295	00003322h
6–6h	"DPMC0 (DPMC0)—Offset 6h" on page 296	0B000000h
7–7h	"DPMC1 (DPMC1)—Offset 7h" on page 298	00000011h
8–8h	"DRFC (DRFC)—Offset 8h" on page 299	03012CA7h
9–9h	"DSCH (DSCH)—Offset 9h" on page 300	00071108h
A–Ah	"DCAL (DCAL)—Offset Ah" on page 301	00001300h
B–Bh	"DRMC (DRMC)—Offset Bh" on page 303	00000000h
C–Ch	"PMSTS (PMSTS)—Offset Ch" on page 303	00000000h
F–Fh	"DCO (DCO)—Offset Fh" on page 304	00000000h
10–10h	"DTRC (DTRC)—Offset 10h" on page 305	00000000h
12–12h	"DCBR (DCBR)—Offset 12h" on page 306	00000000h
20–20h	"DSTAT (DSTAT)—Offset 20h" on page 307	0000000Ah
21–21h	"PGTBL (PGTBL)—Offset 21h" on page 308	00000000h
31–31h	"MISRCCCLR (MISRCCCLR)—Offset 31h" on page 309	00000000h
32–32h	"MISRDDCLR (MISRDDCLR)—Offset 32h" on page 309	00000000h
34–34h	"MISRCCSIG (MISRCCSIG)—Offset 34h" on page 310	FFFFFFFFh
35–35h	"MISRDDSIG (MISRDDSIG)—Offset 35h" on page 310	FFFFFFFFh
37–37h	"MISRECCSIG (MISRECCSIG)—Offset 37h" on page 310	FFFFFFFFh
4A–4Ah	"SSKPD0 (SSKPD0)—Offset 4Ah" on page 311	00000000h
4B–4Bh	"SSKPD1—Offset 4Bh" on page 311	00000000h
50–50h	"BONUS0 (BONUS0)—Offset 50h" on page 312	00000000h
51–51h	"BONUS1—Offset 51h" on page 312	00000000h
60–60h	"DECCCTRL (DECCCTRL)—Offset 60h" on page 313	00000000h
62–62h	"DECCSBECNT (DECCSBECNT)—Offset 62h" on page 314	00000000h
70–70h	"DFUSESTAT (DFUSESTAT)—Offset 70h" on page 314	00000000h
80–83h	"DSCRMSEED (DSCRMSEED)—Offset 80h" on page 315	00000000h
81–81h	"DSCRMLO (DSCRMLO)—Offset 81h" on page 316	00000000h
82–82h	"DSCRMHI (DSCRMHI)—Offset 82h" on page 316	00000000h
E0–E0h	"PMSEL0 (PMSEL0)—Offset E0h" on page 317	00000000h
E1–E1h	"PMSEL1 (PMSEL1)—Offset E1h" on page 317	00000000h
E2–E2h	"PMSEL2—Offset E2h" on page 318	00000000h

Table 158. Summary of Memory Controller Message Bus Registers—Port 0x01

Offset	Register Name (Register Symbol)	Default Value
E3–E3h	"PMSEL3—Offset E3h" on page 319	00000000h
E8–E8h	"PMAUXMAX (PMAUXMAX)—Offset E8h" on page 319	00000000h
E9–E9h	"PMAUXMIN—Offset E9h" on page 320	00000000h
EA–EAh	"PMAUXMAX (PMAUXMAX)—Offset E8h" on page 319	00000000h

12.3.1 DRP—Offset 0h

DRAM Rank Population

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 0h

Op Codes:
h - Read, h - Write

Default: 00000000h

Rsvd_31_24_DRP	ENLPDDR3	DRAMTYPE	DIMM1MIRR	DIMM0MIRR	Rsvd_19_DRP	CKECOPY	RANKREMAP	DIMMFLIP	Rsvd_15_DRP	RSIEN	Rsvd_13_DRP	DIMMDDEN1	DIMMDWID1	Rsvd_8_DRP	DIMMDDEN0	DIMMDWID0	RKEN3	RKEN2	RKEN1	RKEN0
0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0 0	0	0 0	0 0	0	0	0	0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Rsvd_31_24_DRP:** Reserved
23	0h RW/P/L	**ENLPDDR3:** Enable LPDDR3 Mode 0 - LPDDR2 1 - LPDDR3 Note: This bit is functional only when DRP.DRAMTYPE is set to LPDDR2
22	0h RW/P/L	**DRAMTYPE:** DRAM Type 0 - DDR3 1 - LPDDR2
21	0h RW/P/L	**DIMM1MIRR:** Address mapping to DIMM1 is mirrored. BIOS writes value defined in SPD Byte 63. Used as indication to Punit to flip MRS opcode to 2nd rank on DIMM1. This bit has no functional impact on Dunit. 0 - Standard 1 - Mirrored
20	0h RW/P/L	**DIMM0MIRR:** Address mapping to DIMM0 is mirrored. BIOS writes value defined in SPD Byte 63. Used as indication to Punit to flip MRS opcode to 2nd rank on DIMM0. This bit has no functional impact on Dunit. 0 - Standard 1 - Mirrored
19	0h RO	**Rsvd_19_DRP:** Reserved
18	0h RW/P/L	**CKECOPY:** Used for doubling CKE. 0 - no CKE copy 1 - Copy CKE[0] to CKE[1] and CKE[2] to CKE[3] Note: CKE to DDRIO also depends upon RANKREMAP and state of CA Training.
17	0h RW/P/L	**RANKREMAP:** Enables mapping logical rank to physical rank. 0 - no rank remap 1 - rank is remapped If (rank[0] is enabled) Map rank[1] to rank[2] Else (If rank[0] is disabled) Map rank[3:2] to rank[1:0]

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P/L	**DIMMFLIP:** DIMM Flip Required. BIOS must set this bit to 1 if the total size of DIMM1 is greater than the total size of DIMM0. DIMM Flipping simplifies rank decoding in dual-DIMM configuration when the DIMMs are not equal in size by mapping the low addresses to the larger DIMM.
15	0h RO	**Rsvd_15_DRP:** Reserved
14	0h RW/P/L	**RSIEN:** Rank Select Interleave Enable. 0 - Rank Select Interleave Disabled 1 - Rank Select Interleave Enabled Note: Rank select interleave enable should be set the same for both the Dunit and Bunit.
13	0h RO	**Rsvd_13_DRP:** Reserved
12:11	0h RW/P/L	**DIMMDDEN1:** DIMM 1 Device Density. This sets the density of the DRAM devices populated in DIMM 1 (Rank 0 and Rank 1). 00 - 1Gbit 01 - 2Gbit 10 - 4Gbit 11 - 8Gbit
10:9	0h RW/P/L	**DIMMDWID1:** DIMM 1 Device Width. Indicates the width of the DRAM devices populated in DIMM 1 (Rank 0 and Rank 1). 00 - x8 01 - x16 10 - x32 11 - Reserved
8	0h RO	**Rsvd_8_DRP:** Reserved
7:6	0h RW/P/L	**DIMMDDEN0:** DIMM 0 Device Density. This sets the density of the DRAM devices populated in DIMM 0 (Rank 0 and Rank 1). 00 - 1Gbit 01 - 2Gbit 10 - 4Gbit 11 - 8Gbit
5:4	0h RW/P/L	**DIMMDWID0:** DIMM 0 Device Width. Indicates the width of the DRAM devices populated in DIMM 0 (Rank 0 and Rank 1). 00 - x8 01 - x16 10 - x32 11 - Reserved
3	0h RW/P/L	**RKEN3:** DIMM 1, Rank 1 Enabled. Should be set to 1 when DIMM1 is populated and has 2 ranks to enable the use of this rank. Otherwise, must be set to 0.
2	0h RW/P/L	**RKEN2:** DIMM 1, Rank 0 Enabled. Should be set to 1 when DIMM1 is populated to enable the use of this rank. Otherwise, must be set to 0.
1	0h RW/P/L	**RKEN1:** DIMM 0, Rank 1 Enabled. Should be set to 1 when DIMM0 is populated and has 2 ranks to enable the use of this rank. Otherwise, must be set to 0.
0	0h RW/P/L	**RKEN0:** DIMM 0, Rank 0 Enabled. Should be set to 1 when DIMM0 is populated to enable the use of this rank. Otherwise, must be set to 0.

12.3.2 DTR0—Offset 1h

DRAM Timing Register 0

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + 1h

Op Codes:
h - Read, h - Write

Default: 43001110h

Bits	31:28	27:26	25:24	23	22	21	20	19	18	17	16	15	14:12	11:8	7:4	3:2	1:0
Default	0 1 0 0	0 0	1 1	0	0	0	0	0	0	0	0	0	0 0 1	0 0 0 1	0 0 0 1	0 0	0 0
Field	CKEDLY	Rsvd_27_26_DTR0	PMEDLY	Rsvd_23_DTR0	tZQoper	Rsvd_11	tZQCS	Rsvd_19_DTR0	tXSDLL	Rsvd_17_DTR0	tXS	Rsvd_15_DTR0	tCL	tRCD	tRP	Rsvd_3_2_DTR0	DFREQ

Bit Range	Default & Access	Field Name (ID): Description
31:28	4h RW	**CKEDLY:** Additional delay between CK/CKB start and SRX command. This delay is needed for clock to stabilize to meet JEDEC requirements. Delay is CKEDLY multiples of 256 DRAM Clocks. 0ns to 9,600ns (DDR3-800) 0ns to 7,200ns (DDR3-1066)
27:26	0h RO	**Rsvd_27_26_DTR0:** Reserved
25:24	3h RW	**PMEDLY:** The delay, in DRAM clocks, between SR Entry command and Power-Mode message to DDRIO. 0h - 6 DRAM Clocks 1h - 8 DRAM Clocks 2h - 10 DRAM Clocks 3h - 12 DRAM Clocks
23	0h RO	**Rsvd_23_DTR0:** Reserved
22	0h RW	**tZQoper:** The delay, in DRAM clocks, between ZQC-Long command to any command. Note: ZQCL command during DRAM Init flow requires longer latency which is controlled be BIOS. 0h - 256 DRAM Clocks 1h - 384 DRAM Clocks
21	0h RO	**Rsvd_11:** Reserved
20	0h RW	**tZQCS:** The delay, in DRAM clocks, between a ZQC-Short command to any command. 0h - 64 DRAM Clocks 1h - 96 DRAM Clocks
19	0h RO	**Rsvd_19_DTR0:** Reserved
18	0h RW	**tXSDLL:** The delay, in DRAM clocks, between SRX command to any command requiring locked DLL. Only ZQCL can be sent before tXSDLL is done. 0h - tXS + 256 DRAM Clocks 1h - tXS + 384 DRAM Clocks
17	0h RO	**Rsvd_17_DTR0:** Reserved
16	0h RW	**tXS:** The delay, in DRAM clocks, between SRX command to command not requiring locked DLL. The Dunit can send a ZQCL command after tXS. JEDEC defines MAX(5CK, tRFC(min)+10ns) so both values take safety margin. 0h - 256 DRAM Clocks 1h - 384 DRAM Clocks
15	0h RO	**Rsvd_15_DTR0:** Reserved
14:12	1h RW	**tCL:** CAS Latency. Specifies the delay, in DRAM clocks, between the issue of a RD command and the return of valid data on the DQ bus. 0h - 5 DRAM Clocks (DDR3-800) 1h - 6 DRAM Clocks (DDR3-800, 1066. LPDDR2-800) 2h - 7 DRAM Clocks (DDR3-1066, 1333) 3h - 8 DRAM Clocks (DDR3-1066, 1333, 1600. LPDDR2-1066) 4h - 9 DRAM Clocks (DDR3-1333, 1600) 5h - 10 DRAM Clocks (DDR3-1333, 1600. LPDDR3-1333) 6h - 11 DRAM Clocks (DDR3-1600) 7h - Reserved

Bit Range	Default & Access	Field Name (ID): Description
11:8	1h RW	**tRCD:** Activate (RAS) to CAS Delay. Specifies the delay, in DRAM clocks, between an ACT command and a RD/WR command to the same bank. 0h - 5 DRAM Clocks (DDR3-800) 1h - 6 DRAM Clocks (DDR3-800, 1066. LPDDR2-800) 2h - 7 DRAM Clocks (DDR3-1066, 1333) 3h - 8 DRAM Clocks (DDR3-1066, 1333, 1600. LPDDR2-800, 1066) 4h - 9 DRAM Clocks (DDR3-1333, 1600) 5h - 10 DRAM Clocks (DDR3-1333, 1600. LPDDR2-800, 1066. LPDDR3-1333) 6h - 11 DRAM Clocks (DDR3-1600) 7h - 12 DRAM Clocks (LPDDR3-1333) 8h - 13 DRAM Clocks (LPDDR2-1066) 9h - 14 DRAM Clocks Ah - 15 DRAM Clocks Bh - 16 DRAM Clocks (LPDDR3-1333) Others - Reserved
7:4	1h RW	**tRP:** Precharge to Activate Delay. Specifies the delay, in DRAM clocks, between a PRE command and an ACT command to the same bank. 0h - 5 DRAM Clocks (DDR3-800) 1h - 6 DRAM Clocks (DDR3-800, 1066. LPDDR2-800) 2h - 7 DRAM Clocks (DDR3-1066, 1333) 3h - 8 DRAM Clocks (DDR3-1066, 1333, 1600. LPDDR2-800, 1066) 4h - 9 DRAM Clocks (DDR3-1333, 1600) 5h - 10 DRAM Clocks (DDR3-1333, 1600. LPDDR2-800, 1066. LPDDR3-1333) 6h - 11 DRAM Clocks (DDR3-1600) 7h - 12 DRAM Clocks (LPDDR3-1333) 8h - 13 DRAM Clocks (LPDDR2-1066) 9h - 14 DRAM Clocks Ah - 15 DRAM Clocks Bh - 16 DRAM Clocks (LPDDR3-1333) Others - Reserved
3:2	0h RO	**Rsvd_3_2_DTR0:** Reserved
1:0	0h RW	**DFREQ:** DRAM Frequency. Specifies the DDR3 frequency used by Dunit for computing proper cycle to cycle timings. Note: This configuration has no impact on the actual DRAM clock. 0h - DDR3-800 1h - DDR3-1066 2h - DDR3-1333 3h - DDR3-1600

12.3.3 DTR1 (DTR1)—Offset 2h

DRAM Timing Register 1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 2h

Op Codes:
h - Read, h - Write

Default: 02690320h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0
Rsvd_31_DTR1	tRTP			Rsvd_27_26_DTR1		tRRD		tRAS				tFAW				Rsvd_15_14_DTR1		tCCD		tWTP				Rsvd_7_6_DTR1		tCMD		Rsvd_3_DTR1	tWCL		

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rsvd_31_DTR1:** Reserved
30:28	0h RW	**tRTP:** Read to Precharge Delay. The minimal delay between RD command and PRE command to same bank. 00 - 4 DRAM Clocks (DDR3-800 DDR3-1066) 01 - 5 DRAM Clocks (DDR3-1333) 10 - 6 DRAM Clocks (DDR3-1600) 11 - 7 DRAM Clocks

Bit Range	Default & Access	Field Name (ID): Description
27:26	0h RO	**Rsvd_27_26_DTR1:** Reserved
25:24	2h RW	**tRRD:** Row Activation to Row Activation Delay. The minimal time interval between 2 ACT commands to any bank in the same DRAM device. Limits peak current profile. 00 - 4 DRAM Clocks (1KB page DDR3-800, 1066, 1333) (2KB page DDR3-800, LPDDR2-800) 01 - 5 DRAM Clocks (1KB page DDR3-1600) (2KB page DDR3-1333) 10 - 6 DRAM Clocks (2KB page DDR3-1066, 1600. LPDDR3-1333) 11 - 7 DRAM Clocks
23:20	6h RW	**tRAS:** Row Activation Period. The minimal delay, in DRAM clocks, between ACT command and PRE command to same bank. At least equal to tRCD + tCWL + tCCD + tWR 0h -14 DRAM Clocks. 0h - Reserved 1h - 15 DRAM Clocks (DDR3-800) 2h - 16 DRAM Clocks 3h - 17 DRAM Clocks (LPDRR2-800) 4h - 18 DRAM Clocks 5h - 19 DRAM Clocks 6h - 20 DRAM Clocks (DDR3-1066) 7h - 21 DRAM Clocks 8h - 22 DRAM Clocks 9h - 23 DRAM Clocks (LPDRR2-1066) Ah - 24 DRAM Clocks (DDR3-1333) Bh - 25 DRAM Clocks Ch - 26 DRAM Clocks Dh - 27 DRAM Clocks Eh - 28 DRAM Clocks (DDR3-1600. LPDRR3-1333) Fh - 29 DRAM Clocks
19:16	9h RW	**tFAW:** Four Bank Activation Window. A rolling time-frame, in which a maximum of 4 ACT commands (per rank) can be sent. Limits peak current profile. 0h - Reserved 1h - Reserved 2h - 14 DRAM Clocks 3h - 16 DRAM Clocks (1KB page DDR3-800) 4h - 18 DRAM Clocks 5h - 20 DRAM Clocks (2KB page DDR3-800) (1KB page DDR3-1066, 1333. LPDDR2-800) 6h - 22 DRAM Clocks 7h - 24 DRAM Clocks (1KB page DDR3-1600) 8h - 26 DRAM Clocks 9h - 28 DRAM Clocks (2KB page DDR3-1066. LPDDR2-1066) Ah - 30 DRAM Clocks (2KB page DDR3-1333) Bh - 32 DRAM Clocks (2KB page DDR3-1600) Ch - 34 DRAM Clocks (LPDDR3-1333) Others - Reserved
15:14	0h RO	**Rsvd_15_14_DTR1:** Reserved
13:12	0h RW	**tCCD:** CAS to CAS delay. The minimum delay, in DRAM clocks, between 2 RD/WR commands. 0h - 4 DRAM Clocks: Functional mode. (DDR3-800, 1066, 1333, 1600) (LPDDR2-800, 1066) (LPDDR3-1333) 1h - 12 DRAM Clocks: DFX stretch mode (x2) 2h - 18 DRAM Clocks: DFX stretch mode (x4) 3h - Reserved
11:8	3h RW	**tWTP:** Write to Prechange. The minimum delay, in DRAM clocks, between a WR command and a PRE command to the same bank. Value should be computed as 4 + tWCL + tWR. 0h - 14 DRAM Clocks (LPDRR2-800) 1h - 15 DRAM Clocks (DDR3-800) 2h - 16 DRAM Clocks 3h - 17 DRAM Clocks (LPDDR2-1066) 4h - 18 DRAM Clocks (DDR3-1066) 5h - 19 DRAM Clocks 6h - 20 DRAM Clocks 7h - 21 DRAM Clocks (DDR3-1333. LPDDR3-1333) 8h - 22 DRAM Clocks 9h - 23 DRAM Clocks Ah - 24 DRAM Clocks (DDR3-1600) Bh - 25 DRAM Clocks Others - Reserved
7:6	0h RO	**Rsvd_7_6_DTR1:** Reserved
5:4	2h RW	**tCMD:** Command Transport Duration. The time period, in DRAM clocks, that a command occupies the DRAM command bus. 1N is the DDR3 basic requirement. 2N and 3N are extended modes for board signal-integrity. 0h - 1 DRAM Clock (1N) 1h - 2 DRAM Clocks (2N) 2h - 3 DRAM Clocks (3N)
3	0h RO	**Rsvd_3_DTR1:** Reserved
2:0	0h RW	**tWCL:** CAS Write Latency. The delay, in DRAM clocks, between the internal write command and the availability of the first bit of DRAM input data. 0h - 3 DRAM Clocks (LPDDR2-800) 1h - 4 DRAM Clocks (LPDDR2-1066) 2h - 5 DRAM Clocks (DDR3-800) 3h - 6 DRAM Clocks (DDR3-1066. LPDDR3-1333) 4h - 7 DRAM Clocks (DDR3-1333) 5h - 8 DRAM Clocks (DDR3-1600) Others - Reserved

12.3.4 DTR2—Offset 3h

DRAM Timing Register 2

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 3h

Op Codes:
h - Read, h - Write

Default: 00845544h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
Rsvd_31_25_DTR2							tRWDD				Rsvd_20_DTR2	tRWDR				Rsvd_15_DTR2	tWWDD			Rsvd_11_DTR2	tWWDR			Rsvd_7_DTR2	tRRDD			Rsvd_3_DTR2	tRRDR		

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Rsvd_31_25_DTR2:** Reserved
24:21	4h RW	**tRWDD:** Read to Write DQ delay, different DIMMs 0h - Reserved 1h - 6 DRAM Clocks (DDR3) 2h - 7 DRAM Clocks 3h - 8 DRAM Clocks 4h - 9 DRAM Clocks 5h - 10 DRAM Clocks (LPDDR2-800) 6h - 11 DRAM Clocks (LPDDR2-1066) 7h - 12 DRAM Clocks 8h - 13 DRAM Clocks 9h - 14 DRAM Clocks (LPDDR3-1333) Ah - 15 DRAM Clocks Bh - 16 DRAM Clocks Ch - 17 DRAM Clocks Dh - 18 DRAM Clocks Others - Reserved
20	0h RO	**Rsvd_20_DTR2:** Reserved
19:16	4h RW	**tRWDR:** Read to Write DQ delay, different ranks, same DIMM 0h - Reserved 1h - 6 DRAM Clocks (DDR3) 2h - 7 DRAM Clocks 3h - 8 DRAM Clocks 4h - 9 DRAM Clocks 5h - 10 DRAM Clocks (LPDDR2-800) 6h - 11 DRAM Clocks (LPDDR2-1066) 7h - 12 DRAM Clocks 8h - 13 DRAM Clocks 9h - 14 DRAM Clocks (LPDDR3-1333) Ah - 15 DRAM Clocks Bh - 16 DRAM Clocks Ch - 17 DRAM Clocks Dh - 18 DRAM Clocks Others - Reserved
15	0h RO	**Rsvd_15_DTR2:** Reserved
14:12	5h RW	**tWWDD:** Write to Write DQ delay, different DIMMs 0h - 4 DRAM Clocks (LPDRR2-800, 1066. LPDDR3-1333) 1h - 5 DRAM Clocks 2h - 6 DRAM Clocks (DDR3) 3h - 7 DRAM Clocks 4h - 8 DRAM Clocks 5h - 9 DRAM Clocks 6h - 10 DRAM Clocks 7h - Reserved
11	0h RO	**Rsvd_11_DTR2:** Reserved
10:8	5h RW	**tWWDR:** Write to Write DQ delay, different ranks, same DIMM 0h - 4 DRAM Clocks (LPDDR2-800, 1066. LPDDR3-1333) 1h - 5 DRAM Clocks 2h - 6 DRAM Clocks (DDR3) 3h - 7 DRAM Clocks 4h - 8 DRAM Clocks 5h - 9 DRAM Clocks 6h - 10 DRAM Clocks 7h - Reserved
7	0h RO	**Rsvd_7_DTR2:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	4h RW	**tRRDD:** Read to Read DQ delay, different DIMMs 0h - Reserved 1h - 6 DRAM Clocks (DDR3) 2h - 7 DRAM Clocks (LPDDR2-800, 1066. LPDDR3-1333) 3h - 8 DRAM Clocks 4h - 9 DRAM Clocks 5h - 10 DRAM Clocks 6h - 11 DRAM Clocks Others - Reserved
3	0h RO	**Rsvd_3_DTR2:** Reserved
2:0	4h RW	**tRRDR:** Read to Read DQ delay, different ranks, same DIMM 0h - Reserved 1h - 6 DRAM Clocks (DDR3) 2h - 7 DRAM Clocks (LPDDR2-800, 1066. LPDDR3-1333) 3h - 8 DRAM Clocks 4h - 9 DRAM Clocks 5h - 10 DRAM Clocks 6h - 11 DRAM Clocks Others - Reserved

12.3.5 DTR3 (DTR3)—Offset 4h

DRAM Timing Register 3

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 4h

Op Codes:
h - Read, h - Write

Default: 06406255h

Bits	Default	Field
31	0	Rsvd_31_DTR3
30	0	DERATESTAT
29	0	DERATEOVR
28	0	ENDRATE
27:24	0 1 1 0	PWDDLY
23:22	0 1	tXP
21:17	0 0 0 0 0	Rsvd_21_17_DTR3
16:13	0 0 1 1	tWRSR
12	0	Rsvd_12_DTR3
11:8	0 0 1 0	tRWSR
7	0	Rsvd_7_DTR3
6:4	1 0 1	tWRDD
3	0	Rsvd_3_DTR3
2:0	1 0 1	tWRDR

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rsvd_31_DTR3:** Reserved
30	0h RO	**DERATESTAT:** Timing De-rating Status
29	0h RW	**DERATEOVR:** Enabled Timing De-rating Override
28	0h RW	**ENDRATE:** Enabled Dynamic Timing De-rating
27:24	6h RW	**PWDDLY:** RD/WR command to Power-down delay. Non-JEDEC delay for performance enhancement. Delay = PWDDLY x 4 DRAM Clocks.
23:22	1h RW	**tXP:** Delay from CKE asserted high to any DRAM command 0h - 2 DRAM Clocks (DDR3-800 2N) 1h - 3 DRAM Clocks (DDR3-800 1N) (DDR3-1066, 1333 2N) (LPDDR2-800) 2h - 4 DRAM Clocks (DDR3-1066, 1333 1N) (DDR3-1600 2N) (LPDDR2-1066) 3h - 5 DRAM Clocks (DDR3-1600 1N) (LPDDR3-1333)
21:17	0h RO	**Rsvd_21_17_DTR3:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16:13	3h RW	**tWRSR:** Write to Read same rank command delay. Should be set to 4 + tWCL + tWTR 0h - 11 DRAM Clocks (LPDDR2-800) 1h - 12 DRAM Clocks 2h - 13 DRAM Clocks (DDR3-800. LPDDR2-1066) 3h - 14 DRAM Clocks (DDR3-1066) 4h - 15 DRAM Clocks 5h - 16 DRAM Clocks (DDR3-1333. LPDDR3-1333) 6h - 17 DRAM Clocks 7h - 18 DRAM Clocks (DDR3-1600) 8h - 19 DRAM Clocks 9h - 20 DRAM Clocks Others - Reserved
12	0h RO	**Rsvd_12_DTR3:** Reserved
11:8	2h RW	**tRWSR:** Read to Write same rank command delay. Should be set to tCL - tWCL + 6 + board delay if needed. 0h - 6 DRAM Clocks (DDR3) 1h - 7 DRAM Clocks 2h - 8 DRAM Clocks 3h - 9 DRAM Clocks 4h - 10 DRAM Clocks 5h - 11 DRAM Clocks (LPDDR2-800) 6h - 12 DRAM Clocks (LPDDR2-1066) 7h - 13 DRAM Clocks 8h - 14 DRAM Clocks 9h - 15 DRAM Clocks (LPDDR3-1333) Ah - 16 DRAM Clocks Bh - 17 DRAM Clocks Others - Reserved
7	0h RO	**Rsvd_7_DTR3:** Reserved
6:4	5h RW	**tWRDD:** Write to Read DQ delay, different DIMMs 0h - 4 DRAM Clocks (LPDDR3-1333) 1h - 5 DRAM Clocks (LPDDR2-800, 1066) 2h - 6 DRAM Clocks (DDR3) 3h - 7 DRAM Clocks 4h - 8 DRAM Clocks 5h - 9 DRAM Clocks 6h - 10 DRAM Clocks Others - Reserved
3	0h RO	**Rsvd_3_DTR3:** Reserved
2:0	5h RW	**tWRDR:** Write to Read DQ delay, different ranks, same DIMM 0h - Reserved 1h - 4 DRAM Clocks (LPDDR3-1333) 2h - 5 DRAM Clocks (LPDDR2-800, 1066) 3h - 6 DRAM Clocks (DDR3) 4h - 7 DRAM Clocks 5h - 8 DRAM Clocks 6h - 9 DRAM Clocks 7h - 10 DRAM Clocks

12.3.6 DTR4 (DTR4)—Offset 5h

DRAM Timing Register 4

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + 5h

Op Codes:
h - Read, h - Write

Default: 00003322h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0

Bits	Field
31:19	Rsvd_31_19_DTR4
18	WRBODTDIS
17	RDODTDIS
16	TRGSTRDIS
15	Rsvd_15_DTR4
14:12	RDODTSTOP
11	Rsvd_24
10:8	RDODTSTRT
7	Rsvd_7_DTR4
6:4	WRODTSTOP
3:2	Rsvd_3_2_DTR4
1:0	WRODTSTRT

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Rsvd_31_19_DTR4:** Reserved
18	0h RW	**WRBODTDIS:** Disable Write ODT on non-targeted DIMM. When writing to DIMM A, ODT is asserted to the target rank of DIMM A and also to the low rank of DIMM B. This defeature bit is used to disable ODT assertion to the opposite DIMM during write.
17	0h RW	**RDODTDIS:** Disable Read ODT. When reading from DIMM A, ODT is asserted to the low rank of DIMM B. This defeature bit is used to disable ODT assertion during reads.
16	0h RW	**TRGSTRDIS:** Write target rank is not stretched. When set, stretched ODT as defined above is not applied to the write target rank and ODT command is asserted for 6 DRAM clocks. Should not be used when ODT is pulled-in.
15	0h RO	**Rsvd_15_DTR4:** Reserved
14:12	3h RW	**RDODTSTOP:** Read command to ODT de-assert delay Value should be set to: RDODTSTRT+6+(WRODTSTOP-WRODTSTRT) 0h - 6 DRAM Clocks 1h - 7 DRAM Clocks 2h - 8 DRAM Clocks 3h - 9 DRAM Clocks 4h - 10 DRAM Clocks 5h - 11 DRAM Clocks 6h - 12 DRAM Clocks 7h - 13 DRAM Clocks Other - Reserved
11	0h RO	**Rsvd_24:** Reserved
10:8	3h RW	**RDODTSTRT:** Read command to ODT assert delay. Value should be set to tCMD+tCL-tWCL-ODT_PULLIN, where ODT_PULLIN must have the same value as in WRODTSTRT. 0h - 0 DRAM Clocks 1h - 1 DRAM Clocks 2h - 2 DRAM Clocks 3h - 3 DRAM Clocks 4h - 4 DRAM Clocks 5h - 5 DRAM Clocks Other - Reserved
7	0h RO	**Rsvd_7_DTR4:** Reserved
6:4	2h RW	**WRODTSTOP:** Write command to ODT de-assert delay. WRODTSTOP 1N 2N 3N 0h WR+6 N/A N/A 1h WR+7 WR+6 N/A 2h WR+8 WR+7 WR+6 3h WR+9 WR+8 WR+7 4h WR+10 WR+9 WR+8 Other Reserved Reserved Reserved
3:2	0h RO	**Rsvd_3_2_DTR4:** Reserved
1:0	2h RW	**WRODTSTRT:** WR command to ODT assert delay. JEDEC requires ODT to be asserted on the same clock with the WR command. Dunit allows to pull-in by 1 clock in 2N mode and by 1-2 clocks in 3N mode. For most DIMM configurations, this register should be programmed to same value as tCMD. A value of tCMD - ODT_PULLIN can be used according to the table below which shows the ODT command assertion with respect to the WR command assertion. WRODTSTRT 1N 2N 3N 0h WR WR-1 WR-2 1h N/A WR WR-1 2h N/A N/A WR 3h Reserved Reserved Reserved

12.3.7 DPMC0 (DPMC0)—Offset 6h

DRAM Power Management Control 0

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 6h

Op Codes:
h - Read, h - Write

Default: 0B000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18:16	15:13	12:8	7:0
Default	0	0	0	0	1	0	1	1	0	0	0	0	0	0 0 0	0 0 0	0 0 0 0 0	0 0 0 0 0 0 0 0
Field	ENCORECLKGATE	ENCKTRI	ENPHYCLKGATE	REUTCLKGTDIS	Rsvd_27_DPMC0	BLMODE	DISPWRDN	CLKGTDIS	DYNSREN	Rsvd_22_DPMC0	PREAPWDEN	PCLSWKOK	Rsvd_19_DPMC0	PCLSTO	Rsvd_15_13_DPMC0	PMOP	SREDLY

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ENCORECLKGATE:** Enable Core Clock Gate During SR 0h - Core clock gating is disabled. 1h - Dunit enables the generic_clkreq_fsm during Self Refresh. The Dunit will re-enables the clocks upon Self Refresh exit.
30	0h RW	**ENCKTRI:** Enable CK/CKB TriState During PowerDown 0h - Disable CK/CKB Tristate During Powerdown. 1h - Enable CK/CKB Tristate During Powerdown. Note: This is an LPDDR feature only, for DDR3 bit should be set to 0.
29	0h RW	**ENPHYCLKGATE:** Enable PHY Clock Gate During SR 0h - PHY clock gating is disabled. 1h - Dunit will drive the dun_cck_clkreq signal low to turn off the 1x and 2x clock trees from the CCK unit to the DDRO PHY during Self Refresh. The Dunit will re-enables the clocks upon Self Refresh exit.
28	0h RW	**REUTCLKGTDIS:** REUT Clock Gate Disable 0h - REUT clock is gated when DCO.PMICTL is set to 0. 1h - REUT clock is upgated, overriding the DCO.PMICTL config bit. Note: The DCO.REUTLOCK bit overrides this bit.
27	1h RO	**Rsvd_27_DPMC0:** Reserved
26	0h RW	**BLMODE:** Burst Length Mode. Selects the DDR3 Burst Length mode: 0h - BL8 Fixed 1h - BL8/BC4 On-the-Fly Note: This bit should be zero for LPDDR2 and LPDDR3.
25	1h RW	**DISPWRDN:** Disable Power Down. Setting this bit to 1 will block CKE high-)low transitions. May be used by BIOS during init flow and should be set to 0 for functional mode. 0h - The Dunit dynamically controls the CKE pins to place the DRAM device in power down mode. 1h - The Dunit constantly drives the CKE pins high.
24	1h RW	**CLKGTDIS:** Clock Gating Disabled. Setting this bit to 0 allows a large number of internal Dunit clocks to be gated when there is no activity in order to save power. When set to 1, internal clock-gating is disabled. 0h - Enable 1h - Disable
23	0h RW	**DYNSREN:** Dynamic Self-Refresh Enable. Setting this bit to 1, enables automatic SR command to DRAM and PM message to DDRIO when the PMI bus is idle, all pending requests have been served and the and PMI status is less than 2, SREDLY has timed-out, and all JEDEC requirements are satisfied. This register may be changed by BIOS/ FW on-the-fly.
22	0h RO	**Rsvd_22_DPMC0:** Reserved
21	0h RW	**PREAPWDEN:** Send Precharge All Command to a Rank before PD-Enter. Setting this bit to 1 will allow sending a PREA command before PDE command. 0h - Disable 1h - Enable

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**PCLSWKOK:** Wake Allowed for Page Close Timeout. Setting this bit to 1 indicates the Dunit can send DRAM devices a PD-Exit command in order to close single bank if the page timer expired. Note: This bit applies only to cases where at least one other bank in the same rank is open but not timed-out. If all banks in the rank timed-out, a PD-Exit command will be sent regardless of this bit. Must be set to 0 during init/training mode. 0h - Disable 1h - Enable
19	0h RO	**Rsvd_19_DPMC0:** Reserved
18:16	0h RW	**PCLSTO:** Page Close Timeout Period. Specifies the time frame, in ns, from last access to a DRAM page until that page may be scheduled for closing (by sending a PRE command). 0h - Disable page close timer (init/training) 1h - Immediate page close 2h - 30-60 ns to page close 3h - 60-120 ns to page close 4h - 120-240 ns to page close 5h - 240-480 ns to page close 6h - 480-960 ns to page close 7h - 1-2 s to page close
15:13	0h RO	**Rsvd_15_13_DPMC0:** Reserved
12:8	0h RW	**PMOP:** SPID Power Mode Opcode. The PM Message ID the Dunit will send to DDRIO on ispid_pm_pm bus after SR Entry command to DRAM. This message defines the DDRIO power-mode during SR period. Value can be changed on-the-fly to allow different power modes (for example, deeper PM for S3 than for C6). Power saving and Entry/Exit latencies are described in the MODMEM HAS.
7:0	0h RW	**SREDLY:** Self-Refresh Entry delay. The delay, in core-clocks, between PMI idle (no pending requests and PMI status is less than 2) and SR Entry when Dunit is in Dynamic SR mode.

12.3.8 DPMC1 (DPMC1)—Offset 7h

DRAM Power Management Control 1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 7h

Op Codes:

h - Read, h - Write

Default: 00000011h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Rsvd_31_6_DPMC1	CMDTRIST	Rsvd_3_1_DPMC1	CSTRIST

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Rsvd_31_6_DPMC1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:4	1h RW	**CMDTRIST:** Tristate Command and Address Bus to DRAM 0h - CMD/ADDR are never tristated. 1h - CMD/ADDR are tristated only when all CKE are low. 2h - CMD/ADDR are tristated when no valid command. 3h - CMD/ADDR are tristated when no valid command but may never be tristated for less than 2 DRAM clocks. This mode is only valid when tCMD is set to 0h (1N mode).
3:1	0h RO	**Rsvd_3_1_DPMC1:** Reserved
0	1h RW	**CSTRIST:** Tristate Chip-Select 0 - Never tristate. 1 - TriState DRAM CS# pins from SRE to SRX+tXS. Note: DDRIO may tristate during SR so this adds on the boundries.

12.3.9 DRFC (DRFC)—Offset 8h

DRAM Refresh Control

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 8h

Op Codes:
h - Read, h - Write

Default: 03012CA7h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	1	0	0	1	1	1

Rsvd_31_27_DRFC	CUREFRATE	Rsvd_23_22_DFRC	REFDBTCLR	REFSKWDIS	Rsvd_19_18_DRFC	REFCNTMAX	Rsvd_15_DRFC	tREFI Refresh Period	REFWMPNC	REFWMHI	REFWMLO

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Rsvd_31_27_DRFC:** Reserved
26:24	3h RO	**CUREFRATE:** Current Refresh Rate This value is updated by the Dunit TQ Poll logic after executing a Mode Register Read Command to the DRAM Device Temperature Mode Register (MR4). 0h - 4x tREFI, Low temperature operating limit exceeded 1h - 4x tREFI 2h - 2x tREFI 3h - 1x tREFI ((= 85C) 4h - 0.5x tREFI (LPDDR3) 5h - 0.25x tREFI, do not de-rate AC timing 6h - 0.25x tREFI, de-rate AC timing 7h - 0.25x tREFI, High temperature operating limit exceeded Note: This is an LPDDR feature only.
23:22	0h RO	**Rsvd_23_22_DFRC:** Reserved
21	0h RW	**REFDBTCLR:** Clear Refresh Debit before SR Entry When this bit is set, if enough REF commands are pulled-in, Dunit will not send additional REF commands before SR Entry. 0h - Disabled 1h - Enabled
20	0h RW	**REFSKWDIS:** Refresh counters may be increased in 2 policies - skewed or simultaneously. 0h - counters are updated per rank every 1/4 tREFI period. 1h - all counters are updated every tREFI.

Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RO	**Rsvd_19_18_DRFC:** Reserved
17:16	1h RW	**REFCNTMAX:** Refresh Max tREFI Interval. The maximum interval between ant two REF commands per rank. JEDEC allows a maximum of 9 x tREFI intervals. 0h - 6 x tREFI 1h - 7 x tREFI 2h - 8 x tREFI 3h - 9 x tREFI Should not be changed after initial setting.
15	0h RO	**Rsvd_15_DRFC:** Reserved
14:12	2h RW	**tREFI Refresh Period**: Specifies the average time between sending REF commands to DRAM. The Dunit will guarantee that the average time is met, but maintains a certain degree of flexibility in the exact REF scheduling in order to increase overall performance. 0h - Refresh disabled 1h - Reserved for pre-silicon simulation 2h - 3.9 µs (Extended Temperature Range, 85-95°C) 3h - 7.8 µs (Normal Temperature Range, 0-85°C).
11:8	Ch RW	**REFWMPNC:** Refresh Panic Watermark. When the refresh debit counter, per rank, is greater than this value, the Dunit will send a REF command even if there are some pending requests and regardless of the PMI status level. See DDR3 spec for Refresh Postponing/Pulling-In flexibility. May be changed to functional value after init sequence. Value should be greater than, or equal, to REFWMHI. 0h - Reserved 1h - Reserved 2h - Reserved 3h - Reserved 4h - Reserved 5h - Reserved 6h - Reserved 7h - Postpone 2 REF commands 8h - Postpone 3 REF commands 9h - Postpone 4 REF commands Ah - Postpone 5 REF commands Bh - Postpone 6 REF commands Ch - Postpone 7 REF commands Dh - Postpone 8 REF commands Others - Reserved
7:4	Ah RW	**REFWMHI:** Refresh High Watermark. When the refresh debit counter, per rank, is greater than this value, the Dunit will send a REF command even if there are some pending requests to the rank but not if the PMI status is equal to 3. See DDR3 spec for Refresh Postponing/Pulling-In flexibility. May be changed to functional value after init sequence. Value should be greater than, or equal, to REFWMLO. 0h - Reserved 1h - Reserved 2h - Reserved 3h - Reserved 4h - Reserved 5h - Reserved 6h - Reserved 7h - Postpone 2 REF commands 8h - Postpone 3 REF commands 9h - Postpone 4 REF commands Ah - Postpone 5 REF commands Bh - Postpone 6 REF commands Ch - Postpone 7 REF commands Dh - Postpone 8 REF commands Others - Reserved
3:0	7h RW	**REFWMLO:** Opportunistic Refresh Watermark. When the refresh debit counter, per rank, is greater than this value, the Dunit will send a REF command only if there are no pending requests to the rank and the PMI status is less than 3. See DDR3 spec for Refresh Postponing/Pulling-In flexibility. May be changed to functional value after init sequence. 0h - Reserved 1h - Reserved 2h - Reserved 3h - Reserved 4h - Reserved 5h - Reserved 6h - Reserved 7h - Postpone 2 REF commands 8h - Postpone 3 REF commands 9h - Postpone 4 REF commands Ah - Postpone 5 REF commands Bh - Postpone 6 REF commands Ch - Postpone 7 REF commands Dh - Postpone 8 REF commands Others - Reserved

12.3.10 DSCH (DSCH)—Offset 9h

DRAM Scheduler Control

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 9h

Op Codes:
h - Read, h - Write

Default: 00071108h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0

Fields (bit 31 to bit 0): Rsvd_31_19_DSCH | IPREQMAX | Rsvd_15_13_DSCH | NEWBYPDIS | Rsvd_11_10_DSCH | OOOST3DIS | OOODIS | Rsvd_7_5_DSCH | OOOAGETRH

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Rsvd_31_19_DSCH:** Reserved
18:16	7h RW	**IPREQMAX:** Maximal number of In-Process Requests stored in the Dunit. Number of pending requests = IPREQMAX+1; Value may be changed after init/training when PMI is idle.
15:13	0h RO	**Rsvd_15_13_DSCH:** Reserved
12	1h RW	**NEWBYPDIS:** Disable New Request Bypass. Setting this bit to 0 will allow a new request to bypass the normal Dunit internal arbiter when there are no pending commands. 0h - Enable New Request Bypass. 1h - Disable New Request Bypass.
11:10	0h RO	**Rsvd_11_10_DSCH:** Reserved
9	0h RW	**OOOST3DIS:** Out-of-Order Disabled whenPMI status is 3. Valid only if OOODIS is 0; 0 - Remain OOO if status goes up to 3 1 - Disable OOO if status goes to 3 May be changed after init/training flow.
8	1h RW	**OOODIS:** Disable Out-of-Order . 0h - OOO enabled. 1h - OOO disabled. Should be disabled during init/training and can be enabled for functional mode.
7:5	0h RO	**Rsvd_7_5_DSCH:** Reserved
4:0	08h RW	**OOOAGETRH:** Out-of-Order Aging Theshold. Number of PMI requests that can bypass any pending request before OOO will be disabled. This mechanism prevents starvation of pending commands.

12.3.11 DCAL (DCAL)—Offset Ah

DRAM Calibration Control

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + Ah

Op Codes:
h - Read, h - Write

Default: 00001300h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 1 1	0 0 0 0	0 0 0 0

MRRDATA	TQPOLLPER	TQPOLLEN	Rsvd_19_DCAL	TQPOLLRS	TQPOLLSTRT	ZQCALSTRT	ZQCALTYPE	SRXZQCL	Rsvd_11_DCAL	ZQCINT	Rsvd_7_0_DCAL

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MRRDATA:** MRR Data This field contains the data of the last DRAM Mode Register Read (MRR) issued thru message opcode 68h or from a TQ Poll. It is over-written with each MRR command. Note: This is an LPDDR feature only.
23:21	0h RW/P	**TQPOLLPER:** TQ Poll Period 0h - 1 x the current Refresh Period 1h - 2 x the current Refresh Period 2h - 4 x the current Refresh Period 3h - 8 x the current Refresh Period 4h - 16 x the current Refresh Period 5h - 32 x the current Refresh Period 6h - 64 x the current Refresh Period 7h - 128 x the current Refresh Period Note: This is an LPDDR feature only.
20	0h RW/P	**TQPOLLEN:** TQ Poll Enable 0 - Disables periodic TQ polling 1 - Enables periodic TQ polling Note: This is an LPDDR feature only.
19	0h RO	**Rsvd_19_DCAL:** Reserved
18:17	0h RW/P	**TQPOLLRS:** TQ Poll RS This bit selects which rank to poll the LPDDR2 DRAMs internal MR4 register. The assumption is that the temperature will be similar for any rank, and thus polling only a single memory device in the package is sufficient. 00 - Select Rank 0 to poll from 01 - Select Rank 1 to poll from 10 - Select Rank 2 to poll from 11 - Select Rank 3 to poll from Note: This is an LPDDR feature only.
16	0h RW/P	**TQPOLLSTRT:** TQ Poll Start Set this bit to 1 to start a TQPoll. This bit will remain a 1 until the TQPoll process is complete, then it will return to 0. 0 - TQ Poll is done 1 - TQ Poll has started and is in progress Note: This is an LPDDR feature only.
15	0h RW/P	**ZQCALSTRT:** ZQ Calibration Start Set this bit to 1 to start the ZQ calibration sequence. This bit will remain a 1 until the ZQ calibration is complete, then it will return to 0. 0 - ZQ calibration is done 1 - ZQ calibration has started and is in progress
14	0h RW/P	**ZQCALTYPE:** ZQ Calibration Type 0 - Short Calibration 1 - Long Calibration
13:12	1h RW/P	**SRXZQCL:** ZQ Calibration Long After SR Exit Control 0h - ZQCL commands after SRX are sent in parallel. 1h - ZQCL commands are sent serially to ranks (not used). 2h - No ZQCL is sent after SR Exit (for Debug only). 3h Reserved.
11	0h RO	**Rsvd_11_DCAL:** Reserved
10:8	3h RW/P	**ZQCINT:** ZQ Calibration Short Interval. The time interval, in ms, between ZQCS commands to a DRAM device. ZQCS commands are sent to a single DRAM device and commands are distributed and non-overlapping in the interval. 0h - Disabled 1h - 62s (for pre-silicon simulation only) 2h - 31ms 3h - 63ms 4h - 126ms Others - Reserved May be changed on-the-fly in response to thermal events.
7:0	0h RO	**Rsvd_7_0_DCAL:** Reserved

12.3.12 DRMC (DRMC)—Offset Bh

DRAM Reset Management Control

Access Method

Type: Message Bus Register (Size: 32 bits) | **Offset:** [Port: 0x01] + Bh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:17	Bit 16	Bits 15:13	Bit 12	Bits 11:8	Bits 7:5	Bit 4	Bits 3:0
Rsvd_31_17_DRMC	COLDWAKE	Rsvd_15_13_DRMC	ODTMODE	ODTVAL	Rsvd_7_5_DRMC	CKEMODE	CKEVAL

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Rsvd_31_17_DRMC:** Reserved
16	0h RW	**COLDWAKE:** BIOS should set this bit to 1 before sending WAKE command to Dunit after Cold Reset. For S3 Exit, or any other mode in which the DRAM is in SR, this bit must be set to 0.
15:13	0h RO	**Rsvd_15_13_DRMC:** Reserved
12	0h RW	**ODTMODE:** ODT Control Mode 0h - Dunit. 1h - SW override.
11:8	0h RW	**ODTVAL:** When ODTMODE is set to 1, ODT pins to DRAM are overridden by ODTVAL. Used only during init flow by BIOS.
7:5	0h RO	**Rsvd_7_5_DRMC:** Reserved
4	0h RW	**CKEMODE:** CKE Control Mode 0h - Dunit. 1h - SW override.
3:0	0h RW	**CKEVAL:** When CKEMODE is set to 1, CKE pins to DRAM are overridden by CKEVAL. Used only during init flow by BIOS.

12.3.13 PMSTS (PMSTS)—Offset Ch

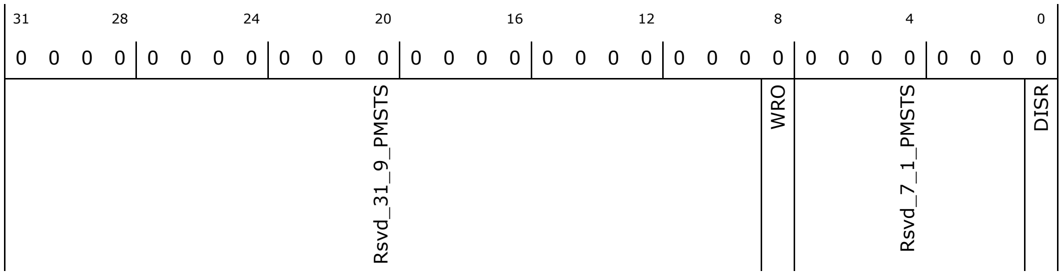
Power Management Status

Access Method

Type: Message Bus Register (Size: 32 bits) | **Offset:** [Port: 0x01] + Ch

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Rsvd_31_9_PMSTS:** Reserved
8	0h RW/P	**WRO:** Warm Reset Occurred. Set by the Punit whenever a Reset Warn is received, and cleared by powergood=0. 0h: No Warm Reset occurred. 1h: Warm Reset occurred. BIOS Requirement. BIOS can check and clear this bit whenever executing POST code. This way BIOS knows that if the bit is set, then DISR indicates whether DRAM entered Self-Refresh.
7:1	0h RO	**Rsvd_7_1_PMSTS:** Reserved
0	0h RW/P	**DISR:** DRAM In Self-Refresh. Set by Dunit hardware after Channel is placed in self refresh as a result of a Power State or a Reset Warn sequence. Cleared by Dunit hardware before starting Channel 0 self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 - DRAM not guaranteed to be in Self-Refresh. 1 - DRAM in Self-Refresh.

12.3.14 DCO (DCO)—Offset Fh

DRAM Control Operation

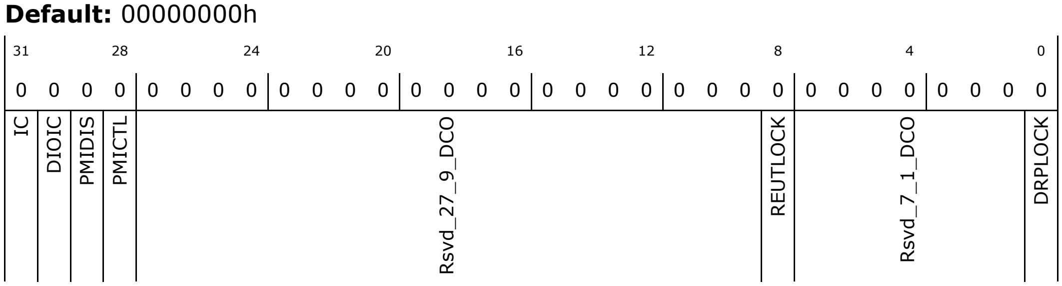
Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + Fh

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IC:** Dunit Initialization Complete. This bit should be set by BIOS after Dunit programming is complete and Dunit is ready to accept PMI requests and perform DRAM maintenance operations.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO	**DIOIC:** Status indication that DDRIO initialization is complete. Reflects ospid_init_complete.
29	0h RW	**PMIDIS:** Disable PMI interface. When set to 1, Following PMI signals are disabled from both Bunit and REUT: PMI Request Irdy, PMI Request Trdy, PMI DataBD Irdy, PMI DataBD Trdy, PMI DataBD BE, PMI DataDB Irdy, PMI DataDB Trdy
28	0h RW	**PMICTL:** PMI Control Select. 0h - PMI is owned by Bunit 1h - PMI is owned by REUT Whenever this bit is toggled, Dunit will flush all pending DRAM requests from previous owner before it accepts requests from new owner. This bit is also used when REUT is disabled in order to gracefully flush pending request and putting DRAM into IDLE state before sending MRS commands in functional mode.
27:9	0h RO	**Rsvd_27_9_DCO:** Reserved
8	0h RW/P/L	**REUTLOCK:** After this bit is set to 1, all REUT is clock gated and locked and cannot be used. REUTLOCK can be set only once, and will only reset when powergood = 0.
7:1	0h RO	**Rsvd_7_1_DCO:** Reserved
0	0h RW/P/L	**DRPLOCK:** After this bit is set to 1, all DRP bits are locked and cannot be written again. DRPLOCK can be written only once. DRPLOCK and DRP bit values will only reset when powergood = 0.

12.3.15 DTRC (DTRC)—Offset 10h

DRAM Training Control

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 10h

Op Codes:
h - Read, h - Write

Default: 00000000h

```
31       28          24          20          16          12          8           4           0
0  0  0  0 | 0  0  0  0 | 0  0  0  0 | 0  0  0  0 | 0  0  0  0 | 0  0  0  0 | 0  0  0  0 | 0  0  0  0
```

Rsvd_31_23_DTRC	CATSTATUS	CATFAIL	CATMASK	CATLPCNT	Rsvd_11_DTRC	CATRS	CATSTART	Rsvd_7_6_DTRC	BLKPHASEB	BLKIPRQNF	BLKPRE	BLKACT	BLKWR	BLKRD

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Rsvd_31_23_DTRC:** Reserved
22:17	0h RO	**CATSTATUS:** CA Training Status
16	0h RO	**CATFAIL:** CA Training Fail 0 - No mismatch between CA and DQ 1 - Mismatch between CA and DQ

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW/L	**CATMASK:** Command/Address Training Mask Mask data for comparison. 0h - No Mask 1h - Mask out data from byte[1] and byte[4] 2h - Mask out data from upper 32bits 3h - Mask both bytes and upper 32bits
13:12	0h RW/L	**CATLPCNT:** Command/Address Training Loop Count
11	0h RO	**Rsvd_11_DTRC:** Reserved
10:9	0h RW/L	**CATRS:** Command/Address Training Rank Select 0h - Rank 0 (DIMM0) is selected 1h - Rank 1 (DIMM0) is selected 2h - Rank 2 (DIMM1) is selected 3h - Rank 3 (DIMM1) is selected
8	0h RW/P/L	**CATSTART:** Command/Address Training Start Set this bit to 1 to start CA training. This bit will remain a 1 until CA training is complete, then it will return to 0. 0 - CA Training is done 1 - CA Training has started and is in progress Note: This is an LPDDR feature only.
7:6	0h RO	**Rsvd_7_6_DTRC:** Reserved
5	0h RW/L	**BLKPHASEB:** Block All PhaseB Commands. Dunit operates at coreclock which is half the frequency of the DRAM clock. When this bit is set, only one command can be scheduled each coreclock. This bit may be used for DFX applications.
4	0h RW/L	**BLKIPRQNF:** Block all IP Requests until Queue is Full. When this bit is set to 1, all Dunit are stalled until the IP pool is full. This bit is self-clearing, and once asserted, writing 0 has no impact. The IPREQ pool is only reopened when the number of pending requests reaches DSCH.IPREQMAX+1.
3	0h RW/L	**BLKPRE:** Block Precharge Commands to DRAM 0 - No Block 1 - Block
2	0h RW/L	**BLKACT:** Block Activate Commands to DRAM 0 - No Block 1 - Block
1	0h RW/L	**BLKWR:** Block Write Commands to DRAM 0 - No Block 1 - Block
0	0h RW/L	**BLKRD:** Block Read Commands to DRAM 0 - No Block 1 - Block

12.3.16 DCBR (DCBR)—Offset 12h

DRAM CB Register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 12h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits	31:9	8	7:2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0	0	0
Field	Rsvd_31_9_DCBR	SRXNRQDIS	Rsvd_7_2_DCBR	DMINV	PHSINV

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Rsvd_31_9_DCBR:** Reserved
8	0h RW	**SRXNRQDIS:** Disable Accepting Requests During Self Refresh Exit 0 - Load PMI requests to Dunit in SR Exit tXSDLL and ZQCoper period 1 - Load PMI requests only after tXSDLL and ZQCoper are complete
7:2	0h RO	**Rsvd_7_2_DCBR:** Reserved
1	0h RW	**DMINV:** Invert DRAM Data Mask 0 - Do not invert DRAM data mask 1 - Invert DRAM data mask
0	0h RW	**PHSINV:** Core/SPID CDC phase control invert. Backup inverter for internal phase indicator in Dunit.

12.3.17 DSTAT (DSTAT)—Offset 20h

Dunit Status

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + 20h

Op Codes:
h - Read, h - Write

Default: 0000000Ah

Bits	31	30:28	27:24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7:5	4:0
Default	0	0 0 0	0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0 0	0 1 0 1 0
Field	Rsvd_31_DSTAT	MAXMEM	Rsvd_27_24_DSTAT	REFOPR3	REFOPR2	REFOPR1	REFOPR0	REFDBT3	REFDBT2	REFDBT1	REFDBT0	IPRQVLD7	IPRQVLD6	IPRQVLD5	IPRQVLD4	IPRQVLD3	IPRQVLD2	IPRQVLD1	IPRQVLD0	Rsvd_7_5_DSTAT	MNT_STATE

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rsvd_31_DSTAT:** Reserved
30:28	0h RO	**MAXMEM:** Reflects the fus_dun_max_supported_memory fuse
27:24	0h RO	**Rsvd_27_24_DSTAT:** Reserved
23	0h RO	**REFOPR3:** Rank 3 Refresh Dept is greater than DRFC.REFWMLO
22	0h RO	**REFOPR2:** Rank 2 Refresh Dept is greater than DRFC.REFWMLO
21	0h RO	**REFOPR1:** Rank 1 Refresh Dept is greater than DRFC.REFWMLO
20	0h RO	**REFOPR0:** Rank 0 Refresh Dept is greater than DRFC.REFWMLO

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**REFDBT3:** Rank 3 has a Refresh Dept
18	0h RO	**REFDBT2:** Rank 2 has a Refresh Dept
17	0h RO	**REFDBT1:** Rank 1 has a Refresh Dept
16	0h RO	**REFDBT0:** Rank 0 has a Refresh Dept
15	0h RO	**IPRQVLD7:** IPREQ Entry 7 contains a valid request.
14	0h RO	**IPRQVLD6:** IPREQ Entry 6 contains a valid request.
13	0h RO	**IPRQVLD5:** IPREQ Entry 5 contains a valid request.
12	0h RO	**IPRQVLD4:** IPREQ Entry 4 contains a valid request.
11	0h RO	**IPRQVLD3:** IPREQ Entry 3 contains a valid request.
10	0h RO	**IPRQVLD2:** IPREQ Entry 2 contains a valid request.
9	0h RO	**IPRQVLD1:** IPREQ Entry 1 contains a valid request.
8	0h RO	**IPRQVLD0:** IPREQ Entry 0 contains a valid request.
7:5	0h RO	**Rsvd_7_5_DSTAT:** Reserved
4:0	0Ah RO	**MNT_STATE:** Dunit Maintenance Internal State

12.3.18 PGTBL (PGTBL)—Offset 21h

DRAM Page Table Status

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 21h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PGTBLVLD

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**PGTBLVLD:** Reflects the open page table entries (4 Ranks x 8 Banks)

12.3.19 MISRCCCLR (MISRCCCLR)—Offset 31h

MISR CMD/CTRL Clear

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + 31h

Op Codes:
h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

MISRCCCLR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h WO	**MISRCCCLR (MISRCCCLR):** Writing any value to this address will reset the MISRCC Signature register value to all Fs.

12.3.20 MISRDDCLR (MISRDDCLR)—Offset 32h

MISR DM/DQ Clear

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + 32h

Op Codes:
h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

MISRDDCLR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h WO	**MISRDDCLR (MISRDDCLR):** Writing any value to this address will reset the MISRDD Signature register value to all Fs.

12.3.21 MISRCCSIG (MISRCCSIG)—Offset 34h

MISR CMD/CTRL Signature

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 34h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SIG																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO	**SIG:** MISR Signature: CMD/CTRL

12.3.22 MISRDDSIG (MISRDDSIG)—Offset 35h

MISR DM/DQ Signature

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 35h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SIG																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO	**SIG:** MISR Signature: DM/DQ

12.3.23 MISRECCSIG (MISRECCSIG)—Offset 37h

MISR ECC Signature

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 37h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SIG																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO	**SIG:** MISR Signature ECC

12.3.24 SSKPD0 (SSKPD0)—Offset 4Ah

Sticky Scratchpad 0

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + 4Ah

Op Codes:
h - Read, h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VAL																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/P	**VAL:** General Purpose Scratchpad. May be used for BIOS for data storage. Value is preserved in warm-reset.

12.3.25 SSKPD1—Offset 4Bh

Sticky Scratchpad 1

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + 4Bh

Op Codes:
h - Read, h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VAL																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/P	**VAL:** General Purpose Scratchpad. May be used for BIOS for data storage. Value is preserved in warm-reset.

12.3.26 BONUS0 (BONUS0)—Offset 50h

Bonus Register 0

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x01] + 50h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits	31:7	6	5:4	3	2	1	0
Default	0000 0000 0000 0000 0000 0000 0	0	00	0	0	0	0
Field	Rsvd_31_4_BONUS0	LPDDRCMDTRI	MRRCMDDLY	CATBUGFIX	SLOWPDXEN	PERFMONEN	DISEARLYSRX

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Rsvd_31_7_BONUS0 (Rsvd_31_4_BONUS0):** Reserved
6	0h RW	**LPDDRCMDTRI:** Enable LPDDR CMD Tri-Stating
5:4	0h RW	**MRRCMDDLY:** Adding addtional delay on MRR followed by read and write command
3	0h RW	**CATBUGFIX:** This is a defeature bit for CA training and should be set to 0 for normal operation.
2	0h RW	**SLOWPDXEN:** This bit is for enabling slow powerdown exit.
1	0h RW	**PERFMONEN:** This bit is for enabling performance monitor.
0	0h RW	**DISEARLYSRX:** This bit is for enabling early SR exit.

12.3.27 BONUS1—Offset 51h

Bonus Register 1

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x01] + 51h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BONUS1

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BONUS1:** Bonus Register 1 (This register is reserved for ECO).

12.3.28 DECCCTRL (DECCCTRL)—Offset 60h

DECC Control Register

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + 60h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Rsvd_31_18_DECCCTRL | ENCBGEN | Rsvd_16_DECCCTRL | CBOV | CLRSBECNT | SYNSEL | CBOEN | DBEEN | SBEEN

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Rsvd_31_18_DECCCTRL:** Reserved
17	0h RW	**ENCBGEN:** DFx: Enable Generation of ECC check bits 0 - Disable check bit generation 1 - Enable check bit generation
16	0b RO	**Rsvd_16_DECCCTRL:** Reserved
15:8	00h RW	**CBOV:** DFx: Check Bit Override (Host Defined Value)
7	00h RW	**CLRSBECNT:** DFx: Clear SERR counter 0 - Allow single bit error count to increment 1 - Clear single bit error count
6:5	00h RW	**SYNSEL:** DFx: Select syndrome bits from 256b read data path. 0h - Selects syndrome bits from read data [63:0] 1h - Selects syndrome bits from read data [127:64] 2h - Selects syndrome bits from read data [191:128] 3h - Selects syndrome bits from read data [255:192]

Bit Range	Default & Access	Field Name (ID): Description
4:2	000h RW	**CBOEN:** DFx: Enable Check Bit Override on 256b write data path 0xx Host generated check bits disabled. 0h - Reserved 1h - Reserved 2h - Reserved 3h - Reserved 4h - Assert Host generated check bits on write data [63:0] 5h - Assert Host generated check bits on write data [127:64] 6h - Assert Host generated check bits on write data [191:128] 7h - Assert Host generated check bits on write data [255:192]
1	0h RW	**DBEEN:** Enable Double Bit Error Detect 0 - Disable double bit error detect 1 - Enable double bit error detect
0	0h RW	**SBEEN:** Enable Single Bit Error Detect and Correct 0 - Disable single bit error detect and correct 1 - Enable single bit error detect and correct

12.3.29 DECCSBECNT (DECCSBECNT)—Offset 62h

DECC Single Bit Error Count Register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 62h

Op Codes:
h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

ECCSBECNT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**ECCSBECNT:** ECC Single Bit Error Count Write a 1 to the CLRSBECNT bit in the DECCCTRL register to clear this register

12.3.30 DFUSESTAT (DFUSESTAT)—Offset 70h

Dunit fuse status register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 70h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FUSESTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**FUSESTAT:** Dunit fuse bits are captured into this register and is available for read [0] fus_dun_ecc_dis. [3:1] fus_dun_max_supporte_memory[2:0]. [5:4] fus_dun_max_devden[1:0] [6] fus_dun_dimm2_dis [7] fus_dun_rank2_dis [8] fus_dun_ooo_dis [9] fus_dun_memx8_dis [10] fus_dun_memx16_dis [11] fus_dun_bc4_dis [12] fus_dun_1n_dis [13] fus_dun_dq_scrambler_dis [15:14] Rsvd [16] fus_dun_32bit_dram_ifc [31:17] Rsvd

12.3.31 DSCRMSEED (DSCRMSEED)—Offset 80h

Dynamic data scrambler seed register ERRATA Reading this register returns the bit fields in reverse order SCRMSEED[31:14], 13'h0, SCRMDIS[0]

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 80h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCRMDIS | Rsvd_30_18_SCRMSEED | SCRMSEED

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**SCRMDIS:** Scrambler Disable 0 - Enables scrambler 1 - Disables scrambler Note: This bit has no impact with Scrambler is disabled by fuse
30:18	0h RO	**Rsvd_30_18_SCRMSEED:** Reserved
17:0	0h RW	**SCRMSEED:** Holds 18 bit scrambler seed value used to feed into LFSR array matrix.

12.3.32 DSCRMLO (DSCRMLO)—Offset 81h

Dynamic data scrambler pattern low register.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 81h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCRMLO

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SCRMLO:** Holds 31:0 bits of scrambler parrem value used to XOR with LFSR array output.

12.3.33 DSCRMHI (DSCRMHI)—Offset 82h

Dynamic data scrambler pattern high register.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + 82h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCRMHI

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SCRMHI:** Holds 63:32 bits of scrambler parrem value used to XOR with LFSR array output.

12.3.34 PMSEL0 (PMSEL0)—Offset E0h

Performance Monitor Event Select 0

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + E0h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DPERFENST	Rsvd_31_14_PMSEL0																EVTMSK0							Rsvd_7_4_PMSEL0				EVTID			

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**DPERFENST:** Dunit Perfmon Enable Status. Reflects DFX Perfmon enable. 0 - Dunit perfmon is disabled. 1 - Dunit perfmon is enabled
30:14	0h RO	**Rsvd_31_14_PMSEL0:** Reserved
13:8	0h RW	**EVTMSK0:** Event Mask
7:4	0h RO	**Rsvd_7_4_PMSEL0:** Reserved
3:0	0h RW	**EVTID:** Event ID

12.3.35 PMSEL1 (PMSEL1)—Offset E1h

Performance Monitor Event Select 1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + E1h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd_31_14_PMSEL1	EVTMSK1	Rsvd_7_4_PMSEL1	EVTID

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Rsvd_31_14_PMSEL1:** Reserved
13:8	0h RW	**EVTMSK1:** Event Mask
7:4	0h RO	**Rsvd_7_4_PMSEL1:** Reserved
3:0	0h RW	**EVTID:** Event ID

12.3.36 PMSEL2—Offset E2h

Performance Monitor Event Select 2

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x01] + E2h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd_31_14_PMSEL2	EVTMSK2	Rsvd_7_4_PMSEL2	EVTID

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Rsvd_31_14_PMSEL2:** Reserved
13:8	0h RW	**EVTMSK2:** Event Mask
7:4	0h RO	**Rsvd_7_4_PMSEL2:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**EVTID:** Event ID

12.3.37 PMSEL3—Offset E3h

Performance Monitor Event Select 3

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + E3h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits	31:14	13:8	7:4	3:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0	0 0 0 0
Field	Rsvd_31_14_PMSEL3	EVTMSK3	Rsvd_7_4_PMSEL3	EVTID

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Rsvd_31_14_PMSEL3:** Reserved
13:8	0h RW	**EVTMSK3:** Event Mask
7:4	0h RO	**Rsvd_7_4_PMSEL3:** Reserved
3:0	0h RW	**EVTID:** Event ID

12.3.38 PMAUXMAX (PMAUXMAX)—Offset E8h

Performance Monitor Address Limit High

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + E8h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:28	Bits 27:0
Rsvd_31_28_PMAUXMAX	MAX

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Rsvd_31_28_PMAUXMAX:** Reserved
27:0	0h RW	**MAX:** Maximal address or maximal latency count. When PMSEL0.EVTID == Ch, this register should be initialized to 0h and at the end of the test bits [11:0] will contain the max latency. When PMSEL0/1/2.EVTID == 5h, this register should be initialized to the highest address the Perfmon test will cover. Bits [27:0] of this register correspond to the physical address bits [32:8].

12.3.39 PMAUXMIN—Offset E9h

Performance Monitor Address Limit Low

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + E9h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:28	Bits 27:0
Rsvd_31_28_PMAUXMIN	MIN

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Rsvd_31_28_PMAUXMIN:** Reserved
27:0	0h RW	**MIN:** Minimal address or minimal latency count. When PMSEL0.EVTID == Ch, this register should be initialized to FFFh and at the end of the test bits [11:0] will contain the min latency. When PMSEL0/1/2.EVTID == 5h, this register should be initialized to the lowest address the Perfmon test will cover. Bits [27:0] of this register correspond to the physical address bits [32:8].

12.3.40 PMAUX (PMAUX)—Offset EAh

Performance Monitor Aux

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x01] + EAh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:11	Bits 10:8	Bits 7:4	Bits 3:0
Rsvd_31_11_PMAUX	PMAUX2	PMAUX1	PMAUX0

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Rsvd_31_11_PMAUX:** Reserved
10:8	0h RW	**PMAUX2:** Additional mask and configuration. See Perfmon Guide.
7:4	0h RW	**PMAUX1:** Additional mask and configuration. See Perfmon Guide.
3:0	0h RW	**PMAUX0:** Additional mask and configuration. See Perfmon Guide.

13 SoC Transaction Router

The SoC Transaction Router is a central hub that routes transactions between the CPU cores, graphics controller, IO and the memory controller. In general, it handles:

- CPU Core Interface: Requests for CPU Core-initiated memory and IO read and write operations and processor-initiated message-signaled interrupt transactions
- Device MMIO and PCI configuration routing
- Buffering and memory arbitration
- PCI Config and MMIO accesses to host device (0/0/0)

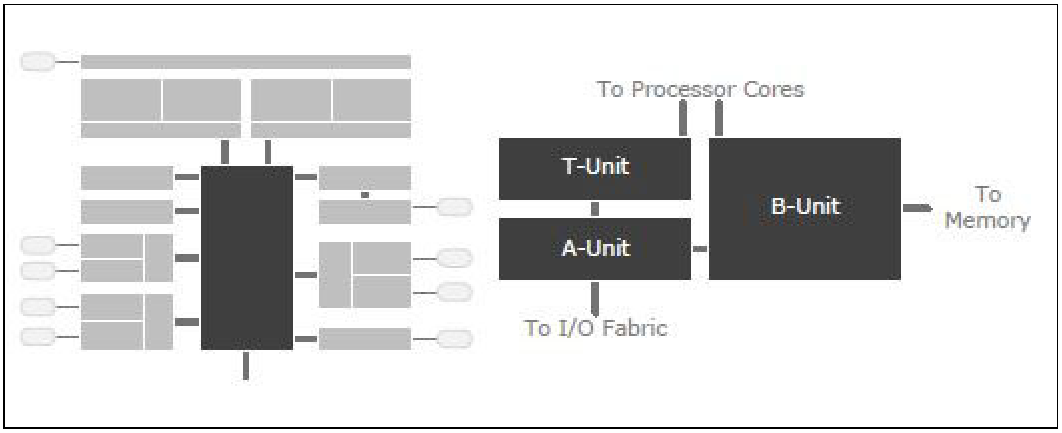
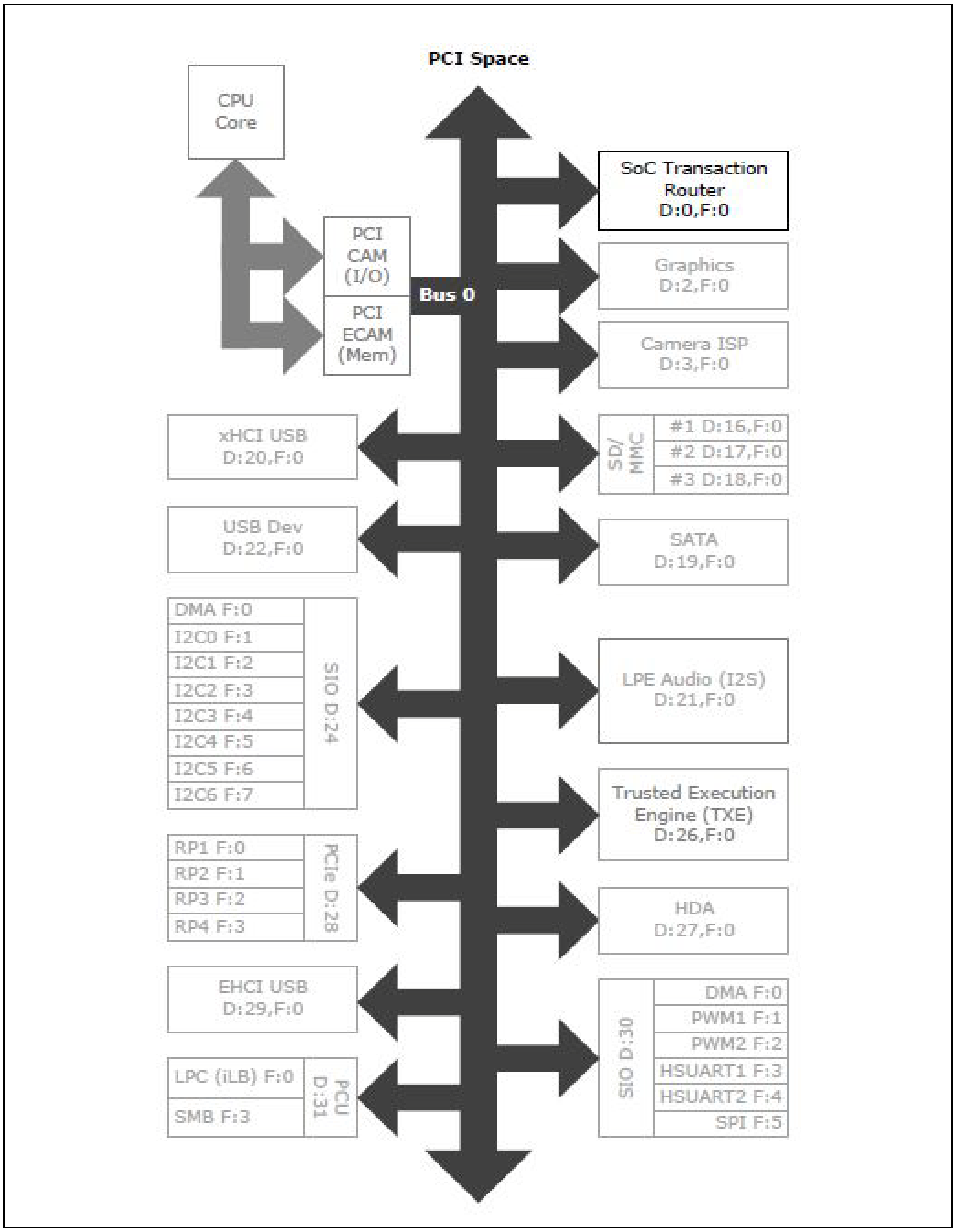


Figure 90. Soc Transaction Router Register Map



§

13.1 Transaction Router A-Unit Message Registers

Table 159. Summary of A-Unit Message Bus Registers—Port 0x00

Offset	Register Name (Register Symbol)	Default Value
10–10h	“ACF8—Offset 10h” on page 324	00000000h
52–52h	“ADBGERRLOG—Offset 52h” on page 325	00000000h

13.1.1 ACF8—Offset 10h

A-Unit Configuration CF8 Value (ACF8) The A-Unit CF8 (PCI Configuration Address Register) is made available for save/restore purposes. This register is saved and restored by the Punit during S0iX transitions in order to ensure proper handling of a possible subsequent CFC transaction after returning from standby or hibernate state. This is carried over from Aunit implementation in LNC.

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x00] + 10h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CFG_MAP_EN	CF8_RESERVED_0							BUS_NUM								DEVICE_NUM					FUNCTION_NUM			DBL_WD						CF8_RESERVED_1	

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CFG_MAP_EN:** Configuration Space Mapping Enable: This bit enables Configuration Space mapping. The value set by full-dword writes to I/O address CF8
30:24	0h RW	**CF8_RESERVED_0:** Reserved. The value set by full-dword writes to I/O address CF8
23:16	0h RW	**BUS_NUM:** Bus Number: This is the target Bus Number of the resulting Configuration request. The value set by full-dword writes to I/O address CF8
15:11	0h RW	**DEVICE_NUM:** Device Number: This is the target Device Number of the resulting Configuration request. The value set by full-dword writes to I/O address CF8
10:8	0h RW	**FUNCTION_NUM:** Function Number: This is the target Function Number of the resulting Configuration request. The value set by full-dword writes to I/O address CF8
7:2	0h RW	**DBL_WD:** Double Word: This is the target dword of the resulting Configuration request. The value set by full-dword writes to I/O address CF8
1:0	0h RW	**CF8_RESERVED_1:** Reserved. This field should be always set to 2'b00. The value set by full-dword writes to I/O address CF8

13.2 SoC Transaction Router PCI Config Access IO Registers

SoC Transaction Router PCI Config Access IO Registers

Table 160. Summary of PCI Configuration Space Access I/O Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
CF8–CF8h	1	“ACF8—Offset CF8h” on page 327	00000000h
CFC–CFFh	4	“ACFC—Offset CFCh” on page 328	00000000h

13.2.1 ACF8—Offset CF8h

A-Unit Configuration CF8 Value (ACF8) The A-Unit CF8 (PCI Configuration Address Register) is made available for save/restore purposes. This register is saved and restored by the Punit during S0iX transitions in order to ensure proper handling of a possible subsequent CFC transaction after returning from standby or hibernate state. This is carried over from Aunit implementation in LNC.

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: CF8h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

CFG_MAP_EN | CF8_RESERVED_0 | BUS_NUM | DEVICE_NUM | FUNCTION_NUM | DBL_WD | CF8_RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CFG_MAP_EN:** Configuration Space Mapping Enable: This bit enables Configuration Space mapping. The value set by full-dword writes to I/O address CF8
30:24	0h RW	**CF8_RESERVED_0:** Reserved. The value set by full-dword writes to I/O address CF8
23:16	0h RW	**BUS_NUM:** Bus Number: This is the target Bus Number of the resulting Configuration request. The value set by full-dword writes to I/O address CF8
15:11	0h RW	**DEVICE_NUM:** Device Number: This is the target Device Number of the resulting Configuration request. The value set by full-dword writes to I/O address CF8
10:8	0h RW	**FUNCTION_NUM:** Function Number: This is the target Function Number of the resulting Configuration request. The value set by full-dword writes to I/O address CF8
7:2	0h RW	**DBL_WD:** Double Word: This is the target dword of the resulting Configuration request. The value set by full-dword writes to I/O address CF8
1:0	0h RW	**CF8_RESERVED_1:** Reserved. This field should be always set to 2'b00. The value set by full-dword writes to I/O address CF8

13.2.2 ACFC—Offset CFCh

A-Unit Configuration CFC Value (ACFC) The A-Unit CFC (PCI Configuration Data Port).

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: CFCh

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CFC_VAL																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**CFC_VAL:** CFC Value: The value set by full-dword writes to I/O address CFC

13.3 Transaction Router B-Unit Message Registers

Table 161. Summary of B-Unit Message Bus Registers—Port 0x03

Offset	Register Name (Register Symbol)	Default Value
8–8h	"BBANKMASK—Offset 8h" on page 330	0000000Eh
9–9h	"BROWMASK—Offset 9h" on page 331	00FFFFFEh
A–Ah	"BRANKMASK—Offset Ah" on page 332	00000004h
1A–1Ah	"BIMRDATA—Offset 1Ah" on page 333	00000000h
1B–1Bh	"BPMRVCTL—Offset 1Bh" on page 334	00000000h
23–23h	"BNOCACHE—Offset 23h" on page 335	00000000h
24–24h	"BNOCACHECTL—Offset 24h" on page 336	00000000h
25–25h	"BMBOUND—Offset 25h" on page 337	40000000h
26–26h	"BMBOUND_HI—Offset 26h" on page 337	80000000h
27–27h	"BECREG—Offset 27h" on page 338	00000000h
2E–2Eh	"BSMMRRL—Offset 2Eh" on page 339	00000000h
2F–2Fh	"BSMMRRH—Offset 2Fh" on page 340	00000000h
30–30h	"BC0AHASHCFG—Offset 30h" on page 340	00000000h
3E–3Eh	"BTHCTRL—Offset 3Eh" on page 342	00000001h
3F–3Fh	"BTHMASK—Offset 3Fh" on page 343	FFFFFFFFh

13.3.1 BBANKMASK—Offset 8h

BUnit Bank Mask (BBANKMASK) The BBANKMASK register is used by the address-aware scheduling mechanism to determine the bit location of the bank bits within a 35 bit addresses. Bits 23:0 of this register are mapped to bits 35:12 of the addresses in the Bunit tag store PnP: The defaultBank mask is assuming static map select which is not available on VLV2. By default hash map is enabled for bank calculation so the default value should be set to 0 according to the HAS.

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x03] + 8h

Op Codes:
h - Read, h - Write

Default: 0000000Eh

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 1 1 0

RESERVED_0 | BANK_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RESERVED_0:** Reserved
23:0	0eh RW	**BANK_MASK:** Bank_mask: Bit mask that corresponds to the location of the bank bits within bits 35:12 of a system address

13.3.2 BROWMASK—Offset 9h

BUnit Row Mask (BROWMASK) The BROWMASK register is used by the address-aware scheduling mechanism to determine the bit location of the row bits within a 35 bit addresses. Bits 23:0 of this register are mapped to bits 35:12 of the addresses in the Bunit tag store

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + 9h

Op Codes:
h - Read, h - Write

Default: 00FFFFFEh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
RESERVED_0								ROW_MASK																							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RESERVED_0:** Reserved
23:0	fffffeh RW	**ROW_MASK:** Row_mask: Bit mask that corresponds to the location of the row bits within bits 35:12 of a system address PnP: Value for perf and powerperf based on drp DIMMDEN0 8Gbit and x16 device which points to column in dunit HAS with rank size 4GB and width x16 (Set all the bits except column bits and we push all the bits up by 1 for system address which makes the mask from bit 14 to bit 34 of system address, hence the value 7ffffc). But VLV will support only 2 ranks so change it to 3ffffc PnP: Set the appropriate value from the Range based on rank density and device width of dram (Note: For 32Bit interfaces, for each of these, simply right shift the corresp option by 1)

13.3.3 BRANKMASK—Offset Ah

BUnit Rank Mask (BRANKMASK) The BRANKMASK register is used by the address-aware scheduling mechanism to determine the bit location of the rank bits within a 35 bit addresses. Bits 9:0 of this register are mapped to bits 35:26 of the addresses in the Bunit tag store

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + Ah

Op Codes:
h - Read, h - Write

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

RESERVED_0 (bits 31:10) | RANK_MASK (bits 9:0)

Bit Range	Default & Access	Field Name (ID): Description
31:10	00h RO	**RESERVED_0:** Reserved
9:0	04h RW	**RANK_MASK:** Rank_mask: Bit mask that corresponds to the location of the rank bits within bits 35:26 of a system address PnP:Set the rankmask from the range based on the rank density and device width of dram used

13.3.4 BIMRDATA—Offset 1Ah

BUnit Protected Memory Region Data Value

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x03] + 1Ah

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LSFR_OUT

RETURN_PATTERN

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**LSFR_OUT:** Return LFSR Output on Range Violation : When set, the BUnit will return a stamped-down version of the output of an LFSR register instead of the data from the data return portion of this register.
30:0	0h RW	**RETURN_PATTERN:** Data Return Pattern for disallowed operations (DataPattern): This 31-bit value will be repeated along the 256-bit data bus and returned to any agent that has performed an access to the restricted access region.

13.3.5 BPMRVCTL—Offset 1Bh

BUnit Protected Memory Range Violation Control

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x03] + 1Bh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	ENABLE_INTR
30:27	RESERVED_0
26	UNS_PFI_LEN
25	UNS_IDI_LEN
24	ECAM_OPC_VIO
23	WB_NON_DRAM_VIO
22	RFO_NON_DRAM_VIO
21:16	PMR_VIO
15	MEM_AXS_2APIC
14	PFI_2_MMIO
13	UNS_PFI_OPC
12	UNS_IDI_OPC
11:8	VIOLATING_AGENT_ID
7:0	VIOLATING_AGENT_ORDERID

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ENABLE_INTR:** Enable Interrupt on Protected Memory Region Violation (EnablePMRInt): When set, the BUnit will latch violation information into this register and send an interrupt request (opcode 0x70) to the PUnit. This bit is cleared upon triggering and must be reset by software in order to trigger again. Memory protection is maintained even while the interrupt/capture mechanism is disabled. It is used to enable software debug of IMR errors, and is not expected to be used in end-user systems
30:27	0h RO	**RESERVED_0:** Reserved
26	0b RO	**UNS_PFI_LEN:** Unsupported PFI length.
25	0b RO	**UNS_IDI_LEN:** Unsupported IDI length.
24	0b RO	**ECAM_OPC_VIO:** ECAM opcode is not PRD or WIL.
23	0b RO	**WB_NON_DRAM_VIO:** IDI WB is not to DRAM space.
22	0b RO	**RFO_NON_DRAM_VIO:** IDI RFO is not to DRAM space.
21:16	0h RO	**PMR_VIO:** Protected Memory Range Violation : This 6-bit value indicates which region was last violated when the interrupt is enabled..
15	0h RO	**MEM_AXS_2APIC:** Memory Access to APIC region from a PFI Agent
14	0h RO	**PFI_2_MMIO:** MMIO Access from a PFI Agent
13	0h RO	**UNS_PFI_OPC:** Unsupported PFI Request Opcode

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**UNS_IDI_OPC:** Unsupported IDI Request Opcode
11:8	0h RO	**VIOLATING_AGENT_ID:** Protect Asset Access Violation Agent ID: This 4-bit value indicates which agent caused the last access violation if the interrupt is enabled. The Agent ID values are assigned starting with the IDI Attach Points first followed by the PFI Agents. For a configuration using 1 IDI Attach point the IDI Attach Point Agent ID would be 0 and the PFI Agent IDs would start at 1. For 2 IDI Attach Points the IDI Attach Points values would be 0 or 1 and the PFI Agent IDs would start at 2.
7:0	0h RO	**VIOLATING_AGENT_ORDERID:** Protect Asset Access Violation Order ID: This value indicates the Order ID of the agent that caused the last access violation, if the interrupt is enabled. If access violation was from an IDI attach point this field latches the LPID.

13.3.6 BNOCACHE—Offset 23h

BUnit Non-Cached Region (BNOCACHE) This register defines a region of memory that, when DMA devices behind PFI agents perform an access (whether snooped or not), will not cause an IDI snoop.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + 23h

Op Codes:

h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

31:16	15:0
UPPER_NO_SNOOP_BOUND	LOWER_NO_SNOOP_BOUND

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**UPPER_NO_SNOOP_BOUND:** Upper Bound (UpperNoSnoopBound): These bits are compared with bits 35:20 of the incoming address to determine the upper 1MB aligned value of the non-snoop range when EnableNoSnoop is set.
15:0	0000h RW	**LOWER_NO_SNOOP_BOUND:** Lower Bound (LowerNoSnoopBound): These bits are compared with bits 35:20 of the incoming address to determine the lower 1MB aligned value of the protected range when EnableNoSnoop is set.

13.3.7 BNOCACHECTL—Offset 24h

BUnit Non-Cached Region (BNOCACHECTL)

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + 24h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_0 (bits 31:1) | ENABLE_NO_SNOOP (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0000h RO	**RESERVED_0:** Reserved
0	0h RW	**ENABLE_NO_SNOOP:** Enabled (EnableNoSnoop): When set, Bunit compares bits 35:20 incoming addresses to Upper and Lower NoSnoop Bounds to see if the transaction should be prevented from issuing a processor snoop operation

13.3.8 BMBOUND—Offset 25h

Bunit Memory/IO Boundary Register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + 25h

Op Codes:
h - Read, h - Write

Default: 40000000h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HOST_IO_BOUNDARY					RESERVED_0																									SEND_ALL_ACCESS_MEM	SEND_BOOT_VECTOR_TO_DRAM

Bit Range	Default & Access	Field Name (ID): Description
31:27	008h RW	**HOST_IO_BOUNDARY:** Host IO Boundary: Bits 31:27 are compared with incoming Host Memory Request addresses to understand whether the associated transactions should be routed to memory space (DRAM) or IO space. The Host IO Boundary starts at this address and continues up to the 4GB address, 0xFFFF_FFFF.
26:2	0000000h RO	**RESERVED_0:** Reserved
1	0h RW	**SEND_ALL_ACCESS_MEM:** Send All Accesses to Memory: When set, all accesses will be sent to memory, regardless of address.
0	0h RW	**SEND_BOOT_VECTOR_TO_DRAM:** When set accesses from 0xFFFF0000-0xFFFFFFFF will be sent to memory regardless of the Host IO Boundary setting.

13.3.9 BMBOUND_HI—Offset 26h

Bunit Memory/IO HI Boundary Register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + 26h

Op Codes:
h - Read, h - Write

Default: 80000000h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HOST_IO_BOUND_HIGH (31:24) | RESERVED_0 (23:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	80h RW	**HOST_IO_BOUND_HIGH:** Host IO Boundary High: Bits 31:24 are compared with bits 35:28 of incoming addresses of all memory accesses above 4GB to understand whether the associated transactions should be routed to memory space (Bunit) or IO space (Aunit). If bits 35:28 of the address are greater than or equal to the Host IO Boundary High register field, then the transaction is routed to the MMIO space.
23:0	0000000h RO	**RESERVED_0:** Reserved

13.3.10 BECREG—Offset 27h

Bunit Extended Configuration Space Config

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x03] + 27h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ECBASE (31:28) | RESERVED_0 (27:1) | ECENABLE (0)

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**ECBASE:** EC Boundary (ECBase): Describes bits [31:28] of the range being used to access memory-mapped configuration space through the AUnit.
27:1	0000000h RO	**RESERVED_0:** Reserved
0	0h RW	**ECENABLE:** EC Enable (ECEnable): When set, causes the ECBase range to be compared to incoming Host Memory Request addresses. If bits [35:28] of a Memory access match the ECBase value, then a posted memory operation is treated as a non-posted operation by the T-unit and A-unit. Additionally, a Memory Write to Configuration Space will be serialized by T-unit and A-unit hardware as Non-Posted Writes

13.3.11 BSMMRRL—Offset 2Eh

Bunit System Management Range Register Low The SMM space is used to protect BIOS or other embedded code from corruption by the operating system. As such, the ranges below only should be set to cover memory space that is mapped into DRAM.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + 2Eh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED_0																SMMSTART															

Bit Range	Default & Access	Field Name (ID): Description
31:16	000h RO	**RESERVED_0:** Reserved
15:0	000h RW	**SMMSTART:** Lower Bound (SMMStart): These bits are compared with bits 35:20 of the incoming address to determine the lower 1MB aligned value of the protected range.

13.3.12 BSMMRRH—Offset 2Fh

Bunit System Management Range Register Hi The SMM space is used to protect BIOS or other embedded code from corruption by the operating system. As such, the ranges below only should be set to cover memory space that is mapped into DRAM.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + 2Fh

Op Codes:
h - Read, h - Write

Default: 00000000h

SMM_ENABLE	IWB_EN	PTI_TRACE_EN	RESERVED_0	SMMEND
31	30	29	28 … 16	15 … 0
0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**SMM_ENABLE:** SMM Enable: Enables the error checking for the System Management region.
30	0h RW	**IWB_EN:** Enables IWB
29	0h RW	**PTI_TRACE_EN:** PTI Trace Enable: Enables snooping of transactions to the SMM region by PTI tracing agents. This bit should be set for VISA Lites so matches/hits to SMM region can be viewed.
28:16	000h RO	**RESERVED_0:** Reserved
15:0	000h RW	**SMMEND:** Upper Bound (SMMEnd): These bits are compared with bits 35:20 of the incoming address to determine the upper 1MB aligned value of the protected range .

13.3.13 BC0AHASHCFG—Offset 30h

The Bunit Address Hash Configuration register can be used to enable a hashing function for specifying the bank and rank bits used by the Dunit. When this Address Hashing function is enabled the Bunit Bank Mask and Rank Mask configuration registers should be disabled by writing it with all 0s.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x03] + 30h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields (bits 31 to 0): RESERVED_0, DIMM1_RANK2_SIZE, DIMM1_PART_WIDTH, RESERVED_1, DIMM0_RANK0_SIZE, DIMM0_PART_WIDTH, RANK3_ENABLE, RANK2_ENABLE, RANK1_ENABLE, RANK0_ENABLE, MEMORY_INTERFACE_WIDTH_32B64B, RANK_INTERLEAVE_ENABLE, DRAM_ADDRESS_HASH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**RESERVED_0:** Reserved
17:15	0h RW	**DIMM1_RANK2_SIZE:** Configures the memory size of the ranks used by the address hash function for DIMM1. Note: If the Dunit DIMM Flip bit is set to 1 this field is the rank size for DIMM0. 0h = 128MB 1h = 256MB 2h = 512MB 3h = 1GB 4h = 2GB 5h = 4GB 6h = 8GB 7h = Reserved
14:13	0h RW	**DIMM1_PART_WIDTH:** Note: If the Dunit DIMM Flip bit is set to 1 this field is the part width for DIMM0. 0h: 8-bit 1h: 16-bit 2h: 32-bit 3h: Reserved
12	0h RO	**RESERVED_1:** Reserved
11:9	0h RW	**DIMM0_RANK0_SIZE:** Configures the memory size of the ranks used by the address hash function for DIMM0. Note: If Dunit DIMM Flip bit is set to 1 this field is the rank size for DIMM1. 0h = 128MB 1h = 256MB 2h = 512MB 3h = 1GB 4h = 2GB 5h = 4GB 6h = 8GB 7h= Reserved // PnP: Set based on how ranks are populated. Assuming RANK0,1 on DIMM0 are used.
8:7	0h RW	**DIMM0_PART_WIDTH:** Note: If the Dunit DIMM Flip bit is set to 1 this field is the part width for DIMM1. // PnP: Set based on how ranks are populated. Assuming x16 0h: 8-bit 1h: 16-bit 2h: 32-bit 3h: Reserved
6	0h RW	**RANK3_ENABLE:** When set Rank3 for DIMM1 is enable Note: If Dunit DIMM Flip bit is set to 1 this field is the rank enable for rank 1.
5	0h RW	**RANK2_ENABLE:** When set Rank2 for DIMM1 is enable Note: If Dunit DIMM Flip bit is set to 1 this field is the rank enable for rank 0.
4	0h RW	**RANK1_ENABLE:** When set Rank1 for DIMM0 is enable Note: If Dunit DIMM Flip bit is set to 1 this field is the rank enable for rank 3.
3	0h RW	**RANK0_ENABLE:** When set Rank0 for DIMM0 is enable Note: If Dunit DIMM Flip bit is set to 1 this field is the rank enable for rank 2.
2	0h RW	**MEMORY_INTERFACE_WIDTH_32B64B:** When set to 1: Configures the hashing function for 64b memory interface. When set to 0: Configures the hashing function for 32b memory interface.
1	0h RW	**RANK_INTERLEAVE_ENABLE:** When Set to 1: Enables hashing function to be used for Dunit Rank Select bits. When Set to 0: Disable the hashing function to be used for Dunit Rank Select bits. PnP: This has to match the RSIEN in DRP register in Dunit
0	0h RW	**DRAM_ADDRESS_HASH_ENABLE:** When Set to 1: Enables hashing function to be used for Dunit Bank and Rank Select bits. When Set to 0: Disable the hashing function to be used for Dunit Bank and Rank Select bits. When disabled the Dunit Bank and Rank select bits are specified using BBANKMASK And BRANKMASK configuration registers.

13.3.14 BTHCTRL—Offset 3Eh

BUnit Throttling Control (BTHCTRL)

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x03] + 3Eh

Op Codes:
h - Read, h - Write

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Field
31:16	AGENT_THROTTLING_ENABLE
15:11	RESERVED_0
10	CLEAR_BW_COUNTER_ON_READS
9	COUNT_CORE_CLOCKS
8	ENABLE_BW_COUNTER_UPDATES
7:0	RANK_SELECTION_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**AGENT_THROTTLING_ENABLE:** Agent[15:0] Throttling Enable: Setting a bit in the 16 bit vector allows the BUnit to be configured to throttle Agents 0 to 15 requests in extreme conditions. /PnP: Leaving the Value for Power as ffff but will likely result in very low perf due to lower bandwidth.
15:11	0h RO	**RESERVED_0:** Reserved
10	0h RW	**CLEAR_BW_COUNTER_ON_READS:** When set clears the Bandwidth Counter when read.
9	0h RW	**COUNT_CORE_CLOCKS:** Count Core Clocks (CountCoreClocks): Debug feature used to cause the Bunit to send bandwidth usage updates based upon 1024 core-clock periods, rather than 1024 us periods. In addition, the values reported during bandwidth counter updates will represent 32-byte quantities transferred, instead of 8k byte quantities.
8	0h RW	**ENABLE_BW_COUNTER_UPDATES:** Enable Bandwidth Counter Updates (EnableBWCounterUpdates): The bandwidth counters always count the reads and writes to even and odd ranks. When updates are enabled, the Bunit will send an update message to the Punit roughly every millisecond with the current values contained in the bandwidth counters. When the message is sent, the counters are reset. When EnableBWCounterUpdates bit is clear, the counters will be reset only by the Clear Bandwidth Counters message.
7:0	01h RW	**RANK_SELECTION_MASK:** Rank Selection Mask (RankPickMask): Bit mask compared to bits [35:28] of the incoming addresses to determine whether that address maps to Rank 'A' or to Rank 'B' PnP: Needs to match RANKMASK reg Note: Dunit RANK Hashing implemented for VLV XORs several address bits to create the Rank Select. Therefore this register no longer selects the actual Rank address of the request. Recommendation is to set this value to 0 and only use EVEN BW Counters in BBWC to determine total memory bandwidth.

13.3.15 BTHMASK—Offset 3Fh

Bunit Throttling Masks (BTHMASK) The BTHMASK register contains the fields that control BUnit throttling of transactions to DRAM. If any channel is throttled 100%, by its field being set to all zeroes, then a system deadlock is possible.

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x03] + 3Fh

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ORWRITE_MASK								ORREAD_MASK								ERWRITE_MASK								ERREAD_MASK							

Bit Range	Default & Access	Field Name (ID): Description
31:24	FFh RW	**ORWRITE_MASK:** Odd Ranks Write Mask (ORWriteMask): The Odd Rank Write mask is an eight bit value that determines the 1us time slices during which write transactions bound for these DRAM ranks will be allowed to proceed through Bunit arbitration.
23:16	FFh RW	**ORREAD_MASK:** Odd Ranks Read Mask (ORReadMask): The Odd Rank Read mask is an eight bit value that determines the 1us time slices during which read transactions bound for these DRAM ranks will be allowed to proceed through Bunit arbitration.
15:8	FFh RW	**ERWRITE_MASK:** Even Rank Write Mask (ERWriteMask): The Even Rank Write mask is an eight bit value that determines the 1us time slices during which write transactions bound for these DRAM ranks will be allowed to proceed through Bunit arbitration.
7:0	FFh RW	**ERREAD_MASK:** Even Rank Read Mask (ERReadMask): The Even Rank Read mask is an eight bit value that determines the 1us time slices during which read transactions bound for these DRAM ranks will be allowed to proceed through Bunit arbitration.

13.4 Transaction Router C-Unit PCI Registers

Table 162. Summary of C-Unit PCI Configuration Registers—0/0/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–0h	1	"CUNIT_REG_DEVICEID—Offset 0h" on page 344	00008086h
4–4h	1	"CUNIT_CFG_REG_PCISTATUS—Offset 4h" on page 345	00000007h
8–8h	1	"CUNIT_CFG_REG_CLASSCODE—Offset 8h" on page 346	06000000h
C–Ch	1	"CUNIT_CFG_REG_HDR_TYPE—Offset Ch" on page 347	00000000h
2C–2Ch	1	"CUNIT_CFG_REG_STRAP_SSID—Offset 2Ch" on page 347	00000000h
D0–D3h	4	"CUNIT_MSG_CTRL_REG—Offset D0h" on page 348	00000000h
D4–D4h	1	"CUNIT_MSG_DATA_REG—Offset D4h" on page 348	00000000h
D8–D8h	1	"CUNIT_MSG_CTRL_REG_EXT—Offset D8h" on page 349	00000000h
F8–F8h	1	"CUNIT_MSG_CTRL_REG_EXT—Offset D8h" on page 349	00000000h

13.4.1 CUNIT_REG_DEVICEID—Offset 0h

CUnit Configuration Register Device ID/Vendor ID. Device ID and Vendor ID Strapped in from top level. Reset value to strapDID[15:3],fuse[2:0], 16'h8086 these bits can be re-written from SETIDVALUE message 1st DW data byte 2, byte 3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:0, F:0] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

DEVICEID_VENDOR_ID | DEVICEID_BIT_22_19 | DEVICEID_BIT_18_16 | DEVICEID_BIT_15_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RW	**DEVICEID_VENDOR_ID:** Device ID and Vendor ID bit [15:7] are strapped in from top level. These bits can be re-written from SETIDVALUE message 1st DW data byte 2, byte 3. for VLV/VLV2, final setting of this field is from SETIDVALUE message, while for TNG it uses the strapped setting. For all SOC's, the RDL defalut is set to the strapped setting in that SOC. Please refer to the SoC documentation to determine the proper Device ID for the chip.
22:19	0h RO	**DEVICEID_bit_22_19 (DEVICEID_BIT_22_19):** Device ID [6:3] Hardwired in the design. SETIDVALUE message will not re-write this field. RDL default is set to the strapped value
18:16	0h RO	**DEVICEID_bit_18_16 (DEVICEID_BIT_18_16):** Device ID [2:0]. Strapped in from top level and tied to fuses to determine product SKU. SETIDVALUE message will not re-write this field.

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**DEVICEID_bit_15_0 (DEVICEID_BIT_15_0):** Hardwired

13.4.2 CUNIT_CFG_REG_PCISTATUS—Offset 4h

CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:0, F:0] + 4h

Default: 00000007h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

PCI_STATUS_PCI_CMD

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000007h RO	**PCI_STATUS_PCI_CMD:** PCI Status and PCI Command. Hardwired to 32'h00000007

13.4.3 CUNIT_CFG_REG_CLASSCODE—Offset 8h

CUnit Configuration register Header Type and Master Latency Time

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:0, F:0] + 8h

Default: 06000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 1 1 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PCI_CLASSCODE_REVID | PCI_BIT_15_8 | PCI_BIT_7_0

Bit Range	Default & Access	Field Name (ID): Description
31:16	0600h RO	**PCI_CLASSCODE_REVID:** PCI Class Code
15:8	00h RO	**PCI_BIT_15_8:** Hardwired to 8'h00
7:0	0h RW	**PCI_BIT_7_0:** PCI revision ID. these bits can be re-written from SETIDVALUE message 1st DW data byte 0

13.4.4 CUNIT_CFG_REG_HDR_TYPE—Offset Ch

CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:0, F:0] + Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MSTRLATENCY_HDRTYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSTRLATENCY_HDRTYPE:** Master Latency Timer and Header Type hardwired to 0

13.4.5 CUNIT_CFG_REG_STRAP_SSID—Offset 2Ch

CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:0, F:0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCI_SUBSYSTEMID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**PCI_SUBSYSTEMID:** PCI Subsystem ID passed in from top-level straps strapSSID[31:0]

13.4.6 CUNIT_MSG_CTRL_REG—Offset D0h

Message Control Register (MCR) - provides the message bus command fields. A write to this register issues a message on the Message Network with the fields specified by the write data. All byte enables must be enabled when writing this register. The physical registers reside in the target unit. This register does not reside in the Cunit.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:0, F:0] + D0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MESSAGE_OPCODE								MESSAGE_PORT								MESSAGE_ADDRESS_OFFSET								MESSAGE_WR_BYTE_ENABLES				RESERVED			

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h WO	**MESSAGE_OPCODE:** Opcode for message to be sent out on message network
23:16	00h WO	**MESSAGE_PORT:** Destination PortID for message to be sent out on message network
15:8	00h WO	**MESSAGE_ADDRESS_OFFSET:** Address offset for message to be sent out on message network
7:4	0h WO	**MESSAGE_WR_BYTE_ENABLES:** Active high byte enables which enable each of the corresponding bytes in the MDR when high.
3:0	00h WO	**RESERVED:** Reserved

13.4.7 CUNIT_MSG_DATA_REG—Offset D4h

Message Data Register (MDR) - provides the means to specify data to be written or retrieving data that was read during a message operation. For messages with a data payload, MDR must be written with the data to be sent prior to a write to MCR. For messages that return data, MDR contains the data read after the write to MCR completes.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:0, F:0] + D4h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Field	MESSAGE_DATA_REG							

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SIDEBAND_DATA_REG (MESSAGE_DATA_REG):** Sideband Data Register (MDR)

13.4.8 CUNIT_MSG_CTRL_REG_EXT—Offset D8h

Message Control Register Extension for MCR/MDR provides bits 31:8 of the address/ offset for sideband transactions that require it. Must be written before MCR. Returns to '0 after MCR is written.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:0, F:0] +D8h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 0 1	1 0 0 0
Field	MSG_CTRL_REG_EXT						RESERVED	

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000 RW	MSG_CTRL_REG_EXT: Message Control Register Extension for MCR/MDR
7:0	00h RO	RESERVED: Reserved

13.4.9 CUNIT_MANUFACTURING_ID—Offset F8h

CUnit Manufacturing ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:0, F:0] + F8h

Default: 00000000h

31:28	27:24	23:16	15:8	7:0
0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
RESERVED	MANUFACTURING_ID_BIT_27_24	MANUFACTURING_ID_BIT_23_16	MANUFACTURING_ID_BIT_15_8	MANUFACTURING_ID_BIT_7_0

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**RESERVED:** Reserved, these bits can be re-written frmo SETIDVALUE message 2nd DW data byte 3 upper nibble
27:24	0h RW	**MANUFACTURING_ID_BIT_27_24:** Dot Portion of Process, these bits can be re-written from SETIDVALUE message 2nd DW data byte 3 lower nibble
23:16	0h RW	**MANUFACTURING_ID_BIT_23_16:** Process Portion of Process ID, these bits can be re-written from SETIDVALUE message 2nd DW data byte 0
15:8	0h RW	**MANUFACTURING_ID_BIT_15_8:** Manufacturing ID (MID), these bits can be re-written from SETIDVALUE message 2nd DW data byte 1
7:0	0h RW	**MANUFACTURING_ID_BIT_7_0:** Manufacturing Stepping ID (MSID), these bits can be re-written from SETIDVALUE message 2nd DW data byte 2

13.5 Transaction Router C-Unit Message Registers

Table 163. Summary of C-Unit Message Bus Registers—Port 0x08

Offset	Register Name (Register Symbol)	Default Value
0–0h	"CUNIT_REG_DEVICEID—Offset 0h" on page 352	00008086h
1–1h	"CUNIT_CFG_REG_PCISTATUS—Offset 1h" on page 353	00000007h
2–2h	"CUNIT_CFG_REG_CLASSCODE—Offset 2h" on page 353	06000000h
3–3h	"CUNIT_CFG_REG_HDR_TYPE—Offset 3h" on page 354	00000000h
B–Bh	"CUNIT_CFG_REG_STRAP_SSID—Offset Bh" on page 355	00000000h
3E–3Eh	"CUNIT_MANUFACTURING_ID—Offset 3Eh" on page 356	00000000h

13.5.1 CUNIT_REG_DEVICEID—Offset 0h

CUnit Configuration Register Device ID/Vendor ID. Device ID and Vendor ID Strapped in from top level. Reset value to strapDID[15:3],fuse[2:0], 16'h8086 these bits can be re-written from SETIDVALUE message 1st DW data byte 2, byte 3

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x08] + 0h

Op Codes:
h - Read, h - Write

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

Fields: DEVICEID_VENDOR_ID | DEVICEID_BIT_22_19 | DEVICEID_BIT_18_16 | DEVICEID_BIT_15_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RW	**DEVICEID_VENDOR_ID:** Device ID and Vendor ID bit [15:7] are strapped in from top level. These bits can be re-written from SETIDVALUE message 1st DW data byte 2, byte 3. for VLV/VLV2, final setting of this field is from SETIDVALUE message, while for TNG it uses the strapped setting. For all SOC's, the RDL defalut is set to the strapped setting in that SOC. Please refer to the SoC documentation to determine the proper Device ID for the chip.
22:19	0h RO	**DEVICEID_bit_22_19 (DEVICEID_BIT_22_19):** Device ID [6:3] Hardwired in the design. SETIDVALUE message will not re-write this field. RDL default is set to the strapped value
18:16	0h RO	**DEVICEID_bit_18_16 (DEVICEID_BIT_18_16):** Device ID [2:0]. Strapped in from top level and tied to fuses to determine product SKU. SETIDVALUE message will not re-write this field.

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**DEVICEID_bit_15_0 (DEVICEID_BIT_15_0):** Hardwired

13.5.2 CUNIT_CFG_REG_PCISTATUS—Offset 1h

CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x08] + 1h

Op Codes:
h - Read, h - Write

Default: 00000007h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

PCI_STATUS_PCI_CMD

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000007h RO	**PCI_STATUS_PCI_CMD:** PCI Status and PCI Command. Hardwired to 32'h00000007

13.5.3 CUNIT_CFG_REG_CLASSCODE—Offset 2h

CUnit Configuration register Header Type and Master Latency Time

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x08] + 2h

Op Codes:
h - Read, h - Write

Default: 06000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 1 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
PCI_CLASSCODE_REVID				PCI_BIT_15_8		PCI_BIT_7_0	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0600h RO	**PCI_CLASSCODE_REVID:** PCI Class Code
15:8	00h RO	**PCI_BIT_15_8:** Hardwired to 8'h00
7:0	0h RW	**PCI_BIT_7_0:** PCI revision ID. these bits can be re-written from SETIDVALUE message 1st DW data byte 0

13.5.4 CUNIT_CFG_REG_HDR_TYPE—Offset 3h

CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x08] + 3h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
MSTRLATENCY_HDRTYPE							

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**MSTRLATENCY_HDRTYPE:** Master Latency Timer and Header Type hardwired to 0

13.5.5 CUNIT_CFG_REG_STRAP_SSID—Offset Bh

CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x08] + Bh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCI_SUBSYSTEMID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**PCI_SUBSYSTEMID:** PCI Subsystem ID passed in from top-level straps strapSSID[31:0]

13.5.6 CUNIT_MANUFACTURING_ID—Offset 3Eh

CUnit Manufacturing ID Register

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x08] + 3Eh

Op Codes:
h - Read, h - Write

Default: 00000000h

31:28	27:24	23:16	15:8	7:0
0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
RESERVED	MANUFACTURING_ID_BIT_27_24	MANUFACTURING_ID_BIT_23_16	MANUFACTURING_ID_BIT_15_8	MANUFACTURING_ID_BIT_7_0

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**RESERVED:** Reserved, these bits can be re-written frmo SETIDVALUE message 2nd DW data byte 3 upper nibble
27:24	0h RW	**MANUFACTURING_ID_BIT_27_24:** Dot Portion of Process, these bits can be re-written from SETIDVALUE message 2nd DW data byte 3 lower nibble
23:16	0h RW	**MANUFACTURING_ID_BIT_23_16:** Process Portion of Process ID, these bits can be re-written from SETIDVALUE message 2nd DW data byte 0
15:8	0h RW	**MANUFACTURING_ID_BIT_15_8:** Manufacturing ID (MID), these bits can be re-written from SETIDVALUE message 2nd DW data byte 1
7:0	0h RW	**MANUFACTURING_ID_BIT_7_0:** Manufacturing Stepping ID (MSID), these bits can be re-written from SETIDVALUE message 2nd DW data byte 2

13.6 Transaction Router P-Unit Message Registers

Table 164. Summary of Transaction Router P-Unit Message Bus Registers—Port 0x04

Offset	Register Name (Register Symbol)	Default Value
1–1h	"THERMAL_SOC_TRIGGER—Offset 1h" on page 358	00000000h
2–2h	"CPU_POWER_BUDGET_CONTROL—Offset 2h" on page 360	00000000h
3–3h	"SOC_POWER_BUDGET_CONTROL—Offset 3h" on page 361	00000000h
4–4h	"TURBO_SOC_OVERRIDE—Offset 4h" on page 361	00000000h
5–5h	"BIOS_RESET_CPL—Offset 5h" on page 362	00000000h
6–6h	"BIOS_CONFIG—Offset 6h" on page 363	00000000h
1D–1Dh	"BIOSCFG_IPDEVTYPE—Offset 1Dh" on page 364	00000000h
1E–1Eh	"PUNIT_S0i2_PREWAKE—Offset 1Eh" on page 364	00000000h
1F–1Fh	"PUNIT_S0i3_PREWAKE—Offset 1Fh" on page 365	00000000h
32–32h	"VEDSSPM0—Offset 32h" on page 365	03000003h
33–33h	"VEDSSPM1—Offset 33h" on page 366	00000000h
36–36h	"DSPSSPM—Offset 36h" on page 367	00000000h
39–39h	"ISPSSPM0—Offset 39h" on page 368	03000003h
3A–3Ah	"ISPSSPM1—Offset 3Ah" on page 368	00000000h
3B–3Bh	"MIOSSPM—Offset 3Bh" on page 369	00000000h
60–60h	"PWRGT_CNT_CTRL—Offset 60h" on page 370	00000000h
61–61h	"PWRGT_STATUS—Offset 61h" on page 371	00000000h
62–62h	"PWRGT_INTREN—Offset 62h" on page 372	00000000h
7C–7Ch	"CPU_SOFT_STRAPS—Offset 7Ch" on page 374	00000000h
80–80h	"PTMC—Offset 80h" on page 375	00000000h
81–81h	"TTR0—Offset 81h" on page 377	00000000h
82–82h	"TTR1—Offset 82h" on page 377	00000000h
83–83h	"TTS—Offset 83h" on page 378	00000000h
84–84h	"TELB—Offset 84h" on page 378	00000000h
85–85h	"TELT—Offset 85h" on page 379	00000000h
86–86h	"TQPR—Offset 86h" on page 380	00000000h
88–88h	"GFXT—Offset 88h" on page 381	00000000h
89–89h	"VEDT—Offset 89h" on page 382	00000000h
8C–8Ch	"ISPT—Offset 8Ch" on page 383	00000000h
B0–B0h	"DTSC—Offset B0h" on page 384	00000000h
B1–B1h	"TRR—Offset B1h" on page 385	00000000h
B2–B2h	"PTPS—Offset B2h" on page 386	00000000h
B3–B3h	"PTTS—Offset B3h" on page 386	00000000h
B4–B4h	"PTTSS—Offset B4h" on page 388	00000000h
B5–B5h	"TE_AUX0—Offset B5h" on page 389	00000000h
B6–B6h	"TE_AUX1—Offset B6h" on page 391	00000000h

Table 164. Summary of Transaction Router P-Unit Message Bus Registers—Port 0x04

Offset	Register Name (Register Symbol)	Default Value
B7–B7h	"TE_AUX2—Offset B7h" on page 392	00000000h
B8–B8h	"TE_AUX3—Offset B8h" on page 394	00000000h
B9–B9h	"TTE_VRIccMax—Offset B9h" on page 395	00000000h
BA–BAh	"TTE_VRHot—Offset BAh" on page 396	00000000h
BB–BBh	"TTE_XXPROCHOT—Offset BBh" on page 397	00000000h
BC–BCh	"TTE_SLM0—Offset BCh" on page 399	00000000h
BD–BDh	"TTE_SLM1—Offset BDh" on page 400	00000000h
BE–BEh	"BWTE—Offset BEh" on page 401	00000000h
BF–BFh	"TTE_SWT—Offset BFh" on page 402	00000000h
D1–D1h	"PUNIT_GPU_EC—Offset D1h" on page 404	00000000h
D2–D2h	"PUNIT_GPU_EC_VIRUS—Offset D2h" on page 404	00000000h
D3–D3h	"PUNIT_GPU_LFM—Offset D3h" on page 405	00000000h
D4–D4h	"PUNIT_GPU_FREQ_REQ—Offset D4h" on page 405	00000000h
D8–D8h	"PUNIT_GPU_FREQ_STS—Offset D8h" on page 406	00000000h
108–108h	"DPTF_TELB—Offset 108h" on page 406	00000000h
109–109h	"DPTF_GFXT—Offset 109h" on page 407	00000000h
10A–10Ah	"DPTF_VEDT—Offset 10Ah" on page 408	00000000h
10B–10Bh	"DPTF_VECT—Offset 10Bh" on page 408	00000000h
10C–10Ch	"DPTF_VSPT—Offset 10Ch" on page 409	00000000h
10D–10Dh	"DPTF_ISPT—Offset 10Dh" on page 410	00000000h

13.6.1 THERMAL_SOC_TRIGGER—Offset 1h

Driver Software (like Burst Mode Governor) may use this register to indicate TSKIN violation.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 1h

Op Codes:
h - Read, h - Write

Default: 00000000h

31:24	23:16	15:12	11	10:8	7:3	2	1	0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0 0	0	0	0
HOTTEST_DIE_TEMP_READING	UNUSED_TSKIN_WARNING_THRESHOLD	TSKIN_TEMP_STATUS1	UNUSED_PMICRO_ICC_MAX	UNUSED_TSKIN_TEMP_STATUS	UNUSED_TSKIN_SPARE	UNUSED_TSKIN_WARNING	CPU_POWER	UNUSED_TSKIN_VIOLATION

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**HOTTEST_DIE_TEMP_READING:** Stores the hottest DTS sample of all thermal sensors in the CPU+SOC.
23:16	0h RW	**UNUSED_TSKIN_WARNING_THRESHOLD:** THIS FIELD IS UNUSED IN VLV/TNG. For platforms which implement a Tskin temperature sensor, this field can be used to specify the temperature limit above which TSKIN_WARNING will be set and Turbo operation will be disabled in the SOC.
15:12	0h RW	**TSKIN_TEMP_STATUS1:** THIS FIELD IS UNUSED IN VLV/TNG. For platforms which implement a Tskin temperature sensor, this field can be used to report the TSKIN temperature value for use by Punit firmware.
11	0h RO	**UNUSED_PMICRO_ICC_MAX:** THIS FIELD IS UNUSED IN VLV/TNG. Bit 11 is used indicate a Vcc Icc max condition. It is driven by the firmware when it gets a SVID update indicating a icc max hot condition. The firmware drives it back low when the hot condition is resolved when it gets a SVID update.
10:8	0h RW	**UNUSED_TSKIN_TEMP_STATUS:** THIS FIELD IS UNUSED IN VLV/TNG. For platforms which implement a Tskin temperature sensor, this field can be used to report the TSKIN temperature value for use by Punit firmware.
7:3	0h RW	**UNUSED_TSKIN_SPARE:** THIS FIELD IS UNUSED IN VLV/TNG. Spare for future tskin related controls
2	0h RW	**UNUSED_TSKIN_WARNING:** THIS FIELD IS UNUSED IN VLV/TNG. Early warning flag for TSKIN to be set by SCU, PUnit or platform driver to take early action to reduce power consumption...When asserted Punit will disable Turbo range of operation for CPU and GPU and limit operation to Guaranteed frequency. For systems which provide TSkin temperature punit may set this bit if Tskin exceeds TSKIN_WARNING_THRESHOLD...0 - Tskin warning is not triggered..1 - Tskin warning is triggered and CPU/GPU operation should be limited to Guaranteed frequencies.
1	0h RW	**CPU_POWER:** Reserved.
0	0h RW	**UNUSED_TSKIN_VIOLATION:** THIS FIELD IS UNUSED IN VLV/TNG. This bit can be set by the SOC or PUnit firmware to indicate that the system thermals are exceeding the TSkin spec. Setting this bit will trigger any enabled CPU thermal throttling mechanisms to take effect. Thermal throttling will remain active until this bit is cleared. For systems which provide TSkin temperature punit may set this bit if Tskin exceeds TSKIN_THROTTLE_THRESHOLD...0 tskin is not violated..1 trigger thermal throttling mechanisms to reduce platform temperature..

13.6.2 CPU_POWER_BUDGET_CONTROL—Offset 2h

TDP power budget utilization/budget for SOC; This register requires SAI security restriction.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 2h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED_7	SPARE						IBC_LIMIT_ENABLE	IBC_RATIO_LIMIT								RESERVED_3	TURBOEM_FCPU_FLOOR							TURBOEM_FCPU_GAIN							

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**RESERVED_7:** reserved
30:25	0h RW	**SPARE:** Reserved.
24	0h RW	**IBC_LIMIT_ENABLE:** Enables IBC IA Pstate Limiting control. When set, the CPU frequency will be limited according to IBC_RATIO_LIMIT.
23:16	0h RW	**IBC_RATIO_LIMIT:** IBC IA Pstate Limiting control for GFX driver to limit the max CPU frequency (bounded by TURBOEM_FCPU_FLOOR and MAX_RATIO_1C). Will only take effect if IBC_LIMIT_ENABLE is set. The CPU ratio is limited to this ratio if Turbo is enabled in the system. Default value of 0 is mapped to MAX_RATIO_1C. Value of 1 is mapped to RATIO 1, etc.
15	0h RW	**RESERVED_3:** reserved
14:8	0h RW	**TURBOEM_FCPU_FLOOR:** Specifies the target ratio floor when the PL1 proportional controller or IBC_RATIO_LIMIT is in effect. Default value of 0 is mapped to GUAR_RATIO. Value of 1 is mapped to RATIO 1, etc. Note that values lower than LFM_RATIO may be clipped by hardware to LFM_RATIO.
7:0	0h RW	**TURBOEM_FCPU_GAIN:** Specifies the scaling factor for PL1 proportional controller to map CPU energy budget to ratio limit during Energy Management Turbo Mode. Target ratio = LFM_RATIO + energy_credit / (gain+1)

13.6.3 SOC_POWER_BUDGET_CONTROL—Offset 3h

Energy Credit available for SOC Turbo

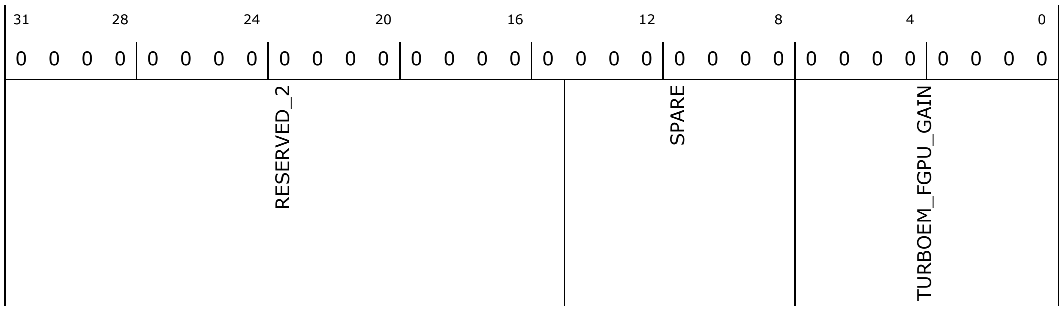
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 3h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**RESERVED_3 (RESERVED_2):** reserved
14:8	0h RO	**SPARE:** reserved
7:0	0h RW	**TURBOEM_FGPU_GAIN (TURBOEM_FGPU_GAIN):** Specifies the scaling factor for PL1 proportional controller to map GFX energy budget to ratio limit during Energy Management Turbo Mode. Target ratio = RPn + energy_credit / (gain+1)

13.6.4 TURBO_SOC_OVERRIDE—Offset 4h

Override CPU-SOC TDP sharing configuration in PKG_TURBO_CFG1; This register requires SAI security restriction.

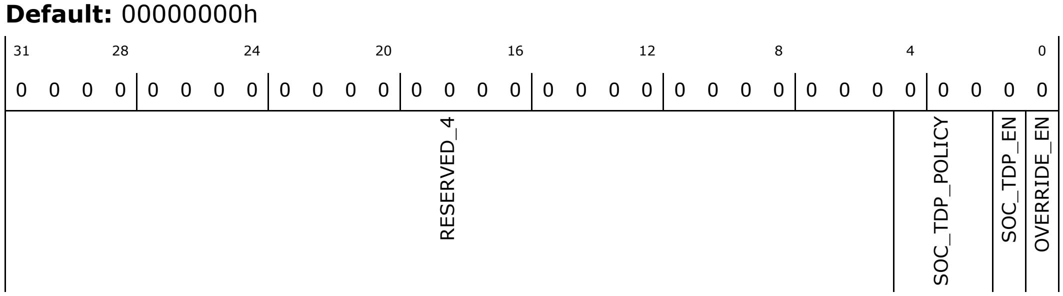
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 4h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**RESERVED_4:** reserved
4:2	0h RW	**SOC_TDP_POLICY:** Overrides PKG_TURBO_CFG1[SOC_TDP_POLICY]. Refer PKG_TURBO_CFG1 register description for more info...Device Driver software may use this register to dynamically adjust power sharing configuration between CPU and SOC
1	0h RW	**SOC_TDP_EN:** Overrides PKG_TURBO_CFG1[SOC_TDP_EN]. Refer to PKG_TURBO_CFG1 register description for more info. ..Device Driver software may use this register to dynamically adjust power sharing configuration between CPU and SOC
0	0h RW	**OVERRIDE_EN:** Allows fields in this register to override corresponding Turbo MSR fields.

13.6.5 BIOS_RESET_CPL—Offset 5h

BIOS Reset Complete.

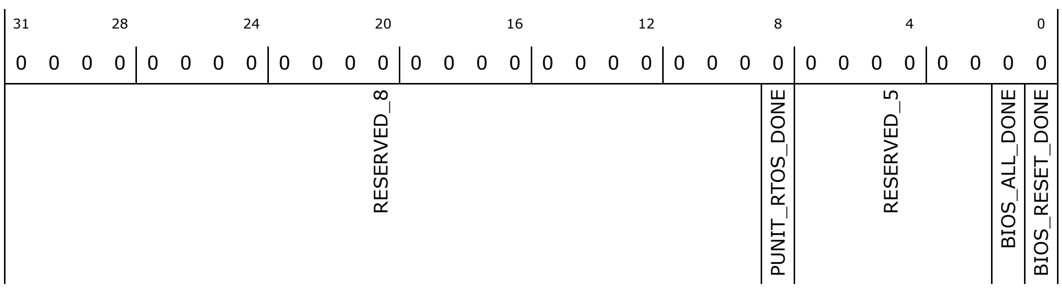
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 5h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**RESERVED_9 (RESERVED_8):** reserved
8	0h RW	**PUNIT_RTOS_DONE:** Punit will set this bit once firmware initialization of all tasks is completed. Simulation may poll this bit to hold-off code execution until Punit has safely initialized.
7:2	0h RW	**RESERVED_5:** Reserved
1	0h RW	**BIOS_ALL_DONE:** This bit indicates to the P unit that it can execute its periodic tasks.
0	0h RW	**BIOS_RESET_DONE:** This bit indicates to the P unit that the Patch loading is completed and the firmware can restart execution. Firmware will poll on this bit to be set. Note: This bit must be sticky once set and can only be cleared by a core reset.

13.6.6 BIOS_CONFIG—Offset 6h

Punit-BIOS controls

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 6h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits	Default	Field
31	0	ECC_EN
30	0	DUAL_CH_DIS
29	0	EFF_ECC_EN
28	0	EFF_DUAL_CH_EN
27:18	0 0 0 0 0 0 0 0 0 0	Reserved_9
17	0	BIOS_PDM
16	0	DFX_PDM_MODE
15:9	0 0 0 0 0 0 0	Reserved_6
8	0	DDRIO_PWRGATE
7	0	GFX_TURBO_DISABLE
6:2	0 0 0 0 0	Reserved_4
1	0	PCIE_PLLOFFOK_EN
0	0	USB_CACHING_EN

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC_EN:** Setting this bit allows using a fused Dual Channel part as a single channel part with the second Channel being used for ECC.
30	0h RW	**DUAL_CH_DIS:** Setting this bit allows using a fused Dual Channel part as a single Channel part.
29	0h RW	**EFF_ECC_EN:** Effective ECC Status bit indicating if ECC is enabled(1) or disabled(0) based on the Fuse and the Downbin bit
28	0h RW	**EFF_DUAL_CH_EN:** Effective Dual Channel Status bit indicating if Dual Channel is enabled(1) or Single Channel is enabled(0)
27:18	0h RW	**Reserved_9:** Unused, reserved for future use.
17	0h RW	**DFX_POWERGATING (BIOS_PDM):** 0: Power Save Mode- Powergate DFX for power savings 1: PERF_MODE or PDM_MODE: Leave DFX blocks powered up BIOS must always set this bit before BIOS_RESET_CPL[1:0] bits are set. BYT-M and BYT-D segments leave DFX Powered up. BYT-T segments provide user option to leave DFX powered up or powered down. BIOS can change the DFX_Powergating bit to 0 to powergate DFX.
16	0h RW	**DFX_PDM_MODE:** This bit has effect only when DFX_Powergating (bit 17) is set. 0: PERF_MODE: Access to Performance Counters for SOCHAPs, Memory Traffic etc. 1: PDM_MODE: Memory BW counts not available but PDM debug messages are available
15:9	0h RW	**Reserved_6:** Reserved
8	0h RW	**DDRIO_PWRGATE:** Firmware sets bit 8 by default to disable ddrio powergating in S0i3. If BIOS writes to this BYTE, it must set bit 8 to avoid clobbering firmware update. DDRIO_PWRGATE is not supported on VLV. This bit is relevant only for SKUs supporting S0i3.
7	0h RW	**GFX_TURBO_DISABLE:** Setting this bit will disable GFX TURBO, even if the Fuses enable it. Setting this bit is not recommended for VLV
6:2	0h RW	**Reserved_4:** Unused, reserved for future use.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**PCIE_PLLOFFOK_EN:** When set, P unit will inform PCIE when the last core is entering and when the first core is exiting PC7 so that PCIE can turn off PLL
0	0h RW	**USB_CACHING_EN:** When set, P unit will inform USB when the last core is entering and first core is exiting PC7 so that USB caching can be enabled. BIOS will set this bit in synch with USB caching enable/disable setting. P unit will do the above handshake if the bit is set, or will skip the handshake if the bit is not set.

13.6.7 BIOSCFG_IPDEVTYPE—Offset 1Dh

This Punit Register controls the Device type during boot for IPS

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 1Dh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															RESERVED																IUNIT_DEVICE_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RW	**RESERVED:** Reserved bits for future use
0	0h RW	**IUNIT_DEVICE_TYPE:** IUNIT is by default Device3 type. By setting this bit the device type of IUNIT changes to Device2.

13.6.8 PUNIT_S0i2_PREWAKE—Offset 1Eh

SB register for pre-wake periods for S0i2

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 1Eh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

s0i2_PREWAKE

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**s0i2_PREWAKE:** BIOS or OS can program this register with a pre-wake value in Guaranteed MCLKs to hide some of the exit latency from S0i2 state to S0 state. P unit will subtract this value from the actual deadline programmed by the OS when requesting for a timer wake.

13.6.9 PUNIT_S0i3_PREWAKE—Offset 1Fh

BIOS or OS can program this register with a pre-wake value in Guaranteed MCLKs to hide some of the exit latency from S0i3 state to S0 state. P unit will subtract this value from the actual deadline programmed by the OS when requesting for a timer wake.

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 1Fh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

s0i3_PREWAKE

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**s0i3_PREWAKE:** S0i3 Prewake Deadline

13.6.10 VEDSSPM0—Offset 32h

Subsystem Config/Status for VED

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 32h

Op Codes:
h - Read, h - Write

Default: 03000003h

Bits 31–0: 0 0 0 0 | 0 0 1 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 1

Fields: Reserved_1 | VEDSSS | Reserved_3 | VEDIE | Reserved_5 | Reserved_6 | VEDSSC

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved_1:** Reserved
25:24	3h RO	**VEDSSS:** 0x03 indicates powered off state, 0x00 indicates powered on state. P unit will write this field to register field to reflect the status for power up or power down for the Video Decode Engine.Driver is expected to poll for the power up status before accessing the IP.
23:16	0h RO	**Reserved_3:** Reserved
15	0h RW	**VEDIE:** VED Power Up Interrupt Enable
14:8	0h RO	**Reserved_5:** Reserved
7:2	0h RO	**Reserved_6:** Reserved
1:0	3h RW	**VEDSSC:** 0x03 indicates powered off state, 0x00 indicates powered on state. Driver will write this field to register field to request power up or power down for the Video Decode Engine.

13.6.11 VEDSSPM1—Offset 33h

Subsystem Px for Ved

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 33h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits 31–0: 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Fields: Reserved_1 | VEDFREQSTAT40 | Reserved_3 | VEDFREQGUAR40 | FREQVALID | Reserved_6 | VEDFREQ40

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved_1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RO	**VEDFREQSTAT40:** VED Frequency Status
23:13	0h RO	**Reserved_3:** Reserved
12:8	0h RW	**VEDFREQGUAR40:** VED Guaranteed Frequency- Place holder for future use.
7	0h RW	**FREQVALID:** if and only if this bit is set the freq requested in the FREQ field will be looked at by the Punit and will clear this field once the freq status is updated
6:5	0h RO	**Reserved_6:** Reserved
4:0	0h RW	**VEDFREQ40:** VED driver requested Frequency

13.6.12 DSPSSPM—Offset 36h

Subsystem Config/Status for Display

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 36h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSPFREQSTAT		Reserved_5														DSPFREQREQ		Reserved_7						Reserved_9							

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**DSPFREQSTAT:** Display frequency status
29:16	0h RO	**Reserved_5:** Reserved
15:14	0h RW	**DSPFREQREQ:** Display frequency request
13:8	0h RO	**Reserved_7:** Reserved
7:0	0h RO	**Reserved_9:** Reserved

13.6.13 ISPSSPM0—Offset 39h

Subsystem Config/Status for ISP

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x04] + 39h

Op Codes:
h - Read, h - Write

Default: 03000003h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 1 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 1

Reserved_1 | ISPSSS | Reserved_3 | Reserved_4 | ISPSSC

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved_1:** Reserved
25:24	3h RO	**ISPSSS:** ISP Subsystem Status0x03 indicates powered off state, 0x00 indicates powered on state. P unit will write this field to register field to reflect the status for power up or power down for the Camera .Driver is expected to poll for the power up status before accessing the IP.
23:8	0h RO	**Reserved_3:** Reserved
7:2	0h RO	**Reserved_4:** Reserved
1:0	3h RW	**ISPSSC:** ISP SubsystemControl- 0x03 indicates powered off state, 0x00 indicates powered on state. Driver will write this field to register field to request power up or power down for the Camera IP.

13.6.14 ISPSSPM1—Offset 3Ah

Subsystem Px for ISP

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x04] + 3Ah

Op Codes:
h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1 | ISPFREQSTAT40 | Reserved_3 | ISPFREQGUAR40 | FREQVALID | Reserved_6 | ISPFREQ40

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved_1:** Reserved
28:24	0h RO	**ISPFREQSTAT40:** ISP Frequency Status
23:13	0h RO	**Reserved_3:** Reserved
12:8	0h RW	**ISPFREQGUAR40:** ISP Guaranteed Frequency
7	0h RW	**FREQVALID:** if and only if this bit is set the freq requested in the FREQ field will be looked at by the Punit and will clear this field once the freq status is updated
6:5	0h RO	**Reserved_6:** Reserved
4:0	0h RW	**ISPFREQ40:** ISP driver requested Frequency

13.6.15 MIOSSPM—Offset 3Bh

Subsystem Config/Status for MIO

Access Method

Type: Message Bus Register (Size: 32 bits)   **Offset:** [Port: 0x04] + 3Bh

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Reserved_1	MIOSSS	Reserved_3	Reserved_4	MIOSSC

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved_1:** Reserved
25:24	0h RO	**MIOSSS:** MIO Subsystem Status Status0x03 indicates powered off state, 0x00 indicates powered on state. P unit will write this field to register field to reflect the status for power up or power down for the MIPI IO .Driver is expected to poll for the power up status before accessing the IP.
23:8	0h RO	**Reserved_3:** Reserved
7:2	0h RO	**Reserved_4:** Reserved
1:0	0h RW	**MIOSSC:** MIO (CSI) SubsystemControl- 0x03 indicates powered off state, 0x00 indicates powered on state. Driver will write this field to register field to request power up or power down for the MIPI controller. Note the implementation does not actually power gate, but will turn off the clock trunks and apply reset to MIO .

13.6.16 PWRGT_CNT_CTRL—Offset 60h

Active Power Gate Control Register;This register indicates the configuration of the voltage islands for the various blocks that the P unit controls. This register is updated by the software driver to request power up / power down of the various sub systems like the graphics, display et all. Each island is controlled by a 2-bit field. 00 -- no clock or power gating, 01 -- clock gating, 10 -- reset and 11 -- power gating.(Encoding is as follows: subsys 0 RENder, 1 media, 3 -Display, DPIO :subsystem 5 Common lane, subs 6-9 TX, subs 10-11 RX)

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 60h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
POWERGATE_RESERVED5		POWERGATE_RESERVED4		POWERGATE_RESERVED3		POWERGATE_RESERVED2		POWERGATE_RX1		POWERGATE_RX0		POWERGATE_TX3		POWERGATE_TX2		POWERGATE_TX1		POWERGATE_TX0		POWERGATE_CMNLN		POWERGATE_RESERVED1		POWERGATE_DISPLAY_CTL		POWERGATE_RESERVED0					

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**POWERGATE_RESERVED5:** Reserved
29:28	0h RW	**POWERGATE_RESERVED4:** Reserved
27:26	0h RW	**POWERGATE_RESERVED3:** Reserved
25:24	0h RW	**POWERGATE_RESERVED2:** Reserved
23:22	0h RW	**POWERGATE_RX1:** Active power gate control for RX lane 0x03 indicates powered off state, 0x00 indicates powered on state
21:20	0h RW	**POWERGATE_RX0:** Active power gate control for RX lane 0x03 indicates powered off state, 0x00 indicates powered on state
19:18	0h RW	**POWERGATE_TX3:** Active power gate control for TX lane 0x03 indicates powered off state, 0x00 indicates powered on state
17:16	0h RW	**POWERGATE_TX2:** Active power gate control for TX lane 0x03 indicates powered off state, 0x00 indicates powered on state
15:14	0h RW	**POWERGATE_TX1:** Active power gate control for TX lane 0x03 indicates powered off state, 0x00 indicates powered on state

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**POWERGATE_TX0:** Active power gate control for TX lane 0x03 indicates powered off state, 0x00 indicates powered on state
11:10	0h RW	**POWERGATE_CMNLN:** Active power gate control for common lane 0x03 indicates powered off state, 0x00 indicates powered on state. Driver will write this field to register field to request power up or power down for the DPIO common lane. Note that before powering up the TX/RX subsystems for DPIO, from a power down state, CMNLN reset (POWERGATE_CMNLN) must be cycled
9:8	0h RW	**POWERGATE_RESERVED1:** Reserved
7:6	0h RW	**POWERGATE_DISPLAY_CTL:** Active power gate control for display, DPIO0x03 indicates powered off state, 0x00 indicates powered on state. Driver will write this field to register field to request power up or power down for the Display Controller
5:0	0h RW	**POWERGATE_RESERVED0:** Reserved

13.6.17 PWRGT_STATUS—Offset 61h

Power Gate Status;This register indicates the status of the voltage islands for the various blocks that the P unit controls. This register is updated by the firmware after servicing request from driver to power up / power down of the various islands. Each island is controlled by a 2-bit field. 00 -- no clock or power gating, 01 -- clock gating, 10 -- reset and 11 -- power gating.(Encoding is as follows: subsys 0 RENder, 1 media, 3 -Display, DPIO :subsystem 5 Common lane, subs 6-9 TX, subs 10-11 RX)

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 61h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits	Default	Field
31:30	0 0	PWRGATESTATUS_RESERVED5
29:28	0 0	PWRGATESTATUS_RESERVED4
27:26	0 0	PWRGATESTATUS_RESERVED3
25:24	0 0	PWRGATESTATUS_RESERVED2
23:22	0 0	PWRGATESTATUS_RX1
21:20	0 0	PWRGATESTATUS_RX0
19:18	0 0	PWRGATESTATUS_TX3
17:16	0 0	PWRGATESTATUS_TX2
15:14	0 0	PWRGATESTATUS_TX1
13:12	0 0	PWRGATESTATUS_TX0
11:10	0 0	PWRGATESTATUS_CMNLN
9:8	0 0	PWRGATESTATUS_RESERVED1
7:6	0 0	PWRGATESTATUS_DISPLAY_CTL
5:4	0 0	PWRGATESTATUS_RESERVED0
3:2	0 0	PWRGATESTATUS_MEDIA
1:0	0 0	PWRGATESTATUS_RENDER

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**PWRGATESTATUS_RESERVED5:** Reserved
29:28	0h RW	**PWRGATESTATUS_RESERVED4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
27:26	0h RW	**PWRGATESTATUS_RESERVED3:** Reserved
25:24	0h RW	**PWRGATESTATUS_RESERVED2:** Reserved
23:22	0h RW	**PWRGATESTATUS_RX1:** Power gate status for RX. Status0x03 indicates powered off state, 0x00 indicates powered on state.
21:20	0h RW	**PWRGATESTATUS_RX0:** Power gate status for RX. Status0x03 indicates powered off state, 0x00 indicates powered on state.
19:18	0h RW	**PWRGATESTATUS_TX3:** Power gate status for TX. Status0x03 indicates powered off state, 0x00 indicates powered on state.
17:16	0h RW	**PWRGATESTATUS_TX2:** Power gate status for TX. Status0x03 indicates powered off state, 0x00 indicates powered on state.
15:14	0h RW	**PWRGATESTATUS_TX1:** Power gate status for TX. Status0x03 indicates powered off state, 0x00 indicates powered on state.
13:12	0h RW	**PWRGATESTATUS_TX0:** Power gate status for TX Status0x03 indicates powered off state, 0x00 indicates powered on state.
11:10	0h RW	**PWRGATESTATUS_CMNLN:** Power gate status for common lane. Status0x03 indicates powered off state, 0x00 indicates powered on state. P unit will write this field to register field to reflect the status for power up or power down for the DPIO common lane
9:8	0h RW	**PWRGATESTATUS_RESERVED1:** Reserved
7:6	0h RW	**PWRGATESTATUS_DISPLAY_CTL:** Power gate status for display, Status0x03 indicates powered off state, 0x00 indicates powered on state. P unit will write this field to register field to reflect the status for power up or power down for the Display controller .Driver is expected to poll for the power up status before accessing the IP.
5:4	0h RW	**PWRGATESTATUS_RESERVED0:** Reserved
3:2	0h RW	**PWRGATESTATUS_MEDIA:** Power gate status for media Status0x03 indicates powered off state, 0x00 indicates powered on state. P unit will write this field to register field to reflect the status for power up or power down for the Media IP. The request for power up or power down for media are hardware triggered.
1:0	0h RW	**PWRGATESTATUS_RENDER:** Power gate status for RENder - Status0x03 indicates powered off state, 0x00 indicates powered on state. P unit will write this field to register field to reflect the status for power up or power down for the Render engine. The request for power up or power down for Render are hardware triggered.

13.6.18 PWRGT_INTREN—Offset 62h

Power Gate Interrupt enable;This register indicates the interrupt enables for the power islands for the various blocks that the P unit controls. The software driver sets this bit to trigger an interrupt when the particular subsystem is brought back to D0. There is one bit for each of the subsystem . At reset/powerup, all IE comes up as 0, indicating interrupts are not enabled. (Encoding is as follows: subsys 0 RENder, 1 media, 3 - Display, no control hook for DPIO)

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 62h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bit	Default	Field
31	0	PWRGINTREN_LISLAND_RESERVED12
30	0	PWRGINTREN_LISLAND_RESERVED11
29	0	PWRGINTREN_LISLAND_RESERVED10
28	0	PWRGINTREN_LISLAND_RESERVED9
27	0	PWRGINTREN_LISLAND_RESERVED8
26	0	PWRGINTREN_LISLAND_RESERVED7
25	0	PWRGINTREN_LISLAND_RESERVED6
24	0	PWRGINTREN_LISLAND_RESERVED5
23	0	PWRGINTREN_LISLAND_RESERVED4
22	0	PWRGINTREN_LISLAND_RESERVED3
21	0	PWRGINTREN_LISLAND_RESERVED2
20	0	PWRGINTREN_LISLAND_RESERVED1
19	0	PWRGINTREN_LISLAND_DISPLAY
18	0	PWRGINTREN_LISLAND_RESERVED0
17	0	PWRGINTREN_LISLAND_MEDIA
16	0	PWRGINTREN_LISLAND_RENDER
15	0	PWRGATEINTREN_RESERVED12
14	0	PWRGATEINTREN_RESERVED11
13	0	PWRGATEINTREN_RESERVED10
12	0	PWRGATEINTREN_RESERVED9
11	0	PWRGATEINTREN_RESERVED8
10	0	PWRGATEINTREN_RESERVED7
9	0	PWRGATEINTREN_RESERVED6
8	0	PWRGATEINTREN_RESERVED5
7	0	PWRGATEINTREN_RESERVED4
6	0	PWRGATEINTREN_RESERVED3
5	0	PWRGATEINTREN_RESERVED2
4	0	PWRGATEINTREN_RESERVED1
3	0	PWRGATEINTREN_DISPLAY
2	0	PWRGATEINTREN_RESERVED0
1	0	PWRGATEINTREN_MEDIA
0	0	PWRGATEINTREN_RENDER

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PWRGINTREN_LISLAND_RESERVED12:** Reserved
30	0h RW	**PWRGINTREN_LISLAND_RESERVED11:** Reserved
29	0h RW	**PWRGINTREN_LISLAND_RESERVED10:** Reserved
28	0h RW	**PWRGINTREN_LISLAND_RESERVED9:** Reserved
27	0h RW	**PWRGINTREN_LISLAND_RESERVED8:** Reserved
26	0h RW	**PWRGINTREN_LISLAND_RESERVED7:** Reserved
25	0h RW	**PWRGINTREN_LISLAND_RESERVED6:** Reserved
24	0h RW	**PWRGINTREN_LISLAND_RESERVED5:** Reserved
23	0h RW	**PWRGINTREN_LISLAND_RESERVED4:** Reserved
22	0h RW	**PWRGINTREN_LISLAND_RESERVED3:** Reserved
21	0h RW	**PWRGINTREN_LISLAND_RESERVED2:** Reserved
20	0h RW	**PWRGINTREN_LISLAND_RESERVED1:** Reserved
19	0h RW	**PWRGINTREN_LISLAND_DISPLAY:** power gate Interrupt sts for local standby island display, no control hook for DPIO. Not used for VLV
18	0h RW	**PWRGINTREN_LISLAND_RESERVED0:** Reserved
17	0h RW	**PWRGINTREN_LISLAND_MEDIA:** power gate Interrupt sts for local standby island media. Not used for VLV

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**PWRGINTREN_LISLAND_RENDER:** power gate Interrupt sts for local standby island RENder. Not used for VLV
15	0h RW	**PWRGATEINTREN_RESERVED12:** Reserved
14	0h RW	**PWRGATEINTREN_RESERVED11:** Reserved
13	0h RW	**PWRGATEINTREN_RESERVED10:** Reserved
12	0h RW	**PWRGATEINTREN_RESERVED9:** Reserved
11	0h RW	**PWRGATEINTREN_RESERVED8:** Reserved
10	0h RW	**PWRGATEINTREN_RESERVED7:** Reserved
9	0h RW	**PWRGATEINTREN_RESERVED6:** Reserved
8	0h RW	**PWRGATEINTREN_RESERVED5:** Reserved
7	0h RW	**PWRGATEINTREN_RESERVED4:** Reserved
6	0h RW	**PWRGATEINTREN_RESERVED3:** Reserved
5	0h RW	**PWRGATEINTREN_RESERVED2:** Reserved
4	0h RW	**PWRGATEINTREN_RESERVED1:** Reserved
3	0h RW	**PWRGATEINTREN_DISPLAY:** power gate interrupt status for display, no control hook for DPIO
2	0h RW	**PWRGATEINTREN_RESERVED0:** Reserved
1	0h RW	**PWRGATEINTREN_MEDIA:** power gate interrupt status for media
0	0h RW	**PWRGATEINTREN_RENDER:** power gate interrupt status for RENder

13.6.19 CPU_SOFT_STRAPS—Offset 7Ch

Register for BIOS software configurable CPU Power on Reset Configuration. This register survives CPU-only reset and SOC Warm reset. BIOS can access is register using CFC/CF8 mechanism. Accessible through MSG Bus Port 04h.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 7Ch

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RESERVED_4	POC_NUM_CORES	RESERVED_2	POC_RUN_BIST

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**RESERVED_4:** Reserved
10:8	0h RW	**POC_NUM_CORES:** Core defeature via BIOS...000b Do not defeature IA cores...001b Only 1 Logical Core is active...010b Only 2 Logical Cores are active...011b Only 3 Logical Cores are active...1xxb Reserved (for 8 Core config).. ..Exposed to CPU microcode as CLPU_CR_RESOLVED_CORE_VECTOR, CLPU_CR_RESOLVED_CORE_VECTOR and CLPU_CR_WHO_AM_I via RESET_CONFIG_CW (CPU PMlink space)... ..Punit will determine the RESOLVED_CORE_VECTOR based on the table in HSD Issue 1214773...
7:1	0h RO	**RESERVED_2:** Reserved
0	0h RW	**POC_RUN_BIST:** Writing a 1 will cause the CPU microcode to execute BIST on the L2$ at CPU reset deassertion (CPU only reset or Warm Reset).

13.6.20 PTMC—Offset 80h

Programmable Thermtrip Management Control

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 80h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RESERVED_1	CPU_MOD1	MOD0_THERM_EN	RESERVED_4	SW_TRIGGER	BW_THROT_EN	XXTTS_THERM_EN	PROCHOT_THERM_EN	SVIDVR_ICC_EN	SVID_THERM_EN	RESERVED_11	AUX3_THERM_EN	AUX2_THERM_EN	AUX1_THERM_EN	AUX0_THERM_EN

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**RESERVED_1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**CPU_MOD1:** CPU Module1: Indicates CPU Module0 can trigger thermal event
16	0h RW	**MOD0_THERM_EN:** CPU Module0: Indicates CPU Module0 can trigger thermal event
15:14	0h RO	**RESERVED_4:** Reserved
13	0h RW	**SW_TRIGGER:** Indicates Software can program SWT register to initiate thermal event
12	0h RW	**BW_THROT_EN:** Indicates excess memory bandwidth can trigger a thermal event
11	0h RW	**XXTTS_THERM_EN:** XXTTS (Reserved): Indicates Thermal Sensor from platform can trigger thermal event (Not supported in Valleyview)
10	0h RW	**PROCHOT_THERM_EN:** XXPROCHOT: Inidicates a Platform Prochot can cause thermal event
9	0h RW	**SVIDVR_ICC_EN:** Indicates the VR Icc Max can cause thermal event...The trip is triggered for both Vcc and Vnn
8	0h RW	**SVID_THERM_EN:** sVID(VR_Icc_Max/VR_Hot): Indicates VR status bits can cause thermal event
7:4	0h RO	**RESERVED_11:** Reserved
3	0h RW	**AUX3_THERM_EN:** AUX3: Indicates AUX3 (Hot Trip) can initiate a thermal event
2	0h RW	**AUX2_THERM_EN:** AUX2: Indicates AUX2 can intiate a thermal event
1	0h RW	**AUX1_THERM_EN:** AUX1: Indicates AUX1 can initiate a thermal event
0	0h RW	**AUX0_THERM_EN:** AUX0: Indicates AUX0 can initiate a thermal event

13.6.21 TTR0—Offset 81h

Rank 0 Bandwidth Trip Thresholds

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 81h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED_1				WR_THRESHOLD		RD_THRESHOLD	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED_1:** Reserved
15:8	0h RW	**WR_THRESHOLD:** Write Threshhold (W): Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank0 Write count from the event counters when there is no external thermal sensor configured for DRAM protection.
7:0	0h RW	**RD_THRESHOLD:** Read Threshhold (R): Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank0 Read count from the event counters when there is no external thermal sensor configured for DRAM protection

13.6.22 TTR1—Offset 82h

Rank 1 Bandwidth Trip Thresholds

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 82h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED_1				WR_THRESHOLD		RD_THRESHOLD	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED_1:** Reserved
15:8	0h RW	**WR_THRESHOLD:** Write Threshhold (W): Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank0 Write count from the event counters when there is no external thermal sensor configured for DRAM protection.
7:0	0h RW	**RD_THRESHOLD:** Read Threshhold (R): Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank0 Read count from the event counters when there is no external thermal sensor configured for DRAM protection

13.6.23 TTS—Offset 83h

VLV Bandwidth Trip Thresholds

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 83h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
RESERVED_1 (31:16)					WR_THRESHOLD (15:8)		RD_THRESHOLD (7:0)	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED_1:** Reserved
15:8	0h RW	**WR_THRESHOLD:** Write Threshold: Indicates a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Write count FOR BOTH RANKS from the event counters when there is no iternal thermal sensor configured for VLV protection.
7:0	0h RW	**RD_THRESHOLD:** Read Threshold: Same as Write Threshold but for Reads from BOTH RANKS.

13.6.24 TELB—Offset 84h

Thermal Enforcement Limits for Bandwidth Trips

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 84h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R1_WR_MASK								R1_RD_MASK								R0_WR_MASK								R0_RD_MASK							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**R1_WR_MASK:** Rank 1 Write Mask: Mask writes to Rank1
23:16	0h RW	**R1_RD_MASK:** Rank 1 Read Mask: Mask reads to Rank1
15:8	0h RW	**R0_WR_MASK:** Rank 0 Write Mask: Mask writes to Rank0
7:0	0h RW	**R0_RD_MASK:** Rank 0 Read Mask: Mask reads to Rank0

13.6.25 TELT—Offset 85h

Thermal Enforcement Limits for Thermal Trips

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 85h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R1_WR_MASK								R1_RD_MASK								R0_WR_MASK								R0_RD_MASK							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**R1_WR_MASK:** Rank 1 Write Mask: Mask writes to Rank1
23:16	0h RW	**R1_RD_MASK:** Rank 1 Read Mask: Mask reads to Rank1
15:8	0h RW	**R0_WR_MASK:** Rank 0 Write Mask: Mask writes to Rank0
7:0	0h RW	**R0_RD_MASK:** Rank 0 Read Mask: Mask reads to Rank0

13.6.26 TQPR—Offset 86h

Thermal Trip TQ Poll Rate Register - This register identifies the rate of TQ poll in LPDDR2 memory.

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x04] + 86h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1 (bits 31:3), TQ_POLL_PERIOD (bits 2:0)

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**Reserved_1:** Reserved
2:0	0h RW	**TQ_POLL_PERIOD:** Def TQ Poll Period: This sets the frequency by which the Dunit polls the DRAM mode register MR4 to determine required refresh rate when thermal event occurs. ..000 1 x the current Refresh Period ..001 2 x the current Refresh Period ..010 4 x the current Refresh Period ..011 8 x the current Refresh Period ..100 16 x the current Refresh Period ..101 32 x the current Refresh Period ..110 64 x the current Refresh Period ..111 128 x the current Refresh Period..

13.6.27 GFXT—Offset 88h

GFX Thermals Control - This register is used to enable clock (On clocks) throttling.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 88h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
Reserved_1				TM2_THROT_GFX		Reserved_3		TM1_THROT_GFX

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved_1:** Resered for future use
15:8	0h RW	**TM2_THROT_GFX:** TM2 Control for GFX
7:3	0h RW	**Reserved_3:** Reserved for future use
2:0	0h RW	**TM1_THROT_GFX:** TM1 Throttling for GFx..3 b000: No Throttle..3 b001: 12.5% Throttle..3 b010: 25% Throttle..3 b011: 37.5% Throttle..3 b100: 50% Throttle..3 b101: 67.5% Throttle..3 b110: 75% Throttle..3 b111: 87.5% Throttle..

13.6.28 VEDT—Offset 89h

VED Thermals Control - This register is used to enable clock (On clocks) throttling.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 89h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:8	Bits 7:3	Bits 2:0
Reserved_1	TM2_THROT_VED	Reserved_3	TM1_THROT_VED

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved_1:** Resered for future use
15:8	0h RW	**TM2_THROT_VED:** TM2 Control for VED
7:3	0h RW	**Reserved_3:** Reserved for future use
2:0	0h RW	**TM1_THROT_VED:** TM1 Throttling for Ved..3 b000: No Throttle..3 b001: 12.5% Throttle..3 b010: 25% Throttle..3 b011: 37.5% Throttle..3 b100: 50% Throttle..3 b101: 67.5% Throttle..3 b110: 75% Throttle..3 b111: 87.5% Throttle..

13.6.29 ISPT—Offset 8Ch

ISP Thermals Control - This register is used to enable clock (On clocks) throttling.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 8Ch

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1	Reserved_2	Reserved_3	TM1_THROT_ISP

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved_1:** Resered for future use
15:8	0h RW	**Reserved_2:** Reserved
7:3	0h RW	**Reserved_3:** Reserved for future use
2:0	0h RW	**TM1_THROT_ISP:** TM1 Throttling for ISP..3 b000: No Throttle..3 b001: 12.5% Throttle..3 b010: 25% Throttle..3 b011: 37.5% Throttle..3 b100: 50% Throttle..3 b101: 67.5% Throttle..3 b110: 75% Throttle..3 b111: 87.5% Throttle..

13.6.30 DTSC—Offset B0h

Digital Thermal Sensor Control

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + B0h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED_1																														DTS1_ENABLE	DTS0_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**RESERVED_1:** Reserved
1	0h RW	**DTS1_ENABLE:** DTS 1 Enable (DTSE1): When set, enables power to DTS 1
0	0h RW	**DTS0_ENABLE:** DTS 0 Enable (DTSE0): When set, enables power to DTS 0

13.6.31 TRR—Offset B1h

Thermometer Read register

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + B1h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED_1																DTS1_TEMP_READ								DTS0_TEMP_READ							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED_1:** Reserved
15:8	0h RO	**DTS1_TEMP_READ:** DTS1 Temperature Reading(DTSTR1): Temperature reading from DTS1. This value is only valid after DTS1 is enabled
7:0	0h RO	**DTS0_TEMP_READ:** DTS0 Temperature Reading(DTSTR0): Temperature reading from DTS0. This value is only valid after DTS0 is enabled

13.6.32 PTPS—Offset B2h

Programmable trip Point settings

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + B2h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AUX3_TRIP_POINT								AUX2_TRIP_POINT								AUX1_TRIP_POINT								AUX0_TRIP_POINT							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**AUX3_TRIP_POINT:** Aux3 Trip Point Setting
23:16	0h RW	**AUX2_TRIP_POINT:** Aux2 Trip Point Setting
15:8	0h RW	**AUX1_TRIP_POINT:** Aux1 Trip Point Setting
7:0	0h RW	**AUX0_TRIP_POINT:** Aux0 Trip Point Setting

13.6.33 PTTS—Offset B3h

Programmable Thermal trip Status

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + B3h

Op Codes:
h - Read, h - Write

Default: 00000000h

31:18	17	16	15:14	13	12	11	10	9	8	7:4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0 0	0	0	0	0	0	0	0 0 0 0	0	0	0	0
RESERVED_1	MOD1_THERM_STATUS	MOD0_THERM_STATUS	RESERVED_4	SWT	BW_STATUS	THERMAL_STATUS	PROCHOT_THERM_STATUS	VR_ICC_THERM_STATUS	VR_HOT_THERM_STATUS	RESERVED_11	AUX3_THERM_STATUS	AUX2_THERM_STATUS	AUX1_THERM_STATUS	AUX0_THERM_STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**RESERVED_1:** Reserved
17	0h RO	**MOD1_THERM_STATUS:** CPU Module1: CPU Module 1 Trip Status
16	0h RO	**MOD0_THERM_STATUS:** CPU Module0: CPU Module 0 Trip Status
15:14	0h RO	**RESERVED_4:** Reserved
13	0h RO	**SWT:** Status to indicate that SW initiated a thermal event
12	0h RO	**BW_STATUS:** BW status
11	0h RO	**THERMAL_STATUS:** XXTTS (Reserved): Platform Thermal Sensor Status
10	0h RO	**PROCHOT_THERM_STATUS:** XXPROCHOT: Platform Prochot Status
9	0h RO	**VR_ICC_THERM_STATUS:** VR_Icc_Max: VR Icc Max Thermal Status
8	0h RO	**VR_HOT_THERM_STATUS:** VR_Hot: VR Hot Thermal Status
7:4	0h RO	**RESERVED_11:** Reserved
3	0h RO	**AUX3_THERM_STATUS:** AUX3: SoC PROCHOT/AUX3 Thermtrip Status
2	0h RO	**AUX2_THERM_STATUS:** AUX2: AUX2 Thermal Trip Status
1	0h RO	**AUX1_THERM_STATUS:** AUX1: AUX2 Thermal Trip Status
0	0h RO	**AUX0_THERM_STATUS:** AUX0: AUX2 Thermal Trip Status

13.6.34 PTTSS—Offset B4h

Programmable Thermal trip Sticky Status (NOTE: 1. Sticky status register is cleared by writing a 1 to it by software)

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + B4h

Op Codes:
h - Read, h - Write

Default: 00000000h

31:18	17	16	15:14	13	12	11	10	9	8	7:4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0 0	0	0	0	0	0	0	0 0 0 0	0	0	0	0
RESERVED_1	MOD1_THERM_STATUS	MOD0_THERM_STATUS	RESERVED_4	SWT	BW_STATUS	THERMAL_STATUS	PROCHOT_THERM_STATUS	VR_ICC_THERM_STATUS	VR_HOT_THERM_STATUS	RESERVED_11	AUX3_THERM_STATUS	AUX2_THERM_STATUS	AUX1_THERM_STATUS	AUX0_THERM_STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**RESERVED_1:** Reserved
17	0h RW	**MOD1_THERM_STATUS:** CPU Module1: CPU Module 1 Trip Status
16	0h RW	**MOD0_THERM_STATUS:** CPU Module0: CPU Module 0 Trip Status
15:14	0h RO	**RESERVED_4:** Reserved
13	0h RO	**SWT:** Status to indicate that SW initiated a thermal event
12	0h RO	**BW_STATUS:** BW status
11	0h RO	**THERMAL_STATUS:** XXTTS (Reserved): Platform Thermal Sensor Status
10	0h RW	**PROCHOT_THERM_STATUS:** XXPROCHOT: Platform Prochot Status
9	0h RW	**VR_ICC_THERM_STATUS:** VR_Icc_Max: VR Icc Max Thermal Status
8	0h RW	**VR_HOT_THERM_STATUS:** VR_Hot: VR Hot Thermal Status
7:4	0h RO	**RESERVED_11:** Reserved
3	0h RW	**AUX3_THERM_STATUS:** AUX3: SoC PROCHOT/AUX3 Thermtrip Status

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**AUX2_THERM_STATUS:** AUX2: AUX2 Thermal Trip Status
1	0h RW	**AUX1_THERM_STATUS:** AUX1: AUX2 Thermal Trip Status
0	0h RW	**AUX0_THERM_STATUS:** AUX0: AUX2 Thermal Trip Status

13.6.35 TE_AUX0—Offset B5h

Thermal Event Aux0

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + B5h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits	31:19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	RESERVED_1	SLM1_PROCHOT_ENABLE	SLM0_PROCHOT_ENABLE	XXPROCHOT_ENABLE	RESERVED_5	Assert_APICA	TQ_POLL	iUnitTM1	MSI_ENABLE	SMI_ENABLE	SCI_ENABLE	SATA_THROTTLE_ENABLE	VSP_TM1_ENABLE	VEC_TM1_ENABLE	VED_TM1_ENABLE	GFX_VNN_THROT	GFX_TM2_ENABLE	GFX_TM1_ENABLE	BW_THROT_ENABLE	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15	0h RO	**RESERVED_5:** Reserved
14	0h RW	**Assert_APICA:** Assert_APICA Enable
13	0h RW	**TQ_POLL:** TQ Poll rate Increase
12	0h RW	**iUnitTM1:** iUnit TM1

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7	0h RW	**VSP_TM1_ENABLE:** VSP TM1 Enable
6	0h RW	**VEC_TM1_ENABLE:** VEC TM1 Enable
5	0h RW	**VED_TM1_ENABLE:** VED TM1 Enable
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.36 TE_AUX1—Offset B6h

Thermal Event Aux1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + B6h

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits	Default	Field
31:19	0 0 0 0 0 0 0 0 0 0 0 0 0	RESERVED_1
18	0	SLM1_PROCHOT_ENABLE
17	0	SLM0_PROCHOT_ENABLE
16	0	XXPROCHOT_ENABLE
15	0	RESERVED_5
14	0	Assert_APICA
13:12	0 0	RESERVED_7
11	0	MSI_ENABLE
10	0	SMI_ENABLE
9	0	SCI_ENABLE
8	0	SATA_THROTTLE_ENABLE
7:5	0 0 0	RESERVED_12
4	0	GFX_VNN_THROT
3	0	GFX_TM2_ENABLE
2	0	GFX_TM1_ENABLE
1	0	BW_THROT_ENABLE
0	0	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15	0h RW	**RESERVED_5:** Reserved
14	0h RW	**Assert_APICA:** Assert_APICA Enable
13:12	0h RW	**RESERVED_7:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_12:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.37 TE_AUX2—Offset B7h

Thermal Event Aux2

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + B7h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_1	SLM1_PROCHOT_ENABLE	SLM0_PROCHOT_ENABLE	XXPROCHOT_ENABLE	RESERVED_5	Assert_APICA	RESERVED_7	MSI_ENABLE	SMI_ENABLE	SCI_ENABLE	SATA_THROTTLE_ENABLE	RESERVED_12	GFX_VNN_THROT	GFX_TM2_ENABLE	GFX_TM1_ENABLE	BW_THROT_ENABLE	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15	0h RW	**RESERVED_5:** Reserved
14	0h RW	**Assert_APICA:** Assert_APICA Enable

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**RESERVED_7:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_12:** Reserved
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.38 TE_AUX3—Offset B8h

Thermal Event Aux3

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + B8h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED_1													SLM1_PROCHOT_ENABLE	SLM0_PROCHOT_ENABLE	XXPROCHOT_ENABLE	RESERVED_5	Assert_APICA	RESERVED_7		MSI_ENABLE	SMI_ENABLE	SCI_ENABLE	SATA_THROTTLE_ENABLE	RESERVED_12			GFX_VNN_THROT	GFX_TM2_ENABLE	GFX_TM1_ENABLE	BW_THROT_ENABLE	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15	0h RW	**RESERVED_5:** Reserved
14	0h RW	**Assert_APICA:** Assert_APICA Enable
13:12	0h RW	**RESERVED_7:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_12:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.39 TTE_VRIccMax—Offset B9h

Thermal Trip Event VR_Icc_MAX

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + B9h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:19	RESERVED_1
18	SLM1_PROCHOT_ENABLE
17	SLM0_PROCHOT_ENABLE
16	XXPROCHOT_ENABLE
15:12	RESERVED_5
11	MSI_ENABLE
10	SMI_ENABLE
9	SCI_ENABLE
8	SATA_THROTTLE_ENABLE
7:5	RESERVED_10
4	GFX_VNN_THROT
3	GFX_TM2_ENABLE
2	GFX_TM1_ENABLE
1	BW_THROT_ENABLE
0	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15:12	0h RW	**RESERVED_5:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_10:** Reserved
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.40 TTE_VRHot—Offset BAh

Thermal Trip Event VR_Hot

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + BAh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:19	RESERVED_1
18	SLM1_PROCHOT_ENABLE
17	SLM0_PROCHOT_ENABLE
16	XXPROCHOT_ENABLE
15:12	RESERVED_5
11	MSI_ENABLE
10	SMI_ENABLE
9	SCI_ENABLE
8	SATA_THROTTLE_ENABLE
7:5	RESERVED_10
4	GFX_VNN_THROT
3	GFX_TM2_ENABLE
2	GFX_TM1_ENABLE
1	BW_THROT_ENABLE
0	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15:12	0h RW	**RESERVED_5:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_10:** Reserved
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.41 TTE_XXPROCHOT—Offset BBh

Thermal Trip Event XXPROCHOT

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + BBh

Op Codes:
h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0 0 0 0	0	0	0	0	0 0 0	0	0	0	0	0
RESERVED_1	SLM1_PROCHOT_ENABLE	SLM0_PROCHOT_ENABLE	XXPROCHOT_ENABLE	RESERVED_5	MSI_ENABLE	SMI_ENABLE	SCI_ENABLE	SATA_THROTTLE_ENABLE	RESERVED_10	GFX_VNN_THROT	GFX_TM2_ENABLE	GFX_TM1_ENABLE	BW_THROT_ENABLE	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15:12	0h RW	**RESERVED_5:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_10:** Reserved
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.42 TTE_SLM0—Offset BCh

Thermal Trip Event SLM0

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + BCh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED_1													SLM1_PROCHOT_ENABLE	SLM0_PROCHOT_ENABLE	XXPROCHOT_ENABLE	RESERVED_5				MSI_ENABLE	SMI_ENABLE	SCI_ENABLE	SATA_THROTTLE_ENABLE	RESERVED_10			GFX_VNN_THROT	GFX_TM2_ENABLE	GFX_TM1_ENABLE	BW_THROT_ENABLE	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15:12	0h RW	**RESERVED_5:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_10:** Reserved
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.43 TTE_SLM1—Offset BDh

Thermal Trip Event SLM1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + BDh

Op Codes:
h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED_1	SLM1_PROCHOT_ENABLE	SLM0_PROCHOT_ENABLE	XXPROCHOT_ENABLE	RESERVED_5	MSI_ENABLE	SMI_ENABLE	SCI_ENABLE	SATA_THROTTLE_ENABLE	RESERVED_10	GFX_VNN_THROT	GFX_TM2_ENABLE	GFX_TM1_ENABLE	BW_THROT_ENABLE	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15:12	0h RW	**RESERVED_5:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_10:** Reserved
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.44 BWTE—Offset BEh

Band width Trip Event

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + BEh

Op Codes:

h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:19	RESERVED_1
18	SLM1_PROCHOT_ENABLE
17	SLM0_PROCHOT_ENABLE
16	XXPROCHOT_ENABLE
15:12	RESERVED_5
11	MSI_ENABLE
10	SMI_ENABLE
9	SCI_ENABLE
8	SATA_THROTTLE_ENABLE
7:5	RESERVED_10
4	GFX_VNN_THROT
3	GFX_TM2_ENABLE
2	GFX_TM1_ENABLE
1	BW_THROT_ENABLE
0	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**RESERVED_5:** Reserved
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7:5	0h RO	**RESERVED_10:** Reserved
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.45 TTE_SWT—Offset BFh

Thermal trip event for software initiated thermal event

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + BFh

Op Codes:
h - Read, h - Write

Default: 00000000h

Bits	Value	Field
31:19	0 0 0 0 0 0 0 0 0 0 0 0 0	RESERVED_1
18	0	SLM1_PROCHOT_ENABLE
17	0	SLM0_PROCHOT_ENABLE
16	0	XXPROCHOT_ENABLE
15:14	0 0	RESERVED_5
13	0	TQ_POLL
12	0	iUnitTM1
11	0	MSI_ENABLE
10	0	SMI_ENABLE
9	0	SCI_ENABLE
8	0	SATA_THROTTLE_ENABLE
7	0	VSP_TM1_ENABLE
6	0	VEC_TM1_ENABLE
5	0	VED_TM1_ENABLE
4	0	GFX_VNN_THROT
3	0	GFX_TM2_ENABLE
2	0	GFX_TM1_ENABLE
1	0	BW_THROT_ENABLE
0	0	DDR_REFRESH_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**RESERVED_1:** Reserved
18	0h RW	**SLM1_PROCHOT_ENABLE:** SLM1 PROCHOT Enable(Reserved for VLV)
17	0h RW	**SLM0_PROCHOT_ENABLE:** SLM0 PROCHOT Enable
16	0h RW	**XXPROCHOT_ENABLE:** XXPROCHOT Note: Unless in debug mode enable XXPROCHOT with caution because XXPROCHOT feedsback into SoC via the Bi-Directional IO and could cause XXPROCHOT to trip as well
15:14	0h RO	**RESERVED_5:** Reserved
13	0h RW	**TQ_POLL:** TQ Poll rate Increase
12	0h RW	**iUnitTM1:** iUnit TM1
11	0h RW	**MSI_ENABLE:** MSI Enable
10	0h RW	**SMI_ENABLE:** SMI Enable
9	0h RW	**SCI_ENABLE:** SCI Enable
8	0h RW	**SATA_THROTTLE_ENABLE:** SATA Throttle Enable
7	0h RW	**VSP_TM1_ENABLE:** VSP TM1 Enable
6	0h RW	**VEC_TM1_ENABLE:** VEC TM1 Enable
5	0h RW	**VED_TM1_ENABLE:** VED TM1 Enable
4	0h RW	**GFX_VNN_THROT:** Graphics Vnn Throttle (Reserved for VLV)
3	0h RW	**GFX_TM2_ENABLE:** GFX TM2 Enable....
2	0h RW	**GFX_TM1_ENABLE:** GFX TM1 Enable....
1	0h RW	**BW_THROT_ENABLE:** BW throttle Enable
0	0h RW	**DDR_REFRESH_ENABLE:** DDR 2X refresh Enable

13.6.46 PUNIT_GPU_EC—Offset D1h

Punit GPU Energy Counter Register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + D1h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPU_EC

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GPU_EC:** GPU Energy Counter Information

13.6.47 PUNIT_GPU_EC_VIRUS—Offset D2h

Punit GPU Energy Counter Virus Register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + D2h

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPU_EC_VIRUS

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GPU_EC_VIRUS:** Initialized to the Virus count value of GPU_EC.

13.6.48 PUNIT_GPU_LFM—Offset D3h

Punit GPU LFM Register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + D3h

Op Codes:
h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

SPARE_BITS | GPU_LFM

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**SPARE_BITS:** Bits to be used in future
7:0	0h RW	**GPU_LFM:** Lowest supported GFX frequency.

13.6.49 PUNIT_GPU_FREQ_REQ—Offset D4h

Punit GPU Frequency Request Register

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + D4h

Op Codes:
h - Read, h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

SPARE_BITS | GFXFREQWISH

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**SPARE_BITS:** Bits to be used in future
7:0	0h RW	**GFXFREQWISH:** Doorbell Register, Frequency Encoding for Frequency Requested in GFX Reg used by Render. For actual frequency encoding please refer Graphics HAS

13.6.50 PUNIT_GPU_FREQ_STS—Offset D8h

Punit GPU Frequency Status Register

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x04] + D8h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RESERVED_7	STATUSFREQID	CZ_CLK_FREQ	RESERVED_4	GPLLENABLE	RESERVED_2	GENFREQSTATUS

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED_7:** Reserved for future use
15:8	0h RO	**STATUSFREQID:** Frequency Encoding for the Frequency Reached
7:6	0h RO	**CZ_CLK_FREQ:** CZ clock Freq encoding is as follows: 00 = 800, 01=1066, 10=1333, 11=Invalid
5	0h RO	**RESERVED_4:** Reserved for future use
4	0h RO	**GPLLENABLE:** 0=graphics clocks not from GPLL...1=graphics clocks from GPLL...
3:1	0h RO	**RESERVED_2:** Reserved for future use
0	0h RO	**GENFREQSTATUS:** Status Register bit to be optionally used by Graphics Driver. This bit Indicates that frequency change is in progress

13.6.51 DPTF_TELB—Offset 108h

Thermal Enforcement Limits for Bandwidth Trips. Write to this Register also triggers Punit to take action to execute. In the RTL the register is listed as MMIO_SPARE4

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x04] + 108h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

R1_WR_MASK	R1_RD_MASK	R0_WR_MASK	R0_RD_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**R1_WR_MASK:** Rank 1 Write Mask: Mask writes to Rank1
23:16	0h RW	**R1_RD_MASK:** Rank 1 Read Mask: Mask reads to Rank1
15:8	0h RW	**R0_WR_MASK:** Rank 0 Write Mask: Mask writes to Rank0
7:0	0h RW	**R0_RD_MASK:** Rank 0 Read Mask: Mask reads to Rank0

13.6.52 DPTF_GFXT—Offset 109h

GFX Thermals Control - This register is used to enable clock (On clocks) throttling.Write to this Register also triggers Punit to take action to execute. In the RTL the register is listed as MMIO_SPARE5

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x04] + 109h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Reserved_1	TM2_THROT_GFX	Reserved_3	TM1_THROT_GFX

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved_1:** Resered for future use
15:8	0h RW	**TM2_THROT_GFX:** TM2 Control for GFX
7:3	0h RW	**Reserved_3:** Reserved for future use

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**TM1_THROT_GFX:** TM1 Throttling for GFx..3 b000: No Throttle..3 b001: 12.5% Throttle..3 b010: 25% Throttle..3 b011: 37.5% Throttle..3 b100: 50% Throttle..3 b101: 67.5% Throttle..3 b110: 75% Throttle..3 b111: 87.5% Throttle..

13.6.53 DPTF_VEDT—Offset 10Ah

VED Thermals Control - This register is used to enable clock (On clocks) throttling.Write to this Register also triggers Punit to take action to execute. In the RTL the register is listed as MMIO_SPARE6

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 10Ah

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:8	Bits 7:3	Bits 2:0
Reserved_1	TM2_THROT_VED	Reserved_3	TM1_THROT_VED

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved_1:** Resered for future use
15:8	0h RW	**TM2_THROT_VED:** TM2 Control for VED
7:3	0h RW	**Reserved_3:** Reserved for future use
2:0	0h RW	**TM1_THROT_VED:** TM1 Throttling for Ved..3 b000: No Throttle..3 b001: 12.5% Throttle..3 b010: 25% Throttle..3 b011: 37.5% Throttle..3 b100: 50% Throttle..3 b101: 67.5% Throttle..3 b110: 75% Throttle..3 b111: 87.5% Throttle..

13.6.54 DPTF_VECT—Offset 10Bh

VEC Thermals Control - This register is used to enable clock (On clocks) throttling.Write to this Register also triggers Punit to take action to execute. In the RTL the register is listed as MMIO_SPARE7

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 10Bh

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1																Reserved_2								Reserved_3					TM1_THROT_GFX		

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved_1:** Resered for future use
15:8	0h RW	**Reserved_2:** Reserved
7:3	0h RW	**Reserved_3:** Reserved for future use
2:0	0h RW	**TM1_THROT_GFX:** TM1 Throttling for Vec..3 b000: No Throttle..3 b001: 12.5% Throttle..3 b010: 25% Throttle..3 b011: 37.5% Throttle..3 b100: 50% Throttle..3 b101: 67.5% Throttle..3 b110: 75% Throttle..3 b111: 87.5% Throttle..

13.6.55 DPTF_VSPT—Offset 10Ch

VSP Thermals Control - This register is used to enable clock (On clocks) throttling.Write to this Register also triggers Punit to take action to execute. In the RTL the register is listed as MMIO_SPARE8

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 10Ch

Op Codes:
h - Read, h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1																Reserved_2								Reserved_3					TM1_THROT_GFX		

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved_1:** Resered for future use
15:8	0h RW	**Reserved_2:** Reserved
7:3	0h RW	**Reserved_3:** Reserved for future use

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**TM1_THROT_GFX:** TM1 Throttling for Vsp..3 b000: No Throttle..3 b001: 12.5% Throttle..3 b010: 25% Throttle..3 b011: 37.5% Throttle..3 b100: 50% Throttle..3 b101: 67.5% Throttle..3 b110: 75% Throttle..3 b111: 87.5% Throttle..

13.6.56 DPTF_ISPT—Offset 10Dh

ISP Thermals Control - This register is used to enable clock (On clocks) throttling.Write to this Register also triggers Punit to take action to execute. In the RTL the register is listed as MMIO_SPARE9

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 10Dh

Op Codes:
h - Read, h - Write

Default: 00000000h

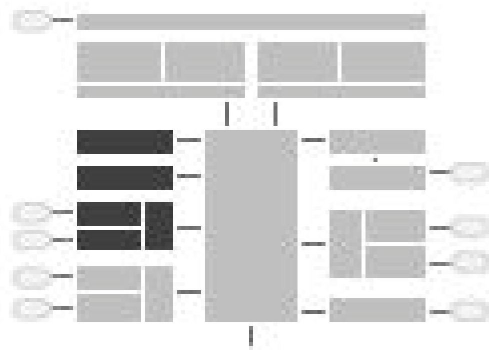
Bits	31:16	15:8	7:3	2:0
Default	0000 0000 0000 0000	0000 0000	0000 0	000
Field	Reserved_1	Reserved_2	Reserved_3	TM1_THROT_ISP

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved_1:** Resered for future use
15:8	0h RW	**Reserved_2:** Reserved
7:3	0h RW	**Reserved_3:** Reserved for future use
2:0	0h RW	**TM1_THROT_ISP:** TM1 Throttling for ISP..3 b000: No Throttle..3 b001: 12.5% Throttle..3 b010: 25% Throttle..3 b011: 37.5% Throttle..3 b100: 50% Throttle..3 b101: 67.5% Throttle..3 b110: 75% Throttle..3 b111: 87.5% Throttle..

14 Graphics, Video and Display

This section provides an overview of Graphics, Video and Display features of the SoC.

This chapter and all contents in it are not applicable to E3805 SKU.

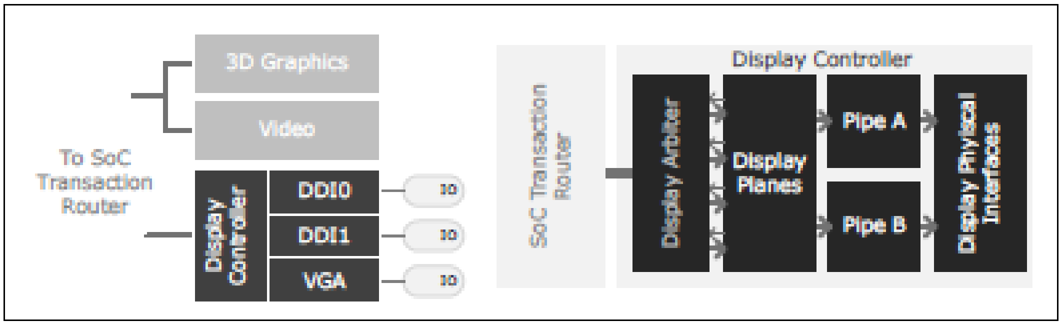


14.1 Features

The key features of the individual blocks are as follows:

- Refreshed seventh generation Intel graphics core with four Execution Units (EUs)
  - 3D graphics hardware acceleration including support for DirectX*11, OCL 1.2, OGL ES Halti/2.0/1.1, OGL 3.2
  - Video decode hardware acceleration including support for H.264, MPEG2, MVC, VC-1, WMV9, JPEG/MJPEG and VP8 formats
  - Video encode hardware acceleration including support for H.264 and MPEG2
  - Display controller, incorporating the display planes, pipes and physical interfaces
  - Four planes available per pipe - 1x Primary, 2x Video Sprite and 1x Cursor- plus a single legacy VGA plane
  - A single Analog Display physical interface, implementing VGA support
  - Two multi-purpose Digital Display Interface (DDI) PHYs implementing HDMI, DVI, DisplayPort (DP) or Embedded DisplayPort (eDP) support

14.2 SoC Graphics Display



The Processor Graphics controller display pipe can be broken down into three components:

- Display Planes
- Display Pipes
- Display Physical Interfaces

A display plane is a single displayed surface in memory and contains one image (desktop, cursor, overlay). It is the portion of the display hardware logic that defines the format and location of a rectangular region of memory that can be displayed on a display output device and delivers that data to a display pipe. This is clocked by the Core Display Clock.

14.2.1 Primary Planes A and B

Planes A and B are the main display planes and are associated with Pipes A and B respectively. Each plane supports per-pixel alpha blending.

14.2.2 Video Sprite Planes A, B, C and D

Video Sprite Planes A, B, C and D are planes optimized for video decode. Planes A and B are associated with Pipe A and Planes C and D are associated with Pipe B.

14.2.3 Cursors A and B

Cursors A and B are small, fixed-sized planes dedicated for mouse cursor acceleration, and are associated with Planes A and B respectively.

14.2.4 VGA

VGA is used for boot, safe mode, legacy games, etc. It can be changed by an application without OS/driver notification, due to legacy requirements.

14.3 Display Pipes

The display pipe blends and synchronizes pixel data received from one or more display planes and adds the timing of the display output device upon which the image is displayed.

The display pipes A and B operate independently of each other at the rate of one pixel per clock. They can attach to any of the display interfaces.

14.4 Display Physical Interfaces

The display physical interfaces consist of output logic and pins that transmit the display data to the associated encoding logic and send the data to the display device. These interfaces can be subdivided into analog (VGA) and digital (DisplayPort*, Embedded DisplayPort*, DVI and HDMI*) interfaces.

14.4.1 Analog Display Physical Interface

The analog port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated Display Data Channel (DDC) signal pair dedicated to the analog port. The intended target device is for a monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactorily but no functionality is added to the signals to enhance that capability.

14.4.1.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function.

Table 165. Analog Display Interface Signals

Signal Name	Direction Plat. Power	Description
VGA_BLUE	O VVGA_GPIO	**Blue Analog Video Output:** This signal is a VGA Analog video output from the internal color palette DAC.
VGA_GREEN	O VVGA_GPIO	**Green Analog Video Output:** This signal is a VGA Analog video output from the internal color palette DAC.
VGA_RED	O VVGA_GPIO	**Red Analog Video Output:** This signal is a VGA Analog video output from the internal color palette DAC.
VGA_HSYNC	O VVGA_GPIO	**VGA Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or "sync interval".

Table 165. Analog Display Interface Signals

Signal Name	Direction Plat. Power	Description
VGA_VSYNC	O VVGA_GPIO	**VGA Vertical Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or "sync interval".
VGA_DDCCLK	I/O VVGA_GPIO	**VGA DDC Clock:** EDID support for an external VGA display
VGA_DDCDATA	I/O VVGA_GPIO	**VGA DDC Data:** EDID support for an external VGA display
VGA_IREF	I	**Resistor Set:** Set point resistor for the internal color palette DAC. A 357ohm+/-0.5% precision resistor is required between VGA_IREF and motherboard ground.
VGA_IRTN	O	This signal is the complement video signal output from the internal color palette DAC channels and this signal connects directly to the ground plane of the board.
LPC_RCOMP	-	VGA Impedance Compensation.

14.4.1.2 Features

Table 166 lists the characteristics of the analog port.

Table 166. Analog Port Characteristics

Signal	Port Characteristics	Support
RGB	Voltage range	0.7 Vp-p nominal only
	CRT/Monitor sense	Analog compare
	Analog copy protection	No
	Sync on green	No
HSYNC VSYNC	Voltage	3.3 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite sync support	No
	Special flat panel sync	No
	Stereo sync	No
DDC	Voltage	External buffered to 5 V
	Control	Through GPIO interface

14.4.1.2.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the VGA monitor. The SoC integrated 320 MHz RAMDAC supports resolutions up to 2560x1600 at 60 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

14.4.1.2.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support are included.

14.4.1.2.3 VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

14.4.1.2.4 Display Data Channel (DDC)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented. The SoC uses the VGA_DDCCLK and VGA_DDCDATA signals to communicate with the analog monitor. The SoC does not generate these signals at 5 V so external pull-up resistors and level shifting circuitry should be implemented on the board.

14.4.2 Digital Display Interfaces

14.4.2.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 167. Display Physical Interfaces Signal Names (Sheet 1 of 2)

Signal Name	Direction	Description	
		HDMI / DVI	DP / eDP
DDI[1,0]_TXP[0] DDI[1,0]_TXP[1] DDI[1,0]_TXP[2] DDI[1,0]_TXP[3]	O	**Ports 1,0: Transmit Signals**	
		TMDS[1,0]_DATAP[2] TMDS[1,0]_DATAP[1] TMDS[1,0]_DATAP[0] TMDS[1,0]_CLKP	DP[1,0]_MAINP[0] DP[1,0]_MAINP[1] DP[1,0]_MAINP[2] DP[1,0]_MAINP[3]

Table 167. Display Physical Interfaces Signal Names (Sheet 2 of 2)

Signal Name	Direction	Description	
		HDMI / DVI	**DP / eDP**
DDI[1,0]_TXN[0] DDI[1,0]_TXN[1] DDI[1,0]_TXN[2] DDI[1,0]_TXN[3]	O	**Ports 1,0: Transmit Complement Signals**	
		TMDS[1,0]_DATAN[2] TMDS[1,0]_DATAN[1] TMDS[1,0]_DATAN[0] TMDS[1,0]_CLKN	DP[1,0]_MAINN[0] DP[1,0]_MAINN[1] DP[1,0]_MAINN[2] DP[1,0]_MAINN[3]
DDI[1,0]_AUXP	I/O	**Ports 1,0: Display Port Auxiliary Channel**	
		Unused	DP[1,0]_AUXP
DDI[1,0]_AUXN	I/O	**Ports 1,0: Display Port Auxiliary Channel Complement**	
		Unused	DP[1,0]_AUXN
DDI[1,0]_HPD	I	**Ports 1,0: Hot Plug Detect**	
		TMDS[1,0]_HPD	DP[1,0]_HPD
DDI[1,0]_DDCCLK	I/O	**Ports 1,0: DDC Clock**	
		TMDS[1,0]_DDCCLK	Unused
DDI[1,0]_DDCDATA	I/O	**Ports 1,0: DDC Data**	
		TMDS[1,0]_DDCDATA	DP[1,0]_EN - Port 0 Enable Strap
DDI[1,0]_BKLTCTL	O	**Ports 1,0: Panel Backlight Brightness Control**	
		HDMI / DVI / DP	**eDP Only**
		Unused	EDP[1,0]_BKLTCTL
DDI[1,0]_BKLTEN	O	**Ports 1,0: Panel Backlight Enable**	
		HDMI / DVI / DP	**eDP Only**
		Unused	EDP[1,0]_BKLTEN
DDI[1,0]_VDDEN	O	**Ports 1,0: Panel Power Enable**	
		HDMI / DVI / DP	**eDP Only**
		Unused	EDP[1,0]_VDDEN
DDI_RCOMP_P/N	I/O	**DDI RCOMP** This signal is used for pre-driver slew rate compensation. An external precision resistor of 402 Ω ±1% should be connected between DDI_RCOMP_P and DDI_RCOMP_N.	

14.4.2.2 Features

14.4.2.3 High Definition Multimedia Interface

The High-Definition Multimedia Interface (HDMI) is provided for transmitting digital audio and video signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. HDMI display interface connecting the SoC and display devices utilizes transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) (not supported by the SoC). As shown in Figure 91 the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the sink.

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the SoC are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

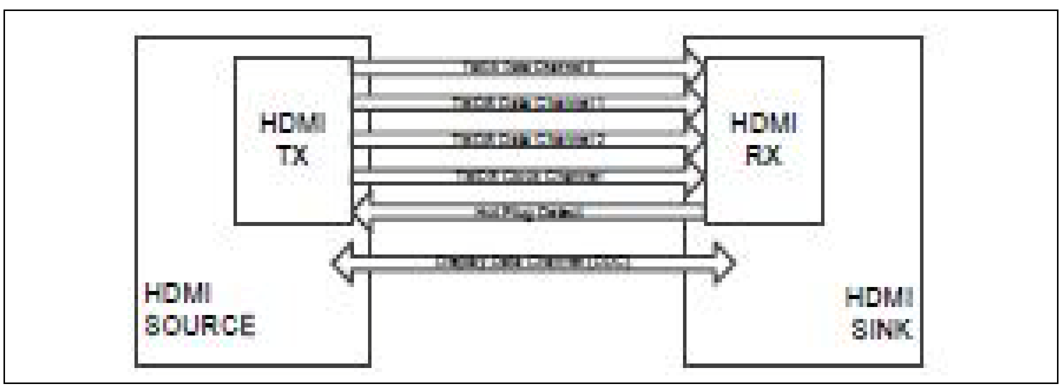
The SoC HDMI interface is designed as per the High-Definition Multimedia Interface Specification 1.4. The SoC supports High-Definition Multimedia Interface Compliance Test Specification 1.4.

14.4.2.3.1 Stereoscopic Support on HDMI

SoC display supports HDMI 1.4 3D video formats. If the HDMI panel is detected to support 3D video format then the SW driver will program Pipe2dB for the correct pipe timing parameters.

The left and right frames can be loaded from independent frame buffers in the main memory. Depending on the input S3D format, the display controller can be enabled do perform frame repositioning, image scaling, line interleaving.

Figure 91. HDMI Overview



14.4.2.4 Digital Video Interface (DVI)

The Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver which is similar to the HDMI protocol but without the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. To drive DVI-I through the back panel the VGA DDC signals are connected along with the digital data and clock signals from one of the Digital Ports. When a system has support for a DVI-I port, then either VGA or the DVI-D through a single DVI-I connector can be driven but not both simultaneously.

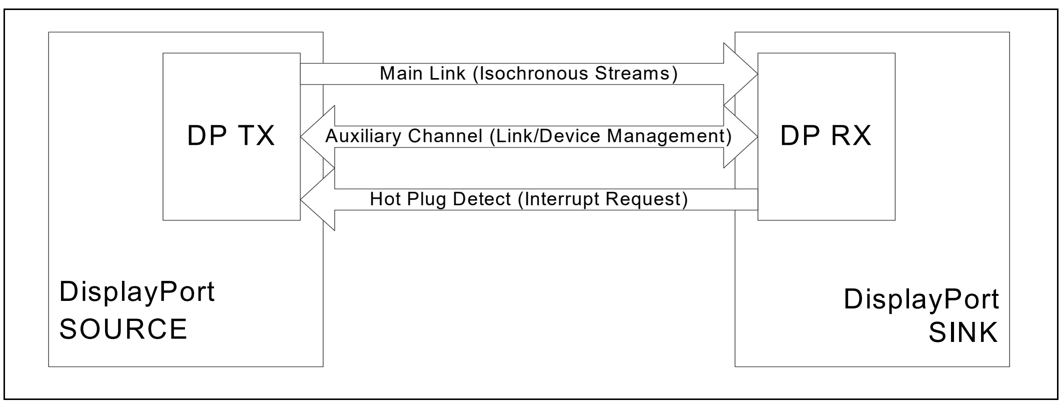
14.4.2.5 Display Port

Display Port is a digital communication interface that utilizes differential signalling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. Display Port is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

A Display Port consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a uni-directional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The SoC supports DisplayPort Standard Version 1.1.

Figure 92. DisplayPort* Overview



14.4.2.6 Embedded DisplayPort (eDP)

Embedded DisplayPort (eDP) is a embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. eDP is supported only on Digital Display Interfaces 0 and/or 1. Like DisplayPort, Embedded DisplayPort also consists of a Main Link, Auxiliary channel, and a optional Hot Plug Detect signal.

Each eDP port can be configured for up-to 4 lanes.

The SoC supports Embedded DisplayPort Standard Version 1.3.

14.4.2.6.1 DisplayPort Auxiliary Channel

A bidirectional AC coupled AUX channel interface replaces the I^2C for EDID read, link management and device control. I^2C-to-Aux bridges are required to connect legacy display devices.

14.4.2.6.2 Hot-Plug Detect (HPD)

The SoC supports HPD for Hot-Plug sink events on the HDMI and DisplayPort interfaces.

14.4.2.6.3 Integrated Audio over HDMI and DisplayPort

SoC can support two audio streams on DP/HDMI ports. Each stream can be programmable to either DDI port. HDMI/DP audio streams can be sent with video streams as follows.

LPE mode: In this mode the uncompressed or compressed audio sample buffers are generated either by OS the audio stack or by audio Lower Power Engine (LPE) and stored in system memory.The display controller fetches audio samples from these buffers, forms an SPDIF frame with VUCP and preamble (if needed), then sends out with video packets.

14.4.2.6.4 High-Bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, etc.) and the sink (panels, monitor, and TV). The SoC supports HDCP 1.4 for content protection over wired displays (HDMI, DisplayPort and Embedded DisplayPort).

14.5 References

- High-Definition Multimedia Interface Specification, Version 1.4
- High-bandwidth Digital Content Protection System, Revision 1.4
- VESA DisplayPort Standard, Version 1.1
- VESA Embedded DisplayPort Standard, Version 1.3

14.6 3D Graphics and Video

The SoC implements a derivative of the Generation 7 graphics engine which consists of rendering engine and bit stream encoder/decoder engine. The rendering engine is used for 3D rendering, media compositing and video encoding. The Graphics engine is built around four execution units (EUs).

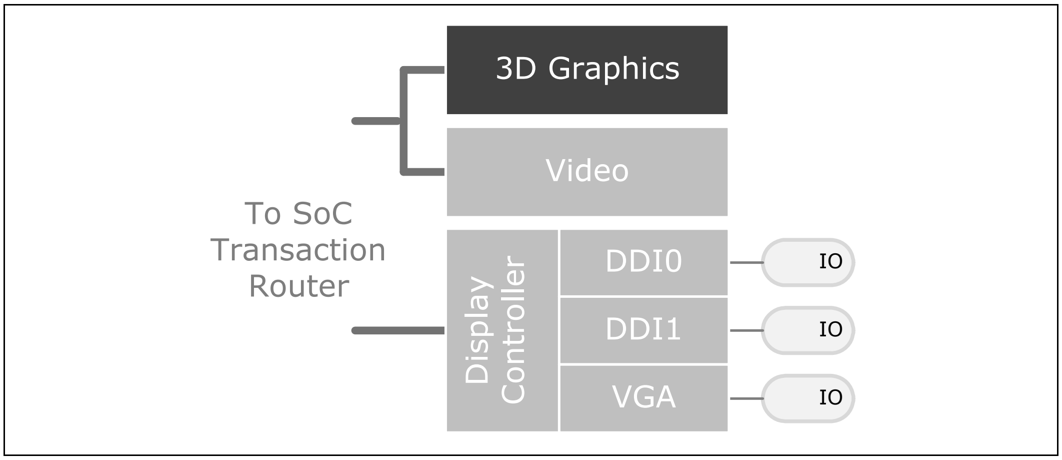
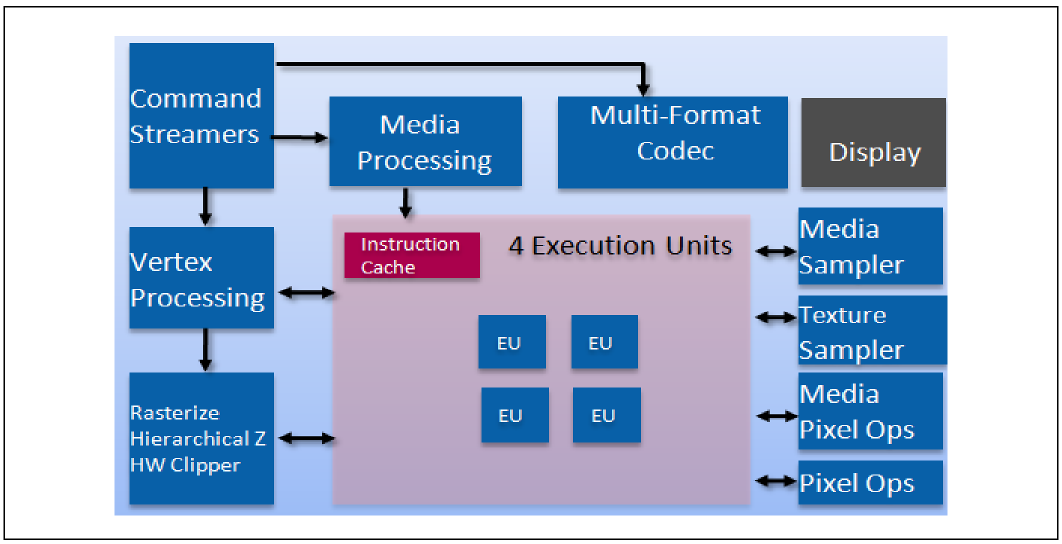


Figure 93. 3D Graphics Block Diagram



14.7 Features

The 3D graphics pipeline architecture simultaneously operates on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine. The Gen 7.0 3D engine provides the following performance and power-management enhancements:

- Hierarchal-Z
- Video quality enhancements

14.7.1 3D Engine Execution Units

- The EUs perform 128-bit wide execution per clock.
- Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing.

14.7.2 3D Pipeline

14.7.2.1 Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

14.7.2.2 Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.

14.7.2.3 Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

14.7.2.4 Clip Stage

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

14.7.2.5 Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

14.7.2.6 Windower/IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

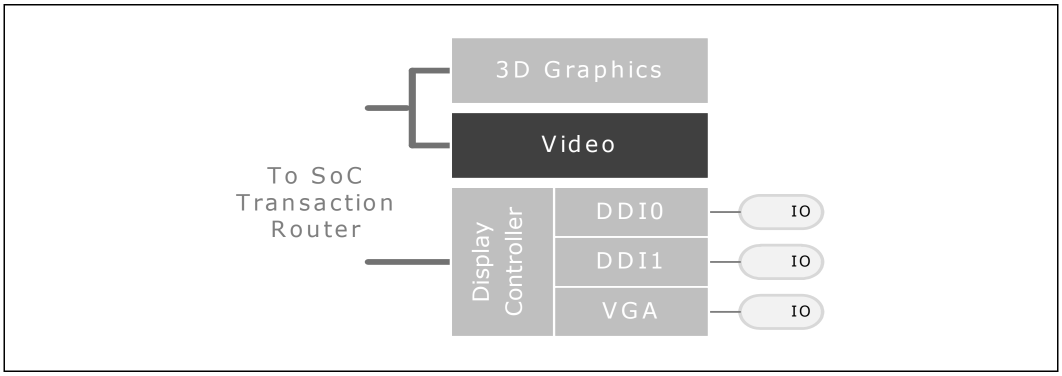
The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

14.7.3 Video Engine

The video engine is part of the Intel Processor Graphics for image processing, play-back and transcode of Video applications. Processor Graphics video engine has a dedicated fixed hardware pipe-line for high quality decode and encode of media content. This engine supports Full HW acceleration for decode of H.264, MPEG -2, MVC, VC-1, WMV9, JPEG/MJPEG contents along with encode of H.264 apart from various video processing features. The new Processor Graphics Video engine adds support for processing features such as frame rate conversion, image stabilization and gamut conversion.

14.8 VED (Video Encode/Decode)

Note: The video engine is part of the Intel Processor Graphics for image processing, play-back and transcode of Video applications. Processor Graphics video engine has a dedicated fixed hardware pipe-line for high quality decode and encode of media content. SoC Video Encode Decode block incorporates VXD 392 video decode core.



14.8.1 Features

The features for the Video decode hardware accelerator in SoC are:

- VED core can be configured on a time division multiplex basis to handle single, dual and multi-stream HD decoding.
- VED provides full hardware acceleration support

Table 170. Hardware Accelerated Video Decode Codec Support

Category	Codec Format
Media decode rate	Upto 1080p@60fps and 3x 4kx2k @30fps (H.264/JPEG/ MJPEG/MVC/MPEG-2 /WMV9/VC1)
Media encode rate	Upto 1080p@60fps and 1x 4kx2k @30fps (H.264)

14.9 PCI Configuration Registers

Table 171. Summary of Graphics, Video and Display PCI Configuration Registers—0/2/0

Offset	Size	Register ID—Description	Default Value
0h	4	"DID—Offset 0h" on page 426	0F318086h
4h	4	"PCICMD_STS—Offset 4h" on page 426	00100000h
8h	4	"RID_CC—Offset 8h" on page 427	03000000h
Ch	4	"HDR—Offset Ch" on page 428	00000000h
10h	4	"GTTMMADR_LSB—Offset 10h" on page 428	00000000h
14h	4	"GTTMMADR_MSB—Offset 14h" on page 429	00000000h
18h	4	"GMADR_LSB—Offset 18h" on page 430	00000008h
1Ch	4	"GMADR_MSB—Offset 1Ch" on page 431	00000000h
20h	4	"IOBAR—Offset 20h" on page 431	00000001h
2Ch	4	"SSID_SID—Offset 2Ch" on page 432	00000000h
34h	4	"CAPPOINT—Offset 34h" on page 432	000000D0h
3Ch	4	"INTRLINE—Offset 3Ch" on page 433	00000100h
50h	4	"GGC—Offset 50h" on page 434	00000028h
5Ch	4	"BDSM—Offset 5Ch" on page 435	00000000h
60h	4	"MSAC—Offset 60h" on page 436	00020000h
70h	4	"BGSM—Offset 70h" on page 437	00000000h
74h	4	"PAVPC—Offset 74h" on page 437	00000000h
90h	4	"MSI_CAPID_MC—Offset 90h" on page 439	0000B005h
94h	4	"MA—Offset 94h" on page 440	00000000h
98h	4	"MD—Offset 98h" on page 440	00000000h
A4h	4	"AFLC—Offset A4h" on page 441	03060013h
A8h	4	"AFCTLSTS—Offset A8h" on page 441	00000000h
B0h	4	"VCID—Offset B0h" on page 442	01070009h
B4h	4	"VCID—Offset B0h" on page 442	00000000h
C4h	4	"FD—Offset C4h" on page 443	00000000h
D0h	4	"PMCAPID—Offset D0h" on page 444	00229001h
D4h	4	"PMCS—Offset D4h" on page 445	00000000h
E0h	4	"SWSMISCI—Offset E0h" on page 445	00000000h
E4h	4	"ASLE—Offset E4h" on page 447	00000000h
F8h	4	"MANID—Offset F8h" on page 447	00000000h
FCh	4	"ASLS—Offset FCh" on page 448	00000000h

14.9.1 DID—Offset 0h

PCI Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits) **DID:** [B:0, D:2, F:0] + 0h

Power Well: Core

Default: 0F318086h

31	28	24	20	16	12	8	4	0
0 0 0 0	1 1 1 1	0 0 1 1	0 0 0 1	1 0 0 0	0 0 0 0	1 0 0 0	0 1 1 0	

31:16	15:0
DEVICEID_0	VENDORID_1

Bit Range	Default & Access	Description
31:16	0F31h RO	**DEVICEID (DEVICEID_0):** DID: Identifier assigned to the dev2 PCI
15:0	8086h RO	**VENDORID (VENDORID_1):** VID: PCI standard identification for Intel

14.9.2 PCICMD_STS—Offset 4h

PCI Command Register and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits) **PCICMD_STS:** [B:0, D:2, F:0] + 4h

Power Well: Core

Default: 00100000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

31:21	20	19	18:16	15:11	10	9:3	2	1	0
RSVD_6	CAPABILITY_LIST_7	INTERRUPT_STATUS_8	RSVD_9	RSVD_0	INTERRUPT_DISABLE_1	RSVD_2	BUS_MASTER_ENABLE_3	MEMORY_SPACE_ENABLE_4	IO_SPACE_ENABLE_5

Bit Range	Default & Access	Description
31:21	000h RO	**RSVD (RSVD_6):** Reserved

Bit Range	Default & Access	Description
20	1b RO	**CAPABILITY_LIST (CAPABILITY_LIST_7):** CAP: CAPPOINT register at 34h provides an offset
19	0b RO	**INTERRUPT_STATUS (INTERRUPT_STATUS_8):** IS: 1= Determined by IIR and IER memory interface register, 0=no interrupt pending
18:16	000b RO	**RSVD (RSVD_9):** Reserved
15:11	00h RO	**RSVD (RSVD_0):** Reserved
10	0b RW	**INTERRUPT_DISABLE (INTERRUPT_DISABLE_1):** ID: 0= Interrupt message enabled, 1= disabled
9:3	00h RO	**RSVD (RSVD_2):** Reserved
2	0b RW	**BUS_MASTER_ENABLE (BUS_MASTER_ENABLE_3):** BME: 0= Blocks the sending of MSI interrupts, 1= permits
1	0b RW	**MEMORY_SPACE_ENABLE (MEMORY_SPACE_ENABLE_4):** MSE: 0= Memory space disabled, 1= enabled
0	0b RW	**IO_SPACE_ENABLE (IO_SPACE_ENABLE_5):** IOSE: 0= I/O space is disabled, 1=enabled

14.9.3 RID_CC—Offset 8h

Revision Identification and Class code registerSOXi Context Save/Restore: Yes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RID_CC: [B:0, D:2, F:0] + 8h

Power Well: Core

Default: 03000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASE_CLASS_CODE_1								SUB_CLASS_CODE_2								PROGRAMMING_INTERFACE_3								REVISION_ID_0							

Bit Range	Default & Access	Description
31:24	00000011b RO	**BASE_CLASS_CODE (BASE_CLASS_CODE_1):** BCC: MGGC0[VAMEN]=0, 03h else 04h

Bit Range	Default & Access	Description
23:16	00000000b RO	**SUB_CLASS_CODE (SUB_CLASS_CODE_2):** MGGC0[VAMEN]= 1, 80h, MGGC0[VAMEN]=0,determined based on GGC register, GMS and IVD
15:8	00h RO	**PROGRAMMING_INTERFACE (PROGRAMMING_INTERFACE_3):** MGGC0[VAMEN]= 0, 00h display controller, =1, 00h NOP
7:0	00000000b RO	**REVISION_ID (REVISION_ID_0):** RID: value of strapRID[7:0] input pin to GVD

14.9.4 HDR—Offset Ch

Header Type

Access Method

Type: PCI Configuration Register (Size: 32 bits)

HDR: [B:0, D:2, F:0] + Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD_0 (31:24), MULTI_FUNCTION_STATUS_1 (23), HEADER_CODE_2 (22:16), RSVD_3 (15:0)

Bit Range	Default & Access	Description
31:24	00h RO	**RSVD (RSVD_0):** Reserved
23	0b RO	**MULTI_FUNCTION_STATUS (MULTI_FUNCTION_STATUS_1):** MFUNC: Integrated graphics is a single function
22:16	00h RO	**HEADER_CODE (HEADER_CODE_2):** HDR: Indicates a type 0 configuration space header format
15:0	0000h RO	**RSVD (RSVD_3):** Reserved

14.9.5 GTTMMADR_LSB—Offset 10h

Gfx Memory Mapped Address Range. This is the base address for all memory mapped registers and GTT table. SOXi Context Save/Restore : Yes This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 512K of that used by MMIO and 2MB used by GTT. GTTADR will begin at (GTTMMADR + 2 MB) while the MMIO base address will be the same as GTTMMADR. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The allocation is for 4MB and the base address is defined by bits [35:22].

Access Method

Type: PCI Configuration Register (Size: 32 bits) | **GTTMMADR_LSB:** [B:0, D:2, F:0] + 10h

Power Well: Core

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MBA_LSB_0										RSVD_1																		RSVD_2	MEMTYP_3		RSVD_4

Bit Range	Default & Access	Description
31:22	000h RW	**MBA_LSB (MBA_LSB_0):** Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).
21:4	00000h RO	**RSVD (RSVD_1):** RSVD: Hardwired to 0 to indicate at least 4MB address range.
3	0b RO	**RSVD (RSVD_2):** Prefetchable Memory (PREFMEM): Hardwired to 0to prevent prefetching.
2:1	00b RO	**MEMTYP (MEMTYP_3):** Memory Type (MEMTYP): 00 : To indicate 32 bit base address 01: Reserved 10 : To indicate 64 bit base address 11: Reserved
0	0b RO	**RSVD (RSVD_4):** Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.

14.9.6 GTTMMADR_MSB—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits) | **GTTMMADR_MSB:** [B:0, D:2, F:0] + 14h

Power Well: Core

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD_0																												MBA_MSB_1			

Bit Range	Default & Access	Description
31:4	00000000h RO	**RSVD (RSVD_0):** Reserved for Memory Base Address (RSVD): Must be set to 0 since addressing above 64GB is not supported.
3:0	0h RO	**MBA_MSB (MBA_MSB_1):** Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).

14.9.7 GMADR_LSB—Offset 18h

Gfx Aperture location. SOXi Context Save/Restore : Yes GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining. Accesses to this range will be translated to DRAM Physical memory addresses. Fence registers may be used to sub-divide this range and allow tiled surfaces (determined by fence registers). The following sizes are supported : 128MB, 256MB, 512MB. (Determined by the MSAC register)

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GMADR_LSB: [B:0, D:2, F:0] + 18h

Power Well: Core

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
RSVD_0			ADMSK512_1	ADMSK256_2	RSVD_3																							PREFMEM_4	MEMTYP_5		RSVD_6

Bit Range	Default & Access	Description
31:29	000b RO	**RSVD (RSVD_0):** Memory Base Address (MBA): Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:29].
28	0b RW/L	**ADMSK512 (ADMSK512_1):** 512MB Address Mask (ADMSK512): This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[2:1]. See MSAC (Dev2, Func 0, offset 62h) for details.
27	0b RW/L	**ADMSK256 (ADMSK256_2):** 256MB Address Mask (ADMSK256): This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[2:1]. See MSAC (Dev 2, Func 0, offset 62h) for details.
26:4	0000000h RO	**RSVD (RSVD_3):** Address Mask (ADM): Hardwired to 0s to indicate at least 128MB address range.
3	1b RO	**PREFMEM (PREFMEM_4):** Prefetchable Memory (PREFMEM): Hardwired to 1 to enable prefetching.
2:1	00b RO	**MEMTYP (MEMTYP_5):** Memory Type (MEMTYP): 00 : To indicate 32 bit base address 01: Reserved 10 : To indicate 64 bit base address 11: Reserved
0	0b RO	**RSVD (RSVD_6):** Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.

14.9.8 GMADR_MSB—Offset 1Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GMADR_MSB: [B:0, D:2, F:0] + 1Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD_0 (bits 31:4), MBA_1 (bits 3:0)

Bit Range	Default & Access	Description
31:4	0000000h RO	**RSVD (RSVD_0):** Memory Base Address (MBA2): Set by the OS, these bits correspond to address signals [63:36].
3:0	0h RO	**MBA (MBA_1):** Memory Base Address (MBA)Set by the OS, these bits correspond to address signals [35:32]

14.9.9 IOBAR—Offset 20h

I/O Base Address. This is used only by SBIOS. This register is the base address for the MMIO_INDEX and MMIO_DATA registers SOXi Context Save/Restore : Yes NOTE : This was at 14h for CDV. This register provides the Base offset of the I/O registers within Device #2. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed : 1)in PM states D1-D3 or 2)if IO Enable is clear or 3)if Device #2 is turned off or 4)if Internal graphics is disabled thru the fuse or fuse override mechanisms. Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then the GMCH claims all 8, 16 or 32 bit IO cycles from the CPU that falls within the 8B claimed.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IOBAR: [B:0, D:2, F:0] + 20h

Power Well: Core

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: RSVD_0 (bits 31:16), BASE_ADDRESS_1 (bits 15:3), RSVD_2 (bits 2:1), RESOURCE_TYPE_RTE_3 (bit 0)

Bit Range	Default & Access	Description
31:16	0000h RO	**RSVD (RSVD_0):** Reserved
15:3	0000h RW	**BASE_ADDRESS (BASE_ADDRESS_1):** BA: Set by the OS, these bits correspond to address signals [15:6].IOBAR is to be used for both GTLC register programming and GTT table programming. This is an indirect access method.
2:1	00b RO	**RSVD (RSVD_2):** Reserved
0	1b RO	**RESOURCE_TYPE_RTE (RESOURCE_TYPE_RTE_3):** Indicates a request for I/O space

14.9.10 SSID_SID—Offset 2Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SSID_SID: [B:0, D:2, F:0] + 2Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBID_1																SUBVID_0															

Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBID (SUBID_1):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.
15:0	0000h RW/O	**SUBVID (SUBVID_0):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

14.9.11 CAPPOINT—Offset 34h

This register points to a linked list of capabilities implemented by this device.For VV, the capability linked list is expected to be : (Head-34, PMCAP-D0, MSI-90, VID-B0, ..End)Old : (Head-34, PMCAP-D0, MSI-90, AFLC-A4, VID-B0, .. End)

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPPOINT: [B:0, D:2, F:0] + 34h

Power Well: Core

Default: 000000D0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0
RSVD_0																								CAPABILITIES_POINTER_1							

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD (RSVD_0):** Reserved
7:0	D0h RW/O	**CAPABILITIES_POINTER (CAPABILITIES_POINTER_1):** The first item in the capabilities list is at address D0h (PMCS). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

14.9.12 INTRLINE—Offset 3Ch

3C - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/ display driver. This 8-bit register is used to communicate interrupt line routing information. It is read/write and must be implemented by the device. POST software will write the routing information into this register as it initializes and configures the system. SOXi Context Save/Restore : Yes The value in this register tells which input of the system interrupt controller(s) the device?s interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information. 3D - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver SOXi Context Save/Restore : Not required

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTRLINE: [B:0, D:2, F:0] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
RSVD0																INTERRUPT_PIN_1								INTRLINE_0							

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
15:8	01h RO	**INTERRUPT_PIN (INTERRUPT_PIN_1):** IPIN: Value indicates which interrupt pin this device uses. This field is hard coded to 1h since Valleyview Device 2 is a single function device. The PCI spec requires that it use INTA#.01h: INTA
7:0	00h RW	**INTRLINE (INTRLINE_0):** ILIN: BIOS written value to communicate interrupt line routing information to the device driverUsed to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device?s interrupt pin is connected.

14.9.13 GGC—Offset 50h

GMCH Graphics Control Register. SOXi Context Save/Restore : Yes Note : CDV supported 64MB maximum. CDV had no GGMS field. Note : CDV had more granularity on the encodings for graphics mode select and only 3 bits.

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

GGC: [B:0, D:2, F:0] + 50h

Default: 00000028h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
RSVD0																RSVD_0	VAMEN_1	RSVD_2				GGMS_3		GMS_4					RSVD_5	VGA_DISABLE_6	GGCLCK_7

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15	0b RO	**RSVD (RSVD_0):** Reserved
14	0b RW/L	**VAMEN (VAMEN_1):** Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
13:10	0h RO	**RSVD (RSVD_2):** Reserved
9:8	00b RW/L	**GGMS (GGMS_3):** GTT Graphics Memory Size (GGMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will drive the base of GSM from DSM only using the GSM size programmed in the register. 0h: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed. 1h: 1 MB of memory pre-allocated for GTT. 2h: 2 MB of memory pre-allocated for GTT. 3h: Reserved. All unspecified encodings of this register field are reserved, hardware functionality is not guaranteed if used.

Bit Range	Default & Access	Description
7:3	00101b RW/L	**GMS (GMS_4):** Graphics Mode Select (GMS). This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. 0h = 0MB 10h = 512MB 1h = 32MB 2h = 64MB 3h = 96MB 4h = 128MB 5h = 160MB 6h = 192MB 7h = 224MB 8h = 256MB 9h = 288MB Ah = 320MB Bh = 352MB Ch = 384MB Dh = 416MB Eh = 448MB Fh = 480MB Other = Reserved When GMS != 000 (and VD=0): Address[31:0] is compared with VGA memory range. (The VGA memory range is A_0000h to B_FFFFh.). If there is a match and MSE = 1 and MEMRD or MEMWR, the access will route as a Rmdwvgamemen_cr cycle on the RMbus. If the RMbus returns a hit the GVD will select the command. As well, when 0 the GVD will check if scldown3_address[15:0] is one of the VGA IO register range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) If there is a match and IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will intiate a (VGA) register cycle on the RMbus. If the RMbus returns a hit the GVD will select the command When GMS == 000 : No address compare will occur against VGA memory range or the VGA IO register range. Also, CC[15:8] is changed to 8?h80 from 8'h00
2	0b RO	**RSVD (RSVD_5):** Reserved
1	0b RW/L	**VGA_DISABLE (VGA_DISABLE_6):** VGA Disable (VD): 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).
0	0b RW/L	**GGCLCK (GGCLCK_7):** When set to 1b, this bit will lock all bits in this register.

14.9.14 BDSM—Offset 5Ch

This register contains the base address of Graphics Data Stolen DRAM memory. Note : IVB located this register in device 0, 0xB0. Mirrored into device 2, 0x5C.Graphics Stolen Memory is within DRAM space. The base of stolen memory will always be below 4G.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BDSM: [B:0, D:2, F:0] + 5Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BDSM_0												RSVD_1																			BDSM_LOCK_2

Bit Range	Default & Access	Description
31:20	000h RW/L	**BDSM (BDSM_0):** BDSM: BASE_OF_Data_STOLEN_MEMORY. This register contains bits 31 to 20 of the base address of Data stolen DRAM memory. For certain GTLC generated accesses, this base register will be added to the GTLC provided offset address, forming the full physical address for the PFI fabric. This is also used as a base for VGA paged accesses. The display engine also uses the register. Signal : gvd_dsp_cfg_BSM_zcznfwh[31:20].
19:1	00000h RO	**RSVD (RSVD_1):** Reserved
0	0b RW/L	**BDSM_LOCK (BDSM_LOCK_2):** This bit will lock all writeable settings in this register, including itself.

14.9.15 MSAC—Offset 60h

This register determines the size of the graphics memory aperture. Only the system BIOS will write this register based on pre- boot address allocation efforts. Graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume. SOXi Context Save/Restore : Yes. The size of the aperture must not be modified by software after its location is written into GMADR (offset 18h).

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSAC: [B:0, D:2, F:0] + 60h

Power Well: Core

Default: 00020000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD_0	LHSAS_1	RSVD_2

Bit Range	Default & Access	Description
31:19	0000h RO	**RSVD (RSVD_0):** Reserved
18:17	01b RW	**LHSAS (LHSAS_1):** Untrusted Aperture Size (LHSAS): 00 : bits [28:27] of GMADR register are made R/W allowing 128MB of GMADR. 01 : bit [28] of GMADR is made R/W and bit [27] of GMADR is forced to zero allowing 256MB of GMADR. 10 : Illegal programming. 11: bits [28:27] of GMADR register are made Read only and forced to zero, allowing only 512MB of GMADR.
16:0	00000h RO	**RSVD (RSVD_2):** Reserved

14.9.16 BGSM—Offset 70h

Base of GTT table in Gfx Stolen Memory SOXi Context Save/Restore : Yes. Note : IVB located this register in device 0, 0xB4. Mirrored into Device 2. The GTT table is located within Graphics Stolen Memory in DRAM space. The base of stolen memory will always be below 4G.

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**BGSM:** [B:0, D:2, F:0] + 70h
Power Well: Core	

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BGSM_0												RSVD_1																			BGSM_LOCK_2

Bit Range	Default & Access	Description
31:20	000h RW/L	**BGSM (BGSM_0):** BGSM: Gfx Base of GTT Stolen Memory. This register contains bits 31 to 20 of the base address of GTT Table in stolen DRAM memory. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 2 offset 50 bits 9:8) from the Graphics Base of Data Stolen Memory (PCI Device 2 offset 5C bits 31:20). Signal : gvd_dsp_Cspgtbladdr_dczfwohdczfwoh[31:20].Note : was 4KB aligned on CDV ie. [31:12]
19:1	00000h RO	**RSVD (RSVD_1):** Reserved
0	0b RW/L	**BGSM_LOCK (BGSM_LOCK_2):** This bit will lock all writeable settings in this register including itself

14.9.17 PAVPC—Offset 74h

Protected Audio Video Control. Similar to IVB, BIOS will program this register for Valleyview (not the Gfx Driver). SOXi Context Save/Restore : Yes. For Valleyview, device 2 configuration accesses to 0x74 and Gfx MMIO accesses to 0x1082C0 will both alias to the same register. This register will be located within Gunit.WOPCMBASE is derived from : BDSMbase + GMS size - WOPCMSZ. Note : IVB currently derives from : TOLUD + WOPCMSZ

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**PAVPC:** [B:0, D:2, F:0] + 74h
Power Well: Core	

Default: 00000000h

31:20	19:18	17:6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0
RSVD_0	RSVD_1	RSVD_2	WOPCMSZ_3	OVTATTACK_4	HVYMODSEL_5	PAVPLOCK_6	PAVPE_7	PCME_8

Bit Range	Default & Access	Description
31:20	000h RO	**RSVD (RSVD_0):** Reserved. This field is used to set the base of Protected Content Memory. This corresponds to bits 31:20 of the system memory address range, giving a 1MB granularity. This value MUST be at least 1MB above the base and below the top of stolen memory. This register is locked (becomes read-only) when PAVPLOCK = 1b.
19:18	00b RO	**RSVD (RSVD_1):** Reserved. Note : IVB provided 256KB granularity, so these 2 bits were RW to support that size option. However, VV will only support 1MB so Gunit will tie bits 19:18 to '00'.
17:6	000h RO	**RSVD (RSVD_2):** Reserved
5	0b RO	**WOPCMSZ (WOPCMSZ_3):** 0b ? 1MB Note : IVB had this as a RW bit with value '1' indicating size 256KB support. Since VV only supports 1MB size, this register is RO for VV. These are the only sizes supported for IVB. The IVB is going to run PAVP3 Mode Serpent applications using per-App selection. Therefore, the size chosen should always be 1MB configuration even if Lite mode is chosen using PAVPC register (bit_3 = 0) for PAVP2 Mode Applications. This is because CB^2 code needs to be always loaded, since an App. Which opts for per-App Serpent mode will also execute the CB^2 code). The driver may consider it a BIOS programming error, if PAVPC Serpent Mode is selected with only 256KB of WOPCM size. However PAVPC Lite Mode with 1M WOPCM size is acceptable and not an error, as this may involve per-App selected Serpent Mode.
4	0b RW/L	**OVTATTACK (OVTATTACK_4):** Override of Unsolicited Connection State Attack and Terminate. 0b Disable Override. Attack Terminate allowed. 1b Enable Override. Attack Terminate disallowed. This register bit is locked (becomes read-only) when PAVPLOCK = 1b
3	0b RW/L	**HVYMODSEL (HVYMODSEL_5):** In IVB, this bit is a care only for PAVP2 mode of operation (and a chicken bit is also set). For IVB PAVP2 mode: 0 : Lite Mode (Non-Serpent Mode) 1: Serpent Mode For PAVP3 mode of operation, this bit_3 is a care, only if the per-App Memory Config is disabled due to the clearing of an additional Chicken bit_9 in IVB Crypto Function Control_1 Reg (@ address 0x320F0h). For chicken bit enabled IVB PAVP3 mode, this one type boot time programming has been replaced by per-Media App. Programming (through the Media Crypto Copy command). Note that IVB PAVP2 or PAVP3 Mode selection is done by programming bit_8 of MFX_MODE ? Video Mode Register. (Note again, that when in PAVP3 Mode, the per-App Memory Config. (Serpent/Lite) feature for enabling, requires the further setting of a global one time chicken bit to be set (bit_9 = ?1/mask_bit_25 = ?1) in the IVB Crypto Function Control_1 Register @ address 0x320F0h). Note : Valleyview does not support PAVP2 mode. Only PAVP3 mode is supported (a superset of PAVP2).
2	0b RW/L	**PAVPLOCK (PAVPLOCK_6):** This bit will lock all writeable contents in this register when set(including itself).Only a hw reset can unlock the register again. This Lock bit if PAVP is enabled (PAVPE = 1)
1	0b RW/L	**PAVPE (PAVPE_7):** 0: PAVP functionality is disabled. 1: enabled. This register is locked when PAVPLOCK=1
0	0b RW/L	**PCME (PCME_8):** PCME = Protected Content Memory Enable This field enables Protected Content Memory within Graphics Stolen Memory. This memory is the same as the WOPCM area. The size of the WOPCM area is defined by bit_5 of this register. WOPCM is the only remaining flavor of range protected memory. 0: WOPCM protection disabled. 1 : WOPCM protection enabled. This bit must be programmed to 1 when PAVP is enabled. With per-App Memory configuration support in IVB, the range check for the WOPCM memory area should always happen when this bit is set, irrespective of Lite or AES mode programming, or PAVP2 or PAVP3 Mode programming.

14.9.18 MSI_CAPID_MC—Offset 90h

Message Signaled Interrupts Capability ID.SOXi Context Save/Restore : Yes. Message Signaled Control Register. SOXi Context Save/Restore : Yes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSI_CAPID_MC: [B:0, D:2, F:0] + 90h

Power Well: Core

Default: 0000B005h

31 28 24	23	22 20	19 17	16	15 12 8	7 4 0
0 0 0 0 0 0 0 0	0	0 0 0	0 0 0	0	1 0 1 1 0 0 0 0	0 0 0 0 0 1 0 1
RSVD_2	ADDRESS_64_BIT_CAPABLE_3	MULTIPLE_MESSAGE_ENABLE_4	MULTIPLE_MESSAGE_CAPABLE_5	MSI_ENABLE_6	POINTER_TO_NEXT_CAPABILITY_0	CAPABILITY_ID_1

Bit Range	Default & Access	Description
31:24	00h RO	**RSVD (RSVD_2):** Reserved
23	0b RO	**ADDRESS_64_BIT_CAPABLE (ADDRESS_64_BIT_CAPABLE_3):** C64: 32-bit capable only
22:20	000b RW	**MULTIPLE_MESSAGE_ENABLE (MULTIPLE_MESSAGE_ENABLE_4):** MME: This field is RW for software compatibility, but only a single message is ever generated. System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
19:17	000b RO	**MULTIPLE_MESSAGE_CAPABLE (MULTIPLE_MESSAGE_CAPABLE_5):** MMC: This device is only single message capable System Software reads this field to determine the number of messages being requested by this device. Value: Number of requests 000: 1. 001- 111: Reserved
16	0b RW	**MSI_ENABLE (MSI_ENABLE_6):** MSIE: If set, MSI is enabled and traditional interrupts are not used to generate interrupts. PCICMDSTS.BME must be set for an MSI to be generated. 0 : MSI interrupts are disabled. 1 : MSI interrupts are enabled. Permits sending an MSI interrupt.
15:8	B0h RW/O	**POINTER_TO_NEXT_CAPABILITY (POINTER_TO_NEXT_CAPABILITY_0):** Points to the next item in the list (B0=VCID support). This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.
7:0	05h RO	**CAPABILITY_ID (CAPABILITY_ID_1):** CAPID: Indicates an MSI capability

14.9.19 MA—Offset 94h

Message Address.SOXi Context Save/Restore : Yes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MA: [B:0, D:2, F:0] + 94h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADDRESS_0																														RSVD_1	

Bit Range	Default & Access	Description
31:2	00000000h RW	**ADDRESS (ADDRESS_0):** MA: Lower 32-bits of the system specified message address, always DW aligned. When the GVD issues an MSI interrupt as a MEMWR on the SCL, the memory address corresponds to the value of this field
1:0	00b RO	**RSVD (RSVD_1):** Reserved

14.9.20 MD—Offset 98h

Message Data.SOXi Context Save/Restore : Yes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MD: [B:0, D:2, F:0] + 98h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD_0																DATA_1															

Bit Range	Default & Access	Description
31:16	0000h RO	**RSVD (RSVD_0):** Reserved
15:0	0000h RW	**DATA (DATA_1):** MD: This 16-bit field is programmed by system software. This is forms the lower word of data for the MSI write transaction.

14.9.21 AFLC—Offset A4h

FLR capability advertisement.SOXi Context Save/Restore : Yes

Access Method

Type: PCI Configuration Register (Size: 32 bits) **AFLC:** [B:0, D:2, F:0] + A4h

Power Well: Core

Default: 03060013h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1

Bits	Field
31:26	RSVD_2
25	FLR_CAP_3
24	TP_CAP_4
23:16	LENGTH_5
15:8	NXT_PTR_0
7:0	CAP_ID_1

Bit Range	Default & Access	Description
31:26	00h RO	**RSVD (RSVD_2):** Reserved
25	1b RO	**FLR_CAP (FLR_CAP_3):** Function Level Reset Capability (FLR_CAP): 0: Function Level Reset is not supported 1: Function Level Reset is supported
24	1b RO	**TP_CAP (TP_CAP_4):** Transactions Pending Capability (TP_CAP): 0: Transactions Pending bit is not supported 1: Transactions Pending bit is supported
23:16	06h RO	**LENGTH (LENGTH_5):** Advanced Features Structure Length (LENGTH): The Advanced Features Capability structure is 6 bytes long.
15:8	00h RW/O	**NXT_PTR (NXT_PTR_0):** Next Pointer (NXT_PTR): Removed FLR capability per HSD 259253. Nulled the next pointer. Points to the next item in the list (B0=Vendor Capabilities ID)This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once so capabilities list can be changed if needed.
7:0	13h RO	**CAP_ID (CAP_ID_1):** Capability Identifier (CAP_ID): A value of 13h identifies that this PCI Function is capable of Advanced Features.

14.9.22 AFCTLSTS—Offset A8h

FLR control. Advanced Feature Status.SOXi Context Save/Restore : Not required

Access Method

Type: PCI Configuration Register (Size: 32 bits) **AFCTLSTS:** [B:0, D:2, F:0] + A8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:16	RSVD0
15:9	RSVD_2
8	TP_3
7:1	RSVD_0
0	INIT_FLR_1

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:9	00h RO	**RSVD (RSVD_2):** Reserved (RSVD):
8	0b RO	**TP (TP_3):** Transaction Pending (TP): 1: The Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. 0: All non-posted transactions have been completed.
7:1	00h RO	**RSVD (RSVD_0):** Reserved (RSVD):
0	0b RW/1S	**INIT_FLR (INIT_FLR_1):** Initiate Function Level Reset (INIT_FLR): A write of 1b initiates Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. Once written 1, FLR will be initiated. During FLR, a read will return 1?s since device 2 reads abort. Once FLR completes, hardware will clear the bit to 0.

14.9.23 VCID—Offset B0h

Vendor Capability ID.SOXi Context Save/Restore : Yes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VCID: [B:0, D:2, F:0] + B0h

Power Well: Core

Default: 01070009h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
VERSION_0								LENGTH_1								NEXT_CAPABILITY_POINTER_2								CAPABILITY_ID_CID_3							

Bit Range	Default & Access	Description
31:24	01h RO	**VERSION (VERSION_0):** VS: Identifies this as the first revision of the CAPID register definition
23:16	07h RO	**LENGTH (LENGTH_1):** LEN: this field has the value of 07h to indicate structure length (8 bytes)
15:8	00h RW/O	**NEXT_CAPABILITY_POINTER (NEXT_CAPABILITY_POINTER_2):** 00 indicates capability list ends here. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.Write-once allowing the capability list to be changed.

Bit Range	Default & Access	Description
7:0	09h RO	**CAPABILITY_ID_CID (CAPABILITY_ID_CID_3):** Identifies this as a vendor dependent capability pointers

14.9.24 VC—Offset B4h

Vendor Capabilities. Any SKU related fuses would be added here.SOXi Context Save/Restore : Not required

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VC: [B:0, D:2, F:0] + B4h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD_0 (bits 31:1), RSVD_1 (bit 0)

Bit Range	Default & Access	Description
31:1	0000000h RO	**Reserved (RSVD_0):** Reserved
0	0b RO	**Reserved (RSVD_1):** Placeholder for sku related fusing. VLV has no need for this

14.9.25 FD—Offset C4h

Functional Disable. used by SBIOS, not by driver.SOXi Context Save/Restore : Yes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

FD: [B:0, D:2, F:0] + C4h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD_0 (bits 31:1), FUNCTION_DISABLE_1 (bit 0)

Bit Range	Default & Access	Description
31:1	00000000h RO	**RSVD (RSVD_0):** Reserved
0	0b RW	**FUNCTION_DISABLE (FUNCTION_DISABLE_1):** FD: 0 : Default - normal operation. 1 : When set, the function is disabled (configuration space is disabled). All new requests on the IOSF Primary bus, including any new configuration cycle requests are not claimed on IOSF Primary. This bit as no effect register accessibility via IOSF SB. Once programmed to '1', the only way to re-enable device 2 is via an IOSF SB write of '0' to this register.

14.9.26 PMCAPID—Offset D0h

Power Management Capabilities ID and PM capabilities.SOXi Context Save/Restore : Yes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCAPID: [B:0, D:2, F:0] + D0h

Power Well: Core

Default: 00229001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

PME_SUPPORT_2 | D2_SUPPORT_3 | D1_SUPPORT_4 | RSVD_5 | DEVICE_SPECIFIC_INITIALIZATION_6 | RSVD_7 | VERSION_8 | NEXT_POINTER_0 | CAPABILITIES_ID_1

Bit Range	Default & Access	Description
31:27	00h RO	**PME_SUPPORT (PME_SUPPORT_2):** PMES The graphics controller does not generate PME
26	0b RO	**D2_SUPPORT (D2_SUPPORT_3):** D2S: D2 not supported
25	0b RO	**D1_SUPPORT (D1_SUPPORT_4):** D1S: D1 not supported
24:22	000b RO	**RSVD (RSVD_5):** Reserved
21	1b RO	**DEVICE_SPECIFIC_INITIALIZATION (DEVICE_SPECIFIC_INITIALIZATION_6):** Hardwired to 1
20:19	00b RO	**RSVD (RSVD_7):** Reserved

Bit Range	Default & Access	Description
18:16	010b RO	**VERSION (VERSION_8):** Verion compliance with revision 1.1 of PCI PM spec
15:8	90h RW/O	**NEXT_POINTER (NEXT_POINTER_0):** Indicates the next item in the capabilities list.This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset. Write once allowing changing of the capabilities list.
7:0	01h RO	**CAPABILITIES_ID (CAPABILITIES_ID_1):** CAPID: SIG defines this ID is 01h for PM

14.9.27 PMCS—Offset D4h

Power Management Control/Status. Driver doesn't use this register. SBIOS doesn't use this register SOXi Context Save/Restore : Yes.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCS: [B:0, D:2, F:0] + D4h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD_0 (bits 31:2) | POWER_STATE_PS_1 (bits 1:0)

Bit Range	Default & Access	Description
31:2	00000000h RO	**RSVD (RSVD_0):** Reserved
1:0	00b RW	**POWER_STATE_PS (POWER_STATE_PS_1):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec. Bits[1:0] Power state 00: D0 Default 01: D1 Not Supported 10: D2 Not Supported 11: D3 Signal : gvd_dsp_power_state_d3_znczfwoh output to 2D.

14.9.28 SWSMISCI—Offset E0h

Software SMI or SCI.To generate a SW SMI event, software should program bit 15:0 and trigger SMI. Note : ILK/SNB/IVB had SCI and SMI separated (E0 and E8) As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, this must be reserved for this register. The SCI mechanism for driver / BIOS communication. SMI is a system wide lock interrupt (halts the all the cores) as opposed to SCI. Vista and Win7 recommend to use the SCI. The SMI is slowly being phased out. This register serves 2 purposes: 1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) Event trigger (bit 0). To generate a SW SCI event, software (System BIOS/Graphics driver) should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a ?0? to ?1? subsequent transition in bit 0 of this register (caused by a software write operation), GMCH sends a single SCI message. The SCI will set the DMISCI bit in its TCO1_STS register and TCOSCI_STS bit in its GPE0 register upon receiving this message from DMI. Once written as 1, software must write a ?0? to this bit to clear it, and all other write transitions (1-)0, 0-)0, 1-)1) or if bit 15 is ?0? will not cause GMCH to send SCI message to DMI link. To generate a SW SMI event, software should program bit 15 to 0 and trigger an SMI.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SWSMISCI: [B:0, D:2, F:0] + E0h

Power Well: Core

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD_0

SMI_OR_SCI_EVENT_SELECT_1

SOFTWARE_SCRATCH_BITS_2

SMI_OR_SCI_EVENT_3

Bit Range	Default & Access	Description
31:16	0000h RO	**RSVD (RSVD_0):** Reserved
15	0b RW	**SMI_OR_SCI_EVENT_SELECT (SMI_OR_SCI_EVENT_SELECT_1):** MCS: SMI or SCI event select. 0 = SMI,1 = SCI
14:1	0000h RW	**SOFTWARE_SCRATCH_BITS (SOFTWARE_SCRATCH_BITS_2):** Used by driver to communicate information to SBIOS
0	0b RW	**SMI_OR_SCI_EVENT (SMI_OR_SCI_EVENT_3):** MCE:MCS=1, setting this bit causes an SCI. MCS=0, setting this bit causes an SMI. A 1 to 0, 0 to 0 or 1 to 1 transition of this bit does not trigger any events. The graphics driver writes to this register as a means to interrupt the SBIOS

14.9.29 ASLE—Offset E4h

System Display Event Register. SBIOS writes this reg to generate interrupt to graphics/display driver.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ASLE: [B:0, D:2, F:0] + E4h

Power Well: Core

Default: 00000000h

Bits	31:24	23:16	15:8	7:0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	ASLE_SCRATCH_TRIGGER_3_0	ASLE_SCRATCH_TRIGGER_2_1	ASLE_SCRATCH_TRIGGER_1_2	ASLE_SCRATCH_TRIGGER_0_3

Bit Range	Default & Access	Description
31:24	00h RW	**ASLE_SCRATCH_TRIGGER_3 (ASLE_SCRATCH_TRIGGER_3_0):** AST3: The writing of this by field (byte) ? even if just writing back the original contents ? will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
23:16	00h RW	**ASLE_SCRATCH_TRIGGER_2 (ASLE_SCRATCH_TRIGGER_2_1):** AST2: The writing of this by field (byte) ? even if just writing back the original contents ? will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
15:8	00h RW	**ASLE_SCRATCH_TRIGGER_1 (ASLE_SCRATCH_TRIGGER_1_2):** AST1: The writing of this by field (byte) ? even if just writing back the original contents ? will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common
7:0	00h RW	**ASLE_SCRATCH_TRIGGER_0 (ASLE_SCRATCH_TRIGGER_0_3):** AST0: The writing of this by field (byte) ? even if just writing back the original contents ? will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common

14.9.30 MANID—Offset F8h

Manufacturing ID. SOXi Context Save/Restore : Not required

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:2, F:0] + F8h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD_0 | STEPPING_ID_1 | MANUFACTURING_ID_2

Bit Range	Default & Access	Description
31:24	00h RO	**RSVD (RSVD_0):** Reserved
23:16	00000000b RO	**Stepping_ID (STEPPING_ID_1):** Hardwired to strapRID[7:0] via top level metal.23:16 - Manufacturing Stepping ID (00 = A0)
15:0	0000h RO	**MANUFACTURING_ID (MANUFACTURING_ID_2):** Hardwired to strapMANID[15:0] via top level metal. 15:8 - Foundry (0Fh = Intel, Others = Reserved) 7:3 - Fab process 12h : Fab code for P1263 13h : P1264 14h : P1265 15h : P1266 ... 1Ah : P1271 (VV POR) Others : Reserved 2:0 - Identifies the dot process 000 = Code for 0 001 = Code for .1 (VV POR) 010 = Code for .2 110 = Code for .4 011 = Code for .7

14.9.31 ASLS—Offset FCh

ASL Storage. The Valleyview display driver does not need this register since memory Operational Region (OpRegion) is available. This register is kept for use as scratch space. SOXi Context Save/Restore : Yes This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ASLS: [B:0, D:2, F:0] + FCh

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCRATCH_0

Bit Range	Default & Access	Description
31:0	00000000h RW	**SCRATCH (SCRATCH_0):** This register provides a means for the BIOS to communicate with the driver. This definition of this scratch register is worked out in common between System BIOS and driver software. Storage for up to 6 devices is possible. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

14.10 Memory Mapped Registers (1 of 2)

Table 172. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3B4–3B4h	1	"CRX (CRX_MDA)—Offset 3B4h" on page 456	00h
3B5–3B5h	1	"CR (CR_MDA)—Offset 3B5h" on page 457	00h
3C0–3C0h	1	"ARX—Offset 3C0h" on page 458	00h
3C1–3C1h	1	"ARX—Offset 3C0h" on page 458	00h
3C4–3C4h	1	"SRX—Offset 3C4h" on page 459	00h
3C5–3C5h	1	"SRX—Offset 3C4h" on page 459	00h
3C6–3C6h	1	"DACMASK—Offset 3C6h" on page 460	00h
3C8–3C8h	1	"DACWX—Offset 3C8h" on page 461	00h
3C9–3C9h	1	"DACDATA—Offset 3C9h" on page 461	00h
3CA–3CAh	1	"FCR (FCR_Read)—Offset 3CAh" on page 462	00h
3CC–3CCh	1	"MSR (MSR_READ)—Offset 3CCh" on page 463	00h
3CE–3CEh	1	"GRX—Offset 3CEh" on page 464	00h
3CF–3CFh	1	"GRX—Offset 3CEh" on page 464	00h
3D4–3D4h	1	"CRX (CRX_CGA)—Offset 3D4h" on page 466	00h
3D5–3D5h	1	"CR (CR_CGA)—Offset 3D5h" on page 466	00h
5010–5013h	4	"GPIOCTL_0—Offset 5010h" on page 467	00000808h
5014–5017h	4	"GPIOCTL_1—Offset 5014h" on page 469	00000808h
5018–501Bh	4	"GPIOCTL_2—Offset 5018h" on page 471	00000808h
501C–501Fh	4	"GPIOCTL_3—Offset 501Ch" on page 472	00000808h
5020–5023h	4	"GPIOCTL_4—Offset 5020h" on page 474	00000808h
5100–5103h	4	"GMBUS0—Offset 5100h" on page 476	00000000h
5104–5107h	4	"GMBUS1—Offset 5104h" on page 477	00000000h
5108–510Bh	4	"GMBUS2—Offset 5108h" on page 479	00000800h
510C–510Fh	4	"GMBUS3—Offset 510Ch" on page 481	00000000h
5110–5113h	4	"GMBUS4—Offset 5110h" on page 482	00000000h
5120–5123h	4	"GMBUS5—Offset 5120h" on page 483	00000000h
5130–5133h	4	"GMBUS6—Offset 5130h" on page 484	00000000h
5134–5137h	4	"GMBUS7—Offset 5134h" on page 484	00000000h
6014–6017h	4	"DPLLA_CTRL—Offset 6014h" on page 485	00002000h
6018–601Bh	4	"DPLLB_CTRL—Offset 6018h" on page 488	00006000h
601C–601Fh	4	"DPLLAMD—Offset 601Ch" on page 491	00000003h
6020–6023h	4	"DPLLBMD—Offset 6020h" on page 493	00000003h
6024–6027h	4	"RAWCLK_FREQ—Offset 6024h" on page 494	0000007Dh
6104–6107h	4	"D_STATE—Offset 6104h" on page 495	20D00400h
6200–6203h	4	"DSPCLK_GATE_D—Offset 6200h" on page 496	10000000h
6204–6207h	4	"DPPSR_CGDIS—Offset 6204h" on page 499	00000200h

Table 172. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6210–6213h	4	"RAMCLK_GATE_D—Offset 6210h" on page 502	00000000h
6500–6503h	4	"FW_BLC_SELF—Offset 6500h" on page 505	00000000h
6504–6507h	4	"MI_ARB—Offset 6504h" on page 506	00000000h
6508–650Bh	4	"CZCLK_CDCLK_FREQ_RATIO—Offset 6508h" on page 506	00000077h
650C–650Fh	4	"GCI_CONTROL—Offset 650Ch" on page 509	00004000h
6510–6513h	4	"GMBUSFREQ—Offset 6510h" on page 511	000000A0h
A000–A003h	4	"DPALETTE_A—Offset A000h" on page 512	00000000h
A800–A803h	4	"DPALETTE_B—Offset A800h" on page 512	00000000h
B000–B003h	4	"MIPIA_DEVICE_READY_REG—Offset B000h" on page 513	00000000h
B004–B007h	4	"MIPIA_INTR_STAT_REG—Offset B004h" on page 514	00000000h
B008–B00Bh	4	"MIPIA_INTR_EN_REG—Offset B008h" on page 516	00000000h
B00C–B00Fh	4	"MIPIA_DSI_FUNC_PRG__REG—Offset B00Ch" on page 518	00000001h
B010–B013h	4	"MIPIA_HS_TX_TIMEOUT_REG—Offset B010h" on page 519	00000000h
B014–B017h	4	"MIPIA_LP_RX_TIMEOUT_REG—Offset B014h" on page 520	00000000h
B018–B01Bh	4	"MIPIA_TURN_AROUND_TIMEOUT_REG—Offset B018h" on page 520	00000000h
B01C–B01Fh	4	"MIPIA_DEVICE_RESET_TIMER—Offset B01Ch" on page 521	00000000h
B020–B023h	4	"MIPIA_DPI_RESOLUTION_REG—Offset B020h" on page 522	00000000h
B024–B027h	4	"MIPIA_DBI_RESOLUTION_REG—Offset B024h" on page 522	00000000h
B028–B02Bh	4	"MIPIA_HORIZ_SYNC_PADDING_COUNT—Offset B028h" on page 523	00000000h
B02C–B02Fh	4	"MIPIA_HORIZ_BACK_PORCH_COUNT—Offset B02Ch" on page 524	00000000h
B030–B033h	4	"MIPIA_HORIZ_FRONT_PORCH_COUNT—Offset B030h" on page 524	00000000h
B034–B037h	4	"MIPIA_HORIZ_ACTIVE_AREA_COUNT—Offset B034h" on page 525	00000000h
B038–B03Bh	4	"MIPIA_VERT_SYNC_PADDING_COUNT—Offset B038h" on page 526	00000000h
B03C–B03Fh	4	"MIPIA_VERT_BACK_PORCH_COUNT—Offset B03Ch" on page 526	00000000h
B040–B043h	4	"MIPIA_VERT_FRONT_PORCH_COUNT—Offset B040h" on page 527	00000000h
B044–B047h	4	"MIPIA_HIGH_LOW_SWITCH_COUNT—Offset B044h" on page 528	00000000h
B048–B04Bh	4	"MIPIA_DPI_CTRL_REG—Offset B048h" on page 529	00000000h
B04C–B04Fh	4	"MIPIA_DPI_DATA_REGISTER—Offset B04Ch" on page 530	00000000h
B050–B053h	4	"MIPIA_INIT_COUNT_REGISTER—Offset B050h" on page 530	00000000h
B054–B057h	4	"MIPIA_MAX_RETURN_PKT_SIZE_REGISTER—Offset B054h" on page 531	00000000h
B058–B05Bh	4	"MIPIA_VIDEO_MODE_FORMAT_REGISTER—Offset B058h" on page 531	00000000h
B05C–B05Fh	4	"MIPIA_EOT_DISABLE_REGISTER—Offset B05Ch" on page 532	00000000h
B060–B063h	4	"MIPIA_LP_BYTECLK_REGISTER—Offset B060h" on page 534	00000000h
B064–B067h	4	"MIPIA_LP_GEN_DATA_REGISTER—Offset B064h" on page 535	00000000h
B068–B06Bh	4	"MIPIA_HS_GEN_DATA_REGISTER—Offset B068h" on page 535	00000000h
B06C–B06Fh	4	"MIPIA_LP_GEN_CTRL_REGISTER—Offset B06Ch" on page 536	00000000h
B070–B073h	4	"MIPIA_HS_GEN_CTRL_REGISTER—Offset B070h" on page 537	00000000h

Table 172. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B074–B077h	4	"MIPIA_GEN_FIFO_STAT_REGISTER—Offset B074h" on page 538	1E060606h
B078–B07Bh	4	"MIPIA_HS_LS_DBI_ENABLE_REG—Offset B078h" on page 539	00000000h
B07C–B07Fh	4	"MIPIA_RESERVED—Offset B07Ch" on page 539	00000000h
B080–B083h	4	"MIPIA_DPHY_PARAM_REG—Offset B080h" on page 540	0B061A04h
B084–B087h	4	"MIPIA_DBI_BW_CTRL_REG—Offset B084h" on page 541	00000000h
B088–B08Bh	4	"MIPIA_CLK_LANE_SWITCHING_TIME_CNT—Offset B088h" on page 541	00000000h
B08C–B08Fh	4	"MIPIA_STOP_STATE_STALL—Offset B08Ch" on page 542	00000000h
B090–B093h	4	"MIPIA_INTR_STAT_REG_1—Offset B090h" on page 543	00000000h
B094–B097h	4	"MIPIA_INTR_EN_REG_1—Offset B094h" on page 543	00000000h
B100–B103h	4	"MIPIA_DBI_TYPEC_CTRL—Offset B100h" on page 544	00000000h
B104–B107h	4	"MIPIA_CTRL—Offset B104h" on page 545	00000000h
B108–B10Bh	4	"MIPIA_DATA_ADD—Offset B108h" on page 546	00000000h
B10C–B10Fh	4	"MIPIA_DATA_LEN—Offset B10Ch" on page 547	00000000h
B110–B113h	4	"MIPIA_CMD_ADD—Offset B110h" on page 547	00000000h
B114–B117h	4	"MIPIA_CMD_LEN—Offset B114h" on page 548	00000000h
B118–B11Bh	4	"MIPIA_RD_DATA_RETURN0—Offset B118h" on page 549	00000000h
B11C–B11Fh	4	"MIPIA_RD_DATA_RETURN1—Offset B11Ch" on page 549	00000000h
B120–B123h	4	"MIPIA_RD_DATA_RETURN2—Offset B120h" on page 550	00000000h
B124–B127h	4	"MIPIA_RD_DATA_RETURN3—Offset B124h" on page 551	00000000h
B128–B12Bh	4	"MIPIA_RD_DATA_RETURN4—Offset B128h" on page 551	00000000h
B12C–B12Fh	4	"MIPIA_RD_DATA_RETURN5—Offset B12Ch" on page 552	00000000h
B130–B133h	4	"MIPIA_RD_DATA_RETURN6—Offset B130h" on page 552	00000000h
B134–B137h	4	"MIPIA_RD_DATA_RETURN7—Offset B134h" on page 553	00000000h
B138–B13Bh	4	"MIPIA_RD_DATA_VALID—Offset B138h" on page 554	00000000h
B800–B803h	4	"MIPIC_DEVICE_READY_REG—Offset B800h" on page 554	00000000h
B804–B807h	4	"MIPIC_INTR_STAT_REG—Offset B804h" on page 555	00000000h
B808–B80Bh	4	"MIPIC_INTR_EN_REG—Offset B808h" on page 557	00000000h
B80C–B80Fh	4	"MIPIC_DSI_FUNC_PRG__REG—Offset B80Ch" on page 559	00000001h
B810–B813h	4	"MIPIC_HS_TX_TIMEOUT_REG—Offset B810h" on page 560	00000000h
B814–B817h	4	"MIPIC_LP_RX_TIMEOUT_REG—Offset B814h" on page 561	00000000h
B818–B81Bh	4	"MIPIC_TURN_AROUND_TIMEOUT_REG—Offset B818h" on page 562	00000000h
B81C–B81Fh	4	"MIPIC_DEVICE_RESET_TIMER—Offset B81Ch" on page 562	00000000h
B820–B823h	4	"MIPIC_DPI_RESOLUTION_REG—Offset B820h" on page 563	00000000h
B824–B827h	4	"MIPIC_DBI_RESOLUTION_REG—Offset B824h" on page 564	00000000h
B828–B82Bh	4	"MIPIC_HORIZ_SYNC_PADDING_COUNT—Offset B828h" on page 564	00000000h
B82C–B82Fh	4	"MIPIC_HORIZ_BACK_PORCH_COUNT—Offset B82Ch" on page 565	00000000h
B830–B833h	4	"MIPIC_HORIZ_FRONT_PORCH_COUNT—Offset B830h" on page 566	00000000h
B834–B837h	4	"MIPIC_HORIZ_ACTIVE_AREA_COUNT—Offset B834h" on page 566	00000000h

Table 172. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B838–B83Bh	4	"MIPIC_VERT_SYNC_PADDING_COUNT—Offset B838h" on page 567	00000000h
B83C–B83Fh	4	"MIPIC_VERT_BACK_PORCH_COUNT—Offset B83Ch" on page 568	00000000h
B840–B843h	4	"MIPIC_VERT_FRONT_PORCH_COUNT—Offset B840h" on page 568	00000000h
B844–B847h	4	"MIPIC_HIGH_LOW_SWITCH_COUNT—Offset B844h" on page 569	00000000h
B848–B84Bh	4	"MIPIC_DPI_CTRL_REG—Offset B848h" on page 570	00000000h
B84C–B84Fh	4	"MIPIC_DPI_DATA_REGISTER—Offset B84Ch" on page 571	00000000h
B850–B853h	4	"MIPIC_INIT_COUNT_REGISTER—Offset B850h" on page 572	00000000h
B854–B857h	4	"MIPIC_MAX_RETURN_PKT_SIZE_REGISTER—Offset B854h" on page 572	00000000h
B858–B85Bh	4	"MIPIC_VIDEO_MODE_FORMAT_REGISTER—Offset B858h" on page 573	00000000h
B85C–B85Fh	4	"MIPIC_EOT_DISABLE_REGISTER—Offset B85Ch" on page 574	00000000h
B860–B863h	4	"MIPIC_LP_BYTECLK_REGISTER—Offset B860h" on page 576	00000000h
B864–B867h	4	"MIPIC_LP_GEN_DATA_REGISTER—Offset B864h" on page 577	00000000h
B868–B86Bh	4	"MIPIC_HS_GEN_DATA_REGISTER—Offset B868h" on page 577	00000000h
B86C–B86Fh	4	"MIPIC_LP_GEN_CTRL_REGISTER—Offset B86Ch" on page 578	00000000h
B870–B873h	4	"MIPIC_HS_GEN_CTRL_REGISTER—Offset B870h" on page 578	00000000h
B874–B877h	4	"MIPIC_GEN_FIFO_STAT_REGISTER—Offset B874h" on page 579	1E060606h
B878–B87Bh	4	"MIPIC_HS_LS_DBI_ENABLE_REG—Offset B878h" on page 581	00000000h
B87C–B87Fh	4	"MIPIC_RESERVED—Offset B87Ch" on page 581	00000000h
B880–B883h	4	"MIPIC_DPHY_PARAM_REG—Offset B880h" on page 582	0B061A04h
B884–B887h	4	"MIPIC_DBI_BW_CTRL_REG—Offset B884h" on page 583	00000000h
B888–B88Bh	4	"MIPIC_CLK_LANE_SWITCHING_TIME_CNT—Offset B888h" on page 583	00000000h
B88C–B88Fh	4	"MIPIC_STOP_STATE_STALL—Offset B88Ch" on page 584	00000000h
B890–B893h	4	"MIPIC_INTR_STAT_REG_1—Offset B890h" on page 585	00000000h
B894–B897h	4	"MIPIC_INTR_EN_REG_1—Offset B894h" on page 585	00000000h
B904–B907h	4	"MIPIC_CTRL—Offset B904h" on page 586	00000000h
B908–B90Bh	4	"MIPIC_DATA_ADD—Offset B908h" on page 587	00000000h
B90C–B90Fh	4	"MIPIC_DATA_LEN—Offset B90Ch" on page 587	00000000h
B910–B913h	4	"MIPIC_CMD_ADD—Offset B910h" on page 588	00000000h
B914–B917h	4	"MIPIC_CMD_LEN—Offset B914h" on page 589	00000000h
B918–B91Bh	4	"MIPIC_RD_DATA_RETURN0—Offset B918h" on page 589	00000000h
B91C–B91Fh	4	"MIPIC_RD_DATA_RETURN1—Offset B91Ch" on page 590	00000000h
B920–B923h	4	"MIPIC_RD_DATA_RETURN2—Offset B920h" on page 591	00000000h
B924–B927h	4	"MIPIC_RD_DATA_RETURN3—Offset B924h" on page 591	00000000h
B928–B92Bh	4	"MIPIC_RD_DATA_RETURN4—Offset B928h" on page 592	00000000h
B92C–B92Fh	4	"MIPIC_RD_DATA_RETURN5—Offset B92Ch" on page 592	00000000h
B930–B933h	4	"MIPIC_RD_DATA_RETURN6—Offset B930h" on page 593	00000000h
B934–B937h	4	"MIPIC_RD_DATA_RETURN7—Offset B934h" on page 594	00000000h

Table 172. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B938–B93Bh	4	"MIPIC_RD_DATA_VALID—Offset B938h" on page 594	00000000h
60000–60003h	4	"HTOTAL_A—Offset 60000h" on page 595	00000000h
60004–60007h	4	"HBLANK_A—Offset 60004h" on page 596	00000000h
60008–6000Bh	4	"HSYNC_A—Offset 60008h" on page 597	00000000h
6000C–6000Fh	4	"VTOTAL_A—Offset 6000Ch" on page 598	00000000h
60010–60013h	4	"VBLANK_A—Offset 60010h" on page 599	00000000h
60014–60017h	4	"VSYNC_A—Offset 60014h" on page 600	00000000h
6001C–6001Fh	4	"PIPESRCA—Offset 6001Ch" on page 601	00000000h
60020–60023h	4	"BCLRPAT_A—Offset 60020h" on page 602	00000000h
60028–6002Bh	4	"VSYNCSHIFT_A—Offset 60028h" on page 603	00000000h
60030–60033h	4	"TRANSADATAM1—Offset 60030h" on page 604	7E000000h
60034–60037h	4	"TRANSADATAN1—Offset 60034h" on page 604	00000000h
60038–6003Bh	4	"TRANSADATAM2—Offset 60038h" on page 605	7E000000h
6003C–6003Fh	4	"TRANSADATAN2—Offset 6003Ch" on page 606	00000000h
60040–60043h	4	"TRANSADPLINKM1—Offset 60040h" on page 606	00000000h
60044–60047h	4	"TRANSADPLINKN1—Offset 60044h" on page 607	00000000h
60048–6004Bh	4	"TRANSADPLINKM2—Offset 60048h" on page 608	00000000h
6004C–6004Fh	4	"TRANSADPLINKN2—Offset 6004Ch" on page 608	00000000h
60050–60053h	4	"CRCCTRLREDA—Offset 60050h" on page 609	00000000h
60054–60057h	4	"CRCCTRLGREENA—Offset 60054h" on page 610	00000000h
60058–6005Bh	4	"CRCCTRLBLUEA—Offset 60058h" on page 610	00000000h
6005C–6005Fh	4	"CRCCTRLALPHAA—Offset 6005Ch" on page 611	00000000h
60060–60063h	4	"CRCRESREDA—Offset 60060h" on page 612	00000000h
60064–60067h	4	"CRCRESGREENA—Offset 60064h" on page 612	00000000h
60068–6006Bh	4	"CRCRESBLUEA—Offset 60068h" on page 613	00000000h
6006C–6006Fh	4	"CRCRESALPHAA—Offset 6006Ch" on page 614	00000000h
60070–60073h	4	"CRCCTRLRESIDUE2A—Offset 60070h" on page 615	00000000h
60080–60083h	4	"CRCRESRESIDUE2A—Offset 60080h" on page 615	00000000h
60090–60093h	4	"PSRCTLA—Offset 60090h" on page 616	00000000h
60094–60097h	4	"PSRSTATA—Offset 60094h" on page 618	00000000h
60098–6009Bh	4	"PSRCRC1A—Offset 60098h" on page 619	00000000h
6009C–6009Fh	4	"PSRCRC2A—Offset 6009Ch" on page 620	00000000h
600A0–600A3h	4	"VSCSDPA—Offset 600A0h" on page 621	00000000h
600B0–600B3h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 600B0h" on page 621	00000000h
600B4–600B7h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 600B4h" on page 622	00000000h
600B8–600BBh	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 600B8h" on page 623	00000000h

Table 172. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
600BC–600BFh	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 600BCh" on page 623	00000000h
600C0–600C3h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 600C0h" on page 624	00000000h
600C4–600C7h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 600C4h" on page 625	00000000h
60200–60203h	4	"VIDEO_DIP_CTL_A—Offset 60200h" on page 625	20200900h
60208–6020Bh	4	"VIDEO_DIP_DATA_A—Offset 60208h" on page 627	00000000h
60210–60213h	4	"VIDEO_DIP_GDCP_PAYLOAD_A—Offset 60210h" on page 628	00000000h
61000–61003h	4	"HTOTAL_B—Offset 61000h" on page 629	00000000h
61004–61007h	4	"HBLANK_B—Offset 61004h" on page 630	00000000h
61008–6100Bh	4	"HSYNC_B—Offset 61008h" on page 631	00000000h
6100C–6100Fh	4	"VTOTAL_B—Offset 6100Ch" on page 631	00000000h
61010–61013h	4	"VBLANK_B—Offset 61010h" on page 632	00000000h
61014–61017h	4	"VSYNC_B—Offset 61014h" on page 633	00000000h
6101C–6101Fh	4	"PIPEBSRC—Offset 6101Ch" on page 634	00000000h
61020–61023h	4	"BCLRPAT_B—Offset 61020h" on page 634	00000000h
61028–6102Bh	4	"VSYNCSHIFT_B—Offset 61028h" on page 635	00000000h
61030–61033h	4	"TRANSBDATAM1—Offset 61030h" on page 636	7E000000h
61034–61037h	4	"TRANSBDATAN1—Offset 61034h" on page 637	00000000h
61038–6103Bh	4	"TRANSBDATAM2—Offset 61038h" on page 638	7E000000h
6103C–6103Fh	4	"TRANSBDATAN2—Offset 6103Ch" on page 638	00000000h
61040–61043h	4	"TRANSBDPLINKM1—Offset 61040h" on page 639	00000000h
61044–61047h	4	"TRANSBDPLINKN1—Offset 61044h" on page 640	00000000h
61048–6104Bh	4	"TRANSBDPLINKM2—Offset 61048h" on page 640	00000000h
6104C–6104Fh	4	"TRANSBDPLINKN2—Offset 6104Ch" on page 641	00000000h

14.10.1 CRX (CRX_MDA)—Offset 3B4h

CRT Controller Index Register

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED	CRT_CONTROLLER_INDEX						

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**RESERVED:** Read as 0.
6:0	0b RW	**CRT_CONTROLLER_INDEX:** These 7 bits are used to select any one of the CRT controller registers to be accessed via the data port at I/O location 3B5h or 3D5h, depending upon whether the graphics system is configured for MDA or CGA emulation. The data port memory address offsets are 3B5h/3D5h.

14.10.2 CR (CR_MDA)—Offset 3B5h

CR index registers

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3B5h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CR_REGISTER_DESCRIPTIONS							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RW	**CR_REGISTER_DESCRIPTIONS:** CR indexed register descriptions

14.10.3 ARX—Offset 3C0h

Attribute Controller Index Register. Includes the 22 registers that share this offset (with different indexes). -enum ARX_e

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
ARX_REGISTER_DESCRIPTIONS							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RW	**ARX_REGISTER_DESCRIPTIONS:** ARX indexed register descriptions

14.10.4 AR—Offset 3C1h

AR index registers. Includes the 21 registers that share this offset (with differnet indexes.) -enum AR_e- in this document will lead to register definitions

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C1h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
AR_REGISTER_DESCRIPTIONS							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RW	**AR_REGISTER_DESCRIPTIONS:** AR indexed register descriptions

14.10.5 SRX—Offset 3C4h

Sequencer Index

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED					SEQUENCER_INDEX		

Bit Range	Default & Access	Field Name (ID): Description
7:3	0b RW	**RESERVED:** Read as 0s.
2:0	0b RW	**SEQUENCER_INDEX:** This field contains a 3-bit Sequencer Index value used to access sequencer data re gisters at indices 0 through 7. Notes: SR02 is referred to in the VGA standard as the Map Mask Register. However, the word map is used with multiple meanings in the VGA standard and was, therefore, deemed too confusing; hence, the reason for calling it the Plane Mask Register. SR07 is a standard VGA register that was not documented by IBM. It is not a graphics controller extension.

14.10.6 SR—Offset 3C5h

SR index registers

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C5h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
SR_REGISTER_DESCRIPTIONS							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RW	**SR_REGISTER_DESCRIPTIONS:** SR indexed register descriptions

14.10.7 DACMASK—Offset 3C6h

Pixel Data Mask Register

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C6h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PIXEL_DATA_MASK							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RW	**PIXEL_DATA_MASK:** In indexed-color mode, the 8 bits of this register are logically ANDed with the 8 bits of pixel data received from the frame buffer for each pixel. The result of this ANDing process becomes the actual index used to select color data positions within the palette. This has the effect of limiting the choice of color data positions that may be specified by the incoming 8-bit data. 0 = Corresponding bit in the resulting 8-bit index being forced to 0. 1 = Allows the corresponding bit in the resulting index to reflect the actual value of the corresponding bit in the incoming 8-bit pixel data.

14.10.8 DACWX—Offset 3C8h

Palette Write Index Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0

PALETTE_WRITE_INDEX

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b WO	**PALETTE_WRITE_INDEX:** The 8-bit index value programmed into this register chooses which of 256 standard color data positions within the palette are to be made accessible for being written via the Palette Data Register (DACDATA). The index value held in this register is automatically incremented when all three bytes of the color data position selected by the current index have been written. This register allows access to the palette even when running non-VGA display modes.

14.10.9 DACDATA—Offset 3C9h

Palette Data Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C9h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PALETTE_DATA							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RW	**PALETTE_DATA:** This byte-wide data port provides read or write access to the three bytes of data of each color data position selected using the Palette Read Index Register (DACRX) or the Palette Write Index Register (DACWX). The three bytes in each color data position are read or written in three successive read or write operations. The first byte read or written specifies the intensity of the red component of the color specified in the selected color data position. The second byte is for the green component, and the third byte is for the blue component. When writing data to a color data position, all three bytes must be written before the hardware will actually update the three bytes of the selected color data position. When reading or writing to a color data position, ensure that neither the Palette Read Index Register (DACRX) or the Palette Write Index Register (DACWX) are written to before all three bytes are read or written. A write to either of these two registers causes the circuitry that automatically cycles through providing access to the bytes for red, green and blue components to be reset such that the byte for the red component is the one that will be accessed by the next read or write operation via this register. This register allows access to the palette even when running non-VGA display modes. Writes to the palette can cause sparkle if not done during inactive video periods. This sparkle is caused by an attempt to write and read the same address on the same cycle. Anti-sparkle circuits will substitute the previous pixel value for the read output.

14.10.10 FCR (FCR_Read)—Offset 3CAh

Feature Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3CAh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED				VSYNC_CONTROL	RESERVED_1		

Bit Range	Default & Access	Field Name (ID): Description
7:4	0b RW	**RESERVED:** Read as 0.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Ena ble output on the VSYNC pin. This capability was not typically very useful..
2:0	0b RW	**RESERVED_1:** Read as 0.

14.10.11 MSR (MSR_READ)—Offset 3CCh

Miscellaneous Output

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3CCh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CRT_VSYNC_POLARITY	CRT_HSYNC_POLA_RITY	PAGE_SELECT	RESERVED	CLOCK_SELECT		A0000_BFFFFH_MEMORY_ACCESS_ENABLE	I_O_ADDRESS_SELECT

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**CRT_VSYNC_POLARITY:** This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. Sync polarity was used in VGA to signal the monitor how many lines of active display are being generated. 0 = Positive Polarity (default). 1 = Negative Polarity.
6	0b RW	**CRT_HSYNC_POLA_RITY:** This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. 0 = Positive Polarity (default). 1 = Negative Polarity

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**PAGE_SELECT:** In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KB page in dis play mem ory for CPU access: 0 = Upper page (default) 1 = Lower page. Selects between two 64KB pages of frame buffer memory during standard VGA odd/ even modes (modes 0h through 5h). Bit 1 of register GR06 can also program this bit in other modes. Note that this bit is would normally set to 1 by the software.
4	0b RW	**RESERVED:** Read as 0.
3:2	0b RW	**CLOCK_SELECT:** These bits can select the dot clock source for the CRT interface. The bits should be used to select the dot clock in standard native VGA modes only. When in the centering or upper left corner modes, these bits should be set to have no effect on the clock rate. The actual frequencies that these bits select, if they have any affect at all, is programmable through the DPLL registers that default to the standard values used for VGA. 00 = CLK0, 25.175 MHz (for standard VGA modes with 640 pixel (8-dot) horizontal resolution) (default) 01 = CLK1, 28.322 MHz. (for standard VGA modes with 720 pixel (9-dot) horizontal resolution) 10 = Was used to select an external clock (now unused) 11 = Reserved
1	0b RW	**A0000_BFFFFH_MEMORY_ACCESS_ENABLE:** VGA Compatibility bit enables access to local video memory (frame buffer) at A0000(BFFFFh. When disabled, accesses to VGA memory are blocked in this region. This bit is independent of and does not block CPU access to the video linear frame buffer at other addresses. Note that it is typical for AGP chipsets to shadow this register to allow proper steering of memory accesses to the proper bus. 0 = Prevent CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture (default). 1 = Allow CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture. This memory must be mapped as UC by the CPU; see VGA Host Access Memory Munging in Display and Overlay Functions.
0	0b RW	**I_O_ADDRESS_SELECT:** This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller re gisters, the Feature Control Register (FCR), and Input Status Register 1 (ST01). Presently ignored (whole range is claimed), but will ignore 3Bx for color configuration or 3Dx for monochrome. Note that it is typical in AGP chipsets to shadow this bit and properly steer I/O cycles to the proper bus for operation where a MDA exists on another bus such as ISA. 0 = Select 3Bxh I/O address (MDA emulation) (default). 1 = Select 3Dxh I/O address (CGA emulation).

14.10.12 GRX—Offset 3CEh

GRX Graphics Controller Index Register

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3CEh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED			SEQUENCER_REGISTER_INDEX				

Bit Range	Default & Access	Field Name (ID): Description
7:5	0b RW	**RESERVED:** Read as 0.
4:0	0b RW	**SEQUENCER_REGISTER_INDEX:** This field selects any one of the graphics controller registers (GR00-GR11]) to be accessed via the data port at I/O (or memory offset) location 3CFh.

14.10.13 GR—Offset 3CFh

GR index registers

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3CFh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
GR_REGISTER_DESCRIPTIONS							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RW	**GR_REGISTER_DESCRIPTIONS:** GR indexed register descriptions

14.10.14 CRX (CRX_CGA)—Offset 3D4h

CRT Controller Index Register

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED	CRT_CONTROLLER_INDEX						

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**RESERVED:** Read as 0.
6:0	0b RW	**CRT_CONTROLLER_INDEX:** These 7 bits are used to select any one of the CRT controller registers to be accessed via the data port at I/O location 3B5h or 3D5h, depending upon whether the graphics system is configured for MDA or CGA emulation. The data port memory address offsets are 3B5h/3D5h.

14.10.15 CR (CR_CGA)—Offset 3D5h

CR index registers

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3D5h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CR_REGISTER_DESCRIPTIONS							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RW	**CR_REGISTER_DESCRIPTIONS:** CR indexed register descriptions

14.10.16 GPIOCTL_0—Offset 5010h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h

Bits	Default	Field
31:13	0000000000000000000	RESERVED
12	0	GPIO_DATA_IN_RO
11	1	GPIO_DATA_VALUE_R_W
10	0	GPIO_DATA_MASK_WO
9	0	GPIO_DATA_DIRECTION_VALUE_R_W
8	0	GPIO_DATA_DIRECTION_MASK_WO
7:5	000	RESERVED_1
4	0	GPIO_CLOCK_DATA_IN_RO
3	1	GPIO_CLOCK_DATA_VALUE_R_W
2	0	GPIO_CLOCK_DATA_MASK_WO
1	0	GPIO_CLOCK_DIRECTION_VALUE_R_W
0	0	GPIO_CLOCK_DIRECTION_MASK_WO

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.

Bit Range	Default & Access	Field Name (ID): Description
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

14.10.17 GPIOCTL_1—Offset 5014h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h

Bits	31:13	12	11	10	9	8	7:5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0	0	0	0 0 0	0	1	0	0	0
Field	RESERVED	GPIO_DATA_IN_RO	GPIO_DATA_VALUE_R_W	GPIO_DATA_MASK_WO	GPIO_DATA_DIRECTION_VALUE_R_W	GPIO_DATA_DIRECTION_MASK_WO	RESERVED_1	GPIO_CLOCK_DATA_IN_RO	GPIO_CLOCK_DATA_VALUE_R_W	GPIO_CLOCK_DATA_MASK_WO	GPIO_CLOCK_DIRECTION_VALUE_R_W	GPIO_CLOCK_DIRECTION_MASK_WO

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)

Bit Range	Default & Access	Field Name (ID): Description
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

14.10.18 GPIOCTL_2—Offset 5018h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h

Bits	Default	Field
31:13	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	RESERVED
12	0	GPIO_DATA_IN_RO
11	1	GPIO_DATA_VALUE_R_W
10	0	GPIO_DATA_MASK_WO
9	0	GPIO_DATA_DIRECTION_VALUE_R_W
8	0	GPIO_DATA_DIRECTION_MASK_WO
7:5	0 0 0	RESERVED_1
4	0	GPIO_CLOCK_DATA_IN_RO
3	1	GPIO_CLOCK_DATA_VALUE_R_W
2	0	GPIO_CLOCK_DATA_MASK_WO
1	0	GPIO_CLOCK_DIRECTION_VALUE_R_W
0	0	GPIO_CLOCK_DIRECTION_MASK_WO

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only

Bit Range	Default & Access	Field Name (ID): Description
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

14.10.19 GPIOCTL_3—Offset 501Ch

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 501Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h

Bits	Default	Field
31:13	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	RESERVED
12	0	GPIO_DATA_IN_RO
11	1	GPIO_DATA_VALUE_R_W
10	0	GPIO_DATA_MASK_WO
9	0	GPIO_DATA_DIRECTION_VALUE_R_W
8	0	GPIO_DATA_DIRECTION_MASK_WO
7:5	0 0 0	RESERVED_1
4	0	GPIO_CLOCK_DATA_IN_RO
3	1	GPIO_CLOCK_DATA_VALUE_R_W
2	0	GPIO_CLOCK_DATA_MASK_WO
1	0	GPIO_CLOCK_DIRECTION_VALUE_R_W
0	0	GPIO_CLOCK_DIRECTION_MASK_WO

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only

Bit Range	Default & Access	Field Name (ID): Description
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

14.10.20 GPIOCTL_4—Offset 5020h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000808h

Bits	Default	Field
31:13	0000 0000 0000 0000 000	RESERVED
12	0	GPIO_DATA_IN_RO
11	1	GPIO_DATA_VALUE_R_W
10	0	GPIO_DATA_MASK_WO
9	0	GPIO_DATA_DIRECTION_VALUE_R_W
8	0	GPIO_DATA_DIRECTION_MASK_WO
7:5	000	RESERVED_1
4	0	GPIO_CLOCK_DATA_IN_RO
3	1	GPIO_CLOCK_DATA_VALUE_R_W
2	0	GPIO_CLOCK_DATA_MASK_WO
1	0	GPIO_CLOCK_DIRECTION_VALUE_R_W
0	0	GPIO_CLOCK_DIRECTION_MASK_WO

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**RESERVED:** Reserved.
12	0b RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	1b RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0b WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0b RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0b WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0b RW	**RESERVED_1:** must be written with zeros.
4	0b RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	1b RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
2	0b WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0b RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.

Bit Range	Default & Access	Field Name (ID): Description
0	0b WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

14.10.21 GMBUS0—Offset 5100h

GMBUS Clock/Port Select gmbus clock and port select (gmbus_register.v reg_gmbus0)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:16	15	14:12	11	10:8	7:3	2:0
Default	0000 0000 0000 0000	0	000	0	000	00000	000
Field	RESERVED	HOLD_TIME_EXTENSION	RESERVED_1	AKSV_BUFFER_SELECT	GMBUS_RATE_SELECT	RESERVED_2	PIN_PAIR_SELECT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15	0b RW	**HOLD_TIME_EXTENSION:** This bit selects the hold time on the data line driven from the GMCH. 0 = Hold time of 0ns 1 = Hold time of 300 ns
14:12	0b RW	**RESERVED_1:** Reserved.
11	0b RW	**AKSV_BUFFER_SELECT:** [DevBLC, DevCTG, DevCDV] This bit selects whether the data to be written over GMBUS comes from the Aksv buffer for HDCP authentication, or from the GMBUS data buffer. Please note that when writing data from the Aksv buffer, all GMBUS protocol must be followed, including indicating the number of bytes to be transferred during the DATA phase of a GMBUS cycle. 0 (Default) Use the GMBUS data buffer (GMBUS3) for data transmission 1 Use the Aksv data buffer (GMBUS6 and GMBUS7) for data transmission. [DevBW, DevCL] Reserved:

Bit Range	Default & Access	Field Name (ID): Description
10:8	0b RW	**GMBUS_RATE_SELECT:** These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed when between transfers when the GMBUS is idle. 1xx = Reserved. 000 = 100 KHz 001 = 50 KHz 010 = 400 KHz 011 = 1 MHz for SDVO
7:3	0b RW	**RESERVED_2:** Reserved.
2:0	0b RW	**PIN_PAIR_SELECT:** This field selects an GMBUS pin pair for use in the GMBUS communication. Use the table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers. 000 = None (disabled) 001 = MIPI I2C use 010 = Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK) 011 = Reserved 100 = DP/HDMI port C Use [DevCTG] 101 = sDVO/HDMI Use 110 = Reserved 111 = D connector control signals

14.10.22 GMBUS1—Offset 5104h

GMBUS Command and Status gmbus command and status (gmbus_register.v reg_gmbus1)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5104h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	SOFTWARE_CLEAR_INTERRUPT_SW_CLR_INT
30	0	SOFTWARE_READY_SW_RDY
29	0	ENABLE_TIMEOUT_ENT
28	0	RESERVED
27:25	000	BUS_CYCLE_SELECT
24:16	000000000	TOTAL_BYTE_COUNT
15:8	00000000	_8_BIT_GMBUS_SLAVE_REGISTER_INDEX_INDEX
7:1	0000000	_7_BIT_GMBUS_SLAVE_ADDRESS_SADDR
0	0	SLAVE_DIRECTION_BIT

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SOFTWARE_CLEAR_INTERRUPT_SW_CLR_INT:** This bit must be clear for normal operation. Setting the bit , then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. 0 = If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. 1 = Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
30	0b RW	**SOFTWARE_READY_SW_RDY:** Data handshake bit used in conjunction with HW_RDY bit. 0 = De-asserted via the assertion event for HW_RDY bit 1 = When asserted by software, results in de-assertion of HW_RDY bit
29	0b RW	**ENABLE_TIMEOUT_ENT:** Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set. 0 = disable timeout counter 1 = enable timeout counter
28	0b RW	**RESERVED:** Reserved.
27:25	0b RW	**BUS_CYCLE_SELECT:** 000 = No GMBUS cycle is generated. 001 = GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT 010 = Reserved 011 = GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT 100 = Generates a STOP if currently in a WAIT or after the completion of the current byte if active. 101 = GMBUS cycle is generated without an INDEX and with a STOP 110 = Reserved 111 = GMBUS cycle is generated with an INDEX and with a STOP GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle. This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase: Note that the three bits can be decoded as follows: 27 = STOP generated 26 = INDEX used 25 = cycle ends in a WAIT
24:16	0b RW	**TOTAL_BYTE_COUNT:** (9-bits). This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle. The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select). Do not change the value of this field during GMBUS cycles transactions.
15:8	0b RW	**_8_BIT_GMBUS_SLAVE_REGISTER_INDEX_INDEX:** This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. Do not change this field during a GMBUS transaction.

Bit Range	Default & Access	Field Name (ID): Description
7:1	0b RW	**_7_BIT_GMBUS_SLAVE_ADDRESS_SADDR:** When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (xx) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. Special Slave Addresses 0000 000R = General Call Address 0000 000W = Start byte 0000 001x = CBUS Address 0000 010x = Reserved 0000 011x = Reserved 0000 1xxx = Reserved 1111 1xxx = Reserved 1111 0xxx = 10-Bit addressing
0	0b RW	**SLAVE_DIRECTION_BIT:** When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. 1 = Indicates that a Read from the slave device operation is to be performed. 0 = Indicates that a Write to slave device operation is to be performed.

14.10.23 GMBUS2—Offset 5108h

GMBUS Status Register gmbus status (gmbus_register.v reg_gmbus2)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5108h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000800h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RESERVED																INUSE	HARDWARE_WAIT_PHASE_HW_WAIT_PHASE_READ_ONLY	SLAVE_STALL_TIMEOUT_ERROR_READ_ONLY	GMBUS_INTERRUPT_STATUS_READ_ONLY	HARDWARE_READY_HW_RDY_READ_ONLY	NAK_INDICATOR_READ_ONLY	GMBUS_ACTIVE_GA_READ_ONLY	CURRENT_BYTE_COUNT_READ_ONLY								

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15	0b RW/1C	**INUSE:** 0 = read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect. 1 = read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and In use . Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0. Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don t know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software s indication that the software use of this resource is now terminated and it is available for other clients. AccessType: One to clear
14	0b RO	**HARDWARE_WAIT_PHASE_HW_WAIT_PHASE_READ_ONLY:** 0 = The GMBUS engine is not in a wait phase. 1 = Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP. Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS. AccessType: Read Only
13	0b RO	**SLAVE_STALL_TIMEOUT_ERROR_READ_ONLY:** This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit. 0 = No slave timeout has occurred. 1 = A slave acknowledge timeout has occurred AccessType: Read Only

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**GMBUS_INTERRUPT_STATUS_READ_ONLY:** This bit indicates that an event that causes a GMBUS interrupt has occurred. 0 = The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the SW_CLR_INT bit. 1 = GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register. [DevCDV, DevCTG]: Reserved AccessType: Read Only
11	1b RO	**HARDWARE_READY_HW_RDY_READ_ONLY:** This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations. This data handshake bit is used in conjunction with the SW_RDY bit. When this bit is changed to asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit. 0 = Condition required for assertion has not occurred or when this bit was a one and: SW_RDY bit has been asserted. During a GMBUS read transaction, after the each read of the data register. During a GMBUS write transaction, after each write of the data register. SW_CLR_INT bit has been cleared. 1 = This bit is asserted under the following conditions: After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit. When an active GMBUS cycle has terminated with a STOP. When during a GMBUS write transaction, the data register needs and can accept another four bytes of data. During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data. This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0. AccessType: Read Only
10	0b RO	**NAK_INDICATOR_READ_ONLY:** Was previously called Slave Acknowledge Timeout Error SATOER. 0 = No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error. 1 = Set by hardware if any expected device acknowledge is not received from the slave within the timeout. AccessType: Read Only
9	0b RO	**GMBUS_ACTIVE_GA_READ_ONLY:** This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not. 0 = The GMBUS controller is currently IDLE. 1 = This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE. AccessType: Read Only
8:0	0b RO	**CURRENT_BYTE_COUNT_READ_ONLY:** Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware. Set to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase. Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register. AccessType: Read Only

14.10.24 GMBUS3—Offset 510Ch

GMBUS Data Buffer gmbus data buffer (gmbus_register.v reg_gmbus3)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 510Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA_BYTE_3								DATA_BYTE_2								DATA_BYTE_1								DATA_BYTE_0							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**DATA_BYTE_3:** gmbus data buffer DATA Byte 3
23:16	0b RW	**DATA_BYTE_2:** gmbus data buffer DATA Byte 2
15:8	0b RW	**DATA_BYTE_1:** gmbus data buffer DATA Byte 1
7:0	0b RW	**DATA_BYTE_0:** gmbus data buffer DATA Byte 0

14.10.25 GMBUS4—Offset 5110h

GMBUS Interrupt Mask gmbus interrupt mask (gmbus_register.v reg_gmbus4)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																											INTERRUPT_MASK				

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0b RW	**INTERRUPT_MASK:** This field specifies which GMBUS interrupts events may contribute to the setting of gmbus interrupt status bit in second level interrupt status register PIPEASTAT. Bit 4: GMBUS Slave stall timeout Bit 3: GMBUS NAK Bit 2: GMBUS Idle Bit 1: Hardware wait (GMBUS cycle without a stop has completed) Bit 0: Hardware ready (Data has been transferred) 0 = Disable this type of GMBUS interrupt 1 = Enable this type of GMBUS interrupt

14.10.26 GMBUS5—Offset 5120h

2 Byte Index Register gmbus index (gmbus_register.v reg_gmbus5)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5120h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30:16	15:0
0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
_2_BYTE_INDEX_ENABLE	RESERVED	_2_BYTE_SLAVE_INDEX

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**_2_BYTE_INDEX_ENABLE:** When this bit is asserted (1), then bits 15:00 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1(15:8) are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
30:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**_2_BYTE_SLAVE_INDEX:** This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

14.10.27 GMBUS6—Offset 5130h

GMBUS Aksv Buffer Low [DevBLC, DevCTG, DevCDV] gmbus data buffer (gmbus_register.v reg_gmbus6)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5130h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA_BYTE_3								DATA_BYTE_2								DATA_BYTE_1								DATA_BYTE_0							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b WO	**DATA_BYTE_3:** gmbus data buffer DATA Byte 3
23:16	0b WO	**DATA_BYTE_2:** gmbus data buffer DATA Byte 2
15:8	0b WO	**DATA_BYTE_1:** gmbus data buffer DATA Byte 1
7:0	0b WO	**DATA_BYTE_0:** gmbus data buffer DATA Byte 0

14.10.28 GMBUS7—Offset 5134h

GMBUS Aksv Buffer High [DevBLC, DevCTG, DevCDV] gmbus data buffer (gmbus_register.v reg_gmbus7)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 5134h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																							AKSV_SELECTION_BIT	DATA_BYTE_5							

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b WO	**RESERVED:** MBZ
8	0b WO	**AKSV_SELECTION_BIT:** [DevVLVP]: • 0 = The fuse value of the Aksv is used. • 1 = The register value of the Aksv is used. Aksv Selection Bit [DevELK, DevCDV]: • 0 = The register value of the Aksv is used. • 1 = The fuse value of the Aksv is used. [DevBLC, DevCTG] Reserved
7:0	0b WO	**DATA_BYTE_5:** gmbus data buffer DATA Byte 5

14.10.29 DPLLA_CTRL—Offset 6014h

DPLL A Control Register DPLL A Control (cpdmmreg.v reg03_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00002000h

Bit	31	30	29	28	27:26	25:24	23:16	15	14	13	12:9	8	7:0
Default	0	0	0	0	0 0	0 0	0 0 0 0 0 0 0 0	0	0	1	0 0 0 0	0	0 0 0 0 0 0 0 0
Field	DPLL_A_VCO_ENABLE	DPLLA_EXTERNAL_CLOCK_BUFFER_ENABLE	REFA_CLOCK_ENABLE	VGA_MODE_DISABLE	ENABLE_SINGLE_DPLLA_FREQUENCY_FOR_BOTH_PIPES	RESERVED	RESERVED_1	RESERVED_2	VCC_VOLTAGE_SELECT	DPLL_A_REFERENCE_INPUT_SELECT	RESERVED_3	DISPLAY_RATE_SWITCH_PIPEA	DPIO_PHYSTATUS_READ_ONLY

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DPLL_A_VCO_ENABLE:** Disabling the PLLA will cause the display dot clock to stop. 0 = DPLLA is disabled in its lowest power state (default) 1 = DPLLA is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	0b RW	**DPLLA_EXTERNAL_CLOCK_BUFFER_ENABLE:** [DevVLVP] 0 = Disable DPLLA clock from being driven out 1 = Enable DPLLA clock to be drive out [DevCDV] Reserved DPLLA Serial DVO High Speed IO clock Enable 0 = High Speed IO Clock Disabled (default) 1 = High Speed IO Clock Enabled (must be set in Serial DVO and HDMI modes)
29	0b RW	**REFA_CLOCK_ENABLE:** [DevCDV, DevVLVP]: Indicate the reference clock of PLL A is enable 0 Disable (default) 1 Enable
28	0b RW	**VGA_MODE_DISABLE:** When in native VGA modes, writes to the VGA MSR register causes the value in the selected (by MSR bits) VGA clock control register to be loaded into the active register. This allows the VGA clock select to select the pixel frequency between the two standard VGA pixel frequencies. 0 = VGA MSR(3:2) Clock Control bits select DPLL A Frequency 1 = Disable VGA Control
27:26	0b RW	**ENABLE_SINGLE_DPLLA_FREQUENCY_FOR_BOTH_PIPES:** [DevVLVP] When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode can allow using only DPLLA to feed both pipes. DPLLB should be shutdown to save power. This control is double buffered. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved [DevCDV] Reserved DPLLA Mode Select : Configure the DPLLA for various supported Display Modes 00 = Reserved 01 = DPLLA in DAC/Serial DVO/UDI/Integrated TV mode 10 = DPLLA in LVDS mode (Mobile devices ONLY) otherwise RESERVED 11 = DP

Bit Range	Default & Access	Field Name (ID): Description
25:24	0b RW	**RESERVED:** [DevCDV, DevVLVP] FPA0/FPA1 P2 Clock Divide: 00 = Divide by 10. This is used when Dot Clock =(270MHz in sDVO, HDMI, or DAC modes 01 = Divide by 5. This is used when Dot Clock)270MHz 10 = Reserved 11 = Reserved For DPLLA in LVDS mode, BITS(27:26)=10 00 = Divide by 14. This is used in Single-Channel LVDS 01 = Divide by 7. This is used in Dual-Channel LVDS 10 = Reserved 11 = Reserved
23:16	0b RW	**RESERVED_1:** [DevCDV, DevVLVP] FPA0/ FPA1 P1 Post Divisor: Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b = Divide by one 00000010b = Divide by two 00000100b = Divide by three 00001000b = Divide by four 00010000b = Divide by five 00100000b = Divide by six 01000000b = Divide by seven 10000000b = Divide by Eight All other values are illegal and should not be used
15	0b RW	**RESERVED_2:** Write as zero PLLA Lock [DevCDV, DevVLVP] (RO) 1 - PLLA Lock 0 PLLA unlock
14	0b RW	**VCC_VOLTAGE_SELECT:** [DevVLVP] This control selects the VCC voltage in DPLL 0 = 1.0 V (default) 1 = voltage for LDO circuit (for TNG use) [DevCDV] Reserved
13	1b RW	**DPLL_A_REFERENCE_INPUT_SELECT:** [DevVLVP] This control selects the integrated core refclk or external OSC refclk as the input clock source to DPLL A. 0 = External refclk pad (27MHz) 1 = Integrated core refclk (default is 100 MHz) [DevCDV] Reserved PLL Reference Input Select: The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder.

Bit Range	Default & Access	Field Name (ID): Description
12:9	0b RW	**RESERVED_3:** [DevCDV, DevVLVP] Parallel to Serial Load Pulse phase selection: Programmable select bits to choose the relative phase of the high speed (10X) DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays (phase 0 represents 1 flop delay) of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 = use clock phase-4 0101 = use clock phase-5 0110 = use clock phase-6 (Default value) 0111 = use clock phase-7 1000 = use clock phase-8 1001 = use clock phase-9 1010 = use clock phase-10 1011 = use clock phase-11 1100 = use clock phase-12 1101 = use clock phase-13 Phases 0 through 3 are not available for Load Pulse selection. [DevCL] The following programming is recommended for Crestline based on PV timing analysis: 1101 use clock phase-13 [DevBLC, DevCTG] Reserved. Programming for load pulse is in PXP AFE config space.
8	0b RW	**DISPLAY_RATE_SWITCH_PIPEA:** [DevCTG, DevCDV, DevVLVP] Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00) [DevBW, DevCL, DevBLC] Reserved
7:0	0b RO	**DPIO_PHYSTATUS_READ_ONLY:** [DevVLVP] This field contains the two 4-bit ModPhy lane status. One for PortB and one for PortC Bit 7:4 = Port C PhyStatus[3:0] Bit 3:0 = Port B PhyStatus[3:0] [DevBW, DevCL, DevBLC, DevCDV] Reserved [DevCTG] FPA1 P1 Post Divisor: Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b - Divide by one 00000010b - Divide by two 00000100b - Divide by three 00001000b - Divide by four 00010000b - Divide by five 00100000b - Divide by six 01000000b - Divide by seven 10000000b - Divide by Eight All other values are illegal and should not be used AccessType: Read Only

14.10.30 DPLLB_CTRL—Offset 6018h

DPLL B Control Registers DPLL B Control (cpdmmreg.v reg04_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00006000h

Bits	Default	Field
31	0	DPLL_B_VCO_ENABLE
30	0	DPLLB_EXTERNAL_CLOCK_BUFFER_ENABLE
29	0	REFB_CLOCK_ENABLE
28	0	VGA_MODE_DISABLE
27:26	0 0	ENABLE_SINGLE_DPLLB_FREQUENCY_FOR_BOTH_PIPES
25:24	0 0	RESERVED
23:16	0 0 0 0 0 0 0 0	RESERVED_1
15	0	RESERVED_2
14	1	DPIO_COMMON_REGISTER_INTERFACE_CLOCK_SELECT_CRICLKSEL
13	1	DPLL_B_REFERENCE_INPUT_SELECT
12:9	0 0 0 0	RESERVED_3
8	0	DISPLAY_RATE_SWITCH_PIPEB
7:0	0 0 0 0 0 0 0 0	RESERVED_4

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DPLL_B_VCO_ENABLE:** Disabling the PLLB will cause the display dot clock to stop. 0 = DPLLB is disabled in its lowest power state (default) 1 = DPLLB is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	0b RW	**DPLLB_EXTERNAL_CLOCK_BUFFER_ENABLE:** [DevVLVP] 0 = Disable DPLLB clock from being driven out 1 = Enable DPLLB clock to be drive out [DevCDV] Reserved DPLLB Serial DVO High Speed IO clock Enable 0 = High Speed IO Clock Disabled (default) 1 = High Speed IO Clock Enabled (must be set in Serial DVO and HDMI modes)
29	0b RW	**REFB_CLOCK_ENABLE:** [DevCDV, DevVLVP]: Indicate the reference clock of PLL A is enable 0 Disable (default) 1 Enable
28	0b RW	**VGA_MODE_DISABLE:** When in native VGA modes, writes to the VGA MSR register causes the value in the selected (by MSR bits) VGA clock control register to be loaded into the active register. This allows the VGA clock select to select the pixel frequency between the two standard VGA pixel frequencies. 0 = VGA MSR(3:2) Clock Control bits select DPLL A Frequency 1 = Disable VGA Control

Bit Range	Default & Access	Field Name (ID): Description
27:26	0b RW	**ENABLE_SINGLE_DPLLB_FREQUENCY_FOR_BOTH_PIPES:** [DevVLVP] When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode can allow using only DPLLB to feed both pipes. DPLLA should be shutdown to save power. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved [DevCDV] Reserved DPLLB Mode Select : Configure the DPLLB for various supported Display Modes 00 = Reserved 01 = DPLLA in DAC/Serial DVO/UDI/Integrated TV mode 10 = DPLLA in LVDS mode (Mobile devices ONLY) otherwise RESERVED 11 = DP
25:24	0b RW	**RESERVED:** [DevCDV, DevVLVP] FPB0/FPB1 P2 Clock Divide: 00 = Divide by 10. This is used when Dot Clock =(270MHz in sDVO, HDMI, or DAC modes 01 = Divide by 5. This is used when Dot Clock)270MHz 10 = Reserved 11 = Reserved For DPLLB in LVDS mode, BITS(27:26)=10 00 = Divide by 14. This is used in Single-Channel LVDS 01 = Divide by 7. This is used in Dual-Channel LVDS 10 = Reserved 11 = Reserved
23:16	0b RW	**RESERVED_1:** [DevCDV, DevVLVP] FPB0/ FPB1 P1 Post Divisor: Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b = Divide by one 00000010b = Divide by two 00000100b = Divide by three 00001000b = Divide by four 00010000b = Divide by five 00100000b = Divide by six 01000000b = Divide by seven 10000000b = Divide by Eight All other values are illegal and should not be used
15	0b RW	**RESERVED_2:** Write as zero PLLB Lock [DevCDV, DevVLVP] (RO) 1 - PLLB Lock 0 PLLB unlock
14	1b RW	**DPIO_COMMON_REGISTER_INTERFACE_CLOCK_SELECT_CRICLKSEL:** [DevVLVP] This bit is to control the clock source for DPIO Common Register Interface 0 = Use external reclk pad 1 = Use integrated core refclk (default)
13	1b RW	**DPLL_B_REFERENCE_INPUT_SELECT:** [DevVLVP] This control selects the integrated core refclk or external OSC refclk as the input clock source to DPLL B. 0 = External refclk pad (27MHz) 1 = Integrated core refclk (default is 100 MHz) [DevCDV] Reserved PLL Reference Input Select: The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder.

Bit Range	Default & Access	Field Name (ID): Description
12:9	0b RW	**RESERVED_3:** [DevCDV, DevVLVP] Parallel to Serial Load Pulse phase selection: Programmable select bits to choose the relative phase of the high speed (10X) DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays (phase 0 represents 1 flop delay) of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 = use clock phase-4 0101 = use clock phase-5 0110 = use clock phase-6 (Default value) 0111 = use clock phase-7 1000 = use clock phase-8 1001 = use clock phase-9 1010 = use clock phase-10 1011 = use clock phase-11 1100 = use clock phase-12 1101 = use clock phase-13 Phases 0 through 3 are not available for Load Pulse selection. [DevCL] The following programming is recommended for Crestline based on PV timing analysis: 1101 use clock phase-13 [DevBLC, DevCTG] Reserved. Programming for load pulse is in PXP AFE config space.
8	0b RW	**DISPLAY_RATE_SWITCH_PIPEB:** [DevCTG, DevCDV, DevVLVP] Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00) [DevBW, DevCL, DevBLC] Reserved
7:0	0b RW	**RESERVED_4:** [DevBW, DevCL, DevBLC, DevCDV, DevVLVP] [DevCTG] FPB1 P1 Post Divisor: Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b - Divide by one 00000010b - Divide by two 00000100b - Divide by three 00001000b - Divide by four 00010000b - Divide by five 00100000b - Divide by six 01000000b - Divide by seven 10000000b - Divide by Eight All other values are illegal and should not be used

14.10.31 DPLLAMD—Offset 601Ch

DPLL A SDVO/HDMI Multiplier/Divisor Register Pipe A multiply (cpdmmreg.v reg15_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 601Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	

RESERVED	DPLL_A_HDMI_DIVIDER_HI_RES	RESERVED_1	DPLL_A_HDMI_DIVIDER_VGA	RESERVED_2	DPLL_A_SDVO_HDMI_MULTIPLIER_HI_RES	RESERVED_3	DPLL_A_SDVO_HDMI_MULTIPLIER_VGA

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** Reserved.
29:24	0b RW	**DPLL_A_HDMI_DIVIDER_HI_RES:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the SDVO/HDMI multiplier. For SDVO and CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the SDVO/HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet 1 Default: 0000 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet 64 pixels per packet)
23:22	0b RW	**RESERVED_1:** Reserved.
21:16	0b RW	**DPLL_A_HDMI_DIVIDER_VGA:** When the source is VGA, these bits specify the HDMI divider. The format of this field is the same as that of the hi-res divider.
15:14	0b RW	**RESERVED_2:** Reserved.
13:8	0b RW	**DPLL_A_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multipler is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000000 (1X) Range: 0 63 (1X 64X)
7:6	0b RW	**RESERVED_3:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:0	000011b RW	**DPLL_A_SDVO_HDMI_MULTIPLIER_VGA:** When the source is VGA, these bits specify the HDMI multiplier. The format of this field is the same as that of the hi-res multiplier. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000011 (4X) Range: 0 63 (1X 64X)

14.10.32 DPLLBMD—Offset 6020h

DPLL B SDVO/HDMI Multiplier/Divisor Register Pipe B multiplyer (cpdmmreg.v reg16_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h

31	28	24	20	16	12	8	4	0

0 0	0 0 0 0 0 0	0 0	0 0 0 0 0 0	0 0	0 0 0 0 0 0	0 0	0 0 0 0 1 1
RESERVED	DPLL_B_HDMI_DIVIDER_HI_RES	RESERVED_1	DPLL_B_HDMI_DIVIDER_VGA	RESERVED_2	DPLL_B_SDVO_HDMI_MULTIPLIER_HI_RES	RESERVED_3	DPLL_B_SDVO_HDMI_MULTIPLIER_VGA

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29:24	0b RW	**DPLL_B_HDMI_DIVIDER_HI_RES:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the SDVO/HDMI multiplier. For SDVO and CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the SDVO/HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet 1 Default: 0000 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet 64 pixels per packet)
23:22	0b RW	**RESERVED_1:** Reserved.
21:16	0b RW	**DPLL_B_HDMI_DIVIDER_VGA:** When the source is VGA, these bits specify the HDMI divider. The format of this field is the same as that of the hi-res divider.
15:14	0b RW	**RESERVED_2:** Reserved.
13:8	0b RW	**DPLL_B_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multipler is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000011 (4X) Range: 0 63 (1X 64X)
7:6	0b RW	**RESERVED_3:** Reserved.
5:0	000011b RW	**DPLL_B_SDVO_HDMI_MULTIPLIER_VGA:** When the source is VGA, these bits specify the HDMI multiplier. The format of this field is the same as that of the hi-res multiplier. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000000 (1X) Range: 0 63 (1X 64X)

14.10.33 RAWCLK_FREQ—Offset 6024h

Rawclk Frequency

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0000007Dh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
RESERVED																						RAWCLK_FREQUENCY									

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**RESERVED:** Project: All Format:
9:0	0001111101b RW	**RAWCLK_FREQUENCY:** Project: All Format: Program this field with rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display.

14.10.34 D_STATE—Offset 6104h

D State Function Control Register Power state behaviour (cpdmmreg.v reg11_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6104h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 20D00400h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
DPLL_LOCK_TIME																RESERVED	DPLL_MIN_POWER_DOWN							RESERVED_1				DOT_CLOCK_PLL_POWER_DOWN_IN_D3	RESERVED_2	RESERVED_3	DOT_CLOCK_GATING

Bit Range	Default & Access	Field Name (ID): Description
31:16	0010000011010000b RW	**DPLL_LOCK_TIME:** (DevCDV): This is the time required to the DPLL to relock. The counter using the HRAW clk (5nsec) and resolution of 5nsec. (SEG DPLL lock time is 42usec)

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW	**RESERVED:** : MBZ
14:8	0000100b RW	**DPLL_MIN_POWER_DOWN:** (DevCDV): This is the minimum time required the DPLL to be power down until it is allowed to turn it on again. The HW counter using HRAW clk (5nsec) and has resolution of 160nsec (SEG DPLL required time is 0.5usec)
7:4	0b RW	**RESERVED_1:** : MBZ
3	0b RW	**DOT_CLOCK_PLL_POWER_DOWN_IN_D3:** This bit determines whether the PCI Power State Powers down the Dot Clock PLLs when in D3. A 0 on this bit does not power down the DPLLs, requiring software to gate them if necessary. When this bit is a 1, the dot PLLs are powered down when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register.
2	0b RW	**RESERVED_2:** Reserved.
1	0b RW	**RESERVED_3:** [DevCDV] Graphics Core Clock Gating: This bit determines whether the PCI Power State gates the Graphics Core clocks when in the D3 state. A 0 on this bit does not gate the clocks, requiring software to gate them if necessary. When this bit is a 1, the graphics core clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register. This register field has no use in current products.
0	0b RW	**DOT_CLOCK_GATING:** This bit determines whether the PCI Power State gates the Dot clocks when in the D3 state. A 0 on this bit does not gate the clocks, requiring software to gate them if necessary. When this bit is a 1, the dot clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register.

14.10.35 DSPCLK_GATE_D—Offset 6200h

Clock Gating Disable for Display Register clock gating (cpdmmreg.v reg12_lt)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 10000000h

31			28				24				20				16				12				8				4				0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HDCPUNIT_CLOCK_GATING_DISABLE	DPUNIT_PIPEB_CLOCK_GATING_DISABLE	VSUNIT_PIPE_A_CLOCK_GATING_DISABLE	VRHUNIT_CLOCK_GATING_DISABLE	VRDUNIT_CLOCK_GATING_DISABLE	AUDUNIT_CLOCK_GATING_DISABLE	DPUNIT_PIPEA_CLOCK_GATING_DISABLE	DPCUNIT_CLOCK_GATING_DISABLE	VSUNIT_PIPE_B_CLOCK_GATING_DISABLE	SPRITE_D_CLOCK_GATING_DISABLE	SPRITE_C_CLOCK_GATING_DISABLE	SPRITE_B_CLOCK_GATING_DISABLE	DVSUNIT_SPRITE_A_CLOCK_GATING_DISABLE	DDBUNIT_CLOCK_GATING_DISABLE	GMBUSUNIT_CLOCK_GATING_DISABLE	DPRUNIT_CLOCK_GATING_DISABLE	DPFUNIT_CLOCK_GATING_DISABLE	DPLRUNIT_PIPE_A_CLOCK_GATING_DISABLE	DPLSUNIT_PIPE_A_CLOCK_GATING_DISABLE	DPTUNIT_CLOCK_GATING_DISABLE	DPOUNIT_CLOCK_GATING_DISABLE	DPBUNIT_PIPE_A_CLOCK_GATING_DISABLE	DCUNIT_PIPE_A_CLOCK_GATING_DISABLE	DPGCUNIT_PIPE_B_CLOCK_GATING_DISABLE	DPGCUNIT_PIPE_A_CLOCK_GATING_DISABLE	DPIOUNIT_CLOCK_GATING_DISABLE	OVFUNIT_CLOCK_GATING_DISABLE	OVBUNIT_CLOCK_GATING_DISABLE	DPLRUNIT_PIPE_B_CLOCK_GATING_DISABLE	DPLSUNIT_PIPE_B_CLOCK_GATING_DISABLE	DPBUNIT_PIPE_B_CLOCK_GATING_DISABLE	DCUNIT_PIPE_B_CLOCK_GATING_DISABLE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**HDCPUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
30	0b RW	**DPUNIT_PIPEB_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
29	0b RW	**VSUNIT_PIPE_A_CLOCK_GATING_DISABLE:** [DevVLVP] (this bit used to be in PCI space in Calistoga) 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
28	1b RW	**VRHUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logicg 1 = Disable clock gating function Clock gating should not be enabled for this unit (this bit should always be set to 1.) [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
27	0b RW	**VRDUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
26	0b RW	**AUDUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
25	0b RW	**DPUNIT_PIPEA_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
24	0b RW	**DPCUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
23	0b RW	**VSUNIT_PIPE_B_CLOCK_GATING_DISABLE:** [DevVLVP] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW]. [DevCDV] and [DevVLVP]: Reserved

Bit Range	Default & Access	Field Name (ID): Description
22	0b RW	**SPRITE_D_CLOCK_GATING_DISABLE:** [DevVLVP] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW]. [DevCDV]: Reserved
21	0b RW	**SPRITE_C_CLOCK_GATING_DISABLE:** [DevVLVP] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW]. [DevCDV]: Reserved
20	0b RW	**SPRITE_B_CLOCK_GATING_DISABLE:** [DevVLVP] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC]. [DevCDV]: Reserved
19	0b RW	**DVSUNIT_SPRITE_A_CLOCK_GATING_DISABLE:** [DevBW] and [DevCL] 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].
18	0b RW	**DDBUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevCTG] Always program this bit to 1
17	0b RW	**GMBUSUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
16	0b RW	**DPRUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
15	0b RW	**DPFUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
14	0b RW	**DPLRUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].
13	0b RW	**DPLSUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].
12	0b RW	**DPTUNIT_CLOCK_GATING_DISABLE:** [DevVLVP] [DevCDV] Dplunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].
11	0b RW	**DPOUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
10	0b RW	**DPBUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
9	0b RW	**DCUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

Bit Range	Default & Access	Field Name (ID): Description
8	0b RW	**DPGCUNIT_PIPE_B_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
7	0b RW	**DPGCUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
6	0b RW	**DPIOUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
5	0b RW	**OVFUNIT_CLOCK_GATING_DISABLE:** [DevBW, DevCL, DevCDV] [DevCTG] DPFCunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
4	0b RW	**OVBUNIT_CLOCK_GATING_DISABLE:** [DevBW, DevCL, DevCDV] [DevCTG] DPFDunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
3	0b RW	**DPLRUNIT_PIPE_B_CLOCK_GATING_DISABLE:** (not in CDV)
2	0b RW	**DPLSUNIT_PIPE_B_CLOCK_GATING_DISABLE:** (not in CDV)
1	0b RW	**DPBUNIT_PIPE_B_CLOCK_GATING_DISABLE:** [DevVLVP] [DevBW, DevCL, DevCDV] Ovuunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].
0	0b RW	**DCUNIT_PIPE_B_CLOCK_GATING_DISABLE:** [DevVLVP] [DevBW, DevCL, DevCDV] Ovlunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].

14.10.36 DPPSR_CGDIS—Offset 6204h

Panel Self Refresh Clock Gating Disable for Display PSR clock gating disable controls (cpdmmreg.v)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6204h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000200h

Bit	Default	Field
31	0	LOW_POWER_SINGLE_PIPE_A_LPSSA_CLOCK_GATING_DISABLE
30	0	LOW_POWER_SINGLE_PIPE_B_LPSSA_CLOCK_GATING_DISABLE
29:26	0000	RESERVED
25	0	DPIO_CLOCK_BUFFER_ENABLE_CLOCK_GATING_DISABLE
24	0	DISPLAY_PLANE_A_PSR_CLOCK_GATING_DISABLE
23	0	DISPLAY_PLANE_B_PSR_CLOCK_GATING_DISABLE
22	0	SPRITE_A_PSR_CLOCK_GATING_DISABLE
21	0	SPRITE_B_PSR_CLOCK_GATING_DISABLE
20	0	SPRITE_C_PSR_CLOCK_GATING_DISABLE
19	0	SPRITE_D_PSR_CLOCK_GATING_DISABLE
18	0	CURSOR_A_PSR_CLOCK_GATING_DISABLE
17	0	CURSOR_B_PSR_CLOCK_GATING_DISABLE
16	0	DISPLAY_BLENDER_A_PSR_CLOCK_GATING_DISABLE
15	0	DISPLAY_BLENDER_B_PSR_CLOCK_GATING_DISABLE
14	0	DISPLAY_GAMMA_CORRECTION_A_PSR_CLOCK_GATING_DISABLE
13	0	DISPLAY_GAMMA_CORRECTION_B_PSR_CLOCK_GATING_DISABLE
12	0	DISPLAY_GCI_PSR_CLOCK_GATING_DISABLE
11	0	AUDFUNIT_PSR_CLOCK_GATING_DISABLE
10	0	AUDBUNIT_PSR_CLOCK_GATING_DISABLE
9	1	CPDUNIT_PSR_CLOCK_GATING_DISABLE
8	0	DDBMUNIT_PSR_CLOCK_GATING_DISABLE
7	0	DPFUNIT_PSR_CLOCK_GATING_DISABLE
6	0	DPIOUNIT_PSR_CLOCK_GATING_DISABLE
5	0	DISPLAYPORT_DPTUNIT_PSR_CLOCK_GATING_DISABLE
4	0	DPOUNIT_PSR_CLOCK_GATING_DISABLE
3	0	HDCPUNIT_PSR_CLOCK_GATING_DISABLE
2	0	VRDUNIT_PSR_CLOCK_GATING_DISABLE
1	0	VRHUNIT_PSR_CLOCK_GATING_DISABLE
0	0	DISPLAY_FUSE_WRAPPER_PSR_CLOCK_GATING_DISABLE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**LOW_POWER_SINGLE_PIPE_A_LPSSA_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. Pipe A shall be enabled 1 = Disable trunk clock gating on pipe A even when LPSSA is on
30	0b RW	**LOW_POWER_SINGLE_PIPE_B_LPSSA_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. Pipe B shall be enabled 1 = Disable trunk clock gating on pipe B even when LPSSA is on
29:26	0b RW	**RESERVED:** Reserved.
25	0b RW	**DPIO_CLOCK_BUFFER_ENABLE_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by DPIO clock buffer enable 1=Disable clock gating function by DPIO clock buffer enable
24	0b RW	**DISPLAY_PLANE_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
23	0b RW	**DISPLAY_PLANE_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
22	0b RW	**SPRITE_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
21	0b RW	**SPRITE_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
20	0b RW	**SPRITE_C_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

Bit Range	Default & Access	Field Name (ID): Description
19	0b RW	**SPRITE_D_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
18	0b RW	**CURSOR_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
17	0b RW	**CURSOR_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
16	0b RW	**DISPLAY_BLENDER_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
15	0b RW	**DISPLAY_BLENDER_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
14	0b RW	**DISPLAY_GAMMA_CORRECTION_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
13	0b RW	**DISPLAY_GAMMA_CORRECTION_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
12	0b RW	**DISPLAY_GCI_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
11	0b RW	**AUDFUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function(default)
10	0b RW	**AUDBUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
9	1b RW	**CPDUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function (default)
8	0b RW	**DDBMUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
7	0b RW	**DPFUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
6	0b RW	**DPIOUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
5	0b RW	**DISPLAYPORT_DPTUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
4	0b RW	**DPOUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
3	0b RW	**HDCPUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
2	0b RW	**VRDUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**VRHUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
0	0b RW	**DISPLAY_FUSE_WRAPPER_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

14.10.37 RAMCLK_GATE_D—Offset 6210h

GFX RAM Clock Gating Disable Register ([DevBLC, DevCTG, DevCDV, DevCL]) memory clock gating (cpdmmreg.v gfxramcg2)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6210h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	RESERVED
30	0	PANEL_FITTER_RAM_CLOCK_GATING_DISABLE
29	0	CURSOR_DATA_BUFFER_RAM_CLOCK_GATING_DISABLE
28	0	AUDM_UNIT_RAM_CLOCK_GATING_DISABLE
27	0	RESERVED_1
26	0	DISPLAY_DATA_BUFFER1_RAM_CLOCK_GATING_DISABLE
25	0	HDCP_UNIT_RAM_CLOCK_GATING_DISABLE
24	0	DPTUNIT_RAM_CLOCK_GATING_DISABLE
23	0	RESERVED_2
22	0	RESERVED_3
21	0	RESERVED_4
20	0	RESERVED_5
19	0	RESERVED_6
18	0	RESERVED_7
17	0	RESERVED_8
16	0	RESERVED_9
15	0	RESERVED_10
14	0	RESERVED_11
13	0	RESERVED_12
12	0	RESERVED_13
11	0	RESERVED_14
10	0	RESERVED_15
9	0	RESERVED_16
8	0	RESERVED_17
7	0	RESERVED_18
6	0	RESERVED_19
5	0	RESERVED_20
4	0	RESERVED_21
3	0	RESERVED_22
2	0	RESERVED_23
1	0	RESERVED_24
0	0	RESERVED_25

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** [DevCDV] TVOUT RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
30	0b RW	**PANEL_FITTER_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

Bit Range	Default & Access	Field Name (ID): Description
29	0b RW	**CURSOR_DATA_BUFFER_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
28	0b RW	**AUDM_UNIT_RAM_CLOCK_GATING_DISABLE:** [DevCTG, DevCDV] [DeBLC] Reserved. [DevCL] WIZ Z coeff readback return FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
27	0b RW	**RESERVED_1:** [DevCDV] [DevCTG] DPFC Unit RAM Clock Gating Disable: [DevBLC] Reserved. [DevCL] Display Data Buffer2 (Overlay) Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
26	0b RW	**DISPLAY_DATA_BUFFER1_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
25	0b RW	**HDCP_UNIT_RAM_CLOCK_GATING_DISABLE:** [DevBLC, DevCTG, DevCDV] [DevCL] ME RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
24	0b RW	**DPTUNIT_RAM_CLOCK_GATING_DISABLE:** [DevVLVP] [DevCTG, DevCDV] DPIOM Unit RAM Clock Gating Disable: [DevBLC] Reserved. [DevCL] WIZ polygon FIFO RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
23	0b RW	**RESERVED_2:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] VF RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
22	0b RW	**RESERVED_3:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] SF RAMClock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
21	0b RW	**RESERVED_4:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] WMIZ Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
20	0b RW	**RESERVED_5:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] TC FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
19	0b RW	**RESERVED_6:** [DevBLC, DevCTG, DevCDV] [DevCL] SV FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
18	0b RW	**RESERVED_7:** [DevCDV] [DevBLC] and [DevCTG] BD Unit RAM Clock Gating Disable: [DevCL] Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

Bit Range	Default & Access	Field Name (ID): Description
17	0b RW	**RESERVED_8:** [DevCDV] [DevBLC] and [DevCTG] BF Unit RAM Clock Gating Disable: [DevCL] URB Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
16	0b RW	**RESERVED_9:** [DevCDV] [DevBLC] and [DevCTG] CS Unit RAM Clock Gating Disable: [DevCL] L2 Instruction Tag RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
15	0b RW	**RESERVED_10:** [DevBLC, DevCDV] [DevCTG] FH Unit RAM Clock Gating Disable: [DevCL] Data RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
14	0b RW	**RESERVED_11:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] TAG RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
13	0b RW	**RESERVED_12:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] L2 Instruction Cache Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
12	0b RW	**RESERVED_13:** [DevCDV] [DevBLC] and [DevCTG] Reserved. [DevCL] MRFRAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
11	0b RW	**RESERVED_14:** [DevCDV] [DevBLC] and [DevCTG] VFM Unit RAM Clock Gating Disable: [DevCL] GRF RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
10	0b RW	**RESERVED_15:** [DevCDV] [DevBLC] and [DevCTG] SFM Unit RAM Clock Gating Disable: [DevCL] Data Cache CAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
9	0b RW	**RESERVED_16:** [DevCDV] [DevBLC] and [DevCTG] WIZM Unit RAM Clock Gating Disable: [DevCL] Data Cache Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
8	0b RW	**RESERVED_17:** [DevCDV] [DevBLC] and [DevCTG] URB Unit RAM Clock Gating Disable: [DevCL] Render Cache Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
7	0b RW	**RESERVED_18:** [DevCDV] [DevBLC] and [DevCTG] IC Unit RAM Clock Gating Disable: [DevCL] Render PA Tag RAM (Z) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
6	0b RW	**RESERVED_19:** [DevCDV] [DevBLC] and [DevCTG] ISC Unit RAM Clock Gating Disable: [DevCL] Render PA Tag RAM (Color) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**RESERVED_20:** [DevCDV] [DevBLC] and [DevCTG] GA Unit RAM Clock Gating Disable: [DevCL] Render Cache Write Back FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
4	0b RW	**RESERVED_21:** [DevCDV] [DevBLC] and [DevCTG] MS Unit RAM Clock Gating Disable: [DevCL] Render Cache (Z) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
3	0b RW	**RESERVED_22:** [DevCDV] [DevBLC] and [DevCTG] RCBP Unit RAM Clock Gating Disable: [DevCL] Render Cache (color) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
2	0b RW	**RESERVED_23:** [DevCDV] [DevBLC] and [DevCTG] RCC Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Cache CAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
1	0b RW	**RESERVED_24:** [DevCDV] [DevBLC] and [DevCTG] RCZ Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Tag RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
0	0b RW	**RESERVED_25:** [DevCDV] [DevBLC] and [DevCTG] MT Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Cache Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

14.10.38 FW_BLC_SELF—Offset 6500h

Display FIFO Watermark

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6500h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bit 15	Bits 14:0
RESERVED	CSPWRDWNEN	RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15	0b RW	**CSPWRDWNEN:** 1 = Dispaly FIFO can go into max_fifo configuration if only one plane A/B is enabled and all other planes, including overlay, are off. 0 = Dont put display FIFO in max_fifo configuration
14:0	0b RW	**RESERVED_1:** Reserved.

14.10.39 MI_ARB—Offset 6504h

Display Arbiter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6504h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RESERVED (bits 31:3), DISPLAY_TRICKLE_FEED_DISABLE (bit 2), RESERVED_1 (bits 1:0)

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**RESERVED:** Reserved.
2	0b RW	**DISPLAY_TRICKLE_FEED_DISABLE:** 1 Disable (Turn off trickle feed Display request). 0 Enable (Default)
1:0	0b RW	**RESERVED_1:** Reserved.

14.10.40 CZCLK_CDCLK_FREQ_RATIO—Offset 6508h

Display CZCLK/CDCLK FREQ Ratio for RMBUS sync

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6508h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000077h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1

Bits 31:9	Bits 8:4	Bits 3:0
RESERVED	DISPLAY_CDCLK_FREQUENCY_ENCODING	CORE_CLOCK_CZCLK_FREQUENCY_ENCODING

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RO	**RESERVED:** Reserved.

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>8:4</td><td>00111b
RO</td><td>DISPLAY_CDCLK_FREQUENCY_ENCODING: DISPLAY CDCLK FREQUENCY ENCODING (* symbol frequencies are POR)
|____|
=====CDCLK FREQ.======	===CDCLK DEVIDE RATIO===	==CD REGISTER ENCODING==	===SKU200==	===SKU266====	====SKU333===	====CD======
=====ENCODING========	=======================	=======(DECIMAL)========	===VCO 800=	===VCO 1600==	====VCO 2000=	===QUAL GEN=
=====================	=======================	========================	====(MHz)==	===(MHz)=====	=====(MHz)===	====RATIO===
____
======5'b00001========	===========1============	===========1============	=====800===	====1600=====	====2000=====	======1=====
____
======5'b00010========	=========1.5============	===========2============	=====533===	====1067=====	====1333=====	======2=====
____
======5'b00011========	===========2============	===========3============	=====400===	=====800=====	====1000=====	======3=====
____
======5'b00100========	=========2.5============	===========4============	=====320*==	=====640=====	=====800=====	======4=====
____
======5'b00101========	===========3============	===========5============	=====267*==	=====533=====	=====667=====	======5=====
____
======5'b00111========	===========4============	===========6============	=====200*==	=====400=====	=====500=====	======7=====
____
======5'b01000========	=========4.5============	===========7============	=====178===	=====356=====	=====444=====	======8=====
____
======5'b01001========	===========5============	===========9============	=====160===	=====320*====	=====400=====	======9=====
____
======5'b01011========	===========6============	==========11============	=====133===	=====267*====	=====300*====	=====11=====
____
======5'b01110========	=========7.5============	==========14============	=====107===	=====213=====	=====267*====	=====14=====
____
======5'b01111========	===========8============	==========15============	=====100===	=====200*====	=====250=====	=====15=====
____
======5'b10001========	===========9============	==========17============	======89===	=====178=====	=====222=====	=====17=====
____
======5'b10011========	==========10============	==========19============	======80===	=====160=====	=====200*====	=====19=====
____
======5'b10111========	==========12============	==========23============	======67===	=====133=====	=====167=====	=====23=====
____
======5'b11101========	==========15============	==========29============	======53===	=====107=====	=====133=====	=====29=====
____
======5'b11111========	==========16============	==========31============	======50===	=====100=====	=====125=====	=====31=====
____	</td></tr>
</table>

<table>
<tr><th>Bit Range</th><th>Default & Access</th><th>Field Name (ID): Description</th></tr>
<tr><td>3:0</td><td>0111b
RO</td><td>CORE_CLOCK_CZCLK_FREQUENCY_ENCODING: CORE CLOCK (CZCLK) FREQUENCY ENCODING (* synbol are POR freq for each SKU)
|____|
=====CZCLK FREQ.======	===CZCLK DEVIDE RATIO===	==CZ REGISTER ENCODING==	===SKU200==	===SKU266====	====SKU333===	====CZ======
=====ENCODING=========	=======================	=======(DECIMAL)========	===VCO 800=	===VCO 1600==	====VCO 2000=	===QUAL GEN=
=====================	=======================	=========================	====(MHz)==	===(MHz)=====	=====(MHz)===	====RATIO===
____
======5'b00001========	===========1============	===========1============	=====800===	====1600=====	====2000=====	======1=====
____
======5'b00010========	=========1.5============	===========2============	=====533===	====1067=====	====1333=====	======2=====
____
======5'b00011========	===========2============	===========3============	=====400===	=====800=====	====1000=====	======3=====
____
======5'b00100========	=========2.5============	===========4============	=====320===	=====640=====	=====800=====	======4=====
____
======5'b00101========	===========3============	===========5============	=====267===	=====533=====	=====667=====	======5=====
____
======5'b00111========	===========4============	===========6============	=====200*==	=====400=====	=====500=====	======7=====
____
======5'b01000========	=========4.5============	===========7============	=====178===	=====356=====	=====444=====	======8=====
____
======5'b01001========	===========5============	===========9============	=====160===	=====320=====	=====400=====	======9=====
____
======5'b01011========	===========6============	==========11============	=====133===	=====267*====	=====333*====	=====11=====
____
======5'b01110========	=========7.5============	==========14============	=====107===	=====213=====	=====267=====	=====14=====
____
======5'b01111========	===========8============	==========15============	=====100===	=====200*====	=====250=====	=====15=====
____	</td></tr>
</table>

14.10.41 GCI_CONTROL—Offset 650Ch

GCI Control Register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 650Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00004000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:28	PFI_CREDIT_INFO_TO_BE_SENT_TO_PONDICHERRY_PFI
27	FORCE_PFI_CREDIT_RESEND_TO_SSA
26:25	RESERVED
24	AES_CLK_GATING_DISABLE
23:15	RESERVED_1
14	VGA_FAST_MODE_DISABLE
13:4	REQUEST_LATENCY_OVERRIDE
3	REQUEST_LATENCY_OVERRIDE_ENABLE
2	AES_DECRYPTION_BYPASS_ENABLE
1	FORCE_AES_SESSION_KEYS_RESEND_TO_AES_BLOCK
0	HP_ARBITRATION_MODE

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**PFI_CREDIT_INFO_TO_BE_SENT_TO_PONDICHERRY_PFI:** Others = reserved 0111 = 15 credits 0110 = 14 credits 0101 = 13 credits 0100 = 12 credits 0011 = 11 credits 0010 = 10 credits 0001 = 9 credits 0000 = 8 credits available to PND (default) Based on the czclk/cdclk ratio, display driver has to determine the appropriate PFI credits to be used
27	0b RW	**FORCE PFI CREDIT RESEND TO SSA (FORCE_PFI_CREDIT_RESEND_TO_SSA):** 0 = Disable PFI credit to resend to SSA. Hardware is responsible to clear this bit after the PFI credit initialization request is sent. 1 = Enable PFI credit to resend to SSA. When driver sets this bit, Display PFI request engine will resend the new PFI credit bit [31:28] to SSA. Hardware is responsible to clear this bit after the PFI credit initialization request is sent.
26:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**AES_CLK_GATING_DISABLE:** 0 = Enable clock gating for AES clock (default) 1 = Disable clock gating for AES clock
23:15	0b RW	**RESERVED_1:** Reserved.
14	1b RW	**VGA_FAST_MODE_DISABLE:** 0 = Fast Mode enabled. The Gfx mem arbiter can accept a vga display read request every clock. Note that the HP Address (G_HP_CONTROL[28:24]) and ID (G_HP_CONTROL[21:16]) FIFO depths must be set to a value greater than 1 when Fast Mode is enabled. 1 = Fast Mode disabled. (default) The Gfx mem arbiter can accept a vga display read request every other clock Programming note: VGA FAST MODE is not supported in VLVP.

Bit Range	Default & Access	Field Name (ID): Description
13:4	0b RW	**REQUEST_LATENCY_OVERRIDE:** If bit 3 of this register is set, the 10-btt Request Latency Override value programmed here is used as the latency offset from the global timer for requests that win arbitration. If bit 3 is not set, normal request latency from streamers is used. Programming note: This value should not be larger than the actual required request latency. Otherwise, it will cause underrun. The guidline is to use latency corresponds to low watermark level or even smaller. When this field is used, the actual request latency is defeatured, either zero or a small value is used but still not causing underrun.
3	0b RW	**REQUEST_LATENCY_OVERRIDE_ENABLE:** 1 = Request Latency Override values in bit[13:4] is used as the latency offset from global timer 0 = Request Latency Override values is disabled. Normal request latency from streamer is used. (default)
2	0b RW	**AES_DECRYPTION_BYPASS_ENABLE:** 0 = AES decryption engine is enabled (Default) 1 = AES decryption engine is bypassed
1	0b RW	**FORCE_AES_SESSION_KEYS_RESEND_TO_AES_BLOCK:** 0 = Disable sending AES session keys to AES when going from Panel Self Refresh (PSR) inactive to PSR active mode (Default). Hardware is responsible to clear this bit after this bit is set to resend the session keys. 1 = Enable sending AES session keys to AES engine when going from PSR inactive to PSR active mode. When driver sets this bit, PAVP engine will resend the session keys to AES engine. Hardware is responsible to clear this bit after the session keys are sent.
0	0b RW	**HP_ARBITRATION_MODE:** 0 = Select hierarchical arbiter 1 = Select backup round robin arbiter

14.10.42 GMBUSFREQ—Offset 6510h

GMBUS frequency binary encoding GMBUS Frequency Binary Encoding Register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6510h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 000000A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits 31:10	Bits 9:0
RESERVED_	CMBUS_CDCLK_FREQUENCY_CDFREQ

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**RESERVED_:** Reserved.
9:0	001010000 0b RW	**CMBUS_CDCLK_FREQUENCY_CDFREQ:** Programmng note: bit[9:2] should be programmed to the number of cdclk that generates 4MHz reference clock freq which is used to generate GMBus clock. This will vary with the cdclk freq. Programming note: For hot plug detect on exact 100ms as long pulse, driver shall program [9:0] = cdclk_1.01

14.10.43 DPALETTE_A—Offset A000h

Pipe A Display Palette

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + A000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:24	23:16	15:8	7:0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	RESERVED	PIPE_A_RED_PALETTE_ENTRY	PIPE_A_GREEN_PALETTE_ENTRY	PIPE_A_BLUE_PALETTE_ENTRY

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** (read only).
23:16	0b RW	**PIPE_A_RED_PALETTE_ENTRY:** 8-bit entries per red color channel in the palette
15:8	0b RW	**PIPE_A_GREEN_PALETTE_ENTRY:** 8-bit entries per green color channel in the palette
7:0	0b RW	**PIPE_A_BLUE_PALETTE_ENTRY:** 8-bit entries per blue color channel in the palette

14.10.44 DPALETTE_B—Offset A800h

Pipe B Display Palette

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + A800h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
RESERVED	PIPE_B_RED_PALETTE_ENTRY	PIPE_B_GREEN_PALETTE_ENTRY	PIPE_B_BLUE_PALETTE_ENTRY

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Read Only.
23:16	0b RW	**PIPE_B_RED_PALETTE_ENTRY:** 8-bit entries per red color channel in the palette
15:8	0b RW	**PIPE_B_GREEN_PALETTE_ENTRY:** 8-bit entries per green color channel in the palette
7:0	0b RW	**PIPE_B_BLUE_PALETTE_ENTRY:** 8-bit entries per blue color channel in the palette

14.10.45 MIPIA_DEVICE_READY_REG—Offset B000h

MIPI A Device Ready Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits 31:4	Bit 3	Bits 2:1	Bit 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0
RESERVED	BUS_POSSESSION	ULPS_STATE	DEVICE_READY_

Bit Range	Default & Access	Field Name (ID): Description
31:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**BUS_POSSESSION:** BUS possession for mipiA
2:1	0b RW	**ULPS_STATE:** ULPS state for mipi pipe A
0	0b RW	**DEVICE_READY_:** Set by the processor to inform that device is ready

14.10.46 MIPIA_INTR_STAT_REG—Offset B004h

interrupt stat reg for mipi pipe A

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TEARING_EFFECT	SPL_PKT_SENT_INTERRUPT	GEN_READ_DATA_AVAIL	LP_GENERIC_WR_FIFO_FULL	HS_GENERIC_WR_FIFO_FULL	RX_PROT_VIOLATION	RX_INVALID_TX_LENGTH	ACK_WITH_NO_ERROR	TURN_AROUND_ACK_TIMEOUT	LP_RX_TIMEOUT	HS_TX_TIMEOUT	DPI_FIFO_UNDERRUN	LOW_CONTENTION	HIGH_CONTENTION	TXDSI_VC_ID_INVALID	TXDSI_DATA_TYPE_NOT_RECOGNISED	TXCHECKSUM_ERROR	TXECC_MULTIBIT_ERROR	TXECC_SINGLE_BIT_ERROR	TXFALSE_CONTROL_ERROR	RXDSI_VC_ID_INVALID	RXDSI_DATA_TYPE_NOT_RECOGNISED	RXCHECKSUM_ERROR	RXECC_MULTIBIT_ERROR	RXECC_SINGLE_BIT_ERROR	RXFALSE_CONTROL_ERROR	RXHS_RECEIVE_TIMEOUT_ERROR	RX_LP_TX_SYNC_ERROR	RXESCAPE_MODE_ENTRY_ERROR	RXEOTSYNCERROR	RXSOTSYNCERROR	RXSOTERROR

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**TEARING_EFFECT:** Set to indicate that tearing effect trigger message is Received
30	0b RW	**SPL_PKT_SENT_INTERRUPT:** Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0b RW	**GEN_READ_DATA_AVAIL:** Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
28	0b RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full

Bit Range	Default & Access	Field Name (ID): Description
27	0b RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0b RW	**RX_PROT_VIOLATION:** Set if DSI protocol violation error is reported in the acknowledge packet by the display device
25	0b RW	**RX_INVALID_TX_LENGTH:** Set if invalid transmission length error is reported in the acknowledge packet by the display device
24	0b RW	**ACK_WITH_NO_ERROR:** Set if acknowledge trigger message is received with out any error
23	0b RW	**TURN_AROUND_ACK_TIMEOUT:** Set if a turn around acknowledgement sequence is not received from the display device
22	0b RW	**LP_RX_TIMEOUT:** Set if a low power reception count expires this interrupt is generated
21	0b RW	**HS_TX_TIMEOUT:** Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
20	0b RW	**DPI_FIFO_UNDERRUN:** Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0b RW	**LOW_CONTENTION:** Set to '1' if a LP low fault is registered by at the D-PHY contention detector
18	0b RW	**HIGH_CONTENTION:** Set to '1' if a LP high fault is registered by at the D-PHY contention detector
17	0b RW	**TXDSI_VC_ID_INVALID:** Set to '1' if the received virtual channel ID is invalid
16	0b RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the received data type is not recognised
15	0b RW	**TXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value during the reception of packets by Arasan_DSI host.
14	0b RW	**TXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
13	0b RW	**TXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
12	0b RW	**TXFALSE_CONTROL_ERROR:** Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host
11	0b RW	**RXDSI_VC_ID_INVALID:** Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
10	0b RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the data type is not recognised by the display device is reported in the Acknowledge packet by the display device
9	0b RW	**RXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value and is reported in the Acknowledge packet by the display device
8	0b RW	**RXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
7	0b RW	**RXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
6	0b RW	**RXFALSE_CONTROL_ERROR:** Set to '1' if a control error is reported in the Acknowledge packet by the display device

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
4	0b RW	**RX_LP_TX_SYNC_ERROR:** Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device
3	0b RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
2	0b RW	**RXEOTSYNCERROR:** RX eot sync Error
1	0b RW	**RXSOTSYNCERROR:** Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
0	0b RW	**RXSOTERROR:** Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

14.10.47 MIPIA_INTR_EN_REG—Offset B008h

mipi pipe A interrupt enable register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	RESERVED
30	0	SPL_PKT_SENT_INTERRUPT
29	0	GEN_READ_DATA_AVAIL
28	0	LP_GENERIC_WR_FIFO_FULL
27	0	HS_GENERIC_WR_FIFO_FULL
26	0	RX_PROT_VIOLATION
25	0	RX_INVALID_TX_LENGTH
24	0	ACK_WITH_NO_ERROR
23	0	TURN_AROUND_ACK_TIMEOUT
22	0	LP_RX_TIMEOUT
21	0	HS_TX_TIMEOUT
20	0	DPI_FIFO_UNDERRUN
19	0	LOW_CONTENTION
18	0	HIGH_CONTENTION
17	0	TXDSI_VC_ID_INVALID
16	0	TXDSI_DATA_TYPE_NOT_RECOGNISED
15	0	TXCHECKSUM_ERROR
14	0	TXECC_MULTIBIT_ERROR
13	0	TXECC_SINGLE_BIT_ERROR
12	0	TXFALSE_CONTROL_ERROR
11	0	RXDSI_VC_ID_INVALID
10	0	RXDSI_DATA_TYPE_NOT_RECOGNISED
9	0	RXCHECKSUM_ERROR
8	0	RXECC_MULTIBIT_ERROR
7	0	RXECC_SINGLE_BIT_ERROR
6	0	RXFALSE_CONTROL_ERROR
5	0	RXHS_RECEIVE_TIMEOUT_ERROR
4	0	RX_LP_TX_SYNC_ERROR
3	0	RXESCAPE_MODE_ENTRY_ERROR
2	0	RXEOTSYNC_ERROR
1	0	RXSOTSYNC_ERROR
0	0	RXSOT_ERROR

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**TEARING_EFFECT (RESERVED):** set to enable tearing effect interrupt.
30	0b RW	**SPL_PKT_SENT_INTERRUPT:** Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register

Bit Range	Default & Access	Field Name (ID): Description
29	0b RW	**GEN_READ_DATA_AVAIL:** Set to enable Generic Read available interrupt
28	0b RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0b RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0b RW	**RX_PROT_VIOLATION:** Set to enable protocol violation error
25	0b RW	**RX_INVALID_TX_LENGTH:** Set to enable invalid transmission length error
24	0b RW	**ACK_WITH_NO_ERROR:** Set to enable acknowledge trigger message reception with out any error
23	0b RW	**TURN_AROUND_ACK_TIMEOUT:** Set to enable turn around acknowledgement ,sequence timeout
22	0b RW	**LP_RX_TIMEOUT:** Set to enable low power reception count timeouts
21	0b RW	**HS_TX_TIMEOUT:** Set to enable a high speed transmission timeout
20	0b RW	**DPI_FIFO_UNDERRUN:** Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0b RW	**LOW_CONTENTION:** Set to enable a LP low fault interrupt
18	0b RW	**HIGH_CONTENTION:** Set to enable a LP high fault interrupt
17	0b RW	**TXDSI_VC_ID_INVALID:** Set to enable the interrupt if the received packets virtual channel ID is invalid
16	0b RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt if the received packets data type is not recognised
15	0b RW	**TXCHECKSUM_ERROR:** Set to enable the interrupt if the computed CRC differs from the received CRC value for the received packets
14	0b RW	**TXECC_MULTIBIT_ERROR:** Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
13	0b RW	**TXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
12	0b RW	**TXFALSE_CONTROL_ERROR:** Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
11	0b RW	**RXDSI_VC_ID_INVALID:** Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
10	0b RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt for the un recognised data type in the acknowledgment packet reports
9	0b RW	**RXCHECKSUM_ERROR:** Set to enable the interrupt for the computed CRC differs from the received CRC value in the acknowledgment packet reports
8	0b RW	**RXECC_MULTIBIT_ERROR:** Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**RXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
6	0b RW	**RXFALSE_CONTROL_ERROR:** Set to enable the interrupt for control error in the acknowledgment packet reports
5	0b RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
4	0b RW	**RX_LP_TX_SYNC_ERROR:** Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports
3	0b RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
2	0b RW	**RXEOTSYNC_ERROR:** Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
1	0b RW	**RXSOTSYNC_ERROR:** Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports
0	0b RW	**RXSOT_ERROR:** Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

14.10.48 MIPIA_DSI_FUNC_PRG__REG—Offset B00Ch

mipi pipe A dsi function program register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B00Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields (from bit 31 to bit 0): RESERVED | SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE | RESERVED_1 | SUPPORTED_FORMAT_IN_VIDEO_MODE | CHANNEL_NUMBER_FOR_COMMAND_MODE | CHANNEL_NUMBER_FOR_VIDEO_MODE | DATA_LANES_PRG_R_EG

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:13	0b RW	**SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE:** 000 --) Reserved, 001 --) 16 bit data , 010 --) 9 bit data , 011 --) 8 bit data , 100 --) option 1 : 101 --) option 2 : 110 to 111 --) Reserved
12:11	0b RW	**RESERVED_1:** Reserved.
10:7	0b RW	**SUPPORTED_FORMAT_IN_VIDEO_MODE:** Supported colour format, 0001 --) RGB565, 0010 --) RGB666, 0011 --) RGB 666 loosely packed format, 0100 --) RGB888
6:5	0b RW	**CHANNEL_NUMBER_FOR_COMMAND_MODE:** Virtual channel number for command mode is programmed by the processor
4:3	0b RW	**CHANNEL_NUMBER_FOR_VIDEO_MODE:** Virtual channel number for command mode is programmed by the processor
2:0	001b RW	**DATA_LANES_PRG_R_EG:** Number of data lanes to be supported is programmed by the processor

14.10.49 MIPIA_HS_TX_TIMEOUT_REG—Offset B010h

mipi piepe A HS TX timout register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								HIGH_SPEED_TX_TIMEOUT_COUNTER																							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:0	0b RW	**HIGH_SPEED_TX_TIMEOUT_COUNTER:** The maximum duration allowed for the DSI host ,to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

14.10.50 MIPIA_LP_RX_TIMEOUT_REG—Offset B014h

mipi pipe A LP RX timeout register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

LOW_POWER_RECEPTION_TIMEOUT_COUNTER

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:0	0b RW	**LOW_POWER_RECEPTION_TIMEOUT_COUNTER:** Timeout value to be checked for received short packets .If the timer expires the DSI Host enters stop state

14.10.51 MIPIA_TURN_AROUND_TIMEOUT_REG—Offset B018h

mipi pipe A turn around timeout register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																										TURN_AROUND_TIMEOUT_REGISTER					

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**RESERVED:** Reserved.
5:0	0b RW	**TURN_AROUND_TIMEOUT_REGISTER:** Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

14.10.52 MIPIA_DEVICE_RESET_TIMER—Offset B01Ch

mipi pipe A device reset timer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B01Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																DEVICE_RESET_TIMER															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**DEVICE_RESET_TIMER:** Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

14.10.53 MIPIA_DPI_RESOLUTION_REG—Offset B020h

mipi piepe A DPI Resolution reg

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VERTICAL_ADDRESS																HORIZONTAL_ADDRESS															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**VERTICAL_ADDRESS:** Shows the vertical address count in lines
15:0	0b RW	**HORIZONTAL_ADDRESS:** Shows the horizontal address count in pixels

14.10.54 MIPIA_DBI_RESOLUTION_REG—Offset B024h

mipi A DBI resolution reg

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																														DBI_FIFO_THRTL	

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**RESERVED:** Reserved.
1:0	0b RW	**DBI_FIFO_THRTL:** DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached: 00 - (1/2) DBI fifo empty 01 - (1/4) DBI fifo empty 10 - 7 locations are empty 11 - Reserved

14.10.55 MIPIA_HORIZ_SYNC_PADDING_COUNT—Offset B028h

mipi A horizontal sync padding out

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																HORIZONTAL_SYNC_PADDING_COUNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0b RW	**HORIZONTAL_SYNC_PADDING_COUNT:** Shows the horizontal sync padding value in terms of txbyteclkhs

14.10.56 MIPIA_HORIZ_BACK_PORCH_COUNT—Offset B02Ch

mipi pipe A horizontal back porch counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B02Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:16) | HORIZONTAL_BACK_PORCH_COUNT (15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_BACK_PORCH_COUNT:** Shows the horizontal back porch value in terms of txbyteclkhs

14.10.57 MIPIA_HORIZ_FRONT_PORCH_COUNT—Offset B030h

mipi pipe A horizontal front porch counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B030h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																HORIZONTAL_FRONT_PORCH_COUNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_FRONT_PORCH_COUNT:** Shows the horizontal front porch value in terms of txbyteclkhs

14.10.58 MIPIA_HORIZ_ACTIVE_AREA_COUNT—Offset B034h

mipi A horizontal active area counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B034h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																HORIZONTAL_ACTIVE_AREA_COUNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_ACTIVE_AREA_COUNT:** Shows the horizontal active area value in terms of txbyteclkhs

14.10.59 MIPIA_VERT_SYNC_PADDING_COUNT—Offset B038h

mipi pipe A vertical sync padding counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B038h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																VERTICAL_SYNC_PADDING_COUNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_SYNC_PADDING_COUNT:** Shows the vertical sync padding value in terms of lines

14.10.60 MIPIA_VERT_BACK_PORCH_COUNT—Offset B03Ch

mipi pipe A vertical back portch counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B03Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
RESERVED	VERTICAL_BACK_PORCH_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_BACK_PORCH_COUNT:** Shows the vertical back porch value in terms of lines

14.10.61 MIPIA_VERT_FRONT_PORCH_COUNT—Offset B040h

mipi pipe A vertical front portch counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
RESERVED	VERTICAL_FRONT_PORCH_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0b RW	**VERTICAL_FRONT_PORCH_COUNT:** Shows the vertical front porch value in terms of lines

14.10.62 MIPIA_HIGH_LOW_SWITCH_COUNT—Offset B044h

mipi A high low switch count

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED (31:16)																HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT (15:0)															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

Bit Range	Default & Access	Field Name (ID): Description
15:0	0b RW	**HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

14.10.63 MIPIA_DPI_CTRL_REG—Offset B048h

mipi A dpi ctrl register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
Field	RESERVED	RSTTRG	HS_LP	BACK_LIGHT_OFF	BACK_LIGHT_ON	COLOR_MODE_OFF	COLOR_MODE_ON	TURN_ON	SHUT_DOWN

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:**
7	0b RW	**RSTTRG:** mipi A dpi ctrl reg RSTTRG
6	0b RW	**HS_LP:** Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode
5	0b RW	**BACK_LIGHT_OFF:** Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel
4	0b RW	**BACK_LIGHT_ON:** Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
3	0b RW	**COLOR_MODE_OFF:** Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
2	0b RW	**COLOR_MODE_ON:** Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
1	0b RW	**TURN_ON:** Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
0	0b RW	**SHUT_DOWN:** Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

14.10.64 MIPIA_DPI_DATA_REGISTER—Offset B04Ch

mipi A dpi data register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B04Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (bits 31:6), COMMAND_BYTE (bits 5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**RESERVED:** Reserved.
5:0	0b RW	**COMMAND_BYTE:** Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

14.10.65 MIPIA_INIT_COUNT_REGISTER—Offset B050h

mipi A init count register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (bits 31:16), MASTER_INIT_TIMER (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**MASTER_INIT_TIMER:** Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

14.10.66 MIPIA_MAX_RETURN_PKT_SIZE_REGISTER—Offset B054h

mipi A max resturn pkt size register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | MAX_RETURN_PKT_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**RESERVED:** Reserved.
9:0	0b RW	**MAX_RETURN_PKT_SIZE:** Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

14.10.67 MIPIA_VIDEO_MODE_FORMAT_REGISTER—Offset B058h

mipi A video mode format register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B058h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:5), RANDOM_DPI_DISPLAY_RESOLUTION_DEFEATURE (4), MIPIA_DISABLE_VIDEO_BTA (3), IP_TG_CONFIG (2), VIDEO_MODE_FMT (1:0)

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RW	**RESERVED:** Reserved.
4	0b RW	**RANDOM_DPI_DISPLAY_RESOLUTION_DEFEATURE:** Set by the processor to support random DPI display resolution 0 - random DPI display resolution support disabled. 1 - random DPI display resolution support enabled.
3	0b RW	**MIPIA_DISABLE_VIDEO_BTA:** Set by the processor to inform the DSI controller to disable the BTA sent at the last blanking line of VFP. By default, this bit is set to 0.0 BTA sending at the last blanking line of VFP is enabled. 1 BTA sentding at teh last blanking line of VFP is disabeld.
2	0b RW	**IP_TG_CONFIG:** Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0. 0 - After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted. 1 - After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP
1:0	0b RW	**VIDEO_MODE_FMT:** Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. 00 Reserved 01 - Non Burst Mode with Sync Pulse 10 - Non Burst Mode with Sync events 11 - Burst Mode

14.10.68 MIPIA_EOT_DISABLE_REGISTER—Offset B05Ch

mipi A eot disable register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B05Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
Field	RESERVED	LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE	HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE	LOW_CONTENTION_RECOVERY_DISABLE	HIGH_CONTENTION_RECOVERY_DISABLE	TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE	TXECC_MULTIBIT_ERR_RECOVERY_DISABLE	CLOCKSTOP	EOT_DIS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** Reserved.
7	0b RW	**LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt. 0 - LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt. 1 - If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx contorller. LP Rx timeout error interrupt will act as an informative interrupt
6	0b RW	**HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt. 0 - HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt. 1 - If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx contorller. HS Tx timeout error interrupt will act as an informative interrupt

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**LOW_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt. 0 - Contention recovery will happen if the processor clears Low contention interrupt. 1 - If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Low contention interrupt will act as an informative interrupt
4	0b RW	**HIGH_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt. 0 - Contention recovery will happen if the processor clears High contention interrupt. 1 - If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG
3	0b RW	**TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognised error interrupt is cleared by the processor. 0 - Error recovery action will be taken if TxDSI data type not recognised error interrupt is cleared by the processor. 1 - If TxDSI data type not recognised error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt
2	0b RW	**TXECC_MULTIBIT_ERR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor. 0 - Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor. 1 - If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt
1	0b RW	**CLOCKSTOP:** Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0. 0 - clock stopping disabled 1 - clock stopping enabled
0	0b RW	**EOT_DIS:** Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward comapatibility of earlier DSI systems, EOT short packet transmission can be disabled. 0 - EOT short packet transmission enabled 1 - EOT short packet transmission disabled

14.10.69 MIPIA_LP_BYTECLK_REGISTER—Offset B060h

mipi A LP bytclk register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED				LP_BYTECLK			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**LP_BYTECLK:** Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

14.10.70 MIPIA_LP_GEN_DATA_REGISTER—Offset B064h

mipi A LP gen DATA register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
LP_GEN_DATA							

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**LP_GEN_DATA:** Data port register used for generic data transfers in low power mode

14.10.71 MIPIA_HS_GEN_DATA_REGISTER—Offset B068h

mipi A HS GEN data register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HS_GEN_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**HS_GEN_DATA:** Data port register used for generic data transfers in low power mode

14.10.72 MIPIA_LP_GEN_CTRL_REGISTER—Offset B06Ch

mipi A LP Gen CTRL register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B06Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | WORD_COUNT | VIRTUAL_CHANNEL | DATA_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b WO	**RESERVED:** Reserved.
23:8	0b WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0b WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended

Bit Range	Default & Access	Field Name (ID): Description
5:0	0b WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write , one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

14.10.73 MIPIA_HS_GEN_CTRL_REGISTER—Offset B070h

mipi A HS GEN CTRL register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B070h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | WORD_COUNT | VIRTUAL_CHANNEL | DATA_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b WO	**RESERVED:** Reserved.
23:8	0b WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0b WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended
5:0	0b WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

14.10.74 MIPIA_GEN_FIFO_STAT_REGISTER—Offset B074h

mipi A gen fifo stat register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B074h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 1E060606h

Bits	31:29	28	27	26	25	24	23:19	18	17	16	15:11	10	9	8	7:3	2	1	0
Default	0 0 0	1	1	1	1	0	0 0 0 0 0	1	1	0	0 0 0 0 0	1	1	0	0 0 0 0 0	1	1	0
Field	RESERVED	DPI_FIFO_EMPTY	DBI_FIFO_EMPTY	LP_CTRL_FIFO_EMPTY	LP_CTRL_FIFO_HALF_EMPTY	LP_CTRL_FIFO_FULL	RESERVED_1	HS_CTRL_FIFO_EMPTY	HS_CTRL_FIFO_HALF_EMPTY	HS_CTRL_FIFO_FULL	RESERVED_2	LP_DATA_FIFO_EMPTY	LP_DATA_FIFO_HALF_EMPTY	LP_DATA_FIFO_FULL	RESERVED_3	HS_DATA_FIFO_EMPTY	HS_DATA_FIFO_HALF_EMPTY	HS_DATA_FIFO_FULL

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RO	**RESERVED:** Reserved.
28	1b RO	**DPI_FIFO_EMPTY:** Default 1
27	1b RO	**DBI_FIFO_EMPTY:** Default 1
26	1b RO	**LP_CTRL_FIFO_EMPTY:** Default 1
25	1b RO	**LP_CTRL_FIFO_HALF_EMPTY:** Default 1
24	0b RO	**LP_CTRL_FIFO_FULL:** Default 0
23:19	0b RO	**RESERVED_1:** Reserved.
18	1b RO	**HS_CTRL_FIFO_EMPTY:** Default 1
17	1b RO	**HS_CTRL_FIFO_HALF_EMPTY:** Default 1
16	0b RO	**HS_CTRL_FIFO_FULL:** Default 0
15:11	0b RO	**RESERVED_2:** Reserved.
10	1b RO	**LP_DATA_FIFO_EMPTY:** Default 1

Bit Range	Default & Access	Field Name (ID): Description
9	1b RO	**LP_DATA_FIFO_HALF_EMPTY:** Default 1
8	0b RO	**LP_DATA_FIFO_FULL:** Default 0
7:3	0b RO	**RESERVED_3:** Reserved.
2	1b RO	**HS_DATA_FIFO_EMPTY:** Default 1
1	1b RO	**HS_DATA_FIFO_HALF_EMPTY:** Default 1
0	0b RO	**HS_DATA_FIFO_FULL:** Default 0

14.10.75 MIPIA_HS_LS_DBI_ENABLE_REG—Offset B078h

Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B078h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

DBI_HS_LS_SWITCH_RE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**RESERVED:** Reserved.
0	0b RW	**DBI_HS_LS_SWITCH_RE:** Set to 1 if DBI packets have to be transmitted in Low power mode Set to 0 if DBI packets have to be transmitted in High speed mode

14.10.76 MIPIA_RESERVED—Offset B07Ch

Reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B07Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RESERVED:** Reserved.

14.10.77 MIPIA_DPHY_PARAM_REG—Offset B080h

mipi A dphy parameter register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0B061A04h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	0	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0

RESERVED	EXIT_ZERO_COUNT	RESERVED_1	TRAIL_COUNT	CLK_ZERO_COUNT	RESERVED_2	PREPARE_COUNT
31:30	29:24	23:21	20:16	15:8	7:6	5:0

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** Reserved.
29:24	001011b RW	**EXIT_ZERO_COUNT:** THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
23:21	0b RW	**RESERVED_1:** Reserved.
20:16	00110b RW	**TRAIL_COUNT:** TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor

Bit Range	Default & Access	Field Name (ID): Description
15:8	00011010b RW	**CLK_ZERO_COUNT:** TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor
7:6	0b RW	**RESERVED_2:** Reserved.
5:0	000100b RW	**PREPARE_COUNT:** TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

14.10.78 MIPIA_DBI_BW_CTRL_REG—Offset B084h

mipi A DBI BW ctrl register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B084h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BANDWIDTH_TIMER

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**BANDWIDTH_TIMER:** DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies. Note: The value programmed in this timer must be greater than the actual time taken to carryout 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

14.10.79 MIPIA_CLK_LANE_SWITCHING_TIME_CNT—Offset B088h

mipi A clk clane switching time counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B088h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LS_HS_SSW_CNT																HS_LS_PWR_SW_CNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**LS_HS_SSW_CNT:** Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	0b RW	**HS_LS_PWR_SW_CNT:** High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

14.10.80 MIPIA_STOP_STATE_STALL—Offset B08Ch

mipi A stop state stall

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B08Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																								MIPIA_STOP_STATE_STALL_COUNTER							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** reserved
7:0	0b RW	**MIPIA_STOP_STATE_STALL_COUNTER:** Delay between (stall the stop state signal) the data transfer is increased based on this counter value. This counter is calculated from txclkesc. Note: If processor programs this register then it needs to reprogram the high_low_ switch counter in B044h and lp_equivalent_byteclk reg in B060h to compensate this delay. High_low_switch_count B044h: High to low switch counter = Actual High to low switch + stop_sta_stall_reg value * Low power clock equivalence value in terms of byte clock LP equivalent byteclk register B060h: LP equivalent byteclk value = txclkesc time/ txbyteclk time * (105 + stop_sta_stall_reg value) / 105 Minimum time of Low Power short packet transfer = 105 txclkesc

14.10.81 MIPIA_INTR_STAT_REG_1—Offset B090h

mipi A interrupt state register 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B090h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:1), MIPIA_RX_CONNECTION_DETECTED (0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**RESERVED:** reserved
0	0b RW	**MIPIA_RX_CONNECTION_DETECTED:** Set to 1'b1 if the contention detected in the display device and is reported in the Acknowledge packet by the display device

14.10.82 MIPIA_INTR_EN_REG_1—Offset B094h

mipi A interrupt enable register 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [GTTMMADR_LSB + 180000h] + B094h
	GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
	GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:1) | MIPIA_ENABLE_RX_CONNECTION_DETECTED (0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**RESERVED:** reserved
0	0b RW	**MIPIA_ENABLE_RX_CONNECTION_DETECTED:** Set to enable the interrupt for contention detected error in the acknowledgement packet reports

14.10.83 MIPIA_DBI_TYPEC_CTRL—Offset B100h

mipi A Dbit typeC ctrl

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [GTTMMADR_LSB + 180000h] + B100h
	GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
	GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VAL	STATUS	OPTION		FREQ				RESERVED															OVERRIDE	OVERRIDE_COUNTER							

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**VAL:** 0= disable DBI TYPE-C interface (default) 1= enable DBI TYPE-C interface Driver to make sure that the command and data buffers are cleared before this bit is changed
30	0b RW	**STATUS:** command and data buffer empty and link completed sending out all serialized data and IDLE 0 = IDLE 1 = work in progress
29:28	0b RW	**OPTION:** TYPE-C option selection 00 option 1 01 option 2 10 option 3 11 no defined functionality
27:24	0b RW	**FREQ:** Type-C clock frequency ; A counter based onczclk is used to generate the TYPE-C Clock. So based on the czclk, a frequency close to the specified below will be generated. Not the exact frequency. 0000 1Mhz (default) 0001 1Mhz 0010 2Mhz 1111 15Mhz
23:9	0b RW	**RESERVED:** Reserved.
8	0b RW	**OVERRIDE:** Use override counter value to derive the TYPE-C clock frequency
7:0	0b RW	**OVERRIDE_COUNTER:** Override counter value to generate the TYPE-C clock

14.10.84 MIPIA_CTRL—Offset B104h

MIPI adapter has a control register with options to control width of the dbi bus and the divide value of the clock that needs to be supplied to the Clocks module so that a 2x divided clock can be provided to the MIPI D-PHY IP. Self refresh capability is in DCS commands. The other 3 controls bits (SD, CM and back light control) are now moved to MIPI IP registers.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B104h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NAME_BITS | ESCAPE_CLOCK_DIVIDER | STATUS | RGB_FLIP | MIPI_2X_CLOCK_DIVIDER

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**NAME_BITS:** Reserved
6:5	0b RW	**ESCAPE_CLOCK_DIVIDER:** Read Only Escape clock divider select for Pipe A and Pipe C Escape clock is shared by both Pipe A and Pipe C so it cant be set different. 00= 1 X (20 Mhz) (default) 01= X (10Mhz) 10= X (5Mhz) Changing this register can only be done when the MIPI device_ready is turned OFF
4:3	0b RW	**STATUS:** 2'b00: low priority on read requests to G-unit 2'b11 : high priority
2	0b RW	**RGB_FLIP:** 1'b0 : RGB data from disp2d is reverted to BGR 1'b1 : RGB data from disp2d is passed as is to MIPI IP
1:0	0b RW	**MIPI_2X_CLOCK_DIVIDER:** Reserved

14.10.85 MIPIA_DATA_ADD—Offset B108h

mipi A data ADD

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B108h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA_MEM_ADDR | DATA_MEM_ADDR_1 | DATA_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RW	**DATA_MEM_ADDR:** When there is updated data for the display panel, S/W programs this register with the memory address to read from
4:1	0b RW	**DATA_MEM_ADDR_1:** Reserved
0	0b RW	**DATA_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.10.86 MIPIA_DATA_LEN—Offset B10Ch

mipiA data length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B10Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:20	19:0
RESERVED	DATA_LENGTH

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**DATA_LENGTH:** This field shows the remaining length of data that needs to be read from memory, Initially set by S/W and is decremented by H/W as reads are issued

14.10.87 MIPIA_CMD_ADD—Offset B110h

mipi A cmd ADD

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

COMMAND_MEM_ADDR	RESERVED	MIPIA_AUTO_PWG_ENABLE	COMMAND_DATA_MODE	COMMAND_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RW	**COMMAND_MEM_ADDR:** When there are new commands that need to be sent to the display panel, S/W programs this register with the memory address to read the commands from
4:3	0b RW	**RESERVED:** MBZ
2	0b RW	**MIPIA_AUTO_PWG_ENABLE:** Idle state: SW driver writes to this bit to enable auto power gating for MIPIA controller 0: default 1: auto power gate is enabled
1	0b RW	**COMMAND_DATA_MODE:** 0: data for memory write command from system buffer that is specified by MIPI data address register 1: data for memory write command from pipe A rendering
0	0b RW	**COMMAND_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.10.88 MIPIA_CMD_LEN—Offset B114h

mipi A clm length

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B114h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

COMMAND_3	COMMAND_2	COMMAND_1	COMMAND_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**COMMAND_3:** This is command 3 length (command + parameters) in bytes

Bit Range	Default & Access	Field Name (ID): Description
23:16	0b RW	**COMMAND_2:** This is command 2 length (command + parameters) in bytes
15:8	0b RW	**COMMAND_1:** This is command 1 length (command + parameters) in bytes
7:0	0b RW	**COMMAND_0:** This is command 0 length (command + parameters) in bytes

14.10.89 MIPIA_RD_DATA_RETURN0—Offset B118h

In addition to the command and data registers, adapter provides 8 read only registers for S/W to read the return data from the panel. At this time the usage case for the read path from the panel is for configuration reads only. Hence, more than 4 bytes of read are not allowed. Maximum read return size in the MIPI IP should be no greater than 32 bytes.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B118h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.90 MIPIA_RD_DATA_RETURN1—Offset B11Ch

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B11Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.91 MIPIA_RD_DATA_RETURN2—Offset B120h

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B120h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.92 MIPIA_RD_DATA_RETURN3—Offset B124h

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B124h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.93 MIPIA_RD_DATA_RETURN4—Offset B128h

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B128h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.94 MIPIA_RD_DATA_RETURN5—Offset B12Ch

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B12Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.95 MIPIA_RD_DATA_RETURN6—Offset B130h

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B130h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.96 MIPIA_RD_DATA_RETURN7—Offset B134h

Refer to the description of MIPIA_RD_DATA_RETURN0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B134h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.97 MIPIA_RD_DATA_VALID—Offset B138h

Refer to the description of MIPIA_RD_DATA_RETURN1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B138h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | READ_DATA_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** Reserved.
7:0	0b RW	**READ_DATA_VALID:** Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. When S/W issues a write '1 to the registers, this bit is cleared

14.10.98 MIPIC_DEVICE_READY_REG—Offset B800h

MIPI C Device Ready Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B800h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | BUS_POSSESSION | ULPS_STATE | DEVICE_READY_

Bit Range	Default & Access	Field Name (ID): Description
31:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**BUS_POSSESSION:** mipi C Bus Possession
2:1	0b RW	**ULPS_STATE:** mipi C ULPS state
0	0b RW	**DEVICE_READY_:** Set by the processor to inform that device is ready

14.10.99 MIPIC_INTR_STAT_REG—Offset B804h

mipi C intrrupt state registr

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B804h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	TEARING_EFFECT
30	0	SPL_PKT_SENT_INTERRUPT
29	0	GEN_READ_DATA_AVAIL
28	0	LP_GENERIC_WR_FIFO_FULL
27	0	HS_GENERIC_WR_FIFO_FULL
26	0	RX_PROT_VIOLATION
25	0	RX_INVALID_TX_LENGTH
24	0	ACK_WITH_NO_ERROR
23	0	TURN_AROUND_ACK_TIMEOUT
22	0	LP_RX_TIMEOUT
21	0	HS_TX_TIMEOUT
20	0	DPI_FIFO_UNDERRUN
19	0	LOW_CONTENTION
18	0	HIGH_CONTENTION
17	0	TXDSI_VC_ID_INVALID
16	0	TXDSI_DATA_TYPE_NOT_RECOGNISED
15	0	TXCHECKSUM_ERROR
14	0	TXECC_MULTIBIT_ERROR
13	0	TXECC_SINGLE_BIT_ERROR
12	0	TXFALSE_CONTROL_ERROR
11	0	RXDSI_VC_ID_INVALID
10	0	RXDSI_DATA_TYPE_NOT_RECOGNISED
9	0	RXCHECKSUM_ERROR
8	0	RXECC_MULTIBIT_ERROR
7	0	RXECC_SINGLE_BIT_ERROR
6	0	RXFALSE_CONTROL_ERROR
5	0	RXHS_RECEIVE_TIMEOUT_ERROR
4	0	RX_LP_TX_SYNC_ERROR
3	0	RXESCAPE_MODE_ENTRY_ERROR
2	0	RXEOTSYNCERROR
1	0	RXSOTSYNCERROR
0	0	RXSOTERROR

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**TEARING_EFFECT:** Set to indicate that tearing effect trigger message is received
30	0b RW	**SPL_PKT_SENT_INTERRUPT:** Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0b RW	**GEN_READ_DATA_AVAIL:** Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
28	0b RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full

Bit Range	Default & Access	Field Name (ID): Description
27	0b RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0b RW	**RX_PROT_VIOLATION:** Set if DSI protocol violation error is reported in the acknowledge packet by the display device
25	0b RW	**RX_INVALID_TX_LENGTH:** Set if invalid transmission length error is reported in the acknowledge packet by the display device
24	0b RW	**ACK_WITH_NO_ERROR:** Set if acknowledge trigger message is received with out any error
23	0b RW	**TURN_AROUND_ACK_TIMEOUT:** Set if a turn around acknowledgement sequence is not received from the display device
22	0b RW	**LP_RX_TIMEOUT:** Set if a low power reception count expires this interrupt is generated
21	0b RW	**HS_TX_TIMEOUT:** Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
20	0b RW	**DPI_FIFO_UNDERRUN:** Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0b RW	**LOW_CONTENTION:** Set to '1' if a LP low fault is registered by at the D-PHY contention detector
18	0b RW	**HIGH_CONTENTION:** Set to '1' if a LP high fault is registered by at the D-PHY contention detector
17	0b RW	**TXDSI_VC_ID_INVALID:** Set to '1' if the received virtual channel ID is invalid
16	0b RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the received data type is not recognised
15	0b RW	**TXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value during the reception of packets by Arasan_DSI host.
14	0b RW	**TXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
13	0b RW	**TXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
12	0b RW	**TXFALSE_CONTROL_ERROR:** Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host
11	0b RW	**RXDSI_VC_ID_INVALID:** Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
10	0b RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the data type is not recognised by the display device is reported in the Acknowledge packet by the display device
9	0b RW	**RXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value and is reported in the Acknowledge packet by the display device
8	0b RW	**RXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
7	0b RW	**RXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
6	0b RW	**RXFALSE_CONTROL_ERROR:** Set to '1' if a control error is reported in the Acknowledge packet by the display device

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
4	0b RW	**RX_LP_TX_SYNC_ERROR:** Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device
3	0b RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
2	0b RW	**RXEOTSYNCERROR:** mipi C RX eot synce error
1	0b RW	**RXSOTSYNCERROR:** Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
0	0b RW	**RXSOTERROR:** Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

14.10.100 MIPIC_INTR_EN_REG—Offset B808h

mipi C intrrupt En reg

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B808h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	RESERVED
30	0	SPL_PKT_SENT_INTERRUPT
29	0	GEN_READ_DATA_AVAIL
28	0	LP_GENERIC_WR_FIFO_FULL
27	0	HS_GENERIC_WR_FIFO_FULL
26	0	RX_PROT_VIOLATION
25	0	RX_INVALID_TX_LENGTH
24	0	ACK_WITH_NO_ERROR
23	0	TURN_AROUND_ACK_TIMEOUT
22	0	LP_RX_TIMEOUT
21	0	HS_TX_TIMEOUT
20	0	DPI_FIFO_UNDERRUN
19	0	LOW_CONTENTION
18	0	HIGH_CONTENTION
17	0	TXDSI_VC_ID_INVALID
16	0	TXDSI_DATA_TYPE_NOT_RECOGNISED
15	0	TXCHECKSUM_ERROR
14	0	TXECC_MULTIBIT_ERROR
13	0	TXECC_SINGLE_BIT_ERROR
12	0	TXFALSE_CONTROL_ERROR
11	0	RXDSI_VC_ID_INVALID
10	0	RXDSI_DATA_TYPE_NOT_RECOGNISED
9	0	RXCHECKSUM_ERROR
8	0	RXECC_MULTIBIT_ERROR
7	0	RXECC_SINGLE_BIT_ERROR
6	0	RXFALSE_CONTROL_ERROR
5	0	RXHS_RECEIVE_TIMEOUT_ERROR
4	0	RX_LP_TX_SYNC_ERROR
3	0	RXESCAPE_MODE_ENTRY_ERROR
2	0	RXEOTSYNC_ERROR
1	0	RXSOTSYNC_ERROR
0	0	RXSOT_ERROR

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**TEARING_EFFECT (RESERVED):** Set to eanble tearing effect
30	0b RW	**SPL_PKT_SENT_INTERRUPT:** Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register

Bit Range	Default & Access	Field Name (ID): Description
29	0b RW	**GEN_READ_DATA_AVAIL:** Set to enable Generic Read available interrupt
28	0b RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0b RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0b RW	**RX_PROT_VIOLATION:** Set to enable protocol violation error
25	0b RW	**RX_INVALID_TX_LENGTH:** Set to enable invalid transmission length error
24	0b RW	**ACK_WITH_NO_ERROR:** Set to enable acknowledge trigger message reception with out any error
23	0b RW	**TURN_AROUND_ACK_TIMEOUT:** Set to enable turn around acknowledgement ,sequence timeout
22	0b RW	**LP_RX_TIMEOUT:** Set to enable low power reception count timeouts
21	0b RW	**HS_TX_TIMEOUT:** Set to enable a high speed transmission timeout
20	0b RW	**DPI_FIFO_UNDERRUN:** Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0b RW	**LOW_CONTENTION:** Set to enable a LP low fault interrupt
18	0b RW	**HIGH_CONTENTION:** Set to enable a LP high fault interrupt
17	0b RW	**TXDSI_VC_ID_INVALID:** Set to enable the interrupt if the received packets virtual channel ID is invalid
16	0b RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt if the received packets data type is not recognised
15	0b RW	**TXCHECKSUM_ERROR:** Set to enable the interrupt if the computed CRC differs from the received CRC value for the received packets
14	0b RW	**TXECC_MULTIBIT_ERROR:** Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
13	0b RW	**TXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
12	0b RW	**TXFALSE_CONTROL_ERROR:** Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
11	0b RW	**RXDSI_VC_ID_INVALID:** Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
10	0b RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt for the un recognised data type in the acknowledgment packet reports
9	0b RW	**RXCHECKSUM_ERROR:** Set to enable the interrupt for the computed CRC differs from the received CRC value in the acknowledgment packet reports
8	0b RW	**RXECC_MULTIBIT_ERROR:** Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**RXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
6	0b RW	**RXFALSE_CONTROL_ERROR:** Set to enable the interrupt for control error in the acknowledgment packet reports
5	0b RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
4	0b RW	**RX_LP_TX_SYNC_ERROR:** Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports
3	0b RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
2	0b RW	**RXEOTSYNC_ERROR:** Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
1	0b RW	**RXSOTSYNC_ERROR:** Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports
0	0b RW	**RXSOT_ERROR:** Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

14.10.101 MIPIC_DSI_FUNC_PRG__REG—Offset B80Ch

mipi C DSI func prg reg

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B80Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

RESERVED	SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE	RESERVED_1	SUPPORTED_FORMAT_IN_VIDEO_MODE	CHANNEL_NUMBER_FOR_COMMAND_MODE	CHANNEL_NUMBER_FOR_VIDEO_MODE	DATA_LANES_PRG_R_EG

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:13	0b RW	**SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE:** 000 --) Reserved, 001 --) 16 bit data , 010 --) 9 bit data , 011 --) 8 bit data , 100 --) option 1 : 101 --) option 2 : 110 to 111 --) Reserved
12:11	0b RW	**RESERVED_1:** Reserved.
10:7	0b RW	**SUPPORTED_FORMAT_IN_VIDEO_MODE:** Supported colour format, 0001 --) RGB565, 0010 --) RGB666, 0011 --) RGB 666 loosely packed format, 0100 --) RGB888
6:5	0b RW	**CHANNEL_NUMBER_FOR_COMMAND_MODE:** Virtual channel number for command mode is programmed by the processor
4:3	0b RW	**CHANNEL_NUMBER_FOR_VIDEO_MODE:** Virtual channel number for command mode is programmed by the processor
2:0	001b RW	**DATA_LANES_PRG_R_EG:** Number of data lanes to be supported is programmed by the processor

14.10.102 MIPIC_HS_TX_TIMEOUT_REG—Offset B810h

mipi C HS TX timeout reg

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B810h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								HIGH_SPEED_TX_TIMEOUT_COUNTER																							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:0	0b RW	**HIGH_SPEED_TX_TIMEOUT_COUNTER:** The maximum duration allowed for the DSI host ,to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

14.10.103 MIPIC_LP_RX_TIMEOUT_REG—Offset B814h

mipi C LP RX timeout reg

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B814h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								LOW_POWER_RECEPTION_TIMEOUT_COUNTER																							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:0	0b RW	**LOW_POWER_RECEPTION_TIMEOUT_COUNTER:** Timeout value to be checked for received short packets .If the timer expires the DSI Host enters stop state

14.10.104 MIPIC_TURN_AROUND_TIMEOUT_REG—Offset B818h

mipi C Turn Arounf timeout reg

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B818h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bits 5:0
RESERVED	TURN_AROUND_TIMEOUT_REGISTER

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**RESERVED:** Reserved.
5:0	0b RW	**TURN_AROUND_TIMEOUT_REGISTER:** Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

14.10.105 MIPIC_DEVICE_RESET_TIMER—Offset B81Ch

mipi C Device reset timer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B81Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																DEVICE_RESET_TIMER															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**DEVICE_RESET_TIMER:** Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

14.10.106 MIPIC_DPI_RESOLUTION_REG—Offset B820h

mipi C dpi Resolution reg

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B820h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VERTICAL_ADDRESS																HORIZONTAL_ADDRESS															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**VERTICAL_ADDRESS:** Shows the vertical address count in lines
15:0	0b RW	**HORIZONTAL_ADDRESS:** Shows the horizontal address count in pixels

14.10.107 MIPIC_DBI_RESOLUTION_REG—Offset B824h

mipi C DBI resolution reg

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B824h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																														DBI_FIFO_THRTL	

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**RESERVED:** Reserved.
1:0	0b RW	**DBI_FIFO_THRTL:** DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached: 00 - (1/2) DBI fifo empty 01 - (1/4) DBI fifo empty 10 - 7 locations are empty 11 - Reserved

14.10.108 MIPIC_HORIZ_SYNC_PADDING_COUNT—Offset B828h

mipi C horizxontal sync padding out

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B828h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED				HORIZONTAL_SYNC_PADDING_COUNT			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_SYNC_PADDING_COUNT:** Shows the horizontal sync padding value in terms of txbyteclkhs

14.10.109 MIPIC_HORIZ_BACK_PORCH_COUNT—Offset B82Ch

mipi C horizontal back portch counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B82Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED				HORIZONTAL_BACK_PORCH_COUNT			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_BACK_PORCH_COUNT:** Shows the horizontal back porch value in terms of txbyteclkhs

14.10.110 MIPIC_HORIZ_FRONT_PORCH_COUNT—Offset B830h

mipi C horizontal front Porch counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B830h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED

HORIZONTAL_FRONT_PORCH_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_FRONT_PORCH_COUNT:** Shows the horizontal front porch value in terms of txbyteclkhs

14.10.111 MIPIC_HORIZ_ACTIVE_AREA_COUNT—Offset B834h

mipi C horizontal active area count

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B834h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
RESERVED	HORIZONTAL_ACTIVE_AREA_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**HORIZONTAL_ACTIVE_AREA_COUNT:** Shows the horizontal active area value in terms of txbyteclkhs

14.10.112 MIPIC_VERT_SYNC_PADDING_COUNT—Offset B838h

mipi C vertical sync padding count

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B838h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
RESERVED	VERTICAL_SYNC_PADDING_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_SYNC_PADDING_COUNT:** Shows the vertical sync padding value in terms of lines

14.10.113 MIPIC_VERT_BACK_PORCH_COUNT—Offset B83Ch

mipic Vertical back porch count

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B83Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																VERTICAL_BACK_PORCH_COUNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_BACK_PORCH_COUNT:** Shows the vertical back porch value in terms of lines

14.10.114 MIPIC_VERT_FRONT_PORCH_COUNT—Offset B840h

mipi C vertical front porch count

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B840h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																VERTICAL_FRONT_PORCH_COUNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**VERTICAL_FRONT_PORCH_COUNT:** Shows the vertical front porch value in terms of lines

14.10.115 MIPIC_HIGH_LOW_SWITCH_COUNT—Offset B844h

mipi C high low switch count

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B844h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs
15:0	0b RW	**HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

14.10.116 MIPIC_DPI_CTRL_REG—Offset B848h

mipi C dpi ctrl reg

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B848h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8	4				0			
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
RESERVED	RSTTRG	HS_LP	BACK_LIGHT_OFF	BACK_LIGHT_ON	COLOR_MODE_OFF	COLOR_MODE_ON	TURN_ON	SHUT_DOWN

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** Reserved.
7	0b RW	**RSTTRG:** mipi C dpi ctrl Reg RSTTRG
6	0b RW	**HS_LP:** Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode
5	0b RW	**BACK_LIGHT_OFF:** Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel
4	0b RW	**BACK_LIGHT_ON:** Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
3	0b RW	**COLOR_MODE_OFF:** Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
2	0b RW	**COLOR_MODE_ON:** Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
1	0b RW	**TURN_ON:** Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
0	0b RW	**SHUT_DOWN:** Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

14.10.117 MIPIC_DPI_DATA_REGISTER—Offset B84Ch

mipiC dpi data register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B84Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8	4 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
RESERVED	COMMAND_BYTE

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**RESERVED:** Reserved.
5:0	0b RW	**COMMAND_BYTE:** Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

14.10.118 MIPIC_INIT_COUNT_REGISTER—Offset B850h

mipi C init counter register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B850h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (bits 31:16) | MASTER_INIT_TIMER (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**MASTER_INIT_TIMER:** Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

14.10.119 MIPIC_MAX_RETURN_PKT_SIZE_REGISTER—Offset B854h

mipi C max return PKT size register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B854h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																						MAX_RETURN_PKT_SIZE										

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**RESERVED:** Reserved.
9:0	0b RW	**MAX_RETURN_PKT_SIZE:** Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

14.10.120 MIPIC_VIDEO_MODE_FORMAT_REGISTER—Offset B858h

mipi C video mode format register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B858h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																											RANDOM_DPI_DISPLAY_RESOLUTION_DEFEATURE	MIPIC_DISABLE_VIDEO_BTA	IP_TG_CONFIG	VIDEO_MODE_FMT	

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RW	**RESERVED:** Reserved.
4	0b RW	**RANDOM_DPI_DISPLAY_RESOLUTION_DEFEATURE:** Set by the processor to support random DPI display resolution 0 - random DPI display resolution support disabled. 1 - random DPI display resolution support enabled.
3	0b RW	**MIPIC_DISABLE_VIDEO_BTA:** Set by the processor to inform the DSI controller to disable the BTA sent at the last blanking line of VFP. By default, this bit is set to 0. 0- BTA sending at the last blanking line of VFP is enabled. 1 - BTA sentding at teh last blanking line of VFP is disabeld.
2	0b RW	**IP_TG_CONFIG:** Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0. 0 - After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted. 1 - After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP
1:0	0b RW	**VIDEO_MODE_FMT:** Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. 00 Reserved 01 - Non Burst Mode with Sync Pulse 10 - Non Burst Mode with Sync events 11 - Burst Mode

14.10.121 MIPIC_EOT_DISABLE_REGISTER—Offset B85Ch

mipi C EOT disable register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B85Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	RESERVED																								LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE	HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE	LOW_CONTENTION_RECOVERY_DISABLE	HIGH_CONTENTION_RECOVERY_DISABLE	TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE	TXECC_MULTIBIT_ERR_RECOVERY_DISABLE	CLOCKSTOP	EOT_DIS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** Reserved.
7	0b RW	**LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt. 0 - LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt. 1 - If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx contorller. LP Rx timeout error interrupt will act as an informative interrupt
6	0b RW	**HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt. 0 - HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt. 1 - If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx contorller. HS Tx timeout error interrupt will act as an informative interrupt
5	0b RW	**LOW_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt. 0 - Contention recovery will happen if the processor clears Low contention interrupt. 1 - If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Low contention interrupt will act as an informative interrupt
4	0b RW	**HIGH_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt. 0 - Contention recovery will happen if the processor clears High contention interrupt. 1 - If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognised error interrupt is cleared by the processor. 0 - Error recovery action will be taken if TxDSI data type not recognised error interrupt is cleared by the processor. 1 - If TxDSI data type not recognised error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt
2	0b RW	**TXECC_MULTIBIT_ERR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor. 0 - Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor. 1 - If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt
1	0b RW	**CLOCKSTOP:** Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0. 0 - clock stopping disabled 1 - clock stopping enabled
0	0b RW	**EOT_DIS:** Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward comapatibility of earlier DSI systems, EOT short packet transmission can be disabled. 0 - EOT short packet transmission enabled 1 - EOT short packet transmission disabled

14.10.122 MIPIC_LP_BYTECLK_REGISTER—Offset B860h

mipi C LP byteclk register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B860h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
RESERVED	LP_BYTECLK

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**LP_BYTECLK:** Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

14.10.123 MIPIC_LP_GEN_DATA_REGISTER—Offset B864h

mipi C LP gen DATA register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B864h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LP_GEN_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**LP_GEN_DATA:** Data port register used for generic data transfers in low power mode

14.10.124 MIPIC_HS_GEN_DATA_REGISTER—Offset B868h

mipi C HS Gen data register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B868h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HS_GEN_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**HS_GEN_DATA:** Data port register used for generic data transfers in low power mode

14.10.125 MIPIC_LP_GEN_CTRL_REGISTER—Offset B86Ch

mipi C LP Gen ctrl register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B86Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								WORD_COUNT																VIRTUAL_CHANNEL		DATA_TYPE					

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b WO	**RESERVED:** Reserved.
23:8	0b WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0b WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended
5:0	0b WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

14.10.126 MIPIC_HS_GEN_CTRL_REGISTER—Offset B870h

mipiC HS

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B870h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED	WORD_COUNT	VIRTUAL_CHANNEL	DATA_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b WO	**RESERVED:** Reserved.
23:8	0b WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0b WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended
5:0	0b WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

14.10.127 MIPIC_GEN_FIFO_STAT_REGISTER—Offset B874h

mipi C gen fifo stat register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B874h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 1E060606h

31	28	24	20	16	12	8	4	0
0 0 0 1	1 1 1 0	0 0 0 0	0 1 1 0	0 0 0 0	0 1 1 0	0 0 0 0	0 1 1 0	

RESERVED	DPI_FIFO_EMPTY	DBI_FIFO_EMPTY	LP_CTRL_FIFO_EMPTY	LP_CTRL_FIFO_HALF_EMPTY	LP_CTRL_FIFO_FULL	RESERVED_1	HS_CTRL_FIFO_EMPTY	HS_CTRL_FIFO_HALF_EMPTY	HS_CTRL_FIFO_FULL	RESERVED_2	LP_DATA_FIFO_EMPTY	LP_DATA_FIFO_HALF_EMPTY	LP_DATA_FIFO_FULL	RESERVED_3	HS_DATA_FIFO_EMPTY	HS_DATA_FIFO_HALF_EMPTY	HS_DATA_FIFO_FULL
0 0 0	1	1	1	1	0	0 0 0 0 0	1	1	0	0 0 0 0 0	1	1	0	0 0 0 0 0	1	1	0

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RO	**RESERVED:** Reserved.
28	1b RO	**DPI_FIFO_EMPTY:** Default 1
27	1b RO	**DBI_FIFO_EMPTY:** Default 1
26	1b RO	**LP_CTRL_FIFO_EMPTY:** Default 1
25	1b RO	**LP_CTRL_FIFO_HALF_EMPTY:** Default 1
24	0b RO	**LP_CTRL_FIFO_FULL:** Default 0
23:19	0b RO	**RESERVED_1:** Reserved.
18	1b RO	**HS_CTRL_FIFO_EMPTY:** Default 1
17	1b RO	**HS_CTRL_FIFO_HALF_EMPTY:** Default 1
16	0b RO	**HS_CTRL_FIFO_FULL:** Default 0
15:11	0b RO	**RESERVED_2:** Reserved.
10	1b RO	**LP_DATA_FIFO_EMPTY:** Default 1
9	1b RO	**LP_DATA_FIFO_HALF_EMPTY:** Default 1
8	0b RO	**LP_DATA_FIFO_FULL:** Default 0
7:3	0b RO	**RESERVED_3:** Reserved.
2	1b RO	**HS_DATA_FIFO_EMPTY:** Default 1
1	1b RO	**HS_DATA_FIFO_HALF_EMPTY:** Default 1

Bit Range	Default & Access	Field Name (ID): Description
0	0b RO	**HS_DATA_FIFO_FULL:** Default 0

14.10.128 MIPIC_HS_LS_DBI_ENABLE_REG—Offset B878h

Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B878h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
RESERVED	DBI_HS_LS_SWITCH_RE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**RESERVED:** Reserved.
0	0b RW	**DBI_HS_LS_SWITCH_RE:** Set to 1 if DBI packets have to be transmitted in Low power mode Set to 0 if DBI packets have to be transmitted in High speed mode

14.10.129 MIPIC_RESERVED—Offset B87Ch

Reserved.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B87Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RESERVED:** Reserved.

14.10.130 MIPIC_DPHY_PARAM_REG—Offset B880h

mipi C dphy param reg

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B880h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0B061A04h

31			28				24				20				16				12				8				4			0
0	0	0	0	1	0	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0
RESERVED		EXIT_ZERO_COUNT						RESERVED_1			TRAIL_COUNT					CLK_ZERO_COUNT								RESERVED_2		PREPARE_COUNT					

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** Reserved.
29:24	001011b RW	**EXIT_ZERO_COUNT:** THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
23:21	0b RW	**RESERVED_1:** Reserved.
20:16	00110b RW	**TRAIL_COUNT:** TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
15:8	00011010b RW	**CLK_ZERO_COUNT:** TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor
7:6	0b RW	**RESERVED_2:** Reserved.
5:0	000100b RW	**PREPARE_COUNT:** TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

14.10.131 MIPIC_DBI_BW_CTRL_REG—Offset B884h

mipi C DBI BW ctrl reg

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B884h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BANDWIDTH_TIMER

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**BANDWIDTH_TIMER:** DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies. Note: The value programmed in this timer must be greater than the actual time taken to carryout 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

14.10.132 MIPIC_CLK_LANE_SWITCHING_TIME_CNT—Offset B888h

mipi C clk lane switching time count

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B888h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LS_HS_SSW_CNT

HS_LS_PWR_SW_CNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**LS_HS_SSW_CNT:** Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	0b RW	**HS_LS_PWR_SW_CNT:** High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

14.10.133 MIPIC_STOP_STATE_STALL—Offset B88Ch

mipi C stop state stall

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B88Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
RESERVED	MIPIC_STOP_STATE_STALL_COUNTER

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** reserved
7:0	0b RW	**MIPIC_STOP_STATE_STALL_COUNTER:** Delay between (stall the stop state signal) the data transfer is increased based on this counter value. This counter is calculated from txclkesc. Note: If processor programs this register then it needs to reprogram the high_low_ switch counter in B844h and lp_equivalent_byteclk reg in B860h to compensate this delay. High_low_switch_count B844h: High to low switch counter = Actual High to low switch + stop_sta_stall_reg value * Low power clock equivalence value in terms of byte clock LP equivalent byteclk register B860h: LP equivalent byteclk value = txclkesc time/ txbyteclk time * (105 + stop_sta_stall_reg value) / 105 Minimum time of Low Power short packet transfer = 105 txclkesc

14.10.134 MIPIC_INTR_STAT_REG_1—Offset B890h

mipi C intrrupt stat register 1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B890h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

MIPIC_RX_CONNECTION_DETECTED

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**RESERVED:** reserved
0	0b RW	**MIPIC_RX_CONNECTION_DETECTED:** Set to 1'b1 if the contention detected in the display device and is reported in the Acknowledge packet by the display device

14.10.135 MIPIC_INTR_EN_REG_1—Offset B894h

mipic interrupt enable register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B894h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:1	0
Default	0000 0000 0000 0000 0000 0000 0000 000	0
Field	RESERVED	MIPIC_ENABLE_RX_CONNECTION_DETECTED

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**RESERVED:** reserved
0	0b RW	**MIPIC_ENABLE_RX_CONNECTION_DETECTED:** Set to enable the interrupt for contention detected error in the acknowledgement packet reports

14.10.136 MIPIC_CTRL—Offset B904h

mipi ctrl reg

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B904h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:5	4:3	2	1:0
Default	0000 0000 0000 0000 0000 0000 000	00	0	00
Field	NAME_BITS	STATUS	RGB_FLIP	MIPI_2X_CLOCK_DIVIDER

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RW	**NAME_BITS:** Reserved
4:3	0b RW	**STATUS:** 2'b00: low priority on read requests to G-unit 2'b11 : high priority
2	0b RW	**RGB_FLIP:** 1'b0 : RGB data from disp2d is reverted to BGR 1'b1 : RGB data from disp2d is passed as is to MIPI IP
1:0	0b RW	**MIPI_2X_CLOCK_DIVIDER:** Reserved

14.10.137 MIPIC_DATA_ADD—Offset B908h

mipi C data ADD

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B908h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

DATA_MEM_ADDR | DATA_MEM_ADDR_1 | DATA_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RW	**DATA_MEM_ADDR:** When there is updated data for the display panel, S/W programs this register with the memory address to read from
4:1	0b RW	**DATA_MEM_ADDR_1:** Reserved
0	0b RW	**DATA_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.10.138 MIPIC_DATA_LEN—Offset B90Ch

mipiC data length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B90Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED												DATA_LENGTH																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**DATA_LENGTH:** This field shows the remaining length of data that needs to be read from memory, Initially set by S/W and is decremented by H/W as reads are issued

14.10.139 MIPIC_CMD_ADD—Offset B910h

mipiC command add

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B910h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COMMAND_MEM_ADDR																											RESERVED		MIPIC_AUTO_PWG_ENABLE	COMMAND_DATA_MODE	COMMAND_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RW	**COMMAND_MEM_ADDR:** When there are new commands that need to be sent to the display panel, S/W programs this register with the memory address to read the commands from
4:3	0b RW	**RESERVED:** MBZ
2	0b RW	**MIPIC_AUTO_PWG_ENABLE:** Idle state: SW driver writes to this bit to enable auto power gating for MIPIC controller 0: default 1: auto power gate is enabled

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**COMMAND_DATA_MODE:** 0: data for memory write command from system buffer that is specified by MIPI data address register 1: data for memory write command from pipe A rendering
0	0b RW	**COMMAND_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.10.140 MIPIC_CMD_LEN—Offset B914h

mipiC commanf Length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B914h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COMMAND_3								COMMAND_2								COMMAND_1								COMMAND_0							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**COMMAND_3:** This is command 3 length (command + parameters) in bytes
23:16	0b RW	**COMMAND_2:** This is command 2 length (command + parameters) in bytes
15:8	0b RW	**COMMAND_1:** This is command 1 length (command + parameters) in bytes
7:0	0b RW	**COMMAND_0:** This is command 0 length (command + parameters) in bytes

14.10.141 MIPIC_RD_DATA_RETURN0—Offset B918h

mipi C Read data return 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B918h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.142 MIPIC_RD_DATA_RETURN1—Offset B91Ch

mipi C read data return 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B91Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.143 MIPIC_RD_DATA_RETURN2—Offset B920h

mipi C read data return 2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B920h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.144 MIPIC_RD_DATA_RETURN3—Offset B924h

mipi C read data return 3

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B924h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.145 MIPIC_RD_DATA_RETURN4—Offset B928h

mipi C read data return 4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B928h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.146 MIPIC_RD_DATA_RETURN5—Offset B92Ch

mipi C read data return 5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B92Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.147 MIPIC_RD_DATA_RETURN6—Offset B930h

mipi C read data return 6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B930h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.148 MIPIC_RD_DATA_RETURN7—Offset B934h

mipi C read data return 7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B934h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RD_DATA_RETURN_PANEL

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

14.10.149 MIPIC_RD_DATA_VALID—Offset B938h

mipi C read data valid

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + B938h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

READ_DATA_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** Reserved.
7:0	0b RW	**READ_DATA_VALID:** Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. When S/W issues a write '1 to the registers, this bit is cleared

14.10.150 HTOTAL_A—Offset 60000h

Pipe A Horizontal Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:29	Bits 28:16	Bits 15:12	Bits 11:0
RESERVED	PIPE_A_HORIZONTAL_TOTAL_DISPLAY_CLOCKS	RESERVED_1	PIPE_A_HORIZONTAL_ACTIVE_DISPLAY_END_PIXELS

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_A_HORIZONTAL_TOTAL_DISPLAY_CLOCKS:** This 13-bit field provides Horizontal Total up to 8192 pixels encompassing the Horizontal Active Display period, front/back border and retrace period. Any pending event (HSYNC, ACTIVE, HBLANK) is reset at HTOTAL and the programmed sequence begins again. This field is programmed to the number of clocks desired minus one. This number of clocks needs to be a multiple of two when driving data out the digital port out the LVDS port in two channel mode. This value should always be equal or greater to the sum of the horizontal active and the horizontal blank, and border region sizes.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0b RW	**RESERVED_1:** Write as zero.
11:0	0b RW	**PIPE_A_HORIZONTAL_ACTIVE_DISPLAY_END_PIXELS:** This 12-bit field provides Horizontal Active Display resolutions up to 4096 pixels. Note that the first horizontal active display pixel is considered pixel number 0. The value programmed should be the (active pixels/line 1). The number of active pixels will be limited to multiples of two pixels when driving the integrated LVDS port in two channel mode. For proper results during VGA centering mode this value needs to be large enough to fit the largest VGA mode supported, this should be at least 720/1440 pixels for standard VGA type modes or 640/1280 pixels if the nine-dot disable bit in the VGA control register is set. When using the internal panel fitting logic, the minimum horizontal size allowed will be three pixels.

14.10.151 HBLANK_A—Offset 60004h

Pipe A Horizontal Blank Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits 31:29	Bits 28:16	Bits 15:13	Bits 12:0
RESERVED	PIPE_A_HORIZONTAL_BLANK_END	RESERVED_1	PIPE_A_HORIZONTAL_BLANK_START

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Read Only.

Bit Range	Default & Access	Field Name (ID): Description
28:16	0b RW	**PIPE_A_HORIZONTAL_BLANK_END:** This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving data out LVDS in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the HTOTAL register.
15:13	0b RW	**RESERVED_1:** Read Only.
12:0	0b RW	**PIPE_A_HORIZONTAL_BLANK_START:** This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving data out the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The value loaded in the register would be equal to RightBorder+Active-1. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the HACTIVE register.

14.10.152 HSYNC_A—Offset 60008h

Pipe A Horizontal Sync Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED			PIPE_A_HORIZONTAL_SYNC_END													RESERVED_1			PIPE_A_HORIZONTAL_SYNC_START												

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_A_HORIZONTAL_SYNC_END:** This 13-bit field specifies the horizontal Sync End position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks in the sync period needs to be a multiple of two when driving data out the LVDS port in two channel mode. This value should be greater than the horizontal sync start position and would be loaded with the Active+RightBorder+FrontPorch+Sync-1.
15:13	0b RW	**RESERVED_1:** Read Only.
12:0	0b RW	**PIPE_A_HORIZONTAL_SYNC_START:** This 13-bit field specifies the horizontal Sync Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Note that when HSYNC Start is programmed equal to HBLANK Start, both HSYNC and HBLANK will be asserted on the same pixel clock. It should never be programmed to less than HBLANK start. The number of cycles from the beginning of the line needs to be a multiple of two when driving data out the LVDS port in two channel mode. This register should not be less than the horizontal active end. This register should be loaded with the Active+RightBorder+FrontPorch-1.

14.10.153 VTOTAL_A—Offset 6000Ch

Pipe A Vertical Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6000Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED			PIPE_A_VERTICAL_TOTAL_DISPLAY_LINES													RESERVED_1			PIPE_A_VERTICAL_ACTIVE_DISPLAY_LINES												

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Read Only.
28:16	0b RW	**PIPE_A_VERTICAL_TOTAL_DISPLAY_LINES:** This 13 bit field provides Vertical Total up to 8192 lines encompassing the Vertical Active Display Lines, top/bottom border and retrace period. The value programmed should be the number of lines required minus one. Vertical total needs to be large enough to be greater than the sum of the vertical active, vertical border, and the vertical blank regions. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.
15:12	0b RW	**RESERVED_1:** Read Only.
11:0	0b RW	**PIPE_A_VERTICAL_ACTIVE_DISPLAY_LINES:** This 12-bit field provides vertical active display resolutions up to 4096 lines. It should be programmed with the desired number of lines minus one. When using the internal panel fitting logic, the minimum vertical active area must be three lines. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.

14.10.154 VBLANK_A—Offset 60010h

Pipe A Vertical Blank Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:29	Bits 28:16	Bits 15:12	Bits 11:0
RESERVED	PIPE_A_VERTICAL_BLANK_END	RESERVED_1	PIPE_A_VERTICAL_BLANK_START

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Read Only.

Bit Range	Default & Access	Field Name (ID): Description
28:16	0b RW	**PIPE_A_VERTICAL_BLANK_END:** This 13-bit field specifies the Vertical Blank End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VBLANK End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. The end of vertical blank should be after the start of vertical blank and before or equal to the vertical total. This register should be loaded with the Vactive+BottomBorder+VBlank-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank end in each field. It does not count the two half lines that get added when operating in modes with half lines. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the VTOTAL register.
15:13	0b RW	**RESERVED_1:** Read Only.
12:0	0b RW	**PIPE_A_VERTICAL_BLANK_START:** This 13-bit field specifies the Vertical Blank Start expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VBLANK Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. Minimum vertical blank size is required to be at least three lines. Blank should start after the end of active. This register is loaded with the Vactive+BottomBorder-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank start in each field. It does not count the two half lines that get added when operating in modes with half lines. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the VACTIVE register.

14.10.155 VSYNC_A—Offset 60014h

Pipe A Vertical Sync Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:29	28:16	15:13	12:0
Default	000	0 0000 0000 0000	000	0 0000 0000 0000
Field	RESERVED	PIPE_A_VERTICAL_SYNC_END	RESERVED_1	PIPE_A_VERTICAL_SYNC_START

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Read Only.

Bit Range	Default & Access	Field Name (ID): Description
28:16	0b RW	**PIPE_A_VERTICAL_SYNC_END:** This 13-bit field specifies the Vertical Sync End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VSYNC End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register should be loaded with Vactive+BottomBorder+FrontPorch+Sync-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync end in each field. It does not count the two half lines that get added when operating in modes with half lines.
15:13	0b RW	**RESERVED_1:** Read Only.
12:0	0b RW	**PIPE_A_VERTICAL_SYNC_START:** This 13-bit field specifies the Vertical Sync Start position expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VSYNC Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register would be loaded with Vactive+BottomBorder+FrontPorch-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync start in each field. It does not count the two half lines that get added when operating in modes with half lines.

14.10.156 PIPESRCA—Offset 6001Ch

Pipe A Source Image Size

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6001Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:28	27:16	15:12	11:0
Default	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
Field	RESERVED	PIPE_A_HORIZONTAL_SOURCE_IMAGE_SIZE	RESERVED_1	PIPE_A_VERTICAL_SOURCE_IMAGE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
27:16	0b RW	**PIPE_A_HORIZONTAL_SOURCE_IMAGE_SIZE:** This 12-bit field specifies Horizontal source image size up to 4096. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. The actual source size must be two times the programmed value in the pixel multiply mode. It must represent a size that is a multiple of two (even numbers) when driving the LVDS port in two channel mode. This implies that for this mode, the value programmed will always be an odd number. Except in the case of panel fitting internal or in an external device, this register field would be programmed to a value identical to the horizontal active. This is the only register of the timing registers that is allowed to be programmed while the pipe is enabled.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PIPE_A_VERTICAL_SOURCE_IMAGE_SIZE:** This 12-bit field specifies the vertical source image size up to 4096 lines. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. Note that the actual number of lines needs to be at least twice the planes programmed value when in the pixel multiply mode. Except in the case of panel fitting internal or in an external device, this register field would be programmed to a value identical to the vertical active. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical source image size in each field.

14.10.157 BCLRPAT_A—Offset 60020h

Pipe A Border Color Pattern Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
RESERVED	PIPE_A_BORDER_RED_CHANNEL_VALUE	PIPE_A_BORDER_GREEN_CHANNEL_VALUE	PIPE_A_BORDER_BLUE_CHANNEL_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**PIPE_A_BORDER_RED_CHANNEL_VALUE:** pipeA border red channel values
15:8	0b RW	**PIPE_A_BORDER_GREEN_CHANNEL_VALUE:** pipeA border green channel values
7:0	0b RW	**PIPE_A_BORDER_BLUE_CHANNEL_VALUE:** pipeA border blue channel values

14.10.158 VSYNCSHIFT_A—Offset 60028h

Vertical Sync Shift Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																			PIPE_A_SECOND_FIELD_VERTICAL_SYNC_SHIFT												

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**RESERVED:** Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
12:0	0b RW	**PIPE_A_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEACONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

14.10.159 TRANSADATAM1—Offset 60030h

Pipe A Data M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60030h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 7E000000h

Bits	31	30:25	24	23:0
Value	0	1 1 1 1 1 1	0	0000 0000 0000 0000 0000 0000
Field	RESERVED	TU1_SIZE	RESERVED_1	PIPE_A_DATA_M1_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:25	111111b RW	**TU1_SIZE:** Project: All This field is the size of the transfer unit for DP, minus one.
24	0b RW	**RESERVED_1:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_DATA_M1_VALUE:** Project: All This field is the M1 value for internal use of the DDA.

14.10.160 TRANSADATAN1—Offset 60034h

Pipe A Data N value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60034h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RESERVED (31:24), PIPE_A_DATA_N1_VALUE (23:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_DATA_N1_VALUE:** Project: All This field is the N1 value for internal use of the DDA.

14.10.161 TRANSADATAM2—Offset 60038h

Pipe A Data M value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60038h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 7E000000h

31			28				24				20				16				12				8				4				0
0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RESERVED (31), TU2_SIZE (30:25), RESERVED_1 (24), PIPE_A_DATA_M2_VALUE (23:0)

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:25	111111b RW	**TU2_SIZE:** Project: All Default Value: ;111111b 64 This field is the size of the transfer unit for DP, minus one.
24	0b RW	**RESERVED_1:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_DATA_M2_VALUE:** Project: All This field is the M2 value for internal use of the DDA.

14.10.162 TRANSADATAN2—Offset 6003Ch

Pipe A Data N value 2

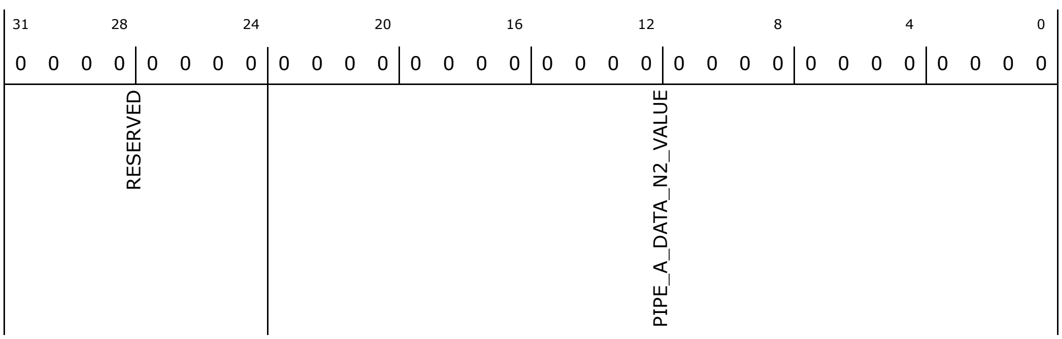
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6003Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_DATA_N2_VALUE:** Project: All This field is the N2 value for internal use of the DDA.

14.10.163 TRANSADPLINKM1—Offset 60040h

Pipe A Link M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | PIPE_A_LINK_M1_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_LINK_M1_VALUE:** Project: All This field is the M1 value for external transmission in the Main Stream Attributes.

14.10.164 TRANSADPLINKN1—Offset 60044h

Pipe A Link N value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | PIPE_A_LINK_N1_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_LINK_N1_VALUE:** Project: All This field is the N1 value for external transmission in the Main Stream Attributes and VB-ID.

14.10.165 TRANSADPLINKM2—Offset 60048h

Pipe A Link M value 2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED

PIPE_A_LINK_M2_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_LINK_M2_VALUE:** Project: All This field is the M2 value for external transmission in the Main Stream Attributes.

14.10.166 TRANSADPLINKN2—Offset 6004Ch

Pipe A Link N value 2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6004Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED

PIPE_A_LINK_N2_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_A_LINK_N2_VALUE:** Project: All This field is the N2 value for external transmission in the Main Stream Attributes and VB-ID.

14.10.167 CRCCTRLREDA—Offset 60050h

Pipe A CRC Color Channel Control Register (Red)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30:27 (28)	26:23 (24)	22:0 (20, 16, 12, 8, 4, 0)
0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ENABLE_COLOR_CRC	CRC_SOURCE_SELECT	RESERVED	EXPECTED_CRC_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_COLOR_CRC:** Enables the CRC calculations. After being enabled for the first time, you need to wait for two VBLANK events for a valid CRC result. After that, a CRC will be generated each frame. 0 = CRC Calculations are disabled 1 = CRC Calculations are enabled
30:27	0b RW	**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 0000: Pipe A (Not available when DisplayPort or TV is enabled on this pipe) [DevVLVP] 0001: sDVOB/HDMIB (30 bit format. Only select when HDMIB is set to pipeA) [DevVLVP] 0010: sDVOC/HDMIC (30 bit format. Only select when HDMIC is set to pipeA) [DevVLVP] 0011: DisplayPort D (40 bit format) [DevCTG] 0100: TV Encoder outputs (30 bit format) 0101: TV filter outputs (30 bit format) 0110: DisplayPort B (40 bit format) [DevCTG, DevCDV, DevVLVP] 0111: DisplayPort C (40 bit format) [DevCTG, DevCDV, DevVLVP] 1000: Audio DP (Audio for DisplayPort (pcdclk). Only select when Audio is on DisplayPort on Pipe A) [DevVLVP] 1001: Audio HDMI (Audio for HDMI (dotclock) Only select when Audio is on HDMI on Pipe A) Others: Reserved
26:23	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

14.10.168 CRCCTRLGREENA—Offset 60054h

Pipe A CRC Color Channel Control Register (, Residual)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | EXPECTED_CRC_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

14.10.169 CRCCTRLBLUEA—Offset 60058h

Pipe A CRC Color Channel Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60058h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED	EXPECTED_CRC_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

14.10.170 CRCCTRLALPHAA—Offset 6005Ch

Pipe A CRC Color Channel Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6005Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED	EXPECTED_CRC_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

14.10.171 CRCRESREDA—Offset 60060h

Pipe A A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:23	Bits 22:0
RESERVED	COLOR_CHANNEL_CRC_RESULT_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

14.10.172 CRCRESGREENA—Offset 60064h

Pipe A A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RESERVED (31:23), COLOR_CHANNEL_CRC_RESULT_VALUE (22:0)

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

14.10.173 CRCRESBLUEA—Offset 60068h

Pipe A A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RESERVED (31:23), COLOR_CHANNEL_CRC_RESULT_VALUE (22:0)

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

14.10.174 CRCRESALPHAA—Offset 6006Ch

Pipe A A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6006Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

31:23	22:0
RESERVED	COLOR_CHANNEL_CRC_RESULT_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

14.10.175 CRCCTRLRESIDUE2A—Offset 60070h

Pipe A CRC Color Channel Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60070h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:23)	EXPECTED_CRC_VALUE (22:0)

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

14.10.176 CRCRESRESIDUE2A—Offset 60080h

Pipe A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:23)	COLOR_CHANNEL_CRC_RESULT_VALUE (22:0)

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

14.10.177 PSRCTLA—Offset 60090h

Pipe A Panel Self Refresh Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60090h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								IDENTICAL_FRAME_THRESHOLD								DPLLA_POWER_DOWN_DELAY					DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY	SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE	PSR_ACTIVE_ENTRY	PSR_SINGLE_FRAME_UPDATE	RESERVED_1		PSR_MODE			PSR_RESET	PSR_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**IDENTICAL_FRAME_THRESHOLD:** : Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
15:11	0b RW	**DPLLA_POWER_DOWN_DELAY:** programmable delay from main link powerdown to DPLLA powerdown. The delay is in number of cdclk clocks.
10	0b RW	**DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY:** . If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
9	0b RW	**SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE:** . If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with Source transmitter state in PSR active bit in DPCD register of the sink.
8	0b RW	**PSR_ACTIVE_ENTRY:** This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
7	0b RW	**PSR_SINGLE_FRAME_UPDATE:** In PSR persistent mode, SW set this bit before writing registers for a flip. After HW finishes signle frame update, it goes back to PSR active ? no RFB state. SW driver may send new single frame update request. Programming note: Reading this bit is updated at the next vblank. Writing this bit to 1 will cause PSR FSM to perform single frame update automatically, no vblank is required. When single frame update is done, it will automatically go back to PSR active ? no RFB update. 60094[2:0] = 3b011.
6:5	0b RW	**RESERVED_1:** Reserved.
4:2	0b RW	**PSR_MODE:** b011-111: reserved. b010: PSR with HW timer. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: PSR with SW timer. In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point. b000: PSR manual (debug) mode. All of PSR state transitions and SDP content is managed by SW driver. SW is responsible to change SDP content for every frame with appropriate values to keep PSR panel in synchronized states.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**PSR_RESET:** If assert all PSR functions are reset back to PSR inactive state. When it needs to resynchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
0	0b RW	**PSR_ENABLE:** Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

14.10.178 PSRSTATA—Offset 60094h

Pipe A PSR status register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60094h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DISPLAY_LOCAL_STANDBY_STATE | RESERVED | REPEAT_FRAME_COUNTER | RESERVED_1 | SDP_SENT | PSR_IN_TRANSITION | RESERVED_2 | PSR_LAST_STATE | PSR_CURRENT_STATE

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RO	**DISPLAY_LOCAL_STANDBY_STATE:** :00: D0 idle state, fetch frame buffer from system memory 01: D0i1 not defined in VLVP 02: D0i2 PSR is active, display controller is trunk gated 03: D0i3 PSR is active, display controller is power gated
29:24	0b RO	**RESERVED:** Reserved.
23:16	0b RO	**REPEAT_FRAME_COUNTER:** : Number of identical frames has been sent by display controller. Value is not roll over at 255.
15:9	0b RO	**RESERVED_1:** Reserved.
8	0b RO	**SDP_SENT:** it indicates if SDP packet has been sent in current frame.
7	0b RO	**PSR_IN_TRANSITION:** There is a period that source already committed to PSR active but sink did not. SW should not change the source state at this time but wait until this status bit is clear. The wait time should in the range of 120-250us in the worst case.

Bit Range	Default & Access	Field Name (ID): Description
6	0b RO	**RESERVED_2:** Reserved.
5:3	0b RO	**PSR_LAST_STATE:** indicate last source state that VLVP PSR state machine were in (debug) 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit
2:0	0b RO	**PSR_CURRENT_STATE:** indicate current source state that VLVP PSR state machine are in 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit

14.10.179 PSRCRC1A—Offset 60098h

Pipe A PSR CRC1 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60098h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRC_VALUE_BITS_15_0_OF_R_COMPONENT

RESERVED

CRC_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RO	**CRC_VALUE_BITS_15_0_OF_R_COMPONENT:** crc values bits 15 to 0 of Red component

Bit Range	Default & Access	Field Name (ID): Description
15:1	0b RO	**RESERVED:** Reserved.
0	0b RO	**CRC_VALID:** CRC calculation complete and valid for previous frame.

14.10.180 PSRCRC2A—Offset 6009Ch

Pipe A PSR CRC2 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6009Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRC_VALUE_BITS_15_0_OF_B_COMPONENT (bits 31:16); CRC_VALUE_BITS_15_0_OF_G_COMPONENT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RO	**CRC_VALUE_BITS_15_0_OF_B_COMPONENT:** crc values bits 15 to 0 of Blue component
15:0	0b RO	**CRC_VALUE_BITS_15_0_OF_G_COMPONENT:** crc values bits 15 to 0 of green component

14.10.181 VSCSDPA—Offset 600A0h

Pipe A VSC SDP register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 600A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SDP_SEND_FREQUENCY		RESERVED														DB1								DB0							

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**SDP_SEND_FREQUENCY:** 00: off, not sending 01: send one every frame 10: send once 11: reserved Programming note: This field shall be programmed either send once or send one every frame when SW driver sets PSR active entry bit. When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
29:16	0b RW	**RESERVED:** Reserved.
15:8	0b RW	**DB1:** : Programmed by display driver in manual mode, auto-generate by display controller in all other modes
7:0	0b RW	**DB0:** : Bits 7:4: Stereo Interface Method Specific ParameterBits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

14.10.182 PIPEAWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS —Offset 600B0h

When color correction matrix enable bit is set in PIPEACONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix like gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 600B0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				C01_COEFFICIENT												RESERVED_1				C00_COEFFICIENT											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C01_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C00_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.10.183 PIPEAWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 600B4h

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 600B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																				C02_COEFFICIENT											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C02_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.10.184 PIPEAWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS —Offset 600B8h

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 600B8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				C11_COEFFICIENT												RESERVED_1				C10_COEFFICIENT											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C11_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C10_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.10.185 PIPEAWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT— Offset 600BCh

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 600BCh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																				C12_COEFFICIENT											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C12_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.10.186 PIPEAWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS —Offset 600C0h

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 600C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				C21_COEFFICIENT												RESERVED_1				C20_COEFFICIENT											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C21_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C20_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.10.187 PIPEAWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 600C4h

Refer to the description of the Pipe A Wide Gamut Color Correction C01_C00 register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 600C4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:0
RESERVED	C22_COEFFICIENT

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C22_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.10.188 VIDEO_DIP_CTL_A—Offset 60200h

Video DIP Control for Pipe A

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 20200900h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0

ENABLE_GRAPHICS_DATA_ISLAND_PACKET | PORT_SELECT | RESERVED | GCP_DIP_ENABLE | DATA_ISLAND_PACKET_TYPE_ENABLE | DIP_BUFFER_INDEX | RESERVED_1 | VIDEO_DIP_TRANSMISSION_FREQUENCY | RESERVED_2 | VIDEO_DIP_BUFFER_SIZE | RESERVED_3 | VIDEO_DIP_RAM_ACCESS_ADDRESS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_GRAPHICS_DATA_ISLAND_PACKET:** mode (bit #9 of port control register) overrides this behavior.
30:29	01b RW	**PORT_SELECT:** Project: All Default Value: 01b Digital Port B This selects which port is to transmit the data island. This field must not be changed while data island transmission is enabled. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B (Default) All 10b Digital Port C Digital Port C All 11b Reserved Reserved All
28:26	0b RW	**RESERVED:** Project: All Format:
25	0b RW	**GCP_DIP_ENABLE:** Project: All Default Value: 0b This bit enables the output of the General Control Packet. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore a DIP buffer for GCP is not needed. Please refer to the GCP payload register for payload details. Writes to this bit take effect immediately. This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode. Value Name Description Project 0b Disable GCP DIP disabled All 1b Enable GCP DIP enabled All
24:21	0001b RW	**DATA_ISLAND_PACKET_TYPE_ENABLE:** Project: All Default Value: 0001b Enable AVI DIP These bits enable the output of a given data island packet (DIP) type. It can be updated while the port is enabled and is immediately updated (not double-buffered). Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Value Name Description Project XXX1b Enable AVI Enable AVI DIP (Default = enabled) All XX1Xb Enable Vendor Enable Vendor-specific DIP (Default = disabled) All X1XXb Enable Gamut Enable Gamut Metadata Packet (Default = disabled) All 1XXXb Enable Source Enable Source Product Description DIP (Default = disabled) All

Bit Range	Default & Access	Field Name (ID): Description
20:19	0b RW	**DIP_BUFFER_INDEX:** Project: All Default Value: 00b This field is used during programming of different DIPs. These bits are used as an index to their respective DIP buffers. The transmission frequency must also be written when programming the buffer. Value Name Description Project 00b AVI AVI DIP (31 bytes of space available) All 01b Vendor-specific Vendor-specific DIP All 10b Reserved Reserved All 11b Source Product Source Product Description DIP All
18	0b RW	**RESERVED_1:** Project: All Format:
17:16	0b RW	**VIDEO_DIP_TRANSMISSION_FREQUENCY:** Project: All Default Value: 00b These bits dictate the frequency of Video DIP transmission for the DIP buffer index designated in bits 20:19. When writing Video DIP data, this value is also latched when the first DW of the Video DIP is written. When read, this value reflects the Video DIP transmission frequency for the Video DIP buffer designated in bits 20:19. This field shall be ignored for Gamut Metadata Packet transmission. Value Name Description Project 00b Send Once Send Once All 01b Every VSync Send Every VSync (Default for AVI) All 10b Every Other Vsync Send at least every other VSync All 11b Reserved Reserved All
15:12	0b RW	**RESERVED_2:** Project: All Format: MBZ
11:8	1001b RO	**VIDEO_DIP_BUFFER_SIZE:** Project: All AccessType: Read Only Default Value: ;1001b This reflects the buffer size in dwords available for the type of Video DIP being indexed by bits 20:19 of this register, including the header. It is hardwired to the maximum size of a Video DIP, 36 bytes. Please note that this count includes ECC bytes, which are not writable by software. These bits are immediately valid after write of the DIP index.
7:4	0b RW	**RESERVED_3:** Project: All Format: MBZ
3:0	0b RO	**VIDEO_DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read Only Selects the DWORD address for access to the Video DIP buffers. This value is automatically incremented after each read or write of the Video DIP Data Register. The value wraps back to zero when it autoincrements past the max address value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

14.10.189 VIDEO_DIP_DATA_A—Offset 60208h

Video Data Island Packet Data for Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60208h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VIDEO_DIP_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**VIDEO_DIP_DATA:** Project: All When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis.

14.10.190 VIDEO_DIP_GDCP_PAYLOAD_A—Offset 60210h

Video Data Island Payload for Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 60210h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | GCP_COLOR_INDICATION | GCP_DEFAULT_PHASE_ENABLE | GCP_AV_MUTE

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**GCP_COLOR_INDICATION:** Project: All Default Value: 0b This bit must be set when in deep color mode. It may optionally be set for 24-bit mode. It must be set if the sink attached to Pipe A can receive GCP data. Value Name Description Project 0b Dont Indicate Dont indicate color depth. CD and PP bits in GCP set to zero All 1b Indicate Indicate color depth using CD bits in GCP. It will be set depending on programmed pixel depth in port control register All
1	0b RW	**GCP_DEFAULT_PHASE_ENABLE:** Project: All Default Value: 0b Indicates the video timings meet alignment requirements such that the following conditions are met: Htotal is an even number Hactive is an even number Hsync is an even number Front and back porches for Hsync are even numbers Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0) Value Name Description Project 0b Clear Default phase bit in GCP is cleared All 1b Require Met Default phase bit in GCP is set. All requirements must be met before setting this bit All
0	0b RW	**GCP_AV_MUTE:** Project: All Default Value: 0b Set AV mute bit in GCP Value Name Description Project 0b Clear AV mute bit in GCP is cleared. When this bit transitions to 0, the AV mute clear flag is sent in the next GCP packet All 1b Set AV mute bit in GCP is set. When this bit transitions to 1, the AV mute set flag is sent in the next GCP packet All

14.10.191 HTOTAL_B—Offset 61000h

Pipe B Horizontal Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED			PIPE_B_HORIZONTAL_TOTAL_DISPLAY													RESERVED_1				PIPE_B_HORIZONTAL_ACTIVE_DISPLAY											

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_HORIZONTAL_TOTAL_DISPLAY:** See pipe A description.
15:12	0b RW	**RESERVED_1:** Write as zero.
11:0	0b RW	**PIPE_B_HORIZONTAL_ACTIVE_DISPLAY:** See pipe A description

14.10.192 HBLANK_B—Offset 61004h

Pipe B Horizontal Blank Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED			PIPE_B_HORIZONTAL_BLANK_END													RESERVED_1			PIPE_B_HORIZONTAL_BLANK_START												

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** . Write as zero.
28:16	0b RW	**PIPE_B_HORIZONTAL_BLANK_END:** See pipe A description
15:13	0b RW	**RESERVED_1:** Write as zero.
12:0	0b RW	**PIPE_B_HORIZONTAL_BLANK_START:** See pipe A description.

14.10.193 HSYNC_B—Offset 61008h

Pipe B Horizontal Sync Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED			PIPE_B_HORIZONTAL_SYNC_END													RESERVED_1			PIPE_B_HORIZONTAL_SYNC_START												

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_HORIZONTAL_SYNC_END:** See pipe A description.
15:13	0b RW	**RESERVED_1:** Write as zero.
12:0	0b RW	**PIPE_B_HORIZONTAL_SYNC_START:** See pipe A description

14.10.194 VTOTAL_B—Offset 6100Ch

Pipe B Vertical Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6100Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31–29	28–16	15–12	11–0
RESERVED	PIPE_B_VERTICAL_TOTAL_DISPLAY	RESERVED_1	PIPE_B_VERTICAL_ACTIVE_DISPLAY

Bits: 31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_VERTICAL_TOTAL_DISPLAY:** See pipe A description.
15:12	0b RW	**RESERVED_1:** Write as zero.
11:0	0b RW	**PIPE_B_VERTICAL_ACTIVE_DISPLAY:** See pipe A description.

14.10.195 VBLANK_B—Offset 61010h

Pipe B Vertical Blank Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31–29	28–16	15–13	12–0
RESERVED	PIPE_B_VERTICAL_BLANK_END	RESERVED_1	PIPE_B_VERTICAL_BLANK_START

Bits: 31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_VERTICAL_BLANK_END:** See pipe A description.
15:13	0b RW	**RESERVED_1:** Write as zero.
12:0	0b RW	**PIPE_B_VERTICAL_BLANK_START:** See pipe A description.

14.10.196 VSYNC_B—Offset 61014h

Pipe B Vertical Sync Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED | PIPE_B_VERTICAL_SYNC_END | RESERVED_1 | PIPE_B_VERTICAL_SYNC_START

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Write as zero.
28:16	0b RW	**PIPE_B_VERTICAL_SYNC_END:** See pipe A description.
15:13	0b RW	**RESERVED_1:** Write as zero.
12:0	0b RW	**PIPE_B_VERTICAL_SYNC_START:** See pipe A description.

14.10.197 PIPEBSRC—Offset 6101Ch

Pipe B Source Image Size

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6101Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED	PIPE_B_HORIZONTAL_SOURCE_IMAGE_SIZE	RESERVED_1	PIPE_B_VERTICAL_SOURCE_IMAGE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PIPE_B_HORIZONTAL_SOURCE_IMAGE_SIZE:** See pipe A description.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PIPE_B_VERTICAL_SOURCE_IMAGE_SIZE:** See pipe A description.

14.10.198 BCLRPAT_B—Offset 61020h

Pipe B Border Color Pattern Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
RESERVED	PIPE_B_RED_CHANNEL_COLOR_VALUE	PIPE_B_GREEN_CHANNEL_COLOR_VALUE	PIPE_B_BLUE_CHANNEL_COLOR_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**PIPE_B_RED_CHANNEL_COLOR_VALUE:** pipeB red color channel values
15:8	0b RW	**PIPE_B_GREEN_CHANNEL_COLOR_VALUE:** pipeB green color channel values
7:0	0b RW	**PIPE_B_BLUE_CHANNEL_COLOR_VALUE:** pipeB blue color channel values

14.10.199 VSYNCSHIFT_B—Offset 61028h

Vertical Sync Shift Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:13: RESERVED
Bits 12:0: PIPE_B_SECOND_FIELD_VERTICAL_SYNC_SHIFT

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**RESERVED:** Write as zero.
12:0	0b RW	**PIPE_B_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEBCONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

14.10.200 TRANSBDATAM1—Offset 61030h

Pipe B Data M value 1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61030h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 7E000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | TU1_SIZE | RESERVED_1 | PIPE_B_DATA_M1_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:25	111111b RW	**TU1_SIZE:** Project: All Default Value: ;111111b 64 See Pipe A description.
24	0b RW	**RESERVED_1:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_DATA_M1_VALUE:** Project: All See Pipe A description.

14.10.201 TRANSBDATAN1—Offset 61034h

Pipe B Data N value 1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61034h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | PIPE_B_DATA_N1_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
23:0	0b RW	**PIPE_B_DATA_N1_VALUE:** Project: All See Pipe A description.

14.10.202 TRANSBDATAM2—Offset 61038h

Pipe B Data M value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61038h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 7E000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED	TU2_SIZE						RESERVED_1	PIPE_B_DATA_M2_VALUE																							

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:25	111111b RW	**TU2_SIZE:** Project: All Default Value: ;111111b 64 See Pipe A description.
24	0b RW	**RESERVED_1:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_DATA_M2_VALUE:** Project: All See Pipe A description.

14.10.203 TRANSBDATAN2—Offset 6103Ch

Pipe B Data N value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6103Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RESERVED | PIPE_B_DATA_N2_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_DATA_N2_VALUE:** Project: All See Pipe A description.

14.10.204 TRANSBDPLINKM1—Offset 61040h

Pipe B Link M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RESERVED | PIPE_B_LINK_M1_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_LINK_M1_VALUE:** Project: All See Pipe A description.

14.10.205 TRANSBDPLINKN1—Offset 61044h

Pipe B Link N value 1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED (31:24) | PIPE_B_LINK_N1_VALUE (23:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_LINK_N1_VALUE:** Project: All See Pipe A description.

14.10.206 TRANSBDPLINKM2—Offset 61048h

Pipe B Link M value 2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED (31:24) | PIPE_B_LINK_M2_VALUE (23:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_LINK_M2_VALUE:** Project: All See Pipe A description.

14.10.207 TRANSBDPLINKN2—Offset 6104Ch

Pipe B Link N value 2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6104Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED

PIPE_B_LINK_N2_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Project: All Format: MBZ
23:0	0b RW	**PIPE_B_LINK_N2_VALUE:** Project: All See Pipe A description.

14.11 Memory Mapped Registers (2 of 2)

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
61050–61053h	4	"CRCCTRLREDB—Offset 61050h" on page 652	00000000h
61054–61057h	4	"CRCCTRLGREENB—Offset 61054h" on page 653	00000000h
61058–6105Bh	4	"CRCCTRLBLUEB—Offset 61058h" on page 654	00000000h
6105C–6105Fh	4	"CRCCTRLALPHAB—Offset 6105Ch" on page 655	00000000h
61060–61063h	4	"CRCRESREDB—Offset 61060h" on page 655	00000000h
61064–61067h	4	"CRCRESGREENB—Offset 61064h" on page 656	00000000h
61068–6106Bh	4	"CRCRESBLUEB—Offset 61068h" on page 657	00000000h
6106C–6106Fh	4	"CRCRESALPHAB—Offset 6106Ch" on page 658	00000000h
61070–61073h	4	"CRCCTRLRESIDUE2B—Offset 61070h" on page 658	00000000h
61080–61083h	4	"CRCRESRESIDUAL2B—Offset 61080h" on page 659	00000000h
61090–61093h	4	"PSRCTLB—Offset 61090h" on page 660	00000000h
61094–61097h	4	"PSRSTATB—Offset 61094h" on page 661	00000000h
61098–6109Bh	4	"PSRCRC1B—Offset 61098h" on page 662	00000000h
6109C–6109Fh	4	"PSRCRC2B—Offset 6109Ch" on page 663	00000000h
610A0–610A3h	4	"VSCSDPB—Offset 610A0h" on page 664	00000000h
610B0–610B3h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 610B0h" on page 665	00000000h
610B4–610B7h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 610B4h" on page 666	00000000h
610B8–610BBh	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 610B8h" on page 666	00000000h
610BC–610BFh	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 610BCh" on page 667	00000000h
610C0–610C3h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 610C0h" on page 668	00000000h
610C4–610C7h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 610C4h" on page 668	00000000h
61100–61103h	4	"ADPA—Offset 61100h" on page 669	00040000h
61104–61107h	4	"CRTIO_DFX—Offset 61104h" on page 672	00008000h
61110–61113h	4	"PORT_HOTPLUG_EN—Offset 61110h" on page 672	00000020h
61114–61117h	4	"PORT_HOTPLUG_STAT—Offset 61114h" on page 675	00000000h
61140–61143h	4	"SDVOHDMIB—Offset 61140h" on page 679	00000018h
61154–61157h	4	"SDVOHDMIB—Offset 61140h" on page 679	00000000h
61160–61163h	4	"HDMIC—Offset 61160h" on page 684	00000018h
61164–61167h	4	"DISPLAY_DIGITAL_PORT_HOT_PLUG_CONTROL_REGISTER—Offset 61164h" on page 688	00000000h
61168–6116Bh	4	"DV_DETERM—Offset 61168h" on page 690	00000000h
61170–61173h	4	"VIDEO_DIP_CTL_B—Offset 61170h" on page 691	20200900h
61174–61177h	4	"VIDEO_DIP_DATA_B—Offset 61174h" on page 693	00000000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
61178–6117Bh	4	"VIDEO_DIP_GDCP_PAYLOAD_B—Offset 61178h" on page 693	00000000h
61190–61193h	4	"MIPIA_PORT_CTRL—Offset 61190h" on page 694	00000000h
61194–61197h	4	"MIPIA_TEARING_CTR—Offset 61194h" on page 697	00000000h
61198–6119Bh	4	"DPA_PIX_GEN_CTRL—Offset 61198h" on page 698	00000000h
611A0–611A3h	4	"MIPIA_AUTOPWG—Offset 611A0h" on page 699	00000000h
611B0–611B3h	4	"DPB_PIX_GEN_CTRL—Offset 611B0h" on page 699	00000000h
61200–61203h	4	"PIPEA_PP_STATUS—Offset 61200h" on page 701	08000000h
61204–61207h	4	"PIPEA_PP_CONTROL—Offset 61204h" on page 702	00000000h
61208–6120Bh	4	"PIPEA_PP_ON_DELAYS—Offset 61208h" on page 704	00000000h
6120C–6120Fh	4	"PIPEA_PP_OFF_DELAYS—Offset 6120Ch" on page 705	00000000h
61210–61213h	4	"PIPEA_PP_DIVISOR—Offset 61210h" on page 706	00270F04h
61230–61233h	4	"PFIT_CONTROL—Offset 61230h" on page 707	20000000h
61234–61237h	4	"PFIT_PGM_RATIOS—Offset 61234h" on page 709	00000000h
61238–6123Bh	4	"RESERVEDUSEDTOBEAUTOSCALINGRATIOSREADBACK—Offset 61238h" on page 710	00000000h
6123C–6123Fh	4	"RESERVEDUSEDTOBESCALINGINITIALPHASE—Offset 6123Ch" on page 710	00000000h
61250–61253h	4	"PIPEA_BLC_PWM_CLT2—Offset 61250h" on page 711	00000000h
61254–61257h	4	"PIPEA_BLC_PWM_CTL—Offset 61254h" on page 712	00000000h
61260–61263h	4	"PIPEA_BLM_HIST_CTL—Offset 61260h" on page 713	00000000h
61264–61267h	4	"PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61264h" on page 714	00000000h
61268–6126Bh	4	"PIPEAHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61268h" on page 715	00000000h
61300–61303h	4	"PIPEB_PP_STATUS—Offset 61300h" on page 716	08000000h
61304–61307h	4	"PIPEB_PP_CONTROL—Offset 61304h" on page 718	00000000h
61308–6130Bh	4	"PIPEB_PP_ON_DELAYS—Offset 61308h" on page 720	00000000h
6130C–6130Fh	4	"PIPEB_PP_OFF_DELAYS—Offset 6130Ch" on page 721	00000000h
61310–61313h	4	"PIPEB_PP_DIVISOR—Offset 61310h" on page 722	00270F04h
61350–61353h	4	"PIPEB_BLC_PWM_CLT2—Offset 61350h" on page 723	00000000h
61354–61357h	4	"PIPEB_BLC_PWM_CTL—Offset 61354h" on page 724	00000000h
61360–61363h	4	"PIPEB_BLM_HIST_CTL—Offset 61360h" on page 725	00000000h
61364–61367h	4	"PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61364h" on page 726	00000000h
61368–6136Bh	4	"PIPEBHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61368h" on page 727	00000000h
61700–61703h	4	"MIPIC_PORT_CTRL—Offset 61700h" on page 728	00000000h
61704–61707h	4	"MIPIC_TEARING_CTR—Offset 61704h" on page 729	00000000h
62000–62003h	4	"AUD_CONFIG_A—Offset 62000h" on page 730	00000000h
62010–62013h	4	"AUD_MISC_CTRL_A—Offset 62010h" on page 731	00000044h
62020–62023h	4	"AUD_VID_DID—Offset 62020h" on page 732	80862882h
62024–62027h	4	"AUD_RID—Offset 62024h" on page 733	00100000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
62028–6202Bh	4	“AUD_CTS_ENABLE_A—Offset 62028h” on page 734	00000000h
6204C–6204Fh	4	“AUD_PWRST—Offset 6204Ch” on page 735	00FFFFFFh
62050–62053h	4	“AUD_HDMIW_HDMIEDID_A—Offset 62050h” on page 737	00000000h
62054–62057h	4	“AUD_HDMIW_INFOFR_A—Offset 62054h” on page 738	00000000h
6207C–6207Fh	4	“AUD_PORT_EN_HD_CFG—Offset 6207Ch” on page 738	00077003h
62080–62083h	4	“AUD_OUT_DIG_CNVT_A—Offset 62080h” on page 740	00000000h
62084–62087h	4	“AUD_OUT_STR_DESC_A—Offset 62084h” on page 742	00000032h
62088–6208Bh	4	“AUD_OUT_CH_STR—Offset 62088h” on page 743	00000000h
620A8–620ABh	4	“AUD_PINW_CONNLNG_LIST—Offset 620A8h” on page 744	00030202h
620AC–620AFh	4	“AUD_PINW_CONNLNG_SEL—Offset 620ACh” on page 745	00000000h
620B4–620B7h	4	“AUD_CNTL_ST_A—Offset 620B4h” on page 746	00005400h
620C0–620C3h	4	“AUD_CNTL_ST2—Offset 620C0h” on page 748	00000000h
620D4–620D7h	4	“AUD_HDMIW_STATUS—Offset 620D4h” on page 749	00000000h
62100–62103h	4	“AUD_CONFIG_B—Offset 62100h” on page 751	00000000h
62110–62113h	4	“AUD_MISC_CTRL_B—Offset 62110h” on page 752	00000044h
62128–6212Bh	4	“AUD_CTS_ENABLE_B—Offset 62128h” on page 753	00000000h
62150–62153h	4	“AUD_HDMIW_HDMIEDID_B—Offset 62150h” on page 754	00000000h
62154–62157h	4	“AUD_HDMIW_INFOFR_B—Offset 62154h” on page 755	00000000h
62180–62183h	4	“AUD_OUT_DIG_CNVT_B—Offset 62180h” on page 755	00000000h
62184–62187h	4	“AUD_OUT_STR_DESC_B—Offset 62184h” on page 757	00000032h
621B4–621B7h	4	“AUD_CNTL_ST_B—Offset 621B4h” on page 758	00005400h
62F00–62F03h	4	“AUD_SSID_DBG—Offset 62F00h” on page 760	80860101h
62F04–62F07h	4	“AUD_PWST1_DBG—Offset 62F04h” on page 761	00000C0Fh
62F08–62F0Bh	4	“AUD_OUT_STR_DESC_A_DBG—Offset 62F08h” on page 762	00000032h
62F0C–62F0Fh	4	“AUD_OUT_DIG_CNVT_A_DBG—Offset 62F0Ch” on page 763	00000001h
62F14–62F17h	4	“AUD_PWST2_DBG—Offset 62F14h” on page 765	0000000Fh
62F18–62F1Bh	4	“AUD_OUT_STR_DESC_B_DBG—Offset 62F18h” on page 766	00000032h
62F1C–62F1Fh	4	“AUD_OUT_DIG_CNVT_B_DBG—Offset 62F1Ch” on page 767	00000001h
62F20–62F23h	4	“AUD_PORT_EN_B_DBG—Offset 62F20h” on page 769	00000003h
62F24–62F27h	4	“AUD_PWST3_DBG—Offset 62F24h” on page 771	00000003h
62F28–62F2Bh	4	“AUD_PORT_EN_C_DBG—Offset 62F28h” on page 771	00000003h
62F2C–62F2Fh	4	“AUD_PORT_EN_D_DBG—Offset 62F2Ch” on page 773	00000003h
62F38–62F3Bh	4	“AUD_CHICKENBIT_REG—Offset 62F38h” on page 774	00000001h
62F40–62F43h	4	“AUD_OUT_DIG_CNVTA_DBG—Offset 62F40h” on page 775	00000000h
62F44–62F47h	4	“AUD_OUT_DIG_CNVTB_DBG—Offset 62F44h” on page 776	00000000h
62F60–62F63h	4	“AUD_CNTL_ST_B_DBG—Offset 62F60h” on page 776	00000000h
62F64–62F67h	4	“AUD_HDMIW_INFOFR_B_DBG—Offset 62F64h” on page 777	00000000h
62F70–62F73h	4	“AUD_CNTL_ST_C_DBG—Offset 62F70h” on page 778	00000000h
62F74–62F77h	4	“AUD_HDMIW_INFOFR_C_DBG—Offset 62F74h” on page 779	00000000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
62F80–62F83h	4	"AUD_CNTL_ST_D_DBG—Offset 62F80h" on page 780	00000000h
62F84–62F87h	4	"AUD_HDMIW_INFOFR_D_DBG—Offset 62F84h" on page 781	00000000h
62F88–62F8Bh	4	"AUD_CONFIG_DEFAULT2_REG_PORTB—Offset 62F88h" on page 782	00000000h
62F8C–62F8Fh	4	"AUD_CONFIG_DEFAULT2_REG_PORTC—Offset 62F8Ch" on page 783	00000000h
62F90–62F93h	4	"AUD_CONFIG_DEFAULT2_REG_PORTD—Offset 62F90h" on page 783	00000000h
62F94–62F97h	4	"AUD_MCTSA—Offset 62F94h" on page 784	00000000h
62F98–62F9Bh	4	"AUD_MCTSB—Offset 62F98h" on page 784	00000000h
64100–64103h	4	"DP_B—Offset 64100h" on page 785	00000018h
64110–64113h	4	"DPB_AUX_CH_CTL—Offset 64110h" on page 788	00050000h
64114–64117h	4	"DPB_AUX_CH_DATA1—Offset 64114h" on page 789	00000000h
64118–6411Bh	4	"DPB_AUX_CH_DATA2—Offset 64118h" on page 790	00000000h
6411C–6411Fh	4	"DPB_AUX_CH_DATA3—Offset 6411Ch" on page 791	00000000h
64120–64123h	4	"DPB_AUX_CH_DATA4—Offset 64120h" on page 791	00000000h
64124–64127h	4	"DPB_AUX_CH_DATA5—Offset 64124h" on page 792	00000000h
64130–64133h	4	"DP_AUX_CH_AKSV_HI—Offset 64130h" on page 792	00000000h
64134–64137h	4	"DP_AUX_CH_AKSV_LO—Offset 64134h" on page 793	00000000h
64150–64153h	4	"DPB_AUX_TST—Offset 64150h" on page 794	00000000h
64200–64203h	4	"DP_C—Offset 64200h" on page 796	00000018h
64210–64213h	4	"DPC_AUX_CH_CTL—Offset 64210h" on page 798	00050000h
64214–64217h	4	"DPC_AUX_CH_DATA1—Offset 64214h" on page 800	00000000h
64218–6421Bh	4	"DPC_AUX_CH_DATA2—Offset 64218h" on page 800	00000000h
6421C–6421Fh	4	"DPC_AUX_CH_DATA3—Offset 6421Ch" on page 801	00000000h
64220–64223h	4	"DPC_AUX_CH_DATA4—Offset 64220h" on page 802	00000000h
64224–64227h	4	"DPC_AUX_CH_DATA5—Offset 64224h" on page 802	00000000h
64228–6422Bh	4	"DPC_AUX_TST—Offset 64228h" on page 803	00000000h
65000–65003h	4	"STREAM_A_LPE_AUD_CONFIG—Offset 65000h" on page 805	00000280h
65008–6500Bh	4	"STREAM_A_LPE_AUD_CH_STATUS_0—Offset 65008h" on page 807	00000000h
6500C–6500Fh	4	"STREAM_A_LPE_AUD_CH_STATUS_1—Offset 6500Ch" on page 807	00000000h
65010–65013h	4	"STREAM_A_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65010h" on page 808	00000000h
65014–65017h	4	"STREAM_A_LPE_AUD_HDMI_N_DP_NAUD—Offset 65014h" on page 809	00000000h
65020–65023h	4	"STREAM_A_LPE_AUD_BUFFER_CONFIG—Offset 65020h" on page 810	00000100h
65024–65027h	4	"STREAM_A_LPE_AUD_BUF_CH_SWP—Offset 65024h" on page 810	00FAC688h
65040–65043h	4	"STREAM_A_LPE_AUD_BUF_A_ADDR—Offset 65040h" on page 812	00000000h
65044–65047h	4	"STREAM_A_LPE_AUD_BUF_A_LENGTH—Offset 65044h" on page 812	00000000h
65048–6504Bh	4	"STREAM_A_LPE_AUD_BUF_B_ADDR—Offset 65048h" on page 813	00000000h
6504C–6504Fh	4	"STREAM_A_LPE_AUD_BUF_B_LENGTH—Offset 6504Ch" on page 814	00000000h
65050–65053h	4	"STREAM_A_LPE_AUD_BUF_C_ADDR—Offset 65050h" on page 814	00000000h
65054–65057h	4	"STREAM_A_LPE_AUD_BUF_C_LENGTH—Offset 65054h" on page 815	00000000h
65058–6505Bh	4	"STREAM_A_LPE_AUD_BUF_D_ADDR—Offset 65058h" on page 815	00000000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6505C–6505Fh	4	"STREAM_A_LPE_AUD_BUF_D_LENGTH—Offset 6505Ch" on page 816	00000000h
65060–65063h	4	"STREAM_A_LPE_AUD_CNTL_ST—Offset 65060h" on page 817	00000000h
65064–65067h	4	"STREAM_A_LPE_AUD_HDMI_STATUS—Offset 65064h" on page 818	00000000h
65068–6506Bh	4	"STREAM_A_LPE_AUD_HDMIW_INFOFR—Offset 65068h" on page 820	00000000h
65800–65803h	4	"STREAM_B_LPE_AUD_CONFIG—Offset 65800h" on page 821	00000280h
65808–6580Bh	4	"STREAM_B_LPE_AUD_CH_STATUS_0—Offset 65808h" on page 823	00000000h
6580C–6580Fh	4	"STREAM_B_LPE_AUD_CH_STATUS_1—Offset 6580Ch" on page 823	00000000h
65810–65813h	4	"STREAM_B_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65810h" on page 824	00000000h
65814–65817h	4	"STREAM_B_LPE_AUD_HDMI_N_DP_NAUD—Offset 65814h" on page 825	00000000h
65820–65823h	4	"STREAM_B_LPE_AUD_BUFFER_CONFIG—Offset 65820h" on page 826	00000100h
65824–65827h	4	"STREAM_B_LPE_AUD_BUF_CH_SWP—Offset 65824h" on page 826	00FAC688h
65840–65843h	4	"STREAM_B_LPE_AUD_BUF_A_ADDR—Offset 65840h" on page 828	00000000h
65844–65847h	4	"STREAM_B_LPE_AUD_BUF_A_LENGTH—Offset 65844h" on page 828	00000000h
65848–6584Bh	4	"STREAM_B_LPE_AUD_BUF_B_ADDR—Offset 65848h" on page 829	00000000h
6584C–6584Fh	4	"STREAM_B_LPE_AUD_BUF_B_LENGTH—Offset 6584Ch" on page 830	00000000h
65850–65853h	4	"STREAM_B_LPE_AUD_BUF_C_ADDR—Offset 65850h" on page 830	00000000h
65854–65857h	4	"STREAM_B_LPE_AUD_BUF_C_LENGTH—Offset 65854h" on page 831	00000000h
65858–6585Bh	4	"STREAM_B_LPE_AUD_BUF_D_ADDR—Offset 65858h" on page 831	00000000h
6585C–6585Fh	4	"STREAM_B_LPE_AUD_BUF_D_LENGTH—Offset 6585Ch" on page 832	00000000h
65860–65863h	4	"STREAM_B_LPE_AUD_CNTL_ST—Offset 65860h" on page 833	00000000h
65864–65867h	4	"STREAM_B_LPE_AUD_HDMI_STATUS—Offset 65864h" on page 835	00000000h
65868–6586Bh	4	"STREAM_B_LPE_AUD_HDMIW_INFOFR—Offset 65868h" on page 836	00000000h
70000–70003h	4	"PIPEA_DSL—Offset 70000h" on page 837	00000000h
70004–70007h	4	"PIPEA_SLC—Offset 70004h" on page 838	00000000h
70008–7000Bh	4	"PIPEACONF—Offset 70008h" on page 839	00000000h
70010–70013h	4	"PIPEAGCMAXRED—Offset 70010h" on page 843	00010000h
70014–70017h	4	"PIPEAGCMAXGREEN—Offset 70014h" on page 844	00010000h
70018–7001Bh	4	"PIPEAGCMAXBLUE—Offset 70018h" on page 845	00010000h
70024–70027h	4	"PIPEASTAT—Offset 70024h" on page 846	00000000h
70028–7002Bh	4	"DPFLIPSTAT—Offset 70028h" on page 850	00000000h
7002C–7002Fh	4	"DPINVGTT—Offset 7002Ch" on page 852	00000000h
70030–70033h	4	"DSPARB—Offset 70030h" on page 854	80008000h
70034–70037h	4	"FW1—Offset 70034h" on page 855	3F8F0F0Fh
70038–7003Bh	4	"FW2—Offset 70038h" on page 856	0B0F0F0Fh
7003C–7003Fh	4	"FW3—Offset 7003Ch" on page 858	00000000h
70040–70043h	4	"PIPEAFRAMECOUNT—Offset 70040h" on page 859	00000000h
70044–70047h	4	"PIPEAFLIPCOUNT—Offset 70044h" on page 860	00000000h
70048–7004Bh	4	"PIPEAMSAMISC—Offset 70048h" on page 860	00000000h
70050–70053h	4	"DDL1—Offset 70050h" on page 861	00000000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70054–70057h	4	"DDL2—Offset 70054h" on page 863	00000000h
70060–70063h	4	"DSPARB2—Offset 70060h" on page 864	00001111h
70064–70067h	4	"DSPHOWM—Offset 70064h" on page 865	00000000h
70068–7006Bh	4	"DSPHOWM1—Offset 70068h" on page 867	00000000h
70070–70073h	4	"FW4—Offset 70070h" on page 869	00040404h
70074–70077h	4	"FW5—Offset 70074h" on page 870	04040404h
70078–7007Bh	4	"FW6—Offset 70078h" on page 871	00000078h
7007C–7007Fh	4	"FW7—Offset 7007Ch" on page 872	040F040Fh
70080–70083h	4	"CURACNTR—Offset 70080h" on page 873	00000000h
70084–70087h	4	"CURABASE—Offset 70084h" on page 874	00000000h
70088–7008Bh	4	"CURAPOS—Offset 70088h" on page 876	00000000h
70090–70093h	4	"CURAPALET_0—Offset 70090h" on page 877	00000000h
70094–70097h	4	"CURAPALET_1—Offset 70094h" on page 878	00000000h
70098–7009Bh	4	"CURAPALET_2—Offset 70098h" on page 878	00000000h
7009C–7009Fh	4	"CURAPALET_3—Offset 7009Ch" on page 879	00000000h
700AC–700AFh	4	"CURALIVEBASE—Offset 700ACh" on page 880	00000000h
700C0–700C3h	4	"CURBCNTR—Offset 700C0h" on page 881	00000000h
700C4–700C7h	4	"CURBBASE—Offset 700C4h" on page 882	00000000h
700C8–700CBh	4	"CURBPOS—Offset 700C8h" on page 884	00000000h
700D0–700D3h	4	"CURBPALET_0—Offset 700D0h" on page 886	00000000h
700D4–700D7h	4	"CURBPALET_1—Offset 700D4h" on page 886	00000000h
700D8–700DBh	4	"CURBPALET_2—Offset 700D8h" on page 887	00000000h
700DC–700DFh	4	"CURBPALET_3—Offset 700DCh" on page 888	00000000h
700EC–700EFh	4	"CURBLIVEBASE—Offset 700ECh" on page 889	00000000h
7017C–7017Fh	4	"DSPAADDR—Offset 7017Ch" on page 890	00000000h
70180–70183h	4	"DSPACNTR—Offset 70180h" on page 891	00000000h
70184–70187h	4	"DSPALINOFF—Offset 70184h" on page 894	00000000h
70188–7018Bh	4	"DSPASTRIDE—Offset 70188h" on page 895	00000000h
70194–70197h	4	"DSPAKEYVAL—Offset 70194h" on page 896	00000000h
70198–7019Bh	4	"DSPAKEYMSK—Offset 70198h" on page 896	00000000h
7019C–7019Fh	4	"DSPASURF—Offset 7019Ch" on page 897	00000000h
701A4–701A7h	4	"DSPATILEOFF—Offset 701A4h" on page 898	00000000h
701AC–701AFh	4	"DSPASURFLIVE—Offset 701ACh" on page 899	00000000h
70400–70403h	4	"CBR1—Offset 70400h" on page 900	00000000h
70404–70407h	4	"CBR2—Offset 70404h" on page 902	00000000h
70408–7040Bh	4	"CCBR—Offset 70408h" on page 905	00000000h
7040C–7040Fh	4	"CBR3—Offset 7040Ch" on page 905	00000000h
70410–70413h	4	"SWF00—Offset 70410h" on page 907	00000000h
70414–70417h	4	"SWF01—Offset 70414h" on page 907	00000000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70418–7041Bh	4	"SWF02—Offset 70418h" on page 908	00000000h
7041C–7041Fh	4	"SWF03—Offset 7041Ch" on page 908	00000000h
70420–70423h	4	"SWF04—Offset 70420h" on page 909	00000000h
70424–70427h	4	"SWF05—Offset 70424h" on page 909	00000000h
70428–7042Bh	4	"SWF06—Offset 70428h" on page 910	00000000h
7042C–7042Fh	4	"SWF07—Offset 7042Ch" on page 910	00000000h
70430–70433h	4	"SWF08—Offset 70430h" on page 911	00000000h
70434–70437h	4	"SWF09—Offset 70434h" on page 911	00000000h
70438–7043Bh	4	"SWF0A—Offset 70438h" on page 912	00000000h
7043C–7043Fh	4	"SWF0B—Offset 7043Ch" on page 912	00000000h
70440–70443h	4	"SWF0C—Offset 70440h" on page 913	00000000h
70444–70447h	4	"SWF0D—Offset 70444h" on page 913	00000000h
70448–7044Bh	4	"SWF0E—Offset 70448h" on page 914	00000000h
7044C–7044Fh	4	"SWF0F—Offset 7044Ch" on page 914	00000000h
70450–70453h	4	"CBR4—Offset 70450h" on page 915	00000000h
71000–71003h	4	"PIPEB_DSL—Offset 71000h" on page 917	00000000h
71004–71007h	4	"PIPEB_SLC—Offset 71004h" on page 918	00000000h
71008–7100Bh	4	"PIPEBCONF—Offset 71008h" on page 919	00000000h
71010–71013h	4	"PIPEBGCMAXRED—Offset 71010h" on page 922	00010000h
71014–71017h	4	"PIPEBGCMAXGREEN—Offset 71014h" on page 923	00010000h
71018–7101Bh	4	"PIPEBGCMAXBLUE—Offset 71018h" on page 923	00010000h
71024–71027h	4	"PIPEBSTAT—Offset 71024h" on page 924	00000000h
71040–71043h	4	"PIPEBFRAMECOUNT—Offset 71040h" on page 928	00000000h
71044–71047h	4	"PIPEBFLIPCOUNT—Offset 71044h" on page 928	00000000h
71048–7104Bh	4	"PIPEBMSAMISC—Offset 71048h" on page 929	00000000h
7117C–7117Fh	4	"DSPBADDR—Offset 7117Ch" on page 930	00000000h
71180–71183h	4	"DSPBCNTR—Offset 71180h" on page 932	01000000h
71184–71187h	4	"DSPBLINOFFSET—Offset 71184h" on page 934	00000000h
71188–7118Bh	4	"DSPBSTRIDE—Offset 71188h" on page 935	00000000h
71194–71197h	4	"DSPBKEYVAL—Offset 71194h" on page 936	00000000h
71198–7119Bh	4	"DSPBKEYMSK—Offset 71198h" on page 937	00000000h
7119C–7119Fh	4	"DSPBSURF—Offset 7119Ch" on page 937	00000000h
711A4–711A7h	4	"DSPBTILEOFF—Offset 711A4h" on page 939	00000000h
711AC–711AFh	4	"DSPBSURFLIVE—Offset 711ACh" on page 940	00000000h
71200–71203h	4	"DSPBFLPQSTAT—Offset 71200h" on page 940	00000000h
71400–71403h	4	"VGACNTRL—Offset 71400h" on page 941	00000000h
71410–71413h	4	"SWF10—Offset 71410h" on page 944	00000000h
71414–71417h	4	"SWF11—Offset 71414h" on page 945	00000000h
71418–7141Bh	4	"SWF12—Offset 71418h" on page 945	00000000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7141C–7141Fh	4	"SWF13—Offset 7141Ch" on page 946	00000000h
71420–71423h	4	"SWF14—Offset 71420h" on page 946	00000000h
71424–71427h	4	"SWF15—Offset 71424h" on page 947	00000000h
71428–7142Bh	4	"SWF16—Offset 71428h" on page 947	00000000h
7142C–7142Fh	4	"SWF17—Offset 7142Ch" on page 948	00000000h
71430–71433h	4	"SWF18—Offset 71430h" on page 948	00000000h
71434–71437h	4	"SWF19—Offset 71434h" on page 949	00000000h
71438–7143Bh	4	"SWF1A—Offset 71438h" on page 949	00000000h
7143C–7143Fh	4	"SWF1B—Offset 7143Ch" on page 950	00000000h
71440–71443h	4	"SWF1C—Offset 71440h" on page 950	00000000h
71444–71447h	4	"SWF1D—Offset 71444h" on page 951	00000000h
71448–7144Bh	4	"SWF1E—Offset 71448h" on page 951	00000000h
7144C–7144Fh	4	"SWF1F—Offset 7144Ch" on page 952	00000000h
72180–72183h	4	"SPACNTR—Offset 72180h" on page 952	00000000h
72184–72187h	4	"SPALINOFF—Offset 72184h" on page 955	00000000h
72188–7218Bh	4	"SPASTRIDE—Offset 72188h" on page 956	00000000h
7218C–7218Fh	4	"SPAPOS—Offset 7218Ch" on page 956	00000000h
72190–72193h	4	"SPASIZE—Offset 72190h" on page 957	00000000h
72194–72197h	4	"SPAKEYMINVAL—Offset 72194h" on page 958	00000000h
72198–7219Bh	4	"SPAKEYMSK—Offset 72198h" on page 959	00000000h
7219C–7219Fh	4	"SPASURF—Offset 7219Ch" on page 959	00000000h
721A0–721A3h	4	"SPAKEYMAXVAL—Offset 721A0h" on page 961	00000000h
721A4–721A7h	4	"SPATILEOFF—Offset 721A4h" on page 962	00000000h
721A8–721ABh	4	"SPACONTALPHA—Offset 721A8h" on page 963	00000000h
721AC–721AFh	4	"SPALIVESURF—Offset 721ACh" on page 963	00000000h
721D0–721D3h	4	"SPACLRC0—Offset 721D0h" on page 965	01000000h
721D4–721D7h	4	"SPACLRC1—Offset 721D4h" on page 966	00000080h
721E0–721E3h	4	"SPAGAMC5—Offset 721E0h" on page 967	00C0C0C0h
721E4–721E7h	4	"SPAGAMC4—Offset 721E4h" on page 968	00808080h
721E8–721EBh	4	"SPAGAMC3—Offset 721E8h" on page 968	00404040h
721EC–721EFh	4	"SPAGAMC2—Offset 721ECh" on page 969	00202020h
721F0–721F3h	4	"SPAGAMC1—Offset 721F0h" on page 970	00101010h
721F4–721F7h	4	"SPAGAMC0—Offset 721F4h" on page 970	00080808h
72280–72283h	4	"SPBCNTR—Offset 72280h" on page 971	00000000h
72284–72287h	4	"SPBLINOFF—Offset 72284h" on page 974	00000000h
72288–7228Bh	4	"SPBSTRIDE—Offset 72288h" on page 974	00000000h
7228C–7228Fh	4	"SPBPOS—Offset 7228Ch" on page 975	00000000h
72290–72293h	4	"SPBSIZE—Offset 72290h" on page 976	00000000h
72294–72297h	4	"SPBKEYMINVAL—Offset 72294h" on page 976	00000000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
72298–7229Bh	4	"SPBKEYMSK—Offset 72298h" on page 977	00000000h
7229C–7229Fh	4	"SPBSURF—Offset 7229Ch" on page 978	00000000h
722A0–722A3h	4	"SPBKEYMAXVAL—Offset 722A0h" on page 979	00000000h
722A4–722A7h	4	"SPBTILEOFF—Offset 722A4h" on page 980	00000000h
722A8–722ABh	4	"SPBCONTALPHA—Offset 722A8h" on page 981	00000000h
722AC–722AFh	4	"SPBLIVESURF—Offset 722ACh" on page 982	00000000h
722D0–722D3h	4	"SPBCLRC0—Offset 722D0h" on page 983	01000000h
722D4–722D7h	4	"SPBCLRC1—Offset 722D4h" on page 984	00000080h
722E0–722E3h	4	"SPBGAMC5—Offset 722E0h" on page 985	00C0C0C0h
722E4–722E7h	4	"SPBGAMC4—Offset 722E4h" on page 986	00808080h
722E8–722EBh	4	"SPBGAMC3—Offset 722E8h" on page 986	00404040h
722EC–722EFh	4	"SPBGAMC2—Offset 722ECh" on page 987	00202020h
722F0–722F3h	4	"SPBGAMC1—Offset 722F0h" on page 988	00101010h
722F4–722F7h	4	"SPBGAMC0—Offset 722F4h" on page 988	00080808h
72380–72383h	4	"SPCCNTR—Offset 72380h" on page 989	00000000h
72384–72387h	4	"SPCLINOFF—Offset 72384h" on page 992	00000000h
72388–7238Bh	4	"SPCSTRIDE—Offset 72388h" on page 992	00000000h
7238C–7238Fh	4	"SPCPOS—Offset 7238Ch" on page 993	00000000h
72390–72393h	4	"SPCSIZE—Offset 72390h" on page 994	00000000h
72394–72397h	4	"SPCKEYMINVAL—Offset 72394h" on page 994	00000000h
72398–7239Bh	4	"SPCKEYMSK—Offset 72398h" on page 995	00000000h
7239C–7239Fh	4	"SPCSURF—Offset 7239Ch" on page 996	00000000h
723A0–723A3h	4	"SPCKEYMAXVAL—Offset 723A0h" on page 997	00000000h
723A4–723A7h	4	"SPCTILEOFF—Offset 723A4h" on page 998	00000000h
723A8–723ABh	4	"SPCCONTALPHA—Offset 723A8h" on page 999	00000000h
723AC–723AFh	4	"SPCLIVESURF—Offset 723ACh" on page 1000	00000000h
723D0–723D3h	4	"SPCCLRC0—Offset 723D0h" on page 1001	01000000h
723D4–723D7h	4	"SPCCLRC1—Offset 723D4h" on page 1002	00000080h
723E0–723E3h	4	"SPCGAMC5—Offset 723E0h" on page 1003	00C0C0C0h
723E4–723E7h	4	"SPCGAMC4—Offset 723E4h" on page 1004	00808080h
723E8–723EBh	4	"SPCGAMC3—Offset 723E8h" on page 1004	00404040h
723EC–723EFh	4	"SPCGAMC2—Offset 723ECh" on page 1005	00202020h
723F0–723F3h	4	"SPCGAMC1—Offset 723F0h" on page 1006	00101010h
723F4–723F7h	4	"SPCGAMC0—Offset 723F4h" on page 1006	00080808h
72414–72417h	4	"SWF30—Offset 72414h" on page 1007	00000000h
72418–7241Bh	4	"SWF31—Offset 72418h" on page 1007	00000000h
7241C–7241Fh	4	"SWF32—Offset 7241Ch" on page 1008	00000000h
72480–72483h	4	"SPDCNTR—Offset 72480h" on page 1008	00000000h
72484–72487h	4	"SPDLINOFF—Offset 72484h" on page 1011	00000000h

Table 173. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
72488–7248Bh	4	"SPDSTRIDE—Offset 72488h" on page 1012	00000000h
7248C–7248Fh	4	"SPDPOS—Offset 7248Ch" on page 1012	00000000h
72490–72493h	4	"SPDSIZE—Offset 72490h" on page 1013	00000000h
72494–72497h	4	"SPDKEYMINVAL—Offset 72494h" on page 1014	00000000h
72498–7249Bh	4	"SPDKEYMSK—Offset 72498h" on page 1015	00000000h
7249C–7249Fh	4	"SPDSURF—Offset 7249Ch" on page 1015	00000000h
724A0–724A3h	4	"SPDKEYMAXVAL—Offset 724A0h" on page 1017	00000000h
724A4–724A7h	4	"SPDTILEOFF—Offset 724A4h" on page 1018	00000000h
724A8–724ABh	4	"SPDCONTALPHA—Offset 724A8h" on page 1019	00000000h
724AC–724AFh	4	"SPDLIVESURF—Offset 724ACh" on page 1019	00000000h
724D0–724D3h	4	"SPDCLRC0—Offset 724D0h" on page 1021	01000000h
724D4–724D7h	4	"SPDCLRC1—Offset 724D4h" on page 1022	00000080h
724E0–724E3h	4	"SPDGAMC5—Offset 724E0h" on page 1023	00C0C0C0h
724E4–724E7h	4	"SPDGAMC4—Offset 724E4h" on page 1024	00808080h
724E8–724EBh	4	"SPDGAMC3—Offset 724E8h" on page 1024	00404040h
724EC–724EFh	4	"SPDGAMC2—Offset 724ECh" on page 1025	00202020h
724F0–724F3h	4	"SPDGAMC1—Offset 724F0h" on page 1026	00101010h
724F4–724F7h	4	"SPDGAMC0—Offset 724F4h" on page 1026	00080808h
73000–73003h	4	"PCSRC—Offset 73000h" on page 1027	00000000h
73004–73007h	4	"PCSTAT—Offset 73004h" on page 1029	00000000h
73008–7300Bh	4	"PCSRC2—Offset 73008h" on page 1031	00000000h
7300C–7300Fh	4	"PCSTAT2—Offset 7300Ch" on page 1033	00000000h

14.11.1 CRCCTRLREDB—Offset 61050h

Pipe B CRC Color Control Register (Red)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30:27	26:23	22:0
0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ENABLE_COLOR_CHANNEL_CRC	CRC_SOURCE_SELECT	RESERVED	EXPECTED_CRC_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_COLOR_CHANNEL_CRC:** After being enabled for the first time, you need to wait for two VBLANK events for a valid CRC result. After that, a CRC will be generated each frame. 0 = CRC Calculations are disabled 1 = CRC Calculations are enabled
30:27	0b RW	**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 0000: Pipe B (Not available when DisplayPort or TV is enabled on this pipe) [DevVLVP] 0001: sDVOB/HDMIB (30 bit format. Only select when HDMIB is set to pipe B) [DevVLVP] 0010: sDVOC/HDMIC (30 bit format. Only select when HDMIC is set to pipe B) [DevVLVP] 0011: DisplayPort D (40 bit format) [DevCTG] 0100: TV Encoder outputs (30 bit format) 0101: TV filter outputs (30 bit format) 0110: DisplayPort B (40 bit format) [DevCTG, DevCDV, DevVLVP] 0111: DisplayPort C (40 bit format) [DevCTG, DevCDV, DevVLVP] 1000: Audio DP (Audio for DisplayPort (pcdclk). Only select when Audio is on DisplayPort on Pipe B) [DevVLVP] 1001: Audio HDMI (Audio for HDMI (dotclock) Only select when Audio is on HDMI on Pipe B) Others: Reserved
26:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

14.11.2 CRCCTRLGREENB—Offset 61054h

Pipe B CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0

RESERVED (bits 31:23) | EXPECTED_CRC_VALUE (bits 22:0)

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

14.11.3 CRCCTRLBLUEB—Offset 61058h

Pipe B CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61058h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0

RESERVED (bits 31:23) | EXPECTED_CRC_VALUE (bits 22:0)

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

14.11.4 CRCCTRLALPHAB—Offset 6105Ch

Pipe B CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6105Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED									EXPECTED_CRC_VALUE																						

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

14.11.5 CRCRESREDB—Offset 61060h

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | COLOR_CHANNEL_CRC_RESULT_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

14.11.6 CRCRESGREENB—Offset 61064h

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | COLOR_CHANNEL_CRC_RESULT_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

14.11.7 CRCRESBLUEB—Offset 61068h

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:23	Bits 22:0
RESERVED	COLOR_CHANNEL_CRC_RESULT_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

14.11.8 CRCRESALPHAB—Offset 6106Ch

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6106Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				RESERVED																COLOR_CHANNEL_CRC_RESULT_VALUE											

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

14.11.9 CRCCTRLRESIDUE2B—Offset 61070h

Pipe B CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61070h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:23	22:0
RESERVED	EXPECTED_CRC_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RW	**RESERVED:** Write as zero
22:0	0b RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

14.11.10 CRCRESRESIDUAL2B—Offset 61080h

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:23	22:0
RESERVED	COLOR_CHANNEL_CRC_RESULT_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:23	0b RO	**RESERVED:** Read only

Bit Range	Default & Access	Field Name (ID): Description
22:0	0b RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

14.11.11 PSRCTLB—Offset 61090h

Pipe B Panel Self Refresh Control

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61090h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | IDENTICAL_FRAME_THRESHOLD | DPLLB_POWER_DOWN_DELAY | DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY | SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE | PSR_ACTIVE_ENTRY | PSR_SINGLE_FRAME_UPDATE | RESERVED_1 | PSR_MODE | PSR_RESET | PSR_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**IDENTICAL_FRAME_THRESHOLD:** : Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
15:11	0b RW	**DPLLB_POWER_DOWN_DELAY:** programmable delay from main link powerdown to DPLLB powerdown. The delay is in number of cdclk clocks.
10	0b RW	**DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY:** . If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
9	0b RW	**SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE:** . If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with Source transmitter state in PSR active bit in DPCD register of the sink.

Bit Range	Default & Access	Field Name (ID): Description
8	0b RW	**PSR_ACTIVE_ENTRY:** This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
7	0b RW	**PSR_SINGLE_FRAME_UPDATE:** In PSR SW or HW mode, SW set this bit before writing registers for a flip. After HW finishes signle frame update, it goes back to PSR active ? no RFB state. SW driver may send new single frame update request. Programming note: Reading this bit is updated at the next vblank. Writing this bit to 1 will cause PSR FSM to perform single frame update automatically, no vblank is required. When single frame update is done, it will automatically go back to PSR active ? no RFB update. 61094[2:0] = 3b011.
6:5	0b RW	**RESERVED_1:** Reserved.
4:2	0b RW	**PSR_MODE:** b011-111: reserved. b010: PSR with HW timer. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: PSR with SW timer. In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point. b000: PSR manual (debug) mode. All of PSR state transitions and SDP content is managed by SW driver. SW is responsible to change SDP content for every frame with appropriate values to keep PSR panel in synchronized states.
1	0b RW	**PSR_RESET:** If assert all PSR functions are reset back to PSR inactive state. When it needs to resynchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
0	0b RW	**PSR_ENABLE:** Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

14.11.12 PSRSTATB—Offset 61094h

Pipe B PSR status register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61094h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31	30:24	23:13	12	11	10	9:8	7:5	4:0
Field	DISPLAY_LOCAL_STANDBY_STATE	RESERVED	REPEAT_FRAME_COUNTER	RESERVED_1	SDP_SENT	PSR_IN_TRANSITION	RESERVED_2	PSR_LAST_STATE	PSR_CURRENT_STATE

Default bits 31–0: 0000 0000 0000 0000 0000 0000 0000 0000

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RO	**DISPLAY_LOCAL_STANDBY_STATE:** :00: D0 idle state, fetch frame buffer from system memory 01: D0i1 not defined in VLVP 02: D0i2 PSR is active, display controller is trunk gated 03: D0i3 PSR is active, display controller is power gated
29:24	0b RO	**RESERVED:** Reserved.
23:16	0b RO	**REPEAT_FRAME_COUNTER:** : Number of identical frames has been sent by display controller. Value is not roll over at 255.
15:9	0b RO	**RESERVED_1:** Reserved.
8	0b RO	**SDP_SENT:** it indicates if SDP packet has been sent in current frame.
7	0b RO	**PSR_IN_TRANSITION:** There is a period that source already committed to PSR active but sink did not. SW should not change the source state at this time but wait until this status bit is clear. The wait time should in the range of 120-250us in the worst case.
6	0b RO	**RESERVED_2:** Reserved.
5:3	0b RO	**PSR_LAST_STATE:** indicate last source state that VLVP PSR state machine were in (debug) 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit
2:0	0b RO	**PSR_CURRENT_STATE:** indicate current source state that VLVP PSR state machine are in 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit

14.11.13 PSRCRC1B—Offset 61098h

Pipe B PSR CRC1 register

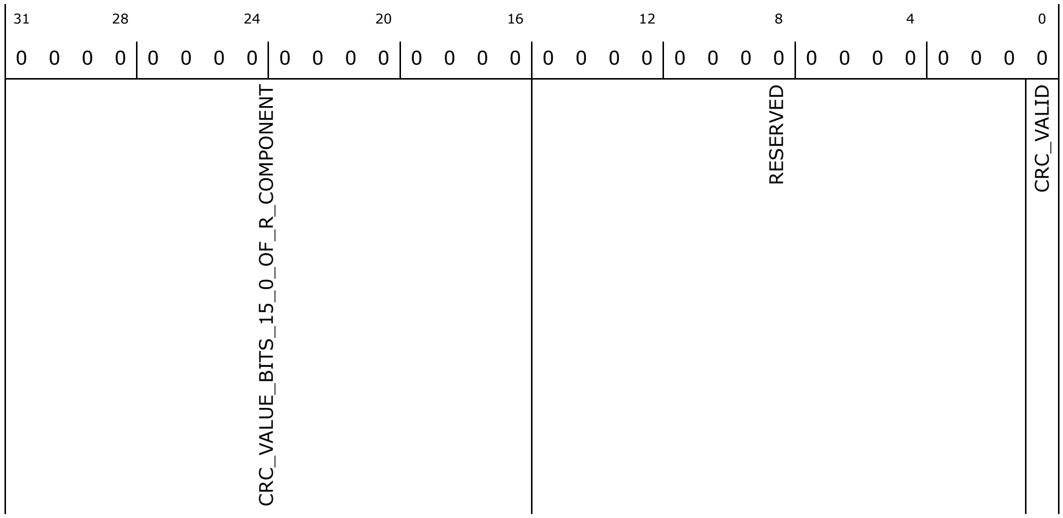
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61098h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RO	**CRC_VALUE_BITS_15_0_OF_R_COMPONENT:** crc values bits 15 to 0 of Red component
15:1	0b RO	**RESERVED:** Reserved.
0	0b RO	**CRC_VALID:** CRC calculation complete and valid for previous frame.

14.11.14 PSRCRC2B—Offset 6109Ch

Pipe B PSR CRC2 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6109Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:16	15:0
Default	0000000000000000	0000000000000000
Field	CRC_VALUE_BITS_15_0_OF_B_COMPONENT	CRC_VALUE_BITS_15_0_OF_G_COMPONENT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RO	**CRC_VALUE_BITS_15_0_OF_B_COMPONENT:** crc values bits 15 to 0 of blue component
15:0	0b RO	**CRC_VALUE_BITS_15_0_OF_G_COMPONENT:** crc values bits 15 to 0 of green component

14.11.15 VSCSDPB—Offset 610A0h

Pipe B VSC SDP register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 610A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:30	29:16	15:8	7:0
Default	00	00000000000000	00000000	00000000
Field	SDP_SEND_FREQUENCY	RESERVED	DB1	DB0

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**SDP_SEND_FREQUENCY:** 00: off, not sending 01: send one every frame 10: send once 11: reserved Programming note: This field shall be programmed either send once or send one every frame when SW driver sets PSR active entry bit. When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
29:16	0b RW	**RESERVED:** Reserved.
15:8	0b RW	**DB1:** Programmed by display driver in manual mode, auto-generate by display controller in all other modes
7:0	0b RW	**DB0:** Bits 7:4: Stereo Interface Method Specific Parameter Bits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

14.11.16 PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 610B0h

When color correction matrix enable bit is set in PIPEBCONF register, each of pixels in the pipe is multiplied with this matrix. Color matrix is used to convert pixels from one RGB color space to another RGB color space. There are many applications for the use of this matrix like gamut mapping between 72 percent color gamut to 92 percent color gamut. Each coefficient is a 12-bit signed fixed-point number. The application of coefficients are as follows:

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 610B0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:28	27:16	15:12	11:0
Default	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
Field	RESERVED	C01_COEFFICIENT	RESERVED_1	C00_COEFFICIENT

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C01_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11:0	0b RW	**C00_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.11.17 PIPEBWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 610B4h

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 610B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																				C02_COEFFICIENT											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C02_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.11.18 PIPEBWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 610B8h

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 610B8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
RESERVED	C11_COEFFICIENT			RESERVED_1	C10_COEFFICIENT			

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C11_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C10_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.11.19 PIPEBWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 610BCh

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 610BCh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
RESERVED					C12_COEFFICIENT			

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C12_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.11.20 PIPEBWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 610C0h

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 610C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

31:28	27:16	15:12	11:0
RESERVED	C21_COEFFICIENT	RESERVED_1	C20_COEFFICIENT

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Reserved.
27:16	0b RW	**C21_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0b RW	**RESERVED_1:** Reserved.
11:0	0b RW	**C20_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.11.21 PIPEBWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 610C4h

Refer to the description of register PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 610C4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:12	RESERVED
11:0	C22_COEFFICIENT

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**RESERVED:** Reserved.
11:0	0b RW	**C22_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

14.11.22 ADPA—Offset 61100h

Analog Display Port Register CRT port control (dprrega.v adp_Q)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00040000h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	Analog_DisplayPort_Enable
30	Pipe_Select
29:26	Reserved
25:24	CRT_Hot_Plug_Detection_Channel_Status
23	CRT_Hot_Plug_Detection_Enable
22	CRT_Hot_Plug_Circuit_Activation_Period
21	CRT_Hot_Plug_Detect_Warmup_Time
20	CRT_Hot_Plug_Detect_Sampling_Period
19:18	CRT_Hot_Plug_Voltage_Compare_Value
17	CRT_Hot_Plug_Reference_Voltage
16	Force_CRT_Hot_Plug_Detect_Trigger
15:10	Reserved_1
9:5	CRTFullScaleOutputVoltageTrimmingControl
4	VSYNC_Polarity_Control
3	HSYNC_Polarity_Control
2	Reserved_2
1	Reserved_3
0	Reserved_4

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Analog_DisplayPort_Enable:** Project: All Default Value: 0b This bit enables or disables the analog port CRT DAC and syncs outputs. Value Name Description Project 0b Disable Disable the analog port DAC and disable output of syncs All 1b Enable Enable the analog port DAC and enable output of syncs All
30	0b RW	**Pipe_Select:** Project: All Default Value: 0b Determines which pipe output will feed this DAC port. Value Name Description Project 0b Pipe A Pipe A All 1b Pipe B Pipe B All
29:26	0b RW	**Reserved:** Project: All Format:
25:24	0b RO	**CRT_Hot_Plug_Detection_Channel_Status:** Project: All AccessType: Read Only Default Value: 00b These bits are set when a CRT hot plug or unplug event has been detected and indicate which color channels were attached. Write a one to these bits to clear the status. The rising or falling edges of these bits are ORed together to go to the main ISR CRT hot plug register bit. Value Name Description Project 00b None No channels attached All 01b Blue Blue channel only is attached All 10b Green Green channel only is attached All 11b Both Both blue and green channel attached All
23	0b RW	**CRT_Hot_Plug_Detection_Enable:** Project: All Default Value: 0b Hot plug detection is used to set status bits or an interrupt on the connection or disconnection of a CRT to the analog display port. Value Name Description Project 0b Disable CRT hot plug detection is disabled All 1b Enable CRT hot plug detection is enabled All
22	0b RW	**CRT_Hot_Plug_Circuit_Activation_Period:** Project: All Default Value: 0b This bit sets the activation period for the CRT hot plug circuit. Value Name Description Project 0b 64 cdclk 64 cdclk periods All 1b 128 cdclk 128 cdclk periods All
21	0b RW	**CRT_Hot_Plug_Detect_Warmup_Time:** Project: All Default Value: 0b This bit sets the warmup time for the CRT hot plug circuit. Value Name Description Project 0b 2M pcdclks 2M pcdclks warmup (approximately 5ms) All 1b 4M pcdclks 4M pcdclks warmup (approximately 10ms) All
20	0b RW	**CRT_Hot_Plug_Detect_Sampling_Period:** Project: All Default Value: 0b This bit determines the length of time between sampling periods when the transcoder is disabled. Value Name Description Project 0b 1G pcdclks 1G pcdclks (approximately 2 seconds) All 1b 2G pcdclks 2G pcdclks (approximately 4 seconds) All
19:18	01b RW	**CRT_Hot_Plug_Voltage_Compare_Value:** Project: All Default Value: 01b A0 Compare value for Vref to determine whether the analog port is connected to a CRT. Value Name Description Project 00b 80 80 All 01b A0 A0 (Default) All 10b C0 C0 All 11b E0 E0 (bit 17 must be = 1) All

Bit Range	Default & Access	Field Name (ID): Description
17	0b RW	**CRT_Hot_Plug_Reference_Voltage:** Project: All Default Value: 0b Value Name Description Project 0b 325mv 325mv All 1b 475mv 475mv (bits 19:18 must be = 11) All
16	0b RW	**Force_CRT_Hot_Plug_Detect_Trigger:** Project: All Default Value: 0b Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger. Value Name Description Project 0b No Trigger No Trigger All 1b Force Trigger Force Trigger All
15:10	0b RW	**Reserved_1:** Project: All Format:
9:5	0b RW	**CRTFullScaleOutputVoltageTrimmingControl:** Project: All Default Value: 0b This controls CRT output voltage trimming to ensure the output voltage is withing VESA spec.
4	0b RW	**VSYNC_Polarity_Control:** Project: All Default Value: 0b The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal. Value Name Description Project 0b Low Active Low All 1b High Active High All
3	0b RW	**HSYNC_Polarity_Control:** Project: All Default Value: 0b The output HSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal. Value Name Description Project 0b Low Active Low All 1b High Active High All
2	0b RW	**Reserved_2:** Project: All Forma
1	0b RW	**Reserved_3:** Project: All Forma Monochrome Enable: [DevVLVP] If the CRT display is a monochrom type, SW driver shall set this bit to enable the CRT circuit to drive only the green channel to CRT and gate off the red and blue channels. 0 = Monochrome disabled (default) 1 = Monochrome enabled
0	0b RW	**Reserved_4:** Project: All Forma Monochrome Enable: [DevVLVP] If the CRT display is a monochrom type, SW driver shall set this bit to enable the CRT circuit to drive only the green channel to CRT and gate off the red and blue channels. 0 = Monochrome disabled (default) 1 = Monochrome enabled 0 = 1.35V is used for analog supply voltage (default) 1 = 1.25V is used for analog supply voltage

14.11.23 CRTIO_DFX—Offset 61104h

CRT port control (dprrega.v crt_dfx)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61104h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00008000h

Bits	31:24	23:16	15	14:12	11:8	7:0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1	0 0 0	0 0 0 0	0 0 0 0 0 0 0 0
Field	RESERVED	BONUS_FOR_CRT	CHOPPING_ENABLE	BONUS_FOR_DPR	MODESEL_DFX_MODE_	DIAGNOSTIC_RO

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** read as zero
23:16	0b RW	**BONUS_FOR_CRT:** bonus for CRT port control
15	1b RW	**CHOPPING_ENABLE:** Chopping enable (for BG circuit)
14:12	0b RW	**BONUS_FOR_DPR:** bonus for DPR crt port control
11:8	0b RW	**MODESEL_DFX_MODE_:** ModeSel (DFx mode)
7:0	0b RO	**DIAGNOSTIC_RO:** Observe signals at CRTIO AccessType: Read Only

14.11.24 PORT_HOTPLUG_EN—Offset 61110h

DPD enable control (dprrega.v ql_hotplugen_Q)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000020h

Bits	Default	Field
31:30	00	RESERVED
29	0	DISPLAYPORT_HDMI_B_HOT_PLUG_INTERRUPT_DETECT_ENABLE
28	0	DISPLAYPORT_HDMI_C_HOT_PLUG_INTERRUPT_DETECT_ENABLE
27	0	DISPLAYPORT_HDMI_D_HOT_PLUG_INTERRUPT_DETECT_ENABLE
26	0	SDVOB_HOT_PLUG_INTERRUPT_DETECT_ENABLE
25	0	SDVOC_HOT_PLUG_INTERRUPT_DETECT_ENABLE
24	0	PIPE_A_AUDIO_INTERRUPT_DETECT_ENABLE
23	0	PIPE_B_AUDIO_INTERRUPT_DETECT_ENABLE
22:19	0000	RESERVED_1
18	0	RESERVED_2
17:16	00	DP_HOTPLUG_SHORT_PULSE_DURATION
15:10	000000	RESERVED_3
9	0	RESERVED_4
8	0	RESERVED_5
7	0	RESERVED_6
6:5	01	RESERVED_7
4	0	RESERVED_8
3	0	RESERVED_9
2	0	RESERVED_10
1:0	00	RESERVED_11

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** mbz
29	0b RW	**DISPLAYPORT_HDMI_B_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCDV, DevCTG, DevELK] This will enable the consideration of the hot plug interrupt status bit for DisplayPort B in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMIB Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMIB Hot Plug Detect Enabled
28	0b RW	**DISPLAYPORT_HDMI_C_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCDV, DevCTG, DevELK] This will enable the consideration of the hot plug interrupt status bit for DisplayPort C in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMIC Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMIC Hot Plug Detect Enabled
27	0b RW	**DISPLAYPORT_HDMI_D_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit for DisplayPort D in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMID Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMID Hot Plug Detect Enabled
26	0b RW	**SDVOB_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit in the Port Hotplug Status register, offset 61114h. This bit enables detection on the SDVOB interrupt input pin pair. 0 = SDVOB Hot Plug Detect Disabled (Default) 1 = SDVOB Hot Plug Detect Enabled

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**SDVOC_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit in the Port Hotplug Status register, offset 61114h. This bit enables detection on the SDVOC interrupt input pin pair. 0 = SDVOC Hot Plug Detect Disabled (Default) 1 = SDVOC Hot Plug Detect Enabled
24	0b RW	**PIPE_A_AUDIO_INTERRUPT_DETECT_ENABLE:** [DevCDV, DevCL, DevCTG, DevVLVP] This bit enables consideration of the pipe A audio interrupt status bit in the Port Hotplug Status Register, offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 = Audio interrupt detect disabled (Default) 1 = Audio interrupt detect enabled
23	0b RW	**PIPE_B_AUDIO_INTERRUPT_DETECT_ENABLE:** [DevVLVP] This bit enables consideration of the pipe B audio interrupt status bit in the Port Hotplug Status Register, offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 = Audio interrupt detect disabled (Default) 1 = Audio interrupt detect enabled
22:19	0b RW	**RESERVED_1:** mbz
18	0b RW	**RESERVED_2:** [DevVLVP] MBZ TV Hot Plug Detect Interrupt Enable: [DevCL, DevCTG] This will enable the consideration of the TV hot plug interrupt status bit. 0 = TV Hot Plug Detect Disabled (bit 10 of the port hotplug status register no longer detects interrupts, Default) 1 = TV Hot Plug Detect Enabled
17:16	0b RW	**DP_HOTPLUG_SHORT_PULSE_DURATION:** [DevCDV, DevCTG, DevELK] These bits define the duration of the pulse defined as a short pulse for DisplayPort ports. Pulse less than this value is detected short pulse. Pulse larger than this value is detected long pulse. For DP, this shall use 2ms as threshold. 00 = 2mS (Default) 01 = 4.5mS 10 = 6mS 11 = 100mS
15:10	0b RW	**RESERVED_3:** mbz
9	0b RW	**RESERVED_4:** [DevVLVP] MBZ. This bit is the same as bit 23 in 61100h [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT Hot plug Interrupt Enable: Hotplug detection is used to cause an interrupt or status bit based on the connection or disconnection of a CRT to the analog video connection. 0 = No hot plug interrupt is enabled (Default) 1 = Hot plug detection is enabled
8	0b RW	**RESERVED_5:** [DevVLVP] MBZ. This bit is the same as bit 22 in 61100h [DevCDV, DevCTG] CRT Hot plug Circuit Activation Period: This bit sets the activation period for the CRT hot plug circuit detection. Setting this bit to 1 is required for the correct operation of CRT DAC detection. 0 = 32 cdclk periods (Default) 1 = 64 cdclk periods
7	0b RW	**RESERVED_6:** [DevVLVP] MBZ. This bit is the same as bit 21 in 61100h [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT DAC on time Value: Powerup time for 0 = CRT DAC requires 2M cdclks for warmup (Default) 1 = CRT DAC requires 4M cdclks for warmup

Bit Range	Default & Access	Field Name (ID): Description
6:5	01b RW	**RESERVED_7:** [DevVLVP] MBZ. This bit is the same as bit 19:18 in 61100h [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT Hot plug Voltage Compare Value: Compare value for CRT hotplug detect Vref to determine whether the analog port is connected to a CRT. The voltage is forced at the beginning of the active region of the screen every 2 seconds. 00 = A0, 01 = B0, (Default) 10 = C0 11 = D0
4	0b RW	**RESERVED_8:** [DevVLVP] MBZ. This bit is the same as bit 20 in 61100h [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT Hot Plug Detect Delay: This bit determines the length of time between polling periods when the DAC/pipe are disabled 0 = 1G cdclks (default) 1 = 2G cdclks
3	0b RW	**RESERVED_9:** [DevVLVP] MBZ [DevCDV, DevCTG, DevBW, DevCL, DevBLC] Force CRT detect trigger: Triggers a CRT hotplug/unplug detection cycle independent of the interrupt enable bit. Bits 5:8 of this register must be correctly programmed when forcing a trigger. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in bits 9:8 of the port hotplug interrupt status register. The CRT interrupt status bit #11 in the hot plug status register (61114) will get set the first time Force CRC detect trigger is used after reset. Software must reset status after a force CRT detect trigger. 0 = No trigger (Default) 1 = Trigger
2	0b RW	**RESERVED_10:** [DevVLVP] MBZ. This bit is the same as bit 17 in 61100h [DevCTG-B] CRT DAC hot plug detection reference voltage selection: 0 = 325mv, bits[6:5] should be set to 01 (Default) 1 = 475mv, bits[6:5] should be set to 11
1:0	0b RW	**RESERVED_11:** mbz

14.11.25 PORT_HOTPLUG_STAT—Offset 61114h

CRT port control (dprrega.v porthotst_aR)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61114h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31:30	0 0	RESERVED
29	0	DISPLAYPORT_HDMIB_HOT_PLUG_INPUT_BUFFER_LIVE_STATE
28	0	DISPLAYPORT_HDMIC_HOT_PLUG_INPUT_BUFFER_LIVE_STATE
27	0	DISPLAYPORTD_HOT_PLUG_INPUT_BUFFER_LIVE_STATE
26:24	0 0 0	RESERVED_1
23	0	PIPE_B_AUDIO_INTERRUPT_LIVE_STATE
22:21	0 0	DISPLAYPORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS
20:19	0 0	DISPLAYPORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS
18:17	0 0	DISPLAYPORT_B_HOT_PLUG_INTERRUPT_DETECT_STATUS
16	0	PIPE_A_AUDIO_INTERRUPT_LIVE_STATE
15	0	DIGITAL_PORT_B_AUDIO_REQUEST_LIVE_STATE
14	0	DIGITAL_PORT_C_AUDIO_REQUEST_LIVE_STATE
13:12	0 0	RESERVED_2
11	0	CRT_HOT_PLUG_INTERRUPT_STATUS
10	0	TV_HOT_PLUG_INTERRUPT_STATUS
9:8	0 0	RESERVED_3
7	0	RESERVED_4
6	0	DISPLAYPORT_D_AUX_INTERRUPT_STATUS
5	0	DISPLAYPORT_C_AUX_INTERRUPT_STATUS
4	0	DISPLAYPORT_B_AUX_INTERRUPT_STATUS
3	0	SDVO_C_HOT_PLUG_INTERRUPT_DETECT_STATUS
2	0	SDVO_B_HOT_PLUG_INTERRUPT_DETECT_STATUS
1	0	PIPE_A_AUDIO_INTERRUPT_DETECT_STATUS
0	0	PIPE_B_AUDIO_INTERRUPT_DETECT_STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** mbz
29	0b RO	**DISPLAYPORT_HDMIB_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** [DevCDV, DevCTG, DevELK] This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPort or HDMI B when bit 29 of the hotplug enable register, offset 61110h is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 = HPD detected active 0 = HPD detected inactive AccessType: Read Only
28	0b RO	**DISPLAYPORT_HDMIC_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** [DevCDV, DevCTG, DevELK] This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPortC when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 = HPD detected high 0 = HPD detected low AccessType: Read Only
27	0b RO	**DISPLAYPORTD_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** [DevCTG] This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPortD when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. Please note that port D is intended for LFP use and therefore HPD may not be present. Bit 2 of the DPD control register must therefore be read to determine whether DPD is used in the system. 1 = HPD detected high 0 = HPD detected low AccessType: Read Only
26:24	0b RW	**RESERVED_1:** mbz

Bit Range	Default & Access	Field Name (ID): Description
23	0b RO	**PIPE_B_AUDIO_INTERRUPT_LIVE_STATE:** [DevVLVP] This read-only bit is used only in ports that use TMDS encoding. It reflects the state of the pipe B audio interrupt request for HDCP when bit 1 of this register is set. This pin signal is active high. It does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
22:21	0b RW/1C	**DISPLAYPORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCTG] This reflects hot plug interrupt status on DisplayPort D. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 27 of the hotplug enable status register is set. 00 = DisplayPort D Hot Plug event not detected 1x = DisplayPort D long pulse Hot Plug event detected X1 = DisplayPort D short pulse Hot Plug event detected AccessType: One to Clear
20:19	0b RW/1C	**DISPLAYPORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCDV, DevCTG, DevELK] This reflects hot plug interrupt status on DisplayPort or HDMI C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 28 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 28, the hot plug input buffer live state, when determining further action: if bit 28 = 0, the bits should be cleared and the port must be disabled. 00 = DisplayPort/HDMI C Hot Plug event not detected 1x = DisplayPort/HDMI C long pulse Hot Plug event detected X1 = DisplayPort C short pulse Hot Plug event detected AccessType: One to Clear
18:17	0b RW/1C	**DISPLAYPORT_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCDV, DevCTG, DevELK] This reflects hot plug interrupt status on DisplayPort B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 29 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 29, the hot plug input buffer live state, when determining further action: if bit 29 = 0, the bits should be cleared and the port must be disabled. 00 = DisplayPort/HDMI B Hot Plug event not detected 1x = DisplayPort/HDMI B long pulse Hot Plug event detected X1 = DisplayPort B short pulse Hot Plug event detected AccessType: One to Clear
16	0b RO	**PIPE_A_AUDIO_INTERRUPT_LIVE_STATE:** [DevCDV, DevCTG, DevCL] This read-only bit is used only in ports that use TMDS encoding. It reflects the state of the pipe A audio interrupt request for HDCP when bit 1 of this register is set. This pin signal is active high. It does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
15	0b RO	**DIGITAL_PORT_B_AUDIO_REQUEST_LIVE_STATE:** [DevCDV, DevCTG, DevCL] This read-only bit is only used on ports using audio. It reflects the state of audio HDCP request when bit 17 of this register is set if audio is enabled on this port. This pin signal is active high. This does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
14	0b RO	**DIGITAL_PORT_C_AUDIO_REQUEST_LIVE_STATE:** [DevCDV, DevCTG, DevCL] This read-only bit is only used on ports using audio. It reflects the state of audio HDCP request when bit 19 of this register is set if audio is enabled on this port. This pin signal is active high. This does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
13:12	0b RW	**RESERVED_2:** mbz

Bit Range	Default & Access	Field Name (ID): Description
11	0b RW/1C	**CRT_HOT_PLUG_INTERRUPT_STATUS:** [DevCDV, DevCTG, DevBW, DevCL, DevBLC] This bit is set when a CRT hot plug or unplug event has been detected. A hot plug or unplug event is defined as the change in connection state of the CRT as determined by the hardware CRT detect sequence which is enabled through bit #9 (CRT hot plug interrupt enable) or bit #3 (Force CRT detect trigger) in the Port_HotPlug_En register 0x61110. After reset, the CRT is considered unconnected even if physically connected until the first detect sequence occurs. Physically plugging or unplugging the CRT device will also be detected as a change of connection state. Writing a 1 to this bit clears it. 0 =CRT Interrupt has not occurred 1 = CRT Interrupt has occurred AccessType: One to Clear
10	0b RW/1C	**TV_HOT_PLUG_INTERRUPT_STATUS:** [DevCTG, DevBW, DevCL, DevBLC] This bit is set when a TV hot plug or unplug event has been detected. Reflects the state of bit 31 of the TV DAC state register, offset 68004-68007h. Software must write a one to these bits to clear the status. 0 =TV Interrupt has not occurred 1 = TV Interrupt has occurred AccessType: One to Clear
9:8	0b RW/1C	**RESERVED_3:** [DevVLVP] MBZ. These info are recorded in 61100h ADPA register[25:24] [DevCDV, DevCTG, DevBW, DevCL, DevBLC] CRT Hot Plug Detection Status (read only): These bits are set when a CRT hot plug or unplug event has been detected. 00 = No channels attached (default) 01 = Blue channel only is attached 10 = Green channel only is attached 11 = Both blue and green channel attached AccessType: One to Clear
7	0b RW	**RESERVED_4:** mbz
6	0b RW/1C	**DISPLAYPORT_D_AUX_INTERRUPT_STATUS:** [DevCTG] This bit is set when a transaction on AUX channel D has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel D control register is set. Writing a 1 to this bit clears it. 0 = AUX channel D Interrupt has not occurred 1 = AUX channel D Interrupt has occurred AccessType: One to Clear
5	0b RW/1C	**DISPLAYPORT_C_AUX_INTERRUPT_STATUS:** [DevCTG, DevCDV] This bit is set when a transaction on AUX channel C has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel C control register is set. Writing a 1 to this bit clears it. 0 = AUX channel C Interrupt has not occurred 1 = AUX channel C Interrupt has occurred AccessType: One to Clear
4	0b RW/1C	**DISPLAYPORT_B_AUX_INTERRUPT_STATUS:** [DevCTG, DevCDV] This bit is set when a transaction on AUX channel B has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel B control register is set. Writing a 1 to this bit clears it. 0 = AUX channel B Interrupt has not occurred 1 = AUX channel B Interrupt has occurred AccessType: One to Clear
3	0b RW/1C	**SDVO_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCTG, DevCDV] This reflects hot plug interrupt status on SDVO port C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 25 of the hotplug enable status register is set. 0 = SDVO Hot Plug event not detected 1 = SDVO Hot Plug event detected AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW/1C	**SDVO_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCTG, DevCDV] This reflects hot plug interrupt status on SDVO port B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 26 of the hotplug enable status register is set. 0 = SDVO Hot Plug event not detected 1 = SDVO Hot Plug event detected AccessType: One to Clear
1	0b RW/1C	**PIPE_A_AUDIO_INTERRUPT_DETECT_STATUS:** [DevCTG, DevCDV, DevCL] This reflects a request for integrated HDCP state change set by audio driver and propagated through the audio hardware. The graphics software must write a one to this bit to clear the status. Upon clearing this bit, the audio ready bit is cleared in the audio registers. The graphics software then must reset audio ready bit 14 in the audio control register, offset 620B4h to 1 when the HDCP interrupt has been serviced. This bit feeds into the first line interrupt status register when bit 24 of the hotplug enable status register is set 0 = Audio interrupt event not detected 1 = Audio interrupt event detected AccessType: One to Clear
0	0b RW/1C	**PIPE_B_AUDIO_INTERRUPT_DETECT_STATUS:** [DevCTG, DevCDV, DevCL] This reflects a request for integrated HDCP state change set by audio driver and propagated through the audio hardware. The graphics software must write a one to this bit to clear the status. Upon clearing this bit, the audio ready bit is cleared in the audio registers. The graphics software then must reset audio ready bit 14 in the audio control register, offset 620B4h to 1 when the HDCP interrupt has been serviced. This bit feeds into the first line interrupt status register when bit 23 of the hotplug enable status register is set 0 = Audio interrupt event not detected 1 = Audio interrupt event detected AccessType: One to Clear

14.11.26 SDVOHDMIB—Offset 61140h

Digital Display Port B Control Register HDMIB port control (dprrega.v sdvo_bQ)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61140h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000018h

Bits	Default	Field
31	0	SDVO_HDMIB_ENABLE_DIGITAL_DISPLAY_PORT_B_ENABLE
30	0	PIPE_SELECT
29	0	RESERVED
28:26	0 0 0	COLOR_FORMAT
25:19	0 0 0 0 0 0 0	RESERVED_1
18	0	SDVO_HDMIB_CLOCK_OUTPUT_INVERSION_TEST_MODE
17:16	0 0	SYMBOL_CLOCK_DUTY_CYCLE
15	0	RESERVED_2
14	0	RESERVED_3
13	0	RESERVED_4
12	0	RESERVED_5
11:10	0 0	ENCODING
9	0	NULL_PACKETS_ENABLED_DURING_VSYNC
8	0	COLOR_RANGE_SELECT
7	0	RESERVED_6
6	0	AUDIO_OUTPUT_ENABLE
5	0	HDCP_PORT_SELECT
4:3	1 1	SYNC_POLARITY
2	0	DIGITAL_PORT_B_DETECTED
1:0	0 0	RESERVED_7

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SDVO_HDMIB_ENABLE_DIGITAL_DISPLAY_PORT_B_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. This port must not be enabled simultaneously with DisplayPort B. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to 0 after disabling the port. This is workaround for hardware issue where the transcoder select set to 1 will prevent DisplayPortB from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to 1) as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat 1 = Enable. This bit enables the Digital Display Port B interface for HDMI or SDVO modes. 0 = Disable and tristates the Digital Display Port B interface for HDMI or SDVO modes.
30	0b RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29	0b RW	**RESERVED:** [DevCDV]: [DevCTG, DevBW, DevCL, DevBLC] Stall Select: This bit selects stall for external scaling functionality only on SDVO. Programming notes: It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe, one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function, as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 = Stall input signal is unused on this port 1 = Stall input signal is used to stall the pipe attached to this port

Bit Range	Default & Access	Field Name (ID): Description
28:26	0b RW	**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color (Default, x3 mode) 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:19	0b RW	**RESERVED_1:** Reserved.
18	0b RW	**SDVO_HDMIB_CLOCK_OUTPUT_INVERSION_TEST_MODE:** Please note that this applies to all modes and is instantly updated. 1 = sDVO/HDMIB Clock output is inverted 0 = sDVO/HDMIB Clock output is NOT inverted (DEFAULT)
17:16	0b RW	**SYMBOL_CLOCK_DUTY_CYCLE:** [DevCDV, DevCTG, DevCL] These bits control the output clock duty cycle to enable EMI mitigation on the external UDI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = (Default) 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 11 = Reserved
15	0b RW	**RESERVED_2:** [DevCDV, DevVLVP]: [DevBW, DevCL, DevBLC] Port Lane Reversal: This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place on the Vblank after being written. It is an OEM configurable feature. 0 = (Default) Not reversed 1 = Reversed
14	0b RW	**RESERVED_3:** Reserved.
13	0b RW	**RESERVED_4:** [DevCDV, DevVLVP]: [DevBW, DevCL, DevBLC] Clock Output Disable: This bit disables the clock output on the digital output port. For 8b/10b modes the clock output should be disabled. 0 = (Default) Clock output enabled 1 = Clock output disabled
12	0b RW	**RESERVED_5:** [DevCDV, DevVLVP]: [DevBW, DevCL, DevBLC, DevCDV] Scrambling enable: This bit enables scrambling for UDI-related modes using ANSI 8b/10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 = Scrambling disabled (Default) 1 = Scrambling enabled
11:10	0b RW	**ENCODING:** [DevCDV, DevCTG, DevCL] These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C. 00 = Reserved 01 = Reserved 10 = TMDS encoding ([DevCL, DevCTG, DevCDV, DevVLVP] external link and HDMI only) See the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved

Bit Range	Default & Access	Field Name (ID): Description
9	0b RW	**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. (Default) 1 = Enable null infoframe packets when Vsync=1 on this port.
8	0b RW	**COLOR_RANGE_SELECT:** [DevCDV, DevCTG, DevCL] This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
7	0b RW	**RESERVED_6:** [DevCDV]: [DevCTG, DevBW, DevCL, DevBLC] sDVOB Border Enable: This bit determines if the border data from native VGA or the timing generator is to be considered valid pixel data at the external component. 1 = Border to the sDVOB encoder is enabled. Blank# is used to generate the DE output (used in all cases except when the external scaler is used in a DVI panel, over SDVO) . 0 = Border to the sDVOB encoder is disabled. DE (Display Enable) is used
6	0b RW	**AUDIO_OUTPUT_ENABLE:** [DevCDV, DevCTG, DevCL] This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = (Default) No audio output on this port 1 = Enable audio on this port
5	0b RW	**HDCP_PORT_SELECT:** [DevCDV, DevCTG, DevCL] This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	11b RW	**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS BLANK+VS BLANK+VS+HS. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0b RO	**DIGITAL_PORT_B_DETECTED:** Read-only bit indicating whether a digital port B was detected during initialization. It signifies the level of the GMBUS port 4 (sDVO B/C) data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port B not detected during initialization 1 = Digital Port B detected during initialization AccessType: Read Only
1:0	0b RW	**RESERVED_7:** MBZ

14.11.27 SDVO—Offset 61154h

DP2 - Digital Port DFT Register ;

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61154h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30:14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SDVO_DC_BALANCE_RESET	RESERVED	PORTC_AUX_LEAKAGE_ENABLE	PORTB_AUX_LEAKAGE_ENABLE	SCRAMBLED_1S_ON_PIPE_B	SCRAMBLED_1S_ON_PIPE_A	IDLE_TIME_SPEEDUP_ON_PIPE_B	IDLE_TIME_SPEEDUP_ON_PIPE_A	TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_TRANSCODE_B	TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_TRANSCODE_A	SCRAMBLED_0S_ON_TRANSCODE_B	SCRAMBLED_0S_ON_TRANSCODE_A	PRBS7_TEST_PATTERN_ON_TRANSCODE_B	PRBS7_TEST_PATTERN_ON_TRANSCODE_A	SCRAMBLER_RESET_ONCE_A_FRAME_ON_TRANSCODE_B	SCRAMBLER_RESET_ONCE_A_FRAME_ON_TRANSCODE_A

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SDVO_DC_BALANCE_RESET:** Project: All Format: Value Name Description Project 0b Not Reset DC Balance circuitry will not be reset on every frame All 1b Reset DC Balance circuitry will be reset on every frame All
30:14	0b RW	**RESERVED:** Project: All Format: MBZ
13	0b RW	**PORTC_AUX_LEAKAGE_ENABLE:** Project: All Format:
12	0b RW	**PORTB_AUX_LEAKAGE_ENABLE:** Project: All Format:
11	0b RW	**SCRAMBLED_1S_ON_PIPE_B:** Project: All Format: Value Name Description Project 0b Disable Disable scrambled 1s All 1b Enable Enable scrambled 1s All

Bit Range	Default & Access	Field Name (ID): Description
10	0b RW	**SCRAMBLED_1S_ON_PIPE_A:** Project: All Format: Value Name Description Project 0b Disable Disable scrambled 1s All 1b Enable Enable scrambled 1s All
9	0b RW	**IDLE_TIME_SPEEDUP_ON_PIPE_B:** Project: All Format: Value Name Description Project 0b Normal Normal idle time All 1b Speedup Speedup idle time All
8	0b RW	**IDLE_TIME_SPEEDUP_ON_PIPE_A:** Project: All Format: Value Name Description Project 0b Normal Normal idle time All 1b Speedup Speedup idle time All
7	0b RW	**TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
6	0b RW	**TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
5	0b RW	**SCRAMBLED_0S_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the scramble 0s All 1b Enable Enable the scramble 0s All
4	0b RW	**SCRAMBLED_0S_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the scramble 0s All 1b Enable Enable the scramble 0s All
3	0b RW	**PRBS7_TEST_PATTERN_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
2	0b RW	**PRBS7_TEST_PATTERN_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
1	0b RW	**SCRAMBLER_RESET_ONCE_A_FRAME_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the scrambler reset once a frame All 1b Enable Enable the scrambler reset once a frame All
0	0b RW	**SCRAMBLER_RESET_ONCE_A_FRAME_ON_TRANSCODE_A:** All Format: Value Name Description Project 0b Disable Disable the scrambler reset once a frame All 1b Enable Enable the scrambler reset once a frame All

14.11.28 HDMIC—Offset 61160h

Digital Display Port C Register HDMIC port control (dprrega.v sdvo_cQ)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61160h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000018h

Bits	31	30	29	28:26	25:19	18	17:16	15	14	13	12	11:10	9	8	7	6	5	4:3	2	1	0
Default	0	0	0	0 0 0	0 0 0 0 0 0 0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	1 1	0	0	0
Field	SDVO_HDMIC_ENABLE_DIGITAL_DISPLAY_PORT_C_ENABLE	PIPE_SELECT	RESERVED	COLOR_FORMAT	RESERVED_1	SDVO_HDMIC_CLOCK_OUTPUT_INVERSION_TEST_MODE	SYMBOL_CLOCK_DUTY_CYCLE	RESERVED_2	RESERVED_3	RESERVED_4	RESERVED_5	ENCODING	NULL_PACKETS_ENABLED_DURING_VSYNC	COLOR_RANGE_SELECT	SDVOC_BORDER_ENABLE	AUDIO_OUTPUT_ENABLE	HDCP_PORT_SELECT	SYNC_POLARITY	DIGITAL_PORT_C_DETECTED	DDI2_PORT_DETECTED	RESERVED_6

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SDVO_HDMIC_ENABLE_DIGITAL_DISPLAY_PORT_C_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port in HDMI. This port must not be enabled simultaneously with DisplayPort C. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to 0 after disabling the port. This is workaround for hardware issue where the transcoder select set to 1 will prevent DPC from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to 1) as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat. 1 = Enable. This bit enables the Digital Display Port C interface for HDMI or DVI modes. 0 = Disable and tristates the Digital Display Port C interface for HDMI or DVI modes.
30	0b RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29	0b RW	**RESERVED:** [DevCDV]: stall Select: This bit selects stall for external scaling functionality only on SDVO. Programming notes: It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe, one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function, as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 = Stall input signal is unused on this port 1 = Stall input signal is used to stall the pipe attached to this port

Bit Range	Default & Access	Field Name (ID): Description
28:26	0b RW	**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color (Default) 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:19	0b RW	**RESERVED_1:** Reserved.
18	0b RW	**SDVO_HDMIC_CLOCK_OUTPUT_INVERSION_TEST_MODE:** Please note that this applies to all modes and is instantly updated. 1 = sDVO/HDMIB Clock output is inverted 0 = sDVO/HDMIB Clock output is NOT inverted (DEFAULT)
17:16	0b RW	**SYMBOL_CLOCK_DUTY_CYCLE:** These bits control the output clock duty cycle to enable EMI mitigation on the external HDMI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = (Default) 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 ([DevCL, DevCTG, DevCDV] HDMI only) 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 ([DevCL, DevCTG, DevCDV] HDMI only) 11 = Reserved
15	0b RW	**RESERVED_2:** [DevCTG, DevCDV, DevVLVP] Port Lane Reversal: This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place on the Vblank after being written. It is an OEM configurable feature. 0 = (Default) Not reversed 1 = Reversed
14	0b RW	**RESERVED_3:** Reserved.
13	0b RW	**RESERVED_4:** [DevCTG, DevCDV, DevVLVP] Clock Output Disable: This bit disables the clock output on the digital output port. For 8b/10b modes the clock output should be disabled. 0 = (Default) Clock output enabled 1 = Clock output disabled ([DevCL] only)
12	0b RW	**RESERVED_5:** [DevCTG, DevCDV, DevVLVP]: Scrambling enable: This bit enables scrambling for UDI-related modes using ANSI 8b/10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 Scrambling disabled (Default) 1 = Scrambling enabled ([DevCL] only)
11:10	0b RW	**ENCODING:** These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C. 00 = Reserved 01 = Reserved 10 = TMDS encoding ([DevCL, DevCTG, DevCDV, DevVLVP] external link and HDMI only) See the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved

Bit Range	Default & Access	Field Name (ID): Description
9	0b RW	**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. (Default) 1 = Enable null infoframe packets when Vsync=1 on this port.
8	0b RW	**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output ([DevCL and DevCTG] only)
7	0b RW	**SDVOC_BORDER_ENABLE:** This bit determines if the border data from native VGA or the timing generator is to be considered valid pixel data at the external component. 1 = Border to the sDVOC encoder is enabled. Blank# is used to generate the DE output (used in all cases except when the external scaler is used in a DVI panel, over SDVO) . 0 = Border to the sDVOC encoder is disabled. DE (Display Enable) is used
6	0b RW	**AUDIO_OUTPUT_ENABLE:** ([DevCL, DevCTG, DevCDV]): This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = (Default) No audio output on this port 1 = Enable audio on this port ([DevCL, DevCTG, DevCDV] only)
5	0b RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port ([DevCL, DevCTG, DevCDV] only)
4:3	11b RW	**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS BLANK+VS BLANK+VS+HS. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0b RO	**DIGITAL_PORT_C_DETECTED:** Read-only bit indicating whether a digital port C was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port C not detected during initialization 1 = Digital Port C detected during initialization (default) AccessType: Read Only
1	0b RO	**DDI2_PORT_DETECTED:** Read-only bit indicating whether the DDI2 port was detected during initialization. It signifies the level of the GMBUS port 1 data line at boot. This bit is valid regardless of whether the port is enabled. 0 = DDI2 Port not detected during initialization 1 = DDI2 Port detected during initialization (default) AccessType: Read Only
0	0b RW	**RESERVED_6:** MBZ

14.11.29 DISPLAY_DIGITAL_PORT_HOT_PLUG_CONTROL_REGISTER—Offset 61164h

display digital poty hot plug control register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61164h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0 0 0 0	0 0 0 0			0 0 0 0				0 0 0 0				0 0 0 0				0 0 0 0				0 0 0 0				0 0 0 0				

Bits	Field
31:21	RESERVED
20	DIGITAL_PORT_D_HOT_PLUG_DETECT_INPUT_ENABLE
19:18	DIGITAL_PORT_D_HOT_PLUG_SHORT_PULSE_DURATION
17:16	DIGITAL_PORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS
15:13	RESERVED_1
12	DIGITAL_PORT_C_HOT_PLUG_DETECT_INPUT_ENABLE
11:10	DIGITAL_PORT_C_HOT_PLUG_SHORT_PULSE_DURATION
9:8	DIGITAL_PORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS
7:5	RESERVED_2
4	DIGITAL_PORT_B_HOT_PLUG_DETECT_INPUT_ENABLE
3:2	DIGITAL_PORT_B_HOT_PLUG_SHORT_PULSE_DURATION
1:0	DIGITAL_PORT_B_HOT_PLUG_INTERRUPT_DETECT_STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:21	0b RW	**RESERVED:** Project: All Format:
20	0b RW	**DIGITAL_PORT_D_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. • Value / Name / Description / Project • 0 / Disable / Buffer disabled /All • 1 / Enable / Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin / All
19:18	0b RW	**DIGITAL_PORT_D_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse. • Value / Name / Description / Project • 00 / 2ms / 2ms / All • 01 / 4.5ms / 4.5ms / All • 10 / 6ms / 6ms / All • 11 / 100ms / 100ms / All

Bit Range	Default & Access	Field Name (ID): Description
17:16	0b RW/1C	**DIGITAL_PORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: 0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. • Value / Name / Description / Project • 00 / No Detect / Digital port hot plug event not detected / All • X1 / Short Detect / Digital port short pulse hot plug event detected / All • 1X / Long Detect / Digital port long pulse hot plug event detected / All
15:13	0b RW	**RESERVED_1:** Project: All Format:
12	0b RW	**DIGITAL_PORT_C_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. • Value / Name / Description / Project • 0 / Disable / Buffer disabled / All • 1 / Enable / Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin / All
11:10	0b RW	**DIGITAL_PORT_C_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse. • Value / Name / Description / Project • 00 / 2ms / 2ms / All • 01 / 4.5ms / 4.5mS / All • 10 / 6ms / 6mS / All • 11 / 100ms / 100mS / All
9:8	0b RW/1C	**DIGITAL_PORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: 0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. • Value / Name / Description / Project • 00 / No Detect / Digital port hot plug event not detected / All • X1 / Short Detect / Digital port short pulse hot plug event detected / All • 1X / Long Detect / Digital port long pulse hot plug event detected / All
7:5	0b RW	**RESERVED_2:** Project: All Format:
4	0b RW	**DIGITAL_PORT_B_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. • Value / Name / Description / Project • 0 / Disable / Buffer disabled / All • 1 / Enable / Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin / All
3:2	0b RW	**DIGITAL_PORT_B_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse. • Value / Name / Description / Project • 00 / 2ms / 2ms / All • 01 / 4.5ms / 4.5ms / All • 10 / 6ms / 6ms / All • 11 / 100ms / 100ms / All

Bit Range	Default & Access	Field Name (ID): Description
1:0	0b RW/1C	**DIGITAL_PORT_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: 0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. • Value / Name / Description / Project • 00 / No Detect / Digital port hot plug event not detected / All • X1 / Short Detect / Digital port short pulse hot plug event detected / All • 1X / Long Detect / Digital port long pulse hot plug event detected / All

14.11.30 DV_DETERM—Offset 61168h

DV Determinism Mode Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61168h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:7	RESERVED
6	DISPLAYPORT_D_PORT_ENABLE_OVERRIDE
5	DISPLAYPORT_C_PORT_ENABLE_OVERRIDE
4	DISPLAYPORT_B_PORT_ENABLE_OVERRIDE
3	DP_SDVO_HDMI_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_B
2	DP_SDVO_HDMI_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_A
1	CRT_LVDS_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_B
0	CRT_LVDS_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_A

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**DISPLAYPORT_D_PORT_ENABLE_OVERRIDE:** Project: All Default Value: 0b • Value / Name / Description / Project • 0b / Normal / Normal operation / All • 1b / Override / DisplayPort D port enable override (controlled from sml0alertb_gp60_mgpio4 pin) / All
5	0b RW	**DISPLAYPORT_C_PORT_ENABLE_OVERRIDE:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override DisplayPort C port enable override (controlled from sus_statb_gp61 pin) All
4	0b RW	**DISPLAYPORT_B_PORT_ENABLE_OVERRIDE:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override DisplayPort B port enable override (controlled from gp57_mgpio5 pin) All
3	0b RW	**DP_SDVO_HDMI_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_B:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override DP/SDVO/HDMI pipe enable override for display pipe B (controlled from gp74_batlowb pin) All
2	0b RW	**DP_SDVO_HDMI_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_A:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override DP/SDVO/HDMI pipe enable override for display pipe A (controlled from slp_s4b pin) All
1	0b RW	**CRT_LVDS_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_B:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override CRT/LVDS pipe enable override for display pipe B (controlled from susclk_gp62 pin) All
0	0b RW	**CRT_LVDS_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_A:** Project: All Default Value: 0b Value Name Description Project 0b Normal Normal operation All 1b Override CRT/LVDS pipe enable override for display pipe A (controlled from slp_mb pin) All

14.11.31 VIDEO_DIP_CTL_B—Offset 61170h

Video DIP Control for Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61170h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 20200900h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0

ENABLE_GRAPHICS_DATA_ISLAND_PACKET | PORT_SELECT | RESERVED | GCP_DIP_ENABLE | DATA_ISLAND_PACKET_TYPE_ENABLE | DIP_BUFFER_INDEX | RESERVED_1 | VIDEO_DIP_TRANSMISSION_FREQUENCY | RESERVED_2 | VIDEO_DIP_BUFFER_SIZE | RESERVED_3 | VIDEO_DIP_RAM_ACCESS_ADDRESS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_GRAPHICS_DATA_ISLAND_PACKET:** Project: All See Pipe A description.
30:29	01b RW	**PORT_SELECT:** Project: All See Pipe A description.
28:26	0b RW	**RESERVED:** Project: All Format:
25	0b RW	**GCP_DIP_ENABLE:** Project: All See Pipe A description. This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode.
24:21	0001b RW	**DATA_ISLAND_PACKET_TYPE_ENABLE:** Project: All See Pipe A description.
20:19	0b RW	**DIP_BUFFER_INDEX:** Project: All See Pipe A description.
18	0b RW	**RESERVED_1:** Project: All Format:
17:16	0b RW	**VIDEO_DIP_TRANSMISSION_FREQUENCY:** Project: All See Pipe A description.
15:12	0b RW	**RESERVED_2:** Project: All Format: MBZ
11:8	1001b RO	**VIDEO_DIP_BUFFER_SIZE:** Project: All AccessType: Read Only Default Value: ;1001b See Pipe A description.
7:4	0b RW	**RESERVED_3:** Project: All Format: MBZ
3:0	0b RO	**VIDEO_DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read only See Pipe A description.

14.11.32 VIDEO_DIP_DATA_B—Offset 61174h

Video Data Island Packet Data for Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61174h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VIDEO_DIP_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**VIDEO_DIP_DATA:** Project: All Format: See Pipe A description.

14.11.33 VIDEO_DIP_GDCP_PAYLOAD_B—Offset 61178h

Video Data Island Payload for Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61178h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | GCP_COLOR_INDICATION | GCP_DEFAULT_PHASE_ENABLE | GCP_AV_MUTE

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**RESERVED:** Project: All Format: MBZ
2	0b RW	**GCP_COLOR_INDICATION:** Project: All See Pipe A description.
1	0b RW	**GCP_DEFAULT_PHASE_ENABLE:** Project: All See Pipe A description.
0	0b RW	**GCP_AV_MUTE:** All See Pipe A description.

14.11.34 MIPIA_PORT_CTRL—Offset 61190h

mipi A port ctrl

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61190h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	EN
30:27	0000	ADJDLY_HSTX
26	0	MIPI_DUAL_LINK_MODE_APPLICABLE_ONLY_IF_MIPI_DUAL_LINK_MODE_IS_ENABLED_THROUGH_MIPI_LANES_CONFIGURATION_BITS
25	0	DITHER
24	0	RESERVED
23	0	SELFLOPPED_HSTX
22	0	RESERVED_1
21:18	0000	FLISDSI_ADJDLY_HSTX_MIPIA
17	0	AFE_LATCHOUT
16	0	LPOUTPUT_HOLD
15	0	FLISDSI_ADJDLYY_HSTX_MIPIC_HIGH_ORDER
14:11	0000	MIPI4DPHY_AdjDly_HSTX_MIPI_C
10:9	00	CSB
8	0	CB
7:5	000	FLISDSI_AdjDly_HSTX_MIPI_C_LOWER_ORDER
4	0	DELAY
3:2	00	EFFECT
1:0	00	MIPI_LANES_CONFIGURATION

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**EN:** When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enable it starts to generate timing for this MIPI port 0 = The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 = The port is enabled
30:27	0b RW	**ADJDLY_HSTX:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
26	0b RW	**MIPI_DUAL_LINK_MODE_APPLICABLE_ONLY_IF_MIPI_DUAL_LINK_MODE_IS_ENABLED_THROUGH_MIPI_LANES_CONFIGURATION_BITS:** 0 = Front-Back mode (default) 1 = Pixel alternative mode
25	0b RW	**DITHER:** This bit enables or disables (bypassing) 8-6-bit color dithering function. The usage of this bit would be on for 18-bpp panels and off for 24-bpp panels. 0 = disabled 1 = enabled
24	0b RW	**RESERVED:** Reserved.
23	0b RW	**SELFLOPPED_HSTX:** This bit will be used to mux between the flopped (new) and unflopped (original) versions of the TX HS clock and data. Default 0 = pass through original unflopped version, if set to 1 = pass through the new flopped version of these signals. We probably need to enable validation to always set these to 1 during startup so we're fully testing this logic as it is the intended way we will run A0
22	0b RW	**RESERVED_1:** Reserved.
21:18	0b RW	**FLISDSI_ADJDLY_HSTX_MIPIA:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
17	0b RW	**AFE_LATCHOUT:** This bit reflect the value of the output latch of CLK A lane in DSI AFE b1 = current value of output latch is 1 (D-PHY is in LP11 state) b0 = current value of output latch is 0 (D-PHY is in LP00 state) The software driver can read this bit to see if the hold value (LP11 or LP00) to initialize from a sleep state (s0i1 or S0i3) correctly
16	0b RW	**LPOUTPUT_HOLD:** 0= disable transparent latche inside DSI AFE. Output are driven by latch value. 1= enable transparent latch inside DSI AFE so data are driven by DSI DPHY
15	0b RW	**FLISDSI_ADJDLYY_HSTX_MIPIC_HIGH_ORDER:** The fourth bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 1'b0 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
14:11	0b RW	**MIPI4DPHY_AdjDly_HSTX_MIPI_C:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals.[Br] Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
10:9	0b RW	**CSB:** Clock input for bandgap voltage sample and hold circuit. Final setting will be based silicon characterization. 00b = 20mhz clock 01b = 10mhz clock 10b = 40mhz clock 11b = reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0b RW	**CB:** Bandgap chicken bit 0 = using Penwell band gap circuit 1 = back to LNC circuit
7:5	0b RW	**FLISDSI_AdjDly_HSTX_MIPI_C_LOWER_ORDER:** The lower 3-bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 3'b000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
4	0b RW	**DELAY:** When set, the TE counter will be count down until
3:2	0b RW	**EFFECT:** 00: No tearing effect required - memory write start as soon as write data is available 01: TE trigger by MIPI DPHY and DSI protocol 10: TE trigger by GPIO pin 11: Reserved
1:0	0b RW	**MIPI_LANES_CONFIGURATION:** 00: All 4 MIPI A lanes are assigned to pipe A. All 4 MIPI C lanes are assigned to pipe B. 01: MIPI dual-link mode with data from pipe A 10: MIPI dual-link mode with data from pipe B 11: Reserved Programming note: when MIPI dual-link mode is enabled, the port enable bits in both MIPI A control register and MIPI C control register shall be enabled.

14.11.35 MIPIA_TEARING_CTR—Offset 61194h

mipi A tearing CTR

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61194h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
RESERVED	TE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**TE:** Number of delay clocks from TE trigger to start sending data to DSI controller

14.11.36 DPA_PIX_GEN_CTRL—Offset 61198h

Display Pipe A Pixel Generator Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61198h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:2	1	0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0
Field	BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_4	BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_3	BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_2	BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_1	RESERVED	MODE_SELECT	PIXEL_GENERATOR_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_4:** Project: All Default Value: 0b
27:24	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_3:** Project: All Default Value: 0b
23:20	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_2:** Project: All Default Value: 0b

Bit Range	Default & Access	Field Name (ID): Description
19:16	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_1:** Project: All Default Value: 0b
15:2	0b RW	**RESERVED:** Project: All Format:
1	0b RW	**MODE_SELECT:** Project: All Default Value: 0b Pixel generator mode select Value Name Description Project 0b LFSR LFSR All 1b Programmable Programmable pixel data register. Setting mode select to 1 will also start the 2-bit counter. All
0	0b RW	**PIXEL_GENERATOR_ENABLE:** All

14.11.37 MIPIA_AUTOPWG—Offset 611A0h

mipi A autopowergating

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 611A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED:** Reserved.

14.11.38 DPB_PIX_GEN_CTRL—Offset 611B0h

Display Pipe B Pixel Generator Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 611B0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31:28	27:24	23:20	19:16	15:2	1	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0
BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_4	BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_3	BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_2	BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_1	RESERVED	MODE_SELECT	PIXEL_GENERATOR_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_4:** Project: All Default Value: 0b
27:24	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_3:** Project: All Default Value: 0b Address: GraphicsAddress[35:32]
23:20	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_2:** Project: All Default Value: 0b
19:16	0b RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_1:** Project: All Default Value: 0b
15:2	0b RW	**RESERVED:** Project: All Format:
1	0b RW	**MODE_SELECT:** Project: All Default Value: 0b Pixel generator mode select Value Name Description Project 0b LFSR LFSR All 1b Programmable Programmable pixel data register. Setting mode select to 1 will also start the 2-bit counter. All
0	0b RW	**PIXEL_GENERATOR_ENABLE:** All Format: Enable

14.11.39 PIPEA_PP_STATUS—Offset 61200h

PipeA Panel Power Status Register ([DevCL, DevCTG, DevCDV]) PP Status (dplrreg.v panel_pwr_sr)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 08000000h

Bits	31	30	29:28	27	26:4	3:0
Default	0	0	0 0	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0
Field	PANEL_POWER_ON_STATUS	REQUIRE_ASSET_STATUS	POWER_SEQUENCE_PROGRESS	POWER_CYCLE_DELAY_ACTIVE	RESERVED	INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**PANEL_POWER_ON_STATUS:** 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a 1 to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.

Bit Range	Default & Access	Field Name (ID): Description
30	0b RO	**REQUIRE_ASSET_STATUS:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled
29:28	0b RO	**POWER_SEQUENCE_PROGRESS:** 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved
27	1b RO	**POWER_CYCLE_DELAY_ACTIVE:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	0b RO	**RESERVED:** Reserved.
3:0	0b RO	**INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG:** 0000 = Power Off Idle (S0.0) 0001 = Power Off, Wait for cycle delay (S0.1) 0010 = Power Off (S0.2) 0011 = Power Off (S0.3) 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Power On Idle (S1.0) 1001 = Power On, (S1.1) 1010 = Power On, (S1.2) 1011 = Power On, Wait for cycle delay (S1.3) 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reset

14.11.40 PIPEA_PP_CONTROL—Offset 61204h

PipeA Panel Power Control Register ([DevCL, DevCTG, DevCDV]) PP Control (dplrreg.v pnl_pwr_cntl)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61204h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WRITE_PROTECT_KEY																RESERVED												EDP_PANEL_VDD_ENABLE	BACKLIGHT_ENABLE	POWER_DOWN_ON_RESET	POWER_STATE_TARGET

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**WRITE_PROTECT_KEY:** ABCD Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write protected. Any write cycles to those write protected registers, while they will complete as normal, will not change the value of the register when write protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write protected registers: (LVDS and Panel sequencing Registers): LVDS Digital Display Port Control Address: 61180h 61183h Pipe A Panel power on sequencing delays - Address: 61208-6120Bh Pipe A Panel power off sequencing delays Address: 6120Ch 6120Fh Pipe A Panel power cycle delay and Reference Divisor Address: 61210h 61213 (DPLL registers): DPLL Control Registers FPA0 DPLL Divisor Register FPA1 DPLL Divisor Register 1 FPB0 DPLL Divisor Register FPB1 DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL Horizontal Total Register HBLANK Horizontal Blank Register HSYNC_ Horizontal Sync Register VTOTAL_ Vertical Total Register VBLANK_ Vertical Blank Register VSYNC_ Vertical Sync Register
15:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**EDP_PANEL_VDD_ENABLE:** [DevCDV]: Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled [DevCLN] Reserved
2	0b RW	**BACKLIGHT_ENABLE:** [DevCTG, DevCDV]: Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled [DevCL] Reserved

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**POWER_DOWN_ON_RESET:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected 1 = Run panel power down sequence when system is reset
0	0b RW	**POWER_STATE_TARGET:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

14.11.41 PIPEA_PP_ON_DELAYS—Offset 61208h

PipeA Panel Power on Sequencing Delays ([DevCL, DevCTG, DevCDV]) PP On Delay values (dplrreg.v DPLRppon_sd)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61208h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:30	PANEL_CONTROL_PORT_SELECT
29	RESERVED
28:16	POWER_UP_DELAY
15:13	RESERVED_1
12:0	POWER_ON_TO_BACKLIGHT_ENABLE_DELAY

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**PANEL_CONTROL_PORT_SELECT:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	0b RW	**RESERVED:** Reserved.
28:16	0b RW	**POWER_UP_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	0b RW	**RESERVED_1:** Reserved.
12:0	0b RW	**POWER_ON_TO_BACKLIGHT_ENABLE_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

14.11.42 PIPEA_PP_OFF_DELAYS—Offset 6120Ch

PipeA Panel Power off Sequencing Delays ([DevCL, DevCTG, DevCDV]) PP Delay Off values (dplrreg.v DPLRppoff_sd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6120Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31:29	28:16	15:13	12:0
000	0000000000000	000	0000000000000
RESERVED	POWER_DOWN_DELAY	RESERVED_1	POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Reserved.
28:16	0b RW	**POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.
15:13	0b RW	**RESERVED_1:** Reserved.
12:0	0b RW	**POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

14.11.43 PIPEA_PP_DIVISOR—Offset 61210h

PipeA Panel Power Cycle Delay and Reference Divisor ([DevCL, DevCTG, DevCDV]) PP Divisor (dplrreg.v DPLRrefdiv_pp_cd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61210h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00270F04h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0

REFERENCE_DIVIDER	RESERVED	POWER_CYCLE_DELAY

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000000 010011100 001111b RW	**REFERENCE_DIVIDER:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value for the display core clock that is for [DevCL and DevCTG] a 200MHz reference value. The following are examples for other memory speeds. Display Core Frequency Value of Field 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	0b RW	**RESERVED:** Reserved.
4:0	00100b RW	**POWER_CYCLE_DELAY:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a +1 value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

14.11.44 PFIT_CONTROL—Offset 61230h

Panel Fitting Controls

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61230h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 20000000h

Bits	Default	Field
31	0	PANEL_FITTING_ENABLED
30:29	0 1	PIPE_SELECT
28:26	0 0 0	SCALING_MODE
25:24	0 0	FILTER_COEFFICIENT_SELECT
23	0	DEBUG_FORCE_TWO_LINE_MODE
22	0	DEBUG_FORCE_THREE_PIXEL_MODE_WHEN_IN_TWO_LINE_MODE
21:19	0 0 0	DEBUG_CREATE_EXTRA_STALLS_IN_VGA_MODE
18:5	0 0 0 0 0 0 0 0 0 0 0 0 0 0	RESERVED
4	0	RESERVED_1
3	0	RESERVED_2
2:0	0 0 0	RESERVED_3

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PANEL_FITTING_ENABLED:** Disables the panel fitting function by forcing pixels to bypass. Panel fitting must be disabled when running VGA native modes or interlaced modes on the same pipe. Panel fitting should be enabled or disabled before the pipe is enabled. 0 = Bypass the panel fitting (1:1 ratio) 1 = Enable panel fitting (Ratios include 1:1)
30:29	01b RW	**PIPE_SELECT:** Indicates the pipe attached to the panel fitter 00 = Panel fitter is attached to Display Pipe A. 01 = Panel fitter is attached to Display Pipe B. This is the default after reset. 10 = Reserved for pipe C 11 = Reserved for pipe D
28:26	0b RW	**SCALING_MODE:** 000 = Auto-scale (source and destination should have the same aspect ratios) 001 = Programmed scaling: Values in register 61234h will be used for horizontal and vertical scaling factors 010 = Pillarbox (example: 4:3 to 16:9 auto conversion) use only when destination has wider aspect ratio than source 011 = Letterbox (example: 16:9 to 4:3 auto conversion) use only when destination has taller aspect ratio than source 1xx = Reserved
25:24	0b RW	**FILTER_COEFFICIENT_SELECT:** Selects the set of predefined filter coefficients to use for panel fitting 00 = Fuzzy filtering 01 = Crisp edge enhancing filtering 10 = Median between fuzzy and crisp filtering 11 = Reserved
23	0b RW	**DEBUG_FORCE_TWO_LINE_MODE:** debug for two line mode
22	0b RW	**DEBUG_FORCE_THREE_PIXEL_MODE_WHEN_IN_TWO_LINE_MODE:** debug force three pixel mode when in two line mode

Bit Range	Default & Access	Field Name (ID): Description
21:19	0b RW	**DEBUG_CREATE_EXTRA_STALLS_IN_VGA_MODE:** 000 = No stall 001 = 33% stall 010 = 50% stall 011 = 66% stall 100 = 75% stall 101 = 80% stall 110 = 90% stall 111 = Reserved
18:5	0b RW	**RESERVED:** Reserved.
4	0b RW	**RESERVED_1:** (was Force One Line Mode) write as zero
3	0b RW	**RESERVED_2:** (was Dither Enable which moved to register 61180h)
2:0	0b RW	**RESERVED_3:** Reserved.

14.11.45 PFIT_PGM_RATIOS—Offset 61234h

Programmed Panel Fitting Ratios

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61234h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:29	28:16	15:13	12:0
Default	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0
Field	RESERVED_	PANEL_FITTING_VERTICAL_RATIO	RESERVED__1	PANEL_FITTING_HORIZONTAL_RATIO

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED_:** Reads as zeros
28:16	0b RW	**PANEL_FITTING_VERTICAL_RATIO:** Vertical scaling ratio for panel fitting.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0b RW	**RESERVED__1:** Reads as zeros
12:0	0b RW	**PANEL_FITTING_HORIZONTAL_RATIO:** Horizontal scaling ratio for panel fitting.

14.11.46 RESERVEDUSEDTOBEAUTOSCALINGRATIOSREADBACK—Offset 61238h

Reserved.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61238h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**RESERVED:** Reserved.

14.11.47 RESERVEDUSEDTOBESCALINGINITIALPHASE—Offset 6123Ch

Reserved.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6123Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED:** Reserved.

14.11.48 PIPEA_BLC_PWM_CLT2—Offset 61250h

PipeA Backlight PWM Control Register 2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61250h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	PWM_ENABLE
30	0	RESERVED__MBZ
29	0	RESERVED_
28	0	BACKLIGHT_POLARITY
27	0	RESERVED
26	0	PHASE_IN_INTERRUPT_STATUS
25	0	PHASE_IN_ENABLE
24	0	PHASE_IN_INTERRUPT_ENABLE
23:16	0 0 0 0 0 0 0 0	PHASE_IN_TIME_BASE
15:8	0 0 0 0 0 0 0 0	PHASE_IN_COUNT
7:0	0 0 0 0 0 0 0 0	PHASE_IN_INCREMENT

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PWM_ENABLE:** This bit enables the PWM counter logic 0 = PWM disabled (drives 0 always) 1 = PWM enabled
30	0b RW	**RESERVED__MBZ:** Reserved.
29	0b RW	**RESERVED_:** Reserved.
28	0b RW	**BACKLIGHT_POLARITY:** This field controls the polarity of the PWM signal. 0 = Active High 1 = Active Low
27	0b RW	**RESERVED:** MBZ
26	0b RW/1C	**PHASE_IN_INTERRUPT_STATUS:** This bit will be set by hardware when a Phase-In interrupt has occurred. Software will clear this bit by writing a 1 , which will reset the interrupt generation. [DevCL-A,B] Reserved AccessType: One to Clear
25	0b RW	**PHASE_IN_ENABLE:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.

Bit Range	Default & Access	Field Name (ID): Description
24	0b RW	**PHASE_IN_INTERRUPT_ENABLE:** Setting this bit enables an interrupt to be generated when the PWM phase in is completed.
23:16	0b RW	**PHASE_IN_TIME_BASE:** This field determines the number of VBLANK events that pass before one increment occurs. 0 = invalid 1 = 1 vblank 2 = 2 vblanks etc.
15:8	0b RW	**PHASE_IN_COUNT:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time, one must write a dummy value to this field, for example, 0 , before writing the real value for the second time.
7:0	0b RW	**PHASE_IN_INCREMENT:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two s complement number.

14.11.49 PIPEA_BLC_PWM_CTL—Offset 61254h

PipeA Backlight PWM Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61254h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
BACKLIGHT_MODULATION_FREQUENCY	BACKLIGHT_DUTY_CYCLE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**BACKLIGHT_MODULATION_FREQUENCY:** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in display core clocks ([DevCTG] 100MHz HRAW clocks) multiplied by 128 or 25MHz S0IX clocks multiplied by 16.
15:0	0b RW	**BACKLIGHT_DUTY_CYCLE:** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in display core clock ([DevCTG] HRAW clock) periods multiplied by 128 or 25MHz S0IX clocks multipled by 16.

14.11.50 PIPEA_BLM_HIST_CTL—Offset 61260h

PipeA Image Enhancement Histogram Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61260h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED
30	0	IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED
29	0	RESERVED_MBZ_IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT
28:26	0 0 0	RESERVED
25	0	HISTOGRAM_MODE_SELECT
24:17	0 0 0 0 0 0 0 0	SYNC_TO_PHASE_IN_COUNT
16	0	RESERVED_1
15:14	0 0	ENHANCEMENT_MODE
13	0	SYNC_TO_PHASE_IN
12	0	BIN_REGISTER_FUNCTION_SELECT
11:8	0 0 0 0	RESERVED_2
7:0	0 0 0 0 0 0 0 0	BIN_REGISTER_INDEX_READ_ONLY

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED:** This bit enables the Image Enhancement histogram logic to collect data. 0 = Image histogram is disabled 1 = The Image histogram is enabled. When this bit is changed from a zero to a one, histogram calculations will begin after the next VBLANK of the assigned pipe.
30	0b RW	**IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED:** This bit enables the Image Enhancement modification table. 0 = disabled 1 = enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.
29	0b RW	**RESERVED_MBZ_IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT:** Each pipe has its own IE function
28:25	0b RW	**RESERVED:** Always write as 0 s.
24	0b RW	**HISTOGRAM_MODE_SELECT:** 0: YUV Luma Mode 1: HSV Intensity Mode - Reserved on [DevCL]
23:16	0b RW	**SYNC_TO_PHASE_IN_COUNT:** This field indicates the phase in count number on which the Image Enhancement table will be loaded if the Sync to Phase in is enabled.
15	0b RW	**RESERVED_1:** Always write as 0.
14:13	0b RW	**ENHANCEMENT_MODE:** 00: Direct look up mode 01: Additive mode 10: Multiplicative mode - Reserved on [DevCL] 11: Reserved
12	0b RW	**SYNC_TO_PHASE_IN:** Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.
11	0b RW	**BIN_REGISTER_FUNCTION_SELECT:** This field indicates what data is being written to or read from the bin data register. 0 = Bin Threshold Count. A read from the bin data register returns that bin s threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31. 1 = Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32
10:7	0b RW	**RESERVED_2:** Always write as 0's.
6:0	0b RW	**BIN_REGISTER_INDEX_READ_ONLY:** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.

14.11.51 PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61264h

PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER index registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61264h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER_REGISTER_DESCRIPTIONS

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER_REGISTER_DESCRIPTIONS:** PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER indexed register descriptions

14.11.52 PIPEAHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61268h

pipeA histrogram threshhold gurband register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61268h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

HISTOGRAM_INTERRUPT_ENABLE | HISTOGRAM_EVENT_STATUS_READ_ONLY | GUARDBAND_INTERRUPT_DELAY | THRESHOLD_GUARDBAND

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**HISTOGRAM_INTERRUPT_ENABLE:** 0 = Disabled 1 = Enabled. This generates a histogram interrupt once a Histogram event occurs.
30	0b RO	**HISTOGRAM_EVENT_STATUS_READ_ONLY:** When a Histogram event has occured, this will get set by the hardware. For any more Histogram events to occur, the software needs to clear this bit by writing a '1'. The default state for this bit is '0'. 0 = Histogram event has not occurred. 1 = Histogram event has occurred. AccessType: Read Only
29:22	0b RW	**GUARDBAND_INTERRUPT_DELAY:** An interrupt is generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. A value of 0 is invalid.
21:0	0b RW	**THRESHOLD_GUARDBAND:** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

14.11.53 PIPEB_PP_STATUS—Offset 61300h

PipeB Panel Power Status Register ([DevVLVP]) PP Status (dplrreg.v panel_pwr_sr)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61300h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 08000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 1 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PANEL_POWER_ON_STATUS | REQUIRE_ASSET_STATUS | POWER_SEQUENCE_PROGRESS | POWER_CYCLE_DELAY_ACTIVE | RESERVED | INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**PANEL_POWER_ON_STATUS:** 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a 1 to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.
30	0b RO	**REQUIRE_ASSET_STATUS:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled
29:28	0b RO	**POWER_SEQUENCE_PROGRESS:** 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved
27	1b RO	**POWER_CYCLE_DELAY_ACTIVE:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	0b RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0b RO	**INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG:** 0000 = Power Off Idle (S0.0) 0001 = Power Off, Wait for cycle delay (S0.1) 0010 = Power Off (S0.2) 0011 = Power Off (S0.3) 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Power On Idle (S1.0) 1001 = Power On, (S1.1) 1010 = Power On, (S1.2) 1011 = Power On, Wait for cycle delay (S1.3) 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reset

14.11.54 PIPEB_PP_CONTROL—Offset 61304h

PipeB Panel Power Control Register ([DevVLVP]) PP Control (dplrreg.v pnl_pwr_cntl)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61304h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:16	15:4	3	2	1	0
Default	0000 0000 0000 0000	0000 0000 0000	0	0	0	0
Field	WRITE_PROTECT_KEY	RESERVED	EDP_PANEL_VDD_ENABLE	BACKLIGHT_ENABLE	POWER_DOWN_ON_RESET	POWER_STATE_TARGET

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**WRITE_PROTECT_KEY:** ABCD Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write protected. Any write cycles to those write protected registers, while they will complete as normal, will not change the value of the register when write protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write protected registers: (Panel sequencing Registers): Pipe B Panel power on sequencing delays - Address: 61308-6130Bh Pipe B Panel power off sequencing delays Address: 6130Ch 6130Fh Pipe B Panel power cycle delay and Reference Divisor Address: 61310h 61313 (DPLL registers): DPLL Control Registers FPA0 DPLL Divisor Register FPA1 DPLL Divisor Register 1 FPB0 DPLL Divisor Register FPB1 DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL Horizontal Total Register HBLANK Horizontal Blank Register HSYNC_ Horizontal Sync Register VTOTAL_ Vertical Total Register VBLANK_ Vertical Blank Register VSYNC_ Vertical Sync Register
15:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**EDP_PANEL_VDD_ENABLE:** [DevCDV]: Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled [DevCLN] Reserved
2	0b RW	**BACKLIGHT_ENABLE:** [DevCTG, DevCDV]: Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled [DevCL] Reserved
1	0b RW	**POWER_DOWN_ON_RESET:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected 1 = Run panel power down sequence when system is reset
0	0b RW	**POWER_STATE_TARGET:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

14.11.55 PIPEB_PP_ON_DELAYS—Offset 61308h

PipeB Panel Power on Sequencing Delays ([DevVLVP]) PP On Delay values (dplrreg.v DPLRppon_sd)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61308h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PANEL_CONTROL_PORT_SELECT | RESERVED | POWER_UP_DELAY | RESERVED_1 | POWER_ON_TO_BACKLIGHT_ENABLE_DELAY

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**PANEL_CONTROL_PORT_SELECT:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	0b RW	**RESERVED:** Reserved.
28:16	0b RW	**POWER_UP_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	0b RW	**RESERVED_1:** Reserved.
12:0	0b RW	**POWER_ON_TO_BACKLIGHT_ENABLE_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

14.11.56 PIPEB_PP_OFF_DELAYS—Offset 6130Ch

PipeB Panel Power off Sequencing Delays ([DevVLVP]) PP Delay Off values (dplrreg.v DPLRppoff_sd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6130Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:29	Bits 28:16	Bits 15:13	Bits 12:0
RESERVED	POWER_DOWN_DELAY	RESERVED_1	POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RW	**RESERVED:** Reserved.
28:16	0b RW	**POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.
15:13	0b RW	**RESERVED_1:** Reserved.
12:0	0b RW	**POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

14.11.57 PIPEB_PP_DIVISOR—Offset 61310h

PipeB Panel Power Cycle Delay and Reference Divisor ([DevVLVP]) PP Divisor (dplrreg.v DPLRrefdiv_pp_cd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61310h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00270F04h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0
REFERENCE_DIVIDER																								RESERVED			POWER_CYCLE_DELAY				

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000000010011100001111b RW	**REFERENCE_DIVIDER:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value for the display core clock that is for [DevCL and DevCTG] a 200MHz reference value. The following are examples for other memory speeds. Display Core Frequency Value of Field 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	0b RW	**RESERVED:** Reserved.
4:0	00100b RW	**POWER_CYCLE_DELAY:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a +1 value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

14.11.58 PIPEB_BLC_PWM_CLT2—Offset 61350h

PipeB Backlight PWM Control Register 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61350h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	PWM_ENABLE
30	0	RESERVED
29	0	RESERVED_1
28	0	BACKLIGHT_POLARITY
27	0	RESERVED_2
26	0	PHASE_IN_INTERRUPT_STATUS
25	0	PHASE_IN_ENABLE
24	0	PHASE_IN_INTERRUPT_ENABLE
23:16	0 0 0 0 0 0 0 0	PHASE_IN_TIME_BASE
15:8	0 0 0 0 0 0 0 0	PHASE_IN_COUNT
7:0	0 0 0 0 0 0 0 0	PHASE_IN_INCREMENT

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PWM_ENABLE:** This bit enables the PWM counter logic 0 = PWM disabled (drives 0 always) 1 = PWM enabled
30	0b RW	**RESERVED:** MBZ
29	0b RW	**RESERVED_1:** Reserved.
28	0b RW	**BACKLIGHT_POLARITY:** This field controls the polarity of the PWM signal. 0 = Active High 1 = Active Low
27	0b RW	**RESERVED_2:** MBZ
26	0b RW/1C	**PHASE_IN_INTERRUPT_STATUS:** This bit will be set by hardware when a Phase-In interrupt has occurred. Software will clear this bit by writing a 1 , which will reset the interrupt generation. [DevCL-A,B] Reserved AccessType: One to Clear
25	0b RW	**PHASE_IN_ENABLE:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.
24	0b RW	**PHASE_IN_INTERRUPT_ENABLE:** Setting this bit enables an interrupt to be generated when the PWM phase in is completed.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0b RW	**PHASE_IN_TIME_BASE:** This field determines the number of VBLANK events that pass before one increment occurs. 0 = invalid 1 = 1 vblank 2 = 2 vblanks etc.
15:8	0b RW	**PHASE_IN_COUNT:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time, one must write a dummy value to this field, for example, 0 , before writing the real value for the second time.
7:0	0b RW	**PHASE_IN_INCREMENT:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two s complement number.

14.11.59 PIPEB_BLC_PWM_CTL—Offset 61354h

PipeB Backlight PWM Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61354h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
BACKLIGHT_MODULATION_FREQUENCY	BACKLIGHT_DUTY_CYCLE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**BACKLIGHT_MODULATION_FREQUENCY:** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in display core clocks ([DevCTG] HRAW clocks) multiplied by 128 or 25MHz S0IX clocks multipled by 16.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0b RW	**BACKLIGHT_DUTY_CYCLE:** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in display core clock ([DevCTG] HRAW clock) periods multiplied by 128 or 25MHz S0IX clocks multiplied by 16.

14.11.60 PIPEB_BLM_HIST_CTL—Offset 61360h

PipeB Image Enhancement Histogram Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61360h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Field
31	IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED
30	IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED
29	RESERVED_MBZ_IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT
28:25	RESERVED
24	HISTOGRAM_MODE_SELECT
23:16	SYNC_TO_PHASE_IN_COUNT
15	RESERVED_1
14:13	ENHANCEMENT_MODE
12	SYNC_TO_PHASE_IN
11	BIN_REGISTER_FUNCTION_SELECT
10:7	RESERVED_2
6:0	BIN_REGISTER_INDEX_READ_ONLY

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED:** This bit enables the Image Enhancement histogram logic to collect data. 0 = Image histogram is disabled 1 = The Image histogram is enabled. When this bit is changed from a zero to a one, histogram calculations will begin after the next VBLANK of the assigned pipe.

Bit Range	Default & Access	Field Name (ID): Description
30	0b RW	**IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED:** This bit enables the Image Enhancement modification table. 0 = disabled 1 = enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.
29	0b RW	**RESERVED_MBZ_IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT:** Each pipe has its own dedicated IE function.
28:25	0b RW	**RESERVED:** Always write as 0 s.
24	0b RW	**HISTOGRAM_MODE_SELECT:** 0: YUV Luma Mode 1: HSV Intensity Mode - Reserved on [DevCL]
23:16	0b RW	**SYNC_TO_PHASE_IN_COUNT:** This field indicates the phase in count number on which the Image Enhancement table will be loaded if the Sync to Phase in is enabled.
15	0b RW	**RESERVED_1:** Always write as 0.
14:13	0b RW	**ENHANCEMENT_MODE:** 00: Direct look up mode 01: Additive mode 10: Multiplicative mode - Reserved on [DevCL] 11: Reserved
12	0b RW	**SYNC_TO_PHASE_IN:** Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.
11	0b RW	**BIN_REGISTER_FUNCTION_SELECT:** This field indicates what data is being written to or read from the bin data register. 0 = Bin Threshold Count. A read from the bin data register returns that bin s threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31. 1 = Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32
10:7	0b RW	**RESERVED_2:** Always write as 0's.
6:0	0b RO	**BIN_REGISTER_INDEX_READ_ONLY:** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set. AccessType: Read Only

14.11.61 PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61364h

PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER index registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61364h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER_REGISTER_DESCRIPTIONS

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER_REGISTER_DESCRIPTIONS:** PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER indexed register descriptions

14.11.62 PIPEBHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61368h

pipe B histogram threshhold gurband register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61368h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

HISTOGRAM_INTERRUPT_ENABLE	HISTOGRAM_EVENT_STATUS_READ_ONLY	GUARDBAND_INTERRUPT_DELAY	THRESHOLD_GUARDBAND

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**HISTOGRAM_INTERRUPT_ENABLE:** 0 = Disabled 1 = Enabled. This generates a histogram interrupt once a Histogram event occurs.
30	0b RO	**HISTOGRAM_EVENT_STATUS_READ_ONLY:** When a Histogram event has occured, this will get set by the hardware. For any more Histogram events to occur, the software needs to clear this bit by writing a '1'. The default state for this bit is '0'. 0 = Histogram event has not occurred. 1 = Histogram event has occurred. AccessType: Read Only
29:22	0b RW	**GUARDBAND_INTERRUPT_DELAY:** An interrupt is generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. A value of 0 is invalid.
21:0	0b RW	**THRESHOLD_GUARDBAND:** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

14.11.63 MIPIC_PORT_CTRL—Offset 61700h

mipi C port ctrl

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61700h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

EN	RESERVED	DITHER	RESERVED_1	RESERVED_2	RESERVED_3	RESERVED_4	RESERVED_5	RESERVED_6	RESERVED_7	DELAY	EFFECT	RESERVED_8

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**EN:** When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enable it starts to generate timing for this MIPI port 0 = The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 = The port is enabled
30:26	0b RW	**RESERVED:** Reserved.
25	0b RW	**DITHER:** This bit enables or disables (bypassing) 8-6-bit color dithering function. The usage of this bit would be on for 18-bpp panels and off for 24-bpp panels. 0 = disabled 1 = enabled
24:22	0b RW	**RESERVED_1:** Reserved.
21	0b RW	**RESERVED_2:** Reserved.
20	0b RW	**RESERVED_3:** Reserved.
19	0b RW	**RESERVED_4:** Reserved.
18:16	0b RW	**RESERVED_5:** Reserved.
15	0b RW	**RESERVED_6:** Reserved.
14:5	0b RW	**RESERVED_7:** Reserved.
4	0b RW	**DELAY:** When set, the TE counter will be count down until
3:2	0b RW	**EFFECT:** 00: No tearing effect required - memory write start as soon as write data is available 01: TE trigger by MIPI DPHY and DSI protocol 10: TE trigger by GPIO pin 11: Reserved
1:0	0b RW	**RESERVED_8:** Reserved.

14.11.64 MIPIC_TEARING_CTR—Offset 61704h

mipi C tearing ctr

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 61704h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Field	Bits	Default
RESERVED	31:16	0000 0000 0000 0000
TE	15:0	0000 0000 0000 0000

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**RESERVED:** Reserved.
15:0	0b RW	**TE:** Number of delay clocks from TE trigger to start sending data to DSI controller

14.11.65 AUD_CONFIG_A—Offset 62000h

Audio Configuration Pipe A

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Field	Bits	Default
RESERVED	31:30	00
N_VALUE_INDEX	29	0
N_PROGRAMMING_ENABLE_TESTMODE	28	0
UPPER_N_VALUE_TESTMODE	27:20	0000 0000
PIXEL_CLOCK_HDMI	19:16	0000
LOWER_N_VALUE_TESTMODE	15:4	0000 0000 0000
DISABLE_NCTS	3	0
RESERVED_1	2:0	000

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
29	0b RW	**N_VALUE_INDEX:** Project: All Default Value: 0b Value Name Description Project 0b HDMI N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6. All 1b DP N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value default h8000. All
28	0b RW	**N_PROGRAMMING_ENABLE_TESTMODE:** Project: All Security: Test This bit enables programming of N values for non-CEA modes. Please note that the Pipe to which audio is attached must be disabled when changing this field.
27:20	0b RW	**UPPER_N_VALUE_TESTMODE:** Project: All Security: Test These are bits [19:12] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field. This register can also be used to program N value for DP for a specific Port. Default value on this register when bit 29 is set to 1 is h7FA6
19:16	0b RW	**PIXEL_CLOCK_HDMI:** Project: All Default Value: 0b This is the target frequency of the CEA/HDMI video mdoe to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DP Link clock. DP Link clock does not require this programming. Note: The Pipe on which audio is attached must be disabled when changing this field. Value Name Description Project 0000b 25.2 / 1.001 MHz 25.2 / 1.001 MHz All 0001b 25.2 MHz 25.2 MHz Program this value for pixel clocks not listed in this field All 0010b 27 MHz 27 MHz All 0011b 27 * 1.001 MHz 27 * 1.001 MHz All 0100b 54 MHz 54 MHz All 0101b 54 * 1.001 MHz 54 * 1.001 MHz All 0110b 74.25 / 1.001 MHz 74.25 / 1.001 MHz All 0111b 74.25 MHz 74.25 MHz All 1000b 148.5 / 1.001 MHz 148.5 / 1.001 MHz All 1001b 148.5 MHz 148.5 MHz All Others Reserved Reserved All
15:4	0b RW	**LOWER_N_VALUE_TESTMODE:** Project: All Security: Test These are bits [11:0] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field. This register can also be used to program N value for DP for a specific Port. Default value on this register when bit 29 is set to 1 is h7FA6
3	0b RW	**DISABLE_NCTS:** Project: All Set this bit to disable N and CTS or M generation for CTM modes. This is to enable prediction of CRC in CTM modes.
2:0	0b RW	**RESERVED_1:** Project: All Format:

14.11.66 AUD_MISC_CTRL_A—Offset 62010h

Audio MISC Control for Pipe A

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000044h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 1 0 0 | 0 1 0 0

RESERVED | SAMPLE_PRESENT_DISABLE | OUTPUT_DELAY | RESERVED_1 | SAMPLE_FABRICATION_EN_BIT | PRO_ALLOWED | RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**RESERVED:** Project: All Format: MBZ
8	0b RW	**SAMPLE_PRESENT_DISABLE:** Project: All Security: Debug This bit is used to Disable sample present for HDMI or DP (Chicken Bit)
7:4	0100b RW	**OUTPUT_DELAY:** Project: All Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
3	0b RW	**RESERVED_1:** Project: All Format: MBZ
2	1b RW	**SAMPLE_FABRICATION_EN_BIT:** Project: All Access: R/W Default Value: ;1b This bit indicates whether internal fabrication of audio samples is enabled during a link underrun. Value Name Description Project 0b Disable Audio fabrication disabled All 1b Enable Audio fabrication enabled All
1	0b RW	**PRO_ALLOWED:** Project: All Access: R/W Default Value: 0b By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode. Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb. Value Name Description Project 0b Consumer Consumer use only All 1b Professional Professional use allowed All
0	0b RW	**RESERVED_2:** All Format: MBZ

14.11.67 AUD_VID_DID—Offset 62020h

Audio Vendor ID / Device ID

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 80862882h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0

VENDOR_ID (31:16), DEVICE_ID (15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	1000000010000110b RO	**VENDOR_ID:** Project: All Format: U16 Used to identify the codec within the PnP system. This field is hardwired within the device. Value = 0x8086
15:0	0010100010000010b RO	**DEVICE_ID:** Project: All Format: U16 Constant used to identify the codec within the PnP system. This field is set by the device hardware. Value = 0x2882 [Valleyview2]

14.11.68 AUD_RID—Offset 62024h

Audio Revision ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:24), MAJOR_REVISION (23:20), MINOR_REVISION (19:16), REVISION_ID (15:8), STEPPING_ID (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:20	0001b RO	**MAJOR_REVISION:** Project: All Default Value: 0001b The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x1
19:16	0b RO	**MINOR_REVISION:** Project: All The minor revision number (rights of the decimal) or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x0
15:8	0b RO	**REVISION_ID:** Project: All The vendors revision number for this given Device ID. This field is hardwired within the device. Value = 0x0

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b RO	**STEPPING_ID:** Project: All An optional vendor stepping number within the given Revision ID. This field is hardwired within the device. Value = 0x0

14.11.69 AUD_CTS_ENABLE_A—Offset 62028h

Audio CTS Programming Enable Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED
CTS_M_VALUE_INDEX
ENABLE_CTS_OR_M_PROGRAMMING
CTS_PROGRAMMING

Bit Range	Default & Access	Field Name (ID): Description
31:22	0b RW	**RESERVED:** Project: All Format:
21	0b RW	**CTS_M_VALUE_INDEX:** Project: All Default Value: 0b Value Name Description Project 0b CTS CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS value. default is 0 All 1b M M value read on bits 21:4 reflects DP M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value All
20	0b RW	**ENABLE_CTS_OR_M_PROGRAMMING:** Project: All When set will enable CTS or M programming.
19:0	0b RW	**CTS_PROGRAMMING:** Project: All These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field.

14.11.70 AUD_PWRST—Offset 6204Ch

Audio Power State (Function Group, Convertor, Pin Widget)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6204Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00FFFFFFh

31 28 24	20		16		12		8		4		0
0 0 0 0 0 0 0 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1
RESERVED	FUNCTION_GROUP_DEVICE_POWER_STATE_CURRENT	FUNCTION_GROUP_DEVICE_POWER_STATE_SET	CONVERTORB_WIDGET_POWER_STATE_CURRENT	CONVERTORB_WIDGET_POWER_STATE_REQUESTED	CONVERTORA_WIDGET_POWER_STATE_CURRENT	CONVERTORA_WIDGET_POWER_STATE_REQUSTED	PIND_WIDGET_POWER_STATE_CURRENT	PIND_WIDGET_POWER_STATE_SET	PINC_WIDGET_POWER_STATE_CURRENT	PINC_WIDGET_POWER_STATE_SET	PINB_WIDGET_POWER_STATE_CURRENT	PINB_WIDGET_POWER_STATE_SET

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:22	11b RO	**FUNCTION_GROUP_DEVICE_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
21:20	11b RO	**FUNCTION_GROUP_DEVICE_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All

Bit Range	Default & Access	Field Name (ID): Description
19:18	11b RO	**CONVERTORB_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
17:16	11b RO	**CONVERTORB_WIDGET_POWER_STATE_REQUESTED:** Project: All Format: Audio Power State Format Power state that was requested by audio software Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
15:14	11b RO	**CONVERTORA_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
13:12	11b RO	**CONVERTORA_WIDGET_POWER_STATE_REQUSTED:** Project: All Format: Audio Power State Format Power state that was requested by audio software Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
11:10	11b RO	**PIND_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
9:8	11b RO	**PIND_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
7:6	11b RO	**PINC_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All

Bit Range	Default & Access	Field Name (ID): Description
5:4	11b RO	**PINC_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
3:2	11b RO	**PINB_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Current power state
1:0	11b RO	**PINB_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All

14.11.71 AUD_HDMIW_HDMIEDID_A—Offset 62050h

HDMI Data EDID Block Pipe A

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EDID_HDMI_DATA_BLOCK

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**EDID_HDMI_DATA_BLOCK:** Project: All Format: Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during gfx reset

14.11.72 AUD_HDMIW_INFOFR_A—Offset 62054h

Audio Widget Data Island Packet Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DATA_ISLAND_PACKET_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**DATA_ISLAND_PACKET_DATA:** Project: All Format: This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

14.11.73 AUD_PORT_EN_HD_CFG—Offset 6207Ch

Audio Port Enable HDAudio Config

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6207Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00077003h

Bits	Default	Field
31:19	0 0 0 0 0 0 0 0 0 0 0 0 0	RESERVED
18	1	PORT_D_AMP_MUTE_STATUS
17	1	PORT_C_AMP_MUTE_STATUS
16	1	PORT_B_AMP_MUTE_STATUS
15	0	RESERVED_1
14	1	PORT_D_OUT_ENABLE
13	1	PORT_C_OUT_ENABLE
12	1	PORT_B_OUT_ENABLE
11:8	0 0 0 0	CONVERTORB_STREAM_ID
7:4	0 0 0 0	CONVERTORA_STREAM_ID
3:2	0 0	RESERVED_2
1	1	CONVERTOR_B_DIGEN
0	1	CONVERTOR_A_DIGEN

Bit Range	Default & Access	Field Name (ID): Description
31:19	0b RO	**RESERVED:** Project: All Format:
18	1b RO	**PORT_D_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
17	1b RO	**PORT_C_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
16	1b RO	**PORT_B_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
15	0b RO	**RESERVED_1:** Project: All Format:
14	1b RO	**PORT_D_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
13	1b RO	**PORT_C_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
12	1b RO	**PORT_B_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
11:8	0b RO	**CONVERTORB_STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)

Bit Range	Default & Access	Field Name (ID): Description
7:4	0b RO	**CONVERTORA_STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
3:2	0b RO	**RESERVED_2:** Project: All Format:
1	1b RO	**CONVERTOR_B_DIGEN:** Project: All Default Value: ;1b Digital Transmission Enabled Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Block Digital data is blocked from passing through the node, regardless of the state All 1b Pass Digital data can pass through the node (Default) All
0	1b RO	**CONVERTOR_A_DIGEN:** Project: All Default Value: ;1b Digital Transmission Enabled Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Block Digital data is blocked from passing through the node, regardless of the state All 1b Pass Digital data can pass through the node (Default) All

14.11.74 AUD_OUT_DIG_CNVT_A—Offset 62080h

Audio Digital Converter Conv A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:24	23:20	19:16	15	14:8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
Field	RESERVED	STREAM_ID	LOWEST_CHANNEL_NUMBER	RESERVED_1	CATEGORY_CODE	LEVEL	PRO	NON_AUDIO	COPY	PRE	VCFG	V	RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
23:20	0b RO	**STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
19:16	0b RO	**LOWEST_CHANNEL_NUMBER:** Project: All Format: Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0b RO	**RESERVED_1:** Project: All Format:
14:8	0b RO	**CATEGORY_CODE:** Project: All Format: S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0b RO	**LEVEL:** Project: All Format: S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0b RO	**PRO:** Project: All Default Value: 0b This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use All 1b Professional Professional use All
5	0b RO	**NON_AUDIO:** Project: All Default Value: 0b Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM All 1b Non PCM Data is non PCM format All
4	0b RO	**COPY:** Project: All Default Value: 0b Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0b RO	**PRE:** Project: All Default Value: 0b Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Disabled Preemphasis is disabled All 1b Enabled Filter preemphasis is enabled All
2	0b RO	**VCFG:** Project: All Format: Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	0b RO	**V:** Project: All Format: Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	0b RO	**RESERVED_2:** All Format: MBZ

14.11.75 AUD_OUT_STR_DESC_A—Offset 62084h

Audio Stream Descriptor Format Conv A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62084h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000032h

Bits	31:29	28:27	26:21	20:16	15	14	13:11	10:8	7	6:4	3:0
Default	000	00	000000	00000	0	0	000	000	0	011	0010
Field	RESERVED	HBR_ENABLE	RESERVED_1	CONVERTOR_CHANNEL_COUNT	RESERVED_2	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULT	SAMPLE_BASE_RATE_DIVISOR	RESERVED_3	BITS_PER_SAMPLE	NUMBER_OF_CHANNELS_IN_A_STREAM

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RO	**RESERVED:** Project: All Format:
28:27	0b RO	**HBR_ENABLE:** Project: All Format: This reflects the current HBR settings.
26:21	0b RO	**RESERVED_1:** Project: All Format:
20:16	0b RO	**CONVERTOR_CHANNEL_COUNT:** Project: All Format: This reflects the Convertor Channel Count programmed through HDAudio.
15	0b RO	**RESERVED_2:** Project: All Format:
14	0b RO	**SAMPLE_BASE_RATE:** Project: All Default Value: 0b 48 kHz Sampling base rate of audio stream. Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0b RO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: 000b 48 kHz Audio stream sample base rate multiple. Value Name Description Project 000b x1 x1 (48 kHz/44.1 kHz or less) All 001b x2 x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b x3 x3 (144 kHz) All 011b x4 x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved All

Bit Range	Default & Access	Field Name (ID): Description
10:8	0b RO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: 000b 48 kHz Audio stream sample base rate divisor. Value Name Description Project 000b Div 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Div 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Div 3 Divide by 3 (16 kHz, 32 kHz) All 011b Div 4 Divide by 4 (11.025 kHz) All 100b Div 5 Divide by 5 (9.6 kHz) All 101b Div 6 Divide by 6 (8 kHz) All 110b Div 7 Divide by 7 All 111b Div 8 Divide by 8 (6 kHz) All
7	0b RO	**RESERVED_3:** Project: All Format: MBZ
6:4	011b RO	**BITS_PER_SAMPLE:** Project: All Default Value: 011b 32 bits Value Name Description Project 000b 8 bit The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 100b 20 bits The data will be packed in memory in 20 bit containers on 32 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved All
3:0	0010b RO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Default Value: 0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 Number of channels in each frame of the stream.

14.11.76 AUD_OUT_CH_STR—Offset 62088h

Audio Channel ID and Stream ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62088h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED		CONVERTER_CHANNEL_MAP_PORTD	DIGITAL_DISPLAY_AUDIO_INDEX_PORTD	CONVERTER_CHANNEL_MAP_PORTC	HDMI_INDEX_PORTC	CONVERTER_CHANNEL_MAP_PORTB	HDMI_INDEX_PORTB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:20	0b RO	**CONVERTER_CHANNEL_MAP_PORTD:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 19:16 is mapped. This field is read only
19:16	0b RO	**DIGITAL_DISPLAY_AUDIO_INDEX_PORTD:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 20:23 of this register.
15:12	0b RO	**CONVERTER_CHANNEL_MAP_PORTC:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 11:8 is mapped. This field is read only
11:8	0b RO	**HDMI_INDEX_PORTC:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 12:15 of this register.
7:4	0b RO	**CONVERTER_CHANNEL_MAP_PORTB:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 3:0 is mapped. This field is read only
3:0	0b RO	**HDMI_INDEX_PORTB:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 4:7 of this register.

14.11.77 AUD_PINW_CONNLNG_LIST—Offset 620A8h

Audio Connection List

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 620A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00030202h

Bits	31:24	23:8	7	6:0
Value	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1 0 0 0 0 0 0 1 0	0	0 0 0 0 0 1 0
Field	RESERVED	CONNECTION_LIST_ENTRY	LONG_FORM	CONNECTION_LIST_LENGTH

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:8	0000001100000010b RO	**CONNECTION_LIST_ENTRY:** Project: All Default Value: 0000001100000010b Connection to Convertor Widget Node 0x0302
7	0b RO	**LONG_FORM:** Project: All Default Value: 0b This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)
6:0	10b RO	**CONNECTION_LIST_LENGTH:** Project: All Default Value: 02h This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

14.11.78 AUD_PINW_CONNLNG_SEL—Offset 620ACh

Audio Connection Select

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 620ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:24	23:16	15:8	7:0
Default	0000 0000	0000 0000	0000 0000	0000 0000
Field	RESERVED	CONNECTION_SELECT_CONTROL_D	CONNECTION_SELECT_CONTROL_C	CONNECTION_SELECT_CONTROL_B

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:16	0b RO	**CONNECTION_SELECT_CONTROL_D:** Project: All Format: Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x00
15:8	0b RO	**CONNECTION_SELECT_CONTROL_C:** Project: All Format: Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00
7:0	0b RO	**CONNECTION_SELECT_CONTROL_B:** Project: All Format: Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00

14.11.79 AUD_CNTL_ST_A—Offset 620B4h

Audio Control State Register Pipe A

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 620B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00005400h

Bits	31	30:29	28:25	24:21	20:18	17:16	15	14:10	9:5	4	3:0
Default	0	00	0000	0000	000	00	0	10101	00000	0	0000
Field	RESERVED	DIP_PORT_SELECT	RESERVED_1	DIP_TYPE_ENABLE_STATUS	DIP_BUFFER_INDEX	DIP_TRANSMISSION_FREQUENCY	RESERVED_2	ELD_BUFFER_SIZE	ELD_ACCESS_ADDRESS	ELD_ACK	DIP_RAM_ACCESS_ADDRESS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:29	0b RO	**DIP_PORT_SELECT:** Project: All AccessType: Read Only Default Value: 00b This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B All 10b Digital Port C Digital Port C All 11b Digital Port D Digital Port D All
28:25	0b RW	**RESERVED_1:** Project: All Format: MBZ
24:21	0b RO	**DIP_TYPE_ENABLE_STATUS:** Project: All AccessType: Read Only Default Value: 0000b These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. Value Name Description Project XXX0b Disable Audio DIP disabled All XXX1b Enable Audio DIP enabled All XX0Xb Disable Generic 1 (ACP) DIP disabled All XX1Xb Enable Generic 1 (ACP) DIP enabled All X0XXb Disable Generic 2 DIP disabled All X1XXb Enable Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 All 1XXXb Reserved Reserved All
20:18	0b RW	**DIP_BUFFER_INDEX:** Project: All Default Value: 0000b This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s. Value Name Description Project 000b Audio Audio DIP (31 bytes of address space, 31 bytes of data) All 001b Gen 1 Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data) All 010b Gen 2 Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) All 011b Gen 3 Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) All 1XXb Reserved Reserved All
17:16	0b RO	**DIP_TRANSMISSION_FREQUENCY:** Project: All AccessType: Read Only Default Value: 00b These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. Value Name Description Project 00b Disable Disabled All 01b Reserved Reserved All 10b Send Once Send Once All 11b Best Effort Best effort (Send at least every other vsync) All
15	0b RW	**RESERVED_2:** Project: All Format: MBZ
14:10	10101b RO	**ELD_BUFFER_SIZE:** Project: All AccessType: Read only 10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

Bit Range	Default & Access	Field Name (ID): Description
9:5	0b RW	**ELD_ACCESS_ADDRESS:** Project: All Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0b RO	**ELD_ACK:** Project: All AccessType: Read Only Acknowledgement from the audio driver that ELD read has been completed
3:0	0b RO	**DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read Only Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

14.11.80 AUD_CNTL_ST2—Offset 620C0h

Audio Control State 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 620C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:10	9	8	7:6	5	4	3:2	1	0
Value	0000 0000 0000 0000 0000 00	0	0	00	0	0	00	0	0
Field	RESERVED	CP_READYD	ELD_VALIDD	RESERVED_1	CP_READYC	ELD_VALIDC	RESERVED_2	CP_READYB	ELD_VALIDB

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**RESERVED:** Project: All Format:
9	0b RW	**CP_READYD:** Project: All Default Value: 0b This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. Value Name Description Project 0b Pending or Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
8	0b RW	**ELD_VALIDD:** Project: All Default Value: 0b This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All

Bit Range	Default & Access	Field Name (ID): Description
7:6	0b RW	**RESERVED_1:** Project: All Format:
5	0b RW	**CP_READYC:** Project: All Default Value: 0b See CP_ReadyD description. Value Name Description Project 0b Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
4	0b RW	**ELD_VALIDC:** Project: All Default Value: 0b See ELD_validD descripion. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All
3:2	0b RW	**RESERVED_2:** Project: All Format:
1	0b RW	**CP_READYB:** Project: All Default Value: 0b See CP_ReadyD description. Value Name Description Project 0b Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
0	0b RW	**ELD_VALIDB:** Project: All Default Value: 0b See ELD_validD descripion. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All

14.11.81 AUD_HDMIW_STATUS—Offset 620D4h

Audio HDMI Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 620D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CONV_B_CDCLK_DOTCLK_FIFO_UNDERRUN	CONV_B_CDCLK_DOTCLK_FIFO_OVERRUN	CONV_A_CDCLK_DOTCLK_FIFO_UNDERRUN	CONV_A_CDCLK_DOTCLK_FIFO_OVERRUN	RESERVED		BCLK_CDCLK_FIFO_OVERRUN	FUNCTION_RESET	RESERVED_1																							

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**CONV_B_CDCLK_DOTCLK_FIFO_UNDERRUN:** Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
30	0b RW	**CONV_B_CDCLK_DOTCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
29	0b RW	**CONV_A_CDCLK_DOTCLK_FIFO_UNDERRUN:** Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
28	0b RW	**CONV_A_CDCLK_DOTCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
27:26	0b RW	**RESERVED:** Project: All Format:
25	0b RW	**BCLK_CDCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between BCLK and CDCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
24	0b RW	**FUNCTION_RESET:** Project: All Security: Debug This bit indicates that an audio function reset occurred through the reset signal on the HD audio bus. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
23:0	0b RW	**RESERVED_1:** Project: All Format:

14.11.82 AUD_CONFIG_B—Offset 62100h

Audio Configuration Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | N_VALUE_INDEX | N_PROGRAMMING_ENABLE_TESTMODE | UPPER_N_VALUE_TESTMODE | PIXEL_CLOCK_HDMI | LOWER_N_VALUE_TESTMODE | DISABLE_NCTS | RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** Project: All Format:
29	0b RW	**N_VALUE_INDEX:** Project: All Default Value: 0b Value Name Description Project 0b HDMI N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6. All 1b DP N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value default h8000. All
28	0b RW	**N_PROGRAMMING_ENABLE_TESTMODE:** Project: All Security: Test See Pipe A description.
27:20	0b RW	**UPPER_N_VALUE_TESTMODE:** Project: All Security: Test See Pipe A description

Bit Range	Default & Access	Field Name (ID): Description
19:16	0b RW	**PIXEL_CLOCK_HDMI:** Project: All Default Value: 0b See Pipe A description. Value Name Description Project 0000b 25.2 / 1.001 MHz 25.2 / 1.001 MHz All 0001b 25.2 MHz 25.2 MHz Program this value for pixel clocks not listed in this field All 0010b 27 MHz 27 MHz All 0011b 27 * 1.001 MHz 27 * 1.001 MHz All 0100b 54 MHz 54 MHz All 0101b 54 * 1.001 MHz 54 * 1.001 MHz All 0110b 74.25 / 1.001 MHz 74.25 / 1.001 MHz All 0111b 74.25 MHz 74.25 MHz All 1000b 148.5 / 1.001 MHz 148.5 / 1.001 MHz All 1001b 148.5 MHz 148.5 MHz All others Reserved Reserved All
15:4	0b RW	**LOWER_N_VALUE_TESTMODE:** Project: All Security: Test See Pipe A description
3	0b RW	**DISABLE_NCTS:** Project: All See Pipe A description
2:0	0b RW	**RESERVED_1:** Project: All Format:

14.11.83 AUD_MISC_CTRL_B—Offset 62110h

Audio MISC Control for Pipe B

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000044h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Bits 31:9	Bit 8	Bits 7:4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	SAMPLE_PRESENT_DISABLE	OUTPUT_DELAY	RESERVED_1	SAMPLE_FABRICATION_EN_BIT	PRO_ALLOWED	RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
8	0b RW	**SAMPLE_PRESENT_DISABLE:** Project: All Security: Debug See Pipe A description
7:4	0100b RW	**OUTPUT_DELAY:** Project: All Default Value: 0100b See Pipe A description.
3	0b RW	**RESERVED_1:** Project: All Format: MBZ
2	1b RW	**SAMPLE_FABRICATION_EN_BIT:** Project: All Access: R/W Default Value: ;1b See Pipe A description. Value Name Description Project 0b Disable Audio fabrication disabled All 1b Enable Audio fabrication enabled All
1	0b RW	**PRO_ALLOWED:** Project: All Access: R/W Default Value: 0b See Pipe A description. Value Name Description Project 0b Consumer Consumer use only All 1b Professional Professional use allowed All
0	0b RW	**RESERVED_2:** All Format: MBZ

14.11.84 AUD_CTS_ENABLE_B—Offset 62128h

Audio CTS Programming Enable Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62128h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED

CTS_M_VALUE_INDEX

ENABLE_CTS_OR_M_PROGRAMMING

CTS_PROGRAMMING

Bit Range	Default & Access	Field Name (ID): Description
31:22	0b RW	**RESERVED:** Project: All Format:
21	0b RW	**CTS_M_VALUE_INDEX:** Project: All Default Value: 0b Value Name Description Project 0b CTS CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS value. default is 0 All 1b M M value read on bits 21:4 reflects DP M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value All
20	0b RW	**ENABLE_CTS_OR_M_PROGRAMMING:** Project: All See Pipe A description.
19:0	0b RW	**CTS_PROGRAMMING:** Project: All See Pipe A description.

14.11.85 AUD_HDMIW_HDMIEDID_B—Offset 62150h

HDMI Data EDID Block Pipe B

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62150h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EDID_HDMI_DATA_BLOCK

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**EDID_HDMI_DATA_BLOCK:** Project: All Format: See Pipe A description

14.11.86 AUD_HDMIW_INFOFR_B—Offset 62154h

Audio Widget Data Island Packet Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62154h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA_ISLAND_PACKET_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**DATA_ISLAND_PACKET_DATA:** Project: All Format: See Pipe A description.

14.11.87 AUD_OUT_DIG_CNVT_B—Offset 62180h

Audio Digital Converter Conv B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62180h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								STREAM_ID				LOWEST_CHANNEL_NUMBER				RESERVED_1	CATEGORY_CODE							LEVEL	PRO	NON_AUDIO	COPY	PRE	VCFG	V	RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format:
23:20	0b RO	**STREAM_ID:** Project: All Format: See Conv A description.
19:16	0b RO	**LOWEST_CHANNEL_NUMBER:** Project: All Format: See Conv A description
15	0b RO	**RESERVED_1:** Project: All Format:
14:8	0b RO	**CATEGORY_CODE:** Project: All Format: See Conv A description
7	0b RO	**LEVEL:** Project: All Format: See Conv A description
6	0b RO	**PRO:** Project: All Default Value: 0b See Conv A description Value Name Description Project 0b Consumer Consumer use All 1b Professional Professional use All
5	0b RO	**NON_AUDIO:** Project: All Default Value: 0b See Conv A description. Value Name Description Project 0b PCM Data is PCM All 1b Non PCM Data is non PCM format All
4	0b RO	**COPY:** Project: All Default Value: 0b See Conv A description Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0b RO	**PRE:** Project: All Default Value: 0b See Conv A description Value Name Description Project 0b Disabled Preemphasis is disabled All 1b Enabled Filter preemphasis is enabled All
2	0b RO	**VCFG:** Project: All Format: See Conv A description
1	0b RO	**V:** Project: All Format: See Conv A description

Bit Range	Default & Access	Field Name (ID): Description
0	0b RO	**RESERVED_2:** All Format: MBZ

14.11.88 AUD_OUT_STR_DESC_B—Offset 62184h

Audio Stream Descriptor Format Conv B

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62184h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000032h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

RESERVED	HBR_ENABLE	RESERVED_1	CONVERTOR_CHANNEL_COUNT	RESERVED_2	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULT	SAMPLE_BASE_RATE_DIVISOR	RESERVED_3	BITS_PER_SAMPLE	NUMBER_OF_CHANNELS_IN_A_STREAM

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b RO	**RESERVED:** Project: All Format:
28:27	0b RO	**HBR_ENABLE:** Project: All Format: See Conv A description.
26:21	0b RO	**RESERVED_1:** Project: All Format:
20:16	0b RO	**CONVERTOR_CHANNEL_COUNT:** Project: All Format: See Conv A description.
15	0b RO	**RESERVED_2:** Project: All Format:
14	0b RO	**SAMPLE_BASE_RATE:** Project: All Default Value: 0b 48 kHz See Conv A description. Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All

Bit Range	Default & Access	Field Name (ID): Description
13:11	0b RO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: 000b 48 kHz See Conv A description. Value Name Description Project 000b x1 x1 (48 kHz/44.1 kHz or less) All 001b x2 x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b x3 x3 (144 kHz) All 011b x4 x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved All
10:8	0b RO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: 000b 48 kHz See Conv A description. Value Name Description Project 000b Div 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Div 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Div 3 Divide by 3 (16 kHz, 32 kHz) All 011b Div 4 Divide by 4 (11.025 kHz) All 100b Div 5 Divide by 5 (9.6 kHz) All 101b Div 6 Divide by 6 (8 kHz) All 110b Div 7 Divide by 7 All 111b Div 8 Divide by 8 (6 kHz) All
7	0b RO	**RESERVED_3:** Project: All Format: MBZ
6:4	011b RO	**BITS_PER_SAMPLE:** Project: All Default Value: 011b 32 bits Value Name Description Project 000b 8 bit The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 100b 20 bits The data will be packed in memory in 20 bit containers on 32 bit boundaries All 010b 24 bits The data will be packed in memory in 24 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All others Res. Reserved All
3:0	0010b RO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Default Value: 0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 See Conv A description.

14.11.89 AUD_CNTL_ST_B—Offset 621B4h

Audio Control State Register Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 621B4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00005400h

31	30:29	28:25	24:21	20:18	17:16	15	14:10	9:5	4	3:0
0	0 0	0 0 0 0	0 0 0 0	0 0 0	0 0	0	1 0 1 0 1	0 0 0 0 0	0	0 0 0 0
RESERVED	DIP_PORT_SELECT	RESERVED_1	DIP_TYPE_ENABLE_STATUS	DIP_BUFFER_INDEX	DIP_TRANSMISSION_FREQUENCY	RESERVED_2	ELD_BUFFER_SIZE	ELD_ACCESS_ADDRESS	ELD_ACK	DIP_RAM_ACCESS_ADDRESS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Project: All Format: MBZ
30:29	0b RO	**DIP_PORT_SELECT:** Project: All AccessType: Read Only Default Value: 00b See Pipe A description. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B All 10b Digital Port C Digital Port C All 11b Digital Port D Digital Port D All
28:25	0b RW	**RESERVED_1:** Project: All Format: MBZ
24:21	0b RO	**DIP_TYPE_ENABLE_STATUS:** Project: All AccessType: Read Only Default Value: 0000b See Pipe A description. Value Name Description Project XXX0b Disable Audio DIP disabled (Default) All XXX1b Enable Audio DIP enabled All XX0Xb Disable Generic 1 (ACP) DIP disabled All XX1Xb Enable Generic 1 (ACP) DIP enabled All X0XXb Disable Generic 2 DIP disabled All X1XXb Enable Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 All 1XXXb Reserved Reserved All
20:18	0b RW	**DIP_BUFFER_INDEX:** Project: All Default Value: 000b See Pipe A description. Value Name Description Project 000b Audio Audio DIP (31 bytes of address space, 31 bytes of data) All 001b Gen 1 Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) All 010b Gen 2 Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) All 011b Gen 3 Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) All 1XXb Reserved Reserved All

Bit Range	Default & Access	Field Name (ID): Description
17:16	0b RO	**DIP_TRANSMISSION_FREQUENCY:** Project: All AccessType: Read Only Default Value: 00b See Pipe A description Value Name Description Project 00b Disable Disabled All 01b Reserved Reserved All 10b Send Once Send Once All 11b Best Effort Best effort (Send at least every other vsync) All
15	0b RW	**RESERVED_2:** Project: All Format: MBZ
14:10	10101b RO	**ELD_BUFFER_SIZE:** Project: All AccessType: Read Only 10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)
9:5	0b RW	**ELD_ACCESS_ADDRESS:** Project: All See Pipe A description.
4	0b RO	**ELD_ACK:** Project: All AccessType: Read Only See Pipe A description.
3:0	0b RO	**DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read only See Pipe A description.

14.11.90 AUD_SSID_DBG—Offset 62F00h

audio SSID debug

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F00h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 80860101h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

SUB_SYSTEM_ID

Bit Range	Default & Access	Field Name (ID): Description
31:0	100000001 000011000 000001000 00001b WO	**SUB_SYSTEM_ID:** Project: All

14.11.91 AUD_PWST1_DBG—Offset 62F04h

audion pwst1 debug

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F04h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000C0Fh

Bits 31:12	Bits 11:10	Bits 9:4	Bits 3:2	Bits 1:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1	0 0 0 0 0 0	1 1	1 1
RESERVED	FUNCTION_GROUP_DEVICE_POWER_STATE	RESERVED_1	CONVERTORA_WIDGET_POWER_STATE	PINB_WIDGET_POWER_STATE

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b WO	**RESERVED:** Project: All Format: MBZ
11:10	11b WO	**FUNCTION_GROUP_DEVICE_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)
9:4	0b WO	**RESERVED_1:** Project: All Format: MBZ
3:2	11b WO	**CONVERTORA_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was requested by audio software Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)
1:0	11b WO	**PINB_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

14.11.92 AUD_OUT_STR_DESC_A_DBG—Offset 62F08h

These values are returned from the device as the Stream Descriptor Format response to a Get Audio Output Converter Widget command.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F08h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000032h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Field
31:29	RESERVED
28:27	HBR_ENABLE
26:22	RESERVED_1
21:16	CONVERTOR_CHANNEL_COUNT
15	RESERVED_2
14	SAMPLE_BASE_RATE
13:11	SAMPLE_BASE_RATE_MULT
10:8	SAMPLE_BASE_RATE_DIVISOR
7	RESERVED_3
6:4	BITS_PER_SAMPLE
3:0	NUMBER_OF_CHANNELS_IN_A_STREAM

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b WO	**RESERVED:** Project: All Format: MBZ
28:27	0b WO	**HBR_ENABLE:** Project: All This reflects the current HBR settings
26:22	0b WO	**RESERVED_1:** Project: All Format: MBZ
21:16	0b WO	**CONVERTOR_CHANNEL_COUNT:** Project: All This reflects the Convertor Channel Count programmed through HDAudio.
15	0b WO	**RESERVED_2:** Project: All Format: MBZ
14	0b WO	**SAMPLE_BASE_RATE:** Project: All Default Value: 0b (48 KHz) Sampling base rate of audio stream Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All

Bit Range	Default & Access	Field Name (ID): Description
13:11	0b WO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: 000b (48 KHz) Audio stream sample base rate multiple Value Name Description Project 000b 1x 48 kHz/44.1 kHz or less All 001b 2x x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b 3x x3 (144 kHz) All 011b 4x x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved
10:8	0b WO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: 000b (indicates divide by 1 which results in 48 KHz) Audio stream sample base rate divisor Value Name Description Project 000b Divide by 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Divide by 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Divide by 3 Divide by 3 (16 kHz, 32 kHz) All 011b Divide by 4 Divide by 4 (11.025 kHz) All 100b Divide by 5 Divide by 5 (9.6 kHz) All 101b Divide by 6 Divide by 6 (8 kHz) All 110b Divide by 7 Divide by 7 All 111b Divide by Divide by 8 (6 kHz) All
7	0b WO	**RESERVED_3:** Project: All Format: MBZ
6:4	011b WO	**BITS_PER_SAMPLE:** Project: All Default Value: 011b (Indicates 24 bits) Audio stream sample base rate multiple Value Name Description Project 000b 8 bits The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 100b 20 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved
3:0	0010b WO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Format: U4+1 Default Value: 0010b (3 channels in each frame) Number of channels in each frame of the stream

14.11.93 AUD_OUT_DIG_CNVT_A_DBG—Offset 62F0Ch

These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F0Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h

31 … 28 … 24	20	16	15	12 … 8		4						0
0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0 0 0 0 0	0	0	0	0	0	0	0	1
RESERVED	STREAM_ID	LOWEST_CHANNEL_NUMBER	RESERVED_1	CATEGORY_CODE	LEVEL	PRO	NON_AUDIO	COPY	PRE	VCFG	V	DIGEN

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b WO	**RESERVED:** Project: All Format: MBZ
23:20	0b WO	**STREAM_ID:** Project: All Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
19:16	0b WO	**LOWEST_CHANNEL_NUMBER:** Project: All Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0b WO	**RESERVED_1:** Project: All Format: MBZ
14:8	0b WO	**CATEGORY_CODE:** Project: All S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0b WO	**LEVEL:** Project: All S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0b WO	**PRO:** Project: All This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use. Default (Consumer) All 1b Professional Professional use All
5	0b WO	**NON_AUDIO:** Project: All Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM (Default) All 1b Non-PCM Data is non PCM format All
4	0b WO	**COPY:** Project: All Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0b WO	**PRE:** Project: All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b None Pre-emphasis is non All 1b Enabled Filter pre-emphasis is enabled All

Bit Range	Default & Access	Field Name (ID): Description
2	0b WO	**VCFG:** Project: All Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	0b WO	**V:** Project: All Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	1b WO	**DIGEN:** All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Blocked Digital data is blocked from passing through the node, regardless of the state All 1b Passed Digital data can pass through the node (Default = 1, enabled) All

14.11.94 AUD_PWST2_DBG—Offset 62F14h

audio pwst2 debug

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F14h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits 31:4	Bits 3:2	Bits 1:0
RESERVED	CONVERTORB_WIDGET_POWER_STATE	PINC_WIDGET_POWER_STATE

Bit Range	Default & Access	Field Name (ID): Description
31:4	0b WO	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
3:2	11b WO	**CONVERTORB_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was requested by audio software Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)
1:0	11b WO	**PINC_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

14.11.95 AUD_OUT_STR_DESC_B_DBG—Offset 62F18h

HDAudio Verb: Converter Widget 2/72D These values are returned from the device as the Stream Descriptor Format response to a Get Audio Output Converter Widget command.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F18h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000032h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

RESERVED | HBR_ENABLE | RESERVED_1 | CONVERTOR_CHANNEL_COUNT | RESERVED_2 | SAMPLE_BASE_RATE | SAMPLE_BASE_RATE_MULT | SAMPLE_BASE_RATE_DIVISOR | RESERVED_3 | BITS_PER_SAMPLE | NUMBER_OF_CHANNELS_IN_A_STREAM

Bit Range	Default & Access	Field Name (ID): Description
31:29	0b WO	**RESERVED:** Project: All Format: MBZ
28:27	0b WO	**HBR_ENABLE:** Project: All This reflects the current HBR settings

Bit Range	Default & Access	Field Name (ID): Description
26:22	0b WO	**RESERVED_1:** Project: All Format: MBZ
21:16	0b WO	**CONVERTOR_CHANNEL_COUNT:** Project: All This reflects the Convertor Channel Count programmed through HDAudio.
15	0b WO	**RESERVED_2:** Project: All Format: MBZ
14	0b WO	**SAMPLE_BASE_RATE:** Project: All Default Value: 0b (48 KHz) Sampling base rate of audio stream Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0b WO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: 000b (48 KHz) Audio stream sample base rate multiple Value Name Description Project 000b 1x 48 kHz/44.1 kHz or less All 001b 2x x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b 3x x3 (144 kHz) All 011b 4x x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved
10:8	0b WO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: 000b (indicates divide by 1 which results in 48 KHz) Audio stream sample base rate divisor Value Name Description Project 000b Divide by 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Divide by 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Divide by 3 Divide by 3 (16 kHz, 32 kHz) All 011b Divide by 4 Divide by 4 (11.025 kHz) All 100b Divide by 5 Divide by 5 (9.6 kHz) All 101b Divide by 6 Divide by 6 (8 kHz) All 110b Divide by 7 Divide by 7 All 111b Divide by Divide by 8 (6 kHz) All
7	0b WO	**RESERVED_3:** Project: All Format: MBZ
6:4	011b WO	**BITS_PER_SAMPLE:** Project: All Default Value: 011b (Indicates 24 bits) Audio stream sample base rate multiple Value Name Description Project 000b 8 bits The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 100b 20 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved
3:0	0010b WO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Format: U4+1 Default Value: 0010b (3 channels in each frame) Number of channels in each frame of the stream

14.11.96 AUD_OUT_DIG_CNVT_B_DBG—Offset 62F1Ch

HDAudio Verb: Converter Widget 70D/70E/73E/73F/706 These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F1Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
RESERVED								STREAM_ID				LOWEST_CHANNEL_NUMBER				RESERVED_1	CATEGORY_CODE							LEVEL	PRO	NON_AUDIO	COPY	PRE	VCFG	V	DIGEN

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b WO	**RESERVED:** Project: All Format: MBZ
23:20	0b WO	**STREAM_ID:** Project: All Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
19:16	0b WO	**LOWEST_CHANNEL_NUMBER:** Project: All Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0b WO	**RESERVED_1:** Project: All Format: MBZ
14:8	0b WO	**CATEGORY_CODE:** Project: All S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0b WO	**LEVEL:** Project: All S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0b WO	**PRO:** Project: All This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use. Default (Consumer) All 1b Professional Professional use All
5	0b WO	**NON_AUDIO:** Project: All Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM (Default) All 1b Non-PCM Data is non PCM format All

Bit Range	Default & Access	Field Name (ID): Description
4	0b WO	**COPY:** Project: All Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0b WO	**PRE:** Project: All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b None Pre-emphasis is non All 1b Enabled Filter pre-emphasis is enabled All
2	0b WO	**VCFG:** Project: All Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	0b WO	**V:** Project: All Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	1b WO	**DIGEN:** All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Blocked Digital data is blocked from passing through the node, regardless of the state All 1b Passed Digital data can pass through the node (Default = 1, enabled) All

14.11.97 AUD_PORT_EN_B_DBG—Offset 62F20h

HDAudio Verb: PinWidget 707/3/734/701 These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F20h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

TAG_7_3	INDEX_2_0	CONNECTION_SELECT_CONTROL_B	CONVERTER_CHANNEL_MAP_PORT_B	HDMI_INDEX_PORT_B	RESERVED	MLP_STREAM	PORT_B_AMP_MUTE_STATUS	PORT_B_OUT_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0b WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0b WO	**CONNECTION_SELECT_CONTROL_B:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0b WO	**CONVERTER_CHANNEL_MAP_PORT_B:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0b WO	**HDMI_INDEX_PORT_B:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0b WO	**RESERVED:** Project: All Format: MBZ
4:2	0b WO	**MLP_STREAM:** Project: All Default Value: 000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All
1	1b WO	**PORT_B_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
0	1b WO	**PORT_B_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

14.11.98 AUD_PWST3_DBG—Offset 62F24h

HDAudio Verb: Pin Widget 705

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F24h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

RESERVED (bits 31:2) | PIND_WIDGET_POWER_STATE (bits 1:0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b WO	**RESERVED:** Project: All Format: MBZ
1:0	11b WO	**PIND_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

14.11.99 AUD_PORT_EN_C_DBG—Offset 62F28h

HDAudio Verb: PinWidget 707/3/734/701 These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F28h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
TAG_7_3					INDEX_2_0			CONNECTION_SELECT_CONTROL_C								CONVERTER_CHANNEL_MAP_PORT_C				HDMI_INDEX_PORT_C				RESERVED			MLP_STREAM			PORT_C_AMP_MUTE_STATUS	PORT_C_OUT_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0b WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0b WO	**CONNECTION_SELECT_CONTROL_C:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0b WO	**CONVERTER_CHANNEL_MAP_PORT_C:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0b WO	**HDMI_INDEX_PORT_C:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0b WO	**RESERVED:** Project: All Format: MBZ
4:2	0b WO	**MLP_STREAM:** Project: All Default Value: 000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All
1	1b WO	**PORT_C_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
0	1b WO	**PORT_C_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

14.11.100 AUD_PORT_EN_D_DBG—Offset 62F2Ch

HDAudio Verb: PinWidget 707/3/734/701 These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F2Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

TAG_7_3	INDEX_2_0	CONNECTION_SELECT_CONTROL_D	CONVERTER_CHANNEL_MAP_PORT_D	HDMI_INDEX_PORT_D	RESERVED	MLP_STREAM	PORT_D_AMP_MUTE_STATUS	PORT_D_OUT_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0b WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0b WO	**CONNECTION_SELECT_CONTROL_D:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0b WO	**CONVERTER_CHANNEL_MAP_PORT_D:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0b WO	**HDMI_INDEX_PORT_D:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0b WO	**RESERVED:** Project: All Format: MBZ
4:2	0b WO	**MLP_STREAM:** Project: All Default Value: 000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All

Bit Range	Default & Access	Field Name (ID): Description
1	1b WO	**PORT_D_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
0	1b WO	**PORT_D_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

14.11.101 AUD_CHICKENBIT_REG—Offset 62F38h

audio chickenbit register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F38h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000001h

Bits	31:2	1	0
Default	0000 0000 0000 0000 0000 0000 0000 00	0	1
Field	RESERVED	PLACE_HOLDER_FOR_ECC_CHICKEN_BIT_PIPE_A	ENABLE_MMIO_HDMI_AUDIO_VERB_PROGRAMMING

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b WO	**RESERVED:** Project: All Format: MBZ
1	0b WO	**PLACE_HOLDER_FOR_ECC_CHICKEN_BIT_PIPE_A:** Project: All audr_ecc_flip_chicken_bit

Bit Range	Default & Access	Field Name (ID): Description
0	1b WO	**ENABLE_MMIO_HDMI_AUDIO_VERB_PROGRAMMING:** All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b HDAudio Programming through HDAudio Azalia All 1b MMIO Programming through MMIO Debug registers All

14.11.102 AUD_OUT_DIG_CNVTA_DBG—Offset 62F40h

HDAudio Verb: Converter Widget 70E/73E These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F40h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED | IEC_CODING_TYPE | RSVD_FOR_DIGITAL__CONVERTER_2A

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b WO	**RESERVED:** Project: All Format: MBZ
11:8	0b WO	**IEC_CODING_TYPE:** Project: All
7:0	0b WO	**RSVD_FOR_DIGITAL__CONVERTER_2A:** Project: All

14.11.103 AUD_OUT_DIG_CNVTB_DBG—Offset 62F44h

HDAudio Verb: Converter Widget 70E/73E These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

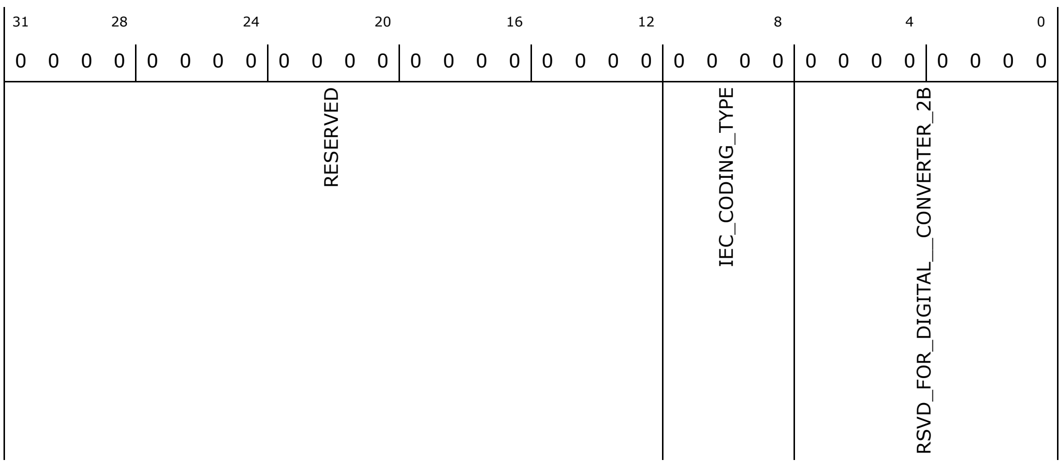
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F44h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0b WO	**RESERVED:** Project: All Format: MBZ
11:8	0b WO	**IEC_CODING_TYPE:** Project: All
7:0	0b WO	**RSVD_FOR_DIGITAL__CONVERTER_2B:** Project: All

14.11.104 AUD_CNTL_ST_B_DBG—Offset 62F60h

HDAudio Verb: Pin Widget 730/732

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F60h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																						INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME		INFOFRAME_PACKET_INDEX			BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS				

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b WO	**RESERVED:** Project: All Format: MBZ
9:8	0b WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: 00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0b WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: 00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0b WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

14.11.105 AUD_HDMIW_INFOFR_B_DBG—Offset 62F64h

HDAudio Verb: Pin Widget 731

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F64h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																								DATA_ISLAND_PACKET_DATA							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b WO	**RESERVED:** Project: All Format: MBZ
7:0	0b WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

14.11.106 AUD_CNTL_ST_C_DBG—Offset 62F70h

HDAudio Verb: Pin Widget 730/732

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F70h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME | INFOFRAME_PACKET_INDEX | BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b WO	**RESERVED:** Project: All Format: MBZ
9:8	0b WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: 00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0b WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: 00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0b WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

14.11.107 AUD_HDMIW_INFOFR_C_DBG—Offset 62F74h

HDAudio Verb: Pin Widget 731

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F74h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																								DATA_ISLAND_PACKET_DATA							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b WO	**RESERVED:** Project: All Format: MBZ
7:0	0b WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

14.11.108 AUD_CNTL_ST_D_DBG—Offset 62F80h

HDAudio Verb: Pin Widget 730/732

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F80h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:10	9:8	7:5	4:0
Field	RESERVED	INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME	INFOFRAME_PACKET_INDEX	BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0	0 0 0 0 0

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b WO	**RESERVED:** Project: All Format: MBZ
9:8	0b WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: 00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0b WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: 00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0b WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

14.11.109 AUD_HDMIW_INFOFR_D_DBG—Offset 62F84h

HDAudio Verb: Pin Widget 731

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F84h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:8) | DATA_ISLAND_PACKET_DATA (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b WO	**RESERVED:** Project: All Format: MBZ
7:0	0b WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

14.11.110 AUD_CONFIG_DEFAULT2_REG_PORTB—Offset 62F88h

HDAudio Verb: Pin Widget 738..73B

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F88h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_BACK (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b WO	**READ_BACK:** Project: All Config Default 2 values of port B rgars being written using the 738/739/73A/73B

14.11.111 AUD_CONFIG_DEFAULT2_REG_PORTC—Offset 62F8Ch

HDAudio Verb: Pin Widget 738..73B

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F8Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_BACK

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b WO	**READ_BACK:** Project: All Config Default 2 values of port C rgars being written using the 738/739/73A/73B

14.11.112 AUD_CONFIG_DEFAULT2_REG_PORTD—Offset 62F90h

HDAudio Verb: Pin Widget 738..73B

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F90h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_BACK

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b WO	**READ_BACK:** Project: All Config Default 2 values of port D rgars being written using the 738/739/73A/73B

14.11.113 AUD_MCTSA—Offset 62F94h

Audio M or CTS Pipe A Values Readback Register

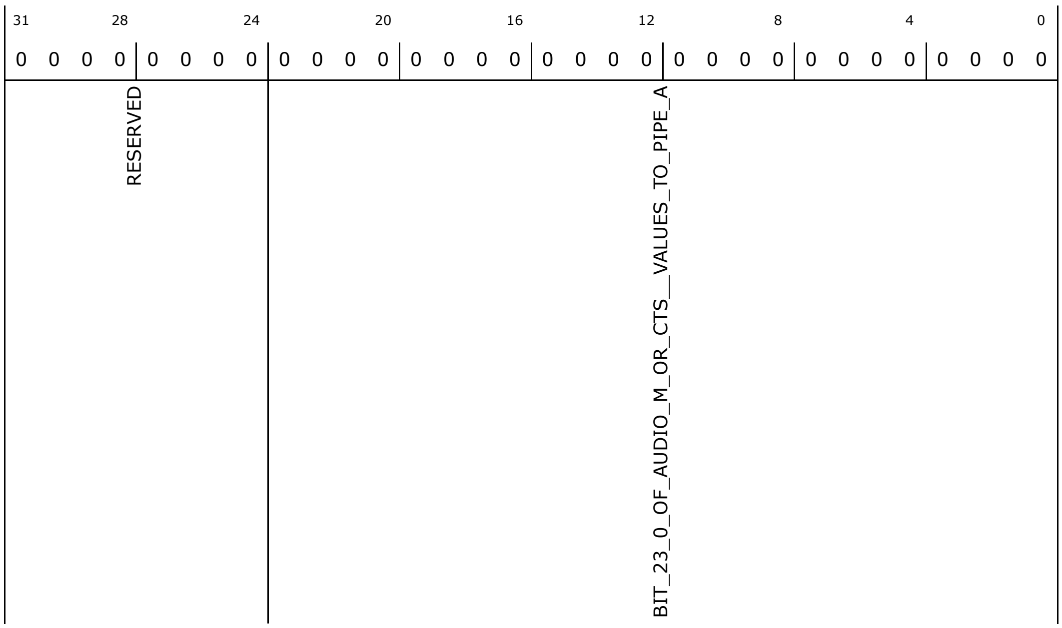
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F94h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format: MBZ
23:0	0b RO	**BIT_23_0_OF_AUDIO_M_OR_CTS__VALUES_TO_PIPE_A:** Project: All

14.11.114 AUD_MCTSB—Offset 62F98h

Audio M or CTS Pipe B Values Readback Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 62F98h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED

BIT_23_0_OF_AUDIO_M_OR_CTS__VALUES_TO_PIPE_B

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Project: All Format: MBZ
23:0	0b RO	**BIT_23_0_OF_AUDIO_M_OR_CTS__VALUES_TO_PIPE_B:** Project: All

14.11.115 DP_B—Offset 64100h

DisplayPort B Control Register [DevCTG, DevCDV] Display Port B control (dprrega_b0.vql_displayb1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64100h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000018h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
DISPLAYPORT_B_ENABLE	PIPE_SELECT	LINK_TRAINING_PATTERN_ENABLE		RESERVED			RESERVED_1			PORT_WIDTH_SELECTION			ENHANCED_FRAMING_ENABLE	RESERVED_2		RESERVED_3	RESERVED_4						ASR_ENABLE	SCRAMBLING_DISABLE	AUDIO_OUTPUT_ENABLE	HDCP_PORT_SELECT	SYNC_POLARITY		DIGITAL_DISPLAY_B_DETECTED	RESERVED_5	DISABLE_FRAMESTART_STALL

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DISPLAYPORT_B_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. 1 = Enable. This bit enables the Display Port B interface. 0 = Disable and tristates the Display Port B interface.
30	0b RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29:28	0b RW	**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled: Repetition of D10.2 characters Default. 01 Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times 11 Link not in training: Send normal pixels
27:25	0b RW	**RESERVED:** [DevCDV]: Voltage swing level set: [DevCTG]: These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration (At CDV moved to register at the DPIO) 000 0.4V (DEFAULT) 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED
24:22	0b RW	**RESERVED_1:** [DevCDV]: Pre-emphasis level set [DevCTG]: These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. At CDV this field move to register in the DPIO. 000 no pre-emphasis (default) 001 3.5dB pre-emphasis (1.5x) 010 6dB pre-emphasis (2x) 011 9.5dB pre-emphasis (3x) RESERVED 1xx RESERVED

Bit Range	Default & Access	Field Name (ID): Description
21:19	0b RW	**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED
18	0b RW	**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 (Default) Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re-enabled
17:16	0b RW	**RESERVED_2:** MBZ
15	0b RW	**RESERVED_3:** [DevCDV]: Port reversal [DevCTG]: Locked once port is enabled. Updates when the port is disabled then re-enabled
14:9	0b RW	**RESERVED_4:** MBZ
8	0b RW	**ASR_ENABLE:** [DevVLV2]: this bit enables the Alternate Scrammbler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 ASR disable
7	0b RW	**SCRAMBLING_DISABLE:** [DevCTG, B-step only, DevCDV]: This bit disables scrambling for this port. 0 = Scrambling enabled (Default) 1 = Scrambling disabled, no SR after initialization at loop 2 of training
6	0b RW	**AUDIO_OUTPUT_ENABLE:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to Normal 0 = Audio output disabled 1 = Audio output enabled
5	0b RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	11b RW	**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0b RO	**DIGITAL_DISPLAY_B_DETECTED:** Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 (port B) data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read Only
1	0b RW	**RESERVED_5:** MBZ
0	0b RW	**DISABLE_FRAMESTART_STALL:** This bit, when set, will disable the framestart window to stall DP AV mixer from sending audio samples before framestart. This applies to BOTH pipes. 0 = Enable framestart window to stall audio samples. (default) 1 = Disable framestart window to stall audio samples.

14.11.116 DPB_AUX_CH_CTL—Offset 64110h

Display Port B AUX Channel Control [DevCDV] AuxB control (dprrega_b0.v auxb_ctl_rdback)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64110h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00050000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SEND_BUSY, DONE, INTERRUPT_ON_DONE, TIME_OUT_ERROR, TIME_OUT_TIMER_VALUE, RECEIVE_ERROR, MESSAGE_SIZE, PRECHARGE_TIME, AUX_AKSV_BUFFER_SELECT, INVERT_MANCHESTER_TEST_MODE, SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE, DISABLE_DE_GLITCH_TEST_MODE, DOUBLE_PRECHARGE_TEST_MODE, _2X_BIT_CLOCK_DIVIDER

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SEND_BUSY:** Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	0b RW/1C	**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	0b RW	**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	0b RW/1C	**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
27:26	0b RW	**TIME_OUT_TIMER_VALUE:** 00: 400us (default) 01: 600us 10: 800us 11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	0b RW/1C	**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
24:20	0b RW	**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or)20 are not allowed.
19:16	0101b RW	**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	0b RW	**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the Aksv buffer for HDCP authentication, or all from the AUX Data registers. Set this bit before initiating a transaction to write Aksv to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header, then the DP_AUX_CH_AKSV_HI, then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the Aksv buffer simultaneously. 0 (Default) Use AUX Data registers for regular data transmission 1 Use Aksv Buffer for part of the data transmission.
14	0b RW	**INVERT_MANCHESTER_TEST_MODE:** 1 = Manchester code rising edge mid-clk signifies one (test mode) 0 = Manchester code rising edge mid-clk signifies zero (default)
13	0b RW	**SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE:** 1 = Only recover clock during sync pattern (test mode) 0 = Recover clock during sync pattern and data phase (default)
12	0b RW	**DISABLE_DE_GLITCH_TEST_MODE:** 1 = Disable serial input de-glitch logic (test mode) 0 = Enable serial input de-glitch logic (default)
11	0b RW	**DOUBLE_PRECHARGE_TEST_MODE:** 1 = Precharge time is doubled 0 = Precharge time is as programmed
10:0	0b RW	**_2X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). [DevCTG-A] the input clock is cdclk. [DevCTG-B, DevCDV] the input clock is hrawclk (200MHz) Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

14.11.117 DPB_AUX_CH_DATA1—Offset 64114h

Display Port B AUX Data Register 1 [DevCTG, DevCDV]

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64114h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AUX_CH_DATA1_31

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA1_31:** 0]: The first Dword of the message. The Msbyte is transmitted first. Reads will give the response data after transaction complete.

14.11.118 DPB_AUX_CH_DATA2—Offset 64118h

Display Port B AUX Data Register 2 [DevCTG, DevCDV] AuxB Data2 (dprrega_b0.v auxb_dpr_data2, ql_auxb_d2)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64118h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AUX_CH_DATA2_31

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA2_31:** 0]: The second Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

14.11.119 DPB_AUX_CH_DATA3—Offset 6411Ch

Display Port B AUX Data Register 3 [DevCTG, DevCDV] AuxB Data3 (dprrega_b0.v auxb_dpr_data3, ql_auxb_d3)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6411Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AUX_CH_DATA3_31

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA3_31:** 0]: The third Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

14.11.120 DPB_AUX_CH_DATA4—Offset 64120h

Display Port B AUX Data Register 4 [DevCTG, DevCDV] AuxB Data4 (dprrega_b0.v auxb_dpr_data4, ql_auxb_d4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64120h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AUX_CH_DATA4_31

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA4_31:** 0]: The fourth Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

14.11.121 DPB_AUX_CH_DATA5—Offset 64124h

Display Port B AUX Data Register 5 [DevCTG, DevCDV] AuxB Data5 (dprrega_b0.v auxb_dpr_data5, ql_auxb_d5)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64124h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AUX_CH_DATA5_31

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA5_31:** 0]: The fifth Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

14.11.122 DP_AUX_CH_AKSV_HI—Offset 64130h

Display Port AUX Aksv Buffer High [DevCTG-B, DevCDV] AuxB AKSV High (dprrega_b0.v dpr_aux_aksv_hi)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64130h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AKSV_BITS_7								AKSV_BITS_15								AKSV_BITS_23								AKSV_BITS_31							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b WO	**AKSV_BITS_7:** 0]
23:16	0b WO	**AKSV_BITS_15:** 8]
15:8	0b WO	**AKSV_BITS_23:** 16]
7:0	0b WO	**AKSV_BITS_31:** 24]

14.11.123 DP_AUX_CH_AKSV_LO—Offset 64134h

Display Port AUX Aksv Buffer Low [DevCTG-B, DevCDV] AuxB AKSV High (dprrega_b0.v dpr_aux_aksv_lo)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64134h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																								AKSV_BITS_39							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b WO	**RESERVED:** MBZ
7:0	0b WO	**AKSV_BITS_39:** 32]

14.11.124 DPB_AUX_TST—Offset 64150h

Display Port B AUX Test Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64150h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DPB_AUX_BUFFER_LOOPBACK_TEST_ENABLE
DPB_AUX_BUFFER_LOOPBACK_TEST_DONE
DPB_AUX_BUFFER_LOOPBACK_TEST_RESULT
DPB_AUX_FULL_TEST_ENABLE
RESERVED
DPB_AUX_SHORT_SYNC
DPB_AUX_CONSTANT_0S_TEST_PATTERN
DPB_AUX_TIGHTEN_FREQUENCY_WINDOW
DPB_AUX_LESS_GOOD_SYNC_0S_REQUIRED
DEGLITCH_AMOUNT
RESERVED_1
DPB_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE
DPB_AUX_DEBUG_STATUS_READBACK
RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DPB_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** Project: All Default Value: 0b Enables test for the DPB-AUX I/O buffer. A 16 cycle clock pattern is output to the I/O buffer and compared against the looped back buffer output. The input clock is cdclk. With input clock at 512MHz the pattern will bea 1 MHz clock. It scales down with lower clock frequencies. The result is found in DP-AUX Buffer Loopback Test Result after DP-AUX Buffer Loopback Test Done is set. Clear this bit to 0 after test is done to return DP-AUX to normal operation. Loopback Test can be run simultaneously on all AUX buffers. Do not enable DP-AUX Buffer Loopback Test and DP-AUX Full Test simultaneously. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test. All
30	0b RO	**DPB_AUX_BUFFER_LOOPBACK_TEST_DONE:** Project: All Default Value: 0b AccessType: Read Only DPB-AUX Buffer Loopback Test has been run and completed. This is not the done for the DP-AUX Full Test. Value Name Description Project 0b Not Done Test not done. DP-AUX Buffer Loopback Test Result is not valid All 1b Done Test done. DP-AUX Buffer Loopback Test Result is now valid All

Bit Range	Default & Access	Field Name (ID): Description
29	0b RO	**DPB_AUX_BUFFER_LOOPBACK_TEST_RESULT:** Project: All Default Value: 0b AccessType: Read Only Result of the DPB-AUX Buffer Loopback Test. Value is only valid after a DP-AUX Loopback Test Done is 1. This is not the result of the DP-AUX Full Test. Value Name Description Project 0b Pass Pass All 1b Fail All
28	0b RW	**DPB_AUX_FULL_TEST_ENABLE:** Project: All Default Value: 0b Enables test for the DPB-AUX core logic transmit and receive functions through the DPB-AUX and DPC-AUX buffers. DPB-AUX and DPC-AUX are interconnected through I/O buffer loopbacks. DPB-AUX is programmed as source to output a 20 byte test pattern. DPC-AUX is programmed as sink to receive the test pattern and reply with a different 20 byte test pattern. Test pattern 1 = 0xA55CC33E E770080C 0E0F0F8F CFEFF81C 3E77E3C8 Test pattern 2 = 0X183C7EE7 C381FF7F 3F1F0F07 030100EE 77CC33A5 Programming sequence: 1. Set DPB-AUX Full Test Enable to 1. 2. Program DPB_AUX_CH_DATA[1-5] with test pattern 1 to transmit as the source. 3. Program DPC_AUX_CH_DATA[1-5] with test pattern 2 to reply with as the sink. 4. Program all DPC_AUX_CH_CTL fields and set Send to 1. 5. Program all DPB_AUX_CH_CTL fields and set Send to 1. Then the test will start. Results checking sequence: 1. Poll DPB_AUX_CH_CTL for Done. To pass, Done must be set within 500us. 2. Read DPB_AUX_CH_CTL register. To pass, Timeout Error and Receive Error must be 0. 3. Read DPC_AUX_CH_CTL register. To pass, Receive Error must be 0. 4. Read DPB_AUX_CH_DATA[1-5] registers. To pass, they must contain test pattern 2. 5. Read DPC_AUX_CH_DATA[1-5] registers. To pass, they must contain test pattern 1. Clear this bit to 0 after test is done to return DP-AUX to normal operation. Test must be repeated with and without lane reversal to verify DPB-AUX buffer combinations. Only enable one DP-AUX Full Test at a time. To abort a test in progress, write the AUX_CH_CTL Send bits to 0 and Full Test Enable to 0. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test All
27:16	0b RW	**RESERVED:** Project: All Format:
15	0b RW	**DPB_AUX_SHORT_SYNC:** Project: All Output just 16 manchester 0s for sync (otherwise 26)
14	0b RW	**DPB_AUX_CONSTANT_0S_TEST_PATTERN:** Project: All Output neverending Manchester encoded 0s for electrical testing
13	0b RW	**DPB_AUX_TIGHTEN_FREQUENCY_WINDOW:** Project: All Tighten the window of allowable receive frequencies
12	0b RW	**DPB_AUX_LESS_GOOD_SYNC_0S_REQUIRED:** Project: All Check for only 8 good sync 0s instead of 12 when receiving
11:10	0b RW	**DEGLITCH_AMOUNT:** Project: All Default Value: 0b Select clock count for deglitch Value Name Description Project 00b 50 ns 25 clocks - GMBUS type - 50ns at 500MHz cdclk All 01b 125 ns 1/4 2X bit clock divider value - 125ns All 10b 62.5 ns 1/8 2X bit clock divider value - 62.5ns All 11b 31.125 ns 1/16 2X bit clock divider value - 31.125ns All
9	0b RW	**RESERVED_1:** Project: All Format:
8	0b RW	**DPB_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE:** Project: All Default Value: 0b Value Name Description Project 0b Okay Multiple edges in window is okay All 1b Error Multiple edges in window is an error All

Bit Range	Default & Access	Field Name (ID): Description
7:6	0b RW	**DPB_AUX_DEBUG_STATUS_READBACK:** Readback of bit clock divide field gives the error type io_aux_data_syncro and aux_io_data and sm_noa[3:0] and clkregen_baddatastop and mdec_toomuchdata and mdec_notbytealign and mdec_multiedgeinwin and Input data Output data Control state machine Error - bad STOP at end of data Error - too much data Error - data not byte aligned Error - multiple edges inside of window Error - multiple edges outside of window All
5:0	0b RW	**RESERVED_2:** Project: All Format:

14.11.125 DP_C—Offset 64200h

Display Port C Control Register [DevCTG, DevCDV,DevVLV] Display Port C control (dprrega_b0.v ql_displayc1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000018h

Bits (31 … 0)	Value	Field
31	0	DISPLAYPORT_C_ENABLE
30	0	PIPE_SELECT
29:28	0 0	LINK_TRAINING_PATTERN_ENABLE
27:25	0 0 0	RESERVED
24:22	0 0 0	RESERVED_1
21:19	0 0 0	PORT_WIDTH_SELECTION
18	0	ENHANCED_FRAMING_ENABLE
17:16	0 0	RESERVED_2
15	0	RESERVED_3
14:9	0 0 0 0 0 0	RESERVED_4
8	0	ASR_ENABLE
7	0	SCRAMBLING_DISABLE
6	0	AUDIO_OUTPUT_ENABLE
5	0	HDCP_PORT_SELECT
4:3	1 1	SYNC_POLARITY
2	0	DIGITAL_DISPLAY_C_DETECTED
1:0	0 0	RESERVED_5

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DISPLAYPORT_C_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. 1 = Enable. This bit enables the Display Port C interface. 0 = Disable and tristates the Display Port C interface.
30	0b RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B

Bit Range	Default & Access	Field Name (ID): Description
29:28	0b RW	**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled: Repetition of D10.2 characters Default. 01 Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times 11 Link not in training: Send normal pixels
27:25	0b RW	**RESERVED:** [DevCDV]: Voltage swing level set [DevCTG]: These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 0.4V (DEFAULT) 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED
24:22	0b RW	**RESERVED_1:** [DevCDV]: Pre-emphasis level set [DevCTG]: These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 no pre-emphasis (default) 001 3.5dB pre-emphasis (1.5x) 010 6dB pre-emphasis (2x) 011 9.5dB pre-emphasis (3x) RESERVED 1xx RESERVED
21:19	0b RW	**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED
18	0b RW	**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 (Default) Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re-enabled
17:16	0b RW	**RESERVED_2:** MBZ
15	0b RW	**RESERVED_3:** [DevCDV]: Port reversal [DevCTG]: Locked once port is enabled. Updates when the port is disabled then re-enabled
14:9	0b RW	**RESERVED_4:** MBZ
8	0b RW	**ASR_ENABLE:** [DevVLV2]: this bit enables the Alternate Scrammbler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 ASR disable
7	0b RW	**SCRAMBLING_DISABLE:** [DevCTG, B-step only, DevCDV]: This bit disables scrambling for this port. 0 = Scrambling enabled (Default) 1 = Scrambling disabled, no SR after initialization at loop 2 of training
6	0b RW	**AUDIO_OUTPUT_ENABLE:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to Normal 0 = Audio output disabled 1 = Audio output enabled

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	11b RW	**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. Please note that in native VGA modes, these bits have no effect. In native VGA modes, sync polarity is determined by VRshr3c2d76b[7:6], the VGA polarity bits in VGA control. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0b RO	**DIGITAL_DISPLAY_C_DETECTED:** Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port (sDVO B/C) data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read only
1:0	0b RW	**RESERVED_5:** MBZ

14.11.126 DPC_AUX_CH_CTL—Offset 64210h

Display Port C AUX Channel Control [DevCTG] AuxC Data1 (dprrega_b0.v auxc_dpr_data1, ql_auxc_d1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64210h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00050000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields (bit 31 → 0)
SEND_BUSY
DONE
INTERRUPT_ON_DONE
TIME_OUT_ERROR
TIME_OUT_TIMER_VALUE
RECEIVE_ERROR
MESSAGE_SIZE
PRECHARGE_TIME
AUX_AKSV_BUFFER_SELECT
INVERT_MANCHESTER_TEST_MODE
SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE
DISABLE_DE_GLITCH_TEST_MODE
DOUBLE_PRECHARGE_TEST_MODE
_2X_BIT_CLOCK_DIVIDER

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SEND_BUSY:** Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	0b RW/1C	**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	0b RW	**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	0b RW/1C	**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
27:26	0b RW	**TIME_OUT_TIMER_VALUE:** 00: 400us (default) 01: 600us 10: 800us 11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	0b RW/1C	**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
24:20	0b RW	**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or)20 are not allowed.
19:16	0101b RW	**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	0b RW	**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the Aksv buffer for HDCP authentication, or all from the AUX Data registers. Set this bit before initiating a transaction to write Aksv to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header, then the DP_AUX_CH_AKSV_HI, then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the Aksv buffer simultaneously. 0 (Default) Use AUX Data registers for regular data transmission 1 Use Aksv Buffer for part of the data transmission.
14	0b RW	**INVERT_MANCHESTER_TEST_MODE:** 1 = Manchester code rising edge mid-clk signifies one (test mode) 0 = Manchester code rising edge mid-clk signifies zero (default)
13	0b RW	**SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE:** 1 = Only recover clock during sync pattern (test mode) 0 = Recover clock during sync pattern and data phase (default)
12	0b RW	**DISABLE_DE_GLITCH_TEST_MODE:** 1 = Disable serial input de-glitch logic (test mode) 0 = Enable serial input de-glitch logic (default)
11	0b RW	**DOUBLE_PRECHARGE_TEST_MODE:** 1 = Precharge time is doubled 0 = Precharge time is as programmed

Bit Range	Default & Access	Field Name (ID): Description
10:0	0b RW	**_2X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). [DevCTG-A] the input clock is cdclk. [DevCTG-B] the input clock is hrawclk. Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

14.11.127 DPC_AUX_CH_DATA1—Offset 64214h

Display Port C AUX Data Register 1 [DevCTG, DevCDV] AuxC Data1 (dprrega_b0.v auxc_dpr_data1, ql_auxc_d1)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64214h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AUX_CH_DATA1_31

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA1_31:** 0]: The first DWord of the message. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

14.11.128 DPC_AUX_CH_DATA2—Offset 64218h

Display Port C AUX Data Register 2 [DevCTG, DevCDV] AuxC Data2 (dprrega_b0.v auxc_dpr_data2, ql_auxc_d2)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64218h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AUX_CH_DATA2_31																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA2_31:** 0]: The second DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

14.11.129 DPC_AUX_CH_DATA3—Offset 6421Ch

Display Port C AUX Data Register 3 [DevCTG, DevCDV] AuxC Data3 (dprrega_b0.v auxc_dpr_data3, ql_auxc_d3)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6421Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AUX_CH_DATA3_31																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA3_31:** 0]: The third DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

14.11.130 DPC_AUX_CH_DATA4—Offset 64220h

Display Port C AUX Data Register 4 [DevCTG, DevCDV] AuxC Data4 (dprrega_b0.v auxc_dpr_data4, ql_auxc_d4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64220h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AUX_CH_DATA4_31

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA4_31:** 0]: The fourth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

14.11.131 DPC_AUX_CH_DATA5—Offset 64224h

Display Port C AUX Data Register 5 [DevCTG, DevCDV] AuxC Data5 (dprrega_b0.v auxc_dpr_data5, ql_auxc_d5)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64224h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AUX_CH_DATA5_31

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**AUX_CH_DATA5_31:** 0]: The fifth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

14.11.132 DPC_AUX_TST—Offset 64228h

Display Port C AUX Test Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 64228h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	DPC_AUX_BUFFER_LOOPBACK_TEST_ENABLE
30	0	DPC_AUX_BUFFER_LOOPBACK_TEST_DONE
29	0	DPC_AUX_BUFFER_LOOPBACK_TEST_RESULT
28	0	DPC_AUX_FULL_TEST_ENABLE
27:16	0000 0000 0000	RESERVED
15	0	DPC_AUX_SHORT_SYNC
14	0	DPC_AUX_CONSTANT_0S_TEST_PATTERN
13	0	DPC_AUX_TIGHTEN_FREQUENCY_WINDOW
12	0	DPC_AUX_LESS_GOOD_SYNC_0S_REQUIRED
11:10	00	DPC_AUX_DEGLITCH_AMOUNT
9	0	RESERVED_1
8	0	DPC_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE
7:6	00	DPC_AUX_DEBUG_STATUS_READBACK
5:0	000000	RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DPC_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** Project: All Default Value: 0b See DPB description. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test. All
30	0b RO	**DPC_AUX_BUFFER_LOOPBACK_TEST_DONE:** Project: All Default Value: 0b AccessType: Read Only See DPB description. Value Name Description Project 0b Not Done Test not done. DP-AUX Buffer Loopback Test Result is not valid All 1b Done Test done. DP-AUX Buffer Loopback Test Result is now valid All

Bit Range	Default & Access	Field Name (ID): Description
29	0b RO	**DPC_AUX_BUFFER_LOOPBACK_TEST_RESULT:** Project: All Default Value: 0b AccessType: Read Only See description for DPB-AUX Buffer Loopback Test Result Value Name Description Project 0b Pass Pass All 1b Fail Fail All
28	0b RW	**DPC_AUX_FULL_TEST_ENABLE:** Project: All Default Value: 0b See DPB description. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test All
27:16	0b RW	**RESERVED:** Project: All Format:
15	0b RW	**DPC_AUX_SHORT_SYNC:** Project: All See DPB description.
14	0b RW	**DPC_AUX_CONSTANT_0S_TEST_PATTERN:** Project: All See DPB description.
13	0b RW	**DPC_AUX_TIGHTEN_FREQUENCY_WINDOW:** Project: All See DPB description.
12	0b RW	**DPC_AUX_LESS_GOOD_SYNC_0S_REQUIRED:** Project: All See DPB description.
11:10	0b RW	**DPC_AUX_DEGLITCH_AMOUNT:** Project: All Default Value: 0b See DPB description. Value Name Description Project 00b 50 ns 25 clocks - GMBUS type - 50ns at 500MHz cdclk All 01b 125 ns 1/4 2X bit clock divider value - 125ns All 10b 62.5 ns 1/8 2X bit clock divider value - 62.5ns All 11b 31.125 ns 1/16 2X bit clock divider value - 31.125ns All
9	0b RW	**RESERVED_1:** Project: All Format:
8	0b RW	**DPC_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE:** Project: All Default Value: 0b Value Name Description Project 0b Okay Multiple edges in window is okay All 1b Error Multiple edges in window is an error All
7:6	0b RW	**DPC_AUX_DEBUG_STATUS_READBACK:** Project: All Default Value: 0b Value Name Description Project 00b Program Readback of bit clock divide field gives the programmed clock frequency All 01b Recover Readback of bit clock divide field gives the recovered clock frequency All 10b Error Type Readback of bit clock divide field gives the error type All
5:0	0b RW	**RESERVED_2:** Project: All Format:

14.11.133 STREAM_A_LPE_AUD_CONFIG—Offset 65000h

LPE Audio Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000280h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
RESERVED															LPE_STREAM_A_PAUSE_RESUME	LPE_HDMI_DP_MODE_ON_STREAM_A	BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL	LEFT_ALIGNMENT	_16_BIT_CONTAINER	UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE	USER_BIT_U	VALIDITY_BIT_V	SAMPLE_FLAT_BIT	SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS	NUM_AUDIO_CHANNELS			FORMAT		LAYOUT	AUDIO_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:17	0b RW	**RESERVED:** Reserved.
16	0b RW	**LPE_STREAM_A_PAUSE_RESUME:** DMA pause fetching at the boundary of buffers when this bit is set, and resume fetching when this bit is cleared. 1- DMA stop requesting more audio sample from buffer A,B,C,D after reading and depleting all data from current buffer 0- DMA resume requesting data from the next available buffer (A,B,C,D). Programming note: this bit should not be used by SW driver. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically
15	0b RW	**LPE_HDMI_DP_MODE_ON_STREAM_A:** 1 = DP mode 0 = HDMI mode (default)
14	0b RW	**BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL:** When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	0b RW	**LEFT_ALIGNMENT:** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container.1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)

Bit Range	Default & Access	Field Name (ID): Description
12	0b RW	**_16_BIT_CONTAINER:** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default)1= 16-bit container 0= 32-bit container
11	0b RW	**UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE:** Set this bit will enble HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Timesstamp packet) are sent to keep sink in sync even no audio sound will heard.1= send underrun packets (silent stream) 0= send null packets (default) Programming note: SW driver shall always set silent stream bit. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
10	0b RW	**USER_BIT_U:** HW will clear this bit ineach sub-frames it sends, But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	1b RW	**VALIDITY_BIT_V:** HW will set this bit in both each sub-frames it sends. But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= Set V bit in sub-frame (default) 0= clear V bit in sub-frame. For debug or testing
8	0b RW	**SAMPLE_FLAT_BIT:** When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	1b RW	**SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS:** Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)
6:4	0b RW	**NUM_AUDIO_CHANNELS:** 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels 110: 8 channels Note: When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because SW ensures that an even number of samples are packed in the audio buffers. Programming note: Bit 6 of of this field is a write only bit. When reads back, it always returns zero. Ensure to write bit 6 to 1?b1 when programming for 6/7/8 audio channels.
3:2	0b RW	**FORMAT:** 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	0b RW	**LAYOUT:** 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) Note: Layout bit doesn t matter for HBR
0	0b RW	**AUDIO_ENABLE:** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted and CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

14.11.134 STREAM_A_LPE_AUD_CH_STATUS_0—Offset 65008h

Audio Channel Status Attributes 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CHANNEL_STATUS_REGISTER_0

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**CHANNEL_STATUS_REGISTER_0:** . These bits are transmitted as attributes of audio packets

14.11.135 STREAM_A_LPE_AUD_CH_STATUS_1—Offset 6500Ch

Audio Channel Status Attributes 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6500Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED | CHANNEL_STATUS_REGISTER_1

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** Reserved.
7:0	0b RW	**CHANNEL_STATUS_REGISTER_1:** . These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

14.11.136 STREAM_A_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65010h

Audio HDMI CTS Register (DP Maud)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED | ENABLE_CTS_M_PROGRAMMING | HDMI_CTS_VALUES

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
24	0b RW	**ENABLE_CTS_M_PROGRAMMING:** 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	0b RW	**HDMI_CTS_VALUES:** These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

14.11.137 STREAM_A_LPE_AUD_HDMI_N_DP_NAUD—Offset 65014h

Audio HDMI N Register (DP Naud)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED							ENABLE_N_PROGRAMMING	HDMI_N_VALUES																							

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**ENABLE_N_PROGRAMMING:** 1 = Enable N programming 0 = Disable N programming
23:0	0b RW	**HDMI_N_VALUES:** These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

14.11.138 STREAM_A_LPE_AUD_BUFFER_CONFIG—Offset 65020h

LPE Audio buffer config

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65020h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000100h

Bits	31:24	23:16	15:11	10:8	7:0
Default	0000 0000	0000 0000	0000 0	001	0000 0000
Field	RESERVED	AUDIO_BUFFER_DELAY	RESERVED_1	DMA_FIFO_WATERMARK	AUDF_FIFO_WATERMARK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**AUDIO_BUFFER_DELAY:** This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	0b RW	**RESERVED_1:** Reserved.
10:8	001b RW	**DMA_FIFO_WATERMARK:** Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	0b RW	**AUDF_FIFO_WATERMARK:** Audio unit has a 96x8 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO occupancy is above the watermark then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again

14.11.139 STREAM_A_LPE_AUD_BUF_CH_SWP—Offset 65024h

Audio Sample Swapping

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00FAC688h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1	1	0	0	0	1	1	0	1	0	0	0	1	0	0	0

Bits	Field
31:24	RESERVED
23:21	SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3
20:18	SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3
17:15	SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2
14:12	SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2
11:9	SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1
8:6	SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1
5:3	SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0
2:0	SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Reserved.
23:21	111b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	110b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	101b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	100b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet
11:9	011b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	010b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
5:3	001b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	0b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

14.11.140 STREAM_A_LPE_AUD_BUF_A_ADDR—Offset 65040h

Address for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_ADDRESS	RESERVED	INTERRUPT_ENABLE	BUFFER_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.11.141 STREAM_A_LPE_AUD_BUF_A_LENGTH—Offset 65044h

Length for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:20) | BUFFER_LENGTH_ (19:0)

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

14.11.142 STREAM_A_LPE_AUD_BUF_B_ADDR—Offset 65048h

Address for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_ADDRESS (31:6) | RESERVED (5:2) | INTERRUPT_ENABLE (1) | BUFFER_VALID (0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.11.143 STREAM_A_LPE_AUD_BUF_B_LENGTH—Offset 6504Ch

Length for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6504Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:20	19:0
Default	0000 0000 0000	0000 0000 0000 0000 0000
Field	RESERVED	BUFFER_LENGTH_

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

14.11.144 STREAM_A_LPE_AUD_BUF_C_ADDR—Offset 65050h

Address for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:6	5:2	1	0
Default	0000 0000 0000 0000 0000 0000 00	0000	0	0
Field	BUFFER_ADDRESS	RESERVED	INTERRUPT_ENABLE	BUFFER_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.11.145 STREAM_A_LPE_AUD_BUF_C_LENGTH—Offset 65054h

Length for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED | BUFFER_LENGTH_

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

14.11.146 STREAM_A_LPE_AUD_BUF_D_ADDR—Offset 65058h

Address for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65058h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_ADDRESS | RESERVED | INTERRUPT_ENABLE | BUFFER_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.11.147 STREAM_A_LPE_AUD_BUF_D_LENGTH—Offset 6505Ch

Length for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6505Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | BUFFER_LENGTH_

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

14.11.148 STREAM_A_LPE_AUD_CNTL_ST—Offset 65060h

LPE Audio Control State Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	RESERVED
30:29	00	RESERVED_1
28:25	0000	RESERVED_
24:21	0000	DIP_TYPE_ENABLE_STATUS_READ_ONLY
20:18	000	DIP_BUFFER_INDEX_R_W
17:16	00	DIP_TRANSMISSION_FREQUENCY_R_W
15	0	CP_READY
14	0	RESERVED_R_W
13:9	00000	RESERVED_2
8:5	0000	RESERVED__1
4	0	RESERVED_3
3:0	0000	DIP_RAM_ACCESS_ADDRESS_R_W

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Reserved.
30:29	0b RW	**RESERVED_1:** Reserved.
28:25	0b RW	**RESERVED_:** for later DIP type if needed: Must be 0.
24:21	0b RW	**DIP_TYPE_ENABLE_STATUS_READ_ONLY:** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status (Default = disabled) XX1X = Generic 1 (ACP) DIP enable status (Default = disabled) X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 (Default = disabled) 1XXX = Reserved
20:18	0b RW	**DIP_BUFFER_INDEX_R_W:** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0 s. 000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved

Bit Range	Default & Access	Field Name (ID): Description
17:16	0b RW	**DIP_TRANSMISSION_FREQUENCY_R_W:** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	0b RW	**CP_READY:** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready CP_ready bit is programmable through Bit 14 for [DevCL, DevBLC]. CP_ready bit is programmable through Bit 15 for [DevCTG]. Bit 15 Reserved for [DevCL, DevBLC].
14	0b RW	**RESERVED_R_W:** ELD valid: This bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.0 = ELD data invalid (default, when writing ELD data, set 0 by software) 1 = ELD data valid (Set by video software only) ELD bit is programmable through Bit 13 for [DevCL, DevBLC]. ELD bit is programmable through Bit 14 for [DevCTG].
13:9	0b RW	**RESERVED_2:** ELD buffer size (read only)10000 = This field reflects the size of the ELD buffer in DWORDs 13:9 reflects ELD buffer size for [DevCTG]. 12:9 reflects ELD buffer size for [DevCL, DevBLC].
8:5	0b RW	**RESERVED__1:** ELD access address (R/W): Selects the DWORD address for access to the ELD buffer (48 bytes). The value wraps back to zero when incremented past the max addressing value 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0b RW	**RESERVED_3:** ELD ACK: Acknowledgement from the audio driver that ELD read has been completed
3:0	0b RW	**DIP_RAM_ACCESS_ADDRESS_R_W:** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

14.11.149 STREAM_A_LPE_AUD_HDMI_STATUS—Offset 65064h

LPE Audio Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31	30	29	28:24	23:16	15	14	13:3	2	1	0
Default	0	0	0	0 0 0 0 0	0 0 0 0 0 0 0 0	0	0	0 0 0 0 0 0 0 0 0 0 0	0	0	0
Field	SAMPLE_BUFFER_UNDERRUN	AUDIO_BANDWIDTH_UNDERRUN_DEBUG	LPE_AUDIO_BUFFER_DONE_STATUS	RESERVED	NUMBER_OF_SAMPLES_BEHIND_DEBUG	SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE	AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE	RESERVED_1	AZALIA_COMPATIBLE_MODE	AUDIO_SAMPLE_RUN_RATE_DEBUG	FUNCTION_RESET_R_W_ONLY

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/1C	**SAMPLE_BUFFER_UNDERRUN:** This bit indicates an underrun in the sample buffer to HDMI controller when it needs to send. This bit is set at the last line of active video when there are no more sample in any valid buffers and HDMI audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	0b RW/1C	**AUDIO_BANDWIDTH_UNDERRUN_DEBUG:** This bit indicates an underrun of audio samples at HDMI audio packet assembly even there is still available sample buffers. Audio bandwidth underrun should not happen in normal functionality but it may happen when audio setting is unappropriate and/or memory bus was blocked by other clients, etc... This bit is set at the last line of active video when there is valid samples in a valid buffer and HDMI audio unit has not satisfied number of audio samples intended in that video frame Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
29	0b RW/1C	**LPE_AUDIO_BUFFER_DONE_STATUS:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	0b RW	**RESERVED:** Reserved.
23:16	0b RO	**NUMBER_OF_SAMPLES_BEHIND_DEBUG:** This field is read only to get the number of audio samples that controller needs to load and send at the time of reading. AccessType: Read Only
15	0b RW	**SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	0b RW	**AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:3	0b RW	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**AZALIA_COMPATIBLE_MODE:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	0b RW	**AUDIO_SAMPLE_RUN_RATE_DEBUG:** When set it allows to fetch sample 128 times than the real sample rate to allow a faster drain of sample bufferes.
0	0b RW	**FUNCTION_RESET_R_W_ONLY:** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

14.11.150 STREAM_A_LPE_AUD_HDMIW_INFOFR—Offset 65068h

Audio HDMI Data Island Packet Data

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA_ISLAND_PACKET_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**DATA_ISLAND_PACKET_DATA:** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

14.11.151 STREAM_B_LPE_AUD_CONFIG—Offset 65800h

LPE Audio Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65800h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000280h

Bits	31:17	16	15	14	13	12	11	10	9	8	7	6:4	3:2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	1	0	1	0 0 0	0 0	0	0
Field	RESERVED	LPE_STREAM_B_PAUSE_RESUME	LPE_HDMI_DP_MODE_ON_STREAM_B	BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL	LEFT_ALIGNMENT	_16_BIT_CONTAINER	UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE	USER_BIT_U	VALIDITY_BIT_V	SAMPLE_FLAT_BIT	SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS	NUM	FORMAT	LAYOUT	AUDIO_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:17	0b RW	**RESERVED:** Reserved.
16	0b RW	**LPE_STREAM_B_PAUSE_RESUME:** DMA pause fetching at the boundary of buffers when this bit is set, and resume fetching when this bit is cleared. 1- DMA stop requesting more audio sample from buffer A,B,C,D after reading and depleting all data from current buffer 0- DMA resume requesting data from the next available buffer (A,B,C,D). Programming note: this bit should not be used by SW driver. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
15	0b RW	**LPE_HDMI_DP_MODE_ON_STREAM_B:** 1= DP mode 0 = HDMI mode (default)
14	0b RW	**BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL:** When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	0b RW	**LEFT_ALIGNMENT:** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container.1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)

Bit Range	Default & Access	Field Name (ID): Description
12	0b RW	**_16_BIT_CONTAINER:** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default)1= 16-bit container 0= 32-bit container
11	0b RW	**UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE:** Set this bit will enble HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Timesstamp packet) are sent to keep sink in sync even no audio sound will heard.1= send underrun packets (silent stream) 0= send null packets (default) Programming note: SW driver shall always set silent stream bit. When SW driver wants to pause audio, it shall invalidate the two newest allocated audio buffers. When the current audio buffers are processed, silent stream is sent automatically.
10	0b RW	**USER_BIT_U:** HW will clear this bit ineach sub-frames it sends, But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	1b RW	**VALIDITY_BIT_V:** HW will set this bit in both each sub-frames it sends. But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= Set V bit in sub-frame (default) 0= clear V bit in sub-frame. For debug or testing
8	0b RW	**SAMPLE_FLAT_BIT:** When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	1b RW	**SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS:** Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)
6:4	0b RW	**NUM:** audio Channels 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels 110: 8 channels Note: When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because SW ensures that an even number of samples are packed in the audio buffers. Programming note: Bit 6 of of this field is a write only bit. When reads back, it always returns zero. Ensure to write bit 6 to 1?b1 when programming for 6/7/8 audio channels.
3:2	0b RW	**FORMAT:** 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	0b RW	**LAYOUT:** 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) Note: Layout bit doesn t matter for HBR
0	0b RW	**AUDIO_ENABLE:** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted and CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

14.11.152 STREAM_B_LPE_AUD_CH_STATUS_0—Offset 65808h

Audio Channel Status Attributes 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65808h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CHANNEL_STATUS_REGISTER_0

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**CHANNEL_STATUS_REGISTER_0:** . These bits are transmitted as attributes of audio packets

14.11.153 STREAM_B_LPE_AUD_CH_STATUS_1—Offset 6580Ch

Audio Channel Status Attributes 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6580Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | CHANNEL_STATUS_REGISTER_1

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**RESERVED:** Reserved.
7:0	0b RW	**CHANNEL_STATUS_REGISTER_1:** . These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

14.11.154 STREAM_B_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65810h

Audio HDMI CTS Register (DP Maud)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65810h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | ENABLE_CTS_M_PROGRAMMING | HDMI_CTS_VALUES

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
24	0b RW	**ENABLE_CTS_M_PROGRAMMING:** 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	0b RW	**HDMI_CTS_VALUES:** These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

14.11.155 STREAM_B_LPE_AUD_HDMI_N_DP_NAUD—Offset 65814h

Audio HDMI N Register (DP Naud)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65814h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED							ENABLE_N_PROGRAMMING	HDMI_N_VALUES																							

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**ENABLE_N_PROGRAMMING:** 1 = Enable N programming 0 = Disable N programming
23:0	0b RW	**HDMI_N_VALUES:** These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

14.11.156 STREAM_B_LPE_AUD_BUFFER_CONFIG—Offset 65820h

LPE Audio buffer config

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65820h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
RESERVED								AUDIO_BUFFER_DELAY								RESERVED_1					DMA_FIFO_WATERMARK			FIFO_WATERMARK							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**AUDIO_BUFFER_DELAY:** This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	0b RW	**RESERVED_1:** Reserved.
10:8	001b RW	**DMA_FIFO_WATERMARK:** Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	0b RW	**FIFO_WATERMARK:** Audio unit has a 96x8 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO occupancy is above the watermark then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again

14.11.157 STREAM_B_LPE_AUD_BUF_CH_SWP—Offset 65824h

Audio Sample Swapping

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65824h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00FAC688h

31:24	23:21	20:18	17:15	14:12	11:9	8:6	5:3	2:0
0 0 0 0 0 0 0 0	1 1 1	1 1 0	1 0 1	1 0 0	0 1 1	0 1 0	0 0 1	0 0 0
RESERVED	SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3	SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3	SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2	SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2	SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1	SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1	SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0	SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RESERVED:** Reserved.
23:21	111b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	110b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	101b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	100b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet
11:9	011b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	010b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
5:3	001b RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	0b RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

14.11.158 STREAM_B_LPE_AUD_BUF_A_ADDR—Offset 65840h

Address for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65840h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: BUFFER_ADDRESS (31:6), RESERVED (5:2), INTERRUPT_ENABLE (1), BUFFER_VALID (0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.11.159 STREAM_B_LPE_AUD_BUF_A_LENGTH—Offset 65844h

Length for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65844h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED												BUFFER_LENGTH_																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

14.11.160 STREAM_B_LPE_AUD_BUF_B_ADDR—Offset 65848h

Address for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65848h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BUFFER_ADDRESS																										RESERVED				INTERRUPT_ENABLE	BUFFER_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.11.161 STREAM_B_LPE_AUD_BUF_B_LENGTH—Offset 6584Ch

Length for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6584Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 … 28	… 24	… 20	… 16	… 12	… 8	… 4	… 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED			BUFFER_LENGTH_				

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

14.11.162 STREAM_B_LPE_AUD_BUF_C_ADDR—Offset 65850h

Address for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65850h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 … 28	… 24	… 20	… 16	… 12	… 8	… 4	… 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Fields: BUFFER_ADDRESS | RESERVED | INTERRUPT_ENABLE | BUFFER_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.11.163 STREAM_B_LPE_AUD_BUF_C_LENGTH—Offset 65854h

Length for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65854h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:20	Bits 19:0
RESERVED	BUFFER_LENGTH_

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

14.11.164 STREAM_B_LPE_AUD_BUF_D_ADDR—Offset 65858h

Address for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65858h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BUFFER_ADDRESS																										RESERVED				INTERRUPT_ENABLE	BUFFER_VALID

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0b RW	**RESERVED:** Reserved.
1	0b RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0b RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

14.11.165 STREAM_B_LPE_AUD_BUF_D_LENGTH—Offset 6585Ch

Length for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 6585Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED												BUFFER_LENGTH_																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RW	**RESERVED:** Reserved.
19:0	0b RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

14.11.166 STREAM_B_LPE_AUD_CNTL_ST—Offset 65860h

LPE Audio Control State Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65860h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields (bit 31 to bit 0): RESERVED, RESERVED_1, RESERVED_FOR_LATER_DIP_TYPE_IF_NEEDED, DIP_TYPE_ENABLE_STATUS_READ_ONLY, DIP_BUFFER_INDEX_R_W, DIP_TRANSMISSION_FREQUENCY_R_W, CP_READY, RESERVED_2, RESERVED_3, RESERVED_, RESERVED_4, DIP_RAM_ACCESS_ADDRESS_R_W

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Reserved.
30:29	0b RW	**RESERVED_1:** Reserved.
28:25	0b RW	**RESERVED_FOR_LATER_DIP_TYPE_IF_NEEDED:** Must be 0.
24:21	0b RO	**DIP_TYPE_ENABLE_STATUS_READ_ONLY:** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status (Default = disabled) XX1X = Generic 1 (ACP) DIP enable status (Default = disabled) X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 (Default = disabled) 1XXX = Reserved AccessType: Read Only

Bit Range	Default & Access	Field Name (ID): Description
20:18	0b RW	**DIP_BUFFER_INDEX_R_W:** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0 s. 000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved
17:16	0b RW	**DIP_TRANSMISSION_FREQUENCY_R_W:** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	0b RW	**CP_READY:** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready CP_ready bit is programmable through Bit 14 for [DevCL, DevBLC]. CP_ready bit is programmable through Bit 15 for [DevCTG]. Bit 15 Reserved for [DevCL, DevBLC].
14	0b RW	**RESERVED_2:** ELD valid: This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. 0 = ELD data invalid (default, when writing ELD data, set 0 by software) 1 = ELD data valid (Set by video software only) ELD bit is programmable through Bit 13 for [DevCL, DevBLC]. ELD bit is programmable through Bit 14 for [DevCTG].
13:9	0b RW	**RESERVED_3:** ELD buffer size (read only)10000 = This field reflects the size of the ELD buffer in DWORDs 13:9 reflects ELD buffer size for [DevCTG]. 12:9 reflects ELD buffer size for [DevCL, DevBLC].
8:5	0b RW	**RESERVED_:** ELD access address (R/W): Selects the DWORD address for access to the ELD buffer (48 bytes). The value wraps back to zero when incremented past the max addressing value 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0b RW	**RESERVED_4:** ELD ACK: Acknowledgement from the audio driver that ELD read has been completed
3:0	0b RW	**DIP_RAM_ACCESS_ADDRESS_R_W:** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

14.11.167 STREAM_B_LPE_AUD_HDMI_STATUS—Offset 65864h

LPE Audio Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65864h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	SAMPLE_BUFFER_UNDERRUN_STATUS
30	0	AUDIO_BANDWIDTH_UNDERRUN_DEBUG_STATUS
29	0	LPE_AUDIO_BUFFER_DONE_STATUS
28:24	0 0 0 0 0	RESERVED
23:16	0 0 0 0 0 0 0 0	NUMBER_OF_SAMPLES_BEHIND_DEBUG
15	0	SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE
14	0	AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE
13:3	0 0 0 0 0 0 0 0 0 0 0	RESERVED_1
2	0	AZALIA_COMPATIBLE_MODE
1	0	AUDIO_SAMPLE_RUN_RATE_DEBUG
0	0	FUNCTION_RESET_R_W_ONLY

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/1C	**SAMPLE_BUFFER_UNDERRUN_STATUS:** This bit indicates an underrun in the sample buffer to HDMI/DP controller when it needs to send. This bit is set at the last line of active video when there are no more sample in any valid buffers and HDMI/DP audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	0b RW/1C	**AUDIO_BANDWIDTH_UNDERRUN_DEBUG_STATUS:** This bit indicates an underrun of audio samples at HDMI audio packet assembly even there is still available sample buffers. Audio bandwidth underrun should not happen in normal functionality but it may happen when audio setting is unappropriate and/or memory bus was blocked by other clients, etc... This bit is set at the last line of active video when there is valid samples in a valid buffer and HDMI audio unit has not satisfied number of audio samples intended in that video frame Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
29	0b RW/1C	**LPE_AUDIO_BUFFER_DONE_STATUS:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0b RO	**NUMBER_OF_SAMPLES_BEHIND_DEBUG:** This field is read only to get the number of audio samples that controller needs to load and send at the time of reading. AccessType: Read Only
15	0b RW	**SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	0b RW	**AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:3	0b RW	**RESERVED_1:** Reserved.
2	0b RW	**AZALIA_COMPATIBLE_MODE:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	0b RW	**AUDIO_SAMPLE_RUN_RATE_DEBUG:** When set it allows to fetch sample 128 times than the real sample rate to allow a faster drain of sample bufferes.
0	0b RW	**FUNCTION_RESET_R_W_ONLY:** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

14.11.168 STREAM_B_LPE_AUD_HDMIW_INFOFR—Offset 65868h

Audio HDMI Data Island Packet Data

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 65868h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA_ISLAND_PACKET_DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**DATA_ISLAND_PACKET_DATA:** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

14.11.169 PIPEA_DSL—Offset 70000h

Pipe A Display Scan Line

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CURRENT_FIELD	RESERVED																		LINE_COUNTER_FOR_DISPLAY_12												

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**CURRENT_FIELD:** [DevBLC, DevCTG, DevCDV] Provides read back of the current field being displayed on display pipe A. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode: 1 = first field (odd field) 0 = second field (even field) [DevBW] and [DevCL] Reserved: Read only.
30:13	0b RO	**RESERVED:** Read only.
12:0	0b RO	**LINE_COUNTER_FOR_DISPLAY_12:** 0]: Provides read back of the display pipe A vertical line counter. This is an indication of the current display scan line to be used by software to synchronize with the display.

14.11.170 PIPEA_SLC—Offset 70004h

Pipe A Display Scan Line Count Range Compare

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INCLUSIVE_EXCLUSIVE	RESERVED		START_SCAN_LINE_NUMBER													RESERVED_1			END_SCAN_LINE_NUMBER												

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**INCLUSIVE_EXCLUSIVE:** 1 = Inclusive: within the range. 0 = Exclusive: outside of the range.
30:29	0b RW	**RESERVED:** Read only.
28:16	0b RW	**START_SCAN_LINE_NUMBER:** [DevBLC, DevCTG, DevCDV] This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1]. [DevBW, DevCL] End Scan Line Number: This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].
15:13	0b RW	**RESERVED_1:** Read only.
12:0	0b RW	**END_SCAN_LINE_NUMBER:** [DevBLC, DevCTG, DevCDV] This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1]. [DevBW] and [DevCL] Start Scan Line Number: This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].

14.11.171 PIPEACONF—Offset 70008h

Pipe A Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	PIPE_A_ENABLE
30	0	PIPE_STATE
29	0	DSI_PLL_LOCK_LOCK
28:27	0 0	FRAME_START_DELAY
26	0	DISPLAY_PORT_AUDIO_ONLY_MODE
25	0	FORCE_BORDER
24	0	PIPE_A_GAMMA_UNIT_MODE
23:21	0 0 0	INTERLACED_MODE
20	0	MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_A_REFRESH
19	0	DISPLAY_OVERLAY_PLANES_OFF
18	0	CURSOR_PLANES_OFF
17:16	0 0	REFRESH_RATE_CXSR_MODE_ASSOCIATION
15	0	COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_A_1_COLOR_CORRECTION_COEFFICIENTS_ARE_ENABLED_TO_PERFORM_COLOR_CORRECTION_0_COLOR_CORRECTION_COEFFICIENTS_ARE_DISABLED_
14	0	DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP
13	0	COLOR_RANGE_SELECT
12	0	S3D_SPRITE_ORDER
11:10	0 0	S3D_SPRITE_INTERLEAVING_FORMAT
9:8	0 0	RESERVED
7:5	0 0 0	BITS_PER_COLOR
4	0	DITHERING_ENABLE
3:2	0 0	DITHERING_TYPE
1	0	DDA_RESET_TEST_MODE
0	0	RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PIPE_A_ENABLE:** Setting this bit to the value of one, turns on pipe A. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at it s lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. 0 = Disable 1 = Enable
30	0b RO	**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled 1 = Enabled AccessType: Read Only
29	0b RO	**DSI_PLL_LOCK_LOCK:** This bit indicates the clocks from DSI PLL are locked. 0 = Unlocked 1 = Locked AccessType: Read only
28:27	0b RW	**FRAME_START_DELAY:** (TEST MODE) Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. Care must be taken to insure that there are enough lines during VBLANK to support this setting. 00 = Frame Start occurs on the first HBLANK after the start of VBLANK 01 = Frame Start occurs on the second HBLANK after the start of VBLANK 10 = Frame Start occurs on the third HBLANK after the start of VBLANK 11 = Frame Start occurs on the forth HBLANK after the start of VBLANK
26	0b RW	**DISPLAY_PORT_AUDIO_ONLY_MODE:** [DevVLVP] Setting this bit to 1 indicates the DisplayPort will output audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	0b RW	**FORCE_BORDER:** : (TEST MODE)0 = Normal Operation 1 = Color information is ignored and border color is substituted during active region
24	0b RW	**PIPE_A_GAMMA_UNIT_MODE:** This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. VGA and indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay or sprite are unaffected by this bit. 0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode
23:21	0b RW	**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift. (2x) 101 = Interlaced using vertical sync shift. Backup option to 110 setting. (2x) 110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used Note: VGA display modes, sDVO line stall, and Panel fitting do not work while in interlaced modes Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	0b RW	**MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_A_REFRESH:** 0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only

Bit Range	Default & Access	Field Name (ID): Description
19	0b RW	**DISPLAY_OVERLAY_PLANES_OFF:** This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
18	0b RW	**CURSOR_PLANES_OFF:** This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the cursor(s) no longer appear on the screen. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
17:16	0b RW	**REFRESH_RATE_CXSR_MODE_ASSOCIATION:** These bits select how refresh rates are tied to big FIFO mode on pipe A. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated dispay panels that support corresponding mode. 00 Default no dynamic refresh rate change enabled. Software control only. 01 Progressive-to-progressive refresh rate change enabled and tied to big FIFO mode. Pixel clock values set in FPA0/FPA1 settings in the DPLLA control register and FPA0/FPA1 divider registers. FPA0 is tied to non-big-FIFO mode 10 Progressive-to-interlaced refresh rate change enabled and tied to big FIFO mode. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 Reserved
15	0b RW	**COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_A_1_COLOR_CORRECTION_COEFFICIENTS_ARE_ENABLED_TO_PERFORM_COLOR_CORRECTION_0_COLOR_CORRECTION_COEFFICIENTS_ARE_DISABLED_:** • 1 = Color Correction Coefficients are enabled to perform color correction • 0 = Color Correction Coefficients are disabled
14	0b RW	**DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP:** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 Normal progressive refresh rate (default) 1 Low Power progressive refresh rate
13	0b RW	**COLOR_RANGE_SELECT:** [DevVLVP]: This bit is used to select the color range of RBG outputs. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
12	0b RW	**S3D_SPRITE_ORDER:** This bit controls the blending order of the sprite planes for S3D support: 0 = Sprite A first. The first line or pixel comes from Sprite A (default) 1 = Sprite B first. The first line or pixel comes from Sprite B
11:10	0b RW	**S3D_SPRITE_INTERLEAVING_FORMAT:** These bits control the Sprite A/B interleaving format in S3D mode 00 = No interleaving 01 = Line interleaving 10 = Pixel interleaving 11 = Reserved
9:8	0b RW	**RESERVED:** [DevCDV, DevVLVP] MBZ Scrambling enable [DevCTG]: This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 = Scrambling disabled (Default) 01 = Scrambling enabled, no SR after initialization at loop 2 of training 10 - RESERVED 11 = Scrambling and SR enabled. Scrambling is reset every 512 BS symbols.

Bit Range	Default & Access	Field Name (ID): Description
7:5	0b RW	**BITS_PER_COLOR:** [DevCTG, DevCDV, DevVLVP]: This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change in DisplayPort. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to DP Frequency Programming in DPLL section of Bspec. 000 = 8 bits per color (Default) 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED
4	0b RW	**DITHERING_ENABLE:** [DevCTG, DevCDV]: This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled (Default) 1 Dithering enabled Programming note: Dithering should only be enabled for 8 bpc or 6 bpc.
3:2	0b RW	**DITHERING_TYPE:** [DevCTG, DevCDV]: This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 - Spatial only (default) 01- Spatio-Temporal 1 10- Spatio-Temporal 2 (testmode) 11- Temporal only (testmode)
1	0b RW	**DDA_RESET_TEST_MODE:** [DevCTG, DevCDV]: 0 Do not reset DDA 1 Reset DDA every 8th display frame
0	0b RW	**RESERVED_1:** Write as zero

14.11.172 PIPEAGCMAXRED—Offset 70010h

Pipe A Gamma Correction Max Red

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (bits 31:17) | MAX_RED_GAMMA_CORRECTION_POINT (bits 16:0)

Bit Range	Default & Access	Field Name (ID): Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	100000000 00000000b RW	**MAX_RED_GAMMA_CORRECTION_POINT:** 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

14.11.173 PIPEAGCMAXGREEN—Offset 70014h

Pipe A Gamma Correction Max Green

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED															MAX_GREEN_GAMMA_CORRECTION_POINT																

Bit Range	Default & Access	Field Name (ID): Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	10000000000000000b RW	**MAX_GREEN_GAMMA_CORRECTION_POINT:** 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

14.11.174 PIPEAGCMAXBLUE—Offset 70018h

Pipe A Gamma Correction Max Blue

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (bits 31:17) | MAX_BLUE_GAMMA_CORRECTION_POINT (bits 16:0)

Bit Range	Default & Access	Field Name (ID): Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	100000000 00000000b RW	**MAX_BLUE_GAMMA_CORRECTION_POINT:** 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

14.11.175 PIPEASTAT—Offset 70024h

Pipe A Display Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	FIFO_A_UNDER_RUN_STATUS
	0	SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE
	0	CRC_ERROR_ENABLE
28	0	CRC_DONE_ENABLE
	0	GMBUS_EVENT_ENABLE
	0	PLANE_A_FLIP_DONE_INTERRUPT_ENABLE
	0	VERTICAL_SYNC_INTERRUPT_ENABLE
24	0	DISPLAY_LINE_COMPARE_ENABLE
	0	DPST_EVENT_ENABLE
	0	SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE
	0	ODD_FIELD_INTERRUPT_EVENT_ENABLE
20	0	EVEN_FIELD_INTERRUPT_EVENT_ENABLE
	0	PERFORMANCE_COUNTER_EVENT_ENABLE
	0	START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE
	0	FRAMESTART_INTERRUPT_ENABLE
16	0	PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE
	0	SPRITE_B_FLIP_DONE_INTERRUPT_STATUS
	0	SPRITE_A_FLIP_DONE_INTERRUPT_STATUS
	0	CRC_ERROR_INTERRUPT_STATUS
12	0	CRC_DONE_INTERRUPT_STATUS
	0	GMBUS_INTERRUPT_STATUS
	0	PLANE_A_FLIP_DONE_INTERRUPT_STATUS
	0	VERTICAL_SYNC_INTERRUPT_STATUS
8	0	DISPLAY_LINE_COMPARE_INTERRUPT_STATUS
	0	DPST_EVENT_STATUS
	0	PIPE_A_PANEL_SELF_REFRESH_STATUS
	0	ODD_FIELD_INTERRUPT_STATUS
4	0	EVEN_FIELD_INTERRUPT_STATUS
	0	PERFORMANCE_MONITOR_EVENT_INTERRUPT
	0	START_OF_VERTICAL_BLANK_INTERRUPT_STATUS
	0	FRAMESTART_INTERRUPT_STATUS
0	0	PIPE_A_HORIZONTAL_BLANK_STATUS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/1C	**FIFO_A_UNDER_RUN_STATUS:** Set when a pipe A FIFO under-run occurs, cleared by a write of a 1. An underrun has occurred on an attempt to pop an empty FIFO. This does not feed into the first line interrupt status register. This will occur naturally during mode changes, to be useful, it should be cleared after a mode change has occurred. This bit is only valid after Pipe A has been completely configured. 1 = FIFO A Underflow occurred 0 = FIFO A Underflow did not occur AccessType: One to Clear
30	0b RW	**SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite B flip done interrupt status bit in the first line interrupt logic 0 = Sprite B Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
29	0b RW	**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Error Detect Disabled 1 = CRC Error Detect Enabled
28	0b RW	**CRC_DONE_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Done Detect Disabled 1 = CRC Done Detect Enabled
27	0b RW	**GMBUS_EVENT_ENABLE:** This will enable the use of the GMBUS interrupt status bit in the first line interrupt/status logic. 0 = No GMBUS event enabled 1 = GMBUS event enabled
26	0b RW	**PLANE_A_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Plane A flip done interrupt status bit in the first line interrupt logic 0 = Plane A flip done Interrupt/Status Disabled 1 = Plane A flip done Interrupt/Status Enabled
25	0b RW	**VERTICAL_SYNC_INTERRUPT_ENABLE:** This will enable the consideration of the vertical sync interrupt status bit in the first line interrupt logic. 0 = Vertical Sync Interrupt/Status Disabled 1 = Vertical Sync Interrupt/Status Enabled
24	0b RW	**DISPLAY_LINE_COMPARE_ENABLE:** This will enable the consideration of the line compare interrupt status bit in the first line interrupt/status logic. 0 = Display Line Compare Interrupt/Status Disabled 1 = Display Line Compare Interrupt/Status Enabled

Bit Range	Default & Access	Field Name (ID): Description
23	0b RW	**DPST_EVENT_ENABLE:** [DevCL, DevCTG, DevCDV]: This interrupt is generated by the DPST logic. 0 = No DPST event enabled 1 = DPST event enabled
22	0b RW	**SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite A flip done interrupt status bit in the first line interrupt logic 0 = Sprite A Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled
21	0b RW	**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** This bit should only be used when this pipe is in an interlaced display timing. 0 = Odd Field Event disable 1 = Odd Field Event enable
20	0b RW	**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** This bit should only be used when this pipe is in an interlaced display timing. 0 = Even field Event disable 1 = Even field Event enable
19	0b RW	**PERFORMANCE_COUNTER_EVENT_ENABLE:** perfomance counter event enable
18	0b RW	**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/ status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	0b RW	**FRAMESTART_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Vertical Blank Interrupt/Status Disabled 1 = Vertical Blank Interrupt/Status Enabled
16	0b RW	**PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** : This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled
15	0b RW/1C	**SPRITE_B_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite B 0 = Sprite B Flip Not Done 1 = Sprite B Flip Done AccessType: One to Clear
14	0b RW/1C	**SPRITE_A_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite A 0 = Sprite A Flip Not Done 1 = Sprite A Flip Done AccessType: One to Clear
13	0b RW/1C	**CRC_ERROR_INTERRUPT_STATUS:** This sticky status bit is set when a Pipe A CRC error is detected. It is cleared by a write of a one. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = No CRC error has occurred 1 = CRC Error Detected AccessType: One to Clear
12	0b RW/1C	**CRC_DONE_INTERRUPT_STATUS:** This sticky status bit is set when Pipe A CRC calculation and compare are complete. It is cleared by a write of a one. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = CRC Not Done 1 = CRC Done AccessType: One to Clear
11	0b RW/1C	**GMBUS_INTERRUPT_STATUS:** This status bit will be set on a GMBUS event. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = GMBUS event has not occurred 1 = GMBUS event has occurred AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
10	0b RW/1C	**PLANE_A_FLIP_DONE_INTERRUPT_STATUS:** Async/Sync Flip Event is completed on Display Plane A 0 = Plane A Flip Not Done 1 = Plane A Flip Done AccessType: One to Clear
9	0b RW/1C	**VERTICAL_SYNC_INTERRUPT_STATUS:** This bit provides a sticky status that is set when a pipe A vertical sync occurs, cleared by a write of a 1. For interlaced timing modes, this occurs once per field, when in progressive, it occurs once per frame. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = Vertical Sync has not occurred 1 = Vertical Sync has occurred AccessType: One to Clear
8	0b RW/1C	**DISPLAY_LINE_COMPARE_INTERRUPT_STATUS:** Set when a pipe A compare match occurs, cleared by a write of a 1. 0 = Display Line Compare has not been satisfied 1 = Display Line Compare has been satisfied AccessType: One to Clear
7	0b RW/1C	**DPST_EVENT_STATUS:** [DevCL, DevCTG, DevCDV]: This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. Multiple DPST events (Histogram or Phase In) can cause this bit to be asserted, determination of which event occurred is done in the DPST registers. 0 = DPST Interrupt has not occurred on pipe A 1 = DPST Interrupt has occurred on pipe A AccessType: One to Clear
6	0b RW/1C	**PIPE_A_PANEL_SELF_REFRESH_STATUS:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe A 1 = PSR interrupt has occurred on pipe A AccessType: One to Clear
5	0b RW/1C	**ODD_FIELD_INTERRUPT_STATUS:** This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear
4	0b RW/1C	**EVEN_FIELD_INTERRUPT_STATUS:** This status bit will be set on a even field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	0b RW/1C	**PERFORMANCE_MONITOR_EVENT_INTERRUPT:** AccessType: One to Clear
2	0b RW/1C	**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW/1C	**FRAMESTART_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Vertical Blank has not occurred 1 = Vertical Blank has occurred AccessType: One to Clear
0	0b RW/1C	**PIPE_A_HORIZONTAL_BLANK_STATUS:** 0 = Pipe A Horizontal Blank has not occurred 1 = Pipe A Horizontal Blank has occurred AccessType: One to Clear

14.11.176 DPFLIPSTAT—Offset 70028h

Display FLIP Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70028h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31:30	00	RESERVED
29	0	DISPLAY_PIPE_B_LINE_COMPARE_INTERRUPT_STATUS_ENABLE
28	0	PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE
27	0	PIPE_B_VERTICAL_BLANK_INTERRUPT_ENABLE
26	0	SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE
25	0	SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE
24	0	PLANE_B_FLIP_DONE_INTERRUPT_ENABLE
23	0	RESERVED_1
22	0	PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_A_0_PSR_INTERRUPT_DISABLED_ON_PIPE_A_1_PSR_INTERRUPT_ENABLED_ON_PIPE_A
21	0	DISPLAY_PIPE_A_LINE_COMPARE_INTERRUPT_STATUS_ENABLE
20	0	PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE
19	0	PIPE_A_VERTICAL_BLANK_INTERRUPT_ENABLE
18	0	SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE
17	0	SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE
16	0	PLANE_A_FLIP_DONE_INTERRUPT_ENABLE
15:0	0000000000000000	RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** MBZ
29	0b RW	**DISPLAY_PIPE_B_LINE_COMPARE_INTERRUPT_STATUS_ENABLE:** 0 = Display Pipe B Line Compare Interrupt Disabled 1 = Display Pipe B Line Compare Interrupt Enabled
28	0b RW	**PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe B Horizontal Blank Interrupt Disabled 1 = Pipe B Horizontal Blank Interrupt Enabled
27	0b RW	**PIPE_B_VERTICAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe B Vertical Blank Interrupt Disabled 1 = Pipe B Vertical Blank Interrupt Enabled
26	0b RW	**SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite D Flip Done Interrupt Disabled 1 = Sprite D Flip Done Interrupt Enabled
25	0b RW	**SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite C Flip Done Interrupt Disabled 1 = Sprite C Flip Done Interrupt Enabled
24	0b RW	**PLANE_B_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Plane B Flip Done Interrupt Disabled 1 = Plane B Flip Done Interrupt Enabled
23	0b RW	**RESERVED_1:** Reserved.
22	0b RW	**PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_A_0_PSR_INTERRUPT_DISABLED_ON_PIPE_A_1_PSR_INTERRUPT_ENABLED_ON_PIPE_A:** • 0 = PSR interrupt Disabled on Pipe A • 1 = PSR Interrupt Enabled on Pipe A
21	0b RW	**DISPLAY_PIPE_A_LINE_COMPARE_INTERRUPT_STATUS_ENABLE:** 0 = Display Pipe A Line Compare Interrupt Disabled 1 = Display Pipe A Line Compare Interrupt Enabled
20	0b RW	**PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe A Horizontal Blank Interrupt Disabled 1 = Pipe A Horizontal Blank Interrupt Enabled
19	0b RW	**PIPE_A_VERTICAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe A Vertical Blank Interrupt Disabled 1 = Pipe A Vertical Blank Interrupt Enabled
18	0b RW	**SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite B Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
17	0b RW	**SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite A Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled
16	0b RW	**PLANE_A_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Plane A Flip Done Interrupt Disabled 1 = Plane A Flip Done Interrupt Enabled
15:0	0b RW	**RESERVED_2:** MBZ

14.11.177 DPINVGTT—Offset 7002Ch

Display Invalid GTT PTE Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7002Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	RESERVED
23	0	CURSOR_B_INVALID_GTT_PTE_INTERRUPT_ENABLE
22	0	CURSOR_A_INVALID_GTT_PTE_INTERRUPT_ENABLE
21	0	SPRITE_D_INVALID_GTT_PTE_INTERRUPT_ENABLE
20	0	SPRITE_C_INVALID_GTT_PTE_INTERRUPT_ENABLE
19	0	PLANE_B_INVALID_GTT_PTE_INTERRUPT_ENABLE
18	0	SPRITE_B_INVALID_GTT_PTE_INTERRUPT_ENABLE
17	0	SPRITE_A_INVALID_GTT_PTE_INTERRUPT_ENABLE
16	0	PLANE_A_INVALID_GTT_PTE_INTERRUPT_ENABLE
15:8	0 0 0 0 0 0 0 0	RESERVED_1
7	0	CURSOR_B_INVALID_GTT_PTE_STATUS
6	0	CURSOR_A_INVALID_GTT_PTE_STATUS
5	0	SPRITE_D_INVALID_GTT_PTE_STATUS
4	0	SPRITE_C_INVALID_GTT_PTE_STATUS
3	0	PLANE_B_INVALID_GTT_PTE_STATUS
2	0	SPRITE_B_INVALID_GTT_PTE_STATUS
1	0	SPRITE_A_INVALID_GTT_PTE_STATUS
0	0	PLANE_A_INVALID_GTT_PTE_STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** MBZ
23	0b RW	**CURSOR_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Cursor B Invalid GTT PTE Interrupt Disabled 1 = Cursor B Invalid GTT PTE Interrupt Enabled
22	0b RW	**CURSOR_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Cursor A Invalid GTT PTE Interrupt Disabled 1 = Cursor A Invalid GTT PTE Interrupt Enabled
21	0b RW	**SPRITE_D_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite D Invalid GTT PTE Interrupt Disabled 1 = Sprite D Invalid GTT PTE Interrupt Enabled
20	0b RW	**SPRITE_C_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite C Invalid GTT PTE Interrupt Disabled 1 = Sprite C Invalid GTT PTE Interrupt Enabled
19	0b RW	**PLANE_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Plane B Invalid GTT PTE Interrupt Disabled 1 = Plane B Invalid GTT PTE Interrupt Enabled
18	0b RW	**SPRITE_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite B Invalid GTT PTE Interrupt Disabled 1 = Sprite B Invalid GTT PTE Interrupt Enabled
17	0b RW	**SPRITE_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite A Invalid GTT PTE Interrupt Disabled 1 = Sprite A Invalid GTT PTE Interrupt Enabled

Bit Range	Default & Access	Field Name (ID): Description
16	0b RW	**PLANE_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Plane A Invalid GTT PTE Interrupt Disabled 1 = Plane A Invalid GTT PTE Interrupt Enabled
15:8	0b RW	**RESERVED_1:** MBZ
7	0b RW/1C	**CURSOR_B_INVALID_GTT_PTE_STATUS:** 0 = Cursor B encountered an invalid GTT PTE has not occurred 1 = Cursor B encountered an invalid GTT PTE has occurred AccessType: One to Clear
6	0b RW/1C	**CURSOR_A_INVALID_GTT_PTE_STATUS:** 0 = Cursor A encountered an invalid GTT PTE has not occurred 1 = Cursor A encountered an invalid GTT PTE has occurred AccessType: One to Clear
5	0b RW/1C	**SPRITE_D_INVALID_GTT_PTE_STATUS:** 0 = Sprite D encountered an invalid GTT PTE has not occurred 1 = Sprite D encountered an invalid GTT PTE has occurred. AccessType: One to Clear
4	0b RW/1C	**SPRITE_C_INVALID_GTT_PTE_STATUS:** 0 = Sprite C encountered an invalid GTT PTE has not occurred 1 = Sprite C encountered an invalid GTT PTE has occurred. AccessType: One to Clear
3	0b RW/1C	**PLANE_B_INVALID_GTT_PTE_STATUS:** 0 = Plane B encountered an invalid GTT PTE has not occurred 1 = Plane B encountered an invalid GTT PTE has occurred. AccessType: One to Clear
2	0b RW/1C	**SPRITE_B_INVALID_GTT_PTE_STATUS:** 0 = Sprite B encountered an invalid GTT PTE has not occurred 1 = Sprite B encountered an invalid GTT PTE has occurred. AccessType: One to Clear
1	0b RW/1C	**SPRITE_A_INVALID_GTT_PTE_STATUS:** 0 = Sprite A encountered an invalid GTT PTE has not occurred 1 = Sprite A encountered an invalid GTT PTE has occurred. AccessType: One to Clear
0	0b RW/1C	**PLANE_A_INVALID_GTT_PTE_STATUS:** 0 = Plane A encountered an invalid GTT PTE has not occurred 1 = Plane A encountered an invalid GTT PTE has occurred. AccessType: One to Clear

14.11.178 DSPARB—Offset 70030h

Display Arbitration Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70030h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 80008000h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPRITE_D_START								SPRITE_CSTART								SPRITE_BSTART								SPRITE_ASTART							

Bit Range	Default & Access	Field Name (ID): Description
31:24	10000000b RW	**SPRITE_D_START:** This field selects the end of the ram used for Sprite C and the start of the RAM for Sprite D. If sprite C is unused, this field can be set to the same value as Sprite C START. If Sprite D is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite C START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite C FIFO will be (Sprite D START-Sprite C START)*64. The size of the Sprite D FIFO will be (TOTALSIZE-Sprite D START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
23:16	0b RW	**SPRITE_CSTART:** This field selects the end of the ram used for display B and the start of the RAM for Sprite C. If display B is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display B FIFO will be (Sprite C START)*64 bytes.
15:8	10000000b RW	**SPRITE_BSTART:** This field selects the end of the ram used for Sprite A and the start of the RAM for Sprite B. If sprite A is unused, this field can be set to the same value as Sprite A START. If Sprite B is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite A START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite A FIFO will be (Sprite B START-Sprite A START)*64. The size of the Sprite B FIFO will be (TOTALSIZE-Sprite B START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
7:0	0b RW	**SPRITE_ASTART:** This field selects the end of the ram used for display A and the start of the RAM for Sprite A. If display A is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display A FIFO will be (Sprite A START)*64 bytes.

14.11.179 FW1—Offset 70034h

Display FIFO Watermark Control 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70034h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 3F8F0F0Fh

31			28				24				20				16				12				8				4				0
0	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

DISPLAY_FIFO_SELF_REFRESH_WATERMARK_PROGRAMMING | RESERVED_ | CURSOR_B_FIFO_WATERMARK_ | DISPLAY_PLANE_B_FIFO_WATERMARK | DISPLAY_PLANE_A_FIFO_WATERMARK

Bit Range	Default & Access	Field Name (ID): Description
31:23	001111111b RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK_PROGRAMMING:** This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note [DevCL, DevCTG, DevCDV]: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.
22	0b RW	**RESERVED_:** MBZ
21:16	001111b RW	**CURSOR_B_FIFO_WATERMARK_:** Number in 64Bs of space in the Cursor B FIFO above which the Cursor B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). DevBW, DevCL, DevCDV] Always program to 8.
15:8	00001111b RW	**DISPLAY_PLANE_B_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). [DevBW, DevCL, DevCDV] Always program to 8.
7:0	00001111b RW	**DISPLAY_PLANE_A_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). [DevBW, DevCL, DevCDV] Always program to 8.

14.11.180 FW2—Offset 70038h

Display FIFO Watermark Control 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70038h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 0B0F0F0Fh

Bits	31	30:28	27:24	23:16	15:14	13:8	7:0
Default	0	0 0 0	1 0 1 1	0 0 0 0 1 1 1 1	0 0	0 0 1 1 1 1	0 0 0 0 1 1 1 1
Field	RESERVED	RESERVED_1	RESERVED_2	RESERVED_3	RESERVED_4	CURSOR_A_FIFO_WATERMARK_	DEVBLKC_DEVCTG_DISPLAY_PLANE_SPRITE_A_FIFO_WATERMARK

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** [DevCDV]: [DevCTG] FBC SR Watermark Enable: Enables the FBC watermarks to be used in the fetch calculation 0: disabled 1: enabled
30:28	0b RW	**RESERVED_1:** [DevCDV]: [DevCTG] FBC SR Watermark: Number of equivalent lines of the primary display SR watermark
27:24	1011b RW	**RESERVED_2:** [DevCDV] [DevCTG] FBC SR HPLL Watermark: Number of equivalent lines of the primary display SR HPLL watermark.
23:16	00001111b RW	**RESERVED_3:** [DevCDV]: [DevBLKC, DevCTG] Display Plane Sprite B FIFO Watermark Number in 64Bs of space in FIFO above which the Display Sprite B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:14	0b RW	**RESERVED_4:** : MBZ
13:8	001111b RW	**CURSOR_A_FIFO_WATERMARK_:** Number in 64Bs of space in the Cursor A FIFO above which the Cursor A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). DevBW, DevCL, DevCDV] Always program to 8.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00001111b RW	**DEVBLKC_DEVCTG_DISPLAY_PLANE_SPRITE_A_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display Sprite A Stream will generate requests to Memory DevBW, DevCL] Display Plane C FIFO Watermark. Number in 64Bs of space in FIFO above which the Display C Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). [DevBW, DevCL, DevCDV] Always program to 8.

14.11.181 FW3—Offset 7003Ch

Display FIFO Watermark Control 3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7003Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	ENABLE_HPLL_OFF_DURING_SELF_REFRESH
30	0	RESERVED
29:24	000000	CURSOR_FIFO_SELF_REFRESH_WATERMARK
23:22	00	RESERVED_1
21:16	000000	HPLL_SELF_REFRESH_CURSOR_WATERMARK
15:9	0000000	RESERVED_
8:0	000000000	HPLL_SELF_REFRESH_DISPLAY_WATERMARK

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_HPLL_OFF_DURING_SELF_REFRESH:** . 0 = Disabled 1 = Enabled [DevCL] This bit may be enabled only if the BLC_PWM_CTL duty cycle register offset (0x61254) is programmed to 100% and non-legacy backlight is enabled. This restriction does not apply when I2C is used for back light modulation. [DevCL] When one or more display pipes are enabled, this bit should be disabled before accessing the 6XXXh MMIO register address space. Software must follow these steps: disable this bit (if enabled and one display pipe is enabled) wait for next vblank (switch from hrawclk back to cdclk will occur) access the 6XXXh address space as needed re-enable this bit Note that the wait on next vblank step requires an enabled display pipe.
30	0b RW	**RESERVED:** : MBZ

Bit Range	Default & Access	Field Name (ID): Description
29:24	0b RW	**CURSOR_FIFO_SELF_REFRESH_WATERMARK:** . Number in 64Bs of space in the Cursor FIFO above which the Cursor Stream will generate requests to Memory during self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
23:22	0b RW	**RESERVED_1:** : MBZ
21:16	0b RW	**HPLL_SELF_REFRESH_CURSOR_WATERMARK:** . Number in 64Bs of space in the Cursor FIFO above which the Cursor Stream will generate requests to Memory during HPLL self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:9	0b RW	**RESERVED_:** MBZ
8:0	0b RW	**HPLL_SELF_REFRESH_DISPLAY_WATERMARK:** . Number in 64Bs of space in the FIFO above which the Display Stream will generate requests to Memory during HPLL self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

14.11.182 PIPEAFRAMECOUNT—Offset 70040h

Pipe A Frame Counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PIPE_A_FRAME_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**PIPE_A_FRAME_COUNT:** Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after 2^32 frames

14.11.183 PIPEAFLIPCOUNT—Offset 70044h

Pipe A Flip Counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PIPE_A_FLIP_COUNTER

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**PIPE_A_FLIP_COUNTER:** Provides read back of the display pipe flip counter. This counter increments on each flip of the surface of the primary plane on this pipe. This includes command streamer asynchronous and synchronous flips and any MMIO writes to the primary plane surface address. It rolls over back to 0 after 2^32 flips

14.11.184 PIPEAMSAMISC—Offset 70048h

Pipe A MSA MISC

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HARDWARE_DRIVE_MSA_MISC1_ENABLE	RESERVED																												MSA_MISC1_FIELD_S3D		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**HARDWARE_DRIVE_MSA_MISC1_ENABLE:** This bit enables hardware to drive MSA MISC1 bit3:1 with the stero 3D left/right eye field indication. Hardware will drive 000 when S3D mode is disabled, 001 when enabled and the upcoming video frame is right eye, 011 when enabled and the upcoming video frame is left eye. When this bit is disabled, software may manually program the MSA MISC1 Field S3D field in bit 2:0 in this register to set MISC1 bit 3:1 0 = Disable hardware driving MSA MISC1 bit 3:1. Allow software to manually program MSA MISC1 bit3:1 through MSA_MISC1_FIELD_S3D (default) 1 = Enable hardware to drive MSA MISC1 bit3:1 for S3D
30:3	0b RW	**RESERVED:** Reserved.
2:0	0b RW	**MSA_MISC1_FIELD_S3D:** This field provides software to manually program MSC1 stereo video attribute for DisplayPort: 000 = No stereo video transported 001 = For progressive video, the next (upcoming) video frame is RIGHT eye 010 = Reserved 011 = For progressive video, the next (upcoming) video frame is LEFT eye 100 = Stacked top and bottom top half represents left-eye view and bottom half represents right-eye view 101 = Stacked top and bottom top half represents right-eye view and bottom half represents left-eye view

14.11.185 DDL1—Offset 70050h

Display FIFO Drain Latency 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70050h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DISPLAY_CURSOR_A_DRAIN_LATENCY_PRECISION_SELECT	CURSOR_A_DRAIN_LATENCY_VALUE							DISPLAY_SPRITE_B_DRAIN_LATENCY_PRECISION_SELECT	SPRITE_B_DRAIN_LATENCY_VALUE							DISPLAY_SPRITE_A_DRAIN_LATENCY_PRECISION_SELECT	SPRITE_A_DRAIN_LATENCY_VALUE							DISPLAY_PLANE_A_DRAIN_LATENCY_PRECISION_SELECT	DISPLAY_PLANE_A_DRAIN_LATENCY_VALUE						

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DISPLAY_CURSOR_A_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multipler to increase precision to be stored in 7-bit Cursor A drain latency value 0 use 32 as precision multipler to increase percision to be stored in 7-bit Cursor A drain latency value
30:24	0b RW	**CURSOR_A_DRAIN_LATENCY_VALUE:** [DevVLVP] For cursor latency, 4 BPP is assumed for all cursor formats. : Programmable drain latency value in time ticks per 64B FIFO entry
23	0b RW	**DISPLAY_SPRITE_B_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multipler to increase precision to be stored in 7-bit Sprite B drain latency value 0 use 32 as precision multipler to increase percision to be stored in 7-bit Sprite B drain latency value
22:16	0b RW	**SPRITE_B_DRAIN_LATENCY_VALUE:** [DevVLVP] Programmable drain latency value in time ticks per 64B FIFO entry
15	0b RW	**DISPLAY_SPRITE_A_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multipler to increase precision to be stored in 7-bit Sprite A drain latency value 0 use 32 as precision multipler to increase percision to be stored in 7-bit Sprite A drain latency value
14:8	0b RW	**SPRITE_A_DRAIN_LATENCY_VALUE:** [DevVLVP] Programmable drain latency value in time ticks per 64B FIFO entry
7	0b RW	**DISPLAY_PLANE_A_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multipler to increase precision to be stored in 7-bit Plane A drain latency value 0 use 32 as precision multipler to increase percision to be stored in 7-bit Plane A drain latency value
6:0	0b RW	**DISPLAY_PLANE_A_DRAIN_LATENCY_VALUE:** [DevVLVP] Programmable drain latency value in time ticks per 64B FIFO entry

14.11.186 DDL2—Offset 70054h

Display FIFO Drain Latency 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70054h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	DISPLAY_CURSOR_B_DRAIN_LATENCY_PRECISION_SELECT
30:24	0 0 0 0 0 0 0	CURSOR_B_DRAIN_LATENCY_VALUE
23	0	DISPLAY_SPRITE_D_DRAIN_LATENCY_PRECISION_SELECT
22:16	0 0 0 0 0 0 0	SPRITE_D_DRAIN_LATENCY_VALUE
15	0	DISPLAY_SPRITE_C_DRAIN_LATENCY_PRECISION_SELECT
14:8	0 0 0 0 0 0 0	SPRITE_C_DRAIN_LATENCY_VALUE
7	0	DISPLAY_PLANE_B_DRAIN_LATENCY_PRECISION_SELECT
6:0	0 0 0 0 0 0 0	DISPLAY_PLANE_B_DRAIN_LATENCY_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DISPLAY_CURSOR_B_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multipler to increase precision to be stored in 7-bit Cursor B drain latency value 0 use 32 as precision multipler to increase percision to be stored in 7-bit Cursor B drain latency value
30:24	0b RW	**CURSOR_B_DRAIN_LATENCY_VALUE:** [DevVLVP] For cursor latency, 4 BPP is assumed for all cursor formats
23	0b RW	**DISPLAY_SPRITE_D_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multipler to increase precision to be stored in 7-bit Sprite D drain latency value 0 use 32 as precision multipler to increase percision to be stored in 7-bit Sprite D drain latency value
22:16	0b RW	**SPRITE_D_DRAIN_LATENCY_VALUE:** [DevVLVP]

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW	**DISPLAY_SPRITE_C_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multipler to increase precision to be stored in 7-bit Sprite C drain latency value 0 use 32 as precision multipler to increase percision to be stored in 7-bit Sprite C drain latency value
14:8	0b RW	**SPRITE_C_DRAIN_LATENCY_VALUE:** [DevVLVP]
7	0b RW	**DISPLAY_PLANE_B_DRAIN_LATENCY_PRECISION_SELECT:** [DevVLVP] 1 use 64 as precision multipler to increase precision to be stored in 7-bit Plane B drain latency value 0 use 32 as precision multipler to increase percision to be stored in 7-bit Plane B drain latency value
6:0	0b RW	**DISPLAY_PLANE_B_DRAIN_LATENCY_VALUE:** [DevVLVP]

14.11.187 DSPARB2—Offset 70060h

Display Arbitration Control 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70060h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00001111h

Bits	Default	Field
31:13	0000 0000 0000 0000 000	RESERVED
12	1	SPRITE_D_START_HIGH_ORDER
11:9	000	RESERVED_1
8	1	SPRITE_CSTART_HIGH_ORDER
7:5	000	RESERVED_MBZ
4	1	SPRITE_B_START_HIGH_ORDER
3:1	000	RESERVED_MBZ_1
0	1	SPRITE_A_START_HIGH_ORDER

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**RESERVED:** Reserved.
12	1b RW	**SPRITE_D_START_HIGH_ORDER:** This field is the high order bits for Sprite D Start pointer. Combinbed with lower order 8-bit Sprite D Start pointer, this field selects the end of the ram used for Sprite C and the start of the RAM for Sprite D. If sprite C is unused, this field can be set to the same value as Sprite C START. If Sprite D is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite C START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite C FIFO will be (Sprite D START-Sprite C START)*64. The size of the Sprite D FIFO will be (TOTALSIZE-Sprite D START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
11:9	0b RW	**RESERVED_1:** Reserved.
8	1b RW	**SPRITE_CSTART_HIGH_ORDER:** This field is the high order bits for Sprite C Start pointer. Combinbed with lower order 8-bit Sprite C Start pointer, this field selects the end of the ram used for display B and the start of the RAM for Sprite C. If display B is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display B FIFO will be (Sprite C START)*64 bytes.
7:5	0b RW	**RESERVED_MBZ:** Reserved.
4	1b RW	**SPRITE_B_START_HIGH_ORDER:** This field is the high order bits for Sprite B Start pointer. Combinbed with lower order 8-bit Sprite B Start pointer, this field selects the end of the ram used for Sprite A and the start of the RAM for Sprite B. If sprite A is unused, this field can be set to the same value as Sprite A START. If Sprite B is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite A START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite A FIFO will be (Sprite B START-Sprite A START)*64. The size of the Sprite B FIFO will be (TOTALSIZE-Sprite B START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
3:1	0b RW	**RESERVED_MBZ_1:** Reserved.
0	1b RW	**SPRITE_A_START_HIGH_ORDER:** This field is the high order bits for Sprite A Start pointer. Combinbed with lower order 8-bit Sprite A Start pointer, this field selects the end of the ram used for display A and the start of the RAM for Sprite A. If display A is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display A FIFO will be (Sprite A START)*64 bytes.

14.11.188 DSPHOWM—Offset 70064h

Display FIFO WM High Order

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70064h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:25	24	23:21	20	19:17	16	15:13	12	11:9	8	7:5	4	3:1	0
Default	0 0 0 0 0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0
Field	RESERVED	DISPLAY_FIFO_SELF_REFRESH_WATERMARK_HIGH_ORDER_PROGRAMMING	RESERVED_1	SPRITE_D_FIFO_WATERMARK_HIGH_ORDER	RESERVED_2	SPRITE_C_FIFO_WATERMARK_HIGH_ORDER	RESERVED_3	DISPLAY_PLANE_B_FIFO_WATERMARK_HIGH_ORDER	RESERVED_4	SPRITE_B_FIFO_WATERMARK_HIGH_ORDER	RESERVED_5	SPRITE_A_FIFO_WATERMARK_HIGH_ORDER	RESERVED_6	DISPLAY_PLANE_A_FIFO_WATERMARK_HIGH_ORDER

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK_HIGH_ORDER_PROGRAMMING:** This field is the high order bit for the SR WM pointer . Combined with the lower order 9-bit SR FIFO WM pointer, it forms a 10-bit SR FIFO WM pointer. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note [DevCL, DevCTG, DevCDV]: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.
23:21	0b RW	**RESERVED_1:** Reserved.
20	0b RW	**SPRITE_D_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM. Combined with lower order 8-bit Sprite D FIFO WM, it forms a 9-bit Sprite D FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
19:17	0b RW	**RESERVED_2:** Reserved.
16	0b RW	**SPRITE_C_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite C FIFO WM. Combined with lower order 8-bit Sprite C FIFO WM, it forms a 9-bit Sprite C FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

Bit Range	Default & Access	Field Name (ID): Description
15:13	0b RW	**RESERVED_3:** Reserved.
12	0b RW	**DISPLAY_PLANE_B_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Display B FIFO WM. Combined with lower order 8-bit Display B FIFO WM, it forms a 9-bit Display B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
11:9	0b RW	**RESERVED_4:** Reserved.
8	0b RW	**SPRITE_B_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite B FIFO WM. Combined with lower order 8-bit Sprite B FIFO WM, it forms a 9-bit Sprite B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:5	0b RW	**RESERVED_5:** MBZ
4	0b RW	**SPRITE_A_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite A FIFO WM. Combined with lower order 8-bit Sprite A FIFO WM, it forms a 9-bit Sprite A FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
3:1	0b RW	**RESERVED_6:** MBZ
0	0b RW	**DISPLAY_PLANE_A_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Display A FIFO WM. Combined with lower order 8-bit Display A FIFO WM, it forms a 9-bit Display A FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

14.11.189 DSPHOWM1—Offset 70068h

Display FIFO WM1 High Order

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70068h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:25	RESERVED
24	DISPLAY_FIFO_SELF_REFRESH_WATERMARK1_HIGH_ORDER_PROGRAMMING
23:21	RESERVED_1
20	SPRITE_D_FIFO_WATERMARK1_HIGH_ORDER
19:17	RESERVED_2
16	SPRITE_C_FIFO_WATERMARK1_HIGH_ORDER
15:13	RESERVED_3
12	DISPLAY_PLANE_B_FIFO_WATERMARK1_HIGH_ORDER
11:9	RESERVED_4
8	SPRITE_B_FIFO_WATERMARK1_HIGH_ORDER
7:5	RESERVED_5
4	SPRITE_A_FIFO_WATERMARK1_HIGH_ORDER
3:1	RESERVED_6
0	DISPLAY_PLANE_A_FIFO_WATERMARK1_HIGH_ORDER

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b RW	**RESERVED:** Reserved.
24	0b RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK1_HIGH_ORDER_PROGRAMMING:** This field is the high order bit for the SR WM1 pointer . Combined with the lower order 9-bit SR FIFO WM1 pointer, it forms a 10-bit SR FIFO WM1 pointer. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note [DevCL, DevCTG, DevCDV]: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.
23:21	0b RW	**RESERVED_1:** Reserved.
20	0b RW	**SPRITE_D_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM1. Combined with lower order 8-bit Sprite D FIFO WM1, it forms a 9-bit Sprite D FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
19:17	0b RW	**RESERVED_2:** Reserved.
16	0b RW	**SPRITE_C_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite C FIFO WM1. Combined with lower order 8-bit Sprite C FIFO WM1, it forms a 9-bit Sprite C FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

Bit Range	Default & Access	Field Name (ID): Description
15:13	0b RW	**RESERVED_3:** Reserved.
12	0b RW	**DISPLAY_PLANE_B_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Display B FIFO WM1. Combined with lower order 8-bit Display B FIFO WM1, it forms a 9-bit Display B FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
11:9	0b RW	**RESERVED_4:** Reserved.
8	0b RW	**SPRITE_B_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite B FIFO WM1. Combined with lower order 8-bit Sprite B FIFO WM1, it forms a 9-bit Sprite B FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:5	0b RW	**RESERVED_5:** MBZ
4	0b RW	**SPRITE_A_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite A FIFO WM1. Combined with lower order 8-bit Sprite A FIFO WM1, it forms a 9-bit Sprite A FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
3:1	0b RW	**RESERVED_6:** MBZ
0	0b RW	**DISPLAY_PLANE_A_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Display A FIFO WM1. Combined with lower order 8-bit Display A FIFO WM1, it forms a 9-bit Display A FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

14.11.190 FW4—Offset 70070h

Display FIFO Watermark1 Control 4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70070h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00040404h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Bits 31:24	Bits 23:16	Bits 15:14	Bits 13:8	Bits 7:0
RESERVED	DISPLAY_SPRITE_B_FIFO_WATERMARK1	RESERVED_1	CURSOR_A_FIFO_WATERMARK1	DISPLAY_SPRITE_A_FIFO_WATERMARK1

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** : MBZ
23:16	00000100b RW	**DISPLAY_SPRITE_B_FIFO_WATERMARK1:** [DevCDV] Number in 64Bs of space in FIFO above which the Display Sprite B Stream will generate request with status 2
15:14	0b RW	**RESERVED_1:** : MBZ
13:8	000100b RW	**CURSOR_A_FIFO_WATERMARK1:** DevCDV] Number in 64Bs of space in the Cursor A FIFO above which the Cursor A Stream will generate requests with status 2 to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:0	00000100b RW	**DISPLAY_SPRITE_A_FIFO_WATERMARK1:** DevCDV] Number in 64Bs of space in FIFO above which the Display Sprite A Stream will generate request with status 2 (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

14.11.191 FW5—Offset 70074h

Display FIFO Watermark1 Control 5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70074h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 04040404h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
DISPLAY_B_FIFO_WATERMARK1								DISPLAY_A_FIFO_WATERMARK1								RESERVED		CURSOR_B_FIFO_WATERMARK1						RESERVED_1		CURSORFIFO_SELF_REFRESH_WATERMARK1					

Bit Range	Default & Access	Field Name (ID): Description
31:24	00000100b RW	**DISPLAY_B_FIFO_WATERMARK1:** [DevCDV] Number in 64Bs of space in FIFO above which the Display B Stream will generate request with status 2
23:16	00000100b RW	**DISPLAY_A_FIFO_WATERMARK1:** [DevCDV] Number in 64Bs of space in FIFO above which the Display A Stream will generate request with status 2
15:14	0b RW	**RESERVED:** : MBZ
13:8	000100b RW	**CURSOR_B_FIFO_WATERMARK1:** DevCDV] Number in 64Bs of space in the Cursor B FIFO above which the Cursor B Stream will generate requests with status 2 to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:6	0b RW	**RESERVED_1:** : MBZ
5:0	000100b RW	**CURSORFIFO_SELF_REFRESH_WATERMARK1:** DevCDV] Number in 64Bs of space in FIFO above which the Display Cursor Stream will generate request with status 2 during memory SR (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

14.11.192 FW6—Offset 70078h

Display FIFO Watermark1 Control 6

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70078h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000078h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
											RESERVED																DISPLAY_FIFO_SELF_REFRESH_WATERMARK1				

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**RESERVED:** : MBZ
8:0	001111000b RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK1:** DevCDV] Number in 64Bs of space in FIFO above which the Display A/B Streamer will generate request with status 2 during max fifo mode (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

14.11.193 FW7—Offset 7007Ch

Display FIFO Watermark Control 7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7007Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 040F040Fh

31:24	23:16	15:8	7:0
0000 0100	0000 1111	0000 0100	0000 1111
DISPLAY_SPRITE_D_FIFO_WATERMARK1	DISPLAY_SPRITE_D_FIFO_WATERMARK	DISPLAY_SPRITE_C_FIFO_WATERMARK1	DISPLAY_SPRITE_C_FIFO_WATERMARK

Bit Range	Default & Access	Field Name (ID): Description
31:24	00000100b RW	**DISPLAY_SPRITE_D_FIFO_WATERMARK1:** [DevVLVP] Number in 64Bs of space in FIFO above which the Display Sprite D Stream will generate request with status 2
23:16	00001111b RW	**DISPLAY_SPRITE_D_FIFO_WATERMARK:** [DevVLVP] Number in 64Bs of space in FIFO above which the Display Sprite D Stream will generate request with status 2
15:8	00000100b RW	**DISPLAY_SPRITE_C_FIFO_WATERMARK1:** DevVLVP] Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2
7:0	00001111b RW	**DISPLAY_SPRITE_C_FIFO_WATERMARK:** DevVLVP] Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2

14.11.194 CURACNTR—Offset 70080h

Cursor A Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70080h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31:30	29:28	27	26	25:16	15	14:6	5	4	3	2:0
00	00	0	0	00 0000 0000	0	000 0000 00	0	0	0	000
RESERVED	PIPE_SELECT	POPUP_CURSOR_ENABLED	CURSOR_GAMMA_ENABLE	RESERVED_1	_180ROTATION	RESERVED_2	CURSOR_MODE_SELECT_BIT	RESERVED_3	RESERVED_4	CURSOR_MODE_SELECT

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** Write as zero.
29:28	0b RW	**PIPE_SELECT:** [DevBW, DevCL, DevCDV] A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned, when both display pipes are being used, it can be switched at any time; the hardware will synchronize the switch. 00 = HW cursor is attached to Display Pipe A. This is the default after reset. 01 = HW cursor is attached to Display Pipe B. 10 = Reserved for pipe C 11 = Reserved for pipe D [DevBLC] and [DevCTG] Reserved: Write as zero.
27	0b RW	**POPUP_CURSOR_ENABLED:** . This bit should be turned on when using Cursor A as a popup cursor. When in popup mode, hardware interprets the cursor base address as a physical address instead of a graphics address.0 = Cursor A is hi-res 1 = Cursor A is popup
26	0b RW	**CURSOR_GAMMA_ENABLE:** This bit only has an effect when using the cursor in a non-VGA mode. In VGA pop-up operation, the cursor data will always bypass the gamma (palette) unit. 0 = Cursor pixel data bypasses gamma correction or palette (default). 1 = Cursor pixel data is gamma to be corrected in the pipe.
25:16	0b RW	**RESERVED_1:** Write as zero
15	0b RW	**_180ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180 Rotation of 32 bit per pixel cursors
14:6	0b RW	**RESERVED_2:** Reserved.
5	0b RW	**CURSOR_MODE_SELECT_BIT:** See following table.
4	0b RW	**RESERVED_3:** Reserved.
3	0b RW	**RESERVED_4:** Reserved.
2:0	0b RW	**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

14.11.195 CURABASE—Offset 70084h

Cursor A Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70084h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bit 5	Bit 4	Bits 3:0
CURSOR_BASE_ADDRESS	RESERVED	DECRYPTION_REQUEST	POPUP_CURSOR_BASE_ADDRESS_MSBS

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**CURSOR_BASE_ADDRESS:** . This field specifies bits 31:6 of the graphics address of the base of the cursor. On [DevBW] and [DevCL] if the cursor is a popup, this field specifies bits 31:6 of the physical address of the base of the cursor, and bits 35:32 of the address are specified in the LSBs of this register. Popup cursor mode is selected within the CURACNTR register.The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	0b RW	**RESERVED:** MBZ
4	0b RW	**DECRYPTION_REQUEST:** This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0b RW	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

14.11.196 CURAPOS—Offset 70088h

Cursor A Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70088h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	CURSOR_Y_POSITION_SIGN_BIT
30:28	000	RESERVED
27:16	0000 0000 0000	CURSOR_Y_POSITION_MAGNITUDE_BITS_11
15	0	CURSOR_X_POSITION_SIGN_BIT
14:12	000	RESERVED_1
11:0	0000 0000 0000	CURSOR_X_POSITION_MAGNITUDE_BITS_11

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image.
30:28	0b RW	**RESERVED:** Write as zero.
27:16	0b RW	**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0: This register provides the magnitude bits of a signed 12-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0). For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image. Enabling the border in VGA (VGA Border Enable bit in the VGA Config register) includes the border in what is considered the active area . For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	0b RW	**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For use as a VGA Popup, the entire cursor must be positioned over the active area of the VGA image. Enabling the border in VGA (VGA Border Enable bit in the VGA Config register) includes the border in what is considered the active area .
14:12	0b RW	**RESERVED_1:** Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
11:0	0b RW	**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0: These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the end of the active video area in the unrotated orientation.

14.11.197 CURAPALET_0—Offset 70090h

Cursor A Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70090h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_OR_Y_VALUE								GREEN_OR_U_VALUE								BLUE_OR_V_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

14.11.198 CURAPALET_1—Offset 70094h

Cursor A Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70094h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_OR_Y_VALUE								GREEN_OR_U_VALUE								BLUE_OR_V_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The daa can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

14.11.199 CURAPALET_2—Offset 70098h

Cursor A Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70098h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RESERVED	RED_OR_Y_VALUE	GREEN_OR_U_VALUE	BLUE_OR_V_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

14.11.200 CURAPALET_3—Offset 7009Ch

Cursor A Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7009Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RESERVED	RED_OR_Y_VALUE	GREEN_OR_U_VALUE	BLUE_OR_V_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0b RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

14.11.201 CURALIVEBASE—Offset 700ACh

Cursor A Live Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bit 5	Bit 4	Bits 3:0
CURSOR_A_LIVE_BASE_ADDRESS	RESERVED	DECRYPTION_REQUEST	POPUP_CURSOR_BASE_ADDRESS_MSBS

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RO	**CURSOR_A_LIVE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for the plane.
5	0b RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**DECRYPTION_REQUEST:** This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0b RO	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

14.11.202 CURBCNTR—Offset 700C0h

Cursor B Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700C0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	31:30	29:28	27	26	25:16	15	14:6	5	4:3	2:0
Field	RESERVED	PIPE_SELECT	RESERVED_1	CURSOR_GAMMA_ENABLE	RESERVED_2	_180ROTATION	RESERVED_3	CURSOR_MODE_SELECT_BIT	RESERVED_4	CURSOR_MODE_SELECT

Bit Range	Default & Access	Field Name (ID): Description
31:30	0b RW	**RESERVED:** Write as zero.
29:28	0b RW	**PIPE_SELECT:** [DevBW, DevCL, DevCDV]: A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned, when both display pipes are being used, it can be switched at any time; the hardware will synchronize the switch. 00 = HW cursor is attached to Display Pipe A. This is the default after reset. 01 = HW cursor is attached to Display Pipe B. 10 = Reserved for to Display Pipe C. 11 = Reserved for to Display Pipe D. Reserved [DevBLC] and [DevCTG]: Write as zero.
27	0b RW	**RESERVED_1:** Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**CURSOR_GAMMA_ENABLE:** 0 = Cursor pixel data bypasses gamma correction (default). 1 = Cursor pixel data is gamma to be corrected.
25:16	0b RW	**RESERVED_2:** Reserved.
15	0b RW	**_180ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180 Rotation of 32 bit per pixel cursors
14:6	0b RW	**RESERVED_3:** Write as zero
5	0b RW	**CURSOR_MODE_SELECT_BIT:** See following table.
4:3	0b RW	**RESERVED_4:** reserved
2:0	0b RW	**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

14.11.203 CURBBASE—Offset 700C4h

Cursor B Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700C4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:6	CURSOR_BASE_ADDRESS
5	RESERVED
4	DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE
3:0	POPUP_CURSOR_BASE_ADDRESS_MSBS

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**CURSOR_BASE_ADDRESS:** This register specifies the graphics address of the entire cursor. It also acts as a trigger event to force the update of active registers on the next display event. The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	0b RW	**RESERVED:** MBZ
4	0b RW	**DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE:** This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0b RW	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

14.11.204 CURBPOS—Offset 700C8h

Cursor B Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700C8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31	30:28	27:16	15	14:12	11:0
Default	0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
Field	CURSOR_Y_POSITION_SIGN_BIT	RESERVED	CURSOR_Y_POSITION_MAGNITUDE_BITS_11	CURSOR_X_POSITION_SIGN_BIT	RESERVED_1	CURSOR_X_POSITION_MAGNITUDE_BITS_11

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen.
30:28	0b RW	**RESERVED:** Write as zero.
27:16	0b RW	**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0: This register provides the magnitude bits of a signed 13-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0) When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	0b RW	**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid.
14:12	0b RW	**RESERVED_1:** Write as zero.
11:0	0b RW	**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0: These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.

14.11.205 CURBPALET_0—Offset 700D0h

Cursor B Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_OR_Y								GREEN_OR_U_VALUE								BLUE_OR_V_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y:** RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

14.11.206 CURBPALET_1—Offset 700D4h

Cursor B Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_OR_Y								GREEN_OR_U_VALUE								BLUE_OR_V_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y:** RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

14.11.207 CURBPALET_2—Offset 700D8h

Cursor B Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700D8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_OR_Y								GREEN_OR_U_VALUE								BLUE_OR_V_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0b RW	**RED_OR_Y:** RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

14.11.208 CURBPALET_3—Offset 700DCh

Cursor B Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700DCh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED	RED_OR_Y	GREEN_OR_U_VALUE	BLUE_OR_V_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero.
23:16	0b RW	**RED_OR_Y:** RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0b RW	**GREEN_OR_U_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the U and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
7:0	0b RW	**BLUE_OR_V_VALUE:** RGB data is full range unsigned numbers. YUV data will be unsigned for the V and excess 128 notation for the YU values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

14.11.209 CURBLIVEBASE—Offset 700ECh

Cursor B Live Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 700ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: CURSOR_B_LIVE_BASE_ADDRESS (31:6), RESERVED (5), DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE (4), POPUP_CURSOR_BASE_ADDRESS_MSBS (3:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RO	**CURSOR_B_LIVE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Cursor B plane.
5	0b RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE:** This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0b RO	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

14.11.210 DSPAADDR—Offset 7017Ch

Display A Async flip Start Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7017Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:4	Bit 3	Bit 2	Bits 1:0
DISPLAY_A_START_ADDRESS_BITS	RESERVED	FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**DISPLAY_A_START_ADDRESS_BITS:** This register provides the start address of the display A plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . Write to this register triggers async flip. The async flip address is written into the Display A Base Address register 0x7019C

Bit Range	Default & Access	Field Name (ID): Description
11:4	0b RW	**RESERVED:** MBZ
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0b RW	**RESERVED_1:** MBZ

14.11.211 DSPACNTR—Offset 70180h

Display A Plane Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70180h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DISPLAY_PLANE_A_PRIMARY_A_ENABLE | DISPLAY_A_GAMMA_ENABLE | DISPLAY_A_SOURCE_PIXEL_FORMAT | PIPE_SELECT | KEY_WINDOW_ENABLE | KEY_ENABLE | PIXEL_MULTIPLY | RESERVED | RESERVED_1 | RESERVED_2 | _180DISPLAY_ROTATION | RESERVED_3 | RESERVED_4 | RESERVED_5 | TILED_SURFACE | RESERVED_6 | RESERVED_7 | S3D_FORCE_DISPLAY_A_BOTTOM

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DISPLAY_PLANE_A_PRIMARY_A_ENABLE:** When this bit is set, the primary plane will generate pixels for display. When set to zero, display plane A memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that display A is assigned. The display pipe must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 = Enable 0 = Disable
30	0b RW	**DISPLAY_A_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane s pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display A pixel data bypasses the display pipe gamma correction logic (default). 1 = Display A pixel data is gamma corrected in the display pipe gamma correction logic.
29:26	0b RW	**DISPLAY_A_SOURCE_PIXEL_FORMAT:** These bits should only be changed after the plane has been disabled. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Pixel format of 8-bit indexed uses the palette. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	0b RO	**PIPE_SELECT:** Plane A always ties to Pipe A. AccessType: Read Only Reserved

Bit Range	Default & Access	Field Name (ID): Description
23	0b RW	**KEY_WINDOW_ENABLE:** . This bit applies only to devices with a display plane C. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and it s Z-order should be programmed to be behind display A for this to be set to a one.0 = Source Key applies to entire display plane A 1 = Source Key applies to only pixels within the intersection between Display A and Display C [DevBLC] and [DevCTG]: Reserved
22	0b RW	**KEY_ENABLE:** . This bit enables source keying for display A. Source keying allows a plane that is behind (below) this plane to show through where the display A key matches the display A data. This function is overloaded to provide display C destination keying when combined with the key window enable bit. Setting this bit is not allowed when the display pixel format includes an alpha channel.0 = Source key is disabled 1 = Source key is enabled [DevBLC] and [DevCTG]: Reserved In destination keying, primary plane pixel will be made transparent when blending with sprite pixel as the destination if the primary src key matches with the primary pixel value.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the pixel multiply mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19	0b RW	**RESERVED:** Software must preserve the contents of this bit.
18	0b RW	**RESERVED_1:** Write as zero
17:16	0b RW	**RESERVED_2:** Software must preserve the contents of this bit.
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. [DevCL] Do not enable 180 rotation together with Frame Buffer Compression0 = No rotation 1 = 180 rotation
14	0b RW	**RESERVED_3:** [DevBW, DevCL, DevCDV]: [DevBLC] and [DevCTG] Display A Trickle Feed Enable: 0 = Trickle Feed Enabled - Display A data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display A data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled. [DevELK] Must always be programmed disabled
13	0b RW	**RESERVED_4:** [DevBW, DevCL, DevCDV]: [DevBLC] and [DevCTG] Display A Data Buffer Partitioning Control: 0 = Display A Data Buffer will encompass Sprite A buffer space when Sprite A is disabled. 1 = Display A Data Buffer will not use Sprite A buffer space when Sprite A is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	0b RW	**RESERVED_5:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0b RW	**TILED_SURFACE:** . This bit indicates that the display A surface data is in tiled memory. The tile pitch is specified in bytes in the DSPASTRIDE register. Only X tiling is supported for display surfaces.When this bit is set, it affects the hardware interpretation of the DSPATILEOFF, DSPALINOFF, and DSPASURF registers. 0 = Display A surface uses linear memory 1 = Display A surface uses X-tiled memory
9	0b RW	**RESERVED_6:** [DevBW, DevCL, DevCDV] Write as zero [DevBLC, DevCTG] Asynchronous Surface Address Update Enable: This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPASURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPASURF MMIO writes will update asynchronously
8:1	0b RW	**RESERVED_7:** Write as zero
0	0b RW	**S3D_FORCE_DISPLAY_A_BOTTOM:** This bit will force the display A plane to be on the bottom of any sprite planes in the Z order. 0 = Display A Z-order is determined by the other control bits in pipe A 1 = Display A is forced to be on the bottom of any sprite planes in Z-order in pipe A

14.11.212 DSPALINOFF—Offset 70184h

Display A Linear Offset Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70184h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DISPLAY_A_OFFSET

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**DISPLAY_A_OFFSET:** This register provides the panning offset into the display A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

14.11.213 DSPASTRIDE—Offset 70188h

Display A Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70188h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DISPLAY_A_STRIDE																										RSVD0					

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**DISPLAY_A_STRIDE:** This is the stride for display A in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. This value is used to determine the line to line increment for the display. This register is updated either through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes. [DevBW, DevCL, DevCDV] The display stride must be power of 2 when doing Asynch Flips. [DevBW, DevCL, DevCDV] The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.
5:0	0b RO	**RSVD0:** Reserved

14.11.214 DSPAKEYVAL—Offset 70194h

Sprite Color Key Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70194h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_KEY_VALUE								GREEN_KEY_VALUE								BLUE_KEY_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	0b RW	**RED_KEY_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

14.11.215 DSPAKEYMSK—Offset 70198h

Sprite Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70198h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED | RED_MASK_VALUE | GREEN_MASK_VALUE | BLUE_MASK_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	0b RW	**RED_MASK_VALUE:** Specifies the color key mask for the sprite red/Cr channel.
15:8	0b RW	**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green/Y channel.
7:0	0b RW	**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue/Cb channel.

14.11.216 DSPASURF—Offset 7019Ch

Display A Surface Base Address Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7019Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DISPLAY_A_SURFACE_BASE_ADDRESS | RESERVED | FLIP_SOURCE | DECRYPTION_REQUEST | RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**DISPLAY_A_SURFACE_BASE_ADDRESS:** . This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPATILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPALINOFF register.This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED:** Reserved.
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0b RW	**RESERVED_1:** MBZ

14.11.217 DSPATILEOFF—Offset 701A4h

Display A Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 701A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				PLANE_START_Y_POSITION												RESERVED_1				PLANE_START_X_POSITION											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation. [DevBW, DevCL, DevCDV] When display stride is 16KB and doing Asynch Flips, do not program the offset to give pans of 7680 to 8191 bytes.

14.11.218 DSPASURFLIVE—Offset 701ACh

Display A Live Surface Base Address Register [DevCTG-B, DevCDV]

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 701ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:0: DISPLAY_A_LIVE_SURFACE_BASE_ADDRESS

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**DISPLAY_A_LIVE_SURFACE_BASE_ADDRESS:** . This gives the live value of the surface base address as being currently used for the plane.

14.11.219 CBR1—Offset 70400h

Chicken Bit Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70400h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	PND_DEADLINE_CALCULATION_DISABLE
30	S0IX_PWM_BACKLIGHT_CLOCK_MUX_SELECT
29	GM_DEGLITCH_EMUL_MODE
28:26	VGA_OOO_QUEUE_DEPTH
25	HPD_PORT_D_49_95MS_TIME_FLAG_BYPASS
24	HPD_PORT_C_49_95MS_TIME_FLAG_BYPASS
23	HPD_PORT_B_49_95MS_TIME_FLAG_BYPASS
22	RESERVED
21	ELPIN_409_SELECT
20	HPD_INPUT_ENABLE
19	CR12_WRITE_COUNTER_RESET
18	RESERVED_2
17	MONITOR_DETECTION
16	INVERT_DPO_FIELD
15	RESERVED_3
14	HPD_TEST_MODE
13	SDVOC_SELECT
12	SDVOB_SELECT
11	VGA_STALL
10	RESERVED_4
9	PIXEL_SIZE
8	IMMEDIATE_ASYNCHRONOUS_FLIPS
7	PIPE_B_FRAME_START_POSITION
6	PIPE_B_PALETTE_WRITE_ENABLE
5	PIPE_A_PALETTE_WRITE_ENABLE
4	VRD_FONT_FIFO_REQUEST_DELAY_ENABLE
3	PIPE_A_FRAME_START_POSITION
2	RESERVED_6
1	PLLB_SAFE_SHUTDOWN_OVERRIDE
0	PLLA_SAFE_SHUTDOWN_OVERRIDE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PND_DEADLINE_CALCULATION_DISABLE:** 1 = PND deadline scheme is disabled. Latency deadline calculation is based on the pre-programmed watermark level and the 2-bit FIFO status region. 0 = PND deadline scheme is enabled. Latency deadline calculation is based on actual FIFO level
30	0b RW	**S0IX_PWM_BACKLIGHT_CLOCK_MUX_SELECT:** This bit is used to select the new pwm backlight control during s0ix mode 0 = select s0ix pwm backlight control based on 25 MHz oscillator clock (default) 1 = select normal pwm backlight control based on hrawclk Programming note: This bit is programmed to select either 200MHz refclk from CCK or 25MHz refclk from XTAL. This bit cannot be changed on the fly.
29	0b RW	**GM_DEGLITCH_EMUL_MODE:** GM deglitch emulation mode
28:26	0b RW	**VGA_OOO_QUEUE_DEPTH:** 0xx = Disable out-of-order stall logic for VGA 100 = Enable out-of-order VGA stall depth of 64 101 = Enable out-of-order VGA stall depth of 48 110 = Enable out-of-order VGA stall depth of 32 111 = Enable out-of-order VGA stall depth of 16
25	0b RW	**HPD_PORT_D_49_95MS_TIME_FLAG_BYPASS:** bypass 49_95ms time flag in Port D Not Used
24	0b RW	**HPD_PORT_C_49_95MS_TIME_FLAG_BYPASS:** bypass 49_95ms time flag in Port C Programming note: VLV uses HPD deglitch time as 50us. For glitches between 50us and 250us during hot plug event, driver may see multiple hpd interrupts, driver shall either service them or ignore them.
23	0b RW	**HPD_PORT_B_49_95MS_TIME_FLAG_BYPASS:** bypass 49_95ms time flag in Port B Programming note: VLV uses HPD deglitch time as 50us. For glitches between 50us and 250us during hot plug event, driver may see multiple hpd interrupts, driver shall either service them or ignore them.
22	0b RW	**RESERVED:** Reserved.
21	0b RW	**ELPIN_409_SELECT:** This bit is used to select one of the elpin 409 bug fixes 0 = vrd_ci_rreq 1 = count comparator
20	0b RW	**HPD_INPUT_PIN_DISABLE (HPD_INPUT_ENABLE):** [DevVLVP]: this bit is used to disable HPD detection in the Display core from using HPD input pin pin 0 = HPD Input pin is enabled to detect HPD detection by Display core (default) 1 = HPD input is pin is disabled to detect HPD detection by Display core
19	0b RW	**CR12_WRITE_COUNTER_RESET:** 0 = Disable CR12 write counter reset 1 = Enable CR12 write counter reset
18	0b RW	**RESERVED_2:** Reserved.
17	0b RW	**MONITOR_DETECTION:** This bit is used to test the monitor detection. Do not program unless directed.
16	0b RW	**INVERT_DPO_FIELD:** Invert DPO interlaced field output. This bit is used to invert the field sense input to the planes from DPO.
15	0b RW	**RESERVED_3:** Reserved.
14	0b RW	**HPD_TEST_MODE:** load programmable value for filter and long pulse value of HPD register 0x70408.
13	0b RW	**SDVOC_SELECT:** sdvoc deglitch logic output select
12	0b RW	**SDVOB_SELECT:** sdvob deglitch logic output select

Bit Range	Default & Access	Field Name (ID): Description
11	0b RW	**VGA_STALL:** Stall native mode VGA when frequency is over 50 MHz. This bit is only used during VGA native mode.
10	0b RW	**RESERVED_4:** to prevent async flip failures.
9	0b RW	**PIXEL_SIZE:** This bit changes the VGA pixel width and height calculations.
8	0b RW	**IMMEDIATE_ASYNCHRONOUS_FLIPS:** This bit causes asynchronous flips to complete immediately upon the start of the vertical blank period. When enabling this feature, frame start should also be moved to the end of the vertical blank period by setting the frame start position bit.
7	0b RW	**PIPE_B_FRAME_START_POSITION:** This bit changes the position of frame start on pipe B. This feature is used in conjunction with the immediate asynchronous flips bit to enable fast asynchronous flips during vertical blanking. 0 = frame start occurs at start of the vertical blank period 1 = frame start occurs at end of the vertical blank period Default: 1, causing frame start to occur at the end of vertical blank
6	0b RW	**PIPE_B_PALETTE_WRITE_ENABLE:** Disables anti-collision logic in the palette during non-blanking periods on pipe B.
5	0b RW	**PIPE_A_PALETTE_WRITE_ENABLE:** Disables anti-collision logic in the palette during non-blanking periods on pipe A
4	0b RW	**VRD_FONT_FIFO_REQUEST_DELAY_ENABLE:** This bit enable VRD font read request delay in VGA mode
3	0b RW	**PIPE_A_FRAME_START_POSITION:** This bit changes the position of frame start on pipe A. This feature is used in conjunction with the immediate asynchronous flips bit to enable fast asynchronous flips during vertical blanking. 0 = frame start occurs at start of the vertical blank period 1 = frame start occurs at end of the vertical blank period Default: 1, causing frame start to occur at the end of vertical blank
2	0b RW	**RESERVED_6:** Reserved.
1	0b RW	**PLLB_SAFE_SHUTDOWN_OVERRIDE:** This bit disables the dependency for pipe B to be disabled before the PLL is shut down
0	0b RW	**PLLA_SAFE_SHUTDOWN_OVERRIDE:** This bit disables the dependency for pipe A to be disabled before the PLL is shut down

14.11.220 CBR2—Offset 70404h

Chicken2 Bit Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70404h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	DPRDDB_VGAENRST_DIS
30:28	000	RESERVED
27	0	DCN_447625
26	0	DPIOMB0UNIT
25	0	DPSEL_OVERRIDE
24	0	DITHERING_ENHANCE_DISABLE
23	0	EDGE
22	0	DPRAUDM_EARLY_HDE_DISABLE
21	0	DPLRUNIT
20	0	DPRAUDM_CKGATE_PKTCNTRL_IDLE_DIS
19	0	DPR_DPIO_PORTOFF_NOT_HBLK_CHICKEN
18	0	MMIO_WRITE_EVENT
17	0	DBLATEN_ARMED_CURA_B
16	0	HPD_INTR_FIX
15	0	RESERVED_1
14	0	PORT_B_LANES_READY_IGNORE
13	0	PORT_C_LANES_READY_IGNORE
12	0	DPLLS_OK_IGNORE
11	0	DPR_DPS_NOA_SCALEEN
10	0	DPR_VS_AFLIPTOTAL_CHICKEN
9	0	DPR_VS_BYTEEN_CHICKEN
8	0	DPR_VS_AFLIPADDR_CHICKEN
7:6	00	DPRDDB_SYNC_SELECT
5	0	DDBMUNIT
4	0	HDCPUNIT
3:2	00	DPRVGA_DPBSTALL_UL_THRESHOLD
1	0	DPRAUDM_SAMPLE_PRESENT_DISABLE
0	0	RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DPRDDB_VGAENRST_DIS:** Enable rise and fall detection of DPRvgadis for DDB reset (dprddb_vgaenrst_dis)
30:28	0b RW	**RESERVED:** Reserved.
27	0b RW	**DCN_447625:** : - x8 support for hybrid gfx, Kwasi requested (dpr_dpio_x8_conc_sel)
26	0b RW	**DPIOMB0UNIT:** ignoring EDP logic when enabling Lanes by the dptc_otxoenb [DevVLVP]: Reserved
25	0b RW	**DPSEL_OVERRIDE:** when this chicken bit is set override the selects to 0 (dpsel_override) timeslice_sync_rst_b = DPRVGAdis | mrchicken2_Q[25]
24	0b RW	**DITHERING_ENHANCE_DISABLE:** Anh need for dithering enhace (dithering_enhance_disable)
23	0b RW	**EDGE:** edgeA/Bvblank, edgeDPSA/Bvblank, curA/Bedgevblank,
22	0b RW	**DPRAUDM_EARLY_HDE_DISABLE:** Chicken bit to Audio unit to disable early RAM FIFO read in 2-channel mode (DPRAUDM_early_hde_disable)
21	0b RW	**DPLRUNIT:** Selects cdclk for pwm logic, pwm logic, uses hrawclk by default (select cdclk in scan mode or by setting a chicken bit) [DevVLVP]: Reserved
20	0b RW	**DPRAUDM_CKGATE_PKTCNTRL_IDLE_DIS:** Chicken bit to disable audclk gating when pktcontrol FSM is idle (DPRAUDM_ckgate_pktcntrl_idle_dis)
19	0b RW	**DPR_DPIO_PORTOFF_NOT_HBLK_CHICKEN:** This bit is needed to qualify the port off with hblank to take care of fragmented audio packet sent off. When chicken bit is enabled, the port off is dependent upon state of hblank, else the legacy behavior rules (dpr_dpio_portoff_not_hblk_chicken)
18	0b RW	**MMIO_WRITE_EVENT:** 0: mmio_write_event = RMDecPipeSLC_pre 1: mmio_write_event = 1'b0
17	0b RW	**DBLATEN_ARMED_CURA_B:** Dblaten_armed_curA/B

Bit Range	Default & Access	Field Name (ID): Description
16	0b RW	**HPD_INTR_FIX:** Freeses hpdb_intr_fix, hpdc_intr_fix, hpdd_intr_fix
15	0b RW	**RESERVED_1:** Reserved.
14	0b RW	**PORT_B_LANES_READY_IGNORE:** 1: Lanes considered as ready for normal operation 0: usual operation: Lanes readiness indications arrived from DPIO SEG outputs [DevVLVP]: Reserved
13	0b RW	**PORT_C_LANES_READY_IGNORE:** 1: Lanes considered as ready for normal operation 0: usual operation: Lanes readiness indications arrived from DPIO SEG outputs [DevVLVP]: Reserved
12	0b RW	**DPLLS_OK_IGNORE:** 1: Both mPHY DPLLs considered as OK ('1'). Lanes can be enabled. 0: usual operation: DPLL readiness indications arrived from DPIO SEG outputs [DevVLVP]: Reserved
11	0b RW	**DPR_DPS_NOA_SCALEEN:** This bit is to enable viewing critical control signals that were added as a result of Cantiga B0 Overlay changes. Default = 0. (dpr_dps_noa_scaleen) 0: Non-scaling signals are sent to NOA bus 1: Scaling signals are sent to the NOA bus
10	0b RW	**DPR_VS_AFLIPTOTAL_CHICKEN:** This chicken bit bypasses the current logic used for calculating the number of requests to make for an asynchronous flip. It will be helpful because the current logic is very difficult to validate. (dpr_vs_afliptotal_chicken)
9	0b RW	**DPR_VS_BYTEEN_CHICKEN:** This chicken bit bypasses the current logic used for selecting the proper byte enables. It is intended to address byte enables during asynchronous flips, but it was easier to bypass the entire byte-enable circuit instead. HSD bug #1932963. (dpr_vs_byteen_chicken)
8	0b RW	**DPR_VS_AFLIPADDR_CHICKEN:** This chicken bit bypasses the current logic used for selecting the starting fetch address of an asynchronous flip. HSD bug #1932964. (dpr_vs_aflipaddr_chicken)
7:6	0b RW	**DPRDDB_SYNC_SELECT:** When set vsync reset is asserted and when clear no reset is asserted. (dprddb_novsyncreset) This selects between VRVSYNC and hi-res VSYCN when set with dprvrd_novsyncreset also set sync_select novsyncreset. (dprddb_sync_select) X0 = No Vsync reset 01 = VGA vsync or hi-res between Nat and UL mode 11 = VGA vsync reset in both UL and native
5	0b RW	**DDBMUNIT:** C0 ECO1 chicken bit defaulted to fix enable
4	0b RW	**HDCPUNIT:** EGLK A5 ECO1 Fix. Read Data Fix For RMBus Protocol. vsmunit: Lock Up Issue.
3:2	0b RW	**DPRVGA_DPBSTALL_UL_THRESHOLD:** VGATEST2 issue fix, Stall throttling done during horiz_blank and UL mode is asserted. (DPRVGA_dpbstall_ul_threshold). 01: DPB to VGA stall during UL mode
1	0b RW	**DPRAUDM_SAMPLE_PRESENT_DISABLE:** When set this bit will disable the sample present bits being set in layout 1 mode of Audio. Default is to enable sample present on Audio. (DPRAUDM_sample_present_disable) vsmunit: FBC/SR Power Fix
0	0b RW	**RESERVED_2:** [DevVLVP] MBZ. This bit si the same as bit 31 in 70450h rega_loadcount_crtdetect

14.11.221 CCBR—Offset 70408h

ChickenCount Bit Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70408h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HPD_AND_CRT_DETECT_TEST_MODES

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**HPD_AND_CRT_DETECT_TEST_MODES:** HPD and CRT detect test mode

14.11.222 CBR3—Offset 7040Ch

Chicken3 Bit Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7040Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:25	24:18	17	16	15	14	13	12	11:10	9	8	7:6	5:4	3:2	1:0
Default	0 0 0 0 0 0 0	0 0 0 0 0 0 0	0	0	0	0	0	0	0 0	0	0	0 0	0 0	0 0	0 0
Field	DPTPIPEB_CHICKEN_BITS	DPTPIPEA_CHICKEN_BITS	PIPEBCLKGATEEN	PIPEACLKGATEEN	MENC16	MENC_NEVERENDING	FREQUENCY_WINDOWING	GOOD_SYNC	SELECT_CDCLK_COUNT_FOR_DEGLITCH	CHICKEN_UNGATECLK	CHICKEN_MULTIEDGEERROR	READBACK	AUXD_GMBUS_CONNECTION	AUXC_GMBUS_CONNECTION	AUXB_GMBUS_CONNECTION

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b RW	**DPTPIPEB_CHICKEN_BITS:** not used [DevVLVP]: Reserved
24:18	0b RW	**DPTPIPEA_CHICKEN_BITS:** not used [DevVLVP]: Reserved
17	0b RW	**PIPEBCLKGATEEN:** Enables reg_pipeBclkgateen_cd reg_pipeBclkgateen_db [DevVLVP]: Reserved
16	0b RW	**PIPEACLKGATEEN:** Enables reg_pipeAclkgateen_cd reg_pipeAclkgateen_da [DevVLVP]: Reserved
15	0b RW	**MENC16:** Chicken to cause MENC to output just 16 manchester 0s for sync (otherwise 26) [DevVLVP]: Reserved
14	0b RW	**MENC_NEVERENDING:** Chicken to cause MENC to output neverending sync 0s for electrical testing [DevVLVP]: Reserved
13	0b RW	**FREQUENCY_WINDOWING:** Chicken to tighten the frequency windowing [DevVLVP]: Reserved
12	0b RW	**GOOD_SYNC:** Chicken to check for only 8 good sync 0s instead of 12 [DevVLVP]: Reserved
11:10	0b RW	**SELECT_CDCLK_COUNT_FOR_DEGLITCH:** 11 = 1/16 2X bit clock divider value - 31.125ns 10 = 1/8 2X bit clock divider value - 62.5ns 01 = 1/4 2X bit clock divider value - 125ns 00 = 25 - GMBUS type 50ns at 500MHz cdclk [DevVLVP]: Reserved
9	0b RW	**CHICKEN_UNGATECLK:** 1 = Ungate clock 0 = Automatic clock gating [DevVLVP]: Reserved
8	0b RW	**CHICKEN_MULTIEDGEERROR:** 1 = Multiple edges in window is an eror 0 = Multiple edges in window is okay [DevVLVP]: Reserved
7:6	0b RW	**READBACK:** 11 = Readback of bit clock divide field gives the error type 01 = Readback gives the recovered clock frequency 00 = Readback gives the programmed clock frequency [DevVLVP]: Reserved
5:4	0b RW	**AUXD_GMBUS_CONNECTION:** Selectes gmbus connection for AUXD [DevVLVP]: Reserved

Bit Range	Default & Access	Field Name (ID): Description
3:2	0b RW	**AUXC_GMBUS_CONNECTION:** Selectes gmbus connection for AUXC [DevVLVP]: Reserved
1:0	0b RW	**AUXB_GMBUS_CONNECTION:** Selectes gmbus connection for AUXB [DevVLVP]: Reserved

14.11.223 SWF00—Offset 70410h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70410h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.224 SWF01—Offset 70414h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70414h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.225 SWF02—Offset 70418h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70418h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.226 SWF03—Offset 7041Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7041Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.227 SWF04—Offset 70420h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70420h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.228 SWF05—Offset 70424h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70424h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.229 SWF06—Offset 70428h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70428h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.230 SWF07—Offset 7042Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7042Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.231 SWF08—Offset 70430h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70430h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.232 SWF09—Offset 70434h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70434h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.233 SWF0A—Offset 70438h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70438h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.234 SWF0B—Offset 7043Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7043Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.235 SWF0C—Offset 70440h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70440h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.236 SWF0D—Offset 70444h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70444h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.237 SWF0E—Offset 70448h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70448h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.238 SWF0F—Offset 7044Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7044Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.239 CBR4—Offset 70450h

Display Chicken Bits 4 ;

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 70450h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	REGA_LOADCOUNT_CRTDETECT
30	0	HPD_TEST_MODE
29	0	RESERVED
28	0	FLIP_MSA_VERTICAL_TOTAL_IN_INTERLACE_MODE
27	0	DRPO_DPT_FIELD_INVERT
26	0	CRC_DOUBLEBUFFER_DISABLE
25	0	HPD_GLITCH_REMOVAL_COUNT_VALUE_SELECTION
24:21	0 0 0 0	SDVO_RX_FIX
20	0	LVDS_LEGACY_WRITE_PROTECTION
19	0	PCH_FIELD_ID_FIX
18:16	0 0 0	RESERVED_1
15:8	0 0 0 0 0 0 0 0	DAC_DOUBLE_LINEARITY_REGISTER
7:6	0 0	DAC_DBL_LIN_RED_CHANNEL_COUNTER_SOURCE_SELECT
5:4	0 0	DAC_DBL_LIN_BLUE_CHANNEL_COUNTER_SOURCE_SELECT
3:2	0 0	DAC_DBL_LIN_GREEN_CHANNEL_COUNTER_SOURCE_SELECT
1	0	DAC_DBL_LIN_COUNTER_2_OVERRIDE_SELECT
0	0	DAC_DBL_LIN_RGB_DAC_DFT_MODE_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**REGA_LOADCOUNT_CRTDETECT:** Project: All Format: Load initial value to crtdetect counter
30	0b RW	**HPD_TEST_MODE:** Project: All Default Value: 0b Load programmable value for filter and long pulse value of HPD Value Name Description Project 0b Short Pulse Short Pulse All 1b Long Pulse Long Pulse All
29	0b RW	**RESERVED:** Project: All Format: PBC

Bit Range	Default & Access	Field Name (ID): Description
28	0b RW	**FLIP_MSA_VERTICAL_TOTAL_IN_INTERLACE_MODE:** Project: All Format: Set to 1 to flip MSA vtotal
27	0b RW	**DRPO_DPT_FIELD_INVERT:** Project: All Format: Invert interlaced field ID output from dptunit.
26	0b RW	**CRC_DOUBLEBUFFER_DISABLE:** Project: All Format: Disable doublebuffering on CRCs so enable/disable and source select will happen immediately.
25	0b RW	**HPD_GLITCH_REMOVAL_COUNT_VALUE_SELECTION:** Project: All Default Value: 0b Value Name Description Project 0b 500us 500us glitch removal All 1b 50us 50us glitch removal All
24:21	0b RW	**SDVO_RX_FIX:** Project: All Format: Program SDVO receiver fix values [DevVLVP]: Reserved
20	0b RW	**LVDS_LEGACY_WRITE_PROTECTION:** Project: All Format: [DevVLVP]: Reserved
19	0b RW	**PCH_FIELD_ID_FIX:** Project: All Format: 1: CPU and PCH field IDs are independent 0: CPU field ID is tied to PCH field ID [DevVLVP]: Reserved
18:16	0b RW	**RESERVED_1:** Project: All Format: MBZ
15:8	0b RW	**DAC_DOUBLE_LINEARITY_REGISTER:** Project: All Format: Project: DevIBX-B Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All
7:6	0b RW	**DAC_DBL_LIN_RED_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: 00b DefaultVaueDesc BitFieldDesc Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of Counter 1 All 11b Counter 2 Counter 2 All Programming Notes Notes Errata Description Project # Desc All
5:4	0b RW	**DAC_DBL_LIN_BLUE_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: 00b Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All
3:2	0b RW	**DAC_DBL_LIN_GREEN_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: 00b Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**DAC_DBL_LIN_COUNTER_2_OVERRIDE_SELECT:** Project: DevIBX-B Default Value: 0b Value Name Description Project 0b No override No override, count value is from counter 2 All 1b Override Override mode enabled, count value is from 8-bit override value All
0	0b RW	**DAC_DBL_LIN_RGB_DAC_DFT_MODE_ENABLE:** Project: DevIBX-B Default Value: 0b Value Name Description Project 0b Disable Normal operation, no test mode enabled All 1b Enable RGB DAC DFT mode enabled All

14.11.240 PIPEB_DSL—Offset 71000h

Display Scan Line

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	CURRENT_FIELD
30:13	RESERVED
12:0	PIPE_B_DISPLAY_LINE_COUNTER

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**CURRENT_FIELD:** [DevBLC, DevCTG, DevCDV] Provides read back of the current field being displayed on display pipe B. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode: 1 = first field (odd field) 0 = second field (even field) [DevBW and DevCL] Reserved: Read only.
30:13	0b RO	**RESERVED:** Read only.
12:0	0b RO	**PIPE_B_DISPLAY_LINE_COUNTER:** This register enables the read back of the display vertical line counter . The display line values are from the pipe B timing generator. They change at the leading edge of HSYNC, and can be safely read at any time.

14.11.241 PIPEB_SLC—Offset 71004h

Pipe B Display Scan Line Range Compare Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30:29	28:16	15:13	12:0
0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0
INCLUSIVE_EXCLUSIVE	RESERVED	START_SCAN_LINE_NUMBER	RESERVED_1	END_SCAN_LINE_NUMBER

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**INCLUSIVE_EXCLUSIVE:** 1 = Inclusive Within Range, 0 = Exclusive Out of Range
30:29	0b RW	**RESERVED:** Read only.
28:16	0b RW	**START_SCAN_LINE_NUMBER:** [DevBLC, DevCTG, DevCDV] This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1]. [DevBW] and [DevCL] End Scan Line Number: This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].
15:13	0b RW	**RESERVED_1:** Read only.
12:0	0b RW	**END_SCAN_LINE_NUMBER:** [DevBLC, DevCTG, DevCDV] This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1]. [DevBW] and [DevCL] Start Scan Line Number: This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].

14.11.242 PIPEBCONF—Offset 71008h

Pipe B Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

PIPE_B_ENABLE
PIPE_STATE
RESERVED
FRAME_START_DELAY
DISPLAY_PORT_AUDIO_ONLY_MODE
FORCE_BORDER
PIPE_B_GAMMA_UNIT_MODE
INTERLACED_MODE
MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_B
DISPLAY_OVERLAY_PLANES_OFF
CURSOR_PLANES_OFF
REFRESH_RATE_CXSR_MODE_ASSOCIATION
COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_B
DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP
COLOR_RANGE_SELECT
S3D_SPRITE_ORDER
S3D_SPRITE_INTERLEAVING_FORMAT
RESERVED_1
BITS_PER_COLOR
DITHERING_ENABLE
DITHERING_TYPE
DDA_RESET_TEST_MODE
RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PIPE_B_ENABLE:** Setting this bit to the value of one, turns on pipe B. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at its lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. Disabling the Pipe and changing the timing registers and re-enabling the pipe before the next VBLANK will cause the mode change to occur at the end of the current frame. This requires no wait on the software s part. On the other hand, if this is the disabling of the pipe, that does require a software wait for VBLANK to occur. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption is at it s lowest state. 1 = Enable 0 = Disable
30	0b RO	**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled 1 = Enabled AccessType: Read Only

Bit Range	Default & Access	Field Name (ID): Description
29	0b RW	**RESERVED:** Write as zero.
28:27	0b RW	**FRAME_START_DELAY:** Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. This would be set to 00 for normal operation. 00 = Frame Start occurs on the first HBLANK after the start of VBLANK 01 = Frame Start occurs on the second HBLANK after the start of VBLANK 10 = Frame Start occurs on the third HBLANK after the start of VBLANK 11 = Frame Start occurs on the forth HBLANK after the start of VBLANK
26	0b RW	**DISPLAY_PORT_AUDIO_ONLY_MODE:** [DevVLVP] Setting this bit to 1 indicates the DisplayPort will output audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	0b RW	**FORCE_BORDER:** : (TEST MODE)0 = Normal Operation 1 = Color information is ignored and border color is substituted during active region
24	0b RW	**PIPE_B_GAMMA_UNIT_MODE:** . This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. VGA and indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay and sprite are unaffected by this bit.0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode
23:21	0b RW	**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift (2x) 101 = Interlaced using vertical sync shift. Backup option to setting 110. (2x) 110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used. Note: VGA display modes, sDVO line stall, and Panel fitting do not work while in interlaced modes Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	0b RW	**MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_B:** .0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only
19	0b RW	**DISPLAY_OVERLAY_PLANES_OFF:** . This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK.0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
18	0b RW	**CURSOR_PLANES_OFF:** . This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.

Bit Range	Default & Access	Field Name (ID): Description
17:16	0b RW	**REFRESH_RATE_CXSR_MODE_ASSOCIATION:** These bits select how refresh rates are tied to CxSR on pipe B. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated dispay panels that support corresponding mode. 00 Default no dynamic refresh rate change enabled. Software control only. 01 Progressive-to-progressive refresh rate change enabled and tied to CxSR. Pixel clock values set in FPB0/FPB1 settings in the DPLLB control register and FPB0/FPB1 divider registers. 10 Progressive-to-interlaced refresh rate change enabled and tied to CxSR. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 Reserved
15	0b RW	**COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_B:** 1 = Color Correction Coefficients are enabled to perform color correction 0 = Color Correction Coefficients are disabled
14	0b RW	**DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP:** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 Normal progressive refresh rate (default) 1 Low Power progressive refresh rate
13	0b RW	**COLOR_RANGE_SELECT:** [DevVLVP]: This bit is used to select the color range of RBG outputs. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
12	0b RW	**S3D_SPRITE_ORDER:** This bit controls the blending order of the sprite planes for S3D support: 0 = Sprite C first. The first line or pixel comes from Sprite C (default) 1 = Sprite D first. The first line or pixel comes from Sprite D
11:10	0b RW	**S3D_SPRITE_INTERLEAVING_FORMAT:** These bits control the Sprite C/D interleaving format in S3D mode 00 = No interleaving 01 = Line interleaving 10 = Pixel interleaving 11 = Reserved
9:8	0b RW	**RESERVED_1:** [DevCDV, DevVLVP] MBZ Scrambling enable [DevCTG]: This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 = Scrambling disabled (Default) 01 = Scrambling enabled, no SR after initialization at loop 2 of training 10 - RESERVED 11 = Scrambling and SR enabled. Scrambling is reset every 512 BS symbols.
7:5	0b RW	**BITS_PER_COLOR:** [DevCTG, DevCDV, DevVLVP]: This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to DP Frequency Programming in DPLL section of Bspec. 000 = 8 bits per color (Default) 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED
4	0b RW	**DITHERING_ENABLE:** [DevCTG, DevCDV]: This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled (Default) 1 Dithering enabled Programming Note: Dithering should only be enabled for 8bpc or 6bpc.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0b RW	**DITHERING_TYPE:** [DevCTG, DevCDV]: This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 - Spatial only (default) 01- Spatio-Temporal 1 10- Spatio-Temporal 2 (testmode) 11- Temporal only (testmode)
1	0b RW	**DDA_RESET_TEST_MODE:** [DevCTG, DevCDV]: 0 Do not reset DDA 1 Reset DDA every 8th display frame
0	0b RW	**RESERVED_2:** Write as zero

14.11.243 PIPEBGCMAXRED—Offset 71010h

Pipe B Gamma Correction Max Red

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71010h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | MAX_RED_GAMMA_CORRECTION_POINT

Bit Range	Default & Access	Field Name (ID): Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	100000000 00000000b RW	**MAX_RED_GAMMA_CORRECTION_POINT:** . 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

14.11.244 PIPEBGCMAXGREEN—Offset 71014h

Pipe B Gamma Correction Max Green

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71014h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (bits 31:17) | MAX_GREEN_GAMMA_CORRECTION_POINT (bits 16:0)

Bit Range	Default & Access	Field Name (ID): Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	100000000 00000000b RW	**MAX_GREEN_GAMMA_CORRECTION_POINT:** . 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

14.11.245 PIPEBGCMAXBLUE—Offset 71018h

Pipe B Gamma Correction Max Blue

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71018h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED (31:17) | MAX_BLUE_GAMMA_CORRECTION_POINT (16:0)

Bit Range	Default & Access	Field Name (ID): Description
31:17	0b RW	**RESERVED:** Reserved.
16:0	10000000000000000b RW	**MAX_BLUE_GAMMA_CORRECTION_POINT:** . 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

14.11.246 PIPEBSTAT—Offset 71024h

Pipe B Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71024h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	PIPE_B_UNDERFLOW_STATUS
	0	SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE
	0	CRC_ERROR_ENABLE
28	0	CRC_DONE_ENABLE
	0	PERFORMANCE_COUNTER2_INTERRUPT_ENABLE
	0	PLANE_B_FLIP_DONE_INTERRUPT_ENABLE
	0	VERTICAL_SYNC_INTERRUPT_ENABLE
24	0	DISPLAY_LINE_COMPARE_ENABLE
	0	BLM_EVENT_ENABLE
	0	SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE
	0	ODD_FIELD_INTERRUPT_EVENT_ENABLE
20	0	EVEN_FIELD_INTERRUPT_EVENT_ENABLE
	0	PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_B
	0	START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE
	0	PIPE_B_FRAMESTART_INTERRUPT_ENABLE
16	0	PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE
	0	SPRITE_D_FLIP_DONE_INTERRUPT_STATUS
	0	SPRITE_C_FLIP_DONE_INTERRUPT_STATUS
	0	CRC_ERROR_STATUS
12	0	CRC_DONE_INTERRUPT_STATUS
	0	SECOND_PERFORMANCE_COUNTER2_INTERRUPT_STATUS
	0	PLANE_B_FLIP_DONE_INTERRUPT_STATUS
	0	PIPE_B_VERTICAL_SYNC_STATUS
8	0	PIPE_B_DISPLAY_LINE_COMPARE_STATUS
	0	BLM_IMAGE_BRIGHTNESS_STATUS
	0	RESERVED
	0	ODD_FIELD_INTERRUPT_STATUS
4	0	EVEN_FIELD_INTERRUPT_STATUS
	0	PIPE_B_PANEL_SELF_REFRESH_STATUS
	0	START_OF_VERTICAL_BLANK_INTERRUPT_STATUS
	0	PIPE_B_FRAMESTART_INTERRUPT_STATUS
0	0	PIPE_B_HORIZONTAL_BLANK_STATUS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/1C	**PIPE_B_UNDERFLOW_STATUS:** This bit is set when an underflow occurs at the display pipe B. It is cleared by writing a one to this bit. This event will occur naturally during mode changes, to be effective, it should be cleared after a mode change. This bit is only valid after Pipe B has been completely configured. 1 = FIFO B Underflow occurred 0 = FIFO B Underflow did not occur AccessType: One to Clear
30	0b RW	**SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite D flip done interrupt status bit in the first line interrupt logic 0 = Sprite D Flip Done Interrupt Disabled 1 = Sprite D Flip Done Interrupt Enabled
29	0b RW	**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Error Detect Disabled 1 = CRC Error Detect Enabled
28	0b RW	**CRC_DONE_ENABLE:** This will enable the consideration of the CRC done status bit in the first line interrupt/status logic. 0 = CRC Done Detect Disabled 1 = CRC Done Detect Enabled
27	0b RW	**PERFORMANCE_COUNTER2_INTERRUPT_ENABLE:** This bit enables the second performance counter interrupt. 0 = Second Performance Counter2 Interrupt Status Disabled 1 = Second Performance Counter2 interrupt Status Enabled
26	0b RW	**PLANE_B_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Plane B flip done interrupt status bit in the first line interrupt logic 0 = Plane B flip done Interrupt/Status Disabled 1 = Plane B flip done Interrupt/Status Enabled
25	0b RW	**VERTICAL_SYNC_INTERRUPT_ENABLE:** 0 = Vertical Sync Interrupt/Status Disabled 1 = Vertical Sync Interrupt/Status Enabled

Bit Range	Default & Access	Field Name (ID): Description
24	0b RW	**DISPLAY_LINE_COMPARE_ENABLE:** 0 = Pipe B Display Line Compare Status Report Disabled 1 = Pipe B Display Line Compare Status report Enabled
23	0b RW	**BLM_EVENT_ENABLE:** [DevCL, DevCTG, DevCDV]: This interrupt is generated by the image brightness segment comparators. Which segment cause an interrupt are controlled by the BLM Histogram control register. 0 = No BLM event enabled 1 = BLM event enabled
22	0b RW	**SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite C flip done interrupt status bit in the first line interrupt logic 0 = Sprite C Flip Done Interrupt Disabled 1 = Sprite C Flip Done Interrupt Enabled
21	0b RW	**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** . This bit should only be used when this pipe is in an interlaced display timing.0 = Odd Field Event disable 1 = Odd Field Event enable
20	0b RW	**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** . This bit should only be used when this pipe is in an interlaced display timing.0 = Even field Event disable 1 = Even field Event enable
19	0b RW	**PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_B:** 0 = PSR interrupt Disabled on Pipe B 1 = PSR Interrupt Enabled on Pipe B
18	0b RW	**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/ status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	0b RW	**PIPE_B_FRAMESTART_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Pipe B Framestart Interrupt/Status Disabled 1 = Pipe B Framestart Interrupt/Status Enabled
16	0b RW	**PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** : This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled
15	0b RW/1C	**SPRITE_D_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite D 0 = Sprite D Flip Not Done 1 = Sprite D Flip Done AccessType: One to Clear
14	0b RW/1C	**SPRITE_C_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite C 0 = Sprite C Flip Not Done 1 = Sprite C Flip Done AccessType: One to Clear
13	0b RW/1C	**CRC_ERROR_STATUS:** This bit is set when a Pipe B CRC error is detected. It is cleared by a write of a one. 0 = No CRC Error 1 = CRC Error detected AccessType: One to Clear
12	0b RW/1C	**CRC_DONE_INTERRUPT_STATUS:** This bit is set when Pipe B CRC calculation and compare are complete. It is cleared by a write of a one. 0 = CRC Not Done 1 = CRC Done AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
11	0b RW/1C	**SECOND_PERFORMANCE_COUNTER2_INTERRUPT_STATUS:** This bit is set when the second performance counter2 generates an interrupt. It is cleared by a write of a one. 0 = Second performance counter interrupt event not asserted 1 = Second performance counter interrtup event asserted AccessType: One to Clear
10	0b RW/1C	**PLANE_B_FLIP_DONE_INTERRUPT_STATUS:** Async/Sync Flip Event is completed on Display Plane B 0 = Plane B Flip Not Done 1 = Plane B Flip Done AccessType: One to Clear
9	0b RW/1C	**PIPE_B_VERTICAL_SYNC_STATUS:** 0 = Vertical Sync not asserted 1 = Vertical Sync asserted AccessType: One to Clear
8	0b RW/1C	**PIPE_B_DISPLAY_LINE_COMPARE_STATUS:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 = Display Line Compare Status not asserted 1 = Display Line Compare Status asserted AccessType: One to Clear
7	0b RW/1C	**BLM_IMAGE_BRIGHTNESS_STATUS:** [DevCL, DevCTG, DevCDV]: This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 =DPST Interrupt has not occurred on pipe B 1 = DPST Interrupt has occurred on pipe B AccessType: One to Clear
6	0b RW	**RESERVED:** MBZ
5	0b RW/1C	**ODD_FIELD_INTERRUPT_STATUS:** . This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set.Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear
4	0b RW/1C	**EVEN_FIELD_INTERRUPT_STATUS:** . This status bit will be set on a even filed VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set.Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	0b RW/1C	**PIPE_B_PANEL_SELF_REFRESH_STATUS:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe B 1 = PSR interrupt has occurred on pipe B AccessType: One to Clear
2	0b RW/1C	**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW/1C	**PIPE_B_FRAMESTART_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Pipe B Framestart Status has not occurred 1 = Pipe B Framestart Status has occurred AccessType: One to Clear
0	0b RW/1C	**PIPE_B_HORIZONTAL_BLANK_STATUS:** 0 = Pipe B Horizontal Blank has not occurred 1 = Pipe B Horizontal Blank has occurred AccessType: One to Clear

14.11.247 PIPEBFRAMECOUNT—Offset 71040h

Pipe B Frame Counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71040h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PIPE_B_FRAME_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**PIPE_B_FRAME_COUNT:** Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after 2^32 frames

14.11.248 PIPEBFLIPCOUNT—Offset 71044h

Pipe B Flip Counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71044h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PIPE_B_FLIP_COUNT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**PIPE_B_FLIP_COUNT:** Provides read back of the display pipe flip counter. This counter increments on each flip of the surface of the primary plane on this pipe. This includes command streamer asynchronous and synchronous flips and any MMIO writes to the primary plane surface address. It rolls over back to 0 after 2^32 flips.

14.11.249 PIPEBMSAMISC—Offset 71048h

Pipe B MSA MISC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71048h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HARDWARE_DRIVE_MSA_MISC1_ENABLE | RESERVED | MSA_MISC1_FIELD_S3D

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**HARDWARE_DRIVE_MSA_MISC1_ENABLE:** This bit enables hardware to drive MSA MISC1 bit3:1 with the stero 3D left/right eye field indication. Hardware will drive 000 when S3D mode is disabled, 001 when enabled and the upcoming video frame is right eye, 011 when enabled and the upcoming video frame is left eye. When this bit is disabled, software may manually program the MSA MISC1 Field S3D field in bit 2:0 in this register to set MISC1 bit 3:1 0 = Disable hardware driving MSA MISC1 bit 3:1. Allow software to manually program MSA MISC1 bit3:1 through MSA_MISC1_FIELD_S3D (default) 1 = Enable hardware to drive MSA MISC1 bit3:1 for S3D
30:3	0b RW	**RESERVED:** Reserved.
2:0	0b RW	**MSA_MISC1_FIELD_S3D:** This field provides software to manually program MSC1 stero video attribute for DisplayPort: 000 = No stereo video transported 001 = For progressive video, the next (upcoming) video frame is RIGHT eye 010 = Reserved 011 = For progressive video, the next (upcoming) video frame is LEFT eye 100 = Stacked top and bottom top half represents left-eye view and bottom half represents right-eye view 101 = Stacked top and bottom top half represents right-eye view and bottom half represents left-eye view

14.11.250 DSPBADDR—Offset 7117Ch

Display B Async flip Start Address Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7117Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:12	11:4	3	2	1:0
Default	0000 0000 0000 0000 0000	0000 0000	0	0	00
Field	DISPLAY_B_START_ADDRESS_BITS	RESERVED_MBZ	FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_MBZ_1

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**DISPLAY_B_START_ADDRESS_BITS:** This register provides the start address of the display B plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . Write to this register triggers async flip The async flip address is written into the Display B Base Address register 0x7119C
11:4	0b RW	**RESERVED_MBZ:** Reserved.
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0b RW	**RESERVED_MBZ_1:** Reserved.

14.11.251 DSPBCNTR—Offset 71180h

Display B/Sprite Plane Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71180h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	DISPLAY_B_SPRITE_PRIMARY_B_ENABLE
30	DISPLAY_B_SPRITE_GAMMA_ENABLE
29:26	DISPLAY_B_SOURCE_PIXEL_FORMAT
25:24	PIPE_SELECT
23	KEY_WINDOW_ENABLE
22	SOURCE_KEY_ENABLE
21:20	PIXEL_MULTIPLY
19:16	RESERVED
15	_180DISPLAY_ROTATION
14	RESERVED_1
13	RESERVED_2
12:11	RESERVED_3
10	TILED_SURFACE
9	RESERVED_4
8:1	RESERVED_5
0	S3D_FORCE_DISPLAY_B_BOTTOM

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**DISPLAY_B_SPRITE_PRIMARY_B_ENABLE:** This bit will enable or disable the display B/sprite. When this bit is set, the plane will generate pixels for display. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 = Enable 0 = Disable
30	0b RW	**DISPLAY_B_SPRITE_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display B pixel data bypasses the pipe gamma correction logic (default). 1 = Display B pixel data is gamma corrected in the pipe gamma correction logic

Bit Range	Default & Access	Field Name (ID): Description
29:26	0b RW	**DISPLAY_B_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/display B. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	01b RO	**PIPE_SELECT:** Plane B always ties to Pipe B. Reserved AccessType: Read Only
23	0b RW	**KEY_WINDOW_ENABLE:** This applies only to devices with a Display Plane C. It determines what area of the screen the source key compare should be applied. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and display A should not be enabled on this pipe for this to be used. The function is only effective when display C is enabled and defined by Z-order to be behind display B. 0 = If keying is enabled, it applies to the entire display B plane 1 = If keying is enabled, it applies only to the intersection between display B and display C [DevBLC] and [DevCTG]: Reserved
22	0b RW	**SOURCE_KEY_ENABLE:** When used as a sprite or a secondary this enables source color keying. Sprite pixel values that match the key will become transparent. Source keying allows a plane that is behind (below) this plane to show through where the display B data matches the display B key. This function is overloaded to provide display C destination keying when combined with the key window enable bit.. Setting this bit is not allowed when the display pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled. [DevBLC] and [DevCTG]: Reserved In destination keying, primary plane pixel will be made transparent when blending with sprite pixel as the destination if the primary src key matches with the primary pixel value.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19:16	0b RW	**RESERVED:** Write as zero
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. [DevCL] Do not enable 180 rotation together with Frame Buffer Compression 0 = No rotation 1 = 180 rotation

Bit Range	Default & Access	Field Name (ID): Description
14	0b RW	**RESERVED_1:** [DevBW, DevCL, DevCDV] [DevBLC, DevCTG] Display B Trickle Feed Enable: 0 = Trickle Feed Enabled - Display B data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display B data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled. [DevELK] Must always be programmed disabled
13	0b RW	**RESERVED_2:** [DevBW, DevCL, DevCDV] [DevBLC, DevCTG] Display B Data Buffer Partitioning Control: 0 = Display B Data Buffer will encompass Sprite B buffer space when Sprite B is disabled. 1 = Display B Data Buffer will not use Sprite B buffer space when Sprite B is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	0b RW	**RESERVED_3:** Reserved.
10	0b RW	**TILED_SURFACE:** This bit indicates that the display B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPBSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPBLINOFF, DSPBTILEOFF, and DSPBSURF registers. 0 = Display B surface uses linear memory 1 = Display B surface uses X-tiled memory
9	0b RW	**RESERVED_4:** [DevBW, DevCL, DevCDV] Write as zero [DevBLC, DevCTG] Asynchronous Surface Address Update Enable: This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPBSURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPBSURF MMIO writes will update asynchronously
8:1	0b RW	**RESERVED_5:** Write as zero
0	0b RW	**S3D_FORCE_DISPLAY_B_BOTTOM:** This bit will force the display B plane to be on the bottom of any sprite planes in the Z order. 0 = Display B Z-order is determined by the other control bits in pipe B 1 = Display B is forced to be on the bottom of any sprite planes in Z-order in pipe B

14.11.252 DSPBLINOFFSET—Offset 71184h

Display B/Sprite Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71184h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DISPLAY_B_OFFSET																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**DISPLAY_B_OFFSET:** This register provides the panning offset into the display B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

14.11.253 DSPBSTRIDE—Offset 71188h

Display B/Sprite Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71188h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DISPLAY_B_SPRITE_STRIDE																										RESERVED					

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**DISPLAY_B_SPRITE_STRIDE:** This is the stride for display B/Sprite in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. The maximum value for this register is fixed. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes. [DevBW, DevCL, DevCDV] The display stride must be power of 2 when doing Asynch Flips. [DevBW, DevCL, DevCDV] The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.
5:0	0b RW	**RESERVED:** Reserved.

14.11.254 DSPBKEYVAL—Offset 71194h

Sprite Color Key Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71194h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_KEY_VALUE								GREEN_KEY_VALUE								BLUE_KEY_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	0b RW	**RED_KEY_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

14.11.255 DSPBKEYMSK—Offset 71198h

Sprite Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71198h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
RESERVED	RED_MASK_VALUE	GREEN_MASK_VALUE	BLUE_MASK_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	0b RW	**RED_MASK_VALUE:** Specifies the color key mask for the sprite red/Cr channel.
15:8	0b RW	**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green/Y channel.
7:0	0b RW	**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue/Cb channel.

14.11.256 DSPBSURF—Offset 7119Ch

Display B Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7119Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

DISPLAY_B_SURFACE_BASE_ADDRESS	RESERVED_MBZ	FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_MBZ_1

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**DISPLAY_B_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPBTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPBLINOFF register. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED_MBZ:** Reserved.
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0b RW	**RESERVED_MBZ_1:** Reserved.

14.11.257 DSPBTILEOFF—Offset 711A4h

Display B Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 711A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				PLANE_START_Y_POSITION												RESERVED_1				PLANE_START_X_POSITION											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation. [DevBW, DevCL, DevCDV] When display stride is 16KB and doing Asynch Flips, do not program the offset to give pans of 7680 to 8191 bytes.

14.11.258 DSPBSURFLIVE—Offset 711ACh

Display B Live Surface Base Address Register [DevCTG-B, DevCDV]

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 711ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DISPLAY_B_LIVE_SURFACE_BASE_ADDRESS

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**DISPLAY_B_LIVE_SURFACE_BASE_ADDRESS:** . This gives the live value of the surface base address as being currently used for the plane.

14.11.259 DSPBFLPQSTAT—Offset 71200h

Flip Queue Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71200h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED	QUEUE_FREE_ENTRY_COUNT_RO	QUEUE_OCCUPIED_ENTRY_COUNT_RO

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RO	**RESERVED:** Write as zero (RO)
15:8	0b RO	**QUEUE_FREE_ENTRY_COUNT_RO:** This value indicates the number of free entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.
7:0	0b RO	**QUEUE_OCCUPIED_ENTRY_COUNT_RO:** This value indicates the number of occupied entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.

14.11.260 VGACNTRL—Offset 71400h

VGA Display Plane Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71400h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VGA_DISPLAY_DISABLE	VGA_POP_UP_2X_CENTERED_MODE_SCALING	VGA_PIPE_SELECT	RESERVED_		VGA_BORDER_ENABLE	VGA_CENTERING_ENABLE		VGA_PALETTE_READ_SELECT	VGA_PALETTE_A_WRITE_DISABLE	DUAL_PIPE_VGA_PALETTE_B_WRITE_DISABLE	LEGACY_VGA_8_BIT_PALETTE_ENABLE	PALETTE_BYPASS_TEST_MODE	NINE_DOT_DISABLE	RESERVED	RESERVED__1									BLINK_DUTY_CYCLE		VSYNC_BLINK_RATE					

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**VGA_DISPLAY_DISABLE:** This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA register settings. VGA display should only be enabled if all display planes other than VGA are disabled. After enabling the VGA, most display planes need to stay disabled, only the VGA popup (cursor A) can be enabled. The VGA display is never trusted. No secrets are allowed in the pre-allocated memory and VGA is limited to access only that memory. During trusted operation (when registers are locked via Lock), this bit will always act as if it was set to a one (disabled VGA display). VGA 132 Column text mode is not supported. 0 = VGA Display Enabled 1 = VGA Display Disabled
30	0b RW	**VGA_POP_UP_2X_CENTERED_MODE_SCALING:** When this bit is set to a one, the VGA and pop-up data is scaled using pixel doubling in both the horizontal and vertical direction for use on un-scaled flat panel displays. Setting this bit allows the VGA to run at higher dot clock frequencies and creates a larger (4x the size) image for better quality on larger displays. It is intended for use in one of the centering modes when not using the internal panel fitting. Do not use it for native VGA modes or when internal panel fitting is used to scale VGA. In the situations where it is used, for 1280 wide or larger panels this bit should be set. For exactly 1280 wide panels, the Nine-dot disable bit should also be set. This operation is in addition to the VGA functions that double the pixels and lines. 0 = VGA display is normal size 1 = VGA and VGA popup data is doubled in the horizontal and vertical direction.
29	0b RW	**VGA_PIPE_SELECT:** This bit only applies to devices with dual pipe support. For devices with a single display pipe, this bit will be ignored. For dual pipe devices, this bit determines which pipe is to receive the VGA display data. This must be changed only when the VGA display is in the disabled state via the VGA display disable bit or during the write to enable VGA display. 0 = Selects Assigns the VGA display to Pipe A 1 = Selects Assigns the VGA display to Pipe B
28:27	0b RW	**RESERVED_:** Software must preserve the contents of these bits.

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**VGA_BORDER_ENABLE:** This bit determines if the VGA border areas during VGA centering modes are included in the active display area and do or do not appear on integrated TV encoder output and devices that use centering such as on DVO connected flat panel, TV displays, or integrated panels. For use with the internal panel fitting logic, the border if enabled will be scaled along with the pixel data. Setting this bit allows the popup to be positioned overlapping the border area of the image. 0 = VGA Border areas are not included in the image size calculations for centering only active area. 1 = VGA Border areas are enabled and is passed to the display pipe for display and used in the image size calculation for centering modes
25:24	0b RW	**VGA_CENTERING_ENABLE:** VGA centering modes use the pipe timing generators to determine the actual display timings. This would normally correspond to the display panel size and timings. The VGA registers determine the centered VGA image height and width. The VGA border may or may not be considered in the calculation selected by the VGA Border Enable bit. For a proper image, the VGA image size should not exceed the pipe timing generator active rectangle. When using the internal panel fitting logic, the horizontal image size needs to be less than or equal to 2048 pixels to generate a proper image. The VGA image will either be centered within the pipe timing rectangle or appear in the upper left corner. Upper left corner centered mode is generally used for external panel scaling where the DVO stall signal is used and is always used for internal panel fitting operation. When panel fitter is enabled on the same pipe as VGA this register setting is ignored and upper left corner centered mode is always selected. When centering is disabled, the VGA CRTC registers determine the display timing compatible with legacy VGA devices for driving CRT like devices. 00 = VGA centering is disabled, VGA operates in Native VGA mode or when driving integrated TV 01 = VGA centering is enabled, VGA image appears in the center of the larger rectangle 10 = VGA centering is enabled, VGA image appears in the upper left corner of the larger rectangle 11 = VGA centering is enabled, VGA image appears in the upper left corner of the larger rectangle
23	0b RW	**VGA_PALETTE_READ_SELECT:** This bit only applies to dual display pipe devices and determines which palette VGA palette read accesses will occur from. 0 = VGA palette reads will access Palette A (default). 1 = VGA palette reads will access Palette B VGA palette reads are reads from I/O address 0x3c9.
22	0b RW	**VGA_PALETTE_A_WRITE_DISABLE:** This determines which palette the VGA palette writes will have as a destination. One or both palettes can be the destination. If both are disabled, writes will not affect the palette RAM contents. 0 = VGA palette writes will update Palette A (default). 1 = VGA palette writes will not update Palette A VGA palette writes are writes to I/O address 0x3C9h.
21	0b RW	**DUAL_PIPE_VGA_PALETTE_B_WRITE_DISABLE:** This determines which palette the VGA palette writes will have as a destination. One or both palettes can be the destination. If both are disabled, writes will not affect the palette RAM contents. 0 = VGA palette writes will update Palette B (default). 1 = VGA palette writes will not update Palette B VGA palette writes are writes to I/O address 0x3C9h.
20	0b RW	**LEGACY_VGA_8_BIT_PALETTE_ENABLE:** This bit only affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. It provides backward compatibility for original VGA programs (in it s default state) as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path. 0 = 6-bit DAC (default). 1 = 8-bit DAC.
19	0b RW	**PALETTE_BYPASS_TEST_MODE:** 0 = Pass VGA data through the palette for translation (Normal Operation) 1 = Bypass the palette for allowing testing without loading palette both VGA and popup data will bypass the palette in this mode.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**NINE_DOT_DISABLE:** Prevents DOS applications from setting the VGA display into a real 9-dot per character operation mode, instead the device emulates that using 8-dots per character. This is intended to provide VGA compatibility on DVI type connectors and integrated panels where there would otherwise not be room for the 720 horizontal pixels or 1440 pixels when horizontally doubled. The VGA register bit SR01(0) functionality is disabled. VGA panning control handles the pseudo 9-dot mode when both this bit is set and SR01(0) is clear. 0 = Enable use of 9-dot enable bit in VGA registers 1 = Ignore the 9-dot per character bit and always use 8
17	0b RW	**RESERVED:** Reserved.
16:8	0b RW	**RESERVED__1:** Software must preserve the contents of these bits.
7:6	0b RW	**BLINK_DUTY_CYCLE:** Controls the VGA text mode blink duty cycle relative to the cursor blink duty cycle. 00 = 100% Duty Cycle, Full Cursor Rate (Default) 01 = 25% Duty Cycle, Cursor Rate 10 = 50% Duty Cycle, Cursor Rate 11 = 75% Duty Cycle, Cursor Rate
5:0	0b RW	**VSYNC_BLINK_RATE:** Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle. These bits are programmed with the (VSYNCs/cycle)/2-1. The proper programming of this register is determined by the VSYNC rate that the display requires when in a VGA display mode.

14.11.261 SWF10—Offset 71410h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71410h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.262 SWF11—Offset 71414h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71414h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.263 SWF12—Offset 71418h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71418h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.264 SWF13—Offset 7141Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7141Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.265 SWF14—Offset 71420h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71420h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.266 SWF15—Offset 71424h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71424h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.267 SWF16—Offset 71428h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71428h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.268 SWF17—Offset 7142Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7142Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.269 SWF18—Offset 71430h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71430h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.270 SWF19—Offset 71434h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71434h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.271 SWF1A—Offset 71438h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71438h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.272 SWF1B—Offset 7143Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7143Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.273 SWF1C—Offset 71440h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71440h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.274 SWF1D—Offset 71444h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71444h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.275 SWF1E—Offset 71448h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 71448h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.276 SWF1F—Offset 7144Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7144Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.277 SPACNTR—Offset 72180h

Sprite A Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72180h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPRITE_A_ENABLE, SPRITE_A_GAMMA_ENABLE, SPRITE_A_SOURCE_PIXEL_FORMAT, SPRITE_A_PIPE_SELECT, RESERVED, SPRITE_SOURCE_KEY_ENABLE, PIXEL_MULTIPLY, COLOR_CONVERSION_DISABLED, YUV_FORMAT, YUV_BYTE_ORDER, _180DISPLAY_ROTATION, RESERVED_1, TILED_SURFACE, RESERVED_2, SPRITE_A_BOTTOM, RESERVED_3, SPRITE_A_Z_ORDER

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SPRITE_A_ENABLE:** This bit will enable or disable the Sprite A. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0b RW	**SPRITE_A_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite A data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite A logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite A pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite A pixel data is gamma corrected in the pipe gamma correction logic
29:26	0b RW	**SPRITE_A_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite A. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0b RW	**SPRITE_A_PIPE_SELECT:** Sprite A always ties to pipe A. Reserved.
23	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22	0b RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite A pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite A pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled. Each sprite has built in source keying enabled/disabled. If the source keying is disabled and no alpha blending is enabled, the pixels are tagged as opaque. If sprite source keying is enabled and no alpha blending is enabled, it works as follows: For YUV sprite data, each yuv channel data is compared with the corresponding channel s key color Low and High (each channel inrange can be masked out). If all three channels are in range between the low and high key values, it is considered source compared. For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared. If the sprite source data compare and matches, then the sprite data will be tagged as transparent when blending with its destination pixel. If the sprite source data does not compare, then the sprite data will be tagged as opaque when blending with its destination pixel.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0b RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0b RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0b RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0b RW	**RESERVED_1:** Reserved.
10	0b RW	**TILED_SURFACE:** This bit indicates that the Sprite A surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite A surface uses linear memory 1 = Sprite A surface uses X-tiled memory
9:3	0b RW	**RESERVED_2:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**SPRITE_A_BOTTOM:** This bit will force the Sprite A plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite A Z order is determined by the other control bits 1 = Sprite A is forced to be on the bottom of the Z order.
1	0b RW	**RESERVED_3:** Reserved.
0	0b RW	**SPRITE_A_Z_ORDER:** With Sprite A and B z-order, bottom control bits, Sprite A plane is placed in a specific z-order among other planes. Display Pipe A Z-orders SA zorderSA bottomSB zorderSB bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PA SA SB CAPA in Black 1000PA SB SA CAPA in Black 0001SB PA SA CAuse src keying on SB 0011SB PA SA CAuse src keying on SB 1001SB SA PA CAuse src keying on SA 1011SB SA PA CAuse src keying on SA 0100SA PA SB CAuse src keying on SA 1100SA PA SB CAuse src keying on SA 0110SA SB PA CAuse src keying on SB 1110SA SB PA CAuse src keying on SB 0: Sprite A z-order is disabled 1: Sprite A z-order is enabled

14.11.278 SPALINOFF—Offset 72184h

Sprite A Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72184h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPRITE_A_OFFSET

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**SPRITE_A_OFFSET:** This register provides the panning offset into the Sprite A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

14.11.279 SPASTRIDE—Offset 72188h

Sprite A Stride Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72188h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPRITE_A_STRIDE | RESERVED

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**SPRITE_A_STRIDE:** This is the stride for Sprite A in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0b RW	**RESERVED:** Reserved.

14.11.280 SPAPOS—Offset 7218Ch

Sprite A Position Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7218Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED	SPRITEY_POSITION			RESERVED_1	SPRITE_X_POSITION		

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

14.11.281 SPASIZE—Offset 72190h

Sprite A Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72190h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED	SPRITE_HEIGHT			RESERVED_1	SPRITE_WIDTH		

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
27:16	0b RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

14.11.282 SPAKEYMINVAL—Offset 72194h

Sprite A Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72194h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:24	23:16	15:8	7:0
RESERVED	RED_KEY_MIN_VALUE	GREEN_KEY_MIN_VALUE	BLUE_KEY_MIN_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

14.11.283 SPAKEYMSK—Offset 72198h

Sprite A Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72198h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0
Field	RESERVED	RED_CHANNEL_ENABLE	GREEN_CHANNEL_ENABLE	BLUE_CHANNEL_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**RESERVED:** Write as zero
2	0b RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0b RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0b RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

14.11.284 SPASURF—Offset 7219Ch

Sprite A Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7219Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPRITE_A_SURFACE_BASE_ADDRESS																				RESERVED								FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_1	

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**SPRITE_A_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED:** : MBZ
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0b RW	**RESERVED_1:** : MBZ

14.11.285 SPAKEYMAXVAL—Offset 721A0h

Sprite A Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:24	23:16	15:8	7:0
RESERVED	RED_KEY_MAX_VALUE	GREEN_KEY_MAX_VALUE	BLUE_KEY_MAX_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
23:16	0b RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

14.11.286 SPATILEOFF—Offset 721A4h

Sprite A Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:28	Bits 27:16	Bits 15:12	Bits 11:0
RESERVED	PLANE_START_Y_POSITION	RESERVED_1	PLANE_START_X_POSITION

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

14.11.287 SPACONTALPHA—Offset 721A8h

Sprite A Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ENABLE_CONSTANT_ALPHA	RESERVED																							SPRITE_A_CONSTANT_ALPHA_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_CONSTANT_ALPHA:** Sprite A Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite A Sprite Constant Alpha is disabled 1 Sprite A Sprite Constant Alpha is enabled
30:8	0b RW	**RESERVED:** : MBZ
7:0	0b RW	**SPRITE_A_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

14.11.288 SPALIVESURF—Offset 721ACh

Sprite A Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPRITE_A_LIVE_SURFACE_BASE_ADDRESS																				RESERVED								FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_1	

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RO	**SPRITE_A_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for the Sprite A plane.
11:4	0b RO	**RESERVED:** : MBZ
3	0b RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0b RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0b RO	**RESERVED_1:** : MBZ

14.11.289 SPACLRC0—Offset 721D0h

Sprite A Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED					CONTRAST									RESERVED_1										BRIGHTNESS							

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:18	001000000b RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0b RW	**RESERVED_1:** Reserved.
7:0	0b RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

14.11.290 SPACLRC1—Offset 721D4h

Sprite A Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

RESERVED	SATURATION_AND_HUE_SIN_SH_SIN	RESERVED_1	SATURATION_AND_HUE_COS_SH_COS

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:16	0b RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0b RW	**RESERVED_1:** Reserved.
9:0	001000000 0b RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

14.11.291 SPAGAMC5—Offset 721E0h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721E0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00C0C0C0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved
23:16	11000000b RW	**RED_V_CR:** gamma correction mapping Red to cr
15:8	11000000b RW	**GREEN_Y:** gamma correction mapping green to Y

Bit Range	Default & Access	Field Name (ID): Description
7:0	11000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.292 SPAGAMC4—Offset 721E4h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721E4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00808080h

31 28	24 20	16 12	8 4 0
0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
RESERVED	RED_V_CR	GREEN_Y	BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	10000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	10000000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	10000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.293 SPAGAMC3—Offset 721E8h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721E8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00404040h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	01000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	01000000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	01000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.294 SPAGAMC2—Offset 721ECh

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00202020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	00100000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00100000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00100000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.295 SPAGAMC1—Offset 721F0h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721F0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00101010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Reserved.
23:16	00010000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00010000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00010000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.296 SPAGAMC0—Offset 721F4h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 721F4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00080808h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00001000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00001000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00001000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.297 SPBCNTR—Offset 72280h

Sprite B Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72280h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits 31 … 0: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Field
31	SPRITE_B_ENABLE
30	SPRITE_B_GAMMA_ENABLE
29:26	SPRITE_B_SOURCE_PIXEL_FORMAT
25:24	SPRITE_B_PIPE_SELECT
23	RESERVED
22	SPRITE_SOURCE_KEY_ENABLE
21:20	PIXEL_MULTIPLY
19	COLOR_CONVERSION_DISABLED
18	YUV_FORMAT
17:16	YUV_BYTE_ORDER
15	_180DISPLAY_ROTATION
14:11	RESERVED_1
10	TILED_SURFACE
9:3	RESERVED_2
2	SPRITE_B_BOTTOM
1	RESERVED_3
0	SPRITE_B_Z_ORDER

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SPRITE_B_ENABLE:** This bit will enable or disable the Sprite B. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable

Bit Range	Default & Access	Field Name (ID): Description
30	0b RW	**SPRITE_B_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite B data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite B logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite B pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite B pixel data is gamma corrected in the pipe gamma correction logic
29:26	0b RW	**SPRITE_B_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite B. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0b RW	**SPRITE_B_PIPE_SELECT:** Sprite B always ties to Pipe A. Reserved
23	0b RW	**RESERVED:** Reserved.
22	0b RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite B pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite B pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0b RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0b RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709

Bit Range	Default & Access	Field Name (ID): Description
17:16	0b RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0b RW	**RESERVED_1:** Reserved.
10	0b RW	**TILED_SURFACE:** This bit indicates that the Sprite B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite B surface uses linear memory 1 = Sprite B surface uses X-tiled memory
9:3	0b RW	**RESERVED_2:** Write as zero
2	0b RW	**SPRITE_B_BOTTOM:** This bit will force the Sprite B plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite B Z order is determined by the other control bits 1 = Sprite B is forced to be on the bottom of the Z order.
1	0b RW	**RESERVED_3:** Reserved.
0	0b RW	**SPRITE_B_Z_ORDER:** With Sprite A and B z-order, bottom control bits, Sprite B plane is placed in a specific z-order among other planes in pipe A. Display Pipe A Z-orders SA zorderSA bottomSB zorderSB bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PA SA SB CAPA in Black 1000PA SB SA CAPA in Black 0001SB PA SA CAuse src keying on SB 0011SB PA SA CAuse src keying on SB 1001SB SA PA CAuse src keying on SA 1011SB SA PA CAuse src keying on SA 0100SA PA SB CAuse src keying on SA 1100SA PA SB CAuse src keying on SA 0110SA SB PA CAuse src keying on SB 1110SA SB PA CAuse src keying on SB 0: Sprite B z-order is disabled 1: Sprite B z-order is enabled

14.11.298 SPBLINOFF—Offset 72284h

Sprite B Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72284h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPRITE_B_OFFSET

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**SPRITE_B_OFFSET:** This register provides the panning offset into the Sprite B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

14.11.299 SPBSTRIDE—Offset 72288h

Sprite B Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72288h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPRITE_B_STRIDE

RESERVED

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**SPRITE_B_STRIDE:** This is the stride for Sprite B in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0b RW	**RESERVED:** Reserved.

14.11.300 SPBPOS—Offset 7228Ch

Sprite B Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7228Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:28	27:16	15:12	11:0
Default	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
Field	RESERVED	SPRITEY_POSITION	RESERVED_1	SPRITE_X_POSITION

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

14.11.301 SPBSIZE—Offset 72290h

Sprite B Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72290h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				SPRITE_HEIGHT												RESERVED_1				SPRITE_WIDTH											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

14.11.302 SPBKEYMINVAL—Offset 72294h

Sprite B Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72294h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_KEY_MIN_VALUE								GREEN_KEY_MIN_VALUE								BLUE_KEY_MIN_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

14.11.303 SPBKEYMSK—Offset 72298h

Sprite B Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72298h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																													RED_CHANNEL_ENABLE	GREEN_CHANNEL_ENABLE	BLUE_CHANNEL_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0b RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0b RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

14.11.304 SPBSURF—Offset 7229Ch

Sprite B Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7229Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:12	11:4	3	2	1:0
SPRITE_B_SURFACE_BASE_ADDRESS	RESERVED_MBZ	FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_MBZ_1

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**SPRITE_B_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED_MBZ:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0b RW	**RESERVED_MBZ_1:** Reserved.

14.11.305 SPBKEYMAXVAL—Offset 722A0h

Sprite B Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:24	23:16	15:8	7:0
RESERVED	RED_KEY_MAX_VALUE	GREEN_KEY_MAX_VALUE	BLUE_KEY_MAX_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

14.11.306 SPBTILEOFF—Offset 722A4h

Sprite B Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:28	27:16	15:12	11:0
RESERVED	PLANE_START_Y_POSITION	RESERVED_1	PLANE_START_X_POSITION

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

14.11.307 SPBCONTALPHA—Offset 722A8h

Sprite B Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31	30:8	7:0
Default	0	0000000 0000 0000 0000 0000	0000 0000
Field	ENABLE_CONSTANT_ALPHA	RESERVED	SPRITE_B_CONSTANT_ALPHA_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_CONSTANT_ALPHA:** Sprite B Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite B Sprite Constant Alpha is disabled 1 Sprite B Sprite Constant Alpha is enabled
30:8	0b RW	**RESERVED:** : MBZ
7:0	0b RW	**SPRITE_B_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

14.11.308 SPBLIVESURF—Offset 722ACh

Sprite B Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:4	Bit 3	Bit 2	Bits 1:0
SPRITE_B_LIVE_SURFACE_BASE_ADDRESS	RESERVED_MBZ	FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_MBZ_1

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RO	**SPRITE_B_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite B plane.
11:4	0b RO	**RESERVED_MBZ:** Reserved.
3	0b RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0b RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0b RO	**RESERVED_MBZ_1:** Reserved.

14.11.309 SPBCLRC0—Offset 722D0h

Sprite B Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED	CONTRAST	RESERVED_1	BRIGHTNESS

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:18	001000000b RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0b RW	**RESERVED_1:** Reserved.
7:0	0b RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

14.11.310 SPBCLRC1—Offset 722D4h

Sprite B Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

RESERVED | SATURATION_AND_HUE_SIN_SH_SIN | RESERVED_1 | SATURATION_AND_HUE_COS_SH_COS

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:16	0b RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0b RW	**RESERVED_1:** Reserved.
9:0	001000000 0b RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

14.11.311 SPBGAMC5—Offset 722E0h

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722E0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00C0C0C0h

Bits	31:24	23:16	15:8	7:0
Value	0 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	1 1 0 0 0 0 0 0	1 1 0 0 0 0 0 0
Field	RESERVED	RED_V_CR	GREEN_Y	BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	11000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	11000000b RW	**GREEN_Y:** gamma correction mapping green to Y

Bit Range	Default & Access	Field Name (ID): Description
7:0	11000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.312 SPBGAMC4—Offset 722E4h

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722E4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00808080h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
RESERVED	RED_V_CR	GREEN_Y	BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	10000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	10000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	10000000b RW	**BLUE_U_CB:** gamma correction mapping CB

14.11.313 SPBGAMC3—Offset 722E8h

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722E8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00404040h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	01000000b RW	**RED_V_CR:** gamma correction mapping red to CR
15:8	01000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	01000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.314 SPBGAMC2—Offset 722ECh

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00202020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00100000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00100000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00100000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

14.11.315 SPBGAMC1—Offset 722F0h

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722F0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00101010h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00010000b RW	**RED_V_CR:** gamma correction mapping red to CR
15:8	00010000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00010000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

14.11.316 SPBGAMC0—Offset 722F4h

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 722F4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00080808h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00001000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00001000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00001000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

14.11.317 SPCCNTR—Offset 72380h

Sprite C Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72380h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	SPRITE_C_ENABLE
30	0	SPRITE_C_GAMMA_ENABLE
29:26	0 0 0 0	SPRITE_C_SOURCE_PIXEL_FORMAT
25:24	0 0	SPRITE_C_PIPE_SELECT
23	0	RESERVED
22	0	SPRITE_SOURCE_KEY_ENABLE
21:20	0 0	PIXEL_MULTIPLY
19	0	COLOR_CONVERSION_DISABLED
18	0	YUV_FORMAT
17:16	0 0	YUV_BYTE_ORDER
15	0	_180DISPLAY_ROTATION
14:11	0 0 0 0	RESERVED_1
10	0	TILED_SURFACE
9:3	0 0 0 0 0 0 0	RESERVED_2
2	0	SPRITE_C_BOTTOM
1	0	RESERVED_3
0	0	SPRITE_C_Z_ORDER

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SPRITE_C_ENABLE:** This bit will enable or disable the Sprite C. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable

Bit Range	Default & Access	Field Name (ID): Description
30	0b RW	**SPRITE_C_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite C data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite C logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite C pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite C pixel data is gamma corrected in the pipe gamma correction logic
29:26	0b RW	**SPRITE_C_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite C. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0b RW	**SPRITE_C_PIPE_SELECT:** Sprite C always ties to Pipe B Reserved.
23	0b RW	**RESERVED:** Reserved.
22	0b RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite C pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite C pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0b RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0b RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709

Bit Range	Default & Access	Field Name (ID): Description
17:16	0b RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0b RW	**RESERVED_1:** Reserved.
10	0b RW	**TILED_SURFACE:** This bit indicates that the Sprite C surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite C surface uses linear memory 1 = Sprite C surface uses X-tiled memory
9:3	0b RW	**RESERVED_2:** Write as zero
2	0b RW	**SPRITE_C_BOTTOM:** This bit will force the Sprite C plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite C Z order is determined by the other control bits 1 = Sprite C is forced to be on the bottom of the Z order.
1	0b RW	**RESERVED_3:** Reserved.
0	0b RW	**SPRITE_C_Z_ORDER:** With Sprite C and D z-order, bottom control bits, Sprite C plane is placed in a specific z-order among other planes in pipe B. Display Pipe B Z-orders SC zorderSC bottomSD zorderSD bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PB SC SD CBPB in Black 1000PB SD SC CBPB in Black 0001SD PB SC CBuse src keying on SD 0011SD PB SC CBuse src keying on SD 1001SD SC PB CBuse src keying on SC 1011SD SC PB CBuse src keying on SC 0100SC PB SD CBuse src keying on SC 1100SC PB SD CBuse src keying on SC 0110SC SD PB CBuse src keying on SD 1110SC SD PB CBuse src keying on SD 0101Not Allowed 0111Not Allowed 1101Not Allowed 1111Not Allowed 1010Not Allowed 1011Not Allowed 0: Sprite C z-order is disabled 1: Sprite C z-order is enabled

14.11.318 SPCLINOFF—Offset 72384h

Sprite C Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72384h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPRITE_C_OFFSET

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**SPRITE_C_OFFSET:** This register provides the panning offset into the Sprite C plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

14.11.319 SPCSTRIDE—Offset 72388h

Sprite C Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72388h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPRITE_C_STRIDE

RESERVED

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**SPRITE_C_STRIDE:** This is the stride for Sprite C in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0b RW	**RESERVED:** Reserved.

14.11.320 SPCPOS—Offset 7238Ch

Sprite C Position Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7238Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31:28	27:16	15:12	11:0
Default	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
Field	RESERVED	SPRITEY_POSITION	RESERVED_1	SPRITE_X_POSITION

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

14.11.321 SPCSIZE—Offset 72390h

Sprite C Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72390h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				SPRITE_HEIGHT												RESERVED_1				SPRITE_WIDTH											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

14.11.322 SPCKEYMINVAL—Offset 72394h

Sprite C Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72394h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | RED_KEY_MIN_VALUE | GREEN_KEY_MIN_VALUE | BLUE_KEY_MIN_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

14.11.323 SPCKEYMSK—Offset 72398h

Sprite C Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72398h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | RED_CHANNEL_ENABLE | GREEN_CHANNEL_ENABLE | BLUE_CHANNEL_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0b RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0b RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

14.11.324 SPCSURF—Offset 7239Ch

Sprite C Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7239Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:4	Bit 3	Bit 2	Bits 1:0
SPRITE_C_SURFACE_BASE_ADDRESS	RESERVED	FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**SPRITE_C_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED:** : MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0b RW	**RESERVED_1:** : MBZ

14.11.325 SPCKEYMAXVAL—Offset 723A0h

Sprite C Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED | RED_KEY_MAX_VALUE | GREEN_KEY_MAX_VALUE | BLUE_KEY_MAX_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the Sprite Clue/Cb channel.

14.11.326 SPCTILEOFF—Offset 723A4h

Sprite C Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED | PLANE_START_Y_POSITION | RESERVED_1 | PLANE_START_X_POSITION

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

14.11.327 SPCCONTALPHA—Offset 723A8h

Sprite C Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31	30:8	7:0
ENABLE_CONSTANT_ALPHA	RESERVED	SPRITE_C_CONSTANT_ALPHA_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_CONSTANT_ALPHA:** Sprite C Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite C Sprite Constant Alpha is disabled 1 Sprite C Sprite Constant Alpha is enabled
30:8	0b RW	**RESERVED:** : MBZ
7:0	0b RW	**SPRITE_C_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

14.11.328 SPCLIVESURF—Offset 723ACh

Sprite C Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPRITE_C_LIVE_SURFACE_BASE_ADDRESS																				RESERVED								FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_1	

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RO	**SPRITE_C_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite C.
11:4	0b RO	**RESERVED:** : MBZ
3	0b RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0b RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0b RO	**RESERVED_1:** : MBZ

14.11.329 SPCCLRC0—Offset 723D0h

Sprite C Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED					CONTRAST									RESERVED_1										BRIGHTNESS							

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:18	001000000b RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0b RW	**RESERVED_1:** Reserved.
7:0	0b RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

14.11.330 SPCCLRC1—Offset 723D4h

Sprite C Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

RESERVED | SATURATION_AND_HUE_SIN_SH_SIN | RESERVED_1 | SATURATION_AND_HUE_COS_SH_COS

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:16	0b RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0b RW	**RESERVED_1:** Reserved.
9:0	001000000 0b RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

14.11.331 SPCGAMC5—Offset 723E0h

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723E0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00C0C0C0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	11000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	11000000b RW	**GREEN_Y:** gamma correction mapping Green to Y

Bit Range	Default & Access	Field Name (ID): Description
7:0	11000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.332 SPCGAMC4—Offset 723E4h

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723E4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00808080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	10000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	10000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	10000000b RW	**BLUE_U_CB:** gamma correction mapping CB

14.11.333 SPCGAMC3—Offset 723E8h

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723E8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00404040h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	01000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	01000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	01000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.334 SPCGAMC2—Offset 723ECh

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00202020h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00100000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00100000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00100000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.335 SPCGAMC1—Offset 723F0h

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723F0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00101010h

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0	0 0 0 1 0 0 0 0	0 0 0 1 0 0 0 0
RESERVED	RED_V_CR	GREEN_Y	BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00010000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00010000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	00010000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.336 SPCGAMC0—Offset 723F4h

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 723F4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00080808h

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0	0 0 0 0 1 0 0 0	0 0 0 0 1 0 0 0
RESERVED	RED_V_CR	GREEN_Y	BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00001000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00001000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	00001000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.337 SWF30—Offset 72414h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72414h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED_

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.338 SWF31—Offset 72418h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72418h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED_																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.339 SWF32—Offset 7241Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7241Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED_																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**RESERVED_:** for Video BIOS and Drivers

14.11.340 SPDCNTR—Offset 72480h

Sprite D Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72480h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

Bits	31	30	29:26	25:24	23	22	21:20	19	18	17:16	15	14:11	10	9:3	2	1	0
Default	0	0	0000	00	0	0	00	0	0	00	0	0000	0	0000000	0	0	0
Field	SPRITE_D_ENABLE	SPRITE_D_GAMMA_ENABLE	SPRITE_D_SOURCE_PIXEL_FORMAT	SPRITE_D_PIPE_SELECT	RESERVED	SPRITE_SOURCE_KEY_ENABLE	PIXEL_MULTIPLY	COLOR_CONVERSION_DISABLED	YUV_FORMAT	YUV_BYTE_ORDER	_180DISPLAY_ROTATION	RESERVED_1	TILED_SURFACE	RESERVED_2	SPRITE_D_BOTTOM	RESERVED_3	SPRITE_D_Z_ORDER

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**SPRITE_D_ENABLE:** This bit will enable or disable the Sprite D. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0b RW	**SPRITE_D_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite D data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite D logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite D pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite D pixel data is gamma corrected in the pipe gamma correction logic
29:26	0b RW	**SPRITE_D_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite D. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0b RW	**SPRITE_D_PIPE_SELECT:** Sprite D always ties to Pipe B. Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23	0b RW	**RESERVED:** Reserved.
22	0b RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite D pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite D pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0b RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0b RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0b RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0b RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0b RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0b RW	**RESERVED_1:** Reserved.
10	0b RW	**TILED_SURFACE:** This bit indicates that the Sprite D surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite D surface uses linear memory 1 = Sprite D surface uses X-tiled memory
9:3	0b RW	**RESERVED_2:** Write as zero
2	0b RW	**SPRITE_D_BOTTOM:** This bit will force the Sprite D plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite D Z order is determined by the other control bits 1 = Sprite D is forced to be on the bottom of the Z order.
1	0b RW	**RESERVED_3:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**SPRITE_D_Z_ORDER:** With Sprite C and D z-order, bottom control bits, Sprite D plane is placed in a specific z-order among other planes in pipe B. Display Pipe B Z-orders SC zorderSC bottomSD zorderSD bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PB SC SD CBPB in Black 1000PB SD SC CBPB in Black 0001SD PB SC CBuse src keying on SD 0011SD PB SC CBuse src keying on SD 1001SD SC PB CBuse src keying on SC 1011SD SC PB CBuse src keying on SC 0100SC PB SD CBuse src keying on SC 1100SC PB SD CBuse src keying on SC 0110SC SD PB CBuse src keying on SD 1110SC SD PB CBuse src keying on SD 0101Not Allowed 0111Not Allowed 1101Not Allowed 1111Not Allowed 1010Not Allowed 1011Not Allowed 0: Sprite D z-order is disabled 1: Sprite D z-order is enabled

14.11.341 SPDLINOFF—Offset 72484h

Sprite D Linear Offset Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72484h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPRITE_D_OFFSET

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**SPRITE_D_OFFSET:** This register provides the panning offset into the Sprite D plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

14.11.342 SPDSTRIDE—Offset 72488h

Sprite D Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72488h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bits 5:0
SPRITE_D_STRIDE	RESERVED

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RW	**SPRITE_D_STRIDE:** This is the stride for Sprite D in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0b RW	**RESERVED:** Reserved.

14.11.343 SPDPOS—Offset 7248Ch

Sprite D Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7248Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				SPRITEY_POSITION												RESERVED_1				SPRITE_X_POSITION											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

14.11.344 SPDSIZE—Offset 72490h

Sprite D Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72490h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED				SPRITE_HEIGHT												RESERVED_1				SPRITE_WIDTH											

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
27:16	0b RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

14.11.345 SPDKEYMINVAL—Offset 72494h

Sprite D Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72494h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED								RED_KEY_MIN_VALUE								GREEN_KEY_MIN_VALUE								BLUE_KEY_MIN_VALUE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero
23:16	0b RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

14.11.346 SPDKEYMSK—Offset 72498h

Sprite D Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 72498h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																													RED_CHANNEL_ENABLE	GREEN_CHANNEL_ENABLE	BLUE_CHANNEL_ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**RESERVED:** Write as zero
2	0b RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0b RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0b RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

14.11.347 SPDSURF—Offset 7249Ch

Sprite D Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7249Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPRITE_D_SURFACE_BASE_ADDRESS																				RESERVED								FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_1	

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**SPRITE_D_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0b RW	**RESERVED:** : MBZ
3	0b RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0b RW	**RESERVED_1:** : MBZ

14.11.348 SPDKEYMAXVAL—Offset 724A0h

Sprite D Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724A0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:24	23:16	15:8	7:0
RESERVED	RED_KEY_MAX_VALUE	GREEN_KEY_MAX_VALUE	BLUE_KEY_MAX_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
23:16	0b RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0b RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0b RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the Sprite blue/Cb channel.

14.11.349 SPDTILEOFF—Offset 724A4h

Sprite D Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724A4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31 … 28	27 … 16	15 … 12	11 … 0
0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
RESERVED	PLANE_START_Y_POSITION	RESERVED_1	PLANE_START_X_POSITION

Bit Range	Default & Access	Field Name (ID): Description
31:28	0b RW	**RESERVED:** Write as zero
27:16	0b RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0b RW	**RESERVED_1:** Write as zero
11:0	0b RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

14.11.350 SPDCONTALPHA—Offset 724A8h

Sprite D Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724A8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31	30:8	7:0
0	0000000 0000 0000 0000 0000	0000 0000
ENABLE_CONSTANT_ALPHA	RESERVED	SPRITE_D_CONSTANT_ALPHA_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**ENABLE_CONSTANT_ALPHA:** Sprite D Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite D Constant Alpha is disabled 1 Sprite D Constant Alpha is enabled
30:8	0b RW	**RESERVED:** : MBZ
7:0	0b RW	**SPRITE_D_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

14.11.351 SPDLIVESURF—Offset 724ACh

Sprite D Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724ACh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:12	11:4	3	2	1:0
SPRITE_D_LIVE_SURFACE_BASE_ADDRESS	RESERVED	FLIP_SOURCE	DECRYPTION_REQUEST	RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RO	**SPRITE_D_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite D
11:4	0b RO	**RESERVED:** : MBZ
3	0b RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0b RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0b RO	**RESERVED_1:** : MBZ

14.11.352 SPDCLRC0—Offset 724D0h

Sprite D Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724D0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 01000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED | CONTRAST | RESERVED_1 | BRIGHTNESS

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:18	001000000b RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0b RW	**RESERVED_1:** Reserved.
7:0	0b RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

14.11.353 SPDCLRC1—Offset 724D4h

Sprite D Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724D4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits 31:27	Bits 26:16	Bits 15:10	Bits 9:0
RESERVED	SATURATION_AND_HUE_SIN_SH_SIN	RESERVED_1	SATURATION_AND_HUE_COS_SH_COS

Bit Range	Default & Access	Field Name (ID): Description
31:27	0b RW	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:16	0b RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0b RW	**RESERVED_1:** Reserved.
9:0	001000000 0b RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

14.11.354 SPDGAMC5—Offset 724E0h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724E0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00C0C0C0h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0
Field	RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	11000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	11000000b RW	**GREEN_Y:** gamma correction mapping Green to Y

Bit Range	Default & Access	Field Name (ID): Description
7:0	11000000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.355 SPDGAMC4—Offset 724E4h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724E4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00808080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	10000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	10000000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	10000000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

14.11.356 SPDGAMC3—Offset 724E8h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724E8h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00404040h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	01000000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	01000000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	01000000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

14.11.357 SPDGAMC2—Offset 724ECh

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724ECh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00202020h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00100000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00100000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00100000b RW	**BLUE_U_CB:** gamma correction mapping Blue to CB

14.11.358 SPDGAMC1—Offset 724F0h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724F0h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00101010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00010000b RW	**RED_V_CR:** gamma correction mapping red to CR
15:8	00010000b RW	**GREEN_Y:** gamma correction mapping green to Y
7:0	00010000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

14.11.359 SPDGAMC0—Offset 724F4h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 724F4h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00080808h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
RESERVED								RED_V_CR								GREEN_Y								BLUE_U_CB							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**RESERVED:** reserved
23:16	00001000b RW	**RED_V_CR:** gamma correction mapping Red to CR
15:8	00001000b RW	**GREEN_Y:** gamma correction mapping Green to Y
7:0	00001000b RW	**BLUE_U_CB:** gamma correction mapping blue to CB

14.11.360 PCSRC—Offset 73000h

Performance Counter Source Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 73000h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	PERFORMANCE_COUNTER_ENABLE
30	RESERVED
29	RESET_COUNTER
28	MAX_OR_MIN
27:22	SOURCE_FOR_PERFORMANCE_COUNTER
21:16	RESERVED_1
15:0	PERFORMANCE_COUNTER_THRESHOLD_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PERFORMANCE_COUNTER_ENABLE:** This bit enables the performance counter. 0 = Performance counter is disabled 1 = Performance counter is enabled.
30	0b RW	**RESERVED:** Reserved.
29	0b RW	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, summing all events in the frame 0 = Reset after each event within the frame

Bit Range	Default & Access	Field Name (ID): Description
28	0b RW	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value. The previous value is used to do the compare. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency
27:22	0b RW	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = VGA Font Request Latency 000010 = VGA Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA)
21:16	0b RW	**RESERVED_1:** Write as zero.
15:0	0b RW	**PERFORMANCE_COUNTER_THRESHOLD_VALUE:** This value is used to compare against the performance counter. If the performance counter matches this value, an interrupt is generated if the interrupt bit is enabled. When the source selected is DDB FIFO status, the threshold value is used to program the value needed to monitor in the DDB FIFO. No interrupt is generated in this condition.

14.11.361 PCSTAT—Offset 73004h

Performance Counter Status Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 73004h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OVERFLOW	RESET_COUNTER	MAX_OR_MIN	SOURCE_FOR_PERFORMANCE_COUNTER	RESERVED	PERFORMANCE_COUNTER_VALUE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**OVERFLOW:** This bit indicates weather the 16 bit counter overflowed or not. 0 = Counter is valid 1 = Counter is invalid since it overflowed
30	0b RO	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, sum of all event in the frame 0 = Reset after each event within the frame
29	0b RO	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value of the previous event. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
28:23	0b RO	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = VGA Font Request Latency 000010 = VGA Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA)
22:16	0b RO	**RESERVED:** Write as zero.
15:0	0b RO	**PERFORMANCE_COUNTER_VALUE:** This is the value of the performance counter for the source indicated in the source field.

14.11.362 PCSRC2—Offset 73008h

Performance Counter Source2 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 73008h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)

GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED	RESERVED_1	RESET_COUNTER	MAX_OR_MIN	SOURCE_FOR_PERFORMANCE_COUNTER						RESERVED_2						PERFORMANCE_COUNTER_THRESHOLD_VALUE															

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**RESERVED:** Programming note: This second performance counter is enabled by the enable bit in the PCSRC1 bit 31.
30	0b RW	**RESERVED_1:** Reserved.
29	0b RW	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, summing all events in the frame 0 = Reset after each event within the frame
28	0b RW	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value. The previous value is used to do the compare. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
27:22	0b RW	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = VGA Font Request Latency 000010 = VGA Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Streamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Streamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB)
21:16	0b RW	**RESERVED_2:** Write as zero.
15:0	0b RW	**PERFORMANCE_COUNTER_THRESHOLD_VALUE:** This value is used to compare against the performance counter. If the performance counter matches this value, an interrupt is generated if the interrupt bit is enabled. When the source selected is DDB FIFO status, the threshold value is used to program the value needed to monitor in the DDB FIFO. No interrupt is generated in this condition.

14.11.363 PCSTAT2—Offset 7300Ch

Performance Counter Status2 Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [GTTMMADR_LSB + 180000h] + 7300Ch

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVERFLOW	RESET_COUNTER	MAX_OR_MIN	SOURCE_FOR_PERFORMANCE_COUNTER						RESERVED							PERFORMANCE_COUNTER_VALUE															

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**OVERFLOW:** This bit indicates weather the 16 bit counter overflowed or not. 0 = Counter is valid 1 = Counter is invalid since it overflowed
30	0b RO	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, sum of all event in the frame 0 = Reset after each event within the frame
29	0b RO	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value of the previous event. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
28:23	0b RO	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = VGA Font Request Latency 000010 = VGA Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 101001 = InSR to HP Put (first put after inSR failing edge) 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB)
22:16	0b RO	**RESERVED:** Write as zero.
15:0	0b RO	**PERFORMANCE_COUNTER_VALUE:** This is the value of the performance counter for the source indicated in the source field.

14.12 Memory Mapped Registers (Read Only)

Table 174. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3BA–3BAh	1	"ST01 (ST01_MDA)—Offset 3BAh" on page 1035	00h
3C2–3C2h	1	"ST00—Offset 3C2h" on page 1036	00h
3C7–3C7h	1	"DACSTATE—Offset 3C7h" on page 1037	00h
3DA–3DAh	1	"ST01 (ST01_CGA)—Offset 3DAh" on page 1038	00h

14.12.1 ST01 (ST01_MDA)—Offset 3BAh

Input Status 1

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3BAh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED_AS_PER_VGA_SPECIFICATION	RESERVED	VIDEO_FEEDBACK_1_0		VER_TI_CAL_RETRACE_VIDEO	RESERVED_1		DIS_PLAY_ENA_BLE_OUTPUT

Bit Range	Default & Access	Field Name (ID): Description
7	0b RO	**RESERVED_AS_PER_VGA_SPECIFICATION:** Read as 0s.
6	0b RO	**RESERVED:** Read as 0.
5:4	0b RO	**VIDEO_FEEDBACK_1_0:** These are diagnostic video bits that are selected by the Color Plane Enable Register. These bits that are programmably connected to 2 of the 8 color bits sent to the palette. Bits 4 and 5 of the Color Plane Enable Register (AR12) selects which two of the 8 possible color bits become connected to these 2 bits of this register. The current software normally does not use these 2 bits. They exist for EGA compatibility.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RO	**VER_TI_CAL_RETRACE_VIDEO:** 0 = VSYNC inactive (Indicates that a vertical retrace interval is not taking place). 1 = VSYNC active (Indicates that a vertical retrace interval is taking place). Note: VGA pixel generation is not locked to the display output but is loosely coupled. A VSYNC indication may not occur during the actual VSYNC going to the display but during the VSYNC that is generated as part of the VGA pixel generation. The exact relationship will vary with the VGA display operational mode. This status bit will remain active when the VGA is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now it is incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. Bits 4 and 5 of the Vertical Retrace End Register (CR11) previously could program this bit to generate an interrupt at the start of the vertical retrace interval. This ability to generate interrupts at the start of the vertical retrace interval is a feature that is largely unused by legacy software. Interrupts are not supported through the VGA register bits.
2:1	0b RO	**RESERVED_1:** Read as 0s.
0	0b RO	**DIS_PLAY_ENA_BLE_OUTPUT:** Display Enable is a status bit (bit 0) in VGA Input Status Register 1 that indicates when either a horizontal retrace interval or a vertical retrace interval is taking place. This was used with the IBM* EGA graphics system (and the ones that preceded it, including MDA and CGA). In those cases, it was important to check the status of this bit to ensure that one or the other retrace intervals was taking place before reading from or writing to the frame buffer. In these earlier systems, reading from or writing to frame buffer at times outside the retrace intervals meant that the CRT controller would be denied access to the frame buffer. This resulted in either snow or a flickering display. This bit provides compatibility with software designed for those early graphics controllers. This bit is currently used in DOS applications that access the palette to prevent the sparkle associated with read and write accesses to the palette ram with the same address on the same clock cycle. This status bit will remain active when the VGA display is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now considered incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. When in panel fitting VGA or centered VGA operation, the meaning of these bits will not be consistent with native VGA timings. 0 = Active display data is being sent to the display. Neither a horizontal retrace interval or a vertical retrace interval is currently taking place. 1 = Either a horizontal retrace interval (horizontal blanking) or a vertical retrace interval (vertical blanking) is currently taking place.

14.12.2 ST00—Offset 3C2h

Input Status 0

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C2h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CRT_INTER_RUPT_PENDING	RESERVED		RGB_COMPARATOR_SENSE	RESERVED_1			

Bit Range	Default & Access	Field Name (ID): Description
7	0b RO	**CRT_INTER_RUPT_PENDING:** This bit is here for EGA compatibility and will always return zero. Note that the generation of interrupts was originally enabled, through bits [4,5] of the Vertical Retrace End Register (CR11). This ability to generate interrupts at the start of the vertical retrace interval is a feature that is typically unused by DOS software and therefore is only supported through other means for use under a operating system support. 0 = CRT (vertical retrace interval) interrupt is not pending. 1 = CRT (vertical retrace interval) interrupt is pending
6:5	0b RO	**RESERVED:** Read as 0s.
4	0b RO	**RGB_COMPARATOR_SENSE:** This bit returns the state of the output of the RGB output comparator(s). Video BIOS uses this bit during POST to determine whether the display is connected and if it is a color or monochrome CRT. BIOS blanks the screen or clears the frame buffer to display only black. Next, BIOS outputs a ramp to the D-to-A converters to test for the presence of a color display by determining which code cause the comparator to switch. Finally, if the BIOS does not detect any termination resistors on Red or Blue, it tests for the presence of a display using the Green signal. The result of each such test is read via this bit. 0 = Below threshold 1 = Above threshold
3:0	0b RO	**RESERVED_1:** Read as 0s.

14.12.3 DACSTATE—Offset 3C7h

DAC State Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C7h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED						DAC_STATE	

Bit Range	Default & Access	Field Name (ID): Description
7:2	0b RO	**RESERVED:** Read as 0.
1:0	0b RO	**DAC_STATE:** This field indicates which of the two index registers was most recently written. Bits [1:0] Index Register Indicated 00 Palette Write Index Register at I/O Address 3C7h (default) 01 Reserved 10 Reserved 11 Palette Read Index Register at I/O Address 3C8h

14.12.4 ST01 (ST01_CGA)—Offset 3DAh

Input Status 1

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3DAh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED_AS_PER_VGA_SPECIFICATION	RESERVED	VIDEO_FEEDBACK_1_0		VER_TI_CAL_RETRACE_VIDEO	RESERVED_1		DIS_PLAY_ENA_BLE_OUTPUT

Bit Range	Default & Access	Field Name (ID): Description
7	0b RO	**RESERVED_AS_PER_VGA_SPECIFICATION:** Read as 0s.
6	0b RO	**RESERVED:** Read as 0.
5:4	0b RO	**VIDEO_FEEDBACK_1_0:** These are diagnostic video bits that are selected by the Color Plane Enable Register. These bits that are programmably connected to 2 of the 8 color bits sent to the palette. Bits 4 and 5 of the Color Plane Enable Register (AR12) selects which two of the 8 possible color bits become connected to these 2 bits of this register. The current software normally does not use these 2 bits. They exist for EGA compatibility.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RO	**VER_TI_CAL_RETRACE_VIDEO:** 0 = VSYNC inactive (Indicates that a vertical retrace interval is not taking place). 1 = VSYNC active (Indicates that a vertical retrace interval is taking place). Note: VGA pixel generation is not locked to the display output but is loosely coupled. A VSYNC indication may not occur during the actual VSYNC going to the display but during the VSYNC that is generated as part of the VGA pixel generation. The exact relationship will vary with the VGA display operational mode. This status bit will remain active when the VGA is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now it is incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. Bits 4 and 5 of the Vertical Retrace End Register (CR11) previously could program this bit to generate an interrupt at the start of the vertical retrace interval. This ability to generate interrupts at the start of the vertical retrace interval is a feature that is largely unused by legacy software. Interrupts are not supported through the VGA register bits.
2:1	0b RO	**RESERVED_1:** Read as 0s.
0	0b RO	**DIS_PLAY_ENA_BLE_OUTPUT:** Display Enable is a status bit (bit 0) in VGA Input Status Register 1 that indicates when either a horizontal retrace interval or a vertical retrace interval is taking place. This was used with the IBM* EGA graphics system (and the ones that preceded it, including MDA and CGA). In those cases, it was important to check the status of this bit to ensure that one or the other retrace intervals was taking place before reading from or writing to the frame buffer. In these earlier systems, reading from or writing to frame buffer at times outside the retrace intervals meant that the CRT controller would be denied access to the frame buffer. This resulted in either snow or a flickering display. This bit provides compatibility with software designed for those early graphics controllers. This bit is currently used in DOS applications that access the palette to prevent the sparkle associated with read and write accesses to the palette ram with the same address on the same clock cycle. This status bit will remain active when the VGA display is disabled and the device is running in high resolution modes (non-VGA) to allow for applications that (now considered incorrect) use these status registers bits. In this case, the status will come from the pipe that the VGA is assigned to. When in panel fitting VGA or centered VGA operation, the meaning of these bits will not be consistent with native VGA timings. 0 = Active display data is being sent to the display. Neither a horizontal retrace interval or a vertical retrace interval is currently taking place. 1 = Either a horizontal retrace interval (horizontal blanking) or a vertical retrace interval (vertical blanking) is currently taking place.

14.13 Memory Mapped Registers (Write Only)

Table 175. Summary of Display Memory Mapped I/O Registers—GTTMMADR_LSB

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3BA–3BAh	1	"FCR (FCR_MDA_Write)—Offset 3BAh" on page 1041	00h
3C2–3C2h	1	"MSR (MSR_Write)—Offset 3C2h" on page 1042	00h
3C7–3C7h	1	"DACRX—Offset 3C7h" on page 1043	00h
3DA–3DAh	1	"FCR (FCR_CGA_Write)—Offset 3DAh" on page 1044	00h

14.13.1 FCR (FCR_MDA_Write)—Offset 3BAh

Feature Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3BAh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED				VSYNC_CONTROL	RESERVED_1		

Bit Range	Default & Access	Field Name (ID): Description
7:4	0b RW	**RESERVED:** Read as 0.
3	0b RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Ena ble output on the VSYNC pin. This capability was not typically very useful..
2:0	0b RW	**RESERVED_1:** Read as 0.

14.13.2 MSR (MSR_Write)—Offset 3C2h

Miscellaneous Output

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C2h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CRT_VSYNC_POLARITY	CRT_HSYNC_POLA_RITY	PAGE_SELECT	RESERVED	CLOCK_SELECT		A0000_BFFFH_MEMORY_ACCESS_ENABLE	I_O_ADDRESS_SELECT

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**CRT_VSYNC_POLARITY:** This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. Sync polarity was used in VGA to signal the monitor how many lines of active display are being generated. 0 = Positive Polarity (default). 1 = Negative Polarity.
6	0b RW	**CRT_HSYNC_POLA_RITY:** This is a legacy function that is used in native VGA modes. For most cases, sync polarity will be controlled by the port control bits. The VGA settings can be optionally selected for compatibility with the original VGA when used in the VGA native mode. 0 = Positive Polarity (default). 1 = Negative Polarity
5	0b RW	**PAGE_SELECT:** In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KB page in dis play mem ory for CPU access: 0 = Upper page (default) 1 = Lower page. Selects between two 64KB pages of frame buffer memory during standard VGA odd/even modes (modes 0h through 5h). Bit 1 of register GR06 can also program this bit in other modes. Note that this bit is would normally set to 1 by the software.
4	0b RW	**RESERVED:** Read as 0.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0b RW	**CLOCK_SELECT:** These bits can select the dot clock source for the CRT interface. The bits should be used to select the dot clock in standard native VGA modes only. When in the centering or upper left corner modes, these bits should be set to have no effect on the clock rate. The actual frequencies that these bits select, if they have any affect at all, is programmable through the DPLL registers that default to the standard values used for VGA. 00 = CLK0, 25.175 MHz (for standard VGA modes with 640 pixel (8-dot) horizontal resolution) (default) 01 = CLK1, 28.322 MHz. (for standard VGA modes with 720 pixel (9-dot) horizontal resolution) 10 = Was used to select an external clock (now unused) 11 = Reserved
1	0b RW	**A0000_BFFFFH_MEMORY_ACCESS_ENABLE:** VGA Compatibility bit enables access to local video memory (frame buffer) at A0000(BFFFFh. When disabled, accesses to VGA memory are blocked in this region. This bit is independent of and does not block CPU access to the video linear frame buffer at other addresses. Note that it is typical for AGP chipsets to shadow this register to allow proper steering of memory accesses to the proper bus. 0 = Prevent CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture (default). 1 = Allow CPU access to memory/registers/ROM through the A0000-BFFFF VGA memory aperture. This memory must be mapped as UC by the CPU; see VGA Host Access Memory Munging in Display and Overlay Functions.
0	0b RW	**I_O_ADDRESS_SELECT:** This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller re gisters, the Feature Control Register (FCR), and Input Status Register 1 (ST01). Presently ignored (whole range is claimed), but will ignore 3Bx for color configuration or 3Dx for monochrome. Note that it is typical in AGP chipsets to shadow this bit and properly steer I/O cycles to the proper bus for operation where a MDA exists on another bus such as ISA. 0 = Select 3Bxh I/O address (MDA emulation) (default). 1 = Select 3Dxh I/O address (CGA emulation).

14.13.3 DACRX—Offset 3C7h

Palette Read Index Register

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3C7h

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PALETTE_READ_INDEX							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0b WO	**PALETTE_READ_INDEX:** The 8-bit index value programmed into this register chooses which of 256 standard color data positions within the palette are to be made accessible for being read from via the Palette Data Register (DACDATA). The index value held in this register is automatically incremented when all three bytes of the color data position selected by the current index have been read. A write to this register will abort a uncompleted palette write sequence. This register allows access to the palette even when running non-VGA display modes.

14.13.4 FCR (FCR_CGA_Write)—Offset 3DAh

Feature Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [GTTMMADR_LSB + 180000h] + 3DAh

GTTMMADR_LSB Type: PCI Configuration Register (Size: 32 bits)
GTTMMADR_LSB Reference: [B:0, D:2, F:0] + 10h

Default: 00h

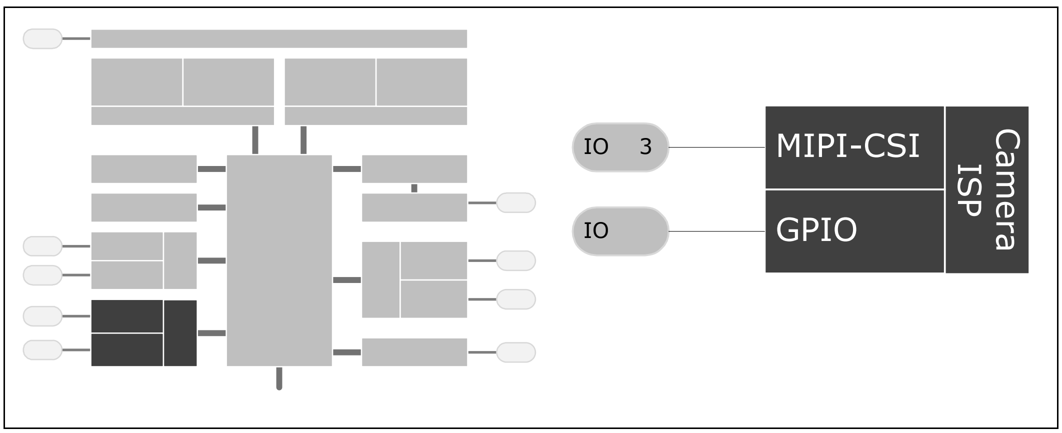
7			4				0
0	0	0	0	0	0	0	0
RESERVED				VSYNC_CONTROL	RESERVED_1		

Bit Range	Default & Access	Field Name (ID): Description
7:4	0b RW	**RESERVED:** Read as 0.
3	0b RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Ena ble output on the VSYNC pin. This capability was not typically very useful..
2:0	0b RW	**RESERVED_1:** Read as 0.

15 MIPI-Camera Serial Interface (CSI) and ISP

Note: The MIPI CSI and controller front end interfaces with three sensors and is capable of simultaneously acquiring three streams, one from each sensor. These three streams are presented to the ISP.

Note: If a 1-lane sensor needs to be connected to a MIPI-CSI port, that port must use a 1-lane port configuration.



15.1 Signal Descriptions

See Chapter 2, “Physical Interfaces” for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal’s function

Table 176. CSI Signals

Signal Name	Direction Plat. Power	Description
MCSI1_CLKP/N	I V1P24S	**Clock Lane:** MIPI CSI input clock lane 0 for port 1.
MCSI1_DP/N[3:0]	I V1P24S	**Data Lanes:** Four MIPI CSI Data Lanes (0-3) for port 1. Lanes 2 and 3 can optionally used as data lanes for port 3.
MCSI2_CLKP/N	I V1P24S	**Clock Lane:** MIPI CSI input clock lane 0 for port 2.
MCSI2_DP/N[0]	I V1P24S	**Data Lane:** Single MIPI CSI Data Lanes for port 2.
MCSI3_CLKP/N	I V1P24S	**Clock Lane:** MIPI CSI input clock lane 0 for port 3.
MCSI_RCOMP	I/O	**Resistor Compensation:** This is for pre-driver slew rate compensation for the MIPI CSI Interface. Contact your Intel representative for details.

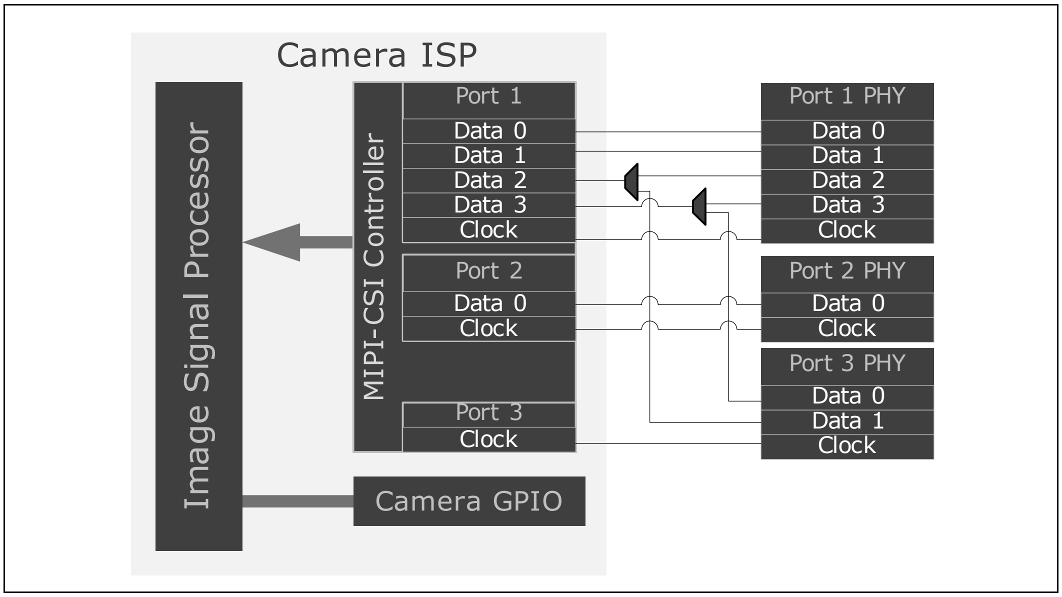
Table 177. GPIO Signals (Sheet 1 of 2)

Signal Name	Direction Plat. Power	Description
MCSI_GPIO[00]	I/O V1P8S	Output from shutter switch when its pressed halfway. This switch state is used to trigger the Auto focus LED for Xenon Flash or Torch mode for LED Flash
MCSI_GPIO[01]	I/O V1P8S	Output from shutter switch when its pressed full way. This switch state is used to trigger Xenon flash or LED Flash
MCSI_GPIO[02]	I/O V1P8S	Active high control signal to Xenon Flash to start charging the Capacitor
MCSI_GPIO[03]	I/O V1P8S	Active low output from Xenon Flash to indicate that the capacitor is fully charged and is ready to be triggered
MCSI_GPIO[04]	I/O V1P8S	Active high Xenon Flash trigger / Enables Torch Mode on LED Flash IC
MCSI_GPIO[05]	I/O V1P8S	Enables Red Eye Reduction LED for Xenon / Triggers STROBE on LED Flash IC /
MCSI_GPIO[06]	I/O V1P8S	Camera Sensor 0 Strobe Output to SoC to indicate beginning of capture / Active high signal to still camera to power down the device.
MCSI_GPIO[07]	I/O V1P8S	Camera Sensor 1 Strobe Output to SoC to indicate beginning of capture / Active high signal to still camera to power down the device.

Table 177. GPIO Signals (Sheet 2 of 2)

Signal Name	Direction Plat. Power	Description
MCSI_GPIO[08]	I/O V1P8S	Active high signal to video camera to power down the device.
MCSI_GPIO[09]	I/O V1P8S	Active low output signal to reset digital still camera #0.
MCSI_GPIO[10]	I/O V1P8S	Active low output signal to reset digital still camera #1
MCSI_GPIO[11]	I/O V1P8S	Active low output signal to reset digital video camera

Figure 94. Camera Connectivity



15.2 Features

- Integrated MIPI-CSI 2.0 interface
- Image Signal Processor (ISP) with DMA and local SRAM
- Imaging data is received by the MIPI-CSI interface and is relayed to the ISP for processing
- Up to five MIPI-CSI 2.0 data lanes
  — Each lane can operate at up to 1GT/s. resulting in roughly 800 Mbit/s of actual pixels
- The MIPI-CSI interface supports lossless compressed image streams to increases the effective bandwidth without losing data

- Up to 24MP sensors supported, and full HD 1080p60
  — Can also support Stereo HD 1080p30
- Up to 3 cameras can be operated simultaneously
  — Stereoscopic Captures
  — Front + Back Camera Usage

15.2.1 Imaging Capabilities

The following table summarizes imaging capabilities.

Table 178. Imaging Capabilities

Feature	Capabilities
Sensor interface	Configurable MIPI-CSI2 interfaces. 3 sensors: x2, x2, x1 or x3, x1, x1 2 sensors: x4, x1
Simultaneous sensors	Up to 3 simultaneous sensors
2D Image capture	24MP @ 15fps
2D video capture	Up to 1080p60
Input formats (Sensor -> SoC)	RAW 8, 10, 12, 14, RGB444, 565, 888, YUV420, 422, JPEG.
Output formats (SoC -> Sensor)	YUV422, YUV420, RAW
Special Features	Image and video stabilization Low light noise reduction Burst mode capture Memory to memory processing 3A (Auto Exposure (AE), Auto White Balance (AWB) and Auto Focus (AF)) High Dynamic Range (HDR) Multi-focus Zero shutter lag

15.2.2 Simultaneous Acquisition

All three cameras can be active at the same time.

SoC will support on-the-fly processing for only one image at a time. While this image is being processed on-the-fly, images from the other two cameras are saved to DRAM for later processing.

15.2.3 Primary Camera Still Image Resolution

Maximum still image resolution for the primary camera in post-processing mode is limited by the resolution of the sensors. Currently 24 Mpixel sensors are supported.

Maximum primary camera on-the-fly still image resolution for primary camera is 16 Mpixel at 18 fps.

Higher resolution, or higher frame rates are supported as long as the product of resolution and frame rate does not exceed 288 Mpixels/s (= 16 Mpixels * 18 fps).

Maximum primary camera on-the-fly stereoscopic still image resolution for primary camera is 8 Mpixel for each of the left and right images at 18 fps. The number of Mpixels can be increased by decreasing the frame rate.

15.2.4 Burst Mode Support

The SoC supports capturing multiple images back to back at maximum sensor resolution. At least 5 images must be captured in burst mode. The maximum number of images that can be so captured is limited only by available system memory. These images need not be processed on-the-fly.

15.2.5 Continuous Mode Capture

SoC supports capturing images and saving them to DRAM in a ring of frame buffers continuously at maximum sensor resolution. These images must then be fetched and processed on-the-fly by the ISP. This adds a round trip to memory for every frame and increases the bandwidth requirements.

15.2.6 Secondary Camera Still Image Resolution

Maximum secondary camera still image resolution is 4 Mpixel at 15 fps.

15.2.7 Primary Camera Video Resolution

Maximum primary camera video resolution is 1080p60.

Maximum primary camera dual video resolution is 1080p30.

Maximum stereo resolution is 1080p30.

15.2.8 Secondary Camera Video Resolution

Maximum secondary camera video resolution is 1080p30.

15.2.9 Bit Depth

Capable of processing 14-bit images at the stated performance levels.

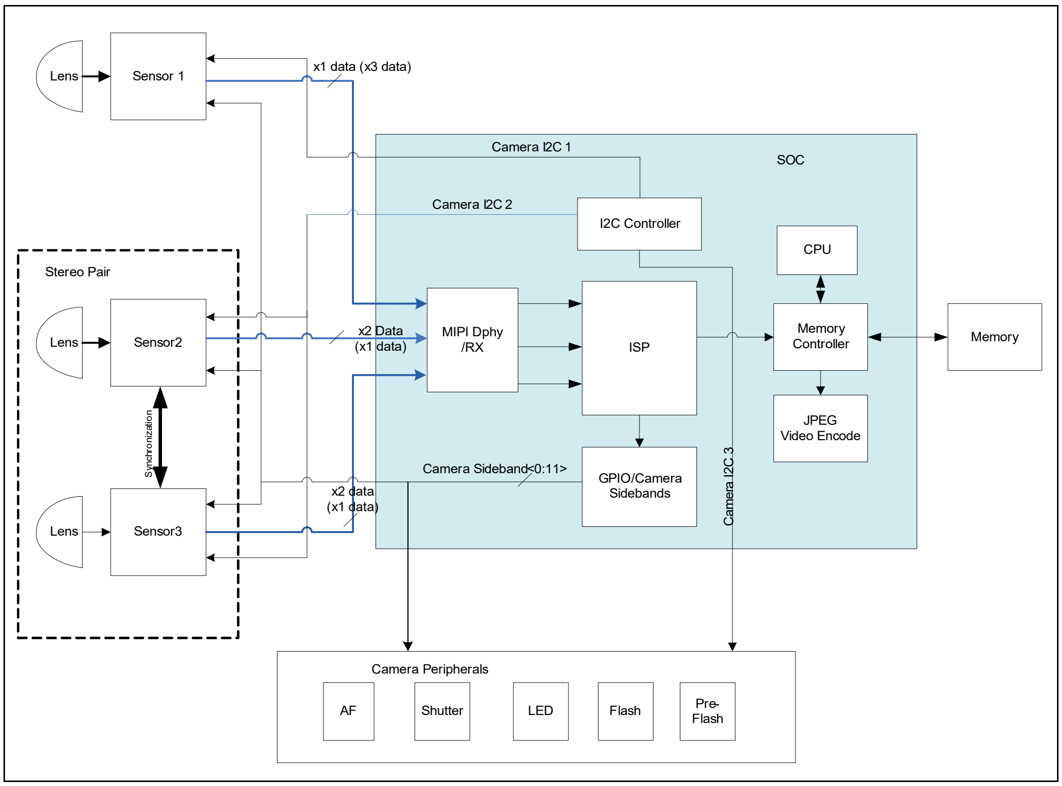
Capable of processing 18-bit images at half the performance levels, i.e. process on-the-fly 16 Mpixel 18-bit images at 7 fps instead of 15 fps.

Capable of processing up to 18-bit precision.

The higher precision processing will be employed mainly for high dynamic range imaging (HDR).

15.3 Imaging Subsystem Integration

Figure 95. Image Processing Components



15.3.1 CPU Core

The CPU core augments the signal processing capabilities of the hardware to perform post-processing on images such as auto focus, auto white balance, and auto exposure. The CPU also runs the drivers that control the GPIOs and I^2C for sensor control.

15.3.2 Imaging Signal Processor (ISP)

The ISP (Imaging Signal Processor) includes a 64-way vector processor enabling high quality camera functionality. Key features include support of three camera sensors.

15.3.2.1 MIPI-CSI-2 Ports

The SoC has three MIPI clock lanes and five MIPI data lanes. The Analog Front End (AFE) and Digital Physical Layer (DPHY) take these lanes and connects them to three virtual ports. Two data lanes are dedicated to each of the rear facing cameras and the remaining one data lane is connected to the front facing camera. The MIPI interfaces follow the MIPI-CSI-2 specifications as defined by the MIPI Alliance. They support YUV420, YUV422, RGB444, RGB555, RGB565, RGB 888 and RAW 8b/10b/12b. Both MIPI ports support compression settings specified in MIPI-CSI-2 draft specification 1.01.00 Annex E. The compression is implemented in Hardware with support for Predictor 1 and Predictor 2. Supported compression schemes:

- 12-8-12
- 12-7-12
- 12-6-12
- 10-8-10
- 10-7-10
- 10-6-10

The data compression schemes above use an X-Y-Z naming convention where X is the number of bits per pixel in the original image, Y is the encoded (compressed) bits per pixel and Z is the decoded (uncompressed) bits per pixel.

15.3.2.2 Camera Sideband for Camera Interface

Twelve (12) GPIO signals are allocated for camera functions, refer to Table 177 for signal names. These GPIOs are multiplexed and are available for other usages without powering on the ISP. The ISP provides a timing control block through which the GPIOs can be controlled to support assertion, de-assertion, pulse widths and delay. The configuration below of camera GPIOs is just an example of how the GPIOs can be used. Several of these functions could be implemented using I^2C, depending on the sensor implementation for the platform.

- Sensor Reset signals
  —Force hardware reset on one or more of the sensors.
- Sensor Single Shot Trigger signal
  —Indicate that the target sensor needs to send a full frame in a single shot mode, or to capture the full frame for flash synchronization.
- PreLight Trigger signal
  —Light up a pilot lamp prior to firing the flash for preventing red-eye.
- Flash Trigger signal
  —Indicate that a full frame is about to be captured. The Flash fires when it detects an assertion of the signal.
- Sensor Strobe Trigger signal
  —Asserted by the target sensor to indicate the start of a full frame, when it is configured in the single shot mode, or to indicate a flash exposed frame for flash synchronization.

15.4 Functional Description

At a high level, the Camera Subsystem supports the following modes:

- Preview
- Image capture
- Video capture

15.4.1 Preview Mode

Once the ISP and the camera subsystem is enabled, the ISP goes into the preview mode where very low resolution frames, such as VGA/480p (programmable), are being processed.

15.4.2 Image Capture

During the image capture mode, the camera subsystem can acquire at a peak throughput of 24 Mpixels @ 15fps. While doing this, it continues to output preview frames simultaneously.

- The ISP can output RAW, RGB or YUV formats. The ISP can capture one full frame at a time or perform burst mode capture, where up to five full back-to-back frames are recorded.
- The ISP will not limit the number of back-to-back full frames captured, but the number is programmable and determined on how much memory can be allocated dynamically.
- The ISP can process all the frames on the fly and writes to memory only after fully processing the frames, without requiring download of any part of the frame for further processing.
  - —The exceptions to this approach are image stabilization and some other advanced functions requiring temporal information over multiple frames.

The ISP can support image stabilization in image capture model.

- The ISP initially outputs preview frames.
- When the user decides to capture the picture, image stabilization is enabled. The ISP checks the previous frame for motion and compensates for it appropriately.

Auto Exposure (AE), Auto Focus (AF), and Auto White Balance (AWB), together known as 3A, are implemented in the CPU to provide flexibility.

15.4.3 Video Capture

During video recording, the ISP can capture video up to 1080p @ 60 fps and output preview frames concurrently. The ISP output video frames to memory in YUV420 or YUV422 format.

15.4.4 ISP Overview

The Camera Subsystem consists of 2 parts, the hardware subsystem and a software stack that implements the ISP functionality on top of this hardware.

The core of the ISP is a vector processor. The vector processor is supported by the following components:

- Interfaces for data and control
- A small input formatter that parallelizes the data
- A scalar (RISC) processor, for system control and low-rate processing
- An accelerator for scaling, digital zoom, and lens distortion correction
- A DMA engine transfers large amounts of data such as input and output image data or large parameter sets between LPDDR2 and the ISP block.

15.4.5 Memory Management Unit (MMU)

The camera subsystem has capabilities to deal with a virtual address space, since a contiguous memory range in the order 16–32MB cannot be guaranteed by the OS.

15.4.5.1 Interface

The MMU performs the lookup required for address translation from a virtual to physical 32-bit address. The lookup tables are stored external to the system. The MMU performs the lookup through a master interface without burst support that is connected to the Open Core Protocol (OCP) master of the subsystem. The MMU configuration registers can be accessed through a 32-bit Core I/O (CIO) slave interface. Additionally there is a 32-bit CIO slave interface connected to the address translator.

15.5 MIPI-CSI-2 Receiver

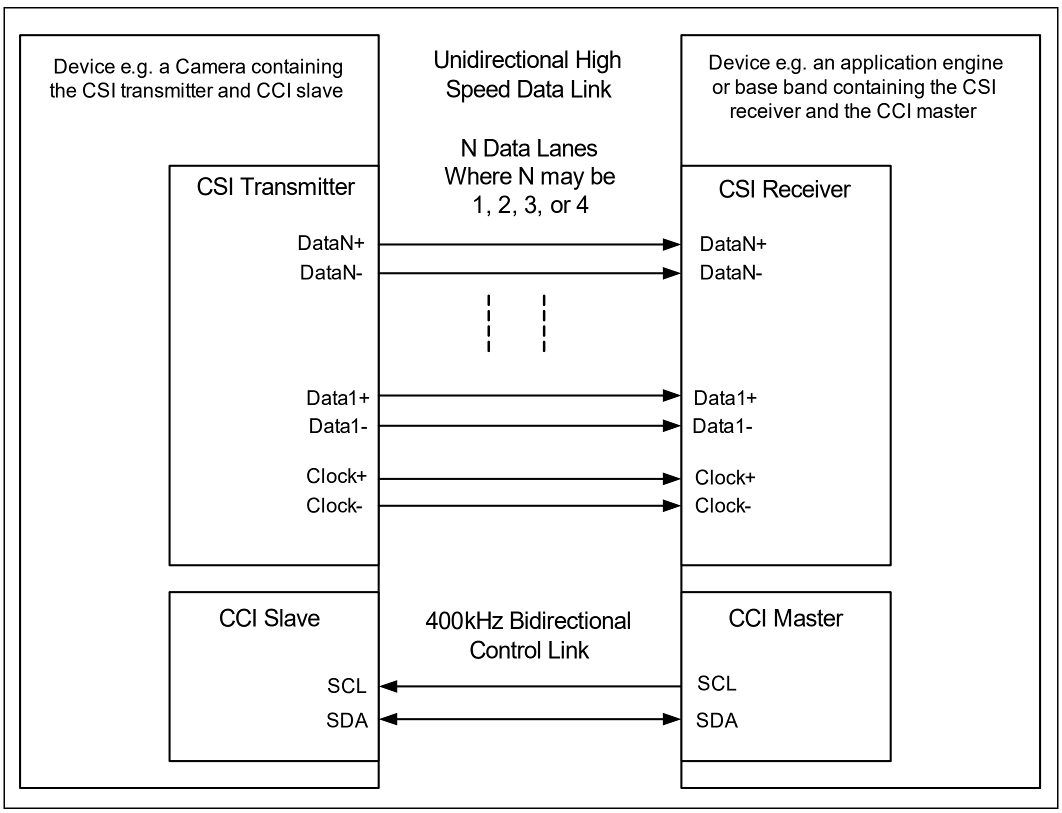
MIPI-CSI-2 devices are camera serial interface devices. They are categorized into two types, a CSI transmitter device with Camera Control Interface (CCI) slave and CSI receiver device with CCI master.

Data transfer by means of MIPI-CSI is unidirectional that is, from transmitter to receiver. CCI data transfer is bidirectional between the CCI slave and master.

Camera Serial Interface Bus (CSI) is a type of serial bus that enables transfer of data between a Transmitter device and a receiver device. The CSI device has a point-to-point connections with another CSI device by means of D-PHYs and as shown in Figure 96.

Similarly, CCI (Camera Control Interface bus) is a type of serial bus that enables transfer back and forth between the master CCI and a Slave CCI Unit.

Figure 96. MIPI-CSI Bus Block Diagram



D-PHY data lane signals are transferred point-to-point differentially using two signal lines and a clock lane. There are two signaling modes, a high speed mode that operates at 1000Mbs and a low power mode that works at 10Mbs. The mode is set to low power mode and a stop state at start up/power up. Depending on the desired data transfer type, the lanes switch between high and low power modes.

The CCI interface consists of an I^2C bus which has a clock line and a bidirectional data line.

The MIPI-CSI-2 devices operate in a layered fashion. There are 5 layers identified at the receiver and transmitter ends.

MIPI-CSI-2 Functional Layers:

- **PHY Layer**:
  - An embedded electrical layer sends and detects start of packet signalling and end of packet signalling on the data lanes. It contains a serializer and deserializer unit to interface with the PPI / lane management unit. There is also a clock divider unit to source and receive the clock during different modes of operation.
- **PPI/Lane Management Unit**:
  - This layer does the lane buffering and distributes the data in the lanes as programmed in a round robin manner and also merges them for the PLI/Low Level Protocol unit.
- **PLI/Low Level Protocol Unit**:
  - This layer packetizes as well as de-packetizes the data with respect to channels, frames, colors and line formats. There are ECC generator and corrector units to recover the data free from errors in the packet headers. There is also a CRC checker or CRC generator unit to pack the payload data with CRC checksum bits for payload data protection.
- **Pixel/Byte to Byte/Pixel Packing Formats**:
  - Conversion of pixel formats to data bytes in the payload data is done depending on the type of image data supported by the application. It also re-converts the raw data bytes to pixel format understandable to the application layer.
- **Application**:
  - Depending on the type of formats, camera types, capability of the camera used by the transmitter, the application layer recovers the image formats and reproduces the image in the display unit. It also works on de-framing the data into pixel-to-packing formats. High level encoding and decoding of image data is handled in the application unit.

15.5.1 MIPI-CSI-2 Receiver Features

CSI Features:

- Compliant to CSI-2 MIPI specification for Camera Serial Interface (Version 1.00)
- Supports standard D-PHY transceiver compliant to the MIPI Specification
- Supports PHY data programmability up to four lanes.
- Supports PHY data time-out programming.
- Has controls to start and re-start the CSI-2 data transmission for synchronization failures and to support recovery.

- The ISP may not support all the data formats that the CSI-2 receiver can handle.
  —Refer to Table 178 for formats supported by the ISP
- Supports all generic short packet data types.
- Single Image Signal Processor interface for pixel transfers to support multiple image streams for all virtual channel numbers.

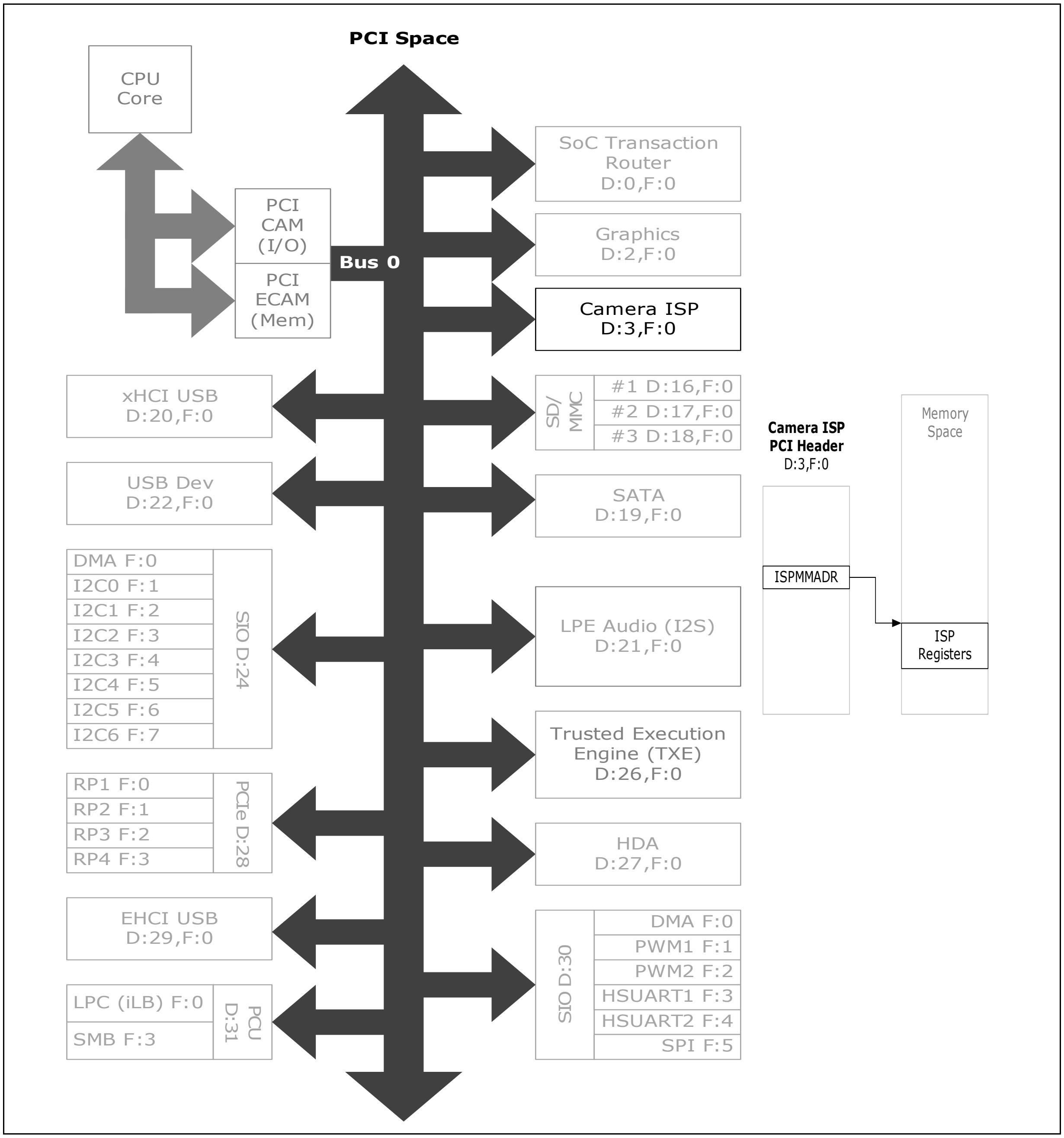
D-PHY Features:

- Supports synchronous transfer in high speed mode with a bit rate of 80-1000Mb/s
- Supports asynchronous transfer in low power mode with a bit rate of 10Mb/s.
- Differential signalling for HS data
- Spaced one-hot encoding for Low Power [LP] data
- Data lanes support transfer of data in high speed as well as low power modes.
- Supports ultra low power mode, escape mode, and high speed mode
- Has a clock divider unit to generate clock for parallel data reception and transmission from and to the PPI unit.
- Activates and disconnects high speed terminators for reception and control mode.
- Activates and disconnects low power terminators for reception and transmission.

15.6 Register Map

Refer to Chapter 3, "Register Access Methods" and Chapter 4, "Mapping Address Spaces" for additional information.

Figure 97. MIPI CSI Register Map



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15.7 Image Signal Processor PCI Configuration Registers

Table 179. Summary of Image Signal Processor PCI Configuration Registers—0/2/0

Offset	Size	Register ID—Description	Default Value
0h	4	"iunit_ID_type (ID)—Offset 0h" on page 1059	0F388086h
4h	4	"iunit_PCICMDSTS_type (PCICMDSTS)—Offset 4h" on page 1059	00100000h
8h	4	"iunit_RIDCC_type (RIDCC)—Offset 8h" on page 1060	04800001h
Ch	4	"iunit_HDR_type (HDR)—Offset Ch" on page 1061	00000000h
10h	4	"iunit_ISPMMADR_type (ISPMMADR)—Offset 10h" on page 1061	00000000h
2Ch	4	"iunit_SSID_type (SSID)—Offset 2Ch" on page 1062	00000000h
34h	4	"iunit_CAPPOINT_type (CAPPOINT)—Offset 34h" on page 1062	00000080h
3Ch	4	"iunit_INTR_type (INTR)—Offset 3Ch" on page 1062	00000000h
80h	4	"iunit_PMCAP_type (PMCAP)—Offset 80h" on page 1063	00229001h
84h	4	"iunit_PMCS_type (PMCS)—Offset 84h" on page 1064	00000000h
90h	4	"iunit_MSI_CAPID_type (MSI_CAPID)—Offset 90h" on page 1064	00000005h
94h	4	"iunit_MSI_ADDRESS_type (MSI_ADDRESS)—Offset 94h" on page 1065	00000000h
98h	4	"iunit_MSI_DATA_type (MSI_DATA)—Offset 98h" on page 1066	00000000h
9Ch	4	"iunit_INTERRUPT_CONTROL_type (INTERRUPT_CONTROL)—Offset 9Ch" on page 1066	00000100h
B0h	4	"iunit_PERF0_type (PERF0)—Offset B0h" on page 1067	00000000h
B4h	4	"iunit_PERF1_type (PERF1)—Offset B4h" on page 1068	00000000h
B8h	4	"iunit_PERF2_type (PERF2)—Offset B8h" on page 1068	00000000h
BCh	4	"iunit_PERF3_type (PERF3)—Offset BCh" on page 1069	00000000h
C0h	4	"iunit_MISR0_type (MISR0)—Offset C0h" on page 1069	FFFFFFFFh
C4h	4	"iunit_MISR1_type (MISR1)—Offset C4h" on page 1070	FFFFFFFFh
C8h	4	"iunit_MISR2_type (MISR2)—Offset C8h" on page 1070	FFFFFFFFh
CCh	4	"iunit_MISR3_type (MISR3)—Offset CCh" on page 1071	FFFFFFFFh
D0h	4	"iunit_MANUFACTURING_ID_type (MANUFACTURING_ID)—Offset D0h" on page 1071	00000000h
D4h	4	"iunit_IUNIT_ACCESS_CTRL_VIOL_type (IUNIT_ACCESS_CTRL_VIOL)—Offset D4h" on page 1071	00000000h
D8h	4	"iunit_IUNIT_DEADLINE_STATUS_type (IUNIT_DEADLINE_STATUS)—Offset D8h" on page 1072	00000000h
DCh	4	"iunit_IUNIT_AFE_HS_CONTROL_type (IUNIT_AFE_HS_CONTROL)—Offset DCh" on page 1073	64000A00h
E0h	4	"iunit_IUNIT_AFE_RCOMP_CONTROL_type (IUNIT_AFE_RCOMP_CONTROL)—Offset E0h" on page 1074	00000000h
E4h	4	"iunit_IUNIT_AFE_TRIM_CONTROL_type (IUNIT_AFE_TRIM_CONTROL)—Offset E4h" on page 1075	00000000h
E8h	4	"iunit_IUNIT_CSI_CONTROL_type (IUNIT_CSI_CONTROL)—Offset E8h" on page 1076	000003F8h
ECh	4	"iunit_IUNIT_DEADLINE_CONTROL_type (IUNIT_DEADLINE_CONTROL)—Offset ECh" on page 1077	040A0100h

Table 179. Summary of Image Signal Processor PCI Configuration Registers—0/2/0

Offset	Size	Register ID—Description	Default Value
F0h	4	"iunit_IUNIT_RCOMP_STATUS_type (IUNIT_RCOMP_STATUS)—Offset F0h" on page 1078	16161616h
F4h	4	"iunit_IUNIT_RCOMP_CONTROL_type (IUNIT_RCOMP_CONTROL)—Offset F4h" on page 1079	00200001h
F8h	4	"iunit_IUNIT_STATUS_type (IUNIT_STATUS)—Offset F8h" on page 1080	0000EB01h
FCh	4	"iunit_IUNIT_CONTROL_type (IUNIT_CONTROL)—Offset FCh" on page 1081	00000103h

15.7.1 iunit_ID_type (ID)—Offset 0h

PCI Device and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits) **ID:** [B:0, D:3, F:0] + 0h

Default: 0F388086h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	1 1 1 1	0 0 1 1	1 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 1 1 0

DIDH	DIDL	VID
31:19	18:16	15:0

Bit Range	Default & Access	Description
31:19	01E7h RO	**DIDH:** DEVICE_IDENTIFICATION_NUMBER_HIGH: Upper bits of ISP Device ID. Connected to straps at IUNIT top level. (Tangier IUNIT Device IDs range from 16'h1178 through 16'h117F. Valleyview IUNIT Device IDs range from 16'h0F38 through 16'h0F3F.)
18:16	000b RO	**DIDL:** DEVICE_IDENTIFICATION_NUMBER_LOW: Lower bits of ISP Device ID. Connected to fuse FB_isp_device_id. (Tangier IUNIT Device IDs range from 16'h1178 through 16'h117F. Valleyview IUNIT Device IDs range from 16'h0F38 through 16'h0F3F.)
15:0	8086h RO	**VID:** VENDOR_IDENTIFICATION_NUMBER: PCI standard identification for Intel.

15.7.2 iunit_PCICMDSTS_type (PCICMDSTS)—Offset 4h

PCI Command and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits) **PCICMDSTS:** [B:0, D:3, F:0] + 4h

Default: 00100000h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

RSVD_31_21	CAP	IS	RSVD_18_11	ID	RSVD_9_3	BME	MSE	RSVD_0_0

Bit Range	Default & Access	Description
31:21	0h RO	**RSVD_31_21:** Reserved
20	1b RO	**CAP:** CAPABILITY_LIST: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list.
19	0b RO	**IS:** INTERRUPT_STATUS: Reflects the state of the interrupt in the camera device. Is set to 1 if IER and IIR are both set. Otherwise is set to 0.
18:11	0h RO	**RSVD_18_11:** Reserved
10	0b RW	**ID:** INTERRUPT_DISABLE: When 1, blocks the sending of ASSERT_INTA and DEASSERT_INTA messages to the Intel Legacy Block (ILB). The interrupt status is not blocked from being reflected in PCICMDSTS.IS. When 0, permits the sending of ASSERT_INTA and DEASSERT_INTA messages to the ILB.
9:3	0h RO	**RSVD_9_3:** Reserved
2	0h RW	**BME:** BUS_MASTER_ENABLE: Enables ISP to function as a PCI compliant master. When 0, blocks the sending of MSI interrupts. When 1, permits the sending of MSI interrupts.
1	0h RW	**MSE:** MEMORY_SPACE_ENABLE: When set, accesses to this device's memory space is enabled. When 1, the ISP will compare the incoming address on the IOSF bus with ISPMMADR(31:22). If there is a match and if the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and present it on the AHB bus. When 0, the ISP will not claim MEMRD or MEMWR IOSF commands.
0	0h RO	**RSVD_0_0:** Reserved

15.7.3 iunit_RIDCC_type (RIDCC)—Offset 8h

Revision Identification and Class Codes

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

RIDCC: [B:0, D:3, F:0] + 8h

Default: 04800001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
BCC								SCC								PI								RID							

Bit Range	Default & Access	Description
31:24	04h RO	**BCC:** BASE_CLASS_CODE: Indicates a multimedia device.
23:16	80h RO	**SCC:** SUB_CLASS_CODE: Indicates other multimedia device.
15:8	0h RO	**PI:** PROGRAMMING_INTERFACE: Default programming interface.
7:0	01h RO	**RID:** REVISION_ID: The value in this field reflects the value of strapRID(7:0) (which is an input pin of ISP) and can be changed with each stepping of the silicon.

15.7.4 iunit_HDR_type (HDR)—Offset Ch

Header Type

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**HDR:** [B:0, D:3, F:0] + Ch

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD_31_24 | MFUNC | HDR | RSVD_15_0

Bit Range	Default & Access	Description
31:24	0h RO	**RSVD_31_24:** Reserved
23	0h RO	**MFUNC:** MULTI_FUNCTION_STATUS: IUNIT is a single function.
22:16	0h RO	**HDR:** HEADER_CODE: Indicates a type 0 header format.
15:0	0h RO	**RSVD_15_0:** Reserved

15.7.5 iunit_ISPMMADR_type (ISPMMADR)—Offset 10h

Memory Mapped Address Range. This is the base address for all memory mapped registers.

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**ISPMMADR:** [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

BA | RSVD_21_0

Bit Range	Default & Access	Description
31:22	0h RW	**BA:** BASE_ADDRESS: Set by the OS, these bits correspond to address signals (31:22). The ISP will compare the IOSF address (31:22) with ISPMMADR(31:22). If there is a match, and PCICMDSTS(1) = MSE = 1 and the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and present it on the AHB bus to the vendor IP.

Bit Range	Default & Access	Description
21:0	0h RO	**RSVD_21_0:** Reserved

15.7.6 iunit_SSID_type (SSID)—Offset 2Ch

Subsystem Identifiers

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

SSID: [B:0, D:3, F:0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															SSID																

Bit Range	Default & Access	Description
31:0	0h RO	**SSID:** SUBSYSTEM_IDENTIFIERS: The value in this field is a copy of the SSID register programmed by the graphics device driver or BIOS in the Device 0/2/0 PCI header. To change the subsystem ID, write to Device 0/2/0 SSID instead of to this SSID.

15.7.7 iunit_CAPPOINT_type (CAPPOINT)—Offset 34h

Capabilities Pointer

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

CAPPOINT: [B:0, D:3, F:0] + 34h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
											RSVD_31_8																CAP				

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD_31_8:** Reserved
7:0	80h RO	**CAP:** CAPABILITIES_POINTER: The first item in the capabilities list is at address 80h.

15.7.8 iunit_INTR_type (INTR)—Offset 3Ch

Interrupt. This register is programmed by SBIOS.

Access Method

Type: PCI Configuration Register (Size: 32 bits) **INTR:** [B:0, D:3, F:0] + 3Ch

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD_31_16				IPIN		ILIN	

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD_31_16:** Reserved
15:8	0h RO	**IPIN:** INTERRUPT_PIN: PCI Device 0/3/0 (IUNIT) is a single function device. If INTx is used, the PCI spec requires that it use INTA#. If INTx is used (FB_intx_supported fuse is 1), then this field is hard coded to 01h. If INTx is not used (FB_intx_supported fuse is 0), this field is hard coded to 00h.
7:0	0h RW	**ILIN:** INTERRUPT_LINE: BIOS written value to communicate interrupt line routing information to the ISP device driver.

15.7.9 iunit_PMCAP_type (PMCAP)—Offset 80h

Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 32 bits) **PMCAP:** [B:0, D:3, F:0] + 80h

Default: 00229001h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 1 0	0 0 1 0	1 0 0 1	0 0 0 0	0 0 0 0	0 0 0 1

Field	Bits
PMES	31:27
D2S	26
D1S	25
RSVD_24_22	24:22
DSI	21
RSVD_20_19	20:19
VS	18:16
NEXT_CAP	15:8
CAPID	7:0

Bit Range	Default & Access	Description
31:27	0h RO	**PMES:** PME_SUPPORT: The camera controller does not generate PME#.
26	0h RO	**D2S:** D2_SUPPORT: The D2 power management state is not supported.
25	0h RO	**D1S:** D1_SUPPORT: The D1 power management state is not supported.
24:22	0h RO	**RSVD_24_22:** Reserved

Bit Range	Default & Access	Description
21	01h RO	**DSI:** DEVICE_SPECIFIC_INITIALIZATION: Hardwired to 1 to indicate that special initialization of the camera controller is required before generic class device driver is to use it.
20:19	0h RO	**RSVD_20_19:** Reserved
18:16	2h RO	**VS:** VERSION: Indicates compliance with revision 1.1 of the PCI Power Management Specification.
15:8	90h RO	**NEXT_CAP:** POINTER_TO_NEXT_CAPABILITY: Indicates the next item in the capabilities list.
7:0	01h RO	**CAPID:** CAPABILITIES: SIG defines this ID is 01h for power management.

15.7.10 iunit_PMCS_type (PMCS)—Offset 84h

Power Management Control/Status.

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

PMCS: [B:0, D:3, F:0] + 84h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD_31_2																														PS	

Bit Range	Default & Access	Description
31:2	0h RO	**RSVD_31_2:** Reserved
1:0	0h RW	**PS:** POWER_STATE: Power management is implemented by writing to control registers in the PUNIT. This field may be programmed by the software driver, but no action is taken based on writing to this field.

15.7.11 iunit_MSI_CAPID_type (MSI_CAPID)—Offset 90h

Message Signaled Interrupts Capability ID and Control Register

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

MSI_CAPID: [B:0, D:3, F:0] + 90h

Default: 00000005h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
RSVD_31_24								C64	MME			MMC			MSIE	NEXT_CAP								CAPID							

Bit Range	Default & Access	Description
31:24	0h RO	**RSVD_31_24:** Reserved
23	0h RO	**C64:** 64_BIT_ADDRESS_CAPABLE: 32-bit capable only.
22:20	0h RW	**MME:** MULTIPLE_MESSAGE_ENABLE: This field is RW for software compatibility, but only a single message is ever generated.
19:17	0h RO	**MMC:** MULTIPLE_MESSAGE_CAPABLE: This device is only single message capable.
16	0h RW	**MSIE:** MSI_ENABLE: If set, MSI is enabled. PCICMDSTS.BME must be set for an MSI to be generated.When 0, blocks the sending of a MSI interrupt. The interrupt status is not blocked from being reflected in the PCICMDSTS.IS bit. When 1, permits sending of a MSI interrupt.
15:8	0h RO	**NEXT_CAP:** POINTER_TO_NEXT_CAPABILITY: Indicates this is the last item in the list.
7:0	05h RO	**CAPID:** CAPABILITY_ID: Indicates an MSI capability.

15.7.12 iunit_MSI_ADDRESS_type (MSI_ADDRESS)—Offset 94h

MSI Message Address

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

MSI_ADDRESS: [B:0, D:3, F:0] + 94h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MA																														RSVD_1_0	

Bit Range	Default & Access	Description
31:2	0h RW	**MA:** MSI_ADDRESS: System specified message address, always DW aligned. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the memory address used is 12xFEE, MSI_ADDRESS[19:0].
1:0	0h RO	**RSVD_1_0:** Reserved

15.7.13 iunit_MSI_DATA_type (MSI_DATA)—Offset 98h

MSI Message Data

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

MSI_DATA: [B:0, D:3, F:0] + 98h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD_31_16 | MD

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD_31_16:** Reserved
15:0	0h RW	**MD:** MSI_DATA: This 16-bit field is programmed by system software and is driven onto the lower word of data during the data phase of the MSI write transaction. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the write data corresponds to the value of this field.

15.7.14 iunit_INTERRUPT_CONTROL_type (INTERRUPT_CONTROL)—Offset 9Ch

INTERRUPT_CONTROL

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

INTERRUPT_CONTROL: [B:0, D:3, F:0] + 9Ch

Default: 00000100h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 0 0 0

RSVD_31_25 | IER | RSVD_23_17 | IIR | RSVD_15_9 | IMR | RSVD_7_1 | ISR

Bit Range	Default & Access	Description
31:25	0h RO	**RSVD_31_25:** Reserved

Bit Range	Default & Access	Description
24	0h RW	**IER:** IER: This is an enable bit that allows the sending of an interrupt to the CPU using either MSI or INTR mechanisms. The interrupt is sent immediately to the CPU. The firmware running on the ISP guarantees ordering by reading the last data write from memory before raising the interrupt. 1 = If MSI_ENABLE is set, then an MSI is sent to the CPU when the IIR bit is set, or if the IIR bit remains set after software writes to this register. If INTERRUPT_DISABLE is not set, then an ASSERT_INTA message is sent to the Intel Legacy Block (ILB) when the IIR bit is set by hardware, or if the IIR bit remains set after software writes to this register. If software clears the IIR bit, and INTERRUPT_DISABLE is not set then a DEASSERT_INTA message is sent to the ILB. 0 = Do not generate an MSI even if the MSI_ENABLE bit is set. Do not send ASSERT_INTA or DEASSERT_INTA messages to the ILB even if the INTERRUPT_DISABLE bit is not set.
23:17	0h RO	**RSVD_23_17:** Reserved
16	0h RW/1C	**IIR:** IIR: This is the persistent value of the interrupt bit. It is set by hardware, and cleared by software. Software must write a 1 to clear this bit. Writing a 0 is a NOP. If both software and hardware attempt to write to this field in the same clock cycle, hardware wins. 1 = An interrupt was received from the vendor IP when the IMR bit was not set, and software has not yet cleared it. 0 = There is no pending interrupt.
15:9	0h RO	**RSVD_15_9:** Reserved
8	1b RW	**IMR:** IMR: Interrupt Mask bit. 1 = IIR bit will not be set when the ISR bit is set. 0 = IIR bit will be set when the ISR bit is set.
7:1	0h RO	**RSVD_7_1:** Reserved
0	0h RO	**ISR:** ISR: Reflects the state of the interrupt line from the vendor IP, after it is synchronized to the czclk domain.

15.7.15 iunit_PERF0_type (PERF0)—Offset B0h

Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PERF0: [B:0, D:3, F:0] + B0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRIFLO

Bit Range	Default & Access	Description
31:0	0h RW/SE	**CRIFLO:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 31:0 of the cumulative_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will enable all four counters.

15.7.16 iunit_PERF1_type (PERF1)—Offset B4h

Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PERF1: [B:0, D:3, F:0] + B4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRIFHI (bits 31:0)

Bit Range	Default & Access	Description
31:0	0h RW/SE	**CRIFHI:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 63:32 of the cumulative_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will disable all four counters.

15.7.17 iunit_PERF2_type (PERF2)—Offset B8h

Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PERF2: [B:0, D:3, F:0] + B8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ACLO (bits 31:0)

Bit Range	Default & Access	Description
31:0	0h RW/SE	**ACLO:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 31:0 of the active_cycles counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear all four counters. The counters should only be cleared after they are disabled.

15.7.18 iunit_PERF3_type (PERF3)—Offset BCh

Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**PERF3:** [B:0, D:3, F:0] + BCh

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD_31_27	MRIF	ACHI

Bit Range	Default & Access	Description
31:27	0h RO	**RSVD_31_27:** Reserved
26:16	0h RW/SE	**MRIF:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 11:0 of the max_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear the max_reads_in_flight counters only. The counters should only be cleared after they are disabled.
15:0	0h RW/SE	**ACHI:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 47:32 of the active_cycles counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear the max_reads_in_flight counters only. The counters should only be cleared after they are disabled.

15.7.19 iunit_MISR0_type (MISR0)—Offset C0h

OCP Master Write Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**MISR0:** [B:0, D:3, F:0] + C0h

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MISR0																															

Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW/C	**MISR0:** MISR0: Write to this register address clears this MISR. This is a 8:1 compression MISR capturing the 256-bit write data on the OCP interface between ISP_CSS and Iunit wrapper.

15.7.20 iunit_MISR1_type (MISR1)—Offset C4h

OCP Master Read Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MISR1: [B:0, D:3, F:0] + C4h

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MISR1																															

Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW/C	**MISR1:** MISR1: Write to this register address clears this MISR. This is a 8:1 compression MISR capturing the 256-bit read return data on the OCP interface between ISP_CSS and Iunit wrapper.

15.7.21 iunit_MISR2_type (MISR2)—Offset C8h

OCP Master Address and Control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MISR2: [B:0, D:3, F:0] + C8h

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MISR2																															

Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW/C	**MISR2:** MISR2: Write to this register address clears this MISR. This is a 4:1 compression MISR capturing the control signals on the OCP Master port in the Iunit.

15.7.22 iunit_MISR3_type (MISR3)—Offset CCh

Scalar Processor output

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**MISR3:** [B:0, D:3, F:0] + CCh

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

MISR3

Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW/C	**MISR3:** MISR3: Write to this register address clears this MISR. This is a 4:1 compression MISR capturing the output signals of the Scalar Processor.

15.7.23 iunit_MANUFACTURING_ID_type (MANUFACTURING_ID)—Offset D0h

Manufacturing ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**MANUFACTURING_ID:** [B:0, D:3, F:0] + D0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD_31_24 | MID

Bit Range	Default & Access	Description
31:24	0h RO	**RSVD_31_24:** Reserved
23:0	0h RO	**MID:** MANUFACTURING_ID: Hardwired to strapMANID(23:0).

15.7.24 iunit_IUNIT_ACCESS_CTRL_VIOL_type (IUNIT_ACCESS_CTRL_VIOL)—Offset D4h

IUNIT Access control violation register

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**IUNIT_ACCESS_CTRL_VIOL:** [B:0, D:3, F:0] + D4h

Default: 00000000h

31	30:21	20	19	18:15	14:8	7	6:0
0	0 0 0 0 0 0 0 0 0 0	0	0	0 0 0 0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0
EN_INTR_ACCESS_CTRL_VIOL	RSVD_30_21	SAI_VIOL	MULTIPLE_SAI_VIOL	RSVD_18_15	VIOL_SAI	RSVD_7_7	INITIAL_SAI

Bit Range	Default & Access	Description
31	0b RW	**EN_INTR_ACCESS_CTRL_VIOL:** Enable Interrupt on access control violation: When set, the IUNIT will latch violation information into this register and send an interrupt request (opcode 0XEE) and (port 0x04) to the PUNIT.
30:21	00h RO	**RSVD_30_21:** Reserved
20	0b RW	**SAI_VIOL:** SAI_VIOL: If set, the IUNIT has detected an SAI violation and has captured the status in this register. This bit must be cleared by software in order for IUNIT to capture the next violation.
19	0b RW	**MULTIPLE_SAI_VIOL:** If set, more than one SAI violation has been detected in the IUNIT. Status for the 1st violation has been captured in this register. It is recommend that software clear this bit whenever it clears bit[20] of this register.
18:15	0h RO	**RSVD_18_15:** Reserved
14:8	00h RW	**VIOL_SAI:** VIOL_SAI: SAI bits that triggered the violation: This 7-bit value indicates the SAI of the subsequent transaction which caused the violation.
7	0b RO	**RSVD_7_7:** Reserved
6:0	00h RW	**INITIAL_SAI:** INITIAL_SAI: This 7-bit value indicates the SAI of the initial transaction for SAI mismatch error codes.

15.7.25 iunit_IUNIT_DEADLINE_STATUS_type (IUNIT_DEADLINE_STATUS)—Offset D8h

IUNIT Deadline Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_DEADLINE_STATUS: [B:0, D:3, F:0] + D8h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:30	Bits 29:11	Bits 10:0
SDRAM_WAKEUP_PSTATE	DN	GT

Bit Range	Default & Access	Description
31:30	0h RO	**SDRAM_WAKEUP_PSTATE:** SDRAM_WAKEUP_PSTATE: State of the SDRAM_WAKEUP state machine. 00b = State machine is idle; 01b = sdram_wakeup seen, waiting for all memory transactions in flight to complete; 10b = All memory transactions are completed, waiting for acknowledgement from czclk domain before returning to idle state;
29:11	0h RO	**DN:** DN: Computed deadline value to be send with the next request on IB PFI bus. This is the internal deadline value. The actual deadline that is sent on the IB PFI bus is the maximum of GT+MDD or DN.
10:0	0h RO	**GT:** GT: Current value of Global Timer

15.7.26 iunit_IUNIT_AFE_HS_CONTROL_type (IUNIT_AFE_HS_CONTROL)—Offset DCh

High-speed termination control MIPI CSI DPHY

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_AFE_HS_CONTROL: [B:0, D:3, F:0] + DCh

Default: 64000A00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

Bits 31:24	Bits 23:22	Bits 21:20	Bits 19:18	Bits 17:16	Bits 15:8	Bits 7:0
HS_CLK_UNGATE_DLY	RSVD_23_22	CSI3_CLK_HS_TERM_OVRD	CSI2_CLK_HS_TERM_OVRD	CSI1_CLK_HS_TERM_OVRD	HS_CLK_EN_DLY	HS_DATA_EN_DLY

Bit Range	Default & Access	Description
31:24	64h RW	**HS_CLK_UNGATE_DLY:** HS_CLK_UNGATE_DLY: Delay between the assertion of HS enable and the ungating of the HS clocks going to the DPHY logic for all clock lanes. HS clocks are gated by default and are ungated after Tclk-settle time. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x64 indicating 200 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.
23:22	0h RW	**RSVD_23_22:** Reserved
21:20	00b RW	**CSI3_CLK_HS_TERM_OVRD:** CSI3_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI3 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
19:18	00b RW	**CSI2_CLK_HS_TERM_OVRD:** CSI2_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI2 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
17:16	00b RW	**CSI1_CLK_HS_TERM_OVRD:** CSI1_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI1 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
15:8	0Ah RW	**HS_CLK_EN_DLY:** HS_CLK_EN_DLY: Delay between the assertion of HS termination enable and the assertion of HS enable for all clock lanes. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x0A indicating 20 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.
7:0	0h RW	**HS_DATA_EN_DLY:** HS_DATA_EN_DLY: Delay between the assertion of HS termination enable and the assertion of HS enable for all data lanes. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x0 indicating 0 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.

15.7.27 iunit_IUNIT_AFE_RCOMP_CONTROL_type (IUNIT_AFE_RCOMP_CONTROL)—Offset E0h

AFE RCOMP control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_AFE_RCOMP_CONTROL: [B:0, D:3, F:0] + E0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD_31_16																RSVD_15_9							ICSI_RCOMPSTATICLEGDIS	RSVD_7_4				ICSI_RCOMPTARGET			

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD_31_16:** Reserved
15:9	0h RW	**RSVD_15_9:** Reserved
8	0b RW	**ICSI_RCOMPSTATICLEGDIS:** ICSI_RCOMPSTATICLEGDIS: Disable RCOMP static leg in AFE
7:4	0h RW	**RSVD_7_4:** Reserved
3:0	0h RW	**ICSI_RCOMPTARGET:** ICSI_RCOMPTARGET: RCOMP target level range is 70ohm to 130ohm differential impedance. 0000b = 50ohms; 0001b = 30ohms; 0010b = 35ohms; 0011b = 40ohms; 0100b = 45ohms; 0101b = 55ohms; 0110b = 60ohms; 0111b = 65ohms;

15.7.28 iunit_IUNIT_AFE_TRIM_CONTROL_type (IUNIT_AFE_TRIM_CONTROL)—Offset E4h

Configurable delay for CSI AFE data/clk lanes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_AFE_TRIM_CONTROL: [B:0, D:3, F:0] + E4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICSI3_HSRXCLKTRIM				ICSI2_HSRXCLKTRIM				ICSI2_HSRXDATATRIM				ICSI1_HSRXCLKTRIM				ICSI1_HSRXDATATRIM															

Bit Range	Default & Access	Description
31:28	0h RW	**ICSI3_HSRXCLKTRIM:** ICSI3_HSRXCLKTRIM: Delay for CSI3 clock lane. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.

Bit Range	Default & Access	Description
27:24	0h RW	**ICSI2_HSRXCLKTRIM:** ICSI2_HSRXCLKTRIM: Delay for CSI2 clock lane. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.
23:20	0h RW	**ICSI2_HSRXDATATRIM:** ICSI2_HSRXDATATRIM: Delay for CSI2 data lane. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.
19:16	0h RW	**ICSI1_HSRXCLKTRIM:** ICSI1_HSRXCLKTRIM: Delay for CSI1 clock lane. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.
15:0	0h RW	**ICSI1_HSRXDATATRIM:** ICSI1_HSRXDATATRIM: Delay for CSI1 data lanes. Refer to the CSI AFE Circuit Architecture Spec (CAS) for the actual delays for each trim value setting.

15.7.29 iunit_IUNIT_CSI_CONTROL_type (IUNIT_CSI_CONTROL)—Offset E8h

Control register for MIPI-CSI

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_CSI_CONTROL: [B:0, D:3, F:0] + E8h

Default: 000003F8h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0

Fields (bit 31 to bit 0): RSVD_31_20, CSI_PORTCONFIG, RSVD_15_10, CSI3_ACTIVE_LANES, CSI2_ACTIVE_LANES, CSI1_ACTIVE_LANES, CSI3_DISABLE, CSI2_DISABLE, CSI1_DISABLE

Bit Range	Default & Access	Description
31:20	0h RW	**RSVD_31_20:** Reserved
19:16	0h RW	**CSI_PORTCONFIG:** CSI_PORTCONFIG: Used to enable the CSI data lanes to CSI ports if FB_csi_portconfig_override fuse is set. This field is ignored if FB_csi_portconfig_override fuse is clear.
15:10	0h RW	**RSVD_15_10:** Reserved
9:8	11b RW	**CSI3_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI3 interface. 1=active, 0=inactive.
7	1b RW	**CSI2_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI2 interface. 1=active, 0=inactive.
6:3	1111b RW	**CSI1_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI1 interface. 1=active, 0=inactive.
2	0b RW	**CSI3_DISABLE:** 1 = Disable MIPI CSI3 interface. 0 = Enable MIPI CSI3 interface if FB_csi_portdisable[2] fuse is cleared

Bit Range	Default & Access	Description
1	0b RW	**CSI2_DISABLE:** 1 = Disable MIPI CSI2 interface. 0 = Enable MIPI CSI2 interface if FB_csi_portdisable[1] fuse is cleared
0	0b RW	**CSI1_DISABLE:** 1 = Disable MIPI CSI1 interface. 0 = Enable MIPI CSI1 interface if FB_csi_portdisable[0] fuse is cleared

15.7.30 iunit_IUNIT_DEADLINE_CONTROL_type (IUNIT_DEADLINE_CONTROL)—Offset ECh

IUNIT Deadline Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_DEADLINE_CONTROL: [B:0, D:3, F:0] + ECh

Default: 040A0100h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3	2	1:0
Default	0 0 0 0	0 1 0 0	0 0 0 0	1 0 1 0	0 0 0 0	0 0 0 1	0 0 0 0	0	0	0 0
Field	FDD		DI		RSVD_15_12	MDD	RSVD_7_4	IGNORE_WAKEUP	DIS_GTP64_CHK	DS

Bit Range	Default & Access	Description
31:24	04h RW	**FDD:** FIRST_DEADLINE_DELAY: Delay between the rising edge of WAKEUP signal and the fake deadline that will be specified for the first request of that line. Unit in 250 nsec. Reset value of 8'h04 indicates FDD = 1 usec.
23:16	0Ah RW	**DI:** DEADLINE_INCREMENT: Difference in deadline times between adjacent requests. If the current request is for 32B, the next deadline will be DI more than the current deadline. If the current request is for 64B, the next deadline will be 2*DI more than the current deadline. Unit in 1/1024 usec. Reset value of 8'h0A indicates DI = 9.765625 nsec.
15:12	0h RW	**RSVD_15_12:** Reserved
11:8	1h RW	**MDD:** MINIMUM_DEADLINE_DELAY: Minimum separation between current Global Timer value and the deadline specified with any request on the PFI interface. Unit is 250 nsec. Reset value of 4'h1 indicates MDD = 250 nsec.
7:4	0h RW	**RSVD_7_4:** Reserved
3	0b RW	**IGNORE_WAKEUP:** If clear, then after each rising edge of sdram_wakeup, the OCP master interface is stalled until all reads in flight and all FIFOs are empty and then the next deadline is set to GT + FDD. If set, the sdram_wakeup signal from ISP_CSS is ignored.
2	0b RW	**DIS_GTP64_CHK:** If clear, then the PFI interface is stalled whenever the next deadline value exceeds GT + 64 usec. This check is a safety measure to make sure that deadline does not drift too far into the future. If set, this check is not performed.

Bit Range	Default & Access	Description
1:0	0h RW	**DS:** DEADLINE_SCHEME: 11b = Reserved; 10b = Reserved; 01b = When WAKEUP is asserted, FDD is added to the current global timer to compute DN. With each request, the deadline sent to Pondicherry is either DN, or the sum of the global timer and MDD, whichever is larger. After each request is sent, DN is computed by adding DI for each 32Byte request sent to either DN or the sum of the global timer and MDD, whichever is larger. Each clock cycle, DN is checked to make sure it is greater than the current global timer, else it is set to the global timer.; 00b = When WAKEUP is asserted, FDD is added to the current global timer to compute DN. With each request, the deadline sent to Pondicherry is either DN, or the sum of the global timer and MDD, whichever is larger. After each request is sent, DN is computed by adding DI for each 32Byte request sent to DN. Each cycle, DN is checked to make sure that it is either greater than the current global timer, or is less than the global timer by no more than 64 usec, else it is set to the global timer minus 64 usec.

15.7.31 iunit_IUNIT_RCOMP_STATUS_type (IUNIT_RCOMP_STATUS)—Offset F0h

IUNIT RCOMP Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_RCOMP_STATUS: [B:0, D:3, F:0] + F0h

Default: 16161616h

31	30:24	23	22:16	15	14:8	7	6:0
0	0 0 1 0 1 1 0	0	0 0 1 0 1 1 0	0	0 0 1 0 1 1 0	0	0 0 1 0 1 1 0
CALIB_EXIT_TOGGLE_LIMIT	CSI3_RCOMP_UPDATE_VALUE	CALIB_EXIT_0101	CSI2_RCOMP_UPDATE_VALUE	CALIB_EXIT_1010	CSI1_RCOMP_UPDATE_VALUE	CALIB_EXIT_ERROR	CSI_RCOMP_CALIBRATION_VALUE

Bit Range	Default & Access	Description
31	0b RO	**CALIB_EXIT_TOGGLE_LIMIT:** CALIB_EXIT_TOGGLE_LIMIT: If set, indicates that the last calibration cycle exited because the number of toggles matched the value specified by the CSI_HS_ROGGLE_LIMIT_CREG_ENC field of the IUNIT_RCOMP_CONTROL register.
30:24	16h RO	**CSI3_RCOMP_UPDATE_VALUE:** MIPI CSI3 RCOMP value: Current RCOMP value on MIPI CSI3 port
23	0b RO	**CALIB_EXIT_0101:** CALIB_EXIT_0101: If set, indicates that the last calibration cycle exited because the last four states of rcompcountup were 0101
22:16	16h RO	**CSI2_RCOMP_UPDATE_VALUE:** MIPI CSI2 RCOMP value: Current RCOMP value on MIPI CSI2 port
15	0b RO	**CALIB_EXIT_1010:** CALIB_EXIT_1010: If set, indicates that the last calibration cycle exited because the last four states of rcompcountup were 1010

Bit Range	Default & Access	Description
14:8	16h RO	**CSI1_RCOMP_UPDATE_VALUE:** MIPI CSI1 RCOMP value: Current RCOMP value on MIPI CSI1 port
7	0b RO	**CALIB_EXIT_ERROR:** CALIB_EXIT_ERROR: If set, indicates that the last calibration cycle exited due to an error condition.
6:0	16h RO	**CSI_RCOMP_CALIBRATION_VALUE:** MIPI CSI RCOMP value from last calibration cycle

15.7.32 iunit_IUNIT_RCOMP_CONTROL_type (IUNIT_RCOMP_CONTROL)—Offset F4h

MIPI CSI RCOMP control register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_RCOMP_CONTROL: [B:0, D:3, F:0] + F4h

Default: 00200001h

Bits	31:24	23	22:21	20:19	18:16	15:11	10	9	8	7:1	0
Value	0 0 0 0 0 0 0 0	0	0 1	0 0	0 0 0	0 0 0 0 0	0	0	0	0 0 0 0 0 0 0	1
Field	RSVD_31_24	CSI_HS_OVR_CLK_GATE_ON_UPDATE	CSI_HS_RCOMP_UPDATE_MODE	CSI_HS_TOGGLE_LIMIT_CREG_ENC	CSI_HS_CALIB_LOOP_DELAY	RSVD_15_11	CSI3_HS_RCOMP_OVR_ENABLE	CSI2_HS_RCOMP_OVR_ENABLE	CSI1_HS_RCOMP_OVR_ENABLE	CSI_HS_RCOMP_OVR_CODE	CSI_HS_RCOMP_ENABLE

Bit Range	Default & Access	Description
31:24	0h RW	**RSVD_31_24:** Reserved
23	0b RW	**CSI_HS_OVR_CLK_GATE_ON_UPDATE:** CSI_HS_OVR_CLK_GATE_ON_UPDATE: If cleared, the high speed clock going to the digital logic is gated when RCOMP update is happening. The clock is gated for a minimum of 100 nsec. If this bit is set, then the high speed clock is not gated during the update cycle.
22:21	01b RW	**CSI_HS_RCOMP_UPDATE_MODE:** CSI_HS_RCOMP_UPDATE_MODE: 00b = RCOMP is updated if the clock lane is in LP11 state. 01b = RCOMP is updated if all the data lanes are in LP11 state. 10b = RCOMP is updated immediately after calibration is completed, or the CSI[1-3]_HS_RCOMP_OVR_ENABLE bits are written to 1 by software. 11b = Reserved.
20:19	0h RW	**CSI_HS_TOGGLE_LIMIT_CREG_ENC:** CSI_HS_TOGGLE_LIMIT_CREG_ENC: HS state machine toggle limit. Number of times RCOMP state machine will toggle before exiting. 2'b00: 6 toggles; 2'b01: 4 toggles; 2'b10: 8 toggles; 2'b11: 10 toggles;

Bit Range	Default & Access	Description
18:16	0h RW	**CSI_HS_CALIB_LOOP_DELAY:** CSI_HS_CALIB_LOOP_DELAY: Delay after applying a new RCOMP value to the AFE, before sampling the count up/down input from the AFE. 0h=)50-53ns; 1h=)60ns; 2h=)70-72ns; 3h=)80-83ns; 4h=)90ns; 5h=)100-102ns; 6h=)125-128ns; 7h=)150ns. At the start of each RCOMP calibration cycle, the state machine waits for 8x this delay before starting to sample the count up/down signal.
15:11	0h RW	**RSVD_15_11:** Reserved
10	0b RW	**CSI3_HS_RCOMP_OVR_ENABLE:** CSI3_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 3. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 3.
9	0b RW	**CSI2_HS_RCOMP_OVR_ENABLE:** CSI2_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 2. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 2.
8	0b RW	**CSI1_HS_RCOMP_OVR_ENABLE:** CSI1_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 1. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 1.
7:1	0h RW	**CSI_HS_RCOMP_OVR_CODE:** CSI_HS_RCOMP_OVR_CODE: Software defined value to use as the RCOMP value for CSI[1-3] ports if the CSI[1-3]_HS_RCOMP_OVR_ENABLE fields are set.
0	1b RW	**CSI_HS_RCOMP_ENABLE:** CSI_HS_RCOMP_ENABLE: Enable CSI HS RCOMP. (Note: This bit does not affect the initial RCOMP at the de-assertion of reset which is controlled by the fuse FB_disable_initial_RCOMP.)

15.7.33 iunit_IUNIT_STATUS_type (IUNIT_STATUS)—Offset F8h

IUNIT Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_STATUS: [B:0, D:3, F:0] + F8h

Default: 0000EB01h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0	0	1

Fields: RSVD_31_18 | ISCLK | CZCLK | RSVD_7_7 | TCGSM | RSVD_3_3 | LCGSM | ISP_BUSY

Bit Range	Default & Access	Description
31:18	0h RO	**RSVD_31_18:** Reserved
17:13	07h RO	**ISCLK:** Reflects the value of cck_isp_isclk_ratio_zcznfwh input pin.
12:8	0Bh RO	**CZCLK:** Reflects the value of cck_xxx_czclk_ratio_zcznfwh input pin.

Bit Range	Default & Access	Description
7	0b RO	**RSVD_7_7:** Reserved
6:4	0h RO	**TCGSM:** ISP trunk clock gating state machine. 0h = RUN_TRUNK_CLK; 1h = STOP_TRUNK_CLK; 2h = WAIT_FOR_RESUME; 3h = START_TRUNK_CLK; 4h = WAIT_FOR_LOCAL_CLK_TO_START. The reset value will be RUN_TRUNK_CLK. If the FB_override_initial_clock_gating fuse is not set, then shortly after reset, the value of this register will automatically change to STOP_TRUNK_CLK.
3	0b RO	**RSVD_3_3:** Reserved
2:1	0h RO	**LCGSM:** ISP local clock gating state machine. 0h = RUN_LOCAL_CLK; 1h = WAIT_FOR_FIFO_EMPTY; 2h = STOP_LOCAL_CLK. The reset value will be RUN_LOCAL_CLK. If the FB_override_initial_clock_gating fuse is not set, then shortly after reset, the value of this register will automatically change to STOP_LOCAL_CLK.
0	1b RO	**ISP_BUSY:** ISP_BUSY: 1 = ISP is busy; 0 = ISP is idle.

15.7.34 iunit_IUNIT_CONTROL_type (IUNIT_CONTROL)—Offset FCh

IUNIT Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IUNIT_CONTROL: [B:0, D:3, F:0] + FCh

Default: 00000103h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1
FUNTION_DISABLE_CFG	FUNCTION_DISABLE_MMIO	RSVD_29_29	PERF_MASK					RSVD_23_22		DISABLE_ISM_IDLE_FREEZE	DISABLE_OCP_PHASE_ORDERING	ICACHE_CMD_WEIGHT	THERM_MASK			MID								RCOMPCLK_GATING_DISABLE	ISPCLK_GATING_DISABLE		DDMA	SRSE		IBEWC	IBERC

Bit Range	Default & Access	Description
31	0b RW	**FUNTION_DISABLE_CFG:** FUNCTION_DISABLE_CFG: When set, the IUNIT stops accepting any new Configuration cycle requests on the IOSF Primary bus including any new configuration cycle requests to clear this bit. Both legacy and MSI interrupts are disabled as well.
30	0b RW	**FUNCTION_DISABLE_MMIO:** FUNCTION_DISABLE_MMIO: When set, the IUNIT stops accepting any new MMIO access requests on the IOSF Primary bus.
29	0b RW	**RSVD_29_29:** Reserved

Bit Range	Default & Access	Description
28:24	0h RW	**PERF_MASK:** PERF_MASK: This field determines the amount of performance throttling applied to ispclk. The value of this field determines how many beat periods of ispclk are killed, where a beat period is defined as 16 ispclk cycles. A 16 cycle period was chosen to make the throttling independent of the actual clock ratio between ispclk and coreclk. Note that clock gating should be enabled when thermal throttling is enabled.
23:22	0h RW	**RSVD_23_22:** Reserved
21	0h RW	**DISABLE_ISM_IDLE_FREEZE:** DISABLE_ISM_IDLE_FREEZE: When IUNIT receive a RESET_WARN message from PUNIT, it will freeze the IOSF primary Idle State Machine (among other things), before sending an OK_TO_RESET message to PUNIT. If the DISABLE_ISM_IDLE_FREEZE bit is set, IUNIT will not freeze the ISM in the IDLE state as part of this reset sequence.
20	0h RW	**DISABLE_OCP_PHASE_ORDERING:** DISABLE_OCP_PHASE_ORDERING: By default, IUNIT will follow the OCP phase ordering protocol and wait until a write command is accepted before accepting the write data corresponding to that command. If the DISABLE_OCP_PHASE_ORDERING bit is set, the IUNIT wrapper will accept the write data independent of the write command.
19	0h RW	**ICACHE_CMD_WEIGHT:** ICACHE_CMD_WEIGHT: 0b = Requests from the OCP master port sending Icache miss traffic will win arbitration over requests from the OCP master port that sends pixel data traffic. 1b = Requests from the two OCP master interfaces will be accepted in a round robin fashion.
18:16	0h RW	**THERM_MASK:** THERM_MASK: This field determines the amount of thermal throttling applied to ispclk. The value of this field determines how many beat periods of ispclk are killed, where a beat period is defined as 16 ispclk cycles. A 16 cycle period was chosen to make the throttling independent of the actual clock ratio between ispclk and coreclk. 000 = No throttling; 001 = 12.5% throttling; 010 = 25% throttling; 011 = 37.5% throttling; 100 = 50% throttling; 101 = 62.5% throttling; 110 = 75% throttling; 111 = 87.5% throttling;
15:8	01h RW	**MID:** MIN_IDLE_DELAY: Minimum wait time after the rising edge of idle, before the clock gating state machine will start the sequence to gate ispclk. Range is 0 to 130 usec. Unit is 0.512 usec. Reset value of 8'h1 indicates MID = 0.512 usec.
7	0b RW	**RCOMPCLK_GATING_DISABLE:** 1 = Disable clock gating for rcompclk. 0 = Enable clock gating for rcompclk. Note: All clock gating is disabled by hardware while reset is asserted, regardless of the state of this field.
6:5	00b RW	**ISPCLK_GATING_DISABLE:** ISPCLK_GATING_DISABLE: 11 = Disable local clock gating and trunk clock gating for ispclk.; 10 = Enable local clock gating for ispclk, but disable trunk clock gating.; 01 = Reserved; 00 = Enable local clock gating and trunk clock gating for ispclk. Note: All clock gating is disabled by hardware while reset is asserted, regardless of the state of this field.
4	0b RW	**DDMA:** 1 = Disable DMA. Stop sending any requests on the IB PFI port. 0 = Enable DMA. IB PFI port operates normally.
3:2	0h RW	**SRSE:** SOFT_RESET_SEQUENCE_ENABLE: If SRSE=2b00: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will a) stop accepting requests on the IOSF primary interface, b) stop accepting new requests from the OCP master interface, c) wait until read data from all earlier read requests received from the OCP master interface have been returned by SSA, d) wait until SSA reads data for all earlier PFI write requests, and e) wait for all DPHY lanes to enter stop state (LP11), and then f) send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b01: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will a) stop accepting requests on the IOSF primary interface, b) stop accepting new requests from the OCP master interface, c) wait until read data from all earlier read requests received from the OCP master interface have been returned by SSA, d) wait until SSA reads data for all earlier PFI write requests, and then e) send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b10: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will wait for all DPHY lanes to enter stop state (LP11), and then send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b11: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will immediately send an IUINT_OK_TO_RESET posted message to PUNIT.

Bit Range	Default & Access	Description
1	1b RW	**IBEWC:** IB_ENABLE_WRITE_COMBINING: When set, enables the combining of adjacent 32-byte write requests to the same cache line. When cleared, each 32-byte write request is sent as a separate request on the IB interface.
0	1b RW	**IBERC:** IB_ENABLE_READ_COMBINING: When set, enables the combining of adjacent 32-byte read requests to the same cache line. When cleared, each 32-byte read request is sent as a separate request on the IB interface.

15.8 Image Signal Processor Memory Mapped IO Registers

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_gpd_gp_reg_reg_gp_sdram_wakeup_type (gpd_gp_reg_reg_gp_sdram_wakeup)—Offset 0h" on page 1124	00000000h
4h	4	"reg_gpd_gp_reg_reg_gp_idle_type (gpd_gp_reg_reg_gp_idle)—Offset 4h" on page 1125	00000000h
8h	4	"reg_gpd_gp_reg_reg_gp_irq_req0_type (gpd_gp_reg_reg_gp_irq_req0)—Offset 8h" on page 1126	00000000h
Ch	4	"reg_gpd_gp_reg_reg_gp_irq_req1_type (gpd_gp_reg_reg_gp_irq_req1)—Offset Ch" on page 1126	00000000h
10h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_type (gpd_gp_reg_reg_gp_sp_stream_stat)—Offset 10h" on page 1127	00022022h
14h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_type (gpd_gp_reg_reg_gp_sp_stream_stat_b)—Offset 14h" on page 1129	00000000h
18h	4	"reg_gpd_gp_reg_reg_gp_isp_stream_stat_type (gpd_gp_reg_reg_gp_isp_stream_stat)—Offset 18h" on page 1131	02200000h
1Ch	4	"reg_gpd_gp_reg_reg_gp_mod_stream_stat_type (gpd_gp_reg_reg_gp_mod_stream_stat)—Offset 1Ch" on page 1133	AA88A222h
20h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond)—Offset 20h" on page 1135	00000000h
24h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond_type (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond)—Offset 24h" on page 1136	00000000h
28h	4	"reg_gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond)—Offset 28h" on page 1137	00000000h
2Ch	4	"reg_gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond)—Offset 2Ch" on page 1137	00000000h
30h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable)—Offset 30h" on page 1138	00000000h
34h	4	"reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable_type (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable)—Offset 34h" on page 1139	00000000h
38h	4	"reg_gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable)—Offset 38h" on page 1139	00000000h
3Ch	4	"reg_gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable)—Offset 3Ch" on page 1140	00000000h
40h	4	"reg_gpd_gp_reg_reg_gp_switch_if_type (gpd_gp_reg_reg_gp_switch_if)—Offset 40h" on page 1141	00000000h
44h	4	"reg_gpd_gp_reg_reg_gp_switch_gdc1_type (gpd_gp_reg_reg_gp_switch_gdc1)—Offset 44h" on page 1142	00000000h
48h	4	"reg_gpd_gp_reg_reg_gp_switch_gdc2_type (gpd_gp_reg_reg_gp_switch_gdc2)—Offset 48h" on page 1142	00000000h
4Ch	4	"reg_gpd_gp_reg_reg_gp_srst_type (gpd_gp_reg_reg_gp_srst)—Offset 4Ch" on page 1143	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
50h	4	"reg_gpd_gp_reg_reg_gp_slv_reg_srst_type (gpd_gp_reg_reg_gp_slv_reg_srst)—Offset 50h" on page 1145	00000000h
100h	4	"reg_gpd_tc_FifoWriteCmd_type (gpd_tc_FifoWriteCmd)—Offset 100h" on page 1146	00000000h
400h	4	"reg_gpd_c_gpio_reg_gpio_doe_type (gpd_c_gpio_reg_gpio_doe)—Offset 400h" on page 1146	00000000h
404h	4	"reg_gpd_c_gpio_reg_gpio_do_select_type (gpd_c_gpio_reg_gpio_do_select)—Offset 404h" on page 1147	00000000h
408h	4	"reg_gpd_c_gpio_reg_gpio_do_0_type (gpd_c_gpio_reg_gpio_do_0)—Offset 408h" on page 1147	00000000h
40Ch	4	"reg_gpd_c_gpio_reg_gpio_do_1_type (gpd_c_gpio_reg_gpio_do_1)—Offset 40Ch" on page 1148	00000000h
410h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_0_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_0)—Offset 410h" on page 1148	00000000h
414h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_1_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_1)—Offset 414h" on page 1149	00000000h
418h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_2_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_2)—Offset 418h" on page 1150	00000000h
41Ch	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_3_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_3)—Offset 41Ch" on page 1150	00000000h
420h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_main_cnt_type (gpd_c_gpio_reg_gpio_do_pwm_main_cnt)—Offset 420h" on page 1151	00000000h
424h	4	"reg_gpd_c_gpio_reg_gpio_do_pwm_enable_type (gpd_c_gpio_reg_gpio_do_pwm_enable)—Offset 424h" on page 1152	00000000h
428h	4	"reg_gpd_c_gpio_reg_gpio_di_debouncemethod_type (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h" on page 1152	00000000h
42Ch	4	"reg_gpd_c_gpio_reg_gpio_di_debounce_cnt0_type (gpd_c_gpio_reg_gpio_di_debounce_cnt0)—Offset 42Ch" on page 1153	00000000h
430h	4	"reg_gpd_c_gpio_reg_gpio_di_debounce_cnt1_type (gpd_c_gpio_reg_gpio_di_debounce_cnt1)—Offset 430h" on page 1154	00000000h
434h	4	"reg_gpd_c_gpio_reg_gpio_di_debounce_cnt2_type (gpd_c_gpio_reg_gpio_di_debounce_cnt2)—Offset 434h" on page 1154	00000000h
438h	4	"reg_gpd_c_gpio_reg_gpio_di_debounce_cnt3_type (gpd_c_gpio_reg_gpio_di_debounce_cnt3)—Offset 438h" on page 1155	00000000h
43Ch	4	"reg_gpd_c_gpio_reg_gpio_di_activelevel_type (gpd_c_gpio_reg_gpio_di_activelevel)—Offset 43Ch" on page 1155	00000FFFh
440h	4	"reg_gpd_c_gpio_reg_gpio_di_debouncemethod_type (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h" on page 1152	00000FFFh
500h	4	"reg_gpd_irq_ctrl_reg_irq_edge_type (gpd_irq_ctrl_reg_irq_edge)—Offset 500h" on page 1157	00000000h
504h	4	"reg_gpd_irq_ctrl_reg_irq_mask_type (gpd_irq_ctrl_reg_irq_mask)—Offset 504h" on page 1157	00000000h
508h	4	"reg_gpd_irq_ctrl_reg_irq_status_type (gpd_irq_ctrl_reg_irq_status)—Offset 508h" on page 1157	00000000h
50Ch	4	"reg_gpd_irq_ctrl_reg_irq_clear_type (gpd_irq_ctrl_reg_irq_clear)—Offset 50Ch" on page 1159	00000000h
510h	4	"reg_gpd_irq_ctrl_reg_irq_enable_type (gpd_irq_ctrl_reg_irq_enable)—Offset 510h" on page 1159	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
514h	4	"reg_gpd_irq_ctrl_reg_irq_level_not_pulse_type (gpd_irq_ctrl_reg_irq_level_not_pulse)—Offset 514h" on page 1160	00000000h
518h	4	"reg_gpd_irq_ctrl_reg_irq_str_out_enable_type (gpd_irq_ctrl_reg_irq_str_out_enable)—Offset 518h" on page 1160	00000000h
600h	4	"reg_gpd_gptimer_reg_reset_type (gpd_gptimer_reg_reset)—Offset 600h" on page 1161	00000000h
604h	4	"reg_gpd_gptimer_overall_enable_type (gpd_gptimer_overall_enable)—Offset 604h" on page 1161	00000000h
608h	4	"reg_gpd_gptimer_enable_timer_0_type (gpd_gptimer_enable_timer_0)—Offset 608h" on page 1162	00000000h
60Ch	4	"reg_gpd_gptimer_enable_timer_1_type (gpd_gptimer_enable_timer_1)—Offset 60Ch" on page 1162	00000000h
610h	4	"reg_gpd_gptimer_enable_timer_2_type (gpd_gptimer_enable_timer_2)—Offset 610h" on page 1163	00000000h
614h	4	"reg_gpd_gptimer_enable_timer_3_type (gpd_gptimer_enable_timer_3)—Offset 614h" on page 1164	00000000h
618h	4	"reg_gpd_gptimer_enable_timer_4_type (gpd_gptimer_enable_timer_4)—Offset 618h" on page 1164	00000000h
61Ch	4	"reg_gpd_gptimer_enable_timer_5_type (gpd_gptimer_enable_timer_5)—Offset 61Ch" on page 1165	00000000h
620h	4	"reg_gpd_gptimer_enable_timer_6_type (gpd_gptimer_enable_timer_6)—Offset 620h" on page 1165	00000000h
624h	4	"reg_gpd_gptimer_enable_timer_7_type (gpd_gptimer_enable_timer_7)—Offset 624h" on page 1166	00000000h
628h	4	"reg_gpd_gptimer_value_timer_0_type (gpd_gptimer_value_timer_0)—Offset 628h" on page 1166	00000000h
62Ch	4	"reg_gpd_gptimer_value_timer_1_type (gpd_gptimer_value_timer_1)—Offset 62Ch" on page 1167	00000000h
630h	4	"reg_gpd_gptimer_value_timer_2_type (gpd_gptimer_value_timer_2)—Offset 630h" on page 1167	00000000h
634h	4	"reg_gpd_gptimer_value_timer_3_type (gpd_gptimer_value_timer_3)—Offset 634h" on page 1168	00000000h
638h	4	"reg_gpd_gptimer_value_timer_4_type (gpd_gptimer_value_timer_4)—Offset 638h" on page 1168	00000000h
63Ch	4	"reg_gpd_gptimer_value_timer_5_type (gpd_gptimer_value_timer_5)—Offset 63Ch" on page 1169	00000000h
640h	4	"reg_gpd_gptimer_value_timer_6_type (gpd_gptimer_value_timer_6)—Offset 640h" on page 1169	00000000h
644h	4	"reg_gpd_gptimer_value_timer_7_type (gpd_gptimer_value_timer_7)—Offset 644h" on page 1170	00000000h
648h	4	"reg_gpd_gptimer_count_type_timer_0_type (gpd_gptimer_count_type_timer_0)—Offset 648h" on page 1170	00000000h
64Ch	4	"reg_gpd_gptimer_count_type_timer_1_type (gpd_gptimer_count_type_timer_1)—Offset 64Ch" on page 1171	00000000h
650h	4	"reg_gpd_gptimer_count_type_timer_2_type (gpd_gptimer_count_type_timer_2)—Offset 650h" on page 1172	00000000h
654h	4	"reg_gpd_gptimer_count_type_timer_3_type (gpd_gptimer_count_type_timer_3)—Offset 654h" on page 1172	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
658h	4	"reg_gpd_gptimer_count_type_timer_4_type (gpd_gptimer_count_type_timer_4)—Offset 658h" on page 1173	00000000h
65Ch	4	"reg_gpd_gptimer_count_type_timer_5_type (gpd_gptimer_count_type_timer_5)—Offset 65Ch" on page 1173	00000000h
660h	4	"reg_gpd_gptimer_count_type_timer_6_type (gpd_gptimer_count_type_timer_6)—Offset 660h" on page 1174	00000000h
664h	4	"reg_gpd_gptimer_count_type_timer_7_type (gpd_gptimer_count_type_timer_7)—Offset 664h" on page 1175	00000000h
668h	4	"reg_gpd_gptimer_signal_select_timer_0_type (gpd_gptimer_signal_select_timer_0)—Offset 668h" on page 1175	00000000h
66Ch	4	"reg_gpd_gptimer_signal_select_timer_1_type (gpd_gptimer_signal_select_timer_1)—Offset 66Ch" on page 1176	00000000h
670h	4	"reg_gpd_gptimer_signal_select_timer_2_type (gpd_gptimer_signal_select_timer_2)—Offset 670h" on page 1177	00000000h
674h	4	"reg_gpd_gptimer_signal_select_timer_3_type (gpd_gptimer_signal_select_timer_3)—Offset 674h" on page 1177	00000000h
678h	4	"reg_gpd_gptimer_signal_select_timer_4_type (gpd_gptimer_signal_select_timer_4)—Offset 678h" on page 1178	00000000h
67Ch	4	"reg_gpd_gptimer_signal_select_timer_5_type (gpd_gptimer_signal_select_timer_5)—Offset 67Ch" on page 1179	00000000h
680h	4	"reg_gpd_gptimer_signal_select_timer_6_type (gpd_gptimer_signal_select_timer_6)—Offset 680h" on page 1179	00000000h
684h	4	"reg_gpd_gptimer_signal_select_timer_7_type (gpd_gptimer_signal_select_timer_7)—Offset 684h" on page 1180	00000000h
688h	4	"reg_gpd_gptimer_irq_trigger_value_0_type (gpd_gptimer_irq_trigger_value_0)—Offset 688h" on page 1181	00000000h
68Ch	4	"reg_gpd_gptimer_irq_trigger_value_1_type (gpd_gptimer_irq_trigger_value_1)—Offset 68Ch" on page 1181	00000000h
690h	4	"reg_gpd_gptimer_irq_timer_select_0_type (gpd_gptimer_irq_timer_select_0)—Offset 690h" on page 1182	00000000h
694h	4	"reg_gpd_gptimer_irq_timer_select_1_type (gpd_gptimer_irq_timer_select_1)—Offset 694h" on page 1182	00000000h
698h	4	"reg_gpd_gptimer_irq_enable_0_type (gpd_gptimer_irq_enable_0)—Offset 698h" on page 1183	00000000h
69Ch	4	"reg_gpd_gptimer_irq_enable_1_type (gpd_gptimer_irq_enable_1)—Offset 69Ch" on page 1183	00000000h
10000h	4	"reg_scp_stat_and_ctrl_type (scp_stat_and_ctrl)—Offset 10000h" on page 1184	000000A0h
10004h	4	"reg_scp_base_address_type (scp_base_address)—Offset 10004h" on page 1185	00000000h
10008h	4	"reg_scp_unused_2_type (scp_unused_2)—Offset 10008h" on page 1186	00000000h
10010h	4	"reg_scp_base_addr_seg_0_MI_xmem_master_int_type (scp_base_addr_seg_0_MI_xmem_master_int)—Offset 10010h" on page 1186	00000000h
10014h	4	"reg_scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master_type (scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master)—Offset 10014h" on page 1187	00000000h
10018h	4	"reg_scp_unused_6_type (scp_unused_6)—Offset 10018h" on page 1188	00000000h
1001Ch	4	"reg_scp_unused_7_type (scp_unused_7)—Offset 1001Ch" on page 1188	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
10024h	4	"reg_scp_debug_pc_type (scp_debug_pc)—Offset 10024h" on page 1188	00000000h
10028h	4	"reg_scp_stall_stat_fifo_loc_mt_am_inst_0_op0_type (scp_stall_stat_fifo_loc_mt_am_inst_0_op0)—Offset 10028h" on page 1189	00000000h
1002Ch	4	"reg_scp_unused_11_type (scp_unused_11)—Offset 1002Ch" on page 1190	00000000h
10030h	4	"reg_scp_pmem_slave_access_type (scp_pmem_slave_access)—Offset 10030h" on page 1191	00000000h
20000h	4	"reg_isp_stat_and_ctrl_type (isp_stat_and_ctrl)—Offset 20000h" on page 1191	000000A0h
20004h	4	"reg_isp_base_address_type (isp_base_address)—Offset 20004h" on page 1193	00000000h
20008h	4	"reg_isp_unused_2_type (isp_unused_2)—Offset 20008h" on page 1193	00000000h
20010h	4	"reg_isp_base_addr_seg_0_MI_base_config_mem_master_type (isp_base_addr_seg_0_MI_base_config_mem_master)—Offset 20010h" on page 1194	00000000h
20014h	4	"reg_isp_unused_5_type (isp_unused_5)—Offset 20014h" on page 1194	00000000h
2001Ch	4	"reg_isp_debug_pc_type (isp_debug_pc)—Offset 2001Ch" on page 1195	00000000h
20020h	4	"reg_isp_stall_stat_base_config_mem_iam_op0_type (isp_stall_stat_base_config_mem_iam_op0)—Offset 20020h" on page 1195	00000000h
20024h	4	"reg_isp_unused_9_type (isp_unused_9)—Offset 20024h" on page 1197	00000000h
20028h	4	"reg_isp_pmem_slave_access_type (isp_pmem_slave_access)—Offset 20028h" on page 1197	00000000h
30000h	4	"reg_ifmt_ift_prim_IF_sw_rst_type (ifmt_ift_prim_IF_sw_rst)—Offset 30000h" on page 1198	00000000h
30004h	4	"reg_ifmt_ift_prim_IF_start_line_type (ifmt_ift_prim_IF_start_line)—Offset 30004h" on page 1198	00000000h
30008h	4	"reg_ifmt_ift_prim_IF_start_column_type (ifmt_ift_prim_IF_start_column)—Offset 30008h" on page 1199	00000000h
3000Ch	4	"reg_ifmt_ift_prim_IF_Cropped_height_type (ifmt_ift_prim_IF_Cropped_height)—Offset 3000Ch" on page 1199	00000000h
30010h	4	"reg_ifmt_ift_prim_IF_Cropped_width_type (ifmt_ift_prim_IF_Cropped_width)—Offset 30010h" on page 1200	00000000h
30014h	4	"reg_ifmt_ift_prim_IF_Vert_Decim_type (ifmt_ift_prim_IF_Vert_Decim)—Offset 30014h" on page 1201	00000000h
30018h	4	"reg_ifmt_ift_prim_IF_Horiz_Decim_type (ifmt_ift_prim_IF_Horiz_Decim)—Offset 30018h" on page 1201	00000000h
3001Ch	4	"reg_ifmt_ift_prim_IF_Horiz_Deinter_type (ifmt_ift_prim_IF_Horiz_Deinter)—Offset 3001Ch" on page 1202	00000000h
30020h	4	"reg_ifmt_ift_prim_IF_Left_Pad_type (ifmt_ift_prim_IF_Left_Pad)—Offset 30020h" on page 1202	00000000h
30024h	4	"reg_ifmt_ift_prim_IF_EOF_Offset_type (ifmt_ift_prim_IF_EOF_Offset)—Offset 30024h" on page 1203	00000000h
30028h	4	"reg_ifmt_ift_prim_IF_Start_addr_type (ifmt_ift_prim_IF_Start_addr)—Offset 30028h" on page 1203	00000000h
3002Ch	4	"reg_ifmt_ift_prim_IF_End_addr_type (ifmt_ift_prim_IF_End_addr)—Offset 3002Ch" on page 1204	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30030h	4	"reg_ifmt_ift_prim_IF_incr_type (ifmt_ift_prim_IF_incr)—Offset 30030h" on page 1205	00000000h
30034h	4	"reg_ifmt_ift_prim_IF_YUV_420_format_type (ifmt_ift_prim_IF_YUV_420_format)—Offset 30034h" on page 1205	00000000h
30038h	4	"reg_ifmt_ift_prim_IF_Vsynch_active_low_type (ifmt_ift_prim_IF_Vsynch_active_low)—Offset 30038h" on page 1206	00000000h
3003Ch	4	"reg_ifmt_ift_prim_IF_Hsynch_active_low_type (ifmt_ift_prim_IF_Hsynch_active_low)—Offset 3003Ch" on page 1206	00000000h
30040h	4	"reg_ifmt_ift_prim_IF_ReEnable_type (ifmt_ift_prim_IF_ReEnable)—Offset 30040h" on page 1207	00000000h
30044h	4	"reg_ifmt_ift_prim_IF_block_input_type (ifmt_ift_prim_IF_block_input)—Offset 30044h" on page 1207	00000000h
30048h	4	"reg_ifmt_ift_prim_IF_Vert_Deinter_type (ifmt_ift_prim_IF_Vert_Deinter)—Offset 30048h" on page 1208	00000000h
30100h	4	"reg_ifmt_ift_prim_IF_FSM_Sync_status_type (ifmt_ift_prim_IF_FSM_Sync_status)—Offset 30100h" on page 1209	00000000h
30104h	4	"reg_ifmt_ift_prim_FSM_Sync_counter_type (ifmt_ift_prim_FSM_Sync_counter)—Offset 30104h" on page 1209	00000000h
30108h	4	"reg_ifmt_ift_prim_FSM_Crop_status_type (ifmt_ift_prim_FSM_Crop_status)—Offset 30108h" on page 1210	00000000h
3010Ch	4	"reg_ifmt_ift_prim_FSM_Crop_line_counter_type (ifmt_ift_prim_FSM_Crop_line_counter)—Offset 3010Ch" on page 1211	00000000h
30110h	4	"reg_ifmt_ift_prim_FSM_Crop_pixel_counter_type (ifmt_ift_prim_FSM_Crop_pixel_counter)—Offset 30110h" on page 1211	00000000h
30114h	4	"reg_ifmt_ift_prim_FSM_Deinterl_idx_buffer_type (ifmt_ift_prim_FSM_Deinterl_idx_buffer)—Offset 30114h" on page 1212	00000000h
30118h	4	"reg_ifmt_ift_prim_FSM_Horiz_Decim_cnt_type (ifmt_ift_prim_FSM_Horiz_Decim_cnt)—Offset 30118h" on page 1213	00000000h
3011Ch	4	"reg_ifmt_ift_prim_FSM_Vertic_Decim_cnt_type (ifmt_ift_prim_FSM_Vertic_Decim_cnt)—Offset 3011Ch" on page 1213	00000000h
30120h	4	"reg_ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt)—Offset 30120h" on page 1214	00000000h
30124h	4	"reg_ifmt_ift_prim_IF_FSM_Padding_status_type (ifmt_ift_prim_IF_FSM_Padding_status)—Offset 30124h" on page 1215	00000000h
30128h	4	"reg_ifmt_ift_prim_IF_FSM_Padding_elem_idx_type (ifmt_ift_prim_IF_FSM_Padding_elem_idx)—Offset 30128h" on page 1215	00000000h
3012Ch	4	"reg_ifmt_ift_prim_IF_FSM_Vec_Sup_type (ifmt_ift_prim_IF_FSM_Vec_Sup)—Offset 3012Ch" on page 1216	00000000h
30130h	4	"reg_ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full)—Offset 30130h" on page 1217	00000000h
30134h	4	"reg_ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept)—Offset 30134h" on page 1217	00000001h
30138h	4	"reg_ifmt_ift_prim_IF_Pixel_Fifo_status_type (ifmt_ift_prim_IF_Pixel_Fifo_status)—Offset 30138h" on page 1218	00000001h
30200h	4	"reg_ifmt_ift_prim_b_IF_sw_rst_type (ifmt_ift_prim_b_IF_sw_rst)—Offset 30200h" on page 1219	00000000h
30204h	4	"reg_ifmt_ift_prim_b_IF_start_line_type (ifmt_ift_prim_b_IF_start_line)—Offset 30204h" on page 1219	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30208h	4	"reg_ifmt_ift_prim_b_IF_start_column_type (ifmt_ift_prim_b_IF_start_column)—Offset 30208h" on page 1220	00000000h
3020Ch	4	"reg_ifmt_ift_prim_b_IF_Cropped_height_type (ifmt_ift_prim_b_IF_Cropped_height)—Offset 3020Ch" on page 1220	00000000h
30210h	4	"reg_ifmt_ift_prim_b_IF_Cropped_width_type (ifmt_ift_prim_b_IF_Cropped_width)—Offset 30210h" on page 1221	00000000h
30214h	4	"reg_ifmt_ift_prim_b_IF_Vert_Decim_type (ifmt_ift_prim_b_IF_Vert_Decim)—Offset 30214h" on page 1222	00000000h
30218h	4	"reg_ifmt_ift_prim_b_IF_Horiz_Decim_type (ifmt_ift_prim_b_IF_Horiz_Decim)—Offset 30218h" on page 1222	00000000h
3021Ch	4	"reg_ifmt_ift_prim_b_IF_Horiz_Deinter_type (ifmt_ift_prim_b_IF_Horiz_Deinter)—Offset 3021Ch" on page 1223	00000000h
30220h	4	"reg_ifmt_ift_prim_b_IF_Left_Pad_type (ifmt_ift_prim_b_IF_Left_Pad)—Offset 30220h" on page 1223	00000000h
30224h	4	"reg_ifmt_ift_prim_b_IF_EOF_Offset_type (ifmt_ift_prim_b_IF_EOF_Offset)—Offset 30224h" on page 1224	00000000h
30228h	4	"reg_ifmt_ift_prim_b_IF_Start_addr_type (ifmt_ift_prim_b_IF_Start_addr)—Offset 30228h" on page 1225	00000000h
3022Ch	4	"reg_ifmt_ift_prim_b_IF_End_addr_type (ifmt_ift_prim_b_IF_End_addr)—Offset 3022Ch" on page 1225	00000000h
30230h	4	"reg_ifmt_ift_prim_b_IF_incr_type (ifmt_ift_prim_b_IF_incr)—Offset 30230h" on page 1226	00000000h
30234h	4	"reg_ifmt_ift_prim_b_IF_YUV_420_format_type (ifmt_ift_prim_b_IF_YUV_420_format)—Offset 30234h" on page 1226	00000000h
30238h	4	"reg_ifmt_ift_prim_b_IF_Vsynch_active_low_type (ifmt_ift_prim_b_IF_Vsynch_active_low)—Offset 30238h" on page 1227	00000000h
3023Ch	4	"reg_ifmt_ift_prim_b_IF_Hsynch_active_low_type (ifmt_ift_prim_b_IF_Hsynch_active_low)—Offset 3023Ch" on page 1228	00000000h
30240h	4	"reg_ifmt_ift_prim_b_IF_ReEnable_type (ifmt_ift_prim_b_IF_ReEnable)—Offset 30240h" on page 1228	00000000h
30244h	4	"reg_ifmt_ift_prim_b_IF_block_input_type (ifmt_ift_prim_b_IF_block_input)—Offset 30244h" on page 1229	00000000h
30248h	4	"reg_ifmt_ift_prim_b_IF_Vert_Deinter_type (ifmt_ift_prim_b_IF_Vert_Deinter)—Offset 30248h" on page 1229	00000000h
30300h	4	"reg_ifmt_ift_prim_b_IF_FSM_Sync_status_type (ifmt_ift_prim_b_IF_FSM_Sync_status)—Offset 30300h" on page 1230	00000000h
30304h	4	"reg_ifmt_ift_prim_b_FSM_Sync_counter_type (ifmt_ift_prim_b_FSM_Sync_counter)—Offset 30304h" on page 1231	00000000h
30308h	4	"reg_ifmt_ift_prim_b_FSM_Crop_status_type (ifmt_ift_prim_b_FSM_Crop_status)—Offset 30308h" on page 1231	00000000h
3030Ch	4	"reg_ifmt_ift_prim_b_FSM_Crop_line_counter_type (ifmt_ift_prim_b_FSM_Crop_line_counter)—Offset 3030Ch" on page 1232	00000000h
30310h	4	"reg_ifmt_ift_prim_b_FSM_Crop_pixel_counter_type (ifmt_ift_prim_b_FSM_Crop_pixel_counter)—Offset 30310h" on page 1233	00000000h
30314h	4	"reg_ifmt_ift_prim_b_FSM_Deinterl_idx_buffer_type (ifmt_ift_prim_b_FSM_Deinterl_idx_buffer)—Offset 30314h" on page 1233	00000000h
30318h	4	"reg_ifmt_ift_prim_b_FSM_Horiz_Decim_cnt_type (ifmt_ift_prim_b_FSM_Horiz_Decim_cnt)—Offset 30318h" on page 1234	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
3031Ch	4	"reg_ifmt_ift_prim_b_FSM_Vertic_Decim_cnt_type (ifmt_ift_prim_b_FSM_Vertic_Decim_cnt)—Offset 3031Ch" on page 1235	00000000h
30320h	4	"reg_ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt)—Offset 30320h" on page 1235	00000000h
30324h	4	"reg_ifmt_ift_prim_b_IF_FSM_Padding_status_type (ifmt_ift_prim_b_IF_FSM_Padding_status)—Offset 30324h" on page 1236	00000000h
30328h	4	"reg_ifmt_ift_prim_b_IF_FSM_Padding_elem_idx_type (ifmt_ift_prim_b_IF_FSM_Padding_elem_idx)—Offset 30328h" on page 1237	00000000h
3032Ch	4	"reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup)—Offset 3032Ch" on page 1237	00000000h
30330h	4	"reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full)—Offset 30330h" on page 1238	00000000h
30334h	4	"reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept)—Offset 30334h" on page 1239	00000001h
30338h	4	"reg_ifmt_ift_prim_b_IF_Pixel_Fifo_status_type (ifmt_ift_prim_b_IF_Pixel_Fifo_status)—Offset 30338h" on page 1239	00000001h
30400h	4	"reg_ifmt_ift_sec_IF_sw_rst_type (ifmt_ift_sec_IF_sw_rst)—Offset 30400h" on page 1240	00000000h
30404h	4	"reg_ifmt_ift_sec_IF_start_line_type (ifmt_ift_sec_IF_start_line)—Offset 30404h" on page 1241	00000000h
30408h	4	"reg_ifmt_ift_sec_IF_start_column_type (ifmt_ift_sec_IF_start_column)—Offset 30408h" on page 1241	00000000h
3040Ch	4	"reg_ifmt_ift_sec_IF_Cropped_height_type (ifmt_ift_sec_IF_Cropped_height)—Offset 3040Ch" on page 1242	00000000h
30410h	4	"reg_ifmt_ift_sec_IF_Cropped_width_type (ifmt_ift_sec_IF_Cropped_width)—Offset 30410h" on page 1243	00000000h
30414h	4	"reg_ifmt_ift_sec_IF_Vert_Decim_type (ifmt_ift_sec_IF_Vert_Decim)—Offset 30414h" on page 1243	00000000h
30418h	4	"reg_ifmt_ift_sec_IF_Horiz_Decim_type (ifmt_ift_sec_IF_Horiz_Decim)—Offset 30418h" on page 1244	00000000h
3041Ch	4	"reg_ifmt_ift_sec_IF_Horiz_Deinter_type (ifmt_ift_sec_IF_Horiz_Deinter)—Offset 3041Ch" on page 1244	00000000h
30420h	4	"reg_ifmt_ift_sec_IF_Left_Pad_type (ifmt_ift_sec_IF_Left_Pad)—Offset 30420h" on page 1245	00000000h
30424h	4	"reg_ifmt_ift_sec_IF_EOF_Offset_type (ifmt_ift_sec_IF_EOF_Offset)—Offset 30424h" on page 1245	00000000h
30428h	4	"reg_ifmt_ift_sec_IF_Start_addr_type (ifmt_ift_sec_IF_Start_addr)—Offset 30428h" on page 1246	00000000h
3042Ch	4	"reg_ifmt_ift_sec_IF_End_addr_type (ifmt_ift_sec_IF_End_addr)—Offset 3042Ch" on page 1247	00000000h
30430h	4	"reg_ifmt_ift_sec_IF_incr_type (ifmt_ift_sec_IF_incr)—Offset 30430h" on page 1247	00000000h
30434h	4	"reg_ifmt_ift_sec_IF_YUV_420_format_type (ifmt_ift_sec_IF_YUV_420_format)—Offset 30434h" on page 1248	00000000h
30438h	4	"reg_ifmt_ift_sec_IF_Vsynch_active_low_type (ifmt_ift_sec_IF_Vsynch_active_low)—Offset 30438h" on page 1248	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
3043Ch	4	"reg_ifmt_ift_sec_IF_Hsynch_active_low_type (ifmt_ift_sec_IF_Hsynch_active_low)—Offset 3043Ch" on page 1249	00000000h
30440h	4	"reg_ifmt_ift_sec_IF_ReEnable_type (ifmt_ift_sec_IF_ReEnable)—Offset 30440h" on page 1250	00000000h
30444h	4	"reg_ifmt_ift_sec_IF_block_input_type (ifmt_ift_sec_IF_block_input)—Offset 30444h" on page 1250	00000000h
30448h	4	"reg_ifmt_ift_sec_IF_Vert_Deinter_type (ifmt_ift_sec_IF_Vert_Deinter)—Offset 30448h" on page 1251	00000000h
30500h	4	"reg_ifmt_ift_sec_IF_FSM_Sync_status_type (ifmt_ift_sec_IF_FSM_Sync_status)—Offset 30500h" on page 1251	00000000h
30504h	4	"reg_ifmt_ift_sec_FSM_Sync_counter_type (ifmt_ift_sec_FSM_Sync_counter)—Offset 30504h" on page 1252	00000000h
30508h	4	"reg_ifmt_ift_sec_FSM_Crop_status_type (ifmt_ift_sec_FSM_Crop_status)—Offset 30508h" on page 1253	00000000h
3050Ch	4	"reg_ifmt_ift_sec_FSM_Crop_line_counter_type (ifmt_ift_sec_FSM_Crop_line_counter)—Offset 3050Ch" on page 1253	00000000h
30510h	4	"reg_ifmt_ift_sec_FSM_Crop_pixel_counter_type (ifmt_ift_sec_FSM_Crop_pixel_counter)—Offset 30510h" on page 1254	00000000h
30514h	4	"reg_ifmt_ift_sec_FSM_Deinterl_idx_buffer_type (ifmt_ift_sec_FSM_Deinterl_idx_buffer)—Offset 30514h" on page 1255	00000000h
30518h	4	"reg_ifmt_ift_sec_FSM_Horiz_Decim_cnt_type (ifmt_ift_sec_FSM_Horiz_Decim_cnt)—Offset 30518h" on page 1255	00000000h
3051Ch	4	"reg_ifmt_ift_sec_FSM_Vertic_Decim_cnt_type (ifmt_ift_sec_FSM_Vertic_Decim_cnt)—Offset 3051Ch" on page 1256	00000000h
30520h	4	"reg_ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt)—Offset 30520h" on page 1257	00000000h
30524h	4	"reg_ifmt_ift_sec_IF_FSM_Padding_status_type (ifmt_ift_sec_IF_FSM_Padding_status)—Offset 30524h" on page 1257	00000000h
30528h	4	"reg_ifmt_ift_sec_IF_FSM_Padding_elem_idx_type (ifmt_ift_sec_IF_FSM_Padding_elem_idx)—Offset 30528h" on page 1258	00000000h
3052Ch	4	"reg_ifmt_ift_sec_IF_FSM_Vec_Sup_type (ifmt_ift_sec_IF_FSM_Vec_Sup)—Offset 3052Ch" on page 1259	00000000h
30530h	4	"reg_ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full)—Offset 30530h" on page 1259	00000000h
30534h	4	"reg_ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept)—Offset 30534h" on page 1260	00000001h
30538h	4	"reg_ifmt_ift_sec_IF_Pixel_Fifo_status_type (ifmt_ift_sec_IF_Pixel_Fifo_status)—Offset 30538h" on page 1261	00000001h
30600h	4	"reg_ifmt_mem_cpy_MemCopy_sw_rst_type (ifmt_mem_cpy_MemCopy_sw_rst)—Offset 30600h" on page 1261	00000000h
30604h	4	"reg_ifmt_mem_cpy_MemCopy_in_endian_type (ifmt_mem_cpy_MemCopy_in_endian)—Offset 30604h" on page 1262	00000000h
30608h	4	"reg_ifmt_mem_cpy_MemCopy_out_endian_type (ifmt_mem_cpy_MemCopy_out_endian)—Offset 30608h" on page 1263	00000000h
3060Ch	4	"reg_ifmt_mem_cpy_MemCopy_bit_swap_type (ifmt_mem_cpy_MemCopy_bit_swap)—Offset 3060Ch" on page 1263	00000000h
30610h	4	"reg_ifmt_mem_cpy_MemCopy_block_synch_type (ifmt_mem_cpy_MemCopy_block_synch)—Offset 30610h" on page 1264	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30614h	4	"reg_ifmt_mem_cpy_MemCopy_packet_synch_type (ifmt_mem_cpy_MemCopy_packet_synch)—Offset 30614h" on page 1265	00000000h
30618h	4	"reg_ifmt_mem_cpy_MemCopy_rd_post_wr_sync_type (ifmt_mem_cpy_MemCopy_rd_post_wr_sync)—Offset 30618h" on page 1265	00000000h
3061Ch	4	"reg_ifmt_mem_cpy_MemCopy_dual_input_type (ifmt_mem_cpy_MemCopy_dual_input)—Offset 3061Ch" on page 1266	00000000h
30620h	4	"reg_ifmt_mem_cpy_MemCopy_ReEnable_type (ifmt_mem_cpy_MemCopy_ReEnable)—Offset 30620h" on page 1267	00000000h
30700h	4	"reg_ifmt_mem_cpy_MemCopy_token_data_type (ifmt_mem_cpy_MemCopy_token_data)—Offset 30700h" on page 1267	00000000h
30704h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Sync_status_type (ifmt_mem_cpy_MemCopy_FSM_Sync_status)—Offset 30704h" on page 1268	00000000h
30708h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt)—Offset 30708h" on page 1269	00000000h
3070Ch	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt)—Offset 3070Ch" on page 1269	00000000h
30710h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt)—Offset 30710h" on page 1270	00000000h
30714h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status_type (ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status)—Offset 30714h" on page 1271	00000000h
30718h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt)—Offset 30718h" on page 1271	00000000h
3071Ch	4	"reg_ifmt_mem_cpy_MemCopy_FSM_CioWr_status_type (ifmt_mem_cpy_MemCopy_FSM_CioWr_status)—Offset 3071Ch" on page 1272	00000004h
30720h	4	"reg_ifmt_mem_cpy_MemCopy_FSM_CioWr_addr_type (ifmt_mem_cpy_MemCopy_FSM_CioWr_addr)—Offset 30720h" on page 1273	00000000h
30800h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg0_type (ifmt_gp_reg_IFMT_input_switch_lut_reg0)—Offset 30800h" on page 1274	00000000h
30804h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg1_type (ifmt_gp_reg_IFMT_input_switch_lut_reg1)—Offset 30804h" on page 1274	00000000h
30808h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg2_type (ifmt_gp_reg_IFMT_input_switch_lut_reg2)—Offset 30808h" on page 1275	00000000h
3080Ch	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg3_type (ifmt_gp_reg_IFMT_input_switch_lut_reg3)—Offset 3080Ch" on page 1276	00000000h
30810h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg4_type (ifmt_gp_reg_IFMT_input_switch_lut_reg4)—Offset 30810h" on page 1276	00000000h
30814h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg5_type (ifmt_gp_reg_IFMT_input_switch_lut_reg5)—Offset 30814h" on page 1277	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
30818h	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg6_type (ifmt_gp_reg_IFMT_input_switch_lut_reg6)—Offset 30818h" on page 1277	00000000h
3081Ch	4	"reg_ifmt_gp_reg_IFMT_input_switch_lut_reg7_type (ifmt_gp_reg_IFMT_input_switch_lut_reg7)—Offset 3081Ch" on page 1278	00000000h
30820h	4	"reg_ifmt_gp_reg_IFMT_input_switch_fsync_lut_type (ifmt_gp_reg_IFMT_input_switch_fsync_lut)—Offset 30820h" on page 1278	00000000h
30824h	4	"reg_ifmt_gp_reg_IFMT_srst_type (ifmt_gp_reg_IFMT_srst)—Offset 30824h" on page 1279	00000000h
30828h	4	"reg_ifmt_gp_reg_IFMT_slv_reg_srst_type (ifmt_gp_reg_IFMT_slv_reg_srst)—Offset 30828h" on page 1280	00000000h
3082Ch	4	"reg_ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type_type (ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type)—Offset 3082Ch" on page 1281	00000000h
30A00h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge)—Offset 30A00h" on page 1281	00000000h
30A04h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask)—Offset 30A04h" on page 1282	00000000h
30A08h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_status_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_status)—Offset 30A08h" on page 1283	00000000h
30A0Ch	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear)—Offset 30A0Ch" on page 1283	00000000h
30A10h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable)—Offset 30A10h" on page 1284	00000000h
30A14h	4	"reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse)—Offset 30A14h" on page 1285	00000000h
40000h	4	"reg_isp_dma_DMA_FSM_Command_type (isp_dma_DMA_FSM_Command)—Offset 40000h" on page 1285	00000001h
41000h	4	"reg_isp_dma_DMA_CH0_Packing_setup_type (isp_dma_DMA_CH0_Packing_setup)—Offset 41000h" on page 1286	00000000h
41004h	4	"reg_isp_dma_DMA_CH1_Packing_setup_type (isp_dma_DMA_CH1_Packing_setup)—Offset 41004h" on page 1287	00000000h
41008h	4	"reg_isp_dma_DMA_CH2_Packing_setup_type (isp_dma_DMA_CH2_Packing_setup)—Offset 41008h" on page 1287	00000000h
4100Ch	4	"reg_isp_dma_DMA_CH3_Packing_setup_type (isp_dma_DMA_CH3_Packing_setup)—Offset 4100Ch" on page 1288	00000000h
41010h	4	"reg_isp_dma_DMA_CH4_Packing_setup_type (isp_dma_DMA_CH4_Packing_setup)—Offset 41010h" on page 1289	00000000h
41014h	4	"reg_isp_dma_DMA_CH5_Packing_setup_type (isp_dma_DMA_CH5_Packing_setup)—Offset 41014h" on page 1290	00000000h
41018h	4	"reg_isp_dma_DMA_CH6_Packing_setup_type (isp_dma_DMA_CH6_Packing_setup)—Offset 41018h" on page 1291	00000000h
4101Ch	4	"reg_isp_dma_DMA_CH7_Packing_setup_type (isp_dma_DMA_CH7_Packing_setup)—Offset 4101Ch" on page 1291	00000000h
41020h	4	"reg_isp_dma_DMA_CH8_Packing_setup_type (isp_dma_DMA_CH8_Packing_setup)—Offset 41020h" on page 1292	00000000h
41024h	4	"reg_isp_dma_DMA_CH9_Packing_setup_type (isp_dma_DMA_CH9_Packing_setup)—Offset 41024h" on page 1293	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41028h	4	"reg_isp_dma_DMA_CH10_Packing_setup_type (isp_dma_DMA_CH10_Packing_setup)—Offset 41028h" on page 1294	00000000h
4102Ch	4	"reg_isp_dma_DMA_CH11_Packing_setup_type (isp_dma_DMA_CH11_Packing_setup)—Offset 4102Ch" on page 1294	00000000h
41030h	4	"reg_isp_dma_DMA_CH12_Packing_setup_type (isp_dma_DMA_CH12_Packing_setup)—Offset 41030h" on page 1295	00000000h
41034h	4	"reg_isp_dma_DMA_CH13_Packing_setup_type (isp_dma_DMA_CH13_Packing_setup)—Offset 41034h" on page 1296	00000000h
41038h	4	"reg_isp_dma_DMA_CH14_Packing_setup_type (isp_dma_DMA_CH14_Packing_setup)—Offset 41038h" on page 1297	00000000h
4103Ch	4	"reg_isp_dma_DMA_CH15_Packing_setup_type (isp_dma_DMA_CH15_Packing_setup)—Offset 4103Ch" on page 1297	00000000h
41040h	4	"reg_isp_dma_DMA_CH16_Packing_setup_type (isp_dma_DMA_CH16_Packing_setup)—Offset 41040h" on page 1298	00000000h
41044h	4	"reg_isp_dma_DMA_CH17_Packing_setup_type (isp_dma_DMA_CH17_Packing_setup)—Offset 41044h" on page 1299	00000000h
41048h	4	"reg_isp_dma_DMA_CH18_Packing_setup_type (isp_dma_DMA_CH18_Packing_setup)—Offset 41048h" on page 1300	00000000h
4104Ch	4	"reg_isp_dma_DMA_CH19_Packing_setup_type (isp_dma_DMA_CH19_Packing_setup)—Offset 4104Ch" on page 1300	00000000h
41050h	4	"reg_isp_dma_DMA_CH20_Packing_setup_type (isp_dma_DMA_CH20_Packing_setup)—Offset 41050h" on page 1301	00000000h
41054h	4	"reg_isp_dma_DMA_CH21_Packing_setup_type (isp_dma_DMA_CH21_Packing_setup)—Offset 41054h" on page 1302	00000000h
41058h	4	"reg_isp_dma_DMA_CH22_Packing_setup_type (isp_dma_DMA_CH22_Packing_setup)—Offset 41058h" on page 1303	00000000h
4105Ch	4	"reg_isp_dma_DMA_CH23_Packing_setup_type (isp_dma_DMA_CH23_Packing_setup)—Offset 4105Ch" on page 1303	00000000h
41060h	4	"reg_isp_dma_DMA_CH24_Packing_setup_type (isp_dma_DMA_CH24_Packing_setup)—Offset 41060h" on page 1304	00000000h
41064h	4	"reg_isp_dma_DMA_CH25_Packing_setup_type (isp_dma_DMA_CH25_Packing_setup)—Offset 41064h" on page 1305	00000000h
41068h	4	"reg_isp_dma_DMA_CH26_Packing_setup_type (isp_dma_DMA_CH26_Packing_setup)—Offset 41068h" on page 1306	00000000h
41070h	4	"reg_isp_dma_DMA_CH28_Packing_setup_type (isp_dma_DMA_CH28_Packing_setup)—Offset 41070h" on page 1306	00000000h
41074h	4	"reg_isp_dma_DMA_CH29_Packing_setup_type (isp_dma_DMA_CH29_Packing_setup)—Offset 41074h" on page 1307	00000000h
41078h	4	"reg_isp_dma_DMA_CH30_Packing_setup_type (isp_dma_DMA_CH30_Packing_setup)—Offset 41078h" on page 1308	00000000h
4107Ch	4	"reg_isp_dma_DMA_CH31_Packing_setup_type (isp_dma_DMA_CH31_Packing_setup)—Offset 4107Ch" on page 1309	00000000h
41100h	4	"reg_isp_dma_DMA_CH0_dev_stride_A_type (isp_dma_DMA_CH0_dev_stride_A)—Offset 41100h" on page 1309	00000000h
41104h	4	"reg_isp_dma_DMA_CH1_dev_stride_A_type (isp_dma_DMA_CH1_dev_stride_A)—Offset 41104h" on page 1310	00000000h
41108h	4	"reg_isp_dma_DMA_CH2_dev_stride_A_type (isp_dma_DMA_CH2_dev_stride_A)—Offset 41108h" on page 1310	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
4110Ch	4	"reg_isp_dma_DMA_CH3_dev_stride_A_type (isp_dma_DMA_CH3_dev_stride_A)—Offset 4110Ch" on page 1311	00000000h
41110h	4	"reg_isp_dma_DMA_CH4_dev_stride_A_type (isp_dma_DMA_CH4_dev_stride_A)—Offset 41110h" on page 1311	00000000h
41114h	4	"reg_isp_dma_DMA_CH5_dev_stride_A_type (isp_dma_DMA_CH5_dev_stride_A)—Offset 41114h" on page 1312	00000000h
41118h	4	"reg_isp_dma_DMA_CH6_dev_stride_A_type (isp_dma_DMA_CH6_dev_stride_A)—Offset 41118h" on page 1312	00000000h
4111Ch	4	"reg_isp_dma_DMA_CH7_dev_stride_A_type (isp_dma_DMA_CH7_dev_stride_A)—Offset 4111Ch" on page 1313	00000000h
41120h	4	"reg_isp_dma_DMA_CH8_dev_stride_A_type (isp_dma_DMA_CH8_dev_stride_A)—Offset 41120h" on page 1313	00000000h
41124h	4	"reg_isp_dma_DMA_CH9_dev_stride_A_type (isp_dma_DMA_CH9_dev_stride_A)—Offset 41124h" on page 1314	00000000h
41128h	4	"reg_isp_dma_DMA_CH10_dev_stride_A_type (isp_dma_DMA_CH10_dev_stride_A)—Offset 41128h" on page 1314	00000000h
4112Ch	4	"reg_isp_dma_DMA_CH11_dev_stride_A_type (isp_dma_DMA_CH11_dev_stride_A)—Offset 4112Ch" on page 1315	00000000h
41130h	4	"reg_isp_dma_DMA_CH12_dev_stride_A_type (isp_dma_DMA_CH12_dev_stride_A)—Offset 41130h" on page 1315	00000000h
41134h	4	"reg_isp_dma_DMA_CH13_dev_stride_A_type (isp_dma_DMA_CH13_dev_stride_A)—Offset 41134h" on page 1316	00000000h
41138h	4	"reg_isp_dma_DMA_CH14_dev_stride_A_type (isp_dma_DMA_CH14_dev_stride_A)—Offset 41138h" on page 1317	00000000h
4113Ch	4	"reg_isp_dma_DMA_CH15_dev_stride_A_type (isp_dma_DMA_CH15_dev_stride_A)—Offset 4113Ch" on page 1317	00000000h
41140h	4	"reg_isp_dma_DMA_CH16_dev_stride_A_type (isp_dma_DMA_CH16_dev_stride_A)—Offset 41140h" on page 1318	00000000h
41144h	4	"reg_isp_dma_DMA_CH17_dev_stride_A_type (isp_dma_DMA_CH17_dev_stride_A)—Offset 41144h" on page 1318	00000000h
41148h	4	"reg_isp_dma_DMA_CH18_dev_stride_A_type (isp_dma_DMA_CH18_dev_stride_A)—Offset 41148h" on page 1319	00000000h
4114Ch	4	"reg_isp_dma_DMA_CH19_dev_stride_A_type (isp_dma_DMA_CH19_dev_stride_A)—Offset 4114Ch" on page 1319	00000000h
41150h	4	"reg_isp_dma_DMA_CH20_dev_stride_A_type (isp_dma_DMA_CH20_dev_stride_A)—Offset 41150h" on page 1320	00000000h
41154h	4	"reg_isp_dma_DMA_CH21_dev_stride_A_type (isp_dma_DMA_CH21_dev_stride_A)—Offset 41154h" on page 1320	00000000h
41200h	4	"reg_isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 41200h" on page 1321	00000000h
41204h	4	"reg_isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A)—Offset 41204h" on page 1322	00000000h
41208h	4	"reg_isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A)—Offset 41208h" on page 1323	00000000h
4120Ch	4	"reg_isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A)—Offset 4120Ch" on page 1324	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41210h	4	"reg_isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A)—Offset 41210h" on page 1325	00000000h
41214h	4	"reg_isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A)—Offset 41214h" on page 1326	00000000h
41218h	4	"reg_isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A)—Offset 41218h" on page 1327	00000000h
4121Ch	4	"reg_isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A)—Offset 4121Ch" on page 1328	00000000h
41220h	4	"reg_isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A)—Offset 41220h" on page 1329	00000000h
41224h	4	"reg_isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A)—Offset 41224h" on page 1330	00000000h
41228h	4	"reg_isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A)—Offset 41228h" on page 1331	00000000h
4122Ch	4	"reg_isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A)—Offset 4122Ch" on page 1332	00000000h
41230h	4	"reg_isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A)—Offset 41230h" on page 1333	00000000h
41234h	4	"reg_isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A)—Offset 41234h" on page 1334	00000000h
41238h	4	"reg_isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A)—Offset 41238h" on page 1335	00000000h
4123Ch	4	"reg_isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A)—Offset 4123Ch" on page 1336	00000000h
41240h	4	"reg_isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A)—Offset 41240h" on page 1337	00000000h
41244h	4	"reg_isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A)—Offset 41244h" on page 1338	00000000h
41248h	4	"reg_isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A)—Offset 41248h" on page 1339	00000000h
4124Ch	4	"reg_isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A)—Offset 4124Ch" on page 1340	00000000h
41250h	4	"reg_isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A)—Offset 41250h" on page 1341	00000000h
41254h	4	"reg_isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A)—Offset 41254h" on page 1342	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41258h	4	"reg_isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A)—Offset 41258h" on page 1343	00000000h
4125Ch	4	"reg_isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A)—Offset 4125Ch" on page 1344	00000000h
41260h	4	"reg_isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A)—Offset 41260h" on page 1345	00000000h
41264h	4	"reg_isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A)—Offset 41264h" on page 1346	00000000h
41268h	4	"reg_isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A)—Offset 41268h" on page 1347	00000000h
4126Ch	4	"reg_isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A)—Offset 4126Ch" on page 1348	00000000h
41270h	4	"reg_isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A)—Offset 41270h" on page 1349	00000000h
41274h	4	"reg_isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A)—Offset 41274h" on page 1350	00000000h
41278h	4	"reg_isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A)—Offset 41278h" on page 1351	00000000h
4127Ch	4	"reg_isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A)—Offset 4127Ch" on page 1352	00000000h
412C0h	4	"reg_isp_dma_DMA_CH22_dev_stride_A_type (isp_dma_DMA_CH22_dev_stride_A)—Offset 412C0h" on page 1353	00000000h
412C4h	4	"reg_isp_dma_DMA_CH23_dev_stride_A_type (isp_dma_DMA_CH23_dev_stride_A)—Offset 412C4h" on page 1354	00000000h
412C8h	4	"reg_isp_dma_DMA_CH24_dev_stride_A_type (isp_dma_DMA_CH24_dev_stride_A)—Offset 412C8h" on page 1354	00000000h
412CCh	4	"reg_isp_dma_DMA_CH25_dev_stride_A_type (isp_dma_DMA_CH25_dev_stride_A)—Offset 412CCh" on page 1355	00000000h
412D0h	4	"reg_isp_dma_DMA_CH26_dev_stride_A_type (isp_dma_DMA_CH26_dev_stride_A)—Offset 412D0h" on page 1355	00000000h
412D4h	4	"reg_isp_dma_DMA_CH27_dev_stride_A_type (isp_dma_DMA_CH27_dev_stride_A)—Offset 412D4h" on page 1356	00000000h
412D8h	4	"reg_isp_dma_DMA_CH28_dev_stride_A_type (isp_dma_DMA_CH28_dev_stride_A)—Offset 412D8h" on page 1357	00000000h
412DCh	4	"reg_isp_dma_DMA_CH29_dev_stride_A_type (isp_dma_DMA_CH29_dev_stride_A)—Offset 412DCh" on page 1357	00000000h
412E0h	4	"reg_isp_dma_DMA_CH30_dev_stride_A_type (isp_dma_DMA_CH30_dev_stride_A)—Offset 412E0h" on page 1358	00000000h
412E4h	4	"reg_isp_dma_DMA_CH31_dev_stride_A_type (isp_dma_DMA_CH31_dev_stride_A)—Offset 412E4h" on page 1358	00000000h
41300h	4	"reg_isp_dma_DMA_CH0_Device_Xb_A_type (isp_dma_DMA_CH0_Device_Xb_A)—Offset 41300h" on page 1359	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41304h	4	"reg_isp_dma_DMA_CH1_Device_Xb_A_type (isp_dma_DMA_CH1_Device_Xb_A)—Offset 41304h" on page 1359	00000000h
41308h	4	"reg_isp_dma_DMA_CH2_Device_Xb_A_type (isp_dma_DMA_CH2_Device_Xb_A)—Offset 41308h" on page 1360	00000000h
4130Ch	4	"reg_isp_dma_DMA_CH3_Device_Xb_A_type (isp_dma_DMA_CH3_Device_Xb_A)—Offset 4130Ch" on page 1361	00000000h
41310h	4	"reg_isp_dma_DMA_CH4_Device_Xb_A_type (isp_dma_DMA_CH4_Device_Xb_A)—Offset 41310h" on page 1361	00000000h
41314h	4	"reg_isp_dma_DMA_CH5_Device_Xb_A_type (isp_dma_DMA_CH5_Device_Xb_A)—Offset 41314h" on page 1362	00000000h
41318h	4	"reg_isp_dma_DMA_CH6_Device_Xb_A_type (isp_dma_DMA_CH6_Device_Xb_A)—Offset 41318h" on page 1363	00000000h
4131Ch	4	"reg_isp_dma_DMA_CH7_Device_Xb_A_type (isp_dma_DMA_CH7_Device_Xb_A)—Offset 4131Ch" on page 1363	00000000h
41320h	4	"reg_isp_dma_DMA_CH8_Device_Xb_A_type (isp_dma_DMA_CH8_Device_Xb_A)—Offset 41320h" on page 1364	00000000h
41324h	4	"reg_isp_dma_DMA_CH9_Device_Xb_A_type (isp_dma_DMA_CH9_Device_Xb_A)—Offset 41324h" on page 1365	00000000h
41328h	4	"reg_isp_dma_DMA_CH10_Device_Xb_A_type (isp_dma_DMA_CH10_Device_Xb_A)—Offset 41328h" on page 1365	00000000h
4132Ch	4	"reg_isp_dma_DMA_CH11_Device_Xb_A_type (isp_dma_DMA_CH11_Device_Xb_A)—Offset 4132Ch" on page 1366	00000000h
41330h	4	"reg_isp_dma_DMA_CH12_Device_Xb_A_type (isp_dma_DMA_CH12_Device_Xb_A)—Offset 41330h" on page 1367	00000000h
41334h	4	"reg_isp_dma_DMA_CH13_Device_Xb_A_type (isp_dma_DMA_CH13_Device_Xb_A)—Offset 41334h" on page 1367	00000000h
41338h	4	"reg_isp_dma_DMA_CH14_Device_Xb_A_type (isp_dma_DMA_CH14_Device_Xb_A)—Offset 41338h" on page 1368	00000000h
4133Ch	4	"reg_isp_dma_DMA_CH15_Device_Xb_A_type (isp_dma_DMA_CH15_Device_Xb_A)—Offset 4133Ch" on page 1369	00000000h
41340h	4	"reg_isp_dma_DMA_CH16_Device_Xb_A_type (isp_dma_DMA_CH16_Device_Xb_A)—Offset 41340h" on page 1369	00000000h
41344h	4	"reg_isp_dma_DMA_CH17_Device_Xb_A_type (isp_dma_DMA_CH17_Device_Xb_A)—Offset 41344h" on page 1370	00000000h
41348h	4	"reg_isp_dma_DMA_CH18_Device_Xb_A_type (isp_dma_DMA_CH18_Device_Xb_A)—Offset 41348h" on page 1371	00000000h
4134Ch	4	"reg_isp_dma_DMA_CH19_Device_Xb_A_type (isp_dma_DMA_CH19_Device_Xb_A)—Offset 4134Ch" on page 1371	00000000h
41350h	4	"reg_isp_dma_DMA_CH20_Device_Xb_A_type (isp_dma_DMA_CH20_Device_Xb_A)—Offset 41350h" on page 1372	00000000h
41354h	4	"reg_isp_dma_DMA_CH21_Device_Xb_A_type (isp_dma_DMA_CH21_Device_Xb_A)—Offset 41354h" on page 1373	00000000h
41358h	4	"reg_isp_dma_DMA_CH22_Device_Xb_A_type (isp_dma_DMA_CH22_Device_Xb_A)—Offset 41358h" on page 1373	00000000h
4135Ch	4	"reg_isp_dma_DMA_CH23_Device_Xb_A_type (isp_dma_DMA_CH23_Device_Xb_A)—Offset 4135Ch" on page 1374	00000000h
41360h	4	"reg_isp_dma_DMA_CH24_Device_Xb_A_type (isp_dma_DMA_CH24_Device_Xb_A)—Offset 41360h" on page 1375	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41364h	4	"reg_isp_dma_DMA_CH25_Device_Xb_A_type (isp_dma_DMA_CH25_Device_Xb_A)—Offset 41364h" on page 1375	00000000h
41368h	4	"reg_isp_dma_DMA_CH26_Device_Xb_A_type (isp_dma_DMA_CH26_Device_Xb_A)—Offset 41368h" on page 1376	00000000h
4136Ch	4	"reg_isp_dma_DMA_CH27_Device_Xb_A_type (isp_dma_DMA_CH27_Device_Xb_A)—Offset 4136Ch" on page 1377	00000000h
41370h	4	"reg_isp_dma_DMA_CH28_Device_Xb_A_type (isp_dma_DMA_CH28_Device_Xb_A)—Offset 41370h" on page 1377	00000000h
41374h	4	"reg_isp_dma_DMA_CH29_Device_Xb_A_type (isp_dma_DMA_CH29_Device_Xb_A)—Offset 41374h" on page 1378	00000000h
41378h	4	"reg_isp_dma_DMA_CH30_Device_Xb_A_type (isp_dma_DMA_CH30_Device_Xb_A)—Offset 41378h" on page 1379	00000000h
4137Ch	4	"reg_isp_dma_DMA_CH31_Device_Xb_A_type (isp_dma_DMA_CH31_Device_Xb_A)—Offset 4137Ch" on page 1379	00000000h
41400h	4	"reg_isp_dma_DMA_CH0_dev_stride_B_type (isp_dma_DMA_CH0_dev_stride_B)—Offset 41400h" on page 1380	00000000h
41404h	4	"reg_isp_dma_DMA_CH1_dev_stride_B_type (isp_dma_DMA_CH1_dev_stride_B)—Offset 41404h" on page 1380	00000000h
41408h	4	"reg_isp_dma_DMA_CH2_dev_stride_B_type (isp_dma_DMA_CH2_dev_stride_B)—Offset 41408h" on page 1381	00000000h
4140Ch	4	"reg_isp_dma_DMA_CH3_dev_stride_B_type (isp_dma_DMA_CH3_dev_stride_B)—Offset 4140Ch" on page 1382	00000000h
41410h	4	"reg_isp_dma_DMA_CH4_dev_stride_B_type (isp_dma_DMA_CH4_dev_stride_B)—Offset 41410h" on page 1382	00000000h
41414h	4	"reg_isp_dma_DMA_CH5_dev_stride_B_type (isp_dma_DMA_CH5_dev_stride_B)—Offset 41414h" on page 1383	00000000h
41418h	4	"reg_isp_dma_DMA_CH6_dev_stride_B_type (isp_dma_DMA_CH6_dev_stride_B)—Offset 41418h" on page 1383	00000000h
4141Ch	4	"reg_isp_dma_DMA_CH7_dev_stride_B_type (isp_dma_DMA_CH7_dev_stride_B)—Offset 4141Ch" on page 1384	00000000h
41420h	4	"reg_isp_dma_DMA_CH8_dev_stride_B_type (isp_dma_DMA_CH8_dev_stride_B)—Offset 41420h" on page 1384	00000000h
41424h	4	"reg_isp_dma_DMA_CH9_dev_stride_B_type (isp_dma_DMA_CH9_dev_stride_B)—Offset 41424h" on page 1385	00000000h
41428h	4	"reg_isp_dma_DMA_CH10_dev_stride_B_type (isp_dma_DMA_CH10_dev_stride_B)—Offset 41428h" on page 1385	00000000h
4142Ch	4	"reg_isp_dma_DMA_CH11_dev_stride_B_type (isp_dma_DMA_CH11_dev_stride_B)—Offset 4142Ch" on page 1386	00000000h
41430h	4	"reg_isp_dma_DMA_CH12_dev_stride_B_type (isp_dma_DMA_CH12_dev_stride_B)—Offset 41430h" on page 1386	00000000h
41434h	4	"reg_isp_dma_DMA_CH13_dev_stride_B_type (isp_dma_DMA_CH13_dev_stride_B)—Offset 41434h" on page 1387	00000000h
41438h	4	"reg_isp_dma_DMA_CH14_dev_stride_B_type (isp_dma_DMA_CH14_dev_stride_B)—Offset 41438h" on page 1387	00000000h
4143Ch	4	"reg_isp_dma_DMA_CH15_dev_stride_B_type (isp_dma_DMA_CH15_dev_stride_B)—Offset 4143Ch" on page 1388	00000000h
41440h	4	"reg_isp_dma_DMA_CH16_dev_stride_B_type (isp_dma_DMA_CH16_dev_stride_B)—Offset 41440h" on page 1388	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41444h	4	"reg_isp_dma_DMA_CH17_dev_stride_B_type (isp_dma_DMA_CH17_dev_stride_B)—Offset 41444h" on page 1389	00000000h
41448h	4	"reg_isp_dma_DMA_CH18_dev_stride_B_type (isp_dma_DMA_CH18_dev_stride_B)—Offset 41448h" on page 1389	00000000h
4144Ch	4	"reg_isp_dma_DMA_CH19_dev_stride_B_type (isp_dma_DMA_CH19_dev_stride_B)—Offset 4144Ch" on page 1390	00000000h
41450h	4	"reg_isp_dma_DMA_CH20_dev_stride_B_type (isp_dma_DMA_CH20_dev_stride_B)—Offset 41450h" on page 1391	00000000h
41454h	4	"reg_isp_dma_DMA_CH21_dev_stride_B_type (isp_dma_DMA_CH21_dev_stride_B)—Offset 41454h" on page 1391	00000000h
41458h	4	"reg_isp_dma_DMA_CH22_dev_stride_B_type (isp_dma_DMA_CH22_dev_stride_B)—Offset 41458h" on page 1392	00000000h
4145Ch	4	"reg_isp_dma_DMA_CH23_dev_stride_B_type (isp_dma_DMA_CH23_dev_stride_B)—Offset 4145Ch" on page 1392	00000000h
41460h	4	"reg_isp_dma_DMA_CH24_dev_stride_B_type (isp_dma_DMA_CH24_dev_stride_B)—Offset 41460h" on page 1393	00000000h
41468h	4	"reg_isp_dma_DMA_CH26_dev_stride_B_type (isp_dma_DMA_CH26_dev_stride_B)—Offset 41468h" on page 1393	00000000h
4146Ch	4	"reg_isp_dma_DMA_CH27_dev_stride_B_type (isp_dma_DMA_CH27_dev_stride_B)—Offset 4146Ch" on page 1394	00000000h
41470h	4	"reg_isp_dma_DMA_CH28_dev_stride_B_type (isp_dma_DMA_CH28_dev_stride_B)—Offset 41470h" on page 1394	00000000h
41474h	4	"reg_isp_dma_DMA_CH29_dev_stride_B_type (isp_dma_DMA_CH29_dev_stride_B)—Offset 41474h" on page 1395	00000000h
41478h	4	"reg_isp_dma_DMA_CH30_dev_stride_B_type (isp_dma_DMA_CH30_dev_stride_B)—Offset 41478h" on page 1396	00000000h
4147Ch	4	"reg_isp_dma_DMA_CH31_dev_stride_B_type (isp_dma_DMA_CH31_dev_stride_B)—Offset 4147Ch" on page 1396	00000000h
41500h	4	"reg_isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 41500h" on page 1397	00000000h
41504h	4	"reg_isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B)—Offset 41504h" on page 1398	00000000h
41508h	4	"reg_isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B)—Offset 41508h" on page 1398	00000000h
4150Ch	4	"reg_isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B)—Offset 4150Ch" on page 1399	00000000h
41510h	4	"reg_isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B)—Offset 41510h" on page 1400	00000000h
41514h	4	"reg_isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B)—Offset 41514h" on page 1401	00000000h
41518h	4	"reg_isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B)—Offset 41518h" on page 1402	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
4151Ch	4	"reg_isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B)—Offset 4151Ch" on page 1403	00000000h
41520h	4	"reg_isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B)—Offset 41520h" on page 1404	00000000h
41524h	4	"reg_isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B)—Offset 41524h" on page 1405	00000000h
41528h	4	"reg_isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B)—Offset 41528h" on page 1406	00000000h
4152Ch	4	"reg_isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B)—Offset 4152Ch" on page 1407	00000000h
41530h	4	"reg_isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B)—Offset 41530h" on page 1408	00000000h
41534h	4	"reg_isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B)—Offset 41534h" on page 1409	00000000h
41538h	4	"reg_isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B)—Offset 41538h" on page 1410	00000000h
4153Ch	4	"reg_isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B)—Offset 4153Ch" on page 1411	00000000h
41540h	4	"reg_isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B)—Offset 41540h" on page 1412	00000000h
41544h	4	"reg_isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B)—Offset 41544h" on page 1413	00000000h
41548h	4	"reg_isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B)—Offset 41548h" on page 1414	00000000h
4154Ch	4	"reg_isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B)—Offset 4154Ch" on page 1415	00000000h
41550h	4	"reg_isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B)—Offset 41550h" on page 1416	00000000h
41554h	4	"reg_isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B)—Offset 41554h" on page 1417	00000000h
41558h	4	"reg_isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B)—Offset 41558h" on page 1418	00000000h
4155Ch	4	"reg_isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B)—Offset 4155Ch" on page 1419	00000000h
41560h	4	"reg_isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B)—Offset 41560h" on page 1420	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41564h	4	"reg_isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B)—Offset 41564h" on page 1421	00000000h
41568h	4	"reg_isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B)—Offset 41568h" on page 1422	00000000h
4156Ch	4	"reg_isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B)—Offset 4156Ch" on page 1423	00000000h
41570h	4	"reg_isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B)—Offset 41570h" on page 1424	00000000h
41574h	4	"reg_isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B)—Offset 41574h" on page 1425	00000000h
41578h	4	"reg_isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B)—Offset 41578h" on page 1426	00000000h
4157Ch	4	"reg_isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B)—Offset 4157Ch" on page 1427	00000000h
41600h	4	"reg_isp_dma_DMA_CH0_Device_Xb_B_type (isp_dma_DMA_CH0_Device_Xb_B)—Offset 41600h" on page 1428	00000000h
41604h	4	"reg_isp_dma_DMA_CH1_Device_Xb_B_type (isp_dma_DMA_CH1_Device_Xb_B)—Offset 41604h" on page 1429	00000000h
41608h	4	"reg_isp_dma_DMA_CH2_Device_Xb_B_type (isp_dma_DMA_CH2_Device_Xb_B)—Offset 41608h" on page 1430	00000000h
4160Ch	4	"reg_isp_dma_DMA_CH3_Device_Xb_B_type (isp_dma_DMA_CH3_Device_Xb_B)—Offset 4160Ch" on page 1430	00000000h
41610h	4	"reg_isp_dma_DMA_CH4_Device_Xb_B_type (isp_dma_DMA_CH4_Device_Xb_B)—Offset 41610h" on page 1431	00000000h
41614h	4	"reg_isp_dma_DMA_CH5_Device_Xb_B_type (isp_dma_DMA_CH5_Device_Xb_B)—Offset 41614h" on page 1432	00000000h
41618h	4	"reg_isp_dma_DMA_CH6_Device_Xb_B_type (isp_dma_DMA_CH6_Device_Xb_B)—Offset 41618h" on page 1432	00000000h
4161Ch	4	"reg_isp_dma_DMA_CH7_Device_Xb_B_type (isp_dma_DMA_CH7_Device_Xb_B)—Offset 4161Ch" on page 1433	00000000h
41620h	4	"reg_isp_dma_DMA_CH8_Device_Xb_B_type (isp_dma_DMA_CH8_Device_Xb_B)—Offset 41620h" on page 1434	00000000h
41624h	4	"reg_isp_dma_DMA_CH9_Device_Xb_B_type (isp_dma_DMA_CH9_Device_Xb_B)—Offset 41624h" on page 1434	00000000h
41628h	4	"reg_isp_dma_DMA_CH10_Device_Xb_B_type (isp_dma_DMA_CH10_Device_Xb_B)—Offset 41628h" on page 1435	00000000h
4162Ch	4	"reg_isp_dma_DMA_CH11_Device_Xb_B_type (isp_dma_DMA_CH11_Device_Xb_B)—Offset 4162Ch" on page 1436	00000000h
41630h	4	"reg_isp_dma_DMA_CH12_Device_Xb_B_type (isp_dma_DMA_CH12_Device_Xb_B)—Offset 41630h" on page 1436	00000000h
41634h	4	"reg_isp_dma_DMA_CH13_Device_Xb_B_type (isp_dma_DMA_CH13_Device_Xb_B)—Offset 41634h" on page 1437	00000000h
41638h	4	"reg_isp_dma_DMA_CH14_Device_Xb_B_type (isp_dma_DMA_CH14_Device_Xb_B)—Offset 41638h" on page 1438	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
4163Ch	4	"reg_isp_dma_DMA_CH15_Device_Xb_B_type (isp_dma_DMA_CH15_Device_Xb_B)—Offset 4163Ch" on page 1438	00000000h
41640h	4	"reg_isp_dma_DMA_CH16_Device_Xb_B_type (isp_dma_DMA_CH16_Device_Xb_B)—Offset 41640h" on page 1439	00000000h
41644h	4	"reg_isp_dma_DMA_CH17_Device_Xb_B_type (isp_dma_DMA_CH17_Device_Xb_B)—Offset 41644h" on page 1440	00000000h
41648h	4	"reg_isp_dma_DMA_CH18_Device_Xb_B_type (isp_dma_DMA_CH18_Device_Xb_B)—Offset 41648h" on page 1440	00000000h
4164Ch	4	"reg_isp_dma_DMA_CH19_Device_Xb_B_type (isp_dma_DMA_CH19_Device_Xb_B)—Offset 4164Ch" on page 1441	00000000h
41650h	4	"reg_isp_dma_DMA_CH20_Device_Xb_B_type (isp_dma_DMA_CH20_Device_Xb_B)—Offset 41650h" on page 1442	00000000h
41654h	4	"reg_isp_dma_DMA_CH21_Device_Xb_B_type (isp_dma_DMA_CH21_Device_Xb_B)—Offset 41654h" on page 1442	00000000h
41658h	4	"reg_isp_dma_DMA_CH22_Device_Xb_B_type (isp_dma_DMA_CH22_Device_Xb_B)—Offset 41658h" on page 1443	00000000h
4165Ch	4	"reg_isp_dma_DMA_CH23_Device_Xb_B_type (isp_dma_DMA_CH23_Device_Xb_B)—Offset 4165Ch" on page 1444	00000000h
41660h	4	"reg_isp_dma_DMA_CH24_Device_Xb_B_type (isp_dma_DMA_CH24_Device_Xb_B)—Offset 41660h" on page 1444	00000000h
41664h	4	"reg_isp_dma_DMA_CH25_Device_Xb_B_type (isp_dma_DMA_CH25_Device_Xb_B)—Offset 41664h" on page 1445	00000000h
41668h	4	"reg_isp_dma_DMA_CH26_Device_Xb_B_type (isp_dma_DMA_CH26_Device_Xb_B)—Offset 41668h" on page 1446	00000000h
4166Ch	4	"reg_isp_dma_DMA_CH27_Device_Xb_B_type (isp_dma_DMA_CH27_Device_Xb_B)—Offset 4166Ch" on page 1446	00000000h
41670h	4	"reg_isp_dma_DMA_CH28_Device_Xb_B_type (isp_dma_DMA_CH28_Device_Xb_B)—Offset 41670h" on page 1447	00000000h
41674h	4	"reg_isp_dma_DMA_CH29_Device_Xb_B_type (isp_dma_DMA_CH29_Device_Xb_B)—Offset 41674h" on page 1448	00000000h
41678h	4	"reg_isp_dma_DMA_CH31_Device_Xb_B_type (isp_dma_DMA_CH31_Device_Xb_B)—Offset 41678h" on page 1448	00000000h
41700h	4	"reg_isp_dma_DMA_CH0_Yb_type (isp_dma_DMA_CH0_Yb)—Offset 41700h" on page 1449	00000000h
41704h	4	"reg_isp_dma_DMA_CH1_Yb_type (isp_dma_DMA_CH1_Yb)—Offset 41704h" on page 1450	00000000h
41708h	4	"reg_isp_dma_DMA_CH2_Yb_type (isp_dma_DMA_CH2_Yb)—Offset 41708h" on page 1450	00000000h
4170Ch	4	"reg_isp_dma_DMA_CH3_Yb_type (isp_dma_DMA_CH3_Yb)—Offset 4170Ch" on page 1451	00000000h
41710h	4	"reg_isp_dma_DMA_CH4_Yb_type (isp_dma_DMA_CH4_Yb)—Offset 41710h" on page 1451	00000000h
41714h	4	"reg_isp_dma_DMA_CH5_Yb_type (isp_dma_DMA_CH5_Yb)—Offset 41714h" on page 1452	00000000h
41718h	4	"reg_isp_dma_DMA_CH6_Yb_type (isp_dma_DMA_CH6_Yb)—Offset 41718h" on page 1452	00000000h
4171Ch	4	"reg_isp_dma_DMA_CH7_Yb_type (isp_dma_DMA_CH7_Yb)—Offset 4171Ch" on page 1453	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41720h	4	"reg_isp_dma_DMA_CH8_Yb_type (isp_dma_DMA_CH8_Yb)—Offset 41720h" on page 1454	00000000h
41724h	4	"reg_isp_dma_DMA_CH9_Yb_type (isp_dma_DMA_CH9_Yb)—Offset 41724h" on page 1454	00000000h
41728h	4	"reg_isp_dma_DMA_CH10_Yb_type (isp_dma_DMA_CH10_Yb)—Offset 41728h" on page 1455	00000000h
4172Ch	4	"reg_isp_dma_DMA_CH11_Yb_type (isp_dma_DMA_CH11_Yb)—Offset 4172Ch" on page 1455	00000000h
41730h	4	"reg_isp_dma_DMA_CH12_Yb_type (isp_dma_DMA_CH12_Yb)—Offset 41730h" on page 1456	00000000h
41734h	4	"reg_isp_dma_DMA_CH13_Yb_type (isp_dma_DMA_CH13_Yb)—Offset 41734h" on page 1456	00000000h
41738h	4	"reg_isp_dma_DMA_CH14_Yb_type (isp_dma_DMA_CH14_Yb)—Offset 41738h" on page 1457	00000000h
4173Ch	4	"reg_isp_dma_DMA_CH15_Yb_type (isp_dma_DMA_CH15_Yb)—Offset 4173Ch" on page 1458	00000000h
41740h	4	"reg_isp_dma_DMA_CH16_Yb_type (isp_dma_DMA_CH16_Yb)—Offset 41740h" on page 1458	00000000h
41744h	4	"reg_isp_dma_DMA_CH17_Yb_type (isp_dma_DMA_CH17_Yb)—Offset 41744h" on page 1459	00000000h
41748h	4	"reg_isp_dma_DMA_CH18_Yb_type (isp_dma_DMA_CH18_Yb)—Offset 41748h" on page 1459	00000000h
4174Ch	4	"reg_isp_dma_DMA_CH19_Yb_type (isp_dma_DMA_CH19_Yb)—Offset 4174Ch" on page 1460	00000000h
41750h	4	"reg_isp_dma_DMA_CH20_Yb_type (isp_dma_DMA_CH20_Yb)—Offset 41750h" on page 1460	00000000h
41754h	4	"reg_isp_dma_DMA_CH21_Yb_type (isp_dma_DMA_CH21_Yb)—Offset 41754h" on page 1461	00000000h
41758h	4	"reg_isp_dma_DMA_CH22_Yb_type (isp_dma_DMA_CH22_Yb)—Offset 41758h" on page 1462	00000000h
4175Ch	4	"reg_isp_dma_DMA_CH23_Yb_type (isp_dma_DMA_CH23_Yb)—Offset 4175Ch" on page 1462	00000000h
41760h	4	"reg_isp_dma_DMA_CH24_Yb_type (isp_dma_DMA_CH24_Yb)—Offset 41760h" on page 1463	00000000h
41764h	4	"reg_isp_dma_DMA_CH25_Yb_type (isp_dma_DMA_CH25_Yb)—Offset 41764h" on page 1463	00000000h
41768h	4	"reg_isp_dma_DMA_CH26_Yb_type (isp_dma_DMA_CH26_Yb)—Offset 41768h" on page 1464	00000000h
4176Ch	4	"reg_isp_dma_DMA_CH27_Yb_type (isp_dma_DMA_CH27_Yb)—Offset 4176Ch" on page 1464	00000000h
41770h	4	"reg_isp_dma_DMA_CH28_Yb_type (isp_dma_DMA_CH28_Yb)—Offset 41770h" on page 1465	00000000h
41774h	4	"reg_isp_dma_DMA_CH29_Yb_type (isp_dma_DMA_CH29_Yb)—Offset 41774h" on page 1466	00000000h
4177Ch	4	"reg_isp_dma_DMA_CH31_Yb_type (isp_dma_DMA_CH31_Yb)—Offset 4177Ch" on page 1466	00000000h
41800h	4	"reg_isp_dma_DMA_CH0_pending_command_type (isp_dma_DMA_CH0_pending_command)—Offset 41800h" on page 1467	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41804h	4	"reg_isp_dma_DMA_CH1_pending_command_type (isp_dma_DMA_CH1_pending_command)—Offset 41804h" on page 1467	00000000h
41808h	4	"reg_isp_dma_DMA_CH2_pending_command_type (isp_dma_DMA_CH2_pending_command)—Offset 41808h" on page 1468	00000000h
4180Ch	4	"reg_isp_dma_DMA_CH3_pending_command_type (isp_dma_DMA_CH3_pending_command)—Offset 4180Ch" on page 1469	00000000h
41810h	4	"reg_isp_dma_DMA_CH4_pending_command_type (isp_dma_DMA_CH4_pending_command)—Offset 41810h" on page 1469	00000000h
41814h	4	"reg_isp_dma_DMA_CH5_pending_command_type (isp_dma_DMA_CH5_pending_command)—Offset 41814h" on page 1470	00000000h
41818h	4	"reg_isp_dma_DMA_CH6_pending_command_type (isp_dma_DMA_CH6_pending_command)—Offset 41818h" on page 1471	00000000h
4181Ch	4	"reg_isp_dma_DMA_CH7_pending_command_type (isp_dma_DMA_CH7_pending_command)—Offset 4181Ch" on page 1471	00000000h
41820h	4	"reg_isp_dma_DMA_CH8_pending_command_type (isp_dma_DMA_CH8_pending_command)—Offset 41820h" on page 1472	00000000h
41824h	4	"reg_isp_dma_DMA_CH9_pending_command_type (isp_dma_DMA_CH9_pending_command)—Offset 41824h" on page 1473	00000000h
41828h	4	"reg_isp_dma_DMA_CH10_pending_command_type (isp_dma_DMA_CH10_pending_command)—Offset 41828h" on page 1473	00000000h
4182Ch	4	"reg_isp_dma_DMA_CH11_pending_command_type (isp_dma_DMA_CH11_pending_command)—Offset 4182Ch" on page 1474	00000000h
41830h	4	"reg_isp_dma_DMA_CH12_pending_command_type (isp_dma_DMA_CH12_pending_command)—Offset 41830h" on page 1475	00000000h
41834h	4	"reg_isp_dma_DMA_CH13_pending_command_type (isp_dma_DMA_CH13_pending_command)—Offset 41834h" on page 1475	00000000h
41838h	4	"reg_isp_dma_DMA_CH14_pending_command_type (isp_dma_DMA_CH14_pending_command)—Offset 41838h" on page 1476	00000000h
4183Ch	4	"reg_isp_dma_DMA_CH15_pending_command_type (isp_dma_DMA_CH15_pending_command)—Offset 4183Ch" on page 1477	00000000h
41840h	4	"reg_isp_dma_DMA_CH16_pending_command_type (isp_dma_DMA_CH16_pending_command)—Offset 41840h" on page 1477	00000000h
41844h	4	"reg_isp_dma_DMA_CH17_pending_command_type (isp_dma_DMA_CH17_pending_command)—Offset 41844h" on page 1478	00000000h
41848h	4	"reg_isp_dma_DMA_CH18_pending_command_type (isp_dma_DMA_CH18_pending_command)—Offset 41848h" on page 1479	00000000h
4184Ch	4	"reg_isp_dma_DMA_CH19_pending_command_type (isp_dma_DMA_CH19_pending_command)—Offset 4184Ch" on page 1479	00000000h
41850h	4	"reg_isp_dma_DMA_CH20_pending_command_type (isp_dma_DMA_CH20_pending_command)—Offset 41850h" on page 1480	00000000h
41854h	4	"reg_isp_dma_DMA_CH21_pending_command_type (isp_dma_DMA_CH21_pending_command)—Offset 41854h" on page 1481	00000000h
41858h	4	"reg_isp_dma_DMA_CH22_pending_command_type (isp_dma_DMA_CH22_pending_command)—Offset 41858h" on page 1481	00000000h
4185Ch	4	"reg_isp_dma_DMA_CH23_pending_command_type (isp_dma_DMA_CH23_pending_command)—Offset 4185Ch" on page 1482	00000000h
41860h	4	"reg_isp_dma_DMA_CH24_pending_command_type (isp_dma_DMA_CH24_pending_command)—Offset 41860h" on page 1483	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
41864h	4	“reg_isp_dma_DMA_CH25_pending_command_type (isp_dma_DMA_CH25_pending_command)—Offset 41864h” on page 1483	00000000h
41868h	4	“reg_isp_dma_DMA_CH26_pending_command_type (isp_dma_DMA_CH26_pending_command)—Offset 41868h” on page 1484	00000000h
4186Ch	4	“reg_isp_dma_DMA_CH27_pending_command_type (isp_dma_DMA_CH27_pending_command)—Offset 4186Ch” on page 1485	00000000h
41870h	4	“reg_isp_dma_DMA_CH28_pending_command_type (isp_dma_DMA_CH28_pending_command)—Offset 41870h” on page 1485	00000000h
41874h	4	“reg_isp_dma_DMA_CH29_pending_command_type (isp_dma_DMA_CH29_pending_command)—Offset 41874h” on page 1486	00000000h
41878h	4	“reg_isp_dma_DMA_CH30_pending_command_type (isp_dma_DMA_CH30_pending_command)—Offset 41878h” on page 1487	00000000h
4187Ch	4	“reg_isp_dma_DMA_CH31_pending_command_type (isp_dma_DMA_CH31_pending_command)—Offset 4187Ch” on page 1487	00000000h
42000h	4	“reg_isp_dma_DMA_command_token_type (isp_dma_DMA_command_token)—Offset 42000h” on page 1488	00000000h
42004h	4	“reg_isp_dma_DMA_command_src_addr_type (isp_dma_DMA_command_src_addr)—Offset 42004h” on page 1489	00000000h
42008h	4	“reg_isp_dma_DMA_command_dst_addr_type (isp_dma_DMA_command_dst_addr)—Offset 42008h” on page 1489	00000000h
4200Ch	4	“reg_isp_dma_DMA_command_ctrl_id_type (isp_dma_DMA_command_ctrl_id)—Offset 4200Ch” on page 1490	00000000h
42010h	4	“reg_isp_dma_DMA_FSM_Ctrl_status_type (isp_dma_DMA_FSM_Ctrl_status)—Offset 42010h” on page 1490	00000001h
42014h	4	“reg_isp_dma_DMA_FSM_Pack_status_type (isp_dma_DMA_FSM_Pack_status)—Offset 42014h” on page 1491	00000001h
42018h	4	“reg_isp_dma_DMA_FSM_request_status_type (isp_dma_DMA_FSM_request_status)—Offset 42018h” on page 1492	00000000h
4201Ch	4	“reg_isp_dma_DMA_FSM_write_status_type (isp_dma_DMA_FSM_write_status)—Offset 4201Ch” on page 1493	00000000h
42110h	4	“reg_isp_dma_DMA_FSM_Ctrl_dev_idx_type (isp_dma_DMA_FSM_Ctrl_dev_idx)—Offset 42110h” on page 1493	00000000h
42114h	4	“reg_isp_dma_DMA_FSM_Pack_cnt_Yb_type (isp_dma_DMA_FSM_Pack_cnt_Yb)—Offset 42114h” on page 1494	00000000h
42118h	4	“reg_isp_dma_DMA_FSM_Request_cnt_Yb_type (isp_dma_DMA_FSM_Request_cnt_Yb)—Offset 42118h” on page 1495	00000000h
4211Ch	4	“reg_isp_dma_DMA_FSM_Write_cnt_Y_type (isp_dma_DMA_FSM_Write_cnt_Y)—Offset 4211Ch” on page 1495	00000000h
42210h	4	“reg_isp_dma_DMA_FSM_Ctrl_req_addr_type (isp_dma_DMA_FSM_Ctrl_req_addr)—Offset 42210h” on page 1496	00000000h
42214h	4	“reg_isp_dma_DMA_FSM_Pack_req_cnt_Xb_type (isp_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 42214h” on page 1496	00000000h
42218h	4	“reg_isp_dma_DMA_FSM_Request_cnt_Xb_type (isp_dma_DMA_FSM_Request_cnt_Xb)—Offset 42218h” on page 1497	00000000h
4221Ch	4	“reg_isp_dma_DMA_FSM_Write_cnt_Xb_type (isp_dma_DMA_FSM_Write_cnt_Xb)—Offset 4221Ch” on page 1498	00000000h
42310h	4	“reg_isp_dma_DMA_FSM_Ctrl_req_stride_type (isp_dma_DMA_FSM_Ctrl_req_stride)—Offset 42310h” on page 1499	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
42314h	4	"reg_isp_dma_DMA_FSM_Pack_wr_cnt_Xb_type (isp_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 42314h" on page 1499	00000000h
42318h	4	"reg_isp_dma_DMA_FSM_Req_remining_Xb_type (isp_dma_DMA_FSM_Req_remining_Xb)—Offset 42318h" on page 1500	00000000h
4231Ch	4	"reg_isp_dma_DMA_FSM_Wr_remining_Xb_type (isp_dma_DMA_FSM_Wr_remining_Xb)—Offset 4231Ch" on page 1501	00000000h
42410h	4	"reg_isp_dma_DMA_FSM_Ctrl_req_Xb_type (isp_dma_DMA_FSM_Ctrl_req_Xb)—Offset 42410h" on page 1501	00000000h
42418h	4	"reg_isp_dma_DMA_FSM_Req_burst_cnt_type (isp_dma_DMA_FSM_Req_burst_cnt)—Offset 42418h" on page 1502	0000FFFFh
4241Ch	4	"reg_isp_dma_DMA_FSM_Wr_burst_cnt_type (isp_dma_DMA_FSM_Wr_burst_cnt)—Offset 4241Ch" on page 1503	0000FFFFh
42510h	4	"reg_isp_dma_DMA_FSM_Ctrl_req_Yb_type (isp_dma_DMA_FSM_Ctrl_req_Yb)—Offset 42510h" on page 1503	00000000h
42610h	4	"reg_isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx_type (isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 42610h" on page 1504	00000000h
42710h	4	"reg_isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx_type (isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 42710h" on page 1505	00000000h
42810h	4	"reg_isp_dma_DMA_FSM_Ctrl_Wr_addr_type (isp_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 42810h" on page 1505	00000000h
42910h	4	"reg_isp_dma_DMA_FSM_Ctrl_Wr_stride_type (isp_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 42910h" on page 1506	00000000h
42A10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_req_Xb_type (isp_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 42A10h" on page 1506	00000000h
42B10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_Yb_type (isp_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 42B10h" on page 1507	00000000h
42C10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_wr_Xb_type (isp_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 42C10h" on page 1508	00000000h
42D10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_req_elem_type (isp_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 42D10h" on page 1508	00000000h
42E10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_wr_elem_type (isp_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 42E10h" on page 1509	00000000h
42F10h	4	"reg_isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id_type (isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 42F10h" on page 1510	00000000h
43000h	4	"reg_isp_dma_Dev_Interf_0_req_side_type (isp_dma_Dev_Interf_0_req_side)—Offset 43000h" on page 1511	00000000h
43004h	4	"reg_isp_dma_Dev_Interf_1_req_side_type (isp_dma_Dev_Interf_1_req_side)—Offset 43004h" on page 1511	00000006h
43008h	4	"reg_isp_dma_Dev_Interf_2_req_side_type (isp_dma_Dev_Interf_2_req_side)—Offset 43008h" on page 1512	00000006h
43100h	4	"reg_isp_dma_Dev_Interf_0_snd_side_type (isp_dma_Dev_Interf_0_snd_side)—Offset 43100h" on page 1513	00000004h
43104h	4	"reg_isp_dma_Dev_Interf_1_snd_side_type (isp_dma_Dev_Interf_1_snd_side)—Offset 43104h" on page 1514	00000006h
43108h	4	"reg_isp_dma_Dev_Interf_2_snd_side_type (isp_dma_Dev_Interf_2_snd_side)—Offset 43108h" on page 1514	00000006h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
43200h	4	"reg_isp_dma_Dev_Interf_0_Fifo_status_type (isp_dma_Dev_Interf_0_Fifo_status)—Offset 43200h" on page 1515	00000004h
43204h	4	"reg_isp_dma_Dev_Interf_1_Fifo_status_type (isp_dma_Dev_Interf_1_Fifo_status)—Offset 43204h" on page 1516	00000004h
43208h	4	"reg_isp_dma_Dev_Interf_2_Fifo_status_type (isp_dma_Dev_Interf_2_Fifo_status)—Offset 43208h" on page 1517	00000004h
43300h	4	"reg_isp_dma_Dev_Interf_0_Req_complete_bust_type (isp_dma_Dev_Interf_0_Req_complete_bust)—Offset 43300h" on page 1518	00000000h
43304h	4	"reg_isp_dma_Dev_Interf_1_Req_complete_bust_type (isp_dma_Dev_Interf_1_Req_complete_bust)—Offset 43304h" on page 1519	00000000h
43308h	4	"reg_isp_dma_Dev_Interf_2_Req_complete_bust_type (isp_dma_Dev_Interf_2_Req_complete_bust)—Offset 43308h" on page 1520	00000000h
43408h	4	"reg_isp_dma_Dev_Interf_2_Max_burst_Size_type (isp_dma_Dev_Interf_2_Max_burst_Size)—Offset 43408h" on page 1520	0000007Fh
50000h	4	"reg_gdc1_reg0_type (gdc1_reg0)—Offset 50000h" on page 1521	00000000h
50004h	4	"reg_gdc1_woi_x_type (gdc1_woi_x)—Offset 50004h" on page 1522	00000000h
50008h	4	"reg_gdc1_woi_y_type (gdc1_woi_y)—Offset 50008h" on page 1522	00000000h
5000Ch	4	"reg_gdc1_bpp_type (gdc1_bpp)—Offset 5000Ch" on page 1523	00000000h
50010h	4	"reg_gdc1_fryipxfrx_start_type (gdc1_fryipxfrx_start)—Offset 50010h" on page 1523	00000000h
50014h	4	"reg_gdc1_oxdim_type (gdc1_oxdim)—Offset 50014h" on page 1524	00000000h
50018h	4	"reg_gdc1_oydim_type (gdc1_oydim)—Offset 50018h" on page 1524	00000000h
5001Ch	4	"reg_gdc1_src_addr_type (gdc1_src_addr)—Offset 5001Ch" on page 1525	00000000h
50020h	4	"reg_gdc1_src_end_type (gdc1_src_end)—Offset 50020h" on page 1525	00000000h
50024h	4	"reg_gdc1_src_wrap_type (gdc1_src_wrap)—Offset 50024h" on page 1526	00000000h
50028h	4	"reg_gdc1_src_stride_type (gdc1_src_stride)—Offset 50028h" on page 1526	00000000h
5002Ch	4	"reg_gdc1_dst_addr_type (gdc1_dst_addr)—Offset 5002Ch" on page 1527	00000000h
50030h	4	"reg_gdc1_dst_stride_type (gdc1_dst_stride)—Offset 50030h" on page 1527	00000000h
50034h	4	"reg_gdc1_dx_type (gdc1_dx)—Offset 50034h" on page 1528	00000000h
50038h	4	"reg_gdc1_dy_type (gdc1_dy)—Offset 50038h" on page 1528	00000000h
5003Ch	4	"reg_gdc1_P0_primX_ixdim_type (gdc1_P0_primX_ixdim)—Offset 5003Ch" on page 1529	00000000h
50040h	4	"reg_gdc1_P0_primY_iydim_type (gdc1_P0_primY_iydim)—Offset 50040h" on page 1529	00000000h
50044h	4	"reg_gdc1_P1_primX_type (gdc1_P1_primX)—Offset 50044h" on page 1530	00000000h
50048h	4	"reg_gdc1_P1_primY_type (gdc1_P1_primY)—Offset 50048h" on page 1530	00000000h
5004Ch	4	"reg_gdc1_P2_primX_type (gdc1_P2_primX)—Offset 5004Ch" on page 1531	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
50050h	4	"reg_gdc1_P2_primY_type (gdc1_P2_primY)—Offset 50050h" on page 1531	00000000h
50054h	4	"reg_gdc1_P3_primX_type (gdc1_P3_primX)—Offset 50054h" on page 1532	00000000h
50058h	4	"reg_gdc1_P3_primY_type (gdc1_P3_primY)—Offset 50058h" on page 1532	00000000h
5005Ch	4	"reg_gdc1_perf_mode_type (gdc1_perf_mode)—Offset 5005Ch" on page 1533	00000000h
50060h	4	"reg_gdc1_interp_type_type (gdc1_interp_type)—Offset 50060h" on page 1534	00000000h
50064h	4	"reg_gdc1_scan_mode_type (gdc1_scan_mode)—Offset 50064h" on page 1534	00000000h
50068h	4	"reg_gdc1_proc_mode_type (gdc1_proc_mode)—Offset 50068h" on page 1535	00000000h
60000h	4	"reg_gdc2_reg0_type (gdc2_reg0)—Offset 60000h" on page 1535	00000000h
60004h	4	"reg_gdc2_woi_x_type (gdc2_woi_x)—Offset 60004h" on page 1536	00000000h
60008h	4	"reg_gdc2_woi_y_type (gdc2_woi_y)—Offset 60008h" on page 1536	00000000h
6000Ch	4	"reg_gdc2_bpp_type (gdc2_bpp)—Offset 6000Ch" on page 1537	00000000h
60010h	4	"reg_gdc2_fryipxfrx_start_type (gdc2_fryipxfrx_start)—Offset 60010h" on page 1537	00000000h
60014h	4	"reg_gdc2_oxdim_type (gdc2_oxdim)—Offset 60014h" on page 1538	00000000h
60018h	4	"reg_gdc2_oydim_type (gdc2_oydim)—Offset 60018h" on page 1538	00000000h
6001Ch	4	"reg_gdc2_src_addr_type (gdc2_src_addr)—Offset 6001Ch" on page 1539	00000000h
60020h	4	"reg_gdc2_src_end_type (gdc2_src_end)—Offset 60020h" on page 1539	00000000h
60024h	4	"reg_gdc2_src_wrap_type (gdc2_src_wrap)—Offset 60024h" on page 1540	00000000h
60028h	4	"reg_gdc2_src_stride_type (gdc2_src_stride)—Offset 60028h" on page 1540	00000000h
6002Ch	4	"reg_gdc2_dst_addr_type (gdc2_dst_addr)—Offset 6002Ch" on page 1541	00000000h
60030h	4	"reg_gdc2_dst_stride_type (gdc2_dst_stride)—Offset 60030h" on page 1541	00000000h
60034h	4	"reg_gdc2_dx_type (gdc2_dx)—Offset 60034h" on page 1542	00000000h
60038h	4	"reg_gdc2_dy_type (gdc2_dy)—Offset 60038h" on page 1542	00000000h
6003Ch	4	"reg_gdc2_P0_primX_ixdim_type (gdc2_P0_primX_ixdim)—Offset 6003Ch" on page 1543	00000000h
60040h	4	"reg_gdc2_P0_primY_iydim_type (gdc2_P0_primY_iydim)—Offset 60040h" on page 1543	00000000h
60044h	4	"reg_gdc2_P1_primX_type (gdc2_P1_primX)—Offset 60044h" on page 1544	00000000h
60048h	4	"reg_gdc2_P1_primY_type (gdc2_P1_primY)—Offset 60048h" on page 1544	00000000h
6004Ch	4	"reg_gdc2_P2_primX_type (gdc2_P2_primX)—Offset 6004Ch" on page 1545	00000000h
60050h	4	"reg_gdc2_P2_primY_type (gdc2_P2_primY)—Offset 60050h" on page 1545	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
60054h	4	"reg_gdc2_P3_primX_type (gdc2_P3_primX)—Offset 60054h" on page 1546	00000000h
60058h	4	"reg_gdc2_P3_primY_type (gdc2_P3_primY)—Offset 60058h" on page 1546	00000000h
6005Ch	4	"reg_gdc2_perf_mode_type (gdc2_perf_mode)—Offset 6005Ch" on page 1547	00000000h
60060h	4	"reg_gdc2_interp_type_type (gdc2_interp_type)—Offset 60060h" on page 1548	00000000h
60064h	4	"reg_gdc2_scan_mode_type (gdc2_scan_mode)—Offset 60064h" on page 1548	00000000h
60068h	4	"reg_gdc2_proc_mode_type (gdc2_proc_mode)—Offset 60068h" on page 1549	00000000h
70000h	4	"reg_data_out_sys_c_mmu_MMU_invalidate_cache_type (data_out_sys_c_mmu_MMU_invalidate_cache)—Offset 70000h" on page 1549	00000000h
70004h	4	"reg_data_out_sys_c_mmu_MMU_page_table_base_type (data_out_sys_c_mmu_MMU_page_table_base)—Offset 70004h" on page 1550	00000000h
80100h	4	"reg_inp_sys_csi_receiver_csi1_dev_ready_type (inp_sys_csi_receiver_csi1_dev_ready)—Offset 80100h" on page 1550	00000000h
80104h	4	"reg_inp_sys_csi_receiver_csi1_int_status_type (inp_sys_csi_receiver_csi1_int_status)—Offset 80104h" on page 1551	00000000h
80108h	4	"reg_inp_sys_csi_receiver_csi1_int_enable_type (inp_sys_csi_receiver_csi1_int_enable)—Offset 80108h" on page 1553	00000000h
8010Ch	4	"reg_inp_sys_csi_receiver_csi1_func_prg_type (inp_sys_csi_receiver_csi1_func_prg)—Offset 8010Ch" on page 1554	0007FFFFh
80110h	4	"reg_inp_sys_csi_receiver_csi1_init_cnt_type (inp_sys_csi_receiver_csi1_init_cnt)—Offset 80110h" on page 1555	00000000h
8011Ch	4	"reg_inp_sys_csi_receiver_csi_backend_fs_ls_type (inp_sys_csi_receiver_csi_backend_fs_ls)—Offset 8011Ch" on page 1555	00000002h
80120h	4	"reg_inp_sys_csi_receiver_csi_backend_ls_dvalid_type (inp_sys_csi_receiver_csi_backend_ls_dvalid)—Offset 80120h" on page 1556	00000002h
80124h	4	"reg_inp_sys_csi_receiver_csi_backend_dvalid_le_type (inp_sys_csi_receiver_csi_backend_dvalid_le)—Offset 80124h" on page 1557	00000002h
80128h	4	"reg_inp_sys_csi_receiver_csi_backend_le_fe_type (inp_sys_csi_receiver_csi_backend_le_fe)—Offset 80128h" on page 1557	00000002h
8012Ch	4	"reg_inp_sys_csi_receiver_csi_backend_fe_fs_type (inp_sys_csi_receiver_csi_backend_fe_fs)—Offset 8012Ch" on page 1558	00000002h
80130h	4	"reg_inp_sys_csi_receiver_csi_backend_le_ls_type (inp_sys_csi_receiver_csi_backend_le_ls)—Offset 80130h" on page 1559	00000004h
80134h	4	"reg_inp_sys_csi_receiver_csi_backend_two_pixel_en_type (inp_sys_csi_receiver_csi_backend_two_pixel_en)—Offset 80134h" on page 1559	00000000h
80138h	4	"reg_inp_sys_csi_receiver_csi1_raw16_18_data_id_type (inp_sys_csi_receiver_csi1_raw16_18_data_id)—Offset 80138h" on page 1560	00000000h
8013Ch	4	"reg_inp_sys_csi_receiver_csi1_sync_cnt_type (inp_sys_csi_receiver_csi1_sync_cnt)—Offset 8013Ch" on page 1561	FFFFFFFFh

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
80140h	4	"reg_inp_sys_csi_receiver_csi1_rx_cnt_type (inp_sys_csi_receiver_csi1_rx_cnt)—Offset 80140h" on page 1561	FFFFFFFFh
80144h	4	"reg_inp_sys_csi_receiver_csi_backend_rst_type (inp_sys_csi_receiver_csi_backend_rst)—Offset 80144h" on page 1562	00000000h
80148h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0)—Offset 80148h" on page 1563	00000000h
8014Ch	4	"reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc0_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc0)—Offset 8014Ch" on page 1564	00000000h
80150h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1)—Offset 80150h" on page 1565	00000000h
80154h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc1_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc1)—Offset 80154h" on page 1566	00000000h
80158h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2)—Offset 80158h" on page 1567	00000000h
8015Ch	4	"reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc2_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc2)—Offset 8015Ch" on page 1569	00000000h
80160h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3)—Offset 80160h" on page 1569	00000000h
80164h	4	"reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc3_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc3)—Offset 80164h" on page 1571	00000000h
80168h	4	"reg_inp_sys_csi_receiver_csi_backend_raw18_reg_type (inp_sys_csi_receiver_csi_backend_raw18_reg)—Offset 80168h" on page 1572	00000000h
8016Ch	4	"reg_inp_sys_csi_receiver_csi_backend_force_raw8_reg_type (inp_sys_csi_receiver_csi_backend_force_raw8_reg)—Offset 8016Ch" on page 1572	00000000h
80170h	4	"reg_inp_sys_csi_receiver_csi_backend_raw16_reg_type (inp_sys_csi_receiver_csi_backend_raw16_reg)—Offset 80170h" on page 1573	00000000h
80200h	4	"reg_inp_sys_csi_receiver_csi2_dev_ready_type (inp_sys_csi_receiver_csi2_dev_ready)—Offset 80200h" on page 1574	00000000h
80204h	4	"reg_inp_sys_csi_receiver_csi2_int_status_type (inp_sys_csi_receiver_csi2_int_status)—Offset 80204h" on page 1575	00000000h
80208h	4	"reg_inp_sys_csi_receiver_csi2_int_enable_type (inp_sys_csi_receiver_csi2_int_enable)—Offset 80208h" on page 1576	00000000h
8020Ch	4	"reg_inp_sys_csi_receiver_csi2_func_prg_type (inp_sys_csi_receiver_csi2_func_prg)—Offset 8020Ch" on page 1577	0007FFFFh
80210h	4	"reg_inp_sys_csi_receiver_csi2_init_cnt_type (inp_sys_csi_receiver_csi2_init_cnt)—Offset 80210h" on page 1578	00000000h
80238h	4	"reg_inp_sys_csi_receiver_csi2_raw16_18_data_id_type (inp_sys_csi_receiver_csi2_raw16_18_data_id)—Offset 80238h" on page 1579	00000000h
8023Ch	4	"reg_inp_sys_csi_receiver_csi2_sync_cnt_type (inp_sys_csi_receiver_csi2_sync_cnt)—Offset 8023Ch" on page 1579	000000FFh

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
80240h	4	"reg_inp_sys_csi_receiver_csi2_rx_cnt_type (inp_sys_csi_receiver_csi2_rx_cnt)—Offset 80240h" on page 1580	000000FFh
80300h	4	"reg_inp_sys_csi_receiver_csi3_dev_ready_type (inp_sys_csi_receiver_csi3_dev_ready)—Offset 80300h" on page 1581	00000000h
80304h	4	"reg_inp_sys_csi_receiver_csi3_int_status_type (inp_sys_csi_receiver_csi3_int_status)—Offset 80304h" on page 1581	00000000h
80308h	4	"reg_inp_sys_csi_receiver_csi3_int_enable_type (inp_sys_csi_receiver_csi3_int_enable)—Offset 80308h" on page 1583	00000000h
8030Ch	4	"reg_inp_sys_csi_receiver_csi3_func_prg_type (inp_sys_csi_receiver_csi3_func_prg)—Offset 8030Ch" on page 1584	0007FFFFh
80310h	4	"reg_inp_sys_csi_receiver_csi3_init_cnt_type (inp_sys_csi_receiver_csi3_init_cnt)—Offset 80310h" on page 1585	00000000h
80338h	4	"reg_inp_sys_csi_receiver_csi3_raw16_18_data_id_type (inp_sys_csi_receiver_csi3_raw16_18_data_id)—Offset 80338h" on page 1585	00000000h
8033Ch	4	"reg_inp_sys_csi_receiver_csi3_sync_cnt_type (inp_sys_csi_receiver_csi3_sync_cnt)—Offset 8033Ch" on page 1586	0000FFFFh
80340h	4	"reg_inp_sys_csi_receiver_csi3_rx_cnt_type (inp_sys_csi_receiver_csi3_rx_cnt)—Offset 80340h" on page 1587	00000000h
80800h	4	"reg_inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl_type (inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl)—Offset 80800h" on page 1588	00000000h
80804h	4	"reg_inp_sys_csi_receiver_csi_sh_be_srst_type (inp_sys_csi_receiver_csi_sh_be_srst)—Offset 80804h" on page 1588	00000000h
80808h	4	"reg_inp_sys_csi_receiver_csi_sh_be_two_ppc_type (inp_sys_csi_receiver_csi_sh_be_two_ppc)—Offset 80808h" on page 1589	00000000h
8080Ch	4	"reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0)—Offset 8080Ch" on page 1590	00000000h
80810h	4	"reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1)—Offset 80810h" on page 1591	00000000h
80814h	4	"reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2)—Offset 80814h" on page 1592	00000000h
80818h	4	"reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3)—Offset 80818h" on page 1594	00000000h
8081Ch	4	"reg_inp_sys_csi_receiver_csi_sh_be_sel_be_type (inp_sys_csi_receiver_csi_sh_be_sel_be)—Offset 8081Ch" on page 1595	00000000h
80820h	4	"reg_inp_sys_csi_receiver_csi_sh_be_raw16_reg_type (inp_sys_csi_receiver_csi_sh_be_raw16_reg)—Offset 80820h" on page 1595	00000000h
80824h	4	"reg_inp_sys_csi_receiver_csi_sh_be_raw18_reg_type (inp_sys_csi_receiver_csi_sh_be_raw18_reg)—Offset 80824h" on page 1596	00000000h
80828h	4	"reg_inp_sys_csi_receiver_csi_sh_be_force_raw8_reg_type (inp_sys_csi_receiver_csi_sh_be_force_raw8_reg)—Offset 80828h" on page 1597	00000000h
8082Ch	4	"reg_inp_sys_csi_receiver_csi_sh_be_irq_stat_reg_type (inp_sys_csi_receiver_csi_sh_be_irq_stat_reg)—Offset 8082Ch" on page 1598	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
80830h	4	"reg_inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg_type (inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg)—Offset 80830h" on page 1598	00000000h
80834h	4	"reg_inp_sys_csi_receiver_csi_sh_be_custom_enable_reg_type (inp_sys_csi_receiver_csi_sh_be_custom_enable_reg)—Offset 80834h" on page 1599	00000000h
81000h	4	"reg_inp_sys_capt_unit_a_reg_CaptStartMode_type (inp_sys_capt_unit_a_reg_CaptStartMode)—Offset 81000h" on page 1600	00000000h
81004h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Start_Addr_type (inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h" on page 1601	00000000h
81008h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size)—Offset 81008h" on page 1601	00000080h
8100Ch	4	"reg_inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions)—Offset 8100Ch" on page 1602	00000003h
81010h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Init_type (inp_sys_capt_unit_a_reg_Capt_Init)—Offset 81010h" on page 1603	00000000h
81014h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Start_Addr_type (inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h" on page 1601	00000000h
81018h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Stop_type (inp_sys_capt_unit_a_reg_Capt_Stop)—Offset 81018h" on page 1604	00000000h
8101Ch	4	"reg_inp_sys_capt_unit_a_reg_Capt_Packet_Length_type (inp_sys_capt_unit_a_reg_Capt_Packet_Length)—Offset 8101Ch" on page 1605	00000000h
81020h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Received_Length_type (inp_sys_capt_unit_a_reg_Capt_Received_Length)—Offset 81020h" on page 1605	00000000h
81024h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets)—Offset 81024h" on page 1606	00000000h
81028h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets)—Offset 81028h" on page 1606	00000000h
8102Ch	4	"reg_inp_sys_capt_unit_a_reg_Capt_Last_Command_type (inp_sys_capt_unit_a_reg_Capt_Last_Command)—Offset 8102Ch" on page 1607	0000000Fh
81030h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Next_Command_type (inp_sys_capt_unit_a_reg_Capt_Next_Command)—Offset 81030h" on page 1608	0000000Fh
81034h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge)—Offset 81034h" on page 1608	0000000Fh
81038h	4	"reg_inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge)—Offset 81038h" on page 1609	0000000Fh
8103Ch	4	"reg_inp_sys_capt_unit_a_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_a_reg_Capt_FSM_State_Info)—Offset 8103Ch" on page 1609	00000000h
82000h	4	"reg_inp_sys_capt_unit_b_reg_CaptStartMode_type (inp_sys_capt_unit_b_reg_CaptStartMode)—Offset 82000h" on page 1610	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
82004h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Start_Addr_type (inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h" on page 1611	00000000h
82008h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size)—Offset 82008h" on page 1612	00000080h
8200Ch	4	"reg_inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions)—Offset 8200Ch" on page 1612	00000003h
82010h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Init_type (inp_sys_capt_unit_b_reg_Capt_Init)—Offset 82010h" on page 1613	00000000h
82014h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Start_Addr_type (inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h" on page 1611	00000000h
82018h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Stop_type (inp_sys_capt_unit_b_reg_Capt_Stop)—Offset 82018h" on page 1614	00000000h
8201Ch	4	"reg_inp_sys_capt_unit_b_reg_Capt_Packet_Length_type (inp_sys_capt_unit_b_reg_Capt_Packet_Length)—Offset 8201Ch" on page 1615	00000000h
82020h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Received_Length_type (inp_sys_capt_unit_b_reg_Capt_Received_Length)—Offset 82020h" on page 1615	00000000h
82024h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets)—Offset 82024h" on page 1616	00000000h
82028h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets)—Offset 82028h" on page 1617	00000000h
8202Ch	4	"reg_inp_sys_capt_unit_b_reg_Capt_Last_Command_type (inp_sys_capt_unit_b_reg_Capt_Last_Command)—Offset 8202Ch" on page 1617	0000000Fh
82030h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Next_Command_type (inp_sys_capt_unit_b_reg_Capt_Next_Command)—Offset 82030h" on page 1618	0000000Fh
82034h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge)—Offset 82034h" on page 1618	0000000Fh
82038h	4	"reg_inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge)—Offset 82038h" on page 1619	0000000Fh
8203Ch	4	"reg_inp_sys_capt_unit_b_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_b_reg_Capt_FSM_State_Info)—Offset 8203Ch" on page 1620	00000000h
83000h	4	"reg_inp_sys_capt_unit_c_reg_CaptStartMode_type (inp_sys_capt_unit_c_reg_CaptStartMode)—Offset 83000h" on page 1621	00000000h
83004h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Start_Addr_type (inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h" on page 1621	00000000h
83008h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size)—Offset 83008h" on page 1622	00000080h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
8300Ch	4	"reg_inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions)—Offset 8300Ch" on page 1623	00000003h
83010h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Init_type (inp_sys_capt_unit_c_reg_Capt_Init)—Offset 83010h" on page 1623	00000000h
83014h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Start_Addr_type (inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h" on page 1621	00000000h
83018h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Stop_type (inp_sys_capt_unit_c_reg_Capt_Stop)—Offset 83018h" on page 1625	00000000h
8301Ch	4	"reg_inp_sys_capt_unit_c_reg_Capt_Packet_Length_type (inp_sys_capt_unit_c_reg_Capt_Packet_Length)—Offset 8301Ch" on page 1625	00000000h
83020h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Received_Length_type (inp_sys_capt_unit_c_reg_Capt_Received_Length)—Offset 83020h" on page 1626	00000000h
83024h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets)—Offset 83024h" on page 1626	00000000h
83028h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets)—Offset 83028h" on page 1627	00000000h
8302Ch	4	"reg_inp_sys_capt_unit_c_reg_Capt_Last_Command_type (inp_sys_capt_unit_c_reg_Capt_Last_Command)—Offset 8302Ch" on page 1628	0000000Fh
83030h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Next_Command_type (inp_sys_capt_unit_c_reg_Capt_Next_Command)—Offset 83030h" on page 1628	0000000Fh
83034h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge)—Offset 83034h" on page 1629	0000000Fh
83038h	4	"reg_inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge)—Offset 83038h" on page 1629	0000000Fh
8303Ch	4	"reg_inp_sys_capt_unit_c_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_c_reg_Capt_FSM_State_Info)—Offset 8303Ch" on page 1630	00000000h
84000h	4	"reg_inp_sys_acq_unit_reg_Acq_Start_Addr_type (inp_sys_acq_unit_reg_Acq_Start_Addr)—Offset 84000h" on page 1631	00000000h
84004h	4	"reg_inp_sys_acq_unit_reg_Acq_Mem_Region_Size_type (inp_sys_acq_unit_reg_Acq_Mem_Region_Size)—Offset 84004h" on page 1632	00000080h
84008h	4	"reg_inp_sys_acq_unit_reg_Acq_Num_Mem_Regions_type (inp_sys_acq_unit_reg_Acq_Num_Mem_Regions)—Offset 84008h" on page 1632	00000003h
8400Ch	4	"reg_inp_sys_acq_unit_reg_Acq_Init_type (inp_sys_acq_unit_reg_Acq_Init)—Offset 8400Ch" on page 1633	00000000h
84010h	4	"reg_inp_sys_acq_unit_reg_Acq_Received_Short_Packets_type (inp_sys_acq_unit_reg_Acq_Received_Short_Packets)—Offset 84010h" on page 1634	00000000h
84014h	4	"reg_inp_sys_acq_unit_reg_Acq_Received_Long_Packets_type (inp_sys_acq_unit_reg_Acq_Received_Long_Packets)—Offset 84014h" on page 1634	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
84018h	4	"reg_inp_sys_acq_unit_reg_Acq_Last_Command_type (inp_sys_acq_unit_reg_Acq_Last_Command)—Offset 84018h" on page 1635	0000000Fh
8401Ch	4	"reg_inp_sys_acq_unit_reg_Acq_Next_Command_type (inp_sys_acq_unit_reg_Acq_Next_Command)—Offset 8401Ch" on page 1635	0000000Fh
84020h	4	"reg_inp_sys_acq_unit_reg_Acq_Last_Acknowledge_type (inp_sys_acq_unit_reg_Acq_Last_Acknowledge)—Offset 84020h" on page 1636	0000000Fh
84024h	4	"reg_inp_sys_acq_unit_reg_Acq_Next_Acknowledge_type (inp_sys_acq_unit_reg_Acq_Next_Acknowledge)—Offset 84024h" on page 1637	0000000Fh
84028h	4	"reg_inp_sys_acq_unit_reg_Acq_FSM_State_Info_type (inp_sys_acq_unit_reg_Acq_FSM_State_Info)—Offset 84028h" on page 1637	00000000h
8402Ch	4	"reg_inp_sys_acq_unit_reg_Acq_Int_Cntr_Info_type (inp_sys_acq_unit_reg_Acq_Int_Cntr_Info)—Offset 8402Ch" on page 1638	00000000h
85000h	4	"reg_inp_sys_dma_DMA_FSM_Command_type (inp_sys_dma_DMA_FSM_Command)—Offset 85000h" on page 1639	00000000h
86000h	4	"reg_inp_sys_dma_DMA_CH0_Packing_setup_type (inp_sys_dma_DMA_CH0_Packing_setup)—Offset 86000h" on page 1640	00000000h
86100h	4	"reg_inp_sys_dma_DMA_CH0_dev_stride_A_type (inp_sys_dma_DMA_CH0_dev_stride_A)—Offset 86100h" on page 1641	00000000h
86200h	4	"reg_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A_type (inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 86200h" on page 1641	00000000h
86300h	4	"reg_inp_sys_dma_DMA_CH0_Device_Xb_A_type (inp_sys_dma_DMA_CH0_Device_Xb_A)—Offset 86300h" on page 1642	00000000h
86400h	4	"reg_inp_sys_dma_DMA_CH0_dev_stride_B_type (inp_sys_dma_DMA_CH0_dev_stride_B)—Offset 86400h" on page 1643	00000000h
86500h	4	"reg_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B_type (inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 86500h" on page 1643	00000000h
86600h	4	"reg_inp_sys_dma_DMA_CH0_Device_Xb_B_type (inp_sys_dma_DMA_CH0_Device_Xb_B)—Offset 86600h" on page 1644	00000000h
86700h	4	"reg_inp_sys_dma_DMA_CH0_Yb_type (inp_sys_dma_DMA_CH0_Yb)—Offset 86700h" on page 1645	00000000h
86800h	4	"reg_inp_sys_dma_DMA_CH0_pending_command_type (inp_sys_dma_DMA_CH0_pending_command)—Offset 86800h" on page 1646	00000000h
87000h	4	"reg_inp_sys_dma_DMA_command_token_type (inp_sys_dma_DMA_command_token)—Offset 87000h" on page 1646	00000000h
87004h	4	"reg_inp_sys_dma_DMA_command_src_addr_type (inp_sys_dma_DMA_command_src_addr)—Offset 87004h" on page 1647	00000000h
87008h	4	"reg_inp_sys_dma_DMA_command_dst_addr_type (inp_sys_dma_DMA_command_dst_addr)—Offset 87008h" on page 1647	00000000h
8700Ch	4	"reg_inp_sys_dma_DMA_command_ctrl_id_type (inp_sys_dma_DMA_command_ctrl_id)—Offset 8700Ch" on page 1648	00000000h
87010h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_status_type (inp_sys_dma_DMA_FSM_Ctrl_status)—Offset 87010h" on page 1649	00000001h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
87014h	4	"reg_inp_sys_dma_DMA_FSM_Pack_status_type (inp_sys_dma_DMA_FSM_Pack_status)—Offset 87014h" on page 1649	00000000h
87018h	4	"reg_inp_sys_dma_DMA_FSM_request_status_type (inp_sys_dma_DMA_FSM_request_status)—Offset 87018h" on page 1650	00000000h
8701Ch	4	"reg_inp_sys_dma_DMA_FSM_write_status_type (inp_sys_dma_DMA_FSM_write_status)—Offset 8701Ch" on page 1651	00000000h
87110h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_dev_idx)—Offset 87110h" on page 1652	00000000h
87114h	4	"reg_inp_sys_dma_DMA_FSM_Pack_cnt_Yb_type (inp_sys_dma_DMA_FSM_Pack_cnt_Yb)—Offset 87114h" on page 1652	00000000h
87118h	4	"reg_inp_sys_dma_DMA_FSM_Request_cnt_Yb_type (inp_sys_dma_DMA_FSM_Request_cnt_Yb)—Offset 87118h" on page 1653	00000000h
8711Ch	4	"reg_inp_sys_dma_DMA_FSM_Write_cnt_Y_type (inp_sys_dma_DMA_FSM_Write_cnt_Y)—Offset 8711Ch" on page 1654	00000000h
87210h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_req_addr_type (inp_sys_dma_DMA_FSM_Ctrl_req_addr)—Offset 87210h" on page 1654	00000000h
87214h	4	"reg_inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb_type (inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 87214h" on page 1655	00000000h
87218h	4	"reg_inp_sys_dma_DMA_FSM_Request_cnt_Xb_type (inp_sys_dma_DMA_FSM_Request_cnt_Xb)—Offset 87218h" on page 1656	00000000h
8721Ch	4	"reg_inp_sys_dma_DMA_FSM_Write_cnt_Xb_type (inp_sys_dma_DMA_FSM_Write_cnt_Xb)—Offset 8721Ch" on page 1656	00000000h
87310h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_req_stride_type (inp_sys_dma_DMA_FSM_Ctrl_req_stride)—Offset 87310h" on page 1657	00000000h
87314h	4	"reg_inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb_type (inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 87314h" on page 1658	00000000h
87318h	4	"reg_inp_sys_dma_DMA_FSM_Req_remining_Xb_type (inp_sys_dma_DMA_FSM_Req_remining_Xb)—Offset 87318h" on page 1658	00000000h
8731Ch	4	"reg_inp_sys_dma_DMA_FSM_Wr_remining_Xb_type (inp_sys_dma_DMA_FSM_Wr_remining_Xb)—Offset 8731Ch" on page 1659	00000000h
87410h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_req_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_req_Xb)—Offset 87410h" on page 1660	00000000h
87418h	4	"reg_inp_sys_dma_DMA_FSM_Req_burst_cnt_type (inp_sys_dma_DMA_FSM_Req_burst_cnt)—Offset 87418h" on page 1660	0000FFFFh
8741Ch	4	"reg_inp_sys_dma_DMA_FSM_Wr_burst_cnt_type (inp_sys_dma_DMA_FSM_Wr_burst_cnt)—Offset 8741Ch" on page 1661	0000FFFFh
87510h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_req_Yb_type (inp_sys_dma_DMA_FSM_Ctrl_req_Yb)—Offset 87510h" on page 1662	00000000h
87610h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 87610h" on page 1662	00000000h
87710h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 87710h" on page 1663	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
87810h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_Wr_addr_type (inp_sys_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 87810h" on page 1664	00000000h
87910h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_Wr_stride_type (inp_sys_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 87910h" on page 1664	00000000h
87A10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 87A10h" on page 1665	00000000h
87B10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_Yb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 87B10h" on page 1666	00000000h
87C10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 87C10h" on page 1666	00000000h
87D10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem_type (inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 87D10h" on page 1667	00000000h
87E10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem_type (inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 87E10h" on page 1668	00000000h
87F10h	4	"reg_inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id_type (inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 87F10h" on page 1668	00000000h
88000h	4	"reg_inp_sys_dma_Dev_Interf_0_req_side_type (inp_sys_dma_Dev_Interf_0_req_side)—Offset 88000h" on page 1669	00000000h
88004h	4	"reg_inp_sys_dma_Dev_Interf_1_req_side_type (inp_sys_dma_Dev_Interf_1_req_side)—Offset 88004h" on page 1670	00000006h
88100h	4	"reg_inp_sys_dma_Dev_Interf_0_snd_side_type (inp_sys_dma_Dev_Interf_0_snd_side)—Offset 88100h" on page 1671	00000004h
88104h	4	"reg_inp_sys_dma_Dev_Interf_1_snd_side_type (inp_sys_dma_Dev_Interf_1_snd_side)—Offset 88104h" on page 1672	00000006h
88200h	4	"reg_inp_sys_dma_Dev_Interf_0_Fifo_status_type (inp_sys_dma_Dev_Interf_0_Fifo_status)—Offset 88200h" on page 1673	00000004h
88204h	4	"reg_inp_sys_dma_Dev_Interf_1_Fifo_status_type (inp_sys_dma_Dev_Interf_1_Fifo_status)—Offset 88204h" on page 1674	00000004h
88300h	4	"reg_inp_sys_dma_Dev_Interf_0_Req_complete_bust_type (inp_sys_dma_Dev_Interf_0_Req_complete_bust)—Offset 88300h" on page 1675	00000000h
88304h	4	"reg_inp_sys_dma_Dev_Interf_1_Req_complete_bust_type (inp_sys_dma_Dev_Interf_1_Req_complete_bust)—Offset 88304h" on page 1676	00000000h
88400h	4	"reg_inp_sys_dma_Dev_Interf_1_Max_burst_Size_type (inp_sys_dma_Dev_Interf_1_Max_burst_Size)—Offset 88400h" on page 1677	0000007Fh
89000h	4	"reg_inp_sys_inp_ctrl_inpsys_captA_start_addr_type (inp_sys_inp_ctrl_inpsys_captA_start_addr)—Offset 89000h" on page 1677	00000000h
89004h	4	"reg_inp_sys_inp_ctrl_inpsys_captB_start_addr_type (inp_sys_inp_ctrl_inpsys_captB_start_addr)—Offset 89004h" on page 1678	00000000h
89008h	4	"reg_inp_sys_inp_ctrl_inpsys_captC_start_addr_type (inp_sys_inp_ctrl_inpsys_captC_start_addr)—Offset 89008h" on page 1679	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
8900Ch	4	"reg_inp_sys_inp_ctrl_inpsys_captA_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captA_mem_region_size)—Offset 8900Ch" on page 1679	00000080h
89010h	4	"reg_inp_sys_inp_ctrl_inpsys_captB_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captB_mem_region_size)—Offset 89010h" on page 1680	00000080h
89014h	4	"reg_inp_sys_inp_ctrl_inpsys_captC_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captC_mem_region_size)—Offset 89014h" on page 1681	00000080h
89018h	4	"reg_inp_sys_inp_ctrl_inpsys_captA_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captA_num_mem_regions)—Offset 89018h" on page 1681	00000003h
8901Ch	4	"reg_inp_sys_inp_ctrl_inpsys_captB_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captB_num_mem_regions)—Offset 8901Ch" on page 1682	00000003h
89020h	4	"reg_inp_sys_inp_ctrl_inpsys_captC_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captC_num_mem_regions)—Offset 89020h" on page 1683	00000003h
89024h	4	"reg_inp_sys_inp_ctrl_inpsys_acq_start_addr_type (inp_sys_inp_ctrl_inpsys_acq_start_addr)—Offset 89024h" on page 1684	00000000h
89028h	4	"reg_inp_sys_inp_ctrl_inpsys_acq_mem_region_size_type (inp_sys_inp_ctrl_inpsys_acq_mem_region_size)—Offset 89028h" on page 1684	00000080h
8902Ch	4	"reg_inp_sys_inp_ctrl_inpsys_acq_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_acq_num_mem_regions)—Offset 8902Ch" on page 1685	00000003h
89030h	4	"reg_inp_sys_inp_ctrl_inpsys_ctrl_init_type (inp_sys_inp_ctrl_inpsys_ctrl_init)—Offset 89030h" on page 1686	00000000h
89034h	4	"reg_inp_sys_inp_ctrl_inpsys_last_cmd_type (inp_sys_inp_ctrl_inpsys_last_cmd)—Offset 89034h" on page 1686	0000000Fh
89038h	4	"reg_inp_sys_inp_ctrl_inpsys_next_cmd_type (inp_sys_inp_ctrl_inpsys_next_cmd)—Offset 89038h" on page 1687	0000000Fh
8903Ch	4	"reg_inp_sys_inp_ctrl_inpsys_last_ack_type (inp_sys_inp_ctrl_inpsys_last_ack)—Offset 8903Ch" on page 1687	0000000Fh
89040h	4	"reg_inp_sys_inp_ctrl_inpsys_next_ack_type (inp_sys_inp_ctrl_inpsys_next_ack)—Offset 89040h" on page 1688	0000000Fh
89044h	4	"reg_inp_sys_inp_ctrl_inpsys_top_fsm_state_type (inp_sys_inp_ctrl_inpsys_top_fsm_state)—Offset 89044h" on page 1688	00000000h
89048h	4	"reg_inp_sys_inp_ctrl_inpsys_captA_fsm_state_type (inp_sys_inp_ctrl_inpsys_captA_fsm_state)—Offset 89048h" on page 1689	00000000h
8904Ch	4	"reg_inp_sys_inp_ctrl_inpsys_captB_fsm_state_type (inp_sys_inp_ctrl_inpsys_captB_fsm_state)—Offset 8904Ch" on page 1690	00000000h
89050h	4	"reg_inp_sys_inp_ctrl_inpsys_captC_fsm_state_type (inp_sys_inp_ctrl_inpsys_captC_fsm_state)—Offset 89050h" on page 1690	00000000h
89054h	4	"reg_inp_sys_inp_ctrl_inpsys_acq_fsm_state_type (inp_sys_inp_ctrl_inpsys_acq_fsm_state)—Offset 89054h" on page 1691	00000000h
89058h	4	"reg_inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region_type (inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region)—Offset 89058h" on page 1692	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
8A000h	4	"reg_inp_sys_gpreg_str_multicastA_sel_type (inp_sys_gpreg_str_multicastA_sel)—Offset 8A000h" on page 1693	00000000h
8A004h	4	"reg_inp_sys_gpreg_str_multicastB_sel_type (inp_sys_gpreg_str_multicastB_sel)—Offset 8A004h" on page 1694	00000000h
8A008h	4	"reg_inp_sys_gpreg_str_multicastC_sel_type (inp_sys_gpreg_str_multicastC_sel)—Offset 8A008h" on page 1694	00000000h
8A00Ch	4	"reg_inp_sys_gpreg_str_mux_sel_type (inp_sys_gpreg_str_mux_sel)—Offset 8A00Ch" on page 1695	00000000h
8A010h	4	"reg_inp_sys_gpreg_str_mon_status_type (inp_sys_gpreg_str_mon_status)—Offset 8A010h" on page 1695	00000000h
8A014h	4	"reg_inp_sys_gpreg_str_mon_irq_cond_type (inp_sys_gpreg_str_mon_irq_cond)—Offset 8A014h" on page 1697	00000000h
8A018h	4	"reg_inp_sys_gpreg_str_mon_irq_en_type (inp_sys_gpreg_str_mon_irq_en)—Offset 8A018h" on page 1698	00000000h
8A01Ch	4	"reg_inp_sys_gpreg_isys_srst_type (inp_sys_gpreg_isys_srst)—Offset 8A01Ch" on page 1699	00000000h
8A020h	4	"reg_inp_sys_gpreg_isys_slv_reg_srst_type (inp_sys_gpreg_isys_slv_reg_srst)—Offset 8A020h" on page 1700	00000000h
8A024h	4	"reg_inp_sys_gpreg_str_deint_portA_cnt_type (inp_sys_gpreg_str_deint_portA_cnt)—Offset 8A024h" on page 1701	00000000h
8A028h	4	"reg_inp_sys_gpreg_str_deint_portB_cnt_type (inp_sys_gpreg_str_deint_portB_cnt)—Offset 8A028h" on page 1702	00000000h
8B008h	4	"reg_inp_sys_fifo_adapter_CSI_generic_short_packet_available_type (inp_sys_fifo_adapter_CSI_generic_short_packet_available)—Offset 8B008h" on page 1702	00000001h
8C000h	4	"reg_inp_sys_irq_ctrl_irq_edge_type (inp_sys_irq_ctrl_irq_edge)—Offset 8C000h" on page 1703	00000000h
8C004h	4	"reg_inp_sys_irq_ctrl_irq_mask_type (inp_sys_irq_ctrl_irq_mask)—Offset 8C004h" on page 1704	00000000h
8C008h	4	"reg_inp_sys_irq_ctrl_irq_status_type (inp_sys_irq_ctrl_irq_status)—Offset 8C008h" on page 1705	00000000h
8C00Ch	4	"reg_inp_sys_irq_ctrl_irq_clear_type (inp_sys_irq_ctrl_irq_clear)—Offset 8C00Ch" on page 1706	00000000h
8C010h	4	"reg_inp_sys_irq_ctrl_irq_en_type (inp_sys_irq_ctrl_irq_en)—Offset 8C010h" on page 1708	00000000h
8C014h	4	"reg_inp_sys_irq_ctrl_irq_level_not_pulse_type (inp_sys_irq_ctrl_irq_level_not_pulse)—Offset 8C014h" on page 1709	00000000h
90000h	4	"reg_isel_gpr_reg_gp_syncgen_enable_type (isel_gpr_reg_gp_syncgen_enable)—Offset 90000h" on page 1710	00000000h
90004h	4	"reg_isel_gpr_reg_gp_syncgen_free_running_type (isel_gpr_reg_gp_syncgen_free_running)—Offset 90004h" on page 1710	00000000h
90008h	4	"reg_isel_gpr_reg_gp_syncgen_pause_type (isel_gpr_reg_gp_syncgen_pause)—Offset 90008h" on page 1711	00000000h
9000Ch	4	"reg_isel_gpr_reg_gp_nr_frames_type (isel_gpr_reg_gp_nr_frames)—Offset 9000Ch" on page 1712	00000000h
90010h	4	"reg_isel_gpr_reg_gp_syngen_nr_pix_type (isel_gpr_reg_gp_syngen_nr_pix)—Offset 90010h" on page 1712	00000000h
90014h	4	"reg_isel_gpr_reg_gp_syngen_nr_lines_type (isel_gpr_reg_gp_syngen_nr_lines)—Offset 90014h" on page 1713	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
90018h	4	"reg_isel_gpr_reg_gp_syngen_hblank_cycles_type (isel_gpr_reg_gp_syngen_hblank_cycles)—Offset 90018h" on page 1714	00000000h
9001Ch	4	"reg_isel_gpr_reg_gp_syngen_vblank_cycles_type (isel_gpr_reg_gp_syngen_vblank_cycles)—Offset 9001Ch" on page 1714	00000000h
90020h	4	"reg_isel_gpr_reg_gp_isel_sof_type (isel_gpr_reg_gp_isel_sof)—Offset 90020h" on page 1715	00000000h
90024h	4	"reg_isel_gpr_reg_gp_isel_eof_type (isel_gpr_reg_gp_isel_eof)—Offset 90024h" on page 1716	00000000h
90028h	4	"reg_isel_gpr_reg_gp_isel_sol_type (isel_gpr_reg_gp_isel_sol)—Offset 90028h" on page 1716	00000000h
9002Ch	4	"reg_isel_gpr_reg_gp_isel_eol_type (isel_gpr_reg_gp_isel_eol)—Offset 9002Ch" on page 1717	00000000h
90030h	4	"reg_isel_gpr_reg_gp_isel_lfsr_enable_type (isel_gpr_reg_gp_isel_lfsr_enable)—Offset 90030h" on page 1717	00000000h
90034h	4	"reg_isel_gpr_reg_gp_isel_lfsr_enable_b_type (isel_gpr_reg_gp_isel_lfsr_enable_b)—Offset 90034h" on page 1718	00000000h
90038h	4	"reg_isel_gpr_reg_gp_isel_lfsr_reset_value_type (isel_gpr_reg_gp_isel_lfsr_reset_value)—Offset 90038h" on page 1719	00000000h
9003Ch	4	"reg_isel_gpr_reg_gp_isel_tpg_enable_type (isel_gpr_reg_gp_isel_tpg_enable)—Offset 9003Ch" on page 1719	00000000h
90040h	4	"reg_isel_gpr_reg_gp_isel_tpg_enable_b_type (isel_gpr_reg_gp_isel_tpg_enable_b)—Offset 90040h" on page 1720	00000000h
90044h	4	"reg_isel_gpr_reg_gp_isel_hor_cnt_mask_type (isel_gpr_reg_gp_isel_hor_cnt_mask)—Offset 90044h" on page 1721	00000000h
90048h	4	"reg_isel_gpr_reg_gp_isel_ver_cnt_mask_type (isel_gpr_reg_gp_isel_ver_cnt_mask)—Offset 90048h" on page 1721	00000000h
9004Ch	4	"reg_isel_gpr_reg_gp_isel_xy_cnt_mask_type (isel_gpr_reg_gp_isel_xy_cnt_mask)—Offset 9004Ch" on page 1722	00000000h
90050h	4	"reg_isel_gpr_reg_gp_isel_hor_cnt_delta_type (isel_gpr_reg_gp_isel_hor_cnt_delta)—Offset 90050h" on page 1723	00000000h
90054h	4	"reg_isel_gpr_reg_gp_isel_ver_cnt_delta_type (isel_gpr_reg_gp_isel_ver_cnt_delta)—Offset 90054h" on page 1723	00000000h
90058h	4	"reg_isel_gpr_reg_gp_isel_tpg_mode_type (isel_gpr_reg_gp_isel_tpg_mode)—Offset 90058h" on page 1724	00000000h
9005Ch	4	"reg_isel_gpr_reg_gp_isel_tpg_red1_type (isel_gpr_reg_gp_isel_tpg_red1)—Offset 9005Ch" on page 1725	00000000h
90060h	4	"reg_isel_gpr_reg_gp_isel_tpg_green1_type (isel_gpr_reg_gp_isel_tpg_green1)—Offset 90060h" on page 1725	00000000h
90064h	4	"reg_isel_gpr_reg_gp_isel_tpg_blue1_type (isel_gpr_reg_gp_isel_tpg_blue1)—Offset 90064h" on page 1726	00000000h
90068h	4	"reg_isel_gpr_reg_gp_isel_tpg_red2_type (isel_gpr_reg_gp_isel_tpg_red2)—Offset 90068h" on page 1727	00000000h
9006Ch	4	"reg_isel_gpr_reg_gp_isel_tpg_green2_type (isel_gpr_reg_gp_isel_tpg_green2)—Offset 9006Ch" on page 1727	00000000h
90070h	4	"reg_isel_gpr_reg_gp_isel_tpg_blue2_type (isel_gpr_reg_gp_isel_tpg_blue2)—Offset 90070h" on page 1728	00000000h
90074h	4	"reg_isel_gpr_reg_gp_isel_ch_id_type (isel_gpr_reg_gp_isel_ch_id)—Offset 90074h" on page 1729	00000000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
90078h	4	"reg_isel_gpr_reg_gp_isel_fmt_type_type (isel_gpr_reg_gp_isel_fmt_type)—Offset 90078h" on page 1729	00000000h
9007Ch	4	"reg_isel_gpr_reg_gp_isel_data_sel_type (isel_gpr_reg_gp_isel_data_sel)—Offset 9007Ch" on page 1730	00000000h
90080h	4	"reg_isel_gpr_reg_gp_isel_sband_sel_type (isel_gpr_reg_gp_isel_sband_sel)—Offset 90080h" on page 1730	00000000h
90084h	4	"reg_isel_gpr_reg_gp_isel_sync_sel_type (isel_gpr_reg_gp_isel_sync_sel)—Offset 90084h" on page 1731	00000000h
90088h	4	"reg_isel_gpr_reg_gp_syncgen_hor_cnt_type (isel_gpr_reg_gp_syncgen_hor_cnt)—Offset 90088h" on page 1732	00000000h
9008Ch	4	"reg_isel_gpr_reg_gp_syncgen_ver_cnt_type (isel_gpr_reg_gp_syncgen_ver_cnt)—Offset 9008Ch" on page 1732	00000000h
90090h	4	"reg_isel_gpr_reg_gp_syncgen_frame_cnt_type (isel_gpr_reg_gp_syncgen_frame_cnt)—Offset 90090h" on page 1733	00000000h
90094h	4	"reg_isel_gpr_reg_gp_soft_reset_type (isel_gpr_reg_gp_soft_reset)—Offset 90094h" on page 1734	00000000h
90100h	4	"reg_isel_fa_send_to_GP_FIFO_type (isel_fa_send_to_GP_FIFO)—Offset 90100h" on page 1734	00000000h
90108h	4	"reg_isel_fa_check_send_to_GP_FIFO_type (isel_fa_check_send_to_GP_FIFO)—Offset 90108h" on page 1735	00000001h
90200h	4	"reg_isel_irq_ctrl_reg_irq_edge_type (isel_irq_ctrl_reg_irq_edge)—Offset 90200h" on page 1736	00000000h
90204h	4	"reg_isel_irq_ctrl_reg_irq_mask_type (isel_irq_ctrl_reg_irq_mask)—Offset 90204h" on page 1736	00000000h
90208h	4	"reg_isel_irq_ctrl_reg_irq_status_type (isel_irq_ctrl_reg_irq_status)—Offset 90208h" on page 1737	00000000h
9020Ch	4	"reg_isel_irq_ctrl_reg_irq_clear_type (isel_irq_ctrl_reg_irq_clear)—Offset 9020Ch" on page 1737	00000000h
90210h	4	"reg_isel_irq_ctrl_reg_irq_enable_type (isel_irq_ctrl_reg_irq_enable)—Offset 90210h" on page 1738	00000000h
90214h	4	"reg_isel_irq_ctrl_reg_irq_level_not_pulse_type (isel_irq_ctrl_reg_irq_level_not_pulse)—Offset 90214h" on page 1739	00000000h
A0000h	4	"reg_icache_out_sys_c_mmu_MMU_invalidate_cache_type (icache_out_sys_c_mmu_MMU_invalidate_cache)—Offset A0000h" on page 1739	00000000h
A0004h	4	"reg_icache_out_sys_c_mmu_MMU_page_table_base_type (icache_out_sys_c_mmu_MMU_page_table_base)—Offset A0004h" on page 1740	00000000h
B0000h	8	"mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first)—Offset B0000h" on page 1741	0000000000000000h
B7FF8h	8	"mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last)—Offset B7FF8h" on page 1741	0000000000000000h
1C0000h	2	"mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1C0000h" on page 1742	0000h
1C0FFEh	2	"mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1C0FFEh" on page 1742	0000h

Table 180. Summary of Image Signal Processor Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size	Register ID—Description	Default Value
1D0000h	2	"mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1D0000h" on page 1743	0000h
1D0FFEh	2	"mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1D0FFEh" on page 1743	0000h
1E0000h	2	"mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1E0000h" on page 1744	0000h
1E0FFEh	2	"mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1E0FFEh" on page 1744	0000h
1F0000h	4	"mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first)—Offset 1F0000h" on page 1745	00000000h
1F0FFCh	4	"mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last)—Offset 1F0FFCh" on page 1745	00000000h
200000h	4	"mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_first_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_first)—Offset 200000h" on page 1746	00000000h
203FFCh	4	"mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_last_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_last)—Offset 203FFCh" on page 1746	00000000h
300000h	4	"mem_scp_dmem_mem_sl_ip_dmem_mem_first_type (scp_dmem_mem_sl_ip_dmem_mem_first)—Offset 300000h" on page 1747	00000000h
307FFCh	4	"mem_scp_dmem_mem_sl_ip_dmem_mem_last_type (scp_dmem_mem_sl_ip_dmem_mem_last)—Offset 307FFCh" on page 1747	00000000h
380008h	4	"reg_fa_sp_isp_send_to_SP_type (fa_sp_isp_send_to_SP)—Offset 380008h" on page 1748	00000000h
38000Ch	4	"reg_fa_sp_isp_send_to_ISP_type (fa_sp_isp_send_to_ISP)—Offset 38000Ch" on page 1748	00000000h
380010h	4	"reg_fa_sp_isp_check_receive_from_SP_type (fa_sp_isp_check_receive_from_SP)—Offset 380010h" on page 1749	00000001h
380014h	4	"reg_fa_sp_isp_check_receive_from_ISP_type (fa_sp_isp_check_receive_from_ISP)—Offset 380014h" on page 1749	00000001h
380018h	4	"reg_fa_sp_isp_check_send_to_SP_type (fa_sp_isp_check_send_to_SP)—Offset 380018h" on page 1750	00000000h
38001Ch	4	"reg_fa_sp_isp_check_send_to_ISP_type (fa_sp_isp_check_send_to_ISP)—Offset 38001Ch" on page 1751	00000000h

15.8.1 reg_gpd_gp_reg_reg_gp_sdram_wakeup_type (gpd_gp_reg_reg_gp_sdram_wakeup)—Offset 0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_sdram_wakeup: [ISPMMADR] + 0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gp_sdram_wakeup (bits 31:1), reg_gp_sdram_wakeup (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_sdram_wakeup:** Unused
0	0h RW	**reg_gp_sdram_wakeup:** when set to 1, this signal will cause the memory controller to bring the external SDRAM into an active state.

15.8.2 reg_gpd_gp_reg_reg_gp_idle_type (gpd_gp_reg_reg_gp_idle)—Offset 4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_idle: [ISPMMADR] + 4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gp_idle (bits 31:1), reg_gp_idle (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_idle:** Unused

Bit Range	Default & Access	Description
0	0h RW	**reg_gp_idle:** Should be set to 1 when ISP system is in ?idle? mode.

15.8.3 reg_gpd_gp_reg_reg_gp_irq_req0_type (gpd_gp_reg_reg_gp_irq_req0)—Offset 8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_irq_req0: [ISPMMADR] + 8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_gp_irq_req0																															reg_gp_irq_req0

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_irq_req0:** Unused
0	0h RW	**reg_gp_irq_req0:** possibly causes an interrupt request (if the host interrupt controller is properly configured)

15.8.4 reg_gpd_gp_reg_reg_gp_irq_req1_type (gpd_gp_reg_reg_gp_irq_req1)—Offset Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_irq_req1: [ISPMMADR] + Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bit	31:1	0
Default	0000 0000 0000 0000 0000 0000 0000 000	0
Field	unused_reg_gp_irq_req1	reg_gp_irq_req1

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_irq_req1:** Unused
0	0h RW	**reg_gp_irq_req1:** possibly causes an interrupt request (if the host interrupt controller is properly configured)

15.8.5 reg_gpd_gp_reg_reg_gp_sp_stream_stat_type (gpd_gp_reg_reg_gp_sp_stream_stat)—Offset 10h

Indicate the status of the streaming ports of the scalar processor. All valid and accept signals of the scalar processor are reflected in this register and in reg_gp_sp_stream_stat_b.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat: [ISPMMADR] + 10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00022022h

Bit	Default	Field
31	0	SP_STR_MON_PIFB2SP_accept
30	0	SP_STR_MON_PIFB2SP_valid
29	0	SP_STR_MON_SP2PIFB_accept
28	0	SP_STR_MON_SP2PIFB_valid
27	0	SP_STR_MON_PIF2SP_accept
26	0	SP_STR_MON_PIF2SP_valid
25	0	SP_STR_MON_SP2PIF_accept
24	0	SP_STR_MON_SP2PIF_valid
23	0	SP_STR_MON_ISYS2SP_accept
22	0	SP_STR_MON_ISYS2SP_valid
21	0	SP_STR_MON_SP2ISYS_accept
20	0	SP_STR_MON_SP2ISYS_valid
19	0	SP_STR_MON_GPD2SP_accept
18	0	SP_STR_MON_GPD2SP_valid
17	1	SP_STR_MON_SP2GPD_accept
16	0	SP_STR_MON_SP2GPD_valid
15	0	SP_STR_MON_ISP2SP_accept
14	0	SP_STR_MON_ISP2SP_valid
13	1	SP_STR_MON_SP2ISP_accept
12	0	SP_STR_MON_SP2ISP_valid
11	0	SP_STR_MON_DMA2SP_accept
10	0	SP_STR_MON_DMA2SP_valid
9	0	SP_STR_MON_SP2DMA_accept
8	0	SP_STR_MON_SP2DMA_valid
7	0	SP_STR_MON_MC2SP_accept
6	0	SP_STR_MON_MC2SP_valid
5	1	SP_STR_MON_SP2MC_accept
4	0	SP_STR_MON_SP2MC_valid
3	0	SP_STR_MON_SIF2SP_accept
2	0	SP_STR_MON_SIF2SP_valid
1	1	SP_STR_MON_SP2SIF_accept
0	0	SP_STR_MON_SP2SIF_valid

Bit Range	Default & Access	Description
31	0h RO	**SP_STR_MON_PIFB2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the primary input formatter B acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.

Bit Range	Default & Access	Description
30	0h RO	**SP_STR_MON_PIFB2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter B acknowledge port and the SP, is present on the primary input formatter B input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
29	0h RO	**SP_STR_MON_SP2PIFB_accept:** Returns the value 1 if the command FIFO between SP and the Primary input formatter B can accept a command from the SP. Returns the value 0 if this FIFO cannot accept a token from the SP.
28	0h RO	**SP_STR_MON_SP2PIFB_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Primary Input Formatter B command FIFO. Returns the value 0 if the SP does not send a command to this FIFO
27	0h RO	**SP_STR_MON_PIF2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the primary input formatter acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
26	0h RO	**SP_STR_MON_PIF2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter acknowledge port and the SP, is present on the primary input formatter input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
25	0h RO	**SP_STR_MON_SP2PIF_accept:** Returns the value 1 if the command FIFO between SP and the Primary input formatter can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
24	0h RO	**SP_STR_MON_SP2PIF_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Primary Input Formatter command FIFO. Returns the value 0 if the SP does not send a command to the Primary Input formatter
23	0h RO	**SP_STR_MON_ISYS2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the input system acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
22	0h RO	**SP_STR_MON_ISYS2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the input system acknowledge port and the SP, is present on the input system input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
21	0h RO	**SP_STR_MON_SP2ISYS_accept:** Returns the value 1 if the command FIFO between SP and the input system can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
20	0h RO	**SP_STR_MON_SP2ISYS_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the input system command FIFO. Returns the value 0 if the SP does not send a command to the input system
19	0h RO	**SP_STR_MON_GPD2SP_accept:** Returns the value 1 if the SP can accept a token from the streaming FIFO between the fifo adpater in GP devices and the SP. Returns 0 if the SP cannot accept a token from this FIFO.
18	0h RO	**SP_STR_MON_GPD2SP_valid:** Returns the value 1 if the streaming FIFO between the fifo adapter in GP devices and the SP has a valid token for the SP. Returns the value 0 if this FIFO is empty.
17	1h RO	**SP_STR_MON_SP2GPD_accept:** Returns the value 1 if the token FIFO between SP and fifo adapter can accept a token from the SP. Returns the value 0 if this token FIFO is full.
16	0h RO	**SP_STR_MON_SP2GPD_valid:** Returns the value 1 if SP sends a token using the streaming port connected to the token FIFO between the SP and the fifo adapter in GP_devices. Returns the value 0 if the SP does not send a token to the fifo adapter.
15	0h RO	**SP_STR_MON_ISP2SP_accept:** Returns the value 1 if the SP can accept a token from the streaming FIFO between the ISP and the SP. Returns 0 if the SP cannot accept a token from this FIFO.
14	0h RO	**SP_STR_MON_ISP2SP_valid:** Returns the value 1 if the streaming FIFO between the ISP and the SP has a valid token for the SP. Returns the value 0 if this FIFO is empty
13	1h RO	**SP_STR_MON_SP2ISP_accept:** Returns the value 1 if the token FIFO between SP and ISP can accept a token from the SP. Returns the value 0 if this token FIFO is full.

Bit Range	Default & Access	Description
12	0h RO	**SP_STR_MON_SP2ISP_valid:** Returns the value 1 if SP sends a token using the streaming port connected to the ISP token FIFO. Returns the value 0 if the SP does not send a token to the ISP
11	0h RO	**SP_STR_MON_DMA2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the DMA acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
10	0h RO	**SP_STR_MON_DMA2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the DMA acknowledge port and the SP, is present on the DMA input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
9	0h RO	**SP_STR_MON_SP2DMA_accept:** Returns the value 1 if the command FIFO between SP and the DMA can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
8	0h RO	**SP_STR_MON_SP2DMA_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the DMA command FIFO. Returns the value 0 if the SP does not send a command to the DMA
7	0h RO	**SP_STR_MON_MC2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the stream2mem acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
6	0h RO	**SP_STR_MON_MC2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the stream2mem acknowledge port and the SP, is present on the stream2mem input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
5	1h RO	**SP_STR_MON_SP2MC_accept:** Returns the value 1 if the command FIFO between SP and the stream2mem can accept a command from the SP. Returns the value 0 if this command FIFO is full.
4	0h RO	**SP_STR_MON_SP2MC_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the stream2mem command FIFO. Returns the value 0 if the SP does not send a command to the stream2mem
3	0h RO	**SP_STR_MON_SIF2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the secondary input formatter acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
2	0h RO	**SP_STR_MON_SIF2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the secondary input formatter acknowledge port and the SP, is present on the secondary input formatter input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
1	1h RO	**SP_STR_MON_SP2SIF_accept:** Returns the value 1 if the command FIFO between SP and the secondary input formatter can accept a command from the SP. Returns the value 0 if this command FIFO is full.
0	0h RO	**SP_STR_MON_SP2SIF_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Secondary Input Formatter command FIFO. Returns the value 0 if the SP does not send a command to the Secondary Input formatter

15.8.6 reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_type (gpd_gp_reg_reg_gp_sp_stream_stat_b)—Offset 14h

Indicate the status of the streaming ports of the scalar processor. All valid and accept signals of the scalar processor are reflected in this register and in reg_gp_sp_stream_stat.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_b: [ISPMMADR] + 14h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:8	unused_reg_gp_sp_stream_stat_b
7	SP_STR_MON_GDC22SP_accept
6	SP_STR_MON_GDC22SP_valid
5	SP_STR_MON_SP2GDC2_accept
4	SP_STR_MON_SP2GDC2_valid
3	SP_STR_MON_GDC12SP_accept
2	SP_STR_MON_GDC12SP_valid
1	SP_STR_MON_SP2GDC1_accept
0	SP_STR_MON_SP2GDC1_valid

Bit Range	Default & Access	Description
31:8	0h RW	**unused_reg_gp_sp_stream_stat_b:** Unused
7	0h RO	**SP_STR_MON_GDC22SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the GDC2 acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
6	0h RO	**SP_STR_MON_GDC22SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC2 acknowledge port and the SP, is present on the GDC2 input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
5	0h RO	**SP_STR_MON_SP2GDC2_accept:** Returns the value 1 if the command FIFO between SP and GDC2 can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
4	0h RO	**SP_STR_MON_SP2GDC2_valid:** Returns the value 1 if SP sends a command using the streaming port connected to GDC2 command FIFO. Returns the value 0 if the SP does not send a command to GDC2
3	0h RO	**SP_STR_MON_GDC12SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the GDC1 acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
2	0h RO	**SP_STR_MON_GDC12SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC1 acknowledge port and the SP, is present on the GDC1 input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
1	0h RO	**SP_STR_MON_SP2GDC1_accept:** Returns the value 1 if the command FIFO between SP and GDC1 can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
0	0h RO	**SP_STR_MON_SP2GDC1_valid:** Returns the value 1 if SP sends a command using the streaming port connected to GDC1 command FIFO. Returns the value 0 if the SP does not send a command to GDC1

15.8.7 reg_gpd_gp_reg_reg_gp_isp_stream_stat_type (gpd_gp_reg_reg_gp_isp_stream_stat)—Offset 18h

Indicate the status of the streaming ports of the vector processor. All valid and accept signals of the vector processor are reflected in this register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_isp_stream_stat: [ISPMMADR] + 18h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 02200000h

Bits	Default	Field
31:28	0 0 0 0	unused_reg_gp_isp_stream_stat
27	0	ISP_STR_MON_SP2ISP_accept
26	0	ISP_STR_MON_SP2ISP_valid
25	1	ISP_STR_MON_ISP2SP_accept
24	0	ISP_STR_MON_ISP2SP_valid
23	0	ISP_STR_MON_GPD2ISP_accept
22	0	ISP_STR_MON_GPD2ISP_valid
21	1	ISP_STR_MON_ISP2GPD_accept
20	0	ISP_STR_MON_ISP2GPD_valid
19	0	ISP_STR_MON_GDC22ISP_accept
18	0	ISP_STR_MON_GDC22ISP_valid
17	0	ISP_STR_MON_ISP2GDC2_accept
16	0	ISP_STR_MON_ISP2GDC2_valid
15	0	ISP_STR_MON_GDC12ISP_accept
14	0	ISP_STR_MON_GDC12ISP_valid
13	0	ISP_STR_MON_ISP2GDC1_accept
12	0	ISP_STR_MON_ISP2GDC1_valid
11	0	ISP_STR_MON_DMA2ISP_accept
10	0	ISP_STR_MON_DMA2ISP_valid
9	0	ISP_STR_MON_ISP2DMA_accept
8	0	ISP_STR_MON_ISP2DMA_valid
7	0	ISP_STR_MON_PIFB2ISP_accept
6	0	ISP_STR_MON_PIFB2ISP_valid
5	0	ISP_STR_MON_ISP2PIFB_accept
4	0	ISP_STR_MON_ISP2PIFB_valid
3	0	ISP_STR_MON_PIF2ISP_accept
2	0	ISP_STR_MON_PIF2ISP_valid
1	0	ISP_STR_MON_ISP2PIF_accept
0	0	ISP_STR_MON_ISP2PIF_valid

Bit Range	Default & Access	Description
31:28	0h RW	**unused_reg_gp_isp_stream_stat:** Unused
27	0h RO	**ISP_STR_MON_SP2ISP_accept:** Returns the value 1 if the ISP can accept a token from the streaming FIFO between the SP and the ISP. Returns 0 if the ISP cannot accept a token from this FIFO.
26	0h RO	**ISP_STR_MON_SP2ISP_valid:** Returns the value 1 if the streaming FIFO between the SP and the ISP has a valid token for the ISP. Returns the value 0 if this FIFO is empty
25	1h RO	**ISP_STR_MON_ISP2SP_accept:** Returns the value 1 if the token FIFO between ISP and SP can accept a token from the ISP. Returns the value 0 if this token FIFO is full.
24	0h RO	**ISP_STR_MON_ISP2SP_valid:** Returns the value 1 if ISP sends a token using the streaming port connected to the SP token FIFO. Returns the value 0 if the ISP does not send a token to the SP
23	0h RO	**ISP_STR_MON_GPD2ISP_accept:** Returns the value 1 if the ISP can accept a token from the streaming FIFO between the fifo adpater in GP devices and the ISP. Returns 0 if the ISP cannot accept a token from this FIFO.
22	0h RO	**ISP_STR_MON_GPD2ISP_valid:** Returns the value 1 if the streaming FIFO between the fifo adapter in GP devices and the ISP has a valid token for the ISP. Returns the value 0 if this FIFO is empty.
21	1h RO	**ISP_STR_MON_ISP2GPD_accept:** Returns the value 1 if the token FIFO between ISP and fifo adapter can accept a token from the ISP. Returns the value 0 if this token FIFO is full.
20	0h RO	**ISP_STR_MON_ISP2GPD_valid:** Returns the value 1 if ISP sends a token using the streaming port connected to the token FIFO between the ISP and the fifo adapter in GP_devices. Returns the value 0 if the ISP does not send a token to the fifo adapter.

Bit Range	Default & Access	Description
19	0h RO	**ISP_STR_MON_GDC22ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the GDC2 acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
18	0h RO	**ISP_STR_MON_GDC22ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC2 acknowledge port and the ISP, is present on the GDC2 input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
17	0h RO	**ISP_STR_MON_ISP2GDC2_accept:** Returns the value 1 if the command FIFO between ISP and GDC2 can accept a command from the ISP. Returns the value 0 if this command FIFO is full.
16	0h RO	**ISP_STR_MON_ISP2GDC2_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the GDC2 command FIFO. Returns the value 0 if the ISP does not send a command to GDC2
15	0h RO	**ISP_STR_MON_GDC12ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the GDC1 acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
14	0h RO	**ISP_STR_MON_GDC12ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC1 acknowledge port and the ISP, is present on the GDC1 input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
13	0h RO	**ISP_STR_MON_ISP2GDC1_accept:** Returns the value 1 if the command FIFO between ISP and GDC1 can accept a command from the ISP. Returns the value 0 if this command FIFO is full.
12	0h RO	**ISP_STR_MON_ISP2GDC1_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the GDC1 command FIFO. Returns the value 0 if the ISP does not send a command to GDC1
11	0h RO	**ISP_STR_MON_DMA2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the DMA acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
10	0h RO	**ISP_STR_MON_DMA2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the DMA acknowledge port and the ISP, is present on the DMA input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
9	0h RO	**ISP_STR_MON_ISP2DMA_accept:** Returns the value 1 if the command FIFO between ISP and the DMA can accept a command from the ISP. Returns the value 0 if this command FIFO cannot accept a token from the ISP.
8	0h RO	**ISP_STR_MON_ISP2DMA_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the DMA command FIFO. Returns the value 0 if the ISP does not send a command to the DMA
7	0h RO	**ISP_STR_MON_PIFB2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the primary input formatter B acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
6	0h RO	**ISP_STR_MON_PIFB2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter B acknowledge port and the ISP, is present on the primary input formatter B input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
5	0h RO	**ISP_STR_MON_ISP2PIFB_accept:** Returns the value 1 if the command FIFO between ISP and the Primary input formatter B can accept a command from the ISP. Returns the value 0 if this FIFO cannot accept a command from the ISP.
4	0h RO	**ISP_STR_MON_ISP2PIFB_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the Primary Input Formatter B command FIFO. Returns the value 0 if the ISP does not send a command to the Primary Input formatter B
3	0h RO	**ISP_STR_MON_PIF2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the primary input formatter acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.

Bit Range	Default & Access	Description
2	0h RO	**ISP_STR_MON_PIF2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter acknowledge port and the ISP, is present on the primary input formatter input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
1	0h RO	**ISP_STR_MON_ISP2PIF_accept:** Returns the value 1 if the command FIFO between ISP and the Primary input formatter can accept a command from the ISP. Returns the value 0 if this command FIFO is full.
0	0h RO	**ISP_STR_MON_ISP2PIF_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the Primary Input Formatter command FIFO. Returns the value 0 if the ISP does not send a command to the Primary Input formatter

15.8.8 reg_gpd_gp_reg_reg_gp_mod_stream_stat_type (gpd_gp_reg_reg_gp_mod_stream_stat)—Offset 1Ch

Indicate the status of the streaming ports of the modules. All module's valid and accept ports used for control are reflected in this register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_mod_stream_stat: [ISPMMADR] + 1Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: AA88A222h

Bit	Value	Field
31	1	MOD_STR_MON_CELLS2GDC2_accept
30	0	MOD_STR_MON_CELLS2GDC2_valid
29	1	MOD_STR_MON_GDC22CELLS_accept
28	0	MOD_STR_MON_GDC22CELLS_valid
27	1	MOD_STR_MON_CELLS2GDC1_accept
26	0	MOD_STR_MON_CELLS2GDC1_valid
25	1	MOD_STR_MON_GDC12CELLS_accept
24	0	MOD_STR_MON_GDC12CELLS_valid
23	1	MOD_STR_MON_SP2DMA_accept
22	0	MOD_STR_MON_SP2DMA_valid
21	0	MOD_STR_MON_DMA2SP_accept
20	0	MOD_STR_MON_DMA2SP_valid
19	1	MOD_STR_MON_ISP2DMA_accept
18	0	MOD_STR_MON_ISP2DMA_valid
17	0	MOD_STR_MON_DMA2ISP_accept
16	0	MOD_STR_MON_DMA2ISP_valid
15	1	MOD_STR_MON_SP2MC_accept
14	0	MOD_STR_MON_SP2MC_valid
13	1	MOD_STR_MON_MC2SP_accept
12	0	MOD_STR_MON_MC2SP_valid
11	0	MOD_STR_MON_SP2SIF_accept
10	0	MOD_STR_MON_SP2SIF_valid
9	1	MOD_STR_MON_SIF2SP_accept
8	0	MOD_STR_MON_SIF2SP_valid
7	0	MOD_STR_MON_CELLS2PIFB_accept
6	0	MOD_STR_MON_CELLS2PIFB_valid
5	1	MOD_STR_MON_PIFB2CELLS_accept
4	0	MOD_STR_MON_PIFB2CELLS_valid
3	0	MOD_STR_MON_CELLS2PIFA_accept
2	0	MOD_STR_MON_CELLS2PIFA_valid
1	1	MOD_STR_MON_PIFA2CELLS_accept
0	0	MOD_STR_MON_PIFA2CELLS_valid

Bit Range	Default & Access	Description
31	1h RO	**MOD_STR_MON_CELLS2GDC2_accept:** Returns the value 1 if the acknowledge FIFO between GDC2 and ISP/SP can accept an acknowledge token from GDC2. Returns the value 0 if this FIFO is full.
30	0h RO	**MOD_STR_MON_CELLS2GDC2_valid:** Returns the value 1 if GDC2 sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if GDC2 does not send an acknowledge token to this FIFO.
29	1h RO	**MOD_STR_MON_GDC22CELLS_accept:** Returns the value 1 if GDC2 can accept a command token from the command FIFO between the ISP/SP and GDC2. Returns the value 0 if GDC2 cannot accept a command token.

Bit Range	Default & Access	Description
28	0h RO	**MOD_STR_MON_GDC22CELLS_valid:** Returns the value 1 if there is a command available on the command fifo between SP/ISP and GDC2. Returns the value 0 if the command FIFO for GDC2 is empty.
27	1h RO	**MOD_STR_MON_CELLS2GDC1_accept:** Returns the value 1 if the acknowledge FIFO between GDC1 and ISP/SP can accept an acknowledge token from GDC1. Returns the value 0 if this FIFO is full.
26	0h RO	**MOD_STR_MON_CELLS2GDC1_valid:** Returns the value 1 if GDC1 sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if GDC1 does not send an acknowledge token to this FIFO.
25	1h RO	**MOD_STR_MON_GDC12CELLS_accept:** Returns the value 1 if GDC1 can accept a command token from the command FIFO between the ISP/SP and GDC1. Returns the value 0 if GDC1 cannot accept a command token.
24	0h RO	**MOD_STR_MON_GDC12CELLS_valid:** Returns the value 1 if there is a command available on the command fifo between SP/ISP and GDC1. Returns the value 0 if the command FIFO for GDC1 is empty.
23	1h RO	**MOD_STR_MON_SP2DMA_accept:** Returns the value 1 if the acknowledge FIFO between the DMA and SP can accept an acknowledge token from the DMA. Returns the value 0 if this FIFO is full.
22	0h RO	**MOD_STR_MON_SP2DMA_valid:** Returns the value 1 if DMA sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the SP. Returns the value 0 if the DMA does not send an acknowledge token to this FIFO.
21	0h RO	**MOD_STR_MON_DMA2SP_accept:** Returns the value 1 if the DMA can accept a command token from the command FIFO between the SP and the DMA. Returns the value 0 if the DMA cannot accept a command token.
20	0h RO	**MOD_STR_MON_DMA2SP_valid:** Returns the value 1 if there is a command available on the command fifo between SP and the DMA. Returns the value 0 if the command FIFO for the DMA is empty.
19	1h RO	**MOD_STR_MON_ISP2DMA_accept:** Returns the value 1 if the acknowledge FIFO between the DMA and ISP can accept an acknowledge token from the DMA. Returns the value 0 if this FIFO is full.
18	0h RO	**MOD_STR_MON_ISP2DMA_valid:** Returns the value 1 if DMA sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP. Returns the value 0 if the DMA does not send an acknowledge token to this FIFO.
17	0h RO	**MOD_STR_MON_DMA2ISP_accept:** Returns the value 1 if the DMA can accept a command token from the command FIFO between the SP and the DMA. Returns the value 0 if the DMA cannot accept a command token.
16	0h RO	**MOD_STR_MON_DMA2ISP_valid:** Returns the value 1 if there is a command available on the command fifo between ISP and the DMA. Returns the value 0 if the command FIFO for the DMA is empty.
15	1h RO	**MOD_STR_MON_SP2MC_accept:** Returns the value 1 if stream2mem can accept a command token from the command FIFO between the SP and the stream2mem. Returns the value 0 if stream2mem cannot accept a command token.
14	0h RO	**MOD_STR_MON_SP2MC_valid:** Returns the value 1 if there is a command available on the command fifo between the SP and the stream2mem. Returns the value 0 if the command FIFO for the stream2mem is empty.
13	1h RO	**MOD_STR_MON_MC2SP_accept:** Returns the value 1 if the acknowledge FIFO between the stream2mem and the SP can accept an acknowledge token from the stream2mem. Returns the value 0 if this FIFO is full.
12	0h RO	**MOD_STR_MON_MC2SP_valid:** Returns the value 1 if the stream2mem sends an acknowledge token using its acknowledge output port connected to the acknowledge FIFO between the stream2mem and the SP. Returns the value 0 if the stream2mem does not send an acknowledge token to this FIFO.
11	0h RO	**MOD_STR_MON_SP2SIF_accept:** Returns the value 1 if secondary input formatter can accept a command token from the command FIFO between the SP and the secondary input formatter. Returns the value 0 if this FIFO is full.

Bit Range	Default & Access	Description
10	0h RO	**MOD_STR_MON_SP2SIF_valid:** Returns the value 1 if there is a command available on the command fifo between the SP and the secondary input formatter. Returns the value 0 if the command FIFO for the secondary input formatter is empty.
9	1h RO	**MOD_STR_MON_SIF2SP_accept:** Returns the value 1 if the acknowledge FIFO between the secondary input formatter and the SP can accept an acknowledge token from the secondary input formatter. Returns the value 0 if this FIFO is full.
8	0h RO	**MOD_STR_MON_SIF2SP_valid:** Returns the value 1 if the secondary input formatter sends an acknowledge token using its acknowledge output port connected to the acknowledge FIFO between the secondary input formatter and the SP. Returns the value 0 if the secondary input formatter does not send an acknowledge token to this FIFO.
7	0h RO	**MOD_STR_MON_CELLS2PIFB_accept:** Returns the value 1 if primary input formatter B can accept a command token from the command FIFO between the ISP/SP and the primary input formatter B. Returns the value 0 if the primary input formatter B cannot accept a command token.
6	0h RO	**MOD_STR_MON_CELLS2PIFB_valid:** Returns the value 1 if there is a command available on the command fifo between SP/ISP and the primary input formatter B. Returns the value 0 if the command FIFO for the primary input formatter B is empty.
5	1h RO	**MOD_STR_MON_PIFB2CELLS_accept:** Returns the value 1 if the acknowledge FIFO between the primary input formatter B and the ISP/SP can accept an acknowledge token from the primary input formatter B. Returns the value 0 if this command FIFO is full.
4	0h RO	**MOD_STR_MON_PIFB2CELLS_valid:** Returns the value 1 if primary input formatter B sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if the primary input formatter B does not send an acknowledge token to this FIFO.
3	0h RO	**MOD_STR_MON_CELLS2PIFA_accept:** Returns the value 1 if primary input formatter A can accept a command token from the command FIFO between the ISP/SP and the primary input formatter A. Returns the value 0 if the primary input formatter A cannot accept a command token.
2	0h RO	**MOD_STR_MON_CELLS2PIFA_valid:** Returns the value 1 if there is a command available on the command fifo between SP/ISP and the primary input formatter A. Returns the value 0 if the command FIFO for the primary input formatter A is empty.
1	1h RO	**MOD_STR_MON_PIFA2CELLS_accept:** Returns the value 1 if the acknowledge FIFO between the primary input formatter A and the ISP/SP can accept an acknowledge token from the primary input formatter A. Returns the value 0 if this command FIFO is full.
0	0h RO	**MOD_STR_MON_PIFA2CELLS_valid:** Returns the value 1 if primary input formatter A sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if the primary input formatter A does not send an acknowledge token to this FIFO.

15.8.9 reg_gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond)—Offset 20h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond: [ISPMMADR] + 20h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_gp_sp_stream_stat_irq_cond

Bit Range	Default & Access	Description
31:0	0h RW	**reg_gp_sp_stream_stat_irq_cond:** This register indicates which condition of the SP streaming ports will enable the SP streaming stat irq output

15.8.10 reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond_type (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond)—Offset 24h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond: [ISPMMADR] + 24h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_sp_stream_stat_b_irq_cond

reg_gp_sp_stream_stat_b_irq_cond

Bit Range	Default & Access	Description
31:8	0h RW	**unused_reg_gp_sp_stream_stat_b_irq_cond:** Unused
7:0	0h RW	**reg_gp_sp_stream_stat_b_irq_cond:** This register indicates which condition of the SP streaming ports b will enable the SP streaming stat b irq output

15.8.11 reg_gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond)—Offset 28h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond:
[ISPMMADR] + 28h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_reg_gp_isp_stream_stat_irq_cond

reg_gp_isp_stream_stat_irq_cond

Bit Range	Default & Access	Description
31:28	0h RW	**unused_reg_gp_isp_stream_stat_irq_cond:** Unused
27:0	0h RW	**reg_gp_isp_stream_stat_irq_cond:** This register indicates which condition of the ISP streaming ports will enable the ISP streaming stat irq output

15.8.12 reg_gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond_type (gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond)—Offset 2Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond:
[ISPMMADR] + 2Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_gp_mod_stream_stat_irq_cond

Bit Range	Default & Access	Description
31:0	0h RW	**reg_gp_mod_stream_stat_irq_cond:** This register indicates which condition of the MOD streaming ports will enable the MOD streaming stat irq output

15.8.13 reg_gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable)—Offset 30h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable:
[ISPMMADR] + 30h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_sp_stream_stat_irq_enable

reg_gp_sp_stream_stat_irq_enable

Bit Range	Default & Access	Description
31:16	0h RW	**unused_reg_gp_sp_stream_stat_irq_enable:** Unused
15:0	0h RW	**reg_gp_sp_stream_stat_irq_enable:** This register enables the SP streaming stat irq output for each of the 16 ports

15.8.14 reg_gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable_type (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable)—Offset 34h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable: [ISPMMADR] + 34h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_sp_stream_stat_b_irq_enable (bits 31:4)
reg_gp_sp_stream_stat_b_irq_enable (bits 3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_gp_sp_stream_stat_b_irq_enable:** Unused
3:0	0h RW	**reg_gp_sp_stream_stat_b_irq_enable:** This register enables the SP streaming stat b irq output for each of the 4 ports

15.8.15 reg_gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable)—Offset 38h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable:** [ISPMMADR] + 38h
	ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
	ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gp_isp_stream_stat_irq_enable (31:14); reg_gp_isp_stream_stat_irq_enable (13:0)

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_isp_stream_stat_irq_enable:** Unused
13:0	0h RW	**reg_gp_isp_stream_stat_irq_enable:** This register enables the ISP streaming stat irq output for each of the 14 ports

15.8.16 reg_gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable_type (gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable:** [ISPMMADR] + 3Ch
	ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
	ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_mod_stream_stat_irq_enable

reg_gp_mod_stream_stat_irq_enable

Bit Range	Default & Access	Description
31:16	0h RW	**unused_reg_gp_mod_stream_stat_irq_enable:** Unused
15:0	0h RW	**reg_gp_mod_stream_stat_irq_enable:** This register enables the MOD streaming stat irq output for each of the 16 ports

15.8.17 reg_gpd_gp_reg_reg_gp_switch_if_type (gpd_gp_reg_reg_gp_switch_if)—Offset 40h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_switch_if: [ISPMMADR] + 40h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_switch_if

reg_gp_switch_if

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_switch_if:** Unused

Bit Range	Default & Access	Description
0	0h RW	**reg_gp_switch_if:** Selects the control stream switch for the primary input formatter and for primary input formatter b. The input formatters can be controlled by the scalar processor (value=1) or by the ISP (value=0)

15.8.18 reg_gpd_gp_reg_reg_gp_switch_gdc1_type (gpd_gp_reg_reg_gp_switch_gdc1)—Offset 44h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_switch_gdc1: [ISPMMADR] + 44h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
unused_reg_gp_switch_gdc1	reg_gp_switch_gdc1

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_switch_gdc1:** Unused
0	0h RW	**reg_gp_switch_gdc1:** Selects the control stream switch for the GDC1. GDC1 can be controlled by the scalar processor (value=1) or the ISP (value=0)

15.8.19 reg_gpd_gp_reg_reg_gp_switch_gdc2_type (gpd_gp_reg_reg_gp_switch_gdc2)—Offset 48h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_switch_gdc2: [ISPMMADR] + 48h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_gp_switch_gdc2																															reg_gp_switch_gdc2

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_switch_gdc2:** Unused
0	0h RW	**reg_gp_switch_gdc2:** Selects the control stream switch for the GDC2. GDC2 can be controlled by the scalar processor (value=1) or the ISP (value=0)

15.8.20 reg_gpd_gp_reg_reg_gp_srst_type (gpd_gp_reg_reg_gp_srst)—Offset 4Ch

Soft reset for several modules in the system. If '1' is written to a bit, the module(s) connected to that bit are held in reset until a '0' is written to that bit.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gp_reg_reg_gp_srst: [ISPMMADR] + 4Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_gp_srst			SRST_WBUS	SRST_HOST12BUS	SRST_NBUS	SRST_OCP2CIO	SRST_SP	SRST_SF_GDC2_CELLS	SRST_SF_GDC1_CELLS	SRST_SF_DMA_CELLS	SRST_SF_ISYS_SP	SRST_SF_MC_SP	SRST_SF_SIF_SP	SRST_SF_PIF_CELLS	SRST_SF_ISP_SP	SRST_DMA	SRST_SLV_GRP_BUS	SRST_ISP	SRST_VEC_BUS	SRST_GDC2	SRST_GDC1	SRST_IFT_SEC_PIPE	SRST_OSYS	SRST_FACELLFIFOS	SRST_GPTIMER	SRST_TC	SRST_GPIO	SRST_GPDEV_CBUS	SRST_IFMT_CBUS	SRST_ISEL_CBUS	SRST_ISYS_CBUS

Bit Range	Default & Access	Description
31:29	0h RW	**unused_reg_gp_srst:** Unused
28	0h RW	**SRST_WBUS:** soft reset bit for the wide bus

Bit Range	Default & Access	Description
27	0h RW	**SRST_HOST12BUS:** soft reset bit for the bus from host to fifo adapters
26	0h RW	**SRST_NBUS:** soft reset bit for the narrow bus
25	0h RW	**SRST_OCP2CIO:** soft reset bit for the OCP2CIO converter
24	0h RW	**SRST_SP:** soft reset bit for the SP
23	0h RW	**SRST_SF_GDC2_CELLS:** soft reset bit for the FIFOs between the GDC2 and the cells
22	0h RW	**SRST_SF_GDC1_CELLS:** soft reset bit for the FIFOs between the GDC1 and the cells
21	0h RW	**SRST_SF_DMA_CELLS:** soft reset bit for the FIFOs between the DMA and the cells
20	0h RW	**SRST_SF_ISYS_SP:** soft reset bit for the FIFOs between the input system and the SP
19	0h RW	**SRST_SF_MC_SP:** soft reset bit for the FIFOs between the stream2memory and the SP
18	0h RW	**SRST_SF_SIF_SP:** soft reset bit for the FIFOs between the secondary input formatter and the SP
17	0h RW	**SRST_SF_PIF_CELLS:** soft reset bit for the FIFOs between the primary input formatters and the cells
16	0h RW	**SRST_SF_ISP_SP:** soft reset bit for the FIFOs between SP and ISP
15	0h RW	**SRST_DMA:** soft reset bit for the DMA
14	0h RW	**SRST_SLV_GRP_BUS:** soft reset bit for the slave group bus
13	0h RW	**SRST_ISP:** soft reset bit for the isp (vector processor)
12	0h RW	**SRST_VEC_BUS:** soft reset bit for the vector bus
11	0h RW	**SRST_GDC2:** soft reset bit for the GDC2 block
10	0h RW	**SRST_GDC1:** soft reset bit for the GDC1 block
9	0h RW	**SRST_IFT_SEC_PIPE:** soft reset bit for the CIO pipeline after the secondary input formatter
8	0h RW	**SRST_OSYS:** soft reset bit for the blocks in the output system cluster
7	0h RW	**SRST_FACELLFIFOS:** soft reset bit for the fifo's connected to the fifo adapter between host and cells
6	0h RW	**SRST_GPTIMER:** soft reset bit for the GP timer block
5	0h RW	**SRST_TC:** soft reset bit for the timed controller block

Bit Range	Default & Access	Description
4	0h RW	**SRST_GPIO:** soft reset bit for the gpio block
3	0h RW	**SRST_GPDEV_CBUS:** soft reset bit for the gp devices cluster control bus
2	0h RW	**SRST_IFMT_CBUS:** soft reset bit for the input formatting cluster control bus
1	0h RW	**SRST_ISEL_CBUS:** soft reset bit for the input selector cluster control bus
0	0h RW	**SRST_ISYS_CBUS:** soft reset bit for the input system control bus

15.8.21 reg_gpd_gp_reg_reg_gp_slv_reg_srst_type (gpd_gp_reg_reg_gp_slv_reg_srst)—Offset 50h

Soft reset for the slave accessible registers in some blocks. If '1' is written to a bit, the attached registers get their default value. They can only be overwritten after writing a '0' to this bit

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gp_reg_reg_gp_slv_reg_srst: [ISPMMADR] + 50h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_slv_reg_srst (bits 31:3), SLV_REG_SRST_GDC2 (bit 2), SLV_REG_SRST_GDC1 (bit 1), SLV_REG_SRST_DMA (bit 0)

Bit Range	Default & Access	Description
31:3	0h RW	**unused_reg_gp_slv_reg_srst:** Unused
2	0h RW	**SLV_REG_SRST_GDC2:** soft reset bit for the slave registers in the GDC2
1	0h RW	**SLV_REG_SRST_GDC1:** soft reset bit for the slave registers in the GDC1
0	0h RW	**SLV_REG_SRST_DMA:** soft reset bit for the slave registers in the DMA

15.8.22 reg_gpd_tc_FifoWriteCmd_type (gpd_tc_FifoWriteCmd)—Offset 100h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_tc_FifoWriteCmd: [ISPMMADR] + 100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FifoWriteCmd

Bit Range	Default & Access	Description
31:0	0h WO	**FifoWriteCmd:** Timed controller Command input. A Timed Controller command consists of 5 32-bit tokens that need to be written sequentially to this register location

15.8.23 reg_gpd_c_gpio_reg_gpio_doe_type (gpd_c_gpio_reg_gpio_doe)—Offset 400h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_c_gpio_reg_gpio_doe: [ISPMMADR] + 400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gpio_doe

reg_gpio_doe

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_doe:** Unused
11:0	0h RW	**reg_gpio_doe:** indicates for each bit whether it is intended to be an input (value='0') or an output (value='1')

15.8.24 reg_gpd_c_gpio_reg_gpio_do_select_type (gpd_c_gpio_reg_gpio_do_select)—Offset 404h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_c_gpio_reg_gpio_do_select: [ISPMMADR] + 404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gpio_do_select

reg_gpio_do_select

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_do_select:** Unused
11:0	0h RW	**reg_gpio_do_select:** indicates for each bit of gpio_do whether it should have the value from source 0 (value='0') or source 1 (value='1').

15.8.25 reg_gpd_c_gpio_reg_gpio_do_0_type (gpd_c_gpio_reg_gpio_do_0)—Offset 408h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_c_gpio_reg_gpio_do_0: [ISPMMADR] + 408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gpio_do_0

reg_gpio_do_0

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_do_0:** Unused
11:0	0h RW	**reg_gpio_do_0:** provides the value for each of the output bits (source 0)

15.8.26 reg_gpd_c_gpio_reg_gpio_do_1_type (gpd_c_gpio_reg_gpio_do_1)—Offset 40Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_c_gpio_reg_gpio_do_1: [ISPMMADR] + 40Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:12	11:0
0000 0000 0000 0000 0000	0000 0000 0000
unused_reg_gpio_do_1	reg_gpio_do_1

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_do_1:** Unused
11:0	0h RW	**reg_gpio_do_1:** provides the value for each of the output bits (source 1)

15.8.27 reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_0_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_0)—Offset 410h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_cnt_0: [ISPMMADR] + 410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_reg_gpio_do_pwm_cnt_0	reg_gpio_do_pwm_cnt_0

Bit Range	Default & Access	Description
31:6	0h RW	**unused_reg_gpio_do_pwm_cnt_0:** Unused
5:0	0h RW	**reg_gpio_do_pwm_cnt_0:** indicates duty cycle for PWM output 0. value d means duty cycle d/64

15.8.28 reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_1_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_1)—Offset 414h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_cnt_1: [ISPMMADR] + 414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_reg_gpio_do_pwm_cnt_1	reg_gpio_do_pwm_cnt_1

Bit Range	Default & Access	Description
31:6	0h RW	**unused_reg_gpio_do_pwm_cnt_1:** Unused

Bit Range	Default & Access	Description
5:0	0h RW	**reg_gpio_do_pwm_cnt_1:** indicates duty cycle for PWM output 1. value d means duty cycle d/64

15.8.29 reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_2_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_2)—Offset 418h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_cnt_2: [ISPMMADR] + 418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6: unused_reg_gpio_do_pwm_cnt_2
Bits 5:0: reg_gpio_do_pwm_cnt_2

Bit Range	Default & Access	Description
31:6	0h RW	**unused_reg_gpio_do_pwm_cnt_2:** Unused
5:0	0h RW	**reg_gpio_do_pwm_cnt_2:** indicates duty cycle for PWM output 2. value d means duty cycle d/64

15.8.30 reg_gpd_c_gpio_reg_gpio_do_pwm_cnt_3_type (gpd_c_gpio_reg_gpio_do_pwm_cnt_3)—Offset 41Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_cnt_3: [ISPMMADR] + 41Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gpio_do_pwm_cnt_3 | reg_gpio_do_pwm_cnt_3

Bit Range	Default & Access	Description
31:6	0h RW	**unused_reg_gpio_do_pwm_cnt_3:** Unused
5:0	0h RW	**reg_gpio_do_pwm_cnt_3:** indicates duty cycle for PWM output 3. value d means duty cycle d/64

15.8.31 reg_gpd_c_gpio_reg_gpio_do_pwm_main_cnt_type (gpd_c_gpio_reg_gpio_do_pwm_main_cnt)—Offset 420h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_main_cnt: [ISPMMADR] + 420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gpio_do_pwm_main_cnt | reg_gpio_do_pwm_main_cnt

Bit Range	Default & Access	Description
31:20	0h RW	**unused_reg_gpio_do_pwm_main_cnt:** Unused

Bit Range	Default & Access	Description
19:0	0h RW	**reg_gpio_do_pwm_main_cnt:** indicates wrapping value for PWM main counter

15.8.32 reg_gpd_c_gpio_reg_gpio_do_pwm_enable_type (gpd_c_gpio_reg_gpio_do_pwm_enable)—Offset 424h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_do_pwm_enable: [ISPMMADR] + 424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gpio_do_pwm_enable

reg_gpio_do_pwm_enable

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_do_pwm_enable:** Unused
11:0	0h RW	**reg_gpio_do_pwm_enable:** indicates per bit whether PWM is on (value='1') or output is fixed '0' (value='0')

15.8.33 reg_gpd_c_gpio_reg_gpio_di_debouncemethod_type (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debouncemethod: [ISPMMADR] + 428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gpio_di_debouncemethod (31:24), reg_gpio_di_debouncemethod (23:0)

Bit Range	Default & Access	Description
31:24	0h RW	**unused_reg_gpio_di_debouncemethod:** Unused
23:0	0h RW	**reg_gpio_di_debouncemethod:** indicates for each input bit which debouncing counter value is chosen: '00': debounce_cnt0, '01': debounce_cnt1, '10': debounce_cnt2, '11': debounce_cnt3'

15.8.34 reg_gpd_c_gpio_reg_gpio_di_debounce_cnt0_type (gpd_c_gpio_reg_gpio_di_debounce_cnt0)—Offset 42Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debounce_cnt0: [ISPMMADR] + 42Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reg_gpio_di_debounce_cnt0 (31:0)

Bit Range	Default & Access	Description
31:0	0h RW	**reg_gpio_di_debounce_cnt0:** Indicates the period an input has to be stable before passing its value to the output*

15.8.35 reg_gpd_c_gpio_reg_gpio_di_debounce_cnt1_type (gpd_c_gpio_reg_gpio_di_debounce_cnt1)—Offset 430h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debounce_cnt1: [ISPMMADR] + 430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

reg_gpio_di_debounce_cnt1

Bit Range	Default & Access	Description
31:0	0h RW	**reg_gpio_di_debounce_cnt1:** Indicates the period an input has to be stable before passing its value to the output*

15.8.36 reg_gpd_c_gpio_reg_gpio_di_debounce_cnt2_type (gpd_c_gpio_reg_gpio_di_debounce_cnt2)—Offset 434h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debounce_cnt2: [ISPMMADR] + 434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

reg_gpio_di_debounce_cnt2

Bit Range	Default & Access	Description
31:0	0h RW	**reg_gpio_di_debounce_cnt2:** Indicates the period an input has to be stable before passing its value to the output

15.8.37 reg_gpd_c_gpio_reg_gpio_di_debounce_cnt3_type (gpd_c_gpio_reg_gpio_di_debounce_cnt3)—Offset 438h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_debounce_cnt3: [ISPMMADR] + 438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_gpio_di_debounce_cnt3

Bit Range	Default & Access	Description
31:0	0h RW	**reg_gpio_di_debounce_cnt3:** Indicates the period an input has to be stable before passing its value to the output

15.8.38 reg_gpd_c_gpio_reg_gpio_di_activelevel_type (gpd_c_gpio_reg_gpio_di_activelevel)—Offset 43Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di_activelevel: [ISPMMADR] + 43Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000FFFh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Fields: unused_reg_gpio_di_activelevel (bits 31:12); reg_gpio_di_activelevel (bits 11:0)

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_di_activelevel:** Unused
11:0	FFFh RW	**reg_gpio_di_activelevel:** indicates for each bit whether it is intended to be active low (value='0') or active high (value='1').

15.8.39 reg_gpd_c_gpio_reg_gpio_di_type (gpd_c_gpio_reg_gpio_di)—Offset 440h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_c_gpio_reg_gpio_di: [ISPMMADR] + 440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000FFFh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Fields: unused_reg_gpio_di (bits 31:12); reg_gpio_di (bits 11:0)

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gpio_di:** Unused
11:0	FFFh RO	**reg_gpio_di:** contains the values of all debounced, active level compensated inputs

15.8.40 reg_gpd_irq_ctrl_reg_irq_edge_type (gpd_irq_ctrl_reg_irq_edge)—Offset 500h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_irq_ctrl_reg_irq_edge: [ISPMMADR] + 500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_irq_edge

Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_edge:** indicates for each bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

15.8.41 reg_gpd_irq_ctrl_reg_irq_mask_type (gpd_irq_ctrl_reg_irq_mask)—Offset 504h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_irq_ctrl_reg_irq_mask: [ISPMMADR] + 504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_irq_mask

Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_mask:** indicates for each bit of irq_di whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

15.8.42 reg_gpd_irq_ctrl_reg_irq_status_type (gpd_irq_ctrl_reg_irq_status)—Offset 508h

Indicates for each bit whether a non-masked interrupt has been generated (value='1'). Can be cleared by writing a '1' into the the corresponding bit of the req_irq_clear register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_irq_ctrl_reg_irq_status: [ISPMMADR] + 508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31	0	IRQ_STAT_SP_SMON_B
30	0	IRQ_STAT_DMA
29	0	IRQ_STAT_SW_1
28	0	IRQ_STAT_SW_0
27	0	IRQ_STAT_GPTIMER_1
26	0	IRQ_STAT_GPTIMER_0
25	0	IRQ_STAT_ISYS_2
24	0	IRQ_STAT_SP_DMEM_ERROR
23	0	IRQ_STAT_SP_IMEM_ERROR
22	0	IRQ_STAT_ISP_DMEM_ERROR
21	0	IRQ_STAT_ISP_BAMEM_ERROR
20	0	IRQ_STAT_ISP_PMEM_ERROR
19	0	IRQ_STAT_MOD_SMON
18	0	IRQ_STAT_ISP_SMON
17	0	IRQ_STAT_SP_SMON
16	0	IRQ_STAT_IFMT
15	0	IRQ_STAT_ISEL
14	0	IRQ_STAT_ISYS
13	0	IRQ_STAT_ISP
12	0	IRQ_STAT_SP
11:0	0 0 0 0 0 0 0 0 0 0 0 0	IRQ_STAT_GPIO_PINS

Bit Range	Default & Access	Description
31	0h RO	**IRQ_STAT_SP_SMON_B:** Represents the irq status of the irq_out from the SP streaming monitor b
30	0h RO	**IRQ_STAT_DMA:** Represents the irq status of the DMA
29	0h RO	**IRQ_STAT_SW_1:** Represents the irq status of the GP register IRQ SW 1
28	0h RO	**IRQ_STAT_SW_0:** Represents the irq status of the GP register IRQ SW 0
27	0h RO	**IRQ_STAT_GPTIMER_1:** Represents the irq status of the irq[1] out signal from the GP Timer block
26	0h RO	**IRQ_STAT_GPTIMER_0:** Represents the irq status of the irq[0] out signal from the GP Timer block
25	0h RO	**IRQ_STAT_ISYS_2:** Represents the irq status of the irq out signal from the input system
24	0h RO	**IRQ_STAT_SP_DMEM_ERROR:** Represents the irq status of the error signal from the SP data memory
23	0h RO	**IRQ_STAT_SP_IMEM_ERROR:** Represents the irq status of the error signal from the SP instruction cache memory
22	0h RO	**IRQ_STAT_ISP_DMEM_ERROR:** Represents the irq status of the error signal from the ISP data memory
21	0h RO	**IRQ_STAT_ISP_BAMEM_ERROR:** Represents the irq status of the error signal from the ISP vector memory
20	0h RO	**IRQ_STAT_ISP_PMEM_ERROR:** Represents the irq status of the error signal from the ISP program memory
19	0h RO	**IRQ_STAT_MOD_SMON:** Represents the irq status of the irq_out from the MOD streaming monitor

Bit Range	Default & Access	Description
18	0h RO	**IRQ_STAT_ISP_SMON:** Represents the irq status of the irq_out from the ISP streaming monitor
17	0h RO	**IRQ_STAT_SP_SMON:** Represents the irq status of the irq_out from the SP streaming monitor
16	0h RO	**IRQ_STAT_IFMT:** Represents the irq status of the irq_out from the input formatting subsystem
15	0h RO	**IRQ_STAT_ISEL:** Represents the irq status of the irq_out from the input selector
14	0h RO	**IRQ_STAT_ISYS:** Represents the irq status of the irq_out from the input system
13	0h RO	**IRQ_STAT_ISP:** Represents the irq status of the irq_out from isp2300
12	0h RO	**IRQ_STAT_SP:** Represents the irq status of the irq_out from scalar processor
11:0	0h RO	**IRQ_STAT_GPIO_PINS:** Represents the irq status of the - potentially debounced - GPIO input pins

15.8.43 reg_gpd_irq_ctrl_reg_irq_clear_type (gpd_irq_ctrl_reg_irq_clear)—Offset 50Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_irq_ctrl_reg_irq_clear: [ISPMMADR] + 50Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_irq_clear

Bit Range	Default & Access	Description
31:0	0h WO	**reg_irq_clear:** Clears (set to '0') bits in reg_irq_status. When writing a '1' into a bit of this register, the corresponding bit in the req_irq_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the req_irq_status is not affected.

15.8.44 reg_gpd_irq_ctrl_reg_irq_enable_type (gpd_irq_ctrl_reg_irq_enable)—Offset 510h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_irq_ctrl_reg_irq_enable: [ISPMMADR] + 510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_irq_enable

Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also affects the IRQ pin (value='1') or not (value='0')

15.8.45 reg_gpd_irq_ctrl_reg_irq_level_not_pulse_type (gpd_irq_ctrl_reg_irq_level_not_pulse)—Offset 514h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_irq_ctrl_reg_irq_level_not_pulse: [ISPMMADR] + 514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_irq_level_not_pulse

Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_level_not_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

15.8.46 reg_gpd_irq_ctrl_reg_irq_str_out_enable_type (gpd_irq_ctrl_reg_irq_str_out_enable)—Offset 518h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_irq_ctrl_reg_irq_str_out_enable: [ISPMMADR] + 518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_irq_str_out_enable

Bit Range	Default & Access	Description
31:0	0h RW	**reg_irq_str_out_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also results in a send token on the irq_str_out port (value='1') or not (value='0')

15.8.47 reg_gpd_gptimer_reg_reset_type (gpd_gptimer_reg_reset)—Offset 600h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_reg_reset: [ISPMMADR] + 600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_reset

reg_reset

Bit Range	Default & Access	Description
31:8	0h RW	**unused_reg_reset:** Unused
7:0	0h WO	**reg_reset:** GP Timer reset. Write '1' to bit x to reset timer x. Write 0xFF to reset all timers.

15.8.48 reg_gpd_gptimer_overall_enable_type (gpd_gptimer_overall_enable)—Offset 604h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_overall_enable: [ISPMMADR] + 604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_overall_enable (31:1), overall_enable (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_overall_enable:** Unused
0	0h RW	**overall_enable:** GP Timer enable. Write '1' to enable all enabled timers, write '0' to disable all timers.

15.8.49 reg_gpd_gptimer_enable_timer_0_type (gpd_gptimer_enable_timer_0)—Offset 608h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_0: [ISPMMADR] + 608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_enable_timer_0 (31:1), enable_timer_0 (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_0:** Unused
0	0h RW	**enable_timer_0:** GP Timer enable. Write '1' to enable timer 0. Write '0' to disable timer 0

15.8.50 reg_gpd_gptimer_enable_timer_1_type (gpd_gptimer_enable_timer_1)—Offset 60Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_enable_timer_1: [ISPMMADR] + 60Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															unused_enable_timer_1																enable_timer_1

Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_1:** Unused
0	0h RW	**enable_timer_1:** GP Timer enable. Write '1' to enable timer 1. Write '0' to disable timer 1

15.8.51 reg_gpd_gptimer_enable_timer_2_type (gpd_gptimer_enable_timer_2)—Offset 610h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_enable_timer_2: [ISPMMADR] + 610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															unused_enable_timer_2																enable_timer_2

Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_2:** Unused
0	0h RW	**enable_timer_2:** GP Timer enable. Write '1' to enable timer 2. Write '0' to disable timer 2

15.8.52 reg_gpd_gptimer_enable_timer_3_type (gpd_gptimer_enable_timer_3)—Offset 614h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_3: [ISPMMADR] + 614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_enable_timer_3 (bits 31:1), enable_timer_3 (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_3:** Unused
0	0h RW	**enable_timer_3:** GP Timer enable. Write '1' to enable timer 3. Write '0' to disable timer 3

15.8.53 reg_gpd_gptimer_enable_timer_4_type (gpd_gptimer_enable_timer_4)—Offset 618h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_4: [ISPMMADR] + 618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_enable_timer_4 (bits 31:1), enable_timer_4 (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_4:** Unused
0	0h RW	**enable_timer_4:** GP Timer enable. Write '1' to enable timer 4. Write '0' to disable timer 4

15.8.54 reg_gpd_gptimer_enable_timer_5_type (gpd_gptimer_enable_timer_5)—Offset 61Ch

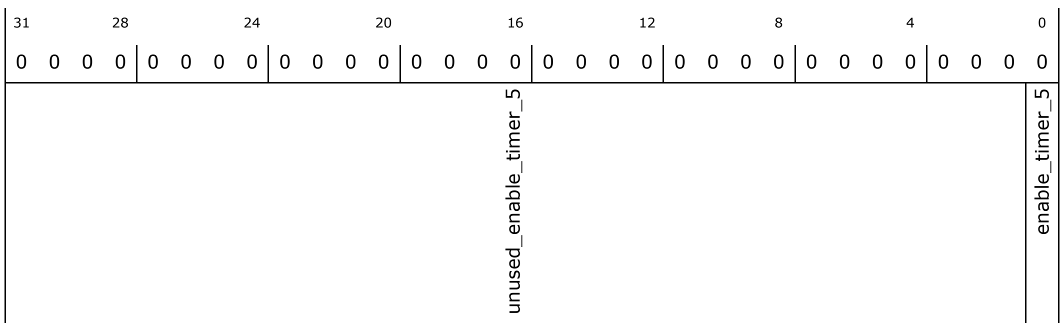
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_5: [ISPMMADR] + 61Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_5:** Unused
0	0h RW	**enable_timer_5:** GP Timer enable. Write '1' to enable timer 5. Write '0' to disable timer 5

15.8.55 reg_gpd_gptimer_enable_timer_6_type (gpd_gptimer_enable_timer_6)—Offset 620h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_enable_timer_6: [ISPMMADR] + 620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_enable_timer_6

enable_timer_6

Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_6:** Unused
0	0h RW	**enable_timer_6:** GP Timer enable. Write '1' to enable timer 6. Write '0' to disable timer 6

15.8.56 reg_gpd_gptimer_enable_timer_7_type (gpd_gptimer_enable_timer_7)—Offset 624h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_enable_timer_7: [ISPMMADR] + 624h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_enable_timer_7

enable_timer_7

Bit Range	Default & Access	Description
31:1	0h RW	**unused_enable_timer_7:** Unused
0	0h RW	**enable_timer_7:** GP Timer enable. Write '1' to enable timer 7. Write '0' to disable timer 7

15.8.57 reg_gpd_gptimer_value_timer_0_type (gpd_gptimer_value_timer_0)—Offset 628h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_value_timer_0: [ISPMMADR] + 628h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

value_timer_0

Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_0:** Returns the value of timer 0

15.8.58 reg_gpd_gptimer_value_timer_1_type (gpd_gptimer_value_timer_1)—Offset 62Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_value_timer_1: [ISPMMADR] + 62Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

value_timer_1

Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_1:** Returns the value of timer 1

15.8.59 reg_gpd_gptimer_value_timer_2_type (gpd_gptimer_value_timer_2)—Offset 630h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_value_timer_2: [ISPMMADR] + 630h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
value_timer_2																															

Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_2:** Returns the value of timer 2

15.8.60 reg_gpd_gptimer_value_timer_3_type (gpd_gptimer_value_timer_3)—Offset 634h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_value_timer_3: [ISPMMADR] + 634h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
value_timer_3																															

Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_3:** Returns the value of timer 3

15.8.61 reg_gpd_gptimer_value_timer_4_type (gpd_gptimer_value_timer_4)—Offset 638h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_value_timer_4: [ISPMMADR] + 638h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

value_timer_4

Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_4:** Returns the value of timer 4

15.8.62 reg_gpd_gptimer_value_timer_5_type (gpd_gptimer_value_timer_5)—Offset 63Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_value_timer_5: [ISPMMADR] + 63Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

value_timer_5

Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_5:** Returns the value of timer 5

15.8.63 reg_gpd_gptimer_value_timer_6_type (gpd_gptimer_value_timer_6)—Offset 640h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_value_timer_6: [ISPMMADR] + 640h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

value_timer_6

Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_6:** Returns the value of timer 6

15.8.64 reg_gpd_gptimer_value_timer_7_type (gpd_gptimer_value_timer_7)—Offset 644h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_value_timer_7: [ISPMMADR] + 644h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

value_timer_7

Bit Range	Default & Access	Description
31:0	0h RO	**value_timer_7:** Returns the value of timer 7

15.8.65 reg_gpd_gptimer_count_type_timer_0_type (gpd_gptimer_count_type_timer_0)—Offset 648h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_count_type_timer_0: [ISPMMADR] + 648h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_count_type_timer_0 (bits 31:2), count_type_timer_0 (bits 1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_0:** Unused
1:0	0h RW	**count_type_timer_0:** Indicates what needs to be counted by timer 0, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

15.8.66 reg_gpd_gptimer_count_type_timer_1_type (gpd_gptimer_count_type_timer_1)—Offset 64Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_count_type_timer_1: [ISPMMADR] + 64Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_count_type_timer_1 (bits 31:2), count_type_timer_1 (bits 1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_1:** Unused
1:0	0h RW	**count_type_timer_1:** Indicates what needs to be counted by timer 1, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

15.8.67 reg_gpd_gptimer_count_type_timer_2_type (gpd_gptimer_count_type_timer_2)—Offset 650h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_count_type_timer_2: [ISPMMADR] + 650h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_count_type_timer_2

count_type_timer_2

Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_2:** Unused
1:0	0h RW	**count_type_timer_2:** Indicates what needs to be counted by timer 2, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

15.8.68 reg_gpd_gptimer_count_type_timer_3_type (gpd_gptimer_count_type_timer_3)—Offset 654h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_count_type_timer_3: [ISPMMADR] + 654h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_count_type_timer_3

count_type_timer_3

Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_3:** Unused
1:0	0h RW	**count_type_timer_3:** Indicates what needs to be counted by timer 3, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

15.8.69 reg_gpd_gptimer_count_type_timer_4_type (gpd_gptimer_count_type_timer_4)—Offset 658h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_count_type_timer_4: [ISPMMADR] + 658h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:2	Bits 1:0
unused_count_type_timer_4	count_type_timer_4

Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_4:** Unused
1:0	0h RW	**count_type_timer_4:** Indicates what needs to be counted by timer 4, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

15.8.70 reg_gpd_gptimer_count_type_timer_5_type (gpd_gptimer_count_type_timer_5)—Offset 65Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_count_type_timer_5: [ISPMMADR] + 65Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_count_type_timer_5 (31:2), count_type_timer_5 (1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_5:** Unused
1:0	0h RW	**count_type_timer_5:** Indicates what needs to be counted by timer 5, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

15.8.71 reg_gpd_gptimer_count_type_timer_6_type (gpd_gptimer_count_type_timer_6)—Offset 660h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_count_type_timer_6: [ISPMMADR] + 660h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_count_type_timer_6 (31:2), count_type_timer_6 (1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_6:** Unused
1:0	0h RW	**count_type_timer_6:** Indicates what needs to be counted by timer 6, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

15.8.72 reg_gpd_gptimer_count_type_timer_7_type (gpd_gptimer_count_type_timer_7)—Offset 664h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_count_type_timer_7: [ISPMMADR] + 664h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_count_type_timer_7 | count_type_timer_7

Bit Range	Default & Access	Description
31:2	0h RW	**unused_count_type_timer_7:** Unused
1:0	0h RW	**count_type_timer_7:** Indicates what needs to be counted by timer 7, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

15.8.73 reg_gpd_gptimer_signal_select_timer_0_type (gpd_gptimer_signal_select_timer_0)—Offset 668h

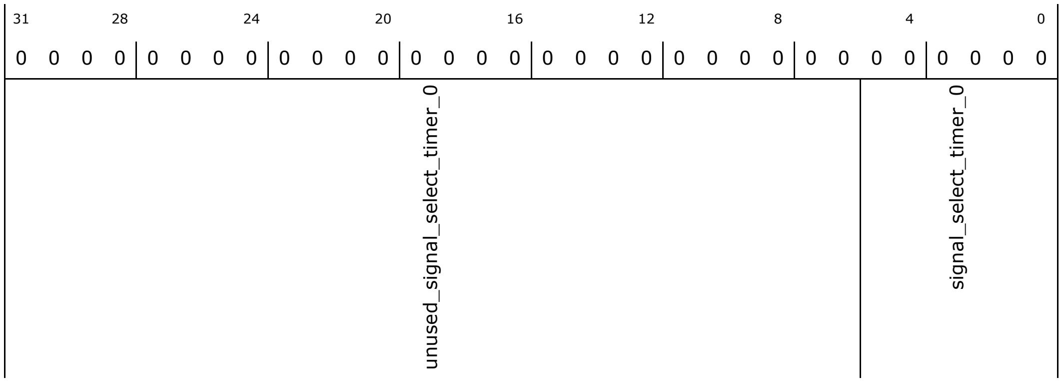
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_signal_select_timer_0: [ISPMMADR] + 668h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_0:** Unused
5:0	0h RW	**signal_select_timer_0:** Selects which of the 55 input signals is counted by timer 0

15.8.74 reg_gpd_gptimer_signal_select_timer_1_type (gpd_gptimer_signal_select_timer_1)—Offset 66Ch

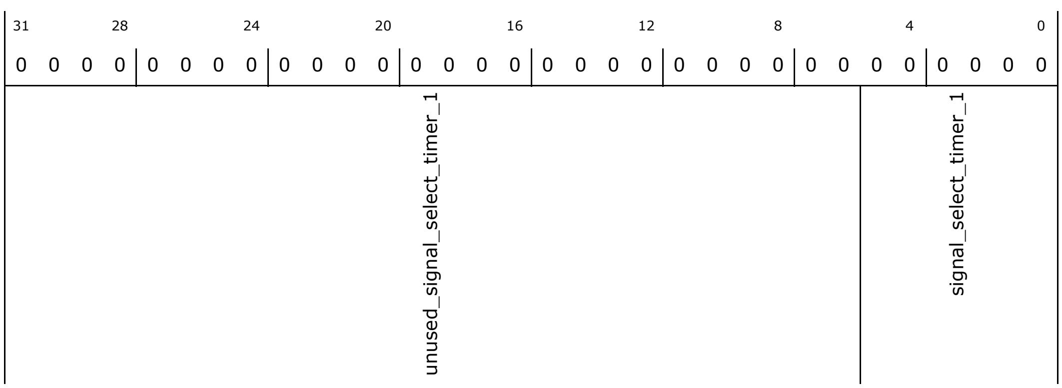
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_1: [ISPMMADR] + 66Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_1:** Unused
5:0	0h RW	**signal_select_timer_1:** Selects which of the 55 input signals is counted by timer 1

15.8.75 reg_gpd_gptimer_signal_select_timer_2_type (gpd_gptimer_signal_select_timer_2)—Offset 670h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_2: [ISPMMADR] + 670h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bits 5:0
unused_signal_select_timer_2	signal_select_timer_2

Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_2:** Unused
5:0	0h RW	**signal_select_timer_2:** Selects which of the 55 input signals is counted by timer 2

15.8.76 reg_gpd_gptimer_signal_select_timer_3_type (gpd_gptimer_signal_select_timer_3)—Offset 674h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_3: [ISPMMADR] + 674h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_signal_select_timer_3	signal_select_timer_3

Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_3:** Unused
5:0	0h RW	**signal_select_timer_3:** Selects which of the 55 input signals is counted by timer 3

15.8.77 reg_gpd_gptimer_signal_select_timer_4_type (gpd_gptimer_signal_select_timer_4)—Offset 678h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_signal_select_timer_4: [ISPMMADR] + 678h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_signal_select_timer_4	signal_select_timer_4

Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_4:** Unused
5:0	0h RW	**signal_select_timer_4:** Selects which of the 55 input signals is counted by timer 4

15.8.78 reg_gpd_gptimer_signal_select_timer_5_type (gpd_gptimer_signal_select_timer_5)—Offset 67Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_signal_select_timer_5: [ISPMMADR] + 67Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_signal_select_timer_5	signal_select_timer_5

Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_5:** Unused
5:0	0h RW	**signal_select_timer_5:** Selects which of the 55 input signals is counted by timer 5

15.8.79 reg_gpd_gptimer_signal_select_timer_6_type (gpd_gptimer_signal_select_timer_6)—Offset 680h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_signal_select_timer_6: [ISPMMADR] + 680h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_signal_select_timer_6 | signal_select_timer_6

Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_6:** Unused
5:0	0h RW	**signal_select_timer_6:** Selects which of the 55 input signals is counted by timer 6

15.8.80 reg_gpd_gptimer_signal_select_timer_7_type (gpd_gptimer_signal_select_timer_7)—Offset 684h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_signal_select_timer_7: [ISPMMADR] + 684h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_signal_select_timer_7 | signal_select_timer_7

Bit Range	Default & Access	Description
31:6	0h RW	**unused_signal_select_timer_7:** Unused
5:0	0h RW	**signal_select_timer_7:** Selects which of the 55 input signals is counted by timer 7

15.8.81 reg_gpd_gptimer_irq_trigger_value_0_type (gpd_gptimer_irq_trigger_value_0)—Offset 688h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_irq_trigger_value_0: [ISPMMADR] + 688h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

irq_trigger_value_0

Bit Range	Default & Access	Description
31:0	0h RW	**irq_trigger_value_0:** IRQ trigger value for interrupt 0. If the timer selected by irq_timer_select_0 reaches this value, irq_0 will be enabled

15.8.82 reg_gpd_gptimer_irq_trigger_value_1_type (gpd_gptimer_irq_trigger_value_1)—Offset 68Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_irq_trigger_value_1: [ISPMMADR] + 68Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

irq_trigger_value_1

Bit Range	Default & Access	Description
31:0	0h RW	**irq_trigger_value_1:** IRQ trigger value for interrupt 1. If the timer selected by irq_timer_select_1 reaches this value, irq_1 will be enabled

15.8.83 reg_gpd_gptimer_irq_timer_select_0_type (gpd_gptimer_irq_timer_select_0)—Offset 690h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_irq_timer_select_0: [ISPMMADR] + 690h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_irq_timer_select_0 (31:3), irq_timer_select_0 (2:0)

Bit Range	Default & Access	Description
31:3	0h RW	**unused_irq_timer_select_0:** Unused
2:0	0h RW	**irq_timer_select_0:** Indicates which of the 8 timers will be used for irq_0 generation

15.8.84 reg_gpd_gptimer_irq_timer_select_1_type (gpd_gptimer_irq_timer_select_1)—Offset 694h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gpd_gptimer_irq_timer_select_1: [ISPMMADR] + 694h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_irq_timer_select_1 (31:3), irq_timer_select_1 (2:0)

Bit Range	Default & Access	Description
31:3	0h RW	**unused_irq_timer_select_1:** Unused
2:0	0h RW	**irq_timer_select_1:** Indicates which of the 8 timers will be used for irq_1 generation

15.8.85 reg_gpd_gptimer_irq_enable_0_type (gpd_gptimer_irq_enable_0)—Offset 698h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_irq_enable_0: [ISPMMADR] + 698h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_irq_enable_0 (bits 31:1), irq_enable_0 (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_irq_enable_0:** Unused
0	0h RW	**irq_enable_0:** Enable interrupt 0

15.8.86 reg_gpd_gptimer_irq_enable_1_type (gpd_gptimer_irq_enable_1)—Offset 69Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gpd_gptimer_irq_enable_1: [ISPMMADR] + 69Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:1	0
Default	0000 0000 0000 0000 0000 0000 0000 000	0
Field	unused_irq_enable_1	irq_enable_1

Bit Range	Default & Access	Description
31:1	0h RW	**unused_irq_enable_1:** Unused
0	0h RW	**irq_enable_1:** Enable interrupt 1

15.8.87 reg_scp_stat_and_ctrl_type (scp_stat_and_ctrl)—Offset 10000h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_stat_and_ctrl: [ISPMMADR] + 10000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000A0h

Bits	Default	Field
31:29	000	unused_stat_and_ctrl
28:24	00000	arb_cont_dmem_Arb_mem_wp_source1
23:19	00000	arb_cont_dmem_Arb_mem_wp_source0
18:14	00000	arb_period_dmem_Arb_mem_wp
13	0	prefetch_enable_flag
12	0	invalidate_cache_flag
11	0	sleeping_irq_mask_flag
10	0	ready_irq_mask_flag
9	0	broken_irq_mask_flag
8	0	irq_clear_flag
7	1	stalling_flag
6	0	sleeping_flag
5	1	ready_flag
4	0	broken_flag
3	0	run_flag
2	0	break_flag
1	0	start_flag
0	0	reset_flag

Bit Range	Default & Access	Description
31:29	0h RW	**unused_stat_and_ctrl:** Unused
28:24	0h RW	**arb_cont_dmem_Arb_mem_wp_source1:** Arbiter contender group bandwidth for dmem_Arb_mem_wp_source1

Bit Range	Default & Access	Description
23:19	0h RW	**arb_cont_dmem_Arb_mem_wp_source0:** Arbiter contender group bandwidth for dmem_Arb_mem_wp_source0
18:14	0h RW	**arb_period_dmem_Arb_mem_wp:** Arbiter period for dmem_Arb_mem_wp
13	0h RW	**prefetch_enable_flag:** Prefetch enable flag for config_ilm_conf_ilm_icache
12	0h RW	**invalidate_cache_flag:** Invalidate cache flag for config_ilm_conf_ilm_icache
11	0h RW	**sleeping_irq_mask_flag:** Sleeping IRQ mask flag
10	0h RW	**ready_irq_mask_flag:** Ready IRQ mask flag
9	0h RW	**broken_irq_mask_flag:** Broken IRQ mask flag
8	0h RW	**irq_clear_flag:** IRQ clear flag
7	1h RO	**stalling_flag:** Stalling flag. Set to one when not executing an instruction.
6	0h RO	**sleeping_flag:** Sleeping flag
5	1h RO	**ready_flag:** Ready flag. Set to one when not executing a program.
4	0h RO	**broken_flag:** Broken flag
3	0h RW	**run_flag:** Run flag
2	0h RW	**break_flag:** Break flag
1	0h WO	**start_flag:** Start flag
0	0h WO	**reset_flag:** Reset flag

15.8.88 reg_scp_base_address_type (scp_base_address)—Offset 10004h

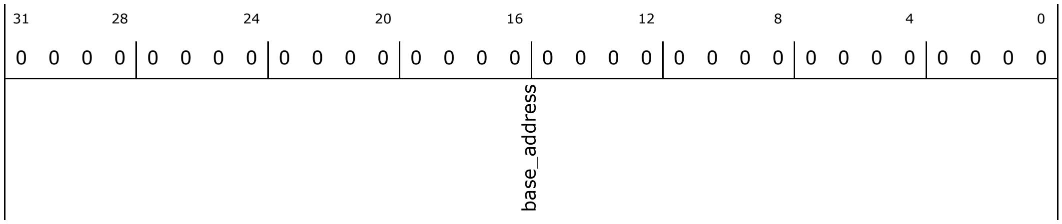
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_base_address: [ISPMMADR] + 10004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**base_address:** Start address

15.8.89 reg_scp_unused_2_type (scp_unused_2)—Offset 10008h

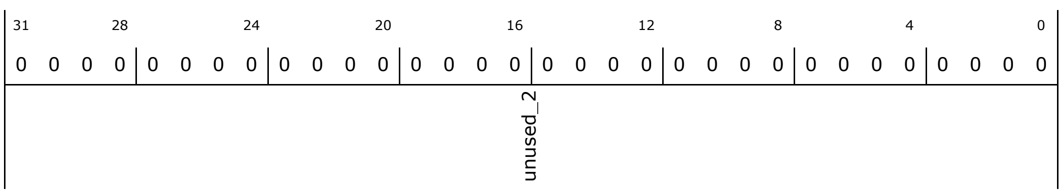
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_unused_2: [ISPMMADR] + 10008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**unused_2:** Unused

15.8.90 reg_scp_base_addr_seg_0_MI_xmem_master_int_type (scp_base_addr_seg_0_MI_xmem_master_int)—Offset 10010h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_base_addr_seg_0_MI_xmem_master_int: [ISPMMADR] + 10010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

base_addr_seg_0_MI_xmem_master_int

Bit Range	Default & Access	Description
31:0	0h RW	**base_addr_seg_0_MI_xmem_master_int:** Base address for segment 0 of master interface xmem_master_int

15.8.91 reg_scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master_type (scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master)—Offset 10014h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master: [ISPMMADR] + 10014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

base_addr_seg_0_MI_config_ilm_conf_ilm_master

Bit Range	Default & Access	Description
31:0	0h RW	**base_addr_seg_0_MI_config_ilm_conf_ilm_master:** Base address for segment 0 of master interface config_ilm_conf_ilm_master

15.8.92 reg_scp_unused_6_type (scp_unused_6)—Offset 10018h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_unused_6: [ISPMMADR] + 10018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_6

Bit Range	Default & Access	Description
31:0	0h RW	**unused_6:** Unused

15.8.93 reg_scp_unused_7_type (scp_unused_7)—Offset 1001Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_unused_7: [ISPMMADR] + 1001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_7

Bit Range	Default & Access	Description
31:0	0h RW	**unused_7:** Unused

15.8.94 reg_scp_debug_pc_type (scp_debug_pc)—Offset 10024h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_debug_pc: [ISPMMADR] + 10024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:0
Default	0000 0000 0000 0000 0000 0000 0000 0000
Field	debug_pc

Bit Range	Default & Access	Description
31:0	0h RO	**debug_pc:** Debug program counter

15.8.95 reg_scp_stall_stat_fifo_loc_mt_am_inst_0_op0_type (scp_stall_stat_fifo_loc_mt_am_inst_0_op0)—Offset 10028h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_stall_stat_fifo_loc_mt_am_inst_0_op0: [ISPMMADR] + 10028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31:15	0 0000 0000 0000 0000	unused_stall_stat_fifo_loc_mt_am_inst_0_op0
14	0	stall_stat_config_ilm_conf_ilm_iam_op1
13	0	stall_stat_config_ilm_conf_ilm_iam_op0
12	0	stall_stat_xmem_loc_mt_am_inst_2_op0
11	0	stall_stat_dmem_loc_mt_am_inst_1_op0
10	0	stall_stat_fifo_loc_mt_am_inst_0_op10
9	0	stall_stat_fifo_loc_mt_am_inst_0_op9
8	0	stall_stat_fifo_loc_mt_am_inst_0_op8
7	0	stall_stat_fifo_loc_mt_am_inst_0_op7
6	0	stall_stat_fifo_loc_mt_am_inst_0_op6
5	0	stall_stat_fifo_loc_mt_am_inst_0_op5
4	0	stall_stat_fifo_loc_mt_am_inst_0_op4
3	0	stall_stat_fifo_loc_mt_am_inst_0_op3
2	0	stall_stat_fifo_loc_mt_am_inst_0_op2
1	0	stall_stat_fifo_loc_mt_am_inst_0_op1
0	0	stall_stat_fifo_loc_mt_am_inst_0_op0

Bit Range	Default & Access	Description
31:15	0h RW	**unused_stall_stat_fifo_loc_mt_am_inst_0_op0:** Unused

Bit Range	Default & Access	Description
14	0h RO	**stall_stat_config_ilm_conf_ilm_iam_op1:** Stalling flag for msink config_ilm_conf_ilm_iam_op1
13	0h RO	**stall_stat_config_ilm_conf_ilm_iam_op0:** Stalling flag for msink config_ilm_conf_ilm_iam_op0
12	0h RO	**stall_stat_xmem_loc_mt_am_inst_2_op0:** Stalling flag for msink xmem_loc_mt_am_inst_2_op0
11	0h RO	**stall_stat_dmem_loc_mt_am_inst_1_op0:** Stalling flag for msink dmem_loc_mt_am_inst_1_op0
10	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op10:** Stalling flag for msink fifo_loc_mt_am_inst_0_op10
9	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op9:** Stalling flag for msink fifo_loc_mt_am_inst_0_op9
8	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op8:** Stalling flag for msink fifo_loc_mt_am_inst_0_op8
7	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op7:** Stalling flag for msink fifo_loc_mt_am_inst_0_op7
6	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op6:** Stalling flag for msink fifo_loc_mt_am_inst_0_op6
5	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op5:** Stalling flag for msink fifo_loc_mt_am_inst_0_op5
4	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op4:** Stalling flag for msink fifo_loc_mt_am_inst_0_op4
3	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op3:** Stalling flag for msink fifo_loc_mt_am_inst_0_op3
2	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op2:** Stalling flag for msink fifo_loc_mt_am_inst_0_op2
1	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op1:** Stalling flag for msink fifo_loc_mt_am_inst_0_op1
0	0h RO	**stall_stat_fifo_loc_mt_am_inst_0_op0:** Stalling flag for msink fifo_loc_mt_am_inst_0_op0

15.8.96 reg_scp_unused_11_type (scp_unused_11)—Offset 1002Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_unused_11: [ISPMMADR] + 1002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_11

Bit Range	Default & Access	Description
31:0	0h RW	**unused_11:** Unused

15.8.97 reg_scp_pmem_slave_access_type (scp_pmem_slave_access)—Offset 10030h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

scp_pmem_slave_access: [ISPMMADR] + 10030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

pmem_slave_access

Bit Range	Default & Access	Description
31:0	0h RW	**pmem_slave_access:** Pmem slave access flag

15.8.98 reg_isp_stat_and_ctrl_type (isp_stat_and_ctrl)—Offset 20000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_stat_and_ctrl: [ISPMMADR] + 20000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000A0h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 1 0	0 0 0 0

Bits 31:17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused_stat_and_ctrl	arb_cont_base_dmem_Arb_data_mem_wp0_source1	arb_cont_base_dmem_Arb_data_mem_wp0_source0	arb_period_base_dmem_Arb_data_mem_wp0	prefetch_enable_flag	invalidate_cache_flag	sleeping_irq_mask_flag	ready_irq_mask_flag	broken_irq_mask_flag	irq_clear_flag	stalling_flag	sleeping_flag	ready_flag	broken_flag	run_flag	break_flag	start_flag	reset_flag

Bit Range	Default & Access	Description
31:17	0h RW	**unused_stat_and_ctrl:** Unused
16	0h RW	**arb_cont_base_dmem_Arb_data_mem_wp0_source1:** Arbiter contender group bandwidth for base_dmem_Arb_data_mem_wp0_source1
15	0h RW	**arb_cont_base_dmem_Arb_data_mem_wp0_source0:** Arbiter contender group bandwidth for base_dmem_Arb_data_mem_wp0_source0
14	0h RW	**arb_period_base_dmem_Arb_data_mem_wp0:** Arbiter period for base_dmem_Arb_data_mem_wp0
13	0h RW	**prefetch_enable_flag:** Prefetch enable flag for base_config_mem_icache
12	0h RW	**invalidate_cache_flag:** Invalidate cache flag for base_config_mem_icache
11	0h RW	**sleeping_irq_mask_flag:** Sleeping IRQ mask flag
10	0h RW	**ready_irq_mask_flag:** Ready IRQ mask flag
9	0h RW	**broken_irq_mask_flag:** Broken IRQ mask flag
8	0h RW	**irq_clear_flag:** IRQ clear flag
7	1h RO	**stalling_flag:** Stalling flag. Set to one when not executing an instruction.
6	0h RO	**sleeping_flag:** Sleeping flag
5	1h RO	**ready_flag:** Ready flag. Set to one when not executing a program.

Bit Range	Default & Access	Description
4	0h RO	**broken_flag:** Broken flag
3	0h RW	**run_flag:** Run flag
2	0h RW	**break_flag:** Break flag
1	0h WO	**start_flag:** Start flag
0	0h WO	**reset_flag:** Reset flag

15.8.99 reg_isp_base_address_type (isp_base_address)—Offset 20004h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_base_address: [ISPMMADR] + 20004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

base_address

Bit Range	Default & Access	Description
31:0	0h RW	**base_address:** Start address

15.8.100 reg_isp_unused_2_type (isp_unused_2)—Offset 20008h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_unused_2: [ISPMMADR] + 20008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_2

Bit Range	Default & Access	Description
31:0	0h RW	**unused_2:** Unused

15.8.101 reg_isp_base_addr_seg_0_MI_base_config_mem_master_type (isp_base_addr_seg_0_MI_base_config_mem_master)—Offset 20010h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_base_addr_seg_0_MI_base_config_mem_master: [ISPMMADR] + 20010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

base_addr_seg_0_MI_base_config_mem_master

Bit Range	Default & Access	Description
31:0	0h RW	**base_addr_seg_0_MI_base_config_mem_master:** Base address for segment 0 of master interface base_config_mem_master

15.8.102 reg_isp_unused_5_type (isp_unused_5)—Offset 20014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_unused_5: [ISPMMADR] + 20014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_5																															

Bit Range	Default & Access	Description
31:0	0h RW	**unused_5:** Unused

15.8.103 reg_isp_debug_pc_type (isp_debug_pc)—Offset 2001Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_debug_pc: [ISPMMADR] + 2001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
debug_pc																															

Bit Range	Default & Access	Description
31:0	0h RO	**debug_pc:** Debug program counter

15.8.104 reg_isp_stall_stat_base_config_mem_iam_op0_type (isp_stall_stat_base_config_mem_iam_op0)—Offset 20020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_stall_stat_base_config_mem_iam_op0: [ISPMMADR] + 20020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	unused_stall_stat_base_config_mem_iam_op0	stall_stat_simd_histogram_loc_mt_am_inst_6_op0	stall_stat_simd_vamem3_loc_mt_am_inst_5_op0	stall_stat_simd_vamem2_loc_mt_am_inst_4_op0	stall_stat_simd_vamem1_loc_mt_am_inst_3_op0	stall_stat_simd_vmem_loc_mt_am_inst_2_op0	stall_stat_base_fifo_loc_mt_am_inst_1_op6	stall_stat_base_fifo_loc_mt_am_inst_1_op5	stall_stat_base_fifo_loc_mt_am_inst_1_op4	stall_stat_base_fifo_loc_mt_am_inst_1_op3	stall_stat_base_fifo_loc_mt_am_inst_1_op2	stall_stat_base_fifo_loc_mt_am_inst_1_op1	stall_stat_base_fifo_loc_mt_am_inst_1_op0	stall_stat_base_dmem_loc_mt_am_inst_0_op0	stall_stat_base_config_mem_iam_op1	stall_stat_base_config_mem_iam_op0

Bit Range	Default & Access	Description
31:15	0h RW	**unused_stall_stat_base_config_mem_iam_op0:** Unused
14	0h RO	**stall_stat_simd_histogram_loc_mt_am_inst_6_op0:** Stalling flag for msink simd_histogram_loc_mt_am_inst_6_op0
13	0h RO	**stall_stat_simd_vamem3_loc_mt_am_inst_5_op0:** Stalling flag for msink simd_vamem3_loc_mt_am_inst_5_op0
12	0h RO	**stall_stat_simd_vamem2_loc_mt_am_inst_4_op0:** Stalling flag for msink simd_vamem2_loc_mt_am_inst_4_op0
11	0h RO	**stall_stat_simd_vamem1_loc_mt_am_inst_3_op0:** Stalling flag for msink simd_vamem1_loc_mt_am_inst_3_op0
10	0h RO	**stall_stat_simd_vmem_loc_mt_am_inst_2_op0:** Stalling flag for msink simd_vmem_loc_mt_am_inst_2_op0
9	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op6:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op6
8	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op5:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op5
7	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op4:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op4
6	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op3:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op3
5	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op2:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op2
4	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op1:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op1
3	0h RO	**stall_stat_base_fifo_loc_mt_am_inst_1_op0:** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op0
2	0h RO	**stall_stat_base_dmem_loc_mt_am_inst_0_op0:** Stalling flag for msink base_dmem_loc_mt_am_inst_0_op0

Bit Range	Default & Access	Description
1	0h RO	**stall_stat_base_config_mem_iam_op1:** Stalling flag for msink base_config_mem_iam_op1
0	0h RO	**stall_stat_base_config_mem_iam_op0:** Stalling flag for msink base_config_mem_iam_op0

15.8.105 reg_isp_unused_9_type (isp_unused_9)—Offset 20024h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_unused_9: [ISPMMADR] + 20024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_9

Bit Range	Default & Access	Description
31:0	0h RW	**unused_9:** Unused

15.8.106 reg_isp_pmem_slave_access_type (isp_pmem_slave_access)—Offset 20028h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_pmem_slave_access: [ISPMMADR] + 20028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

pmem_slave_access

Bit Range	Default & Access	Description
31:0	0h RW	**pmem_slave_access:** Pmem slave access flag

15.8.107 reg_ifmt_ift_prim_IF_sw_rst_type (ifmt_ift_prim_IF_sw_rst)—Offset 30000h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_sw_rst: [ISPMMADR] + 30000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_sw_rst (bits 31:1), IF_sw_rst (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_sw_rst:** Unused
0	0h RW	**IF_sw_rst:** Software Reset

15.8.108 reg_ifmt_ift_prim_IF_start_line_type (ifmt_ift_prim_IF_start_line)—Offset 30004h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_start_line: [ISPMMADR] + 30004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_start_line (bits 31:16), IF_start_line (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_line:** Unused
15:0	0h RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

15.8.109 reg_ifmt_ift_prim_IF_start_column_type (ifmt_ift_prim_IF_start_column)—Offset 30008h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_start_column: [ISPMMADR] + 30008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_IF_start_column	IF_start_column

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_column:** Unused
15:0	0h RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

15.8.110 reg_ifmt_ift_prim_IF_Cropped_height_type (ifmt_ift_prim_IF_Cropped_height)—Offset 3000Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_Cropped_height: [ISPMMADR] + 3000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_Cropped_height	IF_Cropped_height

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_height:** Unused
15:0	0h RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

15.8.111 reg_ifmt_ift_prim_IF_Cropped_width_type (ifmt_ift_prim_IF_Cropped_width)—Offset 30010h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_Cropped_width: [ISPMMADR] + 30010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_Cropped_width	IF_Cropped_width

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_width:** Unused
15:0	0h RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

15.8.112 reg_ifmt_ift_prim_IF_Vert_Decim_type (ifmt_ift_prim_IF_Vert_Decim)—Offset 30014h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Vert_Decim: [ISPMMADR] + 30014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits 31:12	Bits 11:0
0000 0000 0000 0000 0000	0000 0000 0000
unused_IF_Vert_Decim	IF_Vert_Decim

Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Vert_Decim:** Unused
11:0	0h RW	**IF_Vert_Decim:** Vertical decimation factor

15.8.113 reg_ifmt_ift_prim_IF_Horiz_Decim_type (ifmt_ift_prim_IF_Horiz_Decim)—Offset 30018h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Horiz_Decim: [ISPMMADR] + 30018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits 31:12	Bits 11:0
0000 0000 0000 0000 0000	0000 0000 0000
unused_IF_Horiz_Decim	IF_Horiz_Decim

Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Horiz_Decim:** Unused
11:0	0h RW	**IF_Horiz_Decim:** Horizontal decimation factor

15.8.114 reg_ifmt_ift_prim_IF_Horiz_Deinter_type (ifmt_ift_prim_IF_Horiz_Deinter)—Offset 3001Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Horiz_Deinter: [ISPMMADR] + 3001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Horiz_Deinter | IF_Horiz_Deinter

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Horiz_Deinter:** Unused
2:0	0h RW	**IF_Horiz_Deinter:** Horizontal deinterleaving factor

15.8.115 reg_ifmt_ift_prim_IF_Left_Pad_type (ifmt_ift_prim_IF_Left_Pad)—Offset 30020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Left_Pad: [ISPMMADR] + 30020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Left_Pad (31:6)	IF_Left_Pad (5:0)

Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_Left_Pad:** Unused
5:0	0h RW	**IF_Left_Pad:** Left padding: pizel component to be padded at the beggining of each line

15.8.116 reg_ifmt_ift_prim_IF_EOF_Offset_type (ifmt_ift_prim_IF_EOF_Offset)—Offset 30024h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_EOF_Offset: [ISPMMADR] + 30024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_EOF_Offset (31:24)	IF_EOF_Offset (23:0)

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_EOF_Offset:** Unused
23:0	0h RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

15.8.117 reg_ifmt_ift_prim_IF_Start_addr_type (ifmt_ift_prim_IF_Start_addr)—Offset 30028h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_Start_addr: [ISPMMADR] + 30028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Start_addr (31:24), IF_Start_addr (23:0)

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_Start_addr:** Unused
23:0	0h RW	**IF_Start_addr:** Start address in bytes: memory buffer start address

15.8.118 reg_ifmt_ift_prim_IF_End_addr_type (ifmt_ift_prim_IF_End_addr)—Offset 3002Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_End_addr: [ISPMMADR] + 3002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_End_addr (31:24), IF_End_addr (23:0)

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_End_addr:** Unused
23:0	0h RW	**IF_End_addr:** End address in bytes: memory buffer end address

15.8.119 reg_ifmt_ift_prim_IF_incr_type (ifmt_ift_prim_IF_incr)—Offset 30030h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_incr: [ISPMMADR] + 30030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: unused_IF_incr (31:24), IF_incr (23:0)

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_incr:** Unused
23:0	0h RW	**IF_incr:** Word increment in memory word: word increment value after writting each word

15.8.120 reg_ifmt_ift_prim_IF_YUV_420_format_type (ifmt_ift_prim_IF_YUV_420_format)—Offset 30034h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_YUV_420_format: [ISPMMADR] + 30034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: unused_IF_YUV_420_format (31:1), IF_YUV_420_format (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_YUV_420_format:** Unused
0	0h RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

15.8.121 reg_ifmt_ift_prim_IF_Vsynch_active_low_type (ifmt_ift_prim_IF_Vsynch_active_low)—Offset 30038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Vsynch_active_low: [ISPMMADR] + 30038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31	28	24	20	16	12	8	4	0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bit Range	Field
31:1	unused_IF_Vsynch_active_low
0	IF_Vsynch_active_low

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Vsynch_active_low:** Unused
0	0h RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

15.8.122 reg_ifmt_ift_prim_IF_Hsynch_active_low_type (ifmt_ift_prim_IF_Hsynch_active_low)—Offset 3003Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Hsynch_active_low: [ISPMMADR] + 3003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Hsynch_active_low

IF_Hsynch_active_low

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Hsynch_active_low:** Unused
0	0h RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

15.8.123 reg_ifmt_ift_prim_IF_ReEnable_type (ifmt_ift_prim_IF_ReEnable)—Offset 30040h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_ReEnable: [ISPMMADR] + 30040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_ReEnable

IF_ReEnable

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_ReEnable:** Unused
0	0h RW	**IF_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

15.8.124 reg_ifmt_ift_prim_IF_block_input_type (ifmt_ift_prim_IF_block_input)—Offset 30044h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_block_input: [ISPMMADR] + 30044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_block_input

IF_block_input

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_block_input:** Unused
0	0h RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

15.8.125 reg_ifmt_ift_prim_IF_Vert_Deinter_type (ifmt_ift_prim_IF_Vert_Deinter)—Offset 30048h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_Vert_Deinter: [ISPMMADR] + 30048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Vert_Deinter

IF_Vert_Deinter

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Vert_Deinter:** Unused
2:0	0h RW	**IF_Vert_Deinter:** Vertical deinterleaving factor

15.8.126 reg_ifmt_ift_prim_IF_FSM_Sync_status_type (ifmt_ift_prim_IF_FSM_Sync_status)—Offset 30100h

FSM Sync status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Sync_status: [ISPMMADR] + 30100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_FSM_Sync_status (31:4), FSM_Sync_error (3), FSM_Sync_State (2:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Sync_status:** Unused
3	0h RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occured.
2:0	0h RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

15.8.127 reg_ifmt_ift_prim_FSM_Sync_counter_type (ifmt_ift_prim_FSM_Sync_counter)—Offset 30104h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Sync_counter: [ISPMMADR] + 30104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_FSM_Sync_counter (31:16), FSM_Sync_counter (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Sync_counter:** Unused
15:0	0h RO	**FSM_Sync_counter:** FSM Sync counter: counts the pixel components of the request being served (starting from value 1)

15.8.128 reg_ifmt_ift_prim_FSM_Crop_status_type (ifmt_ift_prim_FSM_Crop_status)—Offset 30108h

FSM Crop status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_FSM_Crop_status: [ISPMMADR] + 30108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_FSM_Crop_status (31:4), FSM_Crop_error (3), FSM_Crop_State (2:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_FSM_Crop_status:** Unused
3	0h RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected vsynch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occured.

Bit Range	Default & Access	Description
2:0	0h RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

15.8.129 reg_ifmt_ift_prim_FSM_Crop_line_counter_type (ifmt_ift_prim_FSM_Crop_line_counter)—Offset 3010Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Crop_line_counter: [ISPMMADR] + 3010Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_FSM_Crop_line_counter (bits 31:15); FSM_Crop_line_counter (bits 14:0)

Bit Range	Default & Access	Description
31:15	0h RW	**unused_FSM_Crop_line_counter:** Unused
14:0	0h RO	**FSM_Crop_line_counter:** FSM Crop line counter

15.8.130 reg_ifmt_ift_prim_FSM_Crop_pixel_counter_type (ifmt_ift_prim_FSM_Crop_pixel_counter)—Offset 30110h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Crop_pixel_counter: [ISPMMADR] + 30110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: unused_FSM_Crop_pixel_counter (31:16), FSM_Crop_pixel_counter (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Crop_pixel_counter:** Unused
15:0	0h RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

15.8.131 reg_ifmt_ift_prim_FSM_Deinterl_idx_buffer_type (ifmt_ift_prim_FSM_Deinterl_idx_buffer)—Offset 30114h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Deinterl_idx_buffer: [ISPMMADR] + 30114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: unused_FSM_Deinterl_idx_buffer (31:2), FSM_Deinterl_idx_buffer (1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Deinterl_idx_buffer:** Unused

Bit Range	Default & Access	Description
1:0	0h RO	**FSM_Deinterl_idx_buffer:** FSM Deinterleaving idx buffer

15.8.132 reg_ifmt_ift_prim_FSM_Horiz_Decim_cnt_type (ifmt_ift_prim_FSM_Horiz_Decim_cnt)—Offset 30118h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Horiz_Decim_cnt: [ISPMMADR] + 30118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:0
unused_FSM_Horiz_Decim_cnt	FSM_Horiz_Decim_cnt

Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Horiz_Decim_cnt:** Unused
11:0	0h RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

15.8.133 reg_ifmt_ift_prim_FSM_Vertic_Decim_cnt_type (ifmt_ift_prim_FSM_Vertic_Decim_cnt)—Offset 3011Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Vertic_Decim_cnt: [ISPMMADR] + 3011Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_FSM_Vertic_Decim_cnt																				FSM_Vertic_Decim_cnt											

Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Vertic_Decim_cnt:** Unused
11:0	0h RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

15.8.134 reg_ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt)—Offset 30120h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt: [ISPMMADR] + 30120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_FSM_Vertic_Block_Decim_cnt																														FSM_Vertic_Block_Decim_cnt	

Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Vertic_Block_Decim_cnt:** Unused

Bit Range	Default & Access	Description
1:0	0h RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

15.8.135 reg_ifmt_ift_prim_IF_FSM_Padding_status_type (ifmt_ift_prim_IF_FSM_Padding_status)—Offset 30124h

FSM Padding status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Padding_status: [ISPMMADR] + 30124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_FSM_Padding_status (31:4), FSM_Padding_error (3), FSM_Padding_State (2:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Padding_status:** Unused
3	0h RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occured.
2:0	0h RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

15.8.136 reg_ifmt_ift_prim_IF_FSM_Padding_elem_idx_type (ifmt_ift_prim_IF_FSM_Padding_elem_idx)—Offset 30128h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Padding_elem_idx: [ISPMMADR] + 30128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bits 5:0
unused_IF_FSM_Padding_elem_idx	IF_FSM_Padding_elem_idx

Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_FSM_Padding_elem_idx:** Unused
5:0	0h RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

15.8.137 reg_ifmt_ift_prim_IF_FSM_Vec_Sup_type (ifmt_ift_prim_IF_FSM_Vec_Sup)—Offset 3012Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_IF_FSM_Vec_Sup: [ISPMMADR] + 3012Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
unused_IF_FSM_Vec_Sup	IF_FSM_Vec_Sup

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup:** Unused
0	0h RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

15.8.138 reg_ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full)—Offset 30130h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full: [ISPMMADR] + 30130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_FSM_Vec_Sup_Buf_full (bits 31:3), IF_FSM_Vec_Sup_Buf_full (bits 2:0)

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_FSM_Vec_Sup_Buf_full:** Unused
2:0	0h RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

15.8.139 reg_ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept)—Offset 30134h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept: [ISPMMADR] + 30134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: unused_IF_FSM_Vec_Sup_rd_accept (31:1), IF_FSM_Vec_Sup_rd_accept (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup_rd_accept:** Unused
0	1h RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support fifo rd accept flag

15.8.140 reg_ifmt_ift_prim_IF_Pixel_Fifo_status_type (ifmt_ift_prim_IF_Pixel_Fifo_status)—Offset 30138h

Pixel Fifo status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_IF_Pixel_Fifo_status: [ISPMMADR] + 30138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: unused_IF_Pixel_Fifo_status (31:4), Pixel_Fifo_rd_valid (3), Pixel_Fifo_rd_accept (2), Pixel_Fifo_wr_valid (1), Pixel_Fifo_wr_accept (0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_Pixel_Fifo_status:** Unused

Bit Range	Default & Access	Description
3	0h RO	**Pixel_Fifo_rd_valid:** Fifo has an element to be read
2	0h RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0h RO	**Pixel_Fifo_wr_valid:** There is an element to write into the Fifo
0	1h RO	**Pixel_Fifo_wr_accept:** Fifo is not full(1), Fifo is Full(0)

15.8.141 reg_ifmt_ift_prim_b_IF_sw_rst_type (ifmt_ift_prim_b_IF_sw_rst)—Offset 30200h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_sw_rst: [ISPMMADR] + 30200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_sw_rst (bits 31:1), IF_sw_rst (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_sw_rst:** Unused
0	0h RW	**IF_sw_rst:** Software Reset

15.8.142 reg_ifmt_ift_prim_b_IF_start_line_type (ifmt_ift_prim_b_IF_start_line)—Offset 30204h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_start_line: [ISPMMADR] + 30204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 … 16	15 … 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
unused_IF_start_line	IF_start_line

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_line:** Unused
15:0	0h RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

15.8.143 reg_ifmt_ift_prim_b_IF_start_column_type (ifmt_ift_prim_b_IF_start_column)—Offset 30208h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_start_column: [ISPMMADR] + 30208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 … 16	15 … 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
unused_IF_start_column	IF_start_column

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_column:** Unused
15:0	0h RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

15.8.144 reg_ifmt_ift_prim_b_IF_Cropped_height_type (ifmt_ift_prim_b_IF_Cropped_height)—Offset 3020Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_Cropped_height: [ISPMMADR] + 3020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Cropped_height (bits 31:16); IF_Cropped_height (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_height:** Unused
15:0	0h RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

15.8.145 reg_ifmt_ift_prim_b_IF_Cropped_width_type (ifmt_ift_prim_b_IF_Cropped_width)—Offset 30210h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_Cropped_width: [ISPMMADR] + 30210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Cropped_width (bits 31:16); IF_Cropped_width (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_width:** Unused

Bit Range	Default & Access	Description
15:0	0h RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

15.8.146 reg_ifmt_ift_prim_b_IF_Vert_Decim_type (ifmt_ift_prim_b_IF_Vert_Decim)—Offset 30214h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_Vert_Decim: [ISPMMADR] + 30214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:0
unused_IF_Vert_Decim	IF_Vert_Decim

Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Vert_Decim:** Unused
11:0	0h RW	**IF_Vert_Decim:** Vertical decimation factor

15.8.147 reg_ifmt_ift_prim_b_IF_Horiz_Decim_type (ifmt_ift_prim_b_IF_Horiz_Decim)—Offset 30218h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_Horiz_Decim: [ISPMMADR] + 30218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:0
unused_IF_Horiz_Decim	IF_Horiz_Decim

Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Horiz_Decim:** Unused
11:0	0h RW	**IF_Horiz_Decim:** Horizontal decimation factor

15.8.148 reg_ifmt_ift_prim_b_IF_Horiz_Deinter_type (ifmt_ift_prim_b_IF_Horiz_Deinter)—Offset 3021Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_Horiz_Deinter: [ISPMMADR] + 3021Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:3	Bits 2:0
unused_IF_Horiz_Deinter	IF_Horiz_Deinter

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Horiz_Deinter:** Unused
2:0	0h RW	**IF_Horiz_Deinter:** Horizontal deinterleaving factor

15.8.149 reg_ifmt_ift_prim_b_IF_Left_Pad_type (ifmt_ift_prim_b_IF_Left_Pad)—Offset 30220h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_Left_Pad: [ISPMMADR] + 30220h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_Left_Pad (31:6), IF_Left_Pad (5:0)

Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_Left_Pad:** Unused
5:0	0h RW	**IF_Left_Pad:** Left padding: pizel component to be padded at the beggining of each line

15.8.150 reg_ifmt_ift_prim_b_IF_EOF_Offset_type (ifmt_ift_prim_b_IF_EOF_Offset)—Offset 30224h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_EOF_Offset: [ISPMMADR] + 30224h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_EOF_Offset (31:24), IF_EOF_Offset (23:0)

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_EOF_Offset:** Unused
23:0	0h RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

15.8.151 reg_ifmt_ift_prim_b_IF_Start_addr_type (ifmt_ift_prim_b_IF_Start_addr)—Offset 30228h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_Start_addr: [ISPMMADR] + 30228h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_Start_addr | IF_Start_addr

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_Start_addr:** Unused
23:0	0h RW	**IF_Start_addr:** Start address in bytes: memory buffer start address

15.8.152 reg_ifmt_ift_prim_b_IF_End_addr_type (ifmt_ift_prim_b_IF_End_addr)—Offset 3022Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_End_addr: [ISPMMADR] + 3022Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_End_addr | IF_End_addr

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_End_addr:** Unused
23:0	0h RW	**IF_End_addr:** End address in bytes: memory buffer end address

15.8.153 reg_ifmt_ift_prim_b_IF_incr_type (ifmt_ift_prim_b_IF_incr)—Offset 30230h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_incr: [ISPMMADR] + 30230h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_IF_incr								IF_incr																							

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_incr:** Unused
23:0	0h RW	**IF_incr:** Word increment in memory word: word increment value after writting each word

15.8.154 reg_ifmt_ift_prim_b_IF_YUV_420_format_type (ifmt_ift_prim_b_IF_YUV_420_format)—Offset 30234h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_YUV_420_format: [ISPMMADR] + 30234h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_YUV_420_format

IF_YUV_420_format

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_YUV_420_format:** Unused
0	0h RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

15.8.155 reg_ifmt_ift_prim_b_IF_Vsynch_active_low_type (ifmt_ift_prim_b_IF_Vsynch_active_low)—Offset 30238h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Vsynch_active_low: [ISPMMADR] + 30238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Vsynch_active_low

IF_Vsynch_active_low

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Vsynch_active_low:** Unused
0	0h RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

15.8.156 reg_ifmt_ift_prim_b_IF_Hsynch_active_low_type (ifmt_ift_prim_b_IF_Hsynch_active_low)—Offset 3023Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Hsynch_active_low: [ISPMMADR] + 3023Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_Hsynch_active_low (bits 31:1), IF_Hsynch_active_low (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Hsynch_active_low:** Unused
0	0h RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

15.8.157 reg_ifmt_ift_prim_b_IF_ReEnable_type (ifmt_ift_prim_b_IF_ReEnable)—Offset 30240h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_ReEnable: [ISPMMADR] + 30240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_ReEnable (bits 31:1), IF_ReEnable (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_ReEnable:** Unused
0	0h RW	**IF_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

15.8.158 reg_ifmt_ift_prim_b_IF_block_input_type (ifmt_ift_prim_b_IF_block_input)—Offset 30244h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_block_input: [ISPMMADR] + 30244h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_block_input (bits 31:1); IF_block_input (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_block_input:** Unused
0	0h RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

15.8.159 reg_ifmt_ift_prim_b_IF_Vert_Deinter_type (ifmt_ift_prim_b_IF_Vert_Deinter)—Offset 30248h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_IF_Vert_Deinter: [ISPMMADR] + 30248h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_Vert_Deinter | IF_Vert_Deinter

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Vert_Deinter:** Unused
2:0	0h RW	**IF_Vert_Deinter:** Vertical deinterleaving factor

15.8.160 reg_ifmt_ift_prim_b_IF_FSM_Sync_status_type (ifmt_ift_prim_b_IF_FSM_Sync_status)—Offset 30300h

FSM Sync status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Sync_status: [ISPMMADR] + 30300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_FSM_Sync_status | FSM_Sync_error | FSM_Sync_State

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Sync_status:** Unused
3	0h RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occured.

Bit Range	Default & Access	Description
2:0	0h RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

15.8.161 reg_ifmt_ift_prim_b_FSM_Sync_counter_type (ifmt_ift_prim_b_FSM_Sync_counter)—Offset 30304h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_FSM_Sync_counter: [ISPMMADR] + 30304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_FSM_Sync_counter	FSM_Sync_counter

Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Sync_counter:** Unused
15:0	0h RO	**FSM_Sync_counter:** FSM Sync counter: counts the pixel components of the request being served (starting from value 1)

15.8.162 reg_ifmt_ift_prim_b_FSM_Crop_status_type (ifmt_ift_prim_b_FSM_Crop_status)—Offset 30308h

FSM Crop status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_FSM_Crop_status: [ISPMMADR] + 30308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bit 3	Bits 2:0
unused_FSM_Crop_status	FSM_Crop_error	FSM_Crop_State

Bit Range	Default & Access	Description
31:4	0h RW	**unused_FSM_Crop_status:** Unused
3	0h RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected vsynch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occured.
2:0	0h RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

15.8.163 reg_ifmt_ift_prim_b_FSM_Crop_line_counter_type (ifmt_ift_prim_b_FSM_Crop_line_counter)—Offset 3030Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_prim_b_FSM_Crop_line_counter: [ISPMMADR] + 3030Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:15	Bits 14:0
unused_FSM_Crop_line_counter	FSM_Crop_line_counter

Bit Range	Default & Access	Description
31:15	0h RW	**unused_FSM_Crop_line_counter:** Unused

Bit Range	Default & Access	Description
14:0	0h RO	**FSM_Crop_line_counter:** FSM Crop line counter

15.8.164 reg_ifmt_ift_prim_b_FSM_Crop_pixel_counter_type (ifmt_ift_prim_b_FSM_Crop_pixel_counter)—Offset 30310h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Crop_pixel_counter: [ISPMMADR] + 30310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_FSM_Crop_pixel_counter																FSM_Crop_pixel_counter															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Crop_pixel_counter:** Unused
15:0	0h RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

15.8.165 reg_ifmt_ift_prim_b_FSM_Deinterl_idx_buffer_type (ifmt_ift_prim_b_FSM_Deinterl_idx_buffer)—Offset 30314h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Deinterl_idx_buffer: [ISPMMADR] + 30314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_FSM_Deinterl_idx_buffer

FSM_Deinterl_idx_buffer

Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Deinterl_idx_buffer:** Unused
1:0	0h RO	**FSM_Deinterl_idx_buffer:** FSM Deinterleaving idx buffer

15.8.166 reg_ifmt_ift_prim_b_FSM_Horiz_Decim_cnt_type (ifmt_ift_prim_b_FSM_Horiz_Decim_cnt)—Offset 30318h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Horiz_Decim_cnt: [ISPMMADR] + 30318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_FSM_Horiz_Decim_cnt

FSM_Horiz_Decim_cnt

Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Horiz_Decim_cnt:** Unused
11:0	0h RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

15.8.167 reg_ifmt_ift_prim_b_FSM_Vertic_Decim_cnt_type (ifmt_ift_prim_b_FSM_Vertic_Decim_cnt)—Offset 3031Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Vertic_Decim_cnt: [ISPMMADR] + 3031Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:12	11:0
0000 0000 0000 0000 0000	0000 0000 0000
unused_FSM_Vertic_Decim_cnt	FSM_Vertic_Decim_cnt

Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Vertic_Decim_cnt:** Unused
11:0	0h RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

15.8.168 reg_ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt)—Offset 30320h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt: [ISPMMADR] + 30320h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:2	unused_FSM_Vertic_Block_Decim_cnt
1:0	FSM_Vertic_Block_Decim_cnt

Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Vertic_Block_Decim_cnt:** Unused
1:0	0h RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

15.8.169 reg_ifmt_ift_prim_b_IF_FSM_Padding_status_type (ifmt_ift_prim_b_IF_FSM_Padding_status)—Offset 30324h

FSM Padding status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Padding_status: [ISPMMADR] + 30324h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:4	unused_IF_FSM_Padding_status
3	FSM_Padding_error
2:0	FSM_Padding_State

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Padding_status:** Unused
3	0h RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occured.
2:0	0h RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

15.8.170 reg_ifmt_ift_prim_b_IF_FSM_Padding_elem_idx_type (ifmt_ift_prim_b_IF_FSM_Padding_elem_idx)—Offset 30328h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Padding_elem_idx: [ISPMMADR] + 30328h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bits 5:0
unused_IF_FSM_Padding_elem_idx	IF_FSM_Padding_elem_idx

Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_FSM_Padding_elem_idx:** Unused
5:0	0h RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

15.8.171 reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup)—Offset 3032Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Vec_Sup: [ISPMMADR] + 3032Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_FSM_Vec_Sup

IF_FSM_Vec_Sup

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup:** Unused
0	0h RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

15.8.172 reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full)—Offset 30330h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full: [ISPMMADR] + 30330h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_FSM_Vec_Sup_Buf_full

IF_FSM_Vec_Sup_Buf_full

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_FSM_Vec_Sup_Buf_full:** Unused
2:0	0h RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

15.8.173 reg_ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept)—Offset 30334h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept: [ISPMMADR] + 30334h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: unused_IF_FSM_Vec_Sup_rd_accept (31:1), IF_FSM_Vec_Sup_rd_accept (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup_rd_accept:** Unused
0	1h RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support fifo rd accept flag

15.8.174 reg_ifmt_ift_prim_b_IF_Pixel_Fifo_status_type (ifmt_ift_prim_b_IF_Pixel_Fifo_status)—Offset 30338h

Pixel Fifo status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_prim_b_IF_Pixel_Fifo_status: [ISPMMADR] + 30338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: unused_IF_Pixel_Fifo_status (31:4), Pixel_Fifo_rd_valid (3), Pixel_Fifo_rd_accept (2), Pixel_Fifo_wr_valid (1), Pixel_Fifo_wr_accept (0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_Pixel_Fifo_status:** Unused
3	0h RO	**Pixel_Fifo_rd_valid:** Fifo has an element to be read
2	0h RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0h RO	**Pixel_Fifo_wr_valid:** There is an element to write into the Fifo
0	1h RO	**Pixel_Fifo_wr_accept:** Fifo is not full(1), Fifo is Full(0)

15.8.175 reg_ifmt_ift_sec_IF_sw_rst_type (ifmt_ift_sec_IF_sw_rst)—Offset 30400h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_sw_rst: [ISPMMADR] + 30400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_sw_rst (31:1), IF_sw_rst (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_sw_rst:** Unused

Bit Range	Default & Access	Description
0	0h RW	**IF_sw_rst:** Software Reset

15.8.176 reg_ifmt_ift_sec_IF_start_line_type (ifmt_ift_sec_IF_start_line)—Offset 30404h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_start_line: [ISPMMADR] + 30404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_IF_start_line																IF_start_line															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_line:** Unused
15:0	0h RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

15.8.177 reg_ifmt_ift_sec_IF_start_column_type (ifmt_ift_sec_IF_start_column)—Offset 30408h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_start_column: [ISPMMADR] + 30408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

unused_IF_start_column	IF_start_column

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_start_column:** Unused
15:0	0h RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

15.8.178 reg_ifmt_ift_sec_IF_Cropped_height_type (ifmt_ift_sec_IF_Cropped_height)—Offset 3040Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_Cropped_height: [ISPMMADR] + 3040Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

unused_IF_Cropped_height	IF_Cropped_height

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_height:** Unused
15:0	0h RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

15.8.179 reg_ifmt_ift_sec_IF_Cropped_width_type (ifmt_ift_sec_IF_Cropped_width)—Offset 30410h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_Cropped_width: [ISPMMADR] + 30410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:16: unused_IF_Cropped_width; Bits 15:0: IF_Cropped_width

Bit Range	Default & Access	Description
31:16	0h RW	**unused_IF_Cropped_width:** Unused
15:0	0h RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

15.8.180 reg_ifmt_ift_sec_IF_Vert_Decim_type (ifmt_ift_sec_IF_Vert_Decim)—Offset 30414h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_Vert_Decim: [ISPMMADR] + 30414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:12: unused_IF_Vert_Decim; Bits 11:0: IF_Vert_Decim

Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Vert_Decim:** Unused
11:0	0h RW	**IF_Vert_Decim:** Vertical decimation factor

15.8.181 reg_ifmt_ift_sec_IF_Horiz_Decim_type (ifmt_ift_sec_IF_Horiz_Decim)—Offset 30418h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Horiz_Decim: [ISPMMADR] + 30418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:0
unused_IF_Horiz_Decim	IF_Horiz_Decim

Bit Range	Default & Access	Description
31:12	0h RW	**unused_IF_Horiz_Decim:** Unused
11:0	0h RW	**IF_Horiz_Decim:** Horizontal decimation factor

15.8.182 reg_ifmt_ift_sec_IF_Horiz_Deinter_type (ifmt_ift_sec_IF_Horiz_Deinter)—Offset 3041Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Horiz_Deinter: [ISPMMADR] + 3041Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_Horiz_Deinter | IF_Horiz_Deinter

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Horiz_Deinter:** Unused
2:0	0h RW	**IF_Horiz_Deinter:** Horizontal deinterleaving factor

15.8.183 reg_ifmt_ift_sec_IF_Left_Pad_type (ifmt_ift_sec_IF_Left_Pad)—Offset 30420h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_Left_Pad: [ISPMMADR] + 30420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_Left_Pad | IF_Left_Pad

Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_Left_Pad:** Unused
5:0	0h RW	**IF_Left_Pad:** Left padding: pizel component to be padded at the beggining of each line

15.8.184 reg_ifmt_ift_sec_IF_EOF_Offset_type (ifmt_ift_sec_IF_EOF_Offset)—Offset 30424h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_EOF_Offset: [ISPMMADR] + 30424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_EOF_Offset	IF_EOF_Offset

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_EOF_Offset:** Unused
23:0	0h RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

15.8.185 reg_ifmt_ift_sec_IF_Start_addr_type (ifmt_ift_sec_IF_Start_addr)—Offset 30428h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_Start_addr: [ISPMMADR] + 30428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Start_addr	IF_Start_addr

Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_Start_addr:** Unused
23:0	0h RW	**IF_Start_addr:** Start address in bytes: memory buffer start address

15.8.186 reg_ifmt_ift_sec_IF_End_addr_type (ifmt_ift_sec_IF_End_addr)—Offset 3042Ch

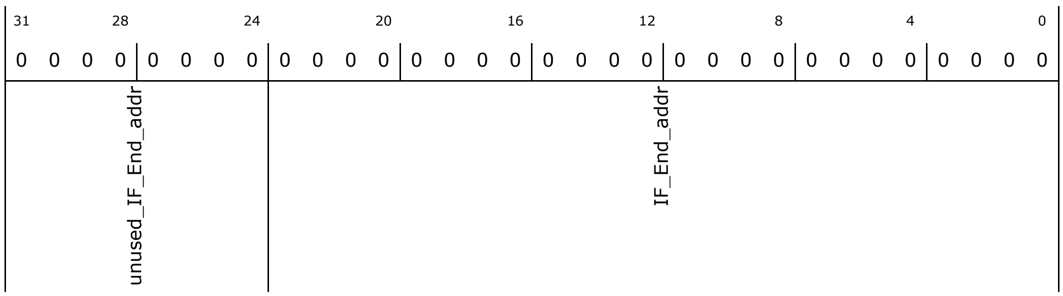
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_End_addr: [ISPMMADR] + 3042Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_End_addr:** Unused
23:0	0h RW	**IF_End_addr:** End address in bytes: memory buffer end address

15.8.187 reg_ifmt_ift_sec_IF_incr_type (ifmt_ift_sec_IF_incr)—Offset 30430h

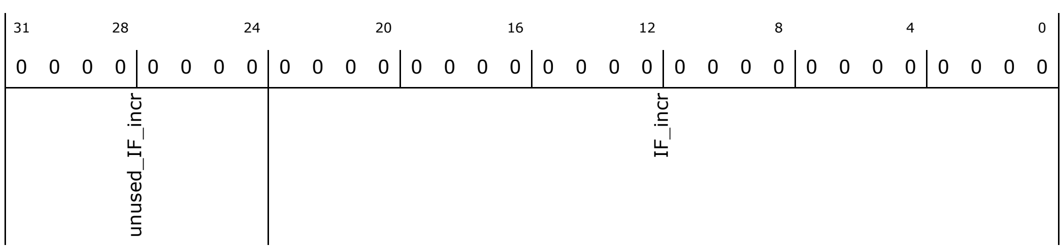
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_incr: [ISPMMADR] + 30430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**unused_IF_incr:** Unused

Bit Range	Default & Access	Description
23:0	0h RW	**IF_incr:** Word increment in memory word: word increment value after writting each word

15.8.188 reg_ifmt_ift_sec_IF_YUV_420_format_type (ifmt_ift_sec_IF_YUV_420_format)—Offset 30434h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_YUV_420_format: [ISPMMADR] + 30434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
unused_IF_YUV_420_format	IF_YUV_420_format

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_YUV_420_format:** Unused
0	0h RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

15.8.189 reg_ifmt_ift_sec_IF_Vsynch_active_low_type (ifmt_ift_sec_IF_Vsynch_active_low)—Offset 30438h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Vsynch_active_low: [ISPMMADR] + 30438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Vsynch_active_low

IF_Vsynch_active_low

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Vsynch_active_low:** Unused
0	0h RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

15.8.190 reg_ifmt_ift_sec_IF_Hsynch_active_low_type (ifmt_ift_sec_IF_Hsynch_active_low)—Offset 3043Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_Hsynch_active_low: [ISPMMADR] + 3043Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Hsynch_active_low

IF_Hsynch_active_low

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_Hsynch_active_low:** Unused
0	0h RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

15.8.191 reg_ifmt_ift_sec_IF_ReEnable_type (ifmt_ift_sec_IF_ReEnable)—Offset 30440h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_ReEnable: [ISPMMADR] + 30440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_ReEnable (31:1), IF_ReEnable (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_ReEnable:** Unused
0	0h RW	**IF_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

15.8.192 reg_ifmt_ift_sec_IF_block_input_type (ifmt_ift_sec_IF_block_input)—Offset 30444h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_block_input: [ISPMMADR] + 30444h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_block_input (31:1), IF_block_input (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_block_input:** Unused
0	0h RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

15.8.193 reg_ifmt_ift_sec_IF_Vert_Deinter_type (ifmt_ift_sec_IF_Vert_Deinter)—Offset 30448h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_Vert_Deinter: [ISPMMADR] + 30448h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_Vert_Deinter

IF_Vert_Deinter

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_Vert_Deinter:** Unused
2:0	0h RW	**IF_Vert_Deinter:** Vertical deinterleaving factor

15.8.194 reg_ifmt_ift_sec_IF_FSM_Sync_status_type (ifmt_ift_sec_IF_FSM_Sync_status)—Offset 30500h

FSM Sync status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Sync_status: [ISPMMADR] + 30500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IF_FSM_Sync_status | FSM_Sync_error | FSM_Sync_State

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Sync_status:** Unused
3	0h RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occured.
2:0	0h RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

15.8.195 reg_ifmt_ift_sec_FSM_Sync_counter_type (ifmt_ift_sec_FSM_Sync_counter)—Offset 30504h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Sync_counter: [ISPMMADR] + 30504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_FSM_Sync_counter | FSM_Sync_counter

Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Sync_counter:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**FSM_Sync_counter:** FSM Sync counter: counts the pixel components of the request being served (starting from value 1)

15.8.196 reg_ifmt_ift_sec_FSM_Crop_status_type (ifmt_ift_sec_FSM_Crop_status)—Offset 30508h

FSM Crop status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_FSM_Crop_status: [ISPMMADR] + 30508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bit 3	Bits 2:0
unused_FSM_Crop_status	FSM_Crop_error	FSM_Crop_State

Bit Range	Default & Access	Description
31:4	0h RW	**unused_FSM_Crop_status:** Unused
3	0h RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected vsynch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occured.
2:0	0h RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

15.8.197 reg_ifmt_ift_sec_FSM_Crop_line_counter_type (ifmt_ift_sec_FSM_Crop_line_counter)—Offset 3050Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_FSM_Crop_line_counter: [ISPMMADR] + 3050Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_FSM_Crop_line_counter (31:15), FSM_Crop_line_counter (14:0)

Bit Range	Default & Access	Description
31:15	0h RW	**unused_FSM_Crop_line_counter:** Unused
14:0	0h RO	**FSM_Crop_line_counter:** FSM Crop line counter

15.8.198 reg_ifmt_ift_sec_FSM_Crop_pixel_counter_type (ifmt_ift_sec_FSM_Crop_pixel_counter)—Offset 30510h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Crop_pixel_counter: [ISPMMADR] + 30510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_FSM_Crop_pixel_counter (31:16), FSM_Crop_pixel_counter (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_FSM_Crop_pixel_counter:** Unused
15:0	0h RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

15.8.199 reg_ifmt_ift_sec_FSM_Deinterl_idx_buffer_type (ifmt_ift_sec_FSM_Deinterl_idx_buffer)—Offset 30514h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Deinterl_idx_buffer: [ISPMMADR] + 30514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_FSM_Deinterl_idx_buffer (bits 31:2), FSM_Deinterl_idx_buffer (bits 1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Deinterl_idx_buffer:** Unused
1:0	0h RO	**FSM_Deinterl_idx_buffer:** FSM Deinterleaving idx buffer

15.8.200 reg_ifmt_ift_sec_FSM_Horiz_Decim_cnt_type (ifmt_ift_sec_FSM_Horiz_Decim_cnt)—Offset 30518h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Horiz_Decim_cnt: [ISPMMADR] + 30518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:12	11:0
unused_FSM_Horiz_Decim_cnt	FSM_Horiz_Decim_cnt

Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Horiz_Decim_cnt:** Unused
11:0	0h RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

15.8.201 reg_ifmt_ift_sec_FSM_Vertic_Decim_cnt_type (ifmt_ift_sec_FSM_Vertic_Decim_cnt)—Offset 3051Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_FSM_Vertic_Decim_cnt: [ISPMMADR] + 3051Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:12	11:0
unused_FSM_Vertic_Decim_cnt	FSM_Vertic_Decim_cnt

Bit Range	Default & Access	Description
31:12	0h RW	**unused_FSM_Vertic_Decim_cnt:** Unused
11:0	0h RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

15.8.202 reg_ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt_type (ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt)—Offset 30520h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt: [ISPMMADR] + 30520h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_FSM_Vertic_Block_Decim_cnt (bits 31:2), FSM_Vertic_Block_Decim_cnt (bits 1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_FSM_Vertic_Block_Decim_cnt:** Unused
1:0	0h RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

15.8.203 reg_ifmt_ift_sec_IF_FSM_Padding_status_type (ifmt_ift_sec_IF_FSM_Padding_status)—Offset 30524h

FSM Padding status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Padding_status: [ISPMMADR] + 30524h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_FSM_Padding_status (31:4), FSM_Padding_error (3), FSM_Padding_State (2:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_FSM_Padding_status:** Unused
3	0h RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occured.
2:0	0h RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

15.8.204 reg_ifmt_ift_sec_IF_FSM_Padding_elem_idx_type (ifmt_ift_sec_IF_FSM_Padding_elem_idx)—Offset 30528h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Padding_elem_idx: [ISPMMADR] + 30528h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_FSM_Padding_elem_idx (31:6), IF_FSM_Padding_elem_idx (5:0)

Bit Range	Default & Access	Description
31:6	0h RW	**unused_IF_FSM_Padding_elem_idx:** Unused
5:0	0h RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

15.8.205 reg_ifmt_ift_sec_IF_FSM_Vec_Sup_type (ifmt_ift_sec_IF_FSM_Vec_Sup)—Offset 3052Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Vec_Sup: [ISPMMADR] + 3052Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IF_FSM_Vec_Sup (31:1), IF_FSM_Vec_Sup (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup:** Unused
0	0h RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

15.8.206 reg_ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full_type (ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full)—Offset 30530h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full: [ISPMMADR] + 30530h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_IF_FSM_Vec_Sup_Buf_full | IF_FSM_Vec_Sup_Buf_full

Bit Range	Default & Access	Description
31:3	0h RW	**unused_IF_FSM_Vec_Sup_Buf_full:** Unused
2:0	0h RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

15.8.207 reg_ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept_type (ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept)—Offset 30534h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept: [ISPMMADR] + 30534h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

unused_IF_FSM_Vec_Sup_rd_accept | IF_FSM_Vec_Sup_rd_accept

Bit Range	Default & Access	Description
31:1	0h RW	**unused_IF_FSM_Vec_Sup_rd_accept:** Unused

Bit Range	Default & Access	Description
0	1h RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support fifo rd accept flag

15.8.208 reg_ifmt_ift_sec_IF_Pixel_Fifo_status_type (ifmt_ift_sec_IF_Pixel_Fifo_status)—Offset 30538h

Pixel Fifo status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_ift_sec_IF_Pixel_Fifo_status: [ISPMMADR] + 30538h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
unused_IF_Pixel_Fifo_status																												Pixel_Fifo_rd_valid	Pixel_Fifo_rd_accept	Pixel_Fifo_wr_valid	Pixel_Fifo_wr_accept

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IF_Pixel_Fifo_status:** Unused
3	0h RO	**Pixel_Fifo_rd_valid:** Fifo has an element to be read
2	0h RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0h RO	**Pixel_Fifo_wr_valid:** There is an element to write into the Fifo
0	1h RO	**Pixel_Fifo_wr_accept:** Fifo is not full(1), Fifo is Full(0)

15.8.209 reg_ifmt_mem_cpy_MemCopy_sw_rst_type (ifmt_mem_cpy_MemCopy_sw_rst)—Offset 30600h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_mem_cpy_MemCopy_sw_rst: [ISPMMADR] + 30600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MemCopy_sw_rst

MemCopy_sw_rst

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_sw_rst:** Unused
0	0h RW	**MemCopy_sw_rst:** Software Reset

15.8.210 reg_ifmt_mem_cpy_MemCopy_in_endian_type (ifmt_mem_cpy_MemCopy_in_endian)—Offset 30604h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_in_endian: [ISPMMADR] + 30604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MemCopy_in_endian

MemCopy_in_endian

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_in_endian:** Unused
0	0h RW	**MemCopy_in_endian:** Input endianness : set to 1 if input is big endian

15.8.211 reg_ifmt_mem_cpy_MemCopy_out_endian_type (ifmt_mem_cpy_MemCopy_out_endian)—Offset 30608h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_out_endian: [ISPMMADR] + 30608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Fields: unused_MemCopy_out_endian (bits 31:1), MemCopy_out_endian (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_out_endian:** Unused
0	0h RW	**MemCopy_out_endian:** Output endianness : set to 1 to deliver output input in big endian

15.8.212 reg_ifmt_mem_cpy_MemCopy_bit_swap_type (ifmt_mem_cpy_MemCopy_bit_swap)—Offset 3060Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_bit_swap: [ISPMMADR] + 3060Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MemCopy_bit_swap | MemCopy_bit_swap

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_bit_swap:** Unused
0	0h RW	**MemCopy_bit_swap:** Bit swapping : set to 1 to swap the bit of the incoming byte

15.8.213 reg_ifmt_mem_cpy_MemCopy_block_synch_type (ifmt_mem_cpy_MemCopy_block_synch)—Offset 30610h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_block_synch: [ISPMMADR] + 30610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MemCopy_block_synch | MemCopy_block_synch

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_block_synch:** Unused
0	0h RW	**MemCopy_block_synch:** Block synchronization pulse active low: set to 1 if start of block and end of block are active low

15.8.214 reg_ifmt_mem_cpy_MemCopy_packet_synch_type (ifmt_mem_cpy_MemCopy_packet_synch)—Offset 30614h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_packet_synch: [ISPMMADR] + 30614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_MemCopy_packet_synch																															MemCopy_packet_synch

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_packet_synch:** Unused
0	0h RW	**MemCopy_packet_synch:** Packet synchronization pulse active low: set to 1 if start of packet and end of packet are active low

15.8.215 reg_ifmt_mem_cpy_MemCopy_rd_post_wr_sync_type (ifmt_mem_cpy_MemCopy_rd_post_wr_sync)—Offset 30618h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_rd_post_wr_sync: [ISPMMADR] + 30618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MemCopy_rd_post_wr_sync

MemCopy_rd_post_wr_sync

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_rd_post_wr_sync:** Unused
0	0h RW	**MemCopy_rd_post_wr_sync:** Enable read post write synchronization: set to 1 to enable read post write check before sending acknowledge

15.8.216 reg_ifmt_mem_cpy_MemCopy_dual_input_type (ifmt_mem_cpy_MemCopy_dual_input)—Offset 3061Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_dual_input: [ISPMMADR] + 3061Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MemCopy_dual_input

MemCopy_dual_input

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_dual_input:** Unused

Bit Range	Default & Access	Description
0	0h RW	**MemCopy_dual_input:** Enable dual byte inputs: set to 1 to enable dual byte input

15.8.217 reg_ifmt_mem_cpy_MemCopy_ReEnable_type (ifmt_mem_cpy_MemCopy_ReEnable)—Offset 30620h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_ReEnable: [ISPMMADR] + 30620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_MemCopy_ReEnable (bits 31:1), MemCopy_ReEnable (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_ReEnable:** Unused
0	0h RW	**MemCopy_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

15.8.218 reg_ifmt_mem_cpy_MemCopy_token_data_type (ifmt_mem_cpy_MemCopy_token_data)—Offset 30700h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_token_data: [ISPMMADR] + 30700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MemCopy_token_data																															

Bit Range	Default & Access	Description
31:0	0h RO	**MemCopy_token_data:** Token data on command port

15.8.219 reg_ifmt_mem_cpy_MemCopy_FSM_Sync_status_type (ifmt_mem_cpy_MemCopy_FSM_Sync_status)—Offset 30704h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Sync_status: [ISPMMADR] + 30704h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_MemCopy_FSM_Sync_status																													MemCopy_FSM_Sync_status		

Bit Range	Default & Access	Description
31:3	0h RW	**unused_MemCopy_FSM_Sync_status:** Unused
2:0	0h RO	**MemCopy_FSM_Sync_status:** FSM Synchronization Status: 0)Idle -- 1)Request Blocks -- 2)Request Packets -- 3)Request Bytes -- 4)Send Acknowledge

15.8.220 reg_ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt)—Offset 30708h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt: [ISPMMADR] + 30708h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_MemCopy_FSM_Sync_bytes_cnt	MemCopy_FSM_Sync_bytes_cnt

Bit Range	Default & Access	Description
31:16	0h RW	**unused_MemCopy_FSM_Sync_bytes_cnt:** Unused
15:0	0h RO	**MemCopy_FSM_Sync_bytes_cnt:** FSM Synchronization bytes counter: counts the number of bytes received and packed

15.8.221 reg_ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt)—Offset 3070Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt: [ISPMMADR] + 3070Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_MemCopy_FSM_Sync_token_cnt

MemCopy_FSM_Sync_token_cnt

Bit Range	Default & Access	Description
31:16	0h RW	**unused_MemCopy_FSM_Sync_token_cnt:** Unused
15:0	0h RO	**MemCopy_FSM_Sync_token_cnt:** FSM Synchronization token amount: counts the number of token processed

15.8.222 reg_ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt)—Offset 30710h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt: [ISPMMADR] + 30710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_MemCopy_FSM_Pack_idx_cnt

MemCopy_FSM_Pack_idx_cnt

Bit Range	Default & Access	Description
31:2	0h RW	**unused_MemCopy_FSM_Pack_idx_cnt:** Unused
1:0	0h RO	**MemCopy_FSM_Pack_idx_cnt:** FSM Pack idx counter: element index

15.8.223 reg_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status_type (ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status)—Offset 30714h

Buffer Full and mask

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status: [ISPMMADR] + 30714h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:3	Bit 2	Bits 1:0
unused_MemCopy_FSM_Buf_Sup_status	field_mask	field_full

Bit Range	Default & Access	Description
31:3	0h RW	**unused_MemCopy_FSM_Buf_Sup_status:** Unused
2	0h RO	**field_mask:** FSM Buffer support mask buffers full to the FSM CioWr
1:0	0h RO	**field_full:** FSM Buffer support one-hot encoding flagging when the buffer are full

15.8.224 reg_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt_type (ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt)—Offset 30718h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt:** [ISPMMADR] + 30718h **ISPMMADR Type:** PCI Configuration Register (Size: 32 bits) **ISPMMADR Reference:** [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MemCopy_FSM_Buf_Sup_cnt (bits 31:1); MemCopy_FSM_Buf_Sup_cnt (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MemCopy_FSM_Buf_Sup_cnt:** Unused
0	0h RO	**MemCopy_FSM_Buf_Sup_cnt:** FSM Buffer support: counter for buffer index

15.8.225 reg_ifmt_mem_cpy_MemCopy_FSM_CioWr_status_type (ifmt_mem_cpy_MemCopy_FSM_CioWr_status)—Offset 3071Ch

FSM CioWr Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**ifmt_mem_cpy_MemCopy_FSM_CioWr_status:** [ISPMMADR] + 3071Ch **ISPMMADR Type:** PCI Configuration Register (Size: 32 bits) **ISPMMADR Reference:** [B:0, D:3, F:0] + 10h

Default: 00000004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Field
31:5	unused_MemCopy_FSM_CioWr_status
4	MemCopy_FSM_CioWr_state
3	MemCopy_FSM_CioWr_rvalid
2	MemCopy_FSM_CioWr_run
1	MemCopy_FSM_CioWr_we_n
0	MemCopy_FSM_CioWr_cs

Bit Range	Default & Access	Description
31:5	0h RW	**unused_MemCopy_FSM_CioWr_status:** Unused
4	0h RO	**MemCopy_FSM_CioWr_state:** 0)Idle - 1)Writing
3	0h RO	**MemCopy_FSM_CioWr_rvalid:** Read valid flag
2	1h RO	**MemCopy_FSM_CioWr_run:** Run flag
1	0h RO	**MemCopy_FSM_CioWr_we_n:** Write enable flag, active low
0	0h RO	**MemCopy_FSM_CioWr_cs:** CS flag

15.8.226 reg_ifmt_mem_cpy_MemCopy_FSM_CioWr_addr_type (ifmt_mem_cpy_MemCopy_FSM_CioWr_addr)—Offset 30720h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_mem_cpy_MemCopy_FSM_CioWr_addr: [ISPMMADR] + 30720h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MemCopy_FSM_CioWr_addr																															

Bit Range	Default & Access	Description
31:0	0h RO	**MemCopy_FSM_CioWr_addr:** FSM CioWr: write address in byte

15.8.227 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg0_type (ifmt_gp_reg_IFMT_input_switch_lut_reg0)—Offset 30800h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg0: [ISPMMADR] + 30800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IFMT_input_switch_lut_reg0																															

Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg0:** GP reg input switch data and hsync look-up table Register 0

15.8.228 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg1_type (ifmt_gp_reg_IFMT_input_switch_lut_reg1)—Offset 30804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg1: [ISPMMADR] + 30804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IFMT_input_switch_lut_reg1

Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg1:** GP reg input switch data and hsync look-up table Register 1

15.8.229 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg2_type (ifmt_gp_reg_IFMT_input_switch_lut_reg2)—Offset 30808h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg2: [ISPMMADR] + 30808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IFMT_input_switch_lut_reg2

Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg2:** GP reg input switch data and hsync look-up table Register 2

15.8.230 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg3_type (ifmt_gp_reg_IFMT_input_switch_lut_reg3)—Offset 3080Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg3: [ISPMMADR] + 3080Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:0: IFMT_input_switch_lut_reg3

Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg3:** GP reg input switch data and hsync look-up table Register 3

15.8.231 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg4_type (ifmt_gp_reg_IFMT_input_switch_lut_reg4)—Offset 30810h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg4: [ISPMMADR] + 30810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:0: IFMT_input_switch_lut_reg4

Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg4:** GP reg input switch data and hsync look-up table Register 4

15.8.232 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg5_type (ifmt_gp_reg_IFMT_input_switch_lut_reg5)—Offset 30814h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg5: [ISPMMADR] + 30814h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IFMT_input_switch_lut_reg5

Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg5:** GP reg input switch data and hsync look-up table Register 5

15.8.233 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg6_type (ifmt_gp_reg_IFMT_input_switch_lut_reg6)—Offset 30818h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg6: [ISPMMADR] + 30818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IFMT_input_switch_lut_reg6

Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg6:** GP reg input switch data and hsync look-up table Register 6

15.8.234 reg_ifmt_gp_reg_IFMT_input_switch_lut_reg7_type (ifmt_gp_reg_IFMT_input_switch_lut_reg7)—Offset 3081Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_lut_reg7: [ISPMMADR] + 3081Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IFMT_input_switch_lut_reg7

Bit Range	Default & Access	Description
31:0	0h RW	**IFMT_input_switch_lut_reg7:** GP reg input switch data and hsync look-up table Register 7

15.8.235 reg_ifmt_gp_reg_IFMT_input_switch_fsync_lut_type (ifmt_gp_reg_IFMT_input_switch_fsync_lut)—Offset 30820h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_fsync_lut: [ISPMMADR] + 30820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:0
unused_IFMT_input_switch_fsync_lut	IFMT_input_switch_fsync_lut

Bit Range	Default & Access	Description
31:12	0h RW	**unused_IFMT_input_switch_fsync_lut:** Unused
11:0	0h RW	**IFMT_input_switch_fsync_lut:** GP reg input switch frame synchronization signal look-up table register

15.8.236 reg_ifmt_gp_reg_IFMT_srst_type (ifmt_gp_reg_IFMT_srst)—Offset 30824h

GP reg soft reset

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_gp_reg_IFMT_srst: [ISPMMADR] + 30824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bit 3	Bit 2	Bit 1	Bit 0
unused_IFMT_srst	mem_cpy	sec_ift	prim_ift_b	prim_ift_a

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IFMT_srst:** Unused
3	0h RW	**mem_cpy:** Soft resets mem copy
2	0h RW	**sec_ift:** Soft resets secondary input formatter
1	0h RW	**prim_ift_b:** Soft resets primary input formatter B
0	0h RW	**prim_ift_a:** Soft resets primary input formatter A

15.8.237 reg_ifmt_gp_reg_IFMT_slv_reg_srst_type (ifmt_gp_reg_IFMT_slv_reg_srst)—Offset 30828h

GP reg slave register soft reset

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_slv_reg_srst: [ISPMMADR] + 30828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bit 3	Bit 2	Bit 1	Bit 0
unused_IFMT_slv_reg_srst	mem_cpy	sec_ift	prim_ift_b	prim_ift_a

Bit Range	Default & Access	Description
31:4	0h RW	**unused_IFMT_slv_reg_srst:** Unused
3	0h RW	**mem_cpy:** Soft resets slave registers of mem copy
2	0h RW	**sec_ift:** Soft resets slave registers of secondary input formatter
1	0h RW	**prim_ift_b:** Soft resets slave registers of primary input formatter B
0	0h RW	**prim_ift_a:** Soft resets slave registers of primary input formatter A

15.8.238 reg_ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type_type (ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type)—Offset 3082Ch

GP reg input switch status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type: [ISPMMADR] + 3082Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IFMT_input_switch_ch_id_fmt_type (31:7), ch_id (6:5), fmt_type (4:0)

Bit Range	Default & Access	Description
31:7	0h RW	**unused_IFMT_input_switch_ch_id_fmt_type:** Unused
6:5	0h RO	**ch_id:** Returns the channel id as it arrives at the input of the input switch
4:0	0h RO	**fmt_type:** Returns the format type as it arrives at the input of the input switch

15.8.239 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge)—Offset 30A00h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge: [ISPMMADR] + 30A00h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

31:5	4:0
unused_IFMT_IRQ_ctrl_edge	IFMT_IRQ_ctrl_edge

Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_edge:** Unused
4:0	0h RW	**IFMT_IRQ_ctrl_edge:** indicates for each irq bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

15.8.240 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask)—Offset 30A04h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask: [ISPMMADR] + 30A04h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

31:5	4:0
unused_IFMT_IRQ_ctrl_mask	IFMT_IRQ_ctrl_mask

Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_mask:** Unused
4:0	0h RW	**IFMT_IRQ_ctrl_mask:** indicates for each irq bit whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

15.8.241 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_status_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_status)—Offset 30A08h

IRQ controller STATUS

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_status: [ISPMMADR] + 30A08h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_IFMT_IRQ_ctrl_status (31:5), sb_changed_irq_stat (4), memcpy_irq_stat (3), ift_sec_irq_stat (2), ift_prim_b_irq_stat (1), ift_prim_irq_stat (0)

Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_status:** Unused
4	0h RO	**sb_changed_irq_stat:** Returns the status of the irq signal indicating a change in either the channel id or the format type
3	0h RO	**memcpy_irq_stat:** Returns the status of the irq generated by the stream to memory device
2	0h RO	**ift_sec_irq_stat:** Returns the status of the irq generated by the secondary input formatter
1	0h RO	**ift_prim_b_irq_stat:** Returns the status of the irq generated by the primary input formatter b
0	0h RO	**ift_prim_irq_stat:** Returns the status of the irq generated by the primary input formatter

15.8.242 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear)—Offset 30A0Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear: [ISPMMADR] + 30A0Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IFMT_IRQ_ctrl_clear | IFMT_IRQ_ctrl_clear

Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_clear:** Unused
4:0	0h WO	**IFMT_IRQ_ctrl_clear:** Clears (set to '0') bits in IFMT_IRQ_ctrl_status. When writing a '1' into a bit of this register, the corresponding bit in the IFMT_IRQ_ctrl_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the IFMT_IRQ_ctrl_status is not affected.

15.8.243 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable)—Offset 30A10h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable: [ISPMMADR] + 30A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_IFMT_IRQ_ctrl_enable | IFMT_IRQ_ctrl_enable

Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_enable:** Unused
4:0	0h RW	**IFMT_IRQ_ctrl_enable:** Indicates for each bit whether an interrupt cause as monitored by the IFMT_IRQ_ctrl_status register also affects the IRQ pin (value='1') or not (value='0')

15.8.244 reg_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse_type (ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse)—Offset 30A14h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse: [ISPMMADR] + 30A14h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:5: unused_IFMT_IRQ_ctrl_edge_pulse
Bits 4:0: IFMT_IRQ_ctrl_edge_pulse

Bit Range	Default & Access	Description
31:5	0h RW	**unused_IFMT_IRQ_ctrl_edge_pulse:** Unused
4:0	0h RW	**IFMT_IRQ_ctrl_edge_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

15.8.245 reg_isp_dma_DMA_FSM_Command_type (isp_dma_DMA_FSM_Command)—Offset 40000h

FSM Command: Last command and State

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Command: [ISPMMADR] + 40000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 31:16: Error_state
Bits 15:4: RSVD0
Bit 3: Error_flag
Bit 2: Stall__flag
Bit 1: Run_flag
Bit 0: Idle_flag

Bit Range	Default & Access	Description
31:16	0h RO	**Error_state:** Lower 16 bits of the last command received and processed
15:4	0b RO	**RSVD0:** Reserved
3	0h RO	**Error_flag:** Error flag
2	0h RO	**Stall__flag:** Stall flag
1	0h RO	**Run_flag:** Run flag
0	1h RO	**Idle_flag:** Idle flag

15.8.246 reg_isp_dma_DMA_CH0_Packing_setup_type (isp_dma_DMA_CH0_Packing_setup)—Offset 41000h

DMA CH 0 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH0_Packing_setup: [ISPMMADR] + 41000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:5	Bit 4	Bits 3:2	Bits 1:0
unused_DMA_CH0_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH0_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
1:0	0h RO	**conn_id:** Connection ID

15.8.247 reg_isp_dma_DMA_CH1_Packing_setup_type (isp_dma_DMA_CH1_Packing_setup)—Offset 41004h

DMA CH 1 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH1_Packing_setup: [ISPMMADR] + 41004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH1_Packing_setup (31:5), extend (4), RSVD0 (3:2), conn_id (1:0)

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH1_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.248 reg_isp_dma_DMA_CH2_Packing_setup_type (isp_dma_DMA_CH2_Packing_setup)—Offset 41008h

DMA CH 2 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH2_Packing_setup: [ISPMMADR] + 41008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:5	4	3:2	1:0
unused_DMA_CH2_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH2_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.249 reg_isp_dma_DMA_CH3_Packing_setup_type (isp_dma_DMA_CH3_Packing_setup)—Offset 4100Ch

DMA CH 3 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH3_Packing_setup: [ISPMMADR] + 4100Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31–5	4	3:2	1:0
unused_DMA_CH3_Packing_setup	extend	RSVD0	conn_id
000000000000000000000000000	0	00	00

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH3_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.250 reg_isp_dma_DMA_CH4_Packing_setup_type (isp_dma_DMA_CH4_Packing_setup)—Offset 41010h

DMA CH 4 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH4_Packing_setup: [ISPMMADR] + 41010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31–5	4	3:2	1:0
unused_DMA_CH4_Packing_setup	extend	RSVD0	conn_id
000000000000000000000000000	0	00	00

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH4_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.251 reg_isp_dma_DMA_CH5_Packing_setup_type (isp_dma_DMA_CH5_Packing_setup)—Offset 41014h

DMA CH 5 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH5_Packing_setup: [ISPMMADR] + 41014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH5_Packing_setup																											extend	RSVD0		conn_id	

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH5_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.252 reg_isp_dma_DMA_CH6_Packing_setup_type (isp_dma_DMA_CH6_Packing_setup)—Offset 41018h

DMA CH 6 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_Packing_setup: [ISPMMADR] + 41018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH6_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH6_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.253 reg_isp_dma_DMA_CH7_Packing_setup_type (isp_dma_DMA_CH7_Packing_setup)—Offset 4101Ch

DMA CH 7 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_Packing_setup: [ISPMMADR] + 4101Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH7_Packing_setup																											extend	RSVD0		conn_id	

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH7_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.254 reg_isp_dma_DMA_CH8_Packing_setup_type (isp_dma_DMA_CH8_Packing_setup)—Offset 41020h

DMA CH 8 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH8_Packing_setup: [ISPMMADR] + 41020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH8_Packing_setup																											extend	RSVD0		conn_id	

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH8_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.255 reg_isp_dma_DMA_CH9_Packing_setup_type (isp_dma_DMA_CH9_Packing_setup)—Offset 41024h

DMA CH 9 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH9_Packing_setup: [ISPMMADR] + 41024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:5	Bit 4	Bits 3:2	Bits 1:0
unused_DMA_CH9_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH9_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.256 reg_isp_dma_DMA_CH10_Packing_setup_type (isp_dma_DMA_CH10_Packing_setup)—Offset 41028h

DMA CH 10 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH10_Packing_setup: [ISPMMADR] + 41028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:5	Bit 4	Bits 3:2	Bits 1:0
unused_DMA_CH10_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH10_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.257 reg_isp_dma_DMA_CH11_Packing_setup_type (isp_dma_DMA_CH11_Packing_setup)—Offset 4102Ch

DMA CH 11 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH11_Packing_setup: [ISPMMADR] + 4102Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

31:5	4	3:2	1:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0
unused_DMA_CH11_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH11_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.258 reg_isp_dma_DMA_CH12_Packing_setup_type (isp_dma_DMA_CH12_Packing_setup)—Offset 41030h

DMA CH 12 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH12_Packing_setup: [ISPMMADR] + 41030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

31:5	4	3:2	1:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0
unused_DMA_CH12_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH12_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.259 reg_isp_dma_DMA_CH13_Packing_setup_type (isp_dma_DMA_CH13_Packing_setup)—Offset 41034h

DMA CH 13 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH13_Packing_setup: [ISPMMADR] + 41034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:5	4	3:2	1:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0
Field	unused_DMA_CH13_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH13_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.260 reg_isp_dma_DMA_CH14_Packing_setup_type (isp_dma_DMA_CH14_Packing_setup)—Offset 41038h

DMA CH 14 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_Packing_setup: [ISPMMADR] + 41038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH14_Packing_setup	extend	RSVDO	conn_id
31:5	4	3:2	1:0

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH14_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.261 reg_isp_dma_DMA_CH15_Packing_setup_type (isp_dma_DMA_CH15_Packing_setup)—Offset 4103Ch

DMA CH 15 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_Packing_setup: [ISPMMADR] + 4103Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

unused_DMA_CH15_Packing_setup | extend | RSVD0 | conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH15_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.262 reg_isp_dma_DMA_CH16_Packing_setup_type (isp_dma_DMA_CH16_Packing_setup)—Offset 41040h

DMA CH 16 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_Packing_setup: [ISPMMADR] + 41040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

unused_DMA_CH16_Packing_setup | extend | RSVD0 | conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH16_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.263 reg_isp_dma_DMA_CH17_Packing_setup_type (isp_dma_DMA_CH17_Packing_setup)—Offset 41044h

DMA CH 17 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH17_Packing_setup: [ISPMMADR] + 41044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:5	Bit 4	Bits 3:2	Bits 1:0
unused_DMA_CH17_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH17_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.264 reg_isp_dma_DMA_CH18_Packing_setup_type (isp_dma_DMA_CH18_Packing_setup)—Offset 41048h

DMA CH 18 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_Packing_setup: [ISPMMADR] + 41048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:5	Bit 4	Bits 3:2	Bits 1:0
unused_DMA_CH18_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH18_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.265 reg_isp_dma_DMA_CH19_Packing_setup_type (isp_dma_DMA_CH19_Packing_setup)—Offset 4104Ch

DMA CH 19 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_Packing_setup: [ISPMMADR] + 4104Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH19_Packing_setup																											extend	RSVD0		conn_id	

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH19_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.266 reg_isp_dma_DMA_CH20_Packing_setup_type (isp_dma_DMA_CH20_Packing_setup)—Offset 41050h

DMA CH 20 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_Packing_setup: [ISPMMADR] + 41050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH20_Packing_setup																											extend	RSVD0		conn_id	

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH20_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.267 reg_isp_dma_DMA_CH21_Packing_setup_type (isp_dma_DMA_CH21_Packing_setup)—Offset 41054h

DMA CH 21 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_Packing_setup: [ISPMMADR] + 41054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:5	Bit 4	Bits 3:2	Bits 1:0
unused_DMA_CH21_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH21_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.268 reg_isp_dma_DMA_CH22_Packing_setup_type (isp_dma_DMA_CH22_Packing_setup)—Offset 41058h

DMA CH 22 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_Packing_setup: [ISPMMADR] + 41058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:5	4	3:2	1:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0
unused_DMA_CH22_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH22_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.269 reg_isp_dma_DMA_CH23_Packing_setup_type (isp_dma_DMA_CH23_Packing_setup)—Offset 4105Ch

DMA CH 23 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_Packing_setup: [ISPMMADR] + 4105Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH23_Packing_setup																											extend	RSVD0		conn_id	

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH23_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.270 reg_isp_dma_DMA_CH24_Packing_setup_type (isp_dma_DMA_CH24_Packing_setup)—Offset 41060h

DMA CH 24 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_Packing_setup: [ISPMMADR] + 41060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH24_Packing_setup																											extend	RSVD0		conn_id	

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH24_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.271 reg_isp_dma_DMA_CH25_Packing_setup_type (isp_dma_DMA_CH25_Packing_setup)—Offset 41064h

DMA CH 25 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH25_Packing_setup: [ISPMMADR] + 41064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH25_Packing_setup | extend | RSVD0 | conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH25_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.272 reg_isp_dma_DMA_CH26_Packing_setup_type (isp_dma_DMA_CH26_Packing_setup)—Offset 41068h

DMA CH 26 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_Packing_setup: [ISPMMADR] + 41068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH26_Packing_setup, extend, RSVD0, conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH26_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.273 reg_isp_dma_DMA_CH28_Packing_setup_type (isp_dma_DMA_CH28_Packing_setup)—Offset 41070h

DMA CH 28 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_Packing_setup: [ISPMMADR] + 41070h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:5	4	3:2	1:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0
unused_DMA_CH28_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH28_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.274 reg_isp_dma_DMA_CH29_Packing_setup_type (isp_dma_DMA_CH29_Packing_setup)—Offset 41074h

DMA CH 29 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_Packing_setup: [ISPMMADR] + 41074h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:5	4	3:2	1:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0
unused_DMA_CH29_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH29_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.275 reg_isp_dma_DMA_CH30_Packing_setup_type (isp_dma_DMA_CH30_Packing_setup)—Offset 41078h

DMA CH 30 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH30_Packing_setup: [ISPMMADR] + 41078h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH30_Packing_setup																											extend	RSVD0		conn_id	

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH30_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.276 reg_isp_dma_DMA_CH31_Packing_setup_type (isp_dma_DMA_CH31_Packing_setup)—Offset 4107Ch

DMA CH 31 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_Packing_setup: [ISPMMADR] + 4107Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:5	4	3:2	1:0
Default	000000000000000000000000000	0	00	00
Field	unused_DMA_CH31_Packing_setup	extend	RSVD0	conn_id

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH31_Packing_setup:** Unused
4	0h RO	**extend:** Zero(0)/Sign(1) extension
3:2	0b RO	**RSVD0:** Reserved
1:0	0h RO	**conn_id:** Connection ID

15.8.277 reg_isp_dma_DMA_CH0_dev_stride_A_type (isp_dma_DMA_CH0_dev_stride_A)—Offset 41100h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_dev_stride_A: [ISPMMADR] + 41100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DMA_CH0_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH0_dev_stride_A:** DMA CH 0 PARAM 1: Device A stride

15.8.278 reg_isp_dma_DMA_CH1_dev_stride_A_type (isp_dma_DMA_CH1_dev_stride_A)—Offset 41104h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_dev_stride_A: [ISPMMADR] + 41104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DMA_CH1_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH1_dev_stride_A:** DMA CH 1 PARAM 1: Device A stride

15.8.279 reg_isp_dma_DMA_CH2_dev_stride_A_type (isp_dma_DMA_CH2_dev_stride_A)—Offset 41108h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_dev_stride_A: [ISPMMADR] + 41108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH2_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH2_dev_stride_A:** DMA CH 2 PARAM 1: Device A stride

15.8.280 reg_isp_dma_DMA_CH3_dev_stride_A_type (isp_dma_DMA_CH3_dev_stride_A)—Offset 4110Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH3_dev_stride_A: [ISPMMADR] + 4110Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH3_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH3_dev_stride_A:** DMA CH 3 PARAM 1: Device A stride

15.8.281 reg_isp_dma_DMA_CH4_dev_stride_A_type (isp_dma_DMA_CH4_dev_stride_A)—Offset 41110h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH4_dev_stride_A: [ISPMMADR] + 41110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH4_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH4_dev_stride_A:** DMA CH 4 PARAM 1: Device A stride

15.8.282 reg_isp_dma_DMA_CH5_dev_stride_A_type (isp_dma_DMA_CH5_dev_stride_A)—Offset 41114h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_dev_stride_A: [ISPMMADR] + 41114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH5_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH5_dev_stride_A:** DMA CH 5 PARAM 1: Device A stride

15.8.283 reg_isp_dma_DMA_CH6_dev_stride_A_type (isp_dma_DMA_CH6_dev_stride_A)—Offset 41118h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_dev_stride_A: [ISPMMADR] + 41118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH6_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH6_dev_stride_A:** DMA CH 6 PARAM 1: Device A stride

15.8.284 reg_isp_dma_DMA_CH7_dev_stride_A_type (isp_dma_DMA_CH7_dev_stride_A)—Offset 4111Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH7_dev_stride_A: [ISPMMADR] + 4111Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH7_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH7_dev_stride_A:** DMA CH 7 PARAM 1: Device A stride

15.8.285 reg_isp_dma_DMA_CH8_dev_stride_A_type (isp_dma_DMA_CH8_dev_stride_A)—Offset 41120h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH8_dev_stride_A: [ISPMMADR] + 41120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH8_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH8_dev_stride_A:** DMA CH 8 PARAM 1: Device A stride

15.8.286 reg_isp_dma_DMA_CH9_dev_stride_A_type (isp_dma_DMA_CH9_dev_stride_A)—Offset 41124h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_dev_stride_A: [ISPMMADR] + 41124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH9_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH9_dev_stride_A:** DMA CH 9 PARAM 1: Device A stride

15.8.287 reg_isp_dma_DMA_CH10_dev_stride_A_type (isp_dma_DMA_CH10_dev_stride_A)—Offset 41128h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_dev_stride_A: [ISPMMADR] + 41128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH10_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH10_dev_stride_A:** DMA CH 10 PARAM 1: Device A stride

15.8.288 reg_isp_dma_DMA_CH11_dev_stride_A_type (isp_dma_DMA_CH11_dev_stride_A)—Offset 4112Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_dev_stride_A: [ISPMMADR] + 4112Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH11_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH11_dev_stride_A:** DMA CH 11 PARAM 1: Device A stride

15.8.289 reg_isp_dma_DMA_CH12_dev_stride_A_type (isp_dma_DMA_CH12_dev_stride_A)—Offset 41130h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH12_dev_stride_A: [ISPMMADR] + 41130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH12_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH12_dev_stride_A:** DMA CH 12 PARAM 1: Device A stride

15.8.290 reg_isp_dma_DMA_CH13_dev_stride_A_type (isp_dma_DMA_CH13_dev_stride_A)—Offset 41134h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH13_dev_stride_A: [ISPMMADR] + 41134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH13_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH13_dev_stride_A:** DMA CH 13 PARAM 1: Device A stride

15.8.291 reg_isp_dma_DMA_CH14_dev_stride_A_type (isp_dma_DMA_CH14_dev_stride_A)—Offset 41138h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_dev_stride_A: [ISPMMADR] + 41138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH14_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH14_dev_stride_A:** DMA CH 14 PARAM 1: Device A stride

15.8.292 reg_isp_dma_DMA_CH15_dev_stride_A_type (isp_dma_DMA_CH15_dev_stride_A)—Offset 4113Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_dev_stride_A: [ISPMMADR] + 4113Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH15_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH15_dev_stride_A:** DMA CH 15 PARAM 1: Device A stride

15.8.293 reg_isp_dma_DMA_CH16_dev_stride_A_type (isp_dma_DMA_CH16_dev_stride_A)—Offset 41140h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_dev_stride_A: [ISPMMADR] + 41140h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH16_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH16_dev_stride_A:** DMA CH 16 PARAM 1: Device A stride

15.8.294 reg_isp_dma_DMA_CH17_dev_stride_A_type (isp_dma_DMA_CH17_dev_stride_A)—Offset 41144h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_dev_stride_A: [ISPMMADR] + 41144h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH17_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH17_dev_stride_A:** DMA CH 17 PARAM 1: Device A stride

15.8.295 reg_isp_dma_DMA_CH18_dev_stride_A_type (isp_dma_DMA_CH18_dev_stride_A)—Offset 41148h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH18_dev_stride_A: [ISPMMADR] + 41148h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH18_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH18_dev_stride_A:** DMA CH 18 PARAM 1: Device A stride

15.8.296 reg_isp_dma_DMA_CH19_dev_stride_A_type (isp_dma_DMA_CH19_dev_stride_A)—Offset 4114Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH19_dev_stride_A: [ISPMMADR] + 4114Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH19_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH19_dev_stride_A:** DMA CH 19 PARAM 1: Device A stride

15.8.297 reg_isp_dma_DMA_CH20_dev_stride_A_type (isp_dma_DMA_CH20_dev_stride_A)—Offset 41150h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH20_dev_stride_A: [ISPMMADR] + 41150h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH20_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH20_dev_stride_A:** DMA CH 20 PARAM 1: Device A stride

15.8.298 reg_isp_dma_DMA_CH21_dev_stride_A_type (isp_dma_DMA_CH21_dev_stride_A)—Offset 41154h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_dev_stride_A: [ISPMMADR] + 41154h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH21_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH21_dev_stride_A:** DMA CH 21 PARAM 1: Device A stride

15.8.299 reg_isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 41200h

DMA CH 0 PARAM 2: Device A Packing LSE cropping/Elements

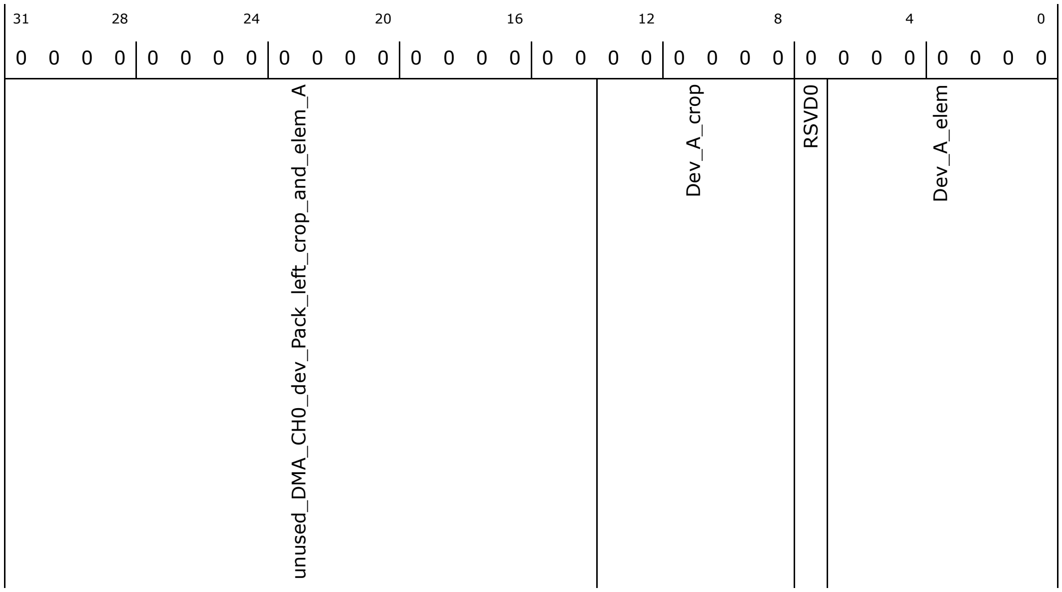
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH0_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.300 reg_isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A)—Offset 41204h

DMA CH 1 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_A:
[ISPMMADR] + 41204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH1_dev_Pack_left_crop_and_elem_A																		Dev_A_crop						RSVD0	Dev_A_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH1_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.301 reg_isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A)—Offset 41208h

DMA CH 2 PARAM 2: Device A Packing LSE cropping/Elements

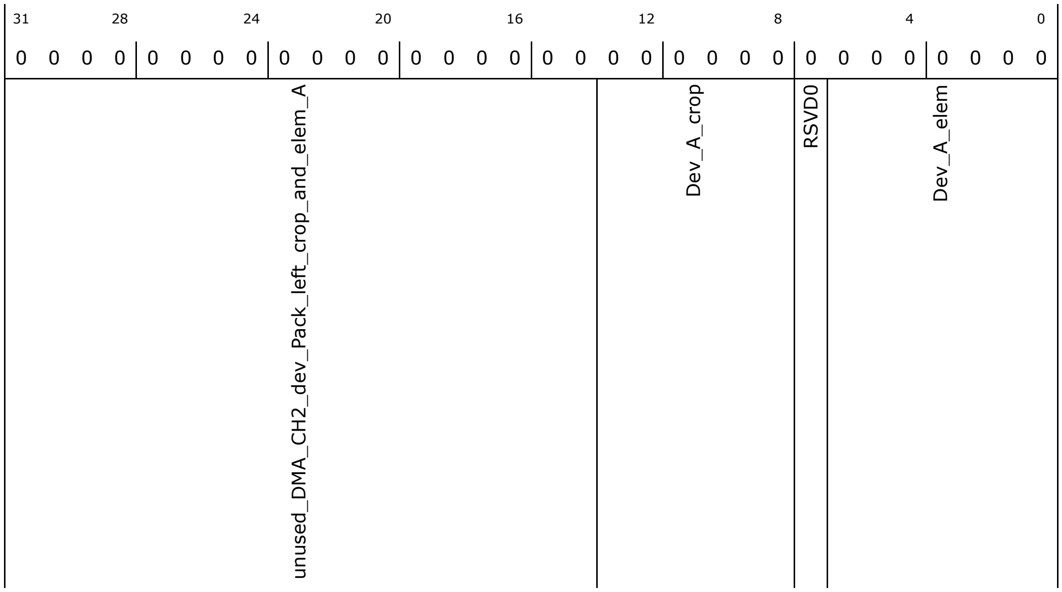
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH2_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.302 reg_isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A)—Offset 4120Ch

DMA CH 3 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4120Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH3_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH3_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.303 reg_isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A)—Offset 41210h

DMA CH 4 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:14	13:8	7	6:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0
unused_DMA_CH4_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH4_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.304 reg_isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A)—Offset 41214h

DMA CH 5 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH5_dev_Pack_left_crop_and_elem_A																		Dev_A_crop						RSVD0	Dev_A_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH5_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.305 reg_isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A)—Offset 41218h

DMA CH 6 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_A:
[ISPMMADR] + 41218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:14	13:8	7	6:0
unused_DMA_CH6_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH6_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.306 reg_isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A)—Offset 4121Ch

DMA CH 7 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_A:
[ISPMMADR] + 4121Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:14	13:8	7	6:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0
Field	unused_DMA_CH7_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH7_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.307 reg_isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A)—Offset 41220h

DMA CH 8 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41220h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH8_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH8_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.308 reg_isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A)—Offset 41224h

DMA CH 9 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41224h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH9_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH9_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.309 reg_isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A)—Offset 41228h

DMA CH 10 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41228h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

unused_DMA_CH10_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH10_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.310 reg_isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A)—Offset 4122Ch

DMA CH 11 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4122Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH11_dev_Pack_left_crop_and_elem_A (31:14), Dev_A_crop (13:8), RSVD0 (7), Dev_A_elem (6:0)

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH11_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.311 reg_isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A)—Offset 41230h

DMA CH 12 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41230h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits 31:14	Bits 13:8	Bit 7	Bits 6:0
unused_DMA_CH12_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH12_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.312 reg_isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A)—Offset 41234h

DMA CH 13 PARAM 2: Device A Packing LSE cropping/Elements

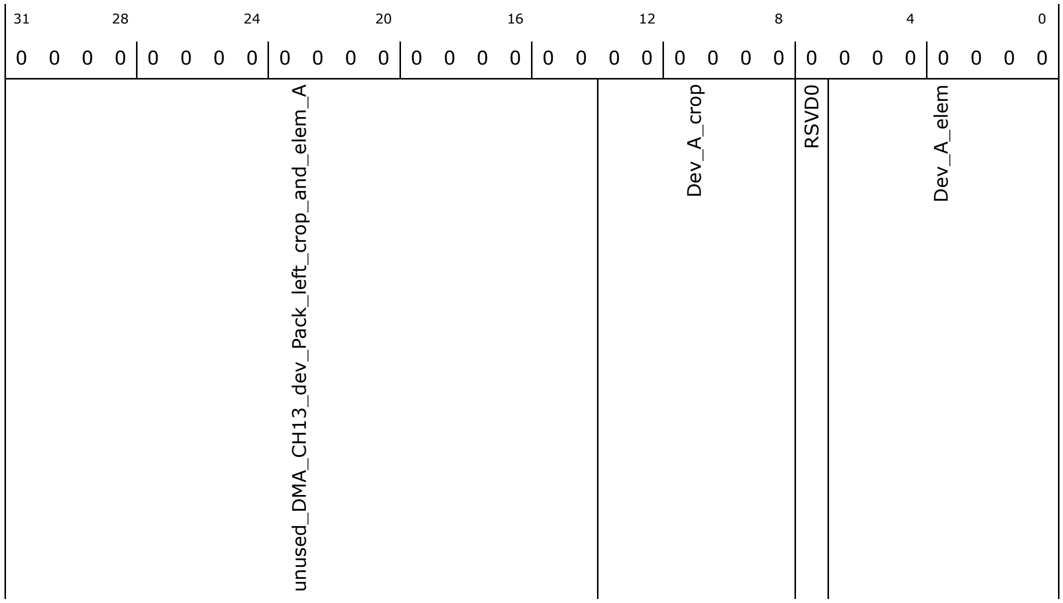
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41234h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH13_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.313 reg_isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A)—Offset 41238h

DMA CH 14 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_DMA_CH14_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH14_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.314 reg_isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A)—Offset 4123Ch

DMA CH 15 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4123Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_DMA_CH15_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH15_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.315 reg_isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A)—Offset 41240h

DMA CH 16 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH16_dev_Pack_left_crop_and_elem_A | Dev_A_crop | RSVD0 | Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH16_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.316 reg_isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A)—Offset 41244h

DMA CH 17 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41244h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH17_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH17_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.317 reg_isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A)—Offset 41248h

DMA CH 18 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41248h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:14	13:8	7	6:0
unused_DMA_CH18_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH18_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.318 reg_isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A)—Offset 4124Ch

DMA CH 19 PARAM 2: Device A Packing LSE cropping/Elements

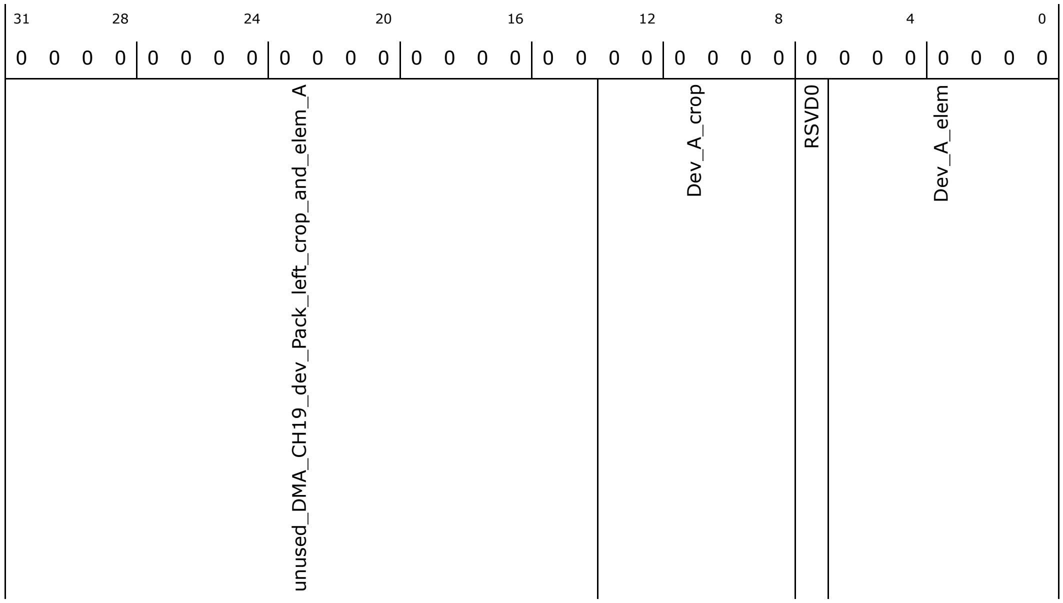
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4124Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH19_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.319 reg_isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A)—Offset 41250h

DMA CH 20 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41250h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH20_dev_Pack_left_crop_and_elem_A | Dev_A_crop | RSVD0 | Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH20_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.320 reg_isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A)—Offset 41254h

DMA CH 21 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41254h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH21_dev_Pack_left_crop_and_elem_A (31:14), Dev_A_crop (13:8), RSVD0 (7), Dev_A_elem (6:0)

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH21_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.321 reg_isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A)—Offset 41258h

DMA CH 22 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41258h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH22_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH22_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.322 reg_isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A)—Offset 4125Ch

DMA CH 23 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4125Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH23_dev_Pack_left_crop_and_elem_A | Dev_A_crop | RSVD0 | Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH23_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.323 reg_isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A)—Offset 41260h

DMA CH 24 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_A:
[ISPMMADR] + 41260h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH24_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH24_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.324 reg_isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A)—Offset 41264h

DMA CH 25 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41264h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:8	Bit 7	Bits 6:0
unused_DMA_CH25_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH25_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.325 reg_isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A)—Offset 41268h

DMA CH 26 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41268h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:14	13:8	7	6:0
unused_DMA_CH26_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH26_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.326 reg_isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A)—Offset 4126Ch

DMA CH 27 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4126Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH27_dev_Pack_left_crop_and_elem_A																		Dev_A_crop						RSVD0	Dev_A_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH27_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.327 reg_isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A)—Offset 41270h

DMA CH 28 PARAM 2: Device A Packing LSE cropping/Elements

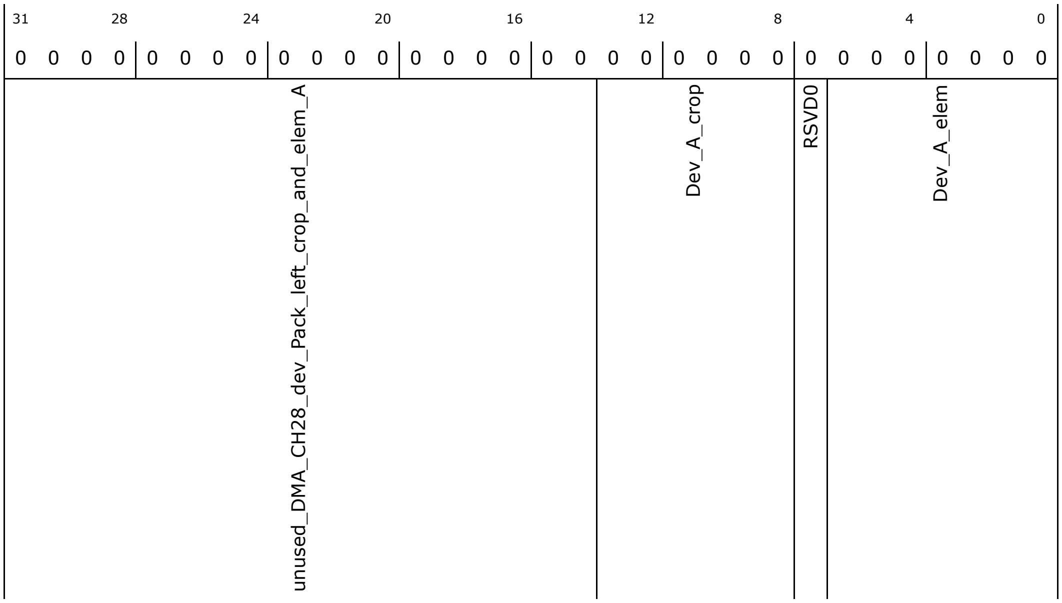
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41270h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH28_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.328 reg_isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A)—Offset 41274h

DMA CH 29 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41274h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:14	13:8	7	6:0
unused_DMA_CH29_dev_Pack_left_crop_and_elem_A	Dev_A_crop	RSVD0	Dev_A_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH29_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.329 reg_isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A)—Offset 41278h

DMA CH 30 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 41278h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH30_dev_Pack_left_crop_and_elem_A (31:14), Dev_A_crop (13:8), RSVD0 (7), Dev_A_elem (6:0)

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH30_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.330 reg_isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A_type (isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A)—Offset 4127Ch

DMA CH 31 PARAM 2: Device A Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 4127Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH31_dev_Pack_left_crop_and_elem_A (31:14), Dev_A_crop (13:8), RSVD0 (7), Dev_A_elem (6:0)

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH31_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.331 reg_isp_dma_DMA_CH22_dev_stride_A_type (isp_dma_DMA_CH22_dev_stride_A)—Offset 412C0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH22_dev_stride_A: [ISPMMADR] + 412C0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH22_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH22_dev_stride_A:** DMA CH 22 PARAM 1: Device A stride

15.8.332 reg_isp_dma_DMA_CH23_dev_stride_A_type (isp_dma_DMA_CH23_dev_stride_A)—Offset 412C4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH23_dev_stride_A: [ISPMMADR] + 412C4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH23_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH23_dev_stride_A:** DMA CH 23 PARAM 1: Device A stride

15.8.333 reg_isp_dma_DMA_CH24_dev_stride_A_type (isp_dma_DMA_CH24_dev_stride_A)—Offset 412C8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH24_dev_stride_A: [ISPMMADR] + 412C8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH24_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH24_dev_stride_A:** DMA CH 24 PARAM 1: Device A stride

15.8.334 reg_isp_dma_DMA_CH25_dev_stride_A_type (isp_dma_DMA_CH25_dev_stride_A)—Offset 412CCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_dev_stride_A: [ISPMMADR] + 412CCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH25_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH25_dev_stride_A:** DMA CH 25 PARAM 1: Device A stride

15.8.335 reg_isp_dma_DMA_CH26_dev_stride_A_type (isp_dma_DMA_CH26_dev_stride_A)—Offset 412D0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH26_dev_stride_A: [ISPMMADR] + 412D0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH26_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH26_dev_stride_A:** DMA CH 26 PARAM 1: Device A stride

15.8.336 reg_isp_dma_DMA_CH27_dev_stride_A_type (isp_dma_DMA_CH27_dev_stride_A)—Offset 412D4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH27_dev_stride_A: [ISPMMADR] + 412D4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH27_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH27_dev_stride_A:** DMA CH 27 PARAM 1: Device A stride

15.8.337 reg_isp_dma_DMA_CH28_dev_stride_A_type (isp_dma_DMA_CH28_dev_stride_A)—Offset 412D8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_dev_stride_A: [ISPMMADR] + 412D8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH28_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH28_dev_stride_A:** DMA CH 28 PARAM 1: Device A stride

15.8.338 reg_isp_dma_DMA_CH29_dev_stride_A_type (isp_dma_DMA_CH29_dev_stride_A)—Offset 412DCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_dev_stride_A: [ISPMMADR] + 412DCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH29_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH29_dev_stride_A:** DMA CH 29 PARAM 1: Device A stride

15.8.339 reg_isp_dma_DMA_CH30_dev_stride_A_type (isp_dma_DMA_CH30_dev_stride_A)—Offset 412E0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH30_dev_stride_A: [ISPMMADR] + 412E0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH30_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH30_dev_stride_A:** DMA CH 30 PARAM 1: Device A stride

15.8.340 reg_isp_dma_DMA_CH31_dev_stride_A_type (isp_dma_DMA_CH31_dev_stride_A)—Offset 412E4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH31_dev_stride_A: [ISPMMADR] + 412E4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH31_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH31_dev_stride_A:** DMA CH 31 PARAM 1: Device A stride

15.8.341 reg_isp_dma_DMA_CH0_Device_Xb_A_type (isp_dma_DMA_CH0_Device_Xb_A)—Offset 41300h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_Device_Xb_A: [ISPMMADR] + 41300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH0_Device_Xb_A

DMA_CH0_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH0_Device_Xb_A:** DMA CH 0 PARAM 3: Device A block width (Xb)

15.8.342 reg_isp_dma_DMA_CH1_Device_Xb_A_type (isp_dma_DMA_CH1_Device_Xb_A)—Offset 41304h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH1_Device_Xb_A: [ISPMMADR] + 41304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH1_Device_Xb_A (bits 31:16) | DMA_CH1_Device_Xb_A (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH1_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH1_Device_Xb_A:** DMA CH 1 PARAM 3: Device A block width (Xb)

15.8.343 reg_isp_dma_DMA_CH2_Device_Xb_A_type (isp_dma_DMA_CH2_Device_Xb_A)—Offset 41308h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH2_Device_Xb_A: [ISPMMADR] + 41308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH2_Device_Xb_A (bits 31:16) | DMA_CH2_Device_Xb_A (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH2_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH2_Device_Xb_A:** DMA CH 2 PARAM 3: Device A block width (Xb)

15.8.344 reg_isp_dma_DMA_CH3_Device_Xb_A_type (isp_dma_DMA_CH3_Device_Xb_A)—Offset 4130Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH3_Device_Xb_A: [ISPMMADR] + 4130Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

31:16	15:0
unused_DMA_CH3_Device_Xb_A	DMA_CH3_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH3_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH3_Device_Xb_A:** DMA CH 3 PARAM 3: Device A block width (Xb)

15.8.345 reg_isp_dma_DMA_CH4_Device_Xb_A_type (isp_dma_DMA_CH4_Device_Xb_A)—Offset 41310h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH4_Device_Xb_A: [ISPMMADR] + 41310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH4_Device_Xb_A	DMA_CH4_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH4_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH4_Device_Xb_A:** DMA CH 4 PARAM 3: Device A block width (Xb)

15.8.346 reg_isp_dma_DMA_CH5_Device_Xb_A_type (isp_dma_DMA_CH5_Device_Xb_A)—Offset 41314h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH5_Device_Xb_A: [ISPMMADR] + 41314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH5_Device_Xb_A	DMA_CH5_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH5_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH5_Device_Xb_A:** DMA CH 5 PARAM 3: Device A block width (Xb)

15.8.347 reg_isp_dma_DMA_CH6_Device_Xb_A_type (isp_dma_DMA_CH6_Device_Xb_A)—Offset 41318h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_Device_Xb_A: [ISPMMADR] + 41318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH6_Device_Xb_A (31:16), DMA_CH6_Device_Xb_A (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH6_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH6_Device_Xb_A:** DMA CH 6 PARAM 3: Device A block width (Xb)

15.8.348 reg_isp_dma_DMA_CH7_Device_Xb_A_type (isp_dma_DMA_CH7_Device_Xb_A)—Offset 4131Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_Device_Xb_A: [ISPMMADR] + 4131Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:16	15:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
unused_DMA_CH7_Device_Xb_A	DMA_CH7_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH7_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH7_Device_Xb_A:** DMA CH 7 PARAM 3: Device A block width (Xb)

15.8.349 reg_isp_dma_DMA_CH8_Device_Xb_A_type (isp_dma_DMA_CH8_Device_Xb_A)—Offset 41320h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_Device_Xb_A: [ISPMMADR] + 41320h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:16	15:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
unused_DMA_CH8_Device_Xb_A	DMA_CH8_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH8_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH8_Device_Xb_A:** DMA CH 8 PARAM 3: Device A block width (Xb)

15.8.350 reg_isp_dma_DMA_CH9_Device_Xb_A_type (isp_dma_DMA_CH9_Device_Xb_A)—Offset 41324h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_Device_Xb_A: [ISPMMADR] + 41324h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH9_Device_Xb_A (bits 31:16), DMA_CH9_Device_Xb_A (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH9_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH9_Device_Xb_A:** DMA CH 9 PARAM 3: Device A block width (Xb)

15.8.351 reg_isp_dma_DMA_CH10_Device_Xb_A_type (isp_dma_DMA_CH10_Device_Xb_A)—Offset 41328h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_Device_Xb_A: [ISPMMADR] + 41328h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH10_Device_Xb_A	DMA_CH10_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH10_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH10_Device_Xb_A:** DMA CH 10 PARAM 3: Device A block width (Xb)

15.8.352 reg_isp_dma_DMA_CH11_Device_Xb_A_type (isp_dma_DMA_CH11_Device_Xb_A)—Offset 4132Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_Device_Xb_A: [ISPMMADR] + 4132Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH11_Device_Xb_A	DMA_CH11_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH11_Device_Xb_A:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH11_Device_Xb_A:** DMA CH 11 PARAM 3: Device A block width (Xb)

15.8.353 reg_isp_dma_DMA_CH12_Device_Xb_A_type (isp_dma_DMA_CH12_Device_Xb_A)—Offset 41330h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_Device_Xb_A: [ISPMMADR] + 41330h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH12_Device_Xb_A	DMA_CH12_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH12_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH12_Device_Xb_A:** DMA CH 12 PARAM 3: Device A block width (Xb)

15.8.354 reg_isp_dma_DMA_CH13_Device_Xb_A_type (isp_dma_DMA_CH13_Device_Xb_A)—Offset 41334h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_Device_Xb_A: [ISPMMADR] + 41334h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH13_Device_Xb_A (31:16), DMA_CH13_Device_Xb_A (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH13_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH13_Device_Xb_A:** DMA CH 13 PARAM 3: Device A block width (Xb)

15.8.355 reg_isp_dma_DMA_CH14_Device_Xb_A_type (isp_dma_DMA_CH14_Device_Xb_A)—Offset 41338h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_Device_Xb_A: [ISPMMADR] + 41338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH14_Device_Xb_A (31:16), DMA_CH14_Device_Xb_A (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH14_Device_Xb_A:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH14_Device_Xb_A:** DMA CH 14 PARAM 3: Device A block width (Xb)

15.8.356 reg_isp_dma_DMA_CH15_Device_Xb_A_type (isp_dma_DMA_CH15_Device_Xb_A)—Offset 4133Ch

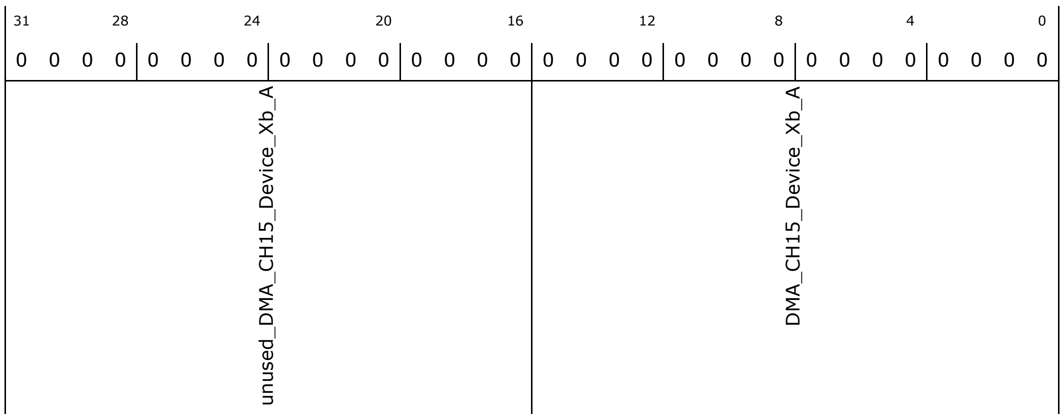
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH15_Device_Xb_A: [ISPMMADR] + 4133Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH15_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH15_Device_Xb_A:** DMA CH 15 PARAM 3: Device A block width (Xb)

15.8.357 reg_isp_dma_DMA_CH16_Device_Xb_A_type (isp_dma_DMA_CH16_Device_Xb_A)—Offset 41340h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH16_Device_Xb_A: [ISPMMADR] + 41340h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH16_Device_Xb_A																DMA_CH16_Device_Xb_A															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH16_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH16_Device_Xb_A:** DMA CH 16 PARAM 3: Device A block width (Xb)

15.8.358 reg_isp_dma_DMA_CH17_Device_Xb_A_type (isp_dma_DMA_CH17_Device_Xb_A)—Offset 41344h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_Device_Xb_A: [ISPMMADR] + 41344h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH17_Device_Xb_A																DMA_CH17_Device_Xb_A															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH17_Device_Xb_A:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH17_Device_Xb_A:** DMA CH 17 PARAM 3: Device A block width (Xb)

15.8.359 reg_isp_dma_DMA_CH18_Device_Xb_A_type (isp_dma_DMA_CH18_Device_Xb_A)—Offset 41348h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_Device_Xb_A: [ISPMMADR] + 41348h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH18_Device_Xb_A																DMA_CH18_Device_Xb_A															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH18_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH18_Device_Xb_A:** DMA CH 18 PARAM 3: Device A block width (Xb)

15.8.360 reg_isp_dma_DMA_CH19_Device_Xb_A_type (isp_dma_DMA_CH19_Device_Xb_A)—Offset 4134Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_Device_Xb_A: [ISPMMADR] + 4134Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH19_Device_Xb_A

DMA_CH19_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH19_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH19_Device_Xb_A:** DMA CH 19 PARAM 3: Device A block width (Xb)

15.8.361 reg_isp_dma_DMA_CH20_Device_Xb_A_type (isp_dma_DMA_CH20_Device_Xb_A)—Offset 41350h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_Device_Xb_A: [ISPMMADR] + 41350h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH20_Device_Xb_A

DMA_CH20_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH20_Device_Xb_A:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH20_Device_Xb_A:** DMA CH 20 PARAM 3: Device A block width (Xb)

15.8.362 reg_isp_dma_DMA_CH21_Device_Xb_A_type (isp_dma_DMA_CH21_Device_Xb_A)—Offset 41354h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH21_Device_Xb_A: [ISPMMADR] + 41354h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH21_Device_Xb_A	DMA_CH21_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH21_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH21_Device_Xb_A:** DMA CH 21 PARAM 3: Device A block width (Xb)

15.8.363 reg_isp_dma_DMA_CH22_Device_Xb_A_type (isp_dma_DMA_CH22_Device_Xb_A)—Offset 41358h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH22_Device_Xb_A: [ISPMMADR] + 41358h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH22_Device_Xb_A	DMA_CH22_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH22_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH22_Device_Xb_A:** DMA CH 22 PARAM 3: Device A block width (Xb)

15.8.364 reg_isp_dma_DMA_CH23_Device_Xb_A_type (isp_dma_DMA_CH23_Device_Xb_A)—Offset 4135Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_Device_Xb_A: [ISPMMADR] + 4135Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH23_Device_Xb_A	DMA_CH23_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH23_Device_Xb_A:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH23_Device_Xb_A:** DMA CH 23 PARAM 3: Device A block width (Xb)

15.8.365 reg_isp_dma_DMA_CH24_Device_Xb_A_type (isp_dma_DMA_CH24_Device_Xb_A)—Offset 41360h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_Device_Xb_A: [ISPMMADR] + 41360h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: bits 31:16 unused_DMA_CH24_Device_Xb_A; bits 15:0 DMA_CH24_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH24_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH24_Device_Xb_A:** DMA CH 24 PARAM 3: Device A block width (Xb)

15.8.366 reg_isp_dma_DMA_CH25_Device_Xb_A_type (isp_dma_DMA_CH25_Device_Xb_A)—Offset 41364h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_Device_Xb_A: [ISPMMADR] + 41364h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH25_Device_Xb_A (31:16) | DMA_CH25_Device_Xb_A (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH25_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH25_Device_Xb_A:** DMA CH 25 PARAM 3: Device A block width (Xb)

15.8.367 reg_isp_dma_DMA_CH26_Device_Xb_A_type (isp_dma_DMA_CH26_Device_Xb_A)—Offset 41368h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_Device_Xb_A: [ISPMMADR] + 41368h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH26_Device_Xb_A (31:16) | DMA_CH26_Device_Xb_A (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH26_Device_Xb_A:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH26_Device_Xb_A:** DMA CH 26 PARAM 3: Device A block width (Xb)

15.8.368 reg_isp_dma_DMA_CH27_Device_Xb_A_type (isp_dma_DMA_CH27_Device_Xb_A)—Offset 4136Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH27_Device_Xb_A: [ISPMMADR] + 4136Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH27_Device_Xb_A	DMA_CH27_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH27_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH27_Device_Xb_A:** DMA CH 27 PARAM 3: Device A block width (Xb)

15.8.369 reg_isp_dma_DMA_CH28_Device_Xb_A_type (isp_dma_DMA_CH28_Device_Xb_A)—Offset 41370h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH28_Device_Xb_A: [ISPMMADR] + 41370h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH28_Device_Xb_A	DMA_CH28_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH28_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH28_Device_Xb_A:** DMA CH 28 PARAM 3: Device A block width (Xb)

15.8.370 reg_isp_dma_DMA_CH29_Device_Xb_A_type (isp_dma_DMA_CH29_Device_Xb_A)—Offset 41374h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_Device_Xb_A: [ISPMMADR] + 41374h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH29_Device_Xb_A	DMA_CH29_Device_Xb_A

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH29_Device_Xb_A:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH29_Device_Xb_A:** DMA CH 29 PARAM 3: Device A block width (Xb)

15.8.371 reg_isp_dma_DMA_CH30_Device_Xb_A_type (isp_dma_DMA_CH30_Device_Xb_A)—Offset 41378h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH30_Device_Xb_A: [ISPMMADR] + 41378h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH30_Device_Xb_A																DMA_CH30_Device_Xb_A															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH30_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH30_Device_Xb_A:** DMA CH 30 PARAM 3: Device A block width (Xb)

15.8.372 reg_isp_dma_DMA_CH31_Device_Xb_A_type (isp_dma_DMA_CH31_Device_Xb_A)—Offset 4137Ch

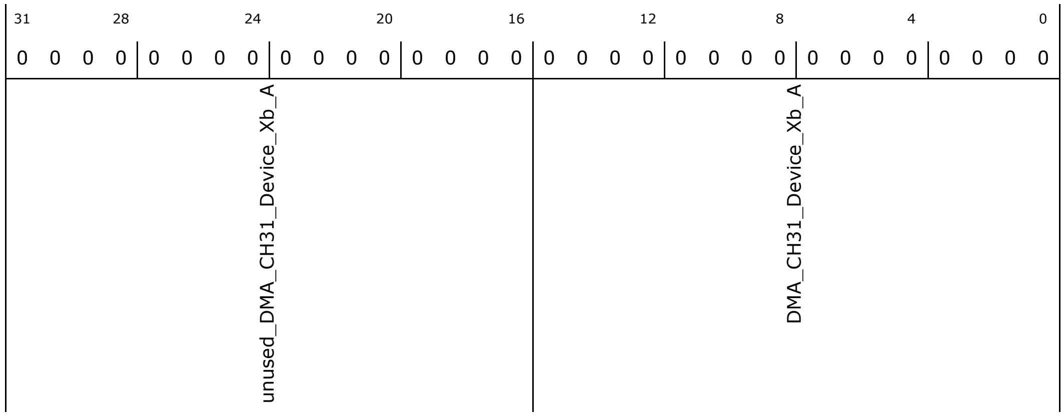
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH31_Device_Xb_A: [ISPMMADR] + 4137Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH31_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH31_Device_Xb_A:** DMA CH 31 PARAM 3: Device A block width (Xb)

15.8.373 reg_isp_dma_DMA_CH0_dev_stride_B_type (isp_dma_DMA_CH0_dev_stride_B)—Offset 41400h

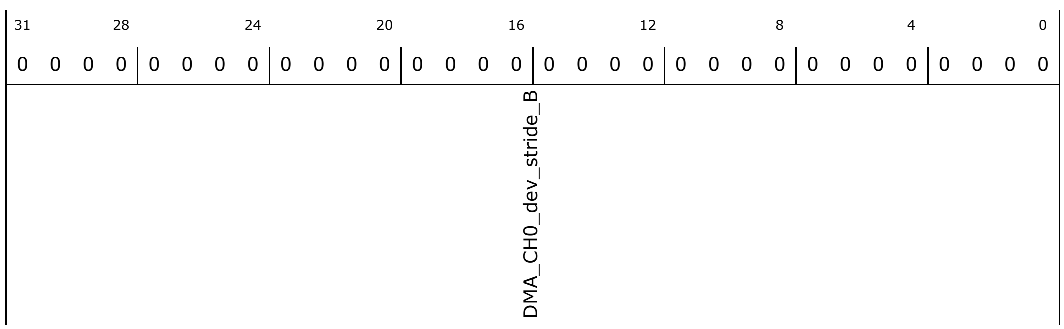
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH0_dev_stride_B: [ISPMMADR] + 41400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH0_dev_stride_B:** DMA CH 0 PARAM 4: Device B stride

15.8.374 reg_isp_dma_DMA_CH1_dev_stride_B_type (isp_dma_DMA_CH1_dev_stride_B)—Offset 41404h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_dev_stride_B: [ISPMMADR] + 41404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH1_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH1_dev_stride_B:** DMA CH 1 PARAM 4: Device B stride

15.8.375 reg_isp_dma_DMA_CH2_dev_stride_B_type (isp_dma_DMA_CH2_dev_stride_B)—Offset 41408h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_dev_stride_B: [ISPMMADR] + 41408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH2_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH2_dev_stride_B:** DMA CH 2 PARAM 4: Device B stride

15.8.376 reg_isp_dma_DMA_CH3_dev_stride_B_type (isp_dma_DMA_CH3_dev_stride_B)—Offset 4140Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_dev_stride_B: [ISPMMADR] + 4140Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH3_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH3_dev_stride_B:** DMA CH 3 PARAM 4: Device B stride

15.8.377 reg_isp_dma_DMA_CH4_dev_stride_B_type (isp_dma_DMA_CH4_dev_stride_B)—Offset 41410h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_dev_stride_B: [ISPMMADR] + 41410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH4_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH4_dev_stride_B:** DMA CH 4 PARAM 4: Device B stride

15.8.378 reg_isp_dma_DMA_CH5_dev_stride_B_type (isp_dma_DMA_CH5_dev_stride_B)—Offset 41414h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH5_dev_stride_B: [ISPMMADR] + 41414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH5_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH5_dev_stride_B:** DMA CH 5 PARAM 4: Device B stride

15.8.379 reg_isp_dma_DMA_CH6_dev_stride_B_type (isp_dma_DMA_CH6_dev_stride_B)—Offset 41418h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH6_dev_stride_B: [ISPMMADR] + 41418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH6_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH6_dev_stride_B:** DMA CH 6 PARAM 4: Device B stride

15.8.380 reg_isp_dma_DMA_CH7_dev_stride_B_type (isp_dma_DMA_CH7_dev_stride_B)—Offset 4141Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_dev_stride_B: [ISPMMADR] + 4141Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH7_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH7_dev_stride_B:** DMA CH 7 PARAM 4: Device B stride

15.8.381 reg_isp_dma_DMA_CH8_dev_stride_B_type (isp_dma_DMA_CH8_dev_stride_B)—Offset 41420h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_dev_stride_B: [ISPMMADR] + 41420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH8_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH8_dev_stride_B:** DMA CH 8 PARAM 4: Device B stride

15.8.382 reg_isp_dma_DMA_CH9_dev_stride_B_type (isp_dma_DMA_CH9_dev_stride_B)—Offset 41424h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_dev_stride_B: [ISPMMADR] + 41424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH9_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH9_dev_stride_B:** DMA CH 9 PARAM 4: Device B stride

15.8.383 reg_isp_dma_DMA_CH10_dev_stride_B_type (isp_dma_DMA_CH10_dev_stride_B)—Offset 41428h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_dev_stride_B: [ISPMMADR] + 41428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH10_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH10_dev_stride_B:** DMA CH 10 PARAM 4: Device B stride

15.8.384 reg_isp_dma_DMA_CH11_dev_stride_B_type (isp_dma_DMA_CH11_dev_stride_B)—Offset 4142Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_dev_stride_B: [ISPMMADR] + 4142Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH11_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH11_dev_stride_B:** DMA CH 11 PARAM 4: Device B stride

15.8.385 reg_isp_dma_DMA_CH12_dev_stride_B_type (isp_dma_DMA_CH12_dev_stride_B)—Offset 41430h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_dev_stride_B: [ISPMMADR] + 41430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH12_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH12_dev_stride_B:** DMA CH 12 PARAM 4: Device B stride

15.8.386 reg_isp_dma_DMA_CH13_dev_stride_B_type (isp_dma_DMA_CH13_dev_stride_B)—Offset 41434h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_dev_stride_B: [ISPMMADR] + 41434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH13_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH13_dev_stride_B:** DMA CH 13 PARAM 4: Device B stride

15.8.387 reg_isp_dma_DMA_CH14_dev_stride_B_type (isp_dma_DMA_CH14_dev_stride_B)—Offset 41438h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_dev_stride_B: [ISPMMADR] + 41438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH14_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH14_dev_stride_B:** DMA CH 14 PARAM 4: Device B stride

15.8.388 reg_isp_dma_DMA_CH15_dev_stride_B_type (isp_dma_DMA_CH15_dev_stride_B)—Offset 4143Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH15_dev_stride_B: [ISPMMADR] + 4143Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH15_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH15_dev_stride_B:** DMA CH 15 PARAM 4: Device B stride

15.8.389 reg_isp_dma_DMA_CH16_dev_stride_B_type (isp_dma_DMA_CH16_dev_stride_B)—Offset 41440h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH16_dev_stride_B: [ISPMMADR] + 41440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH16_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH16_dev_stride_B:** DMA CH 16 PARAM 4: Device B stride

15.8.390 reg_isp_dma_DMA_CH17_dev_stride_B_type (isp_dma_DMA_CH17_dev_stride_B)—Offset 41444h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_dev_stride_B: [ISPMMADR] + 41444h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH17_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH17_dev_stride_B:** DMA CH 17 PARAM 4: Device B stride

15.8.391 reg_isp_dma_DMA_CH18_dev_stride_B_type (isp_dma_DMA_CH18_dev_stride_B)—Offset 41448h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH18_dev_stride_B: [ISPMMADR] + 41448h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH18_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH18_dev_stride_B:** DMA CH 18 PARAM 4: Device B stride

15.8.392 reg_isp_dma_DMA_CH19_dev_stride_B_type (isp_dma_DMA_CH19_dev_stride_B)—Offset 4144Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH19_dev_stride_B: [ISPMMADR] + 4144Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH19_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH19_dev_stride_B:** DMA CH 19 PARAM 4: Device B stride

15.8.393 reg_isp_dma_DMA_CH20_dev_stride_B_type (isp_dma_DMA_CH20_dev_stride_B)—Offset 41450h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_dev_stride_B: [ISPMMADR] + 41450h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH20_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH20_dev_stride_B:** DMA CH 20 PARAM 4: Device B stride

15.8.394 reg_isp_dma_DMA_CH21_dev_stride_B_type (isp_dma_DMA_CH21_dev_stride_B)—Offset 41454h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_dev_stride_B: [ISPMMADR] + 41454h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH21_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH21_dev_stride_B:** DMA CH 21 PARAM 4: Device B stride

15.8.395 reg_isp_dma_DMA_CH22_dev_stride_B_type (isp_dma_DMA_CH22_dev_stride_B)—Offset 41458h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_dev_stride_B: [ISPMMADR] + 41458h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH22_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH22_dev_stride_B:** DMA CH 22 PARAM 4: Device B stride

15.8.396 reg_isp_dma_DMA_CH23_dev_stride_B_type (isp_dma_DMA_CH23_dev_stride_B)—Offset 4145Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_dev_stride_B: [ISPMMADR] + 4145Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH23_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH23_dev_stride_B:** DMA CH 23 PARAM 4: Device B stride

15.8.397 reg_isp_dma_DMA_CH24_dev_stride_B_type (isp_dma_DMA_CH24_dev_stride_B)—Offset 41460h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH24_dev_stride_B: [ISPMMADR] + 41460h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH24_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH24_dev_stride_B:** DMA CH 24 PARAM 4: Device B stride

15.8.398 reg_isp_dma_DMA_CH26_dev_stride_B_type (isp_dma_DMA_CH26_dev_stride_B)—Offset 41468h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH26_dev_stride_B: [ISPMMADR] + 41468h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH26_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH26_dev_stride_B:** DMA CH 26 PARAM 4: Device B stride

15.8.399 reg_isp_dma_DMA_CH27_dev_stride_B_type (isp_dma_DMA_CH27_dev_stride_B)—Offset 4146Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH27_dev_stride_B: [ISPMMADR] + 4146Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH27_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH27_dev_stride_B:** DMA CH 27 PARAM 4: Device B stride

15.8.400 reg_isp_dma_DMA_CH28_dev_stride_B_type (isp_dma_DMA_CH28_dev_stride_B)—Offset 41470h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH28_dev_stride_B: [ISPMMADR] + 41470h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DMA_CH28_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH28_dev_stride_B:** DMA CH 28 PARAM 4: Device B stride

15.8.401 reg_isp_dma_DMA_CH29_dev_stride_B_type (isp_dma_DMA_CH29_dev_stride_B)—Offset 41474h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH29_dev_stride_B: [ISPMMADR] + 41474h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DMA_CH29_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH29_dev_stride_B:** DMA CH 29 PARAM 4: Device B stride

15.8.402 reg_isp_dma_DMA_CH30_dev_stride_B_type (isp_dma_DMA_CH30_dev_stride_B)—Offset 41478h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH30_dev_stride_B: [ISPMMADR] + 41478h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH30_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH30_dev_stride_B:** DMA CH 30 PARAM 4: Device B stride

15.8.403 reg_isp_dma_DMA_CH31_dev_stride_B_type (isp_dma_DMA_CH31_dev_stride_B)—Offset 4147Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH31_dev_stride_B: [ISPMMADR] + 4147Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH31_dev_stride_B

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH31_dev_stride_B:** DMA CH 30 PARAM 4: Device B stride

15.8.404 reg_isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 41500h

DMA CH 0 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:14	13:8	7	6:0
Default	0000 0000 0000 0000 00	00 0000	0	000 0000
Field	unused_DMA_CH0_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH0_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.405 reg_isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B)—Offset 41504h

DMA CH 1 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:14	13:8	7	6:0
unused_DMA_CH1_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH1_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.406 reg_isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B)—Offset 41508h

DMA CH 2 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Field
31:14	unused_DMA_CH2_dev_Pack_left_crop_and_elem_B
13:8	Dev_B_crop
7	RSVD0
6:0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH2_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.407 reg_isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B)—Offset 4150Ch

DMA CH 3 PARAM 5: Device B Packing LSE cropping/Elements

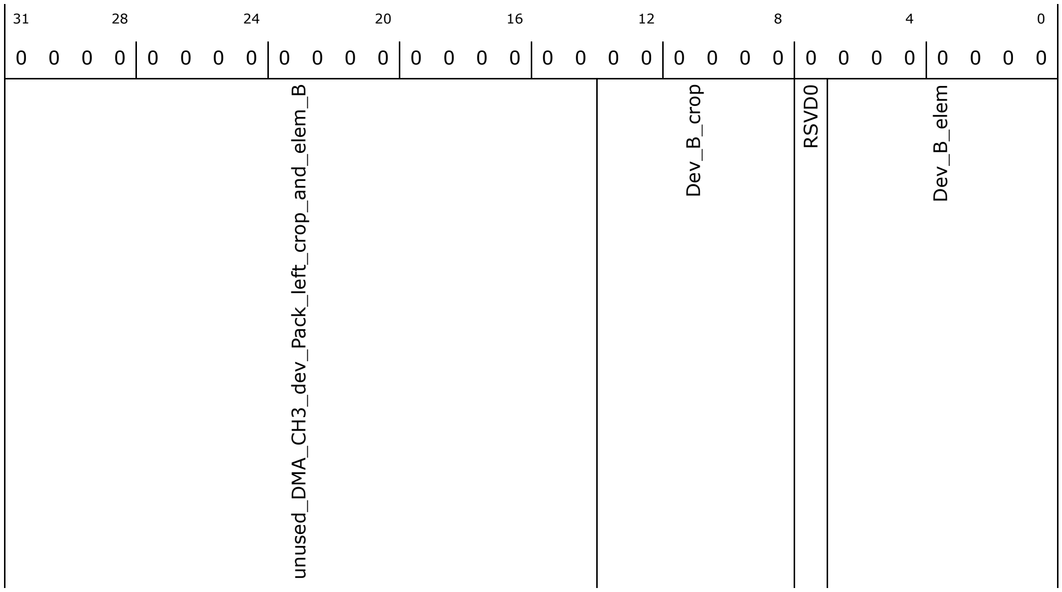
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4150Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH3_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.408 reg_isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B)—Offset 41510h

DMA CH 4 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:8	Bit 7	Bits 6:0
unused_DMA_CH4_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH4_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.409 reg_isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B)—Offset 41514h

DMA CH 5 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH5_dev_Pack_left_crop_and_elem_B:
[ISPMMADR] + 41514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH5_dev_Pack_left_crop_and_elem_B																		Dev_B_crop						RSVD0	Dev_B_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH5_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.410 reg_isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B)—Offset 41518h

DMA CH 6 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH6_dev_Pack_left_crop_and_elem_B																		Dev_B_crop						RSVD0	Dev_B_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH6_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.411 reg_isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B)—Offset 4151Ch

DMA CH 7 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4151Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH7_dev_Pack_left_crop_and_elem_B | Dev_B_crop | RSVD0 | Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH7_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.412 reg_isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B)—Offset 41520h

DMA CH 8 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41520h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

unused_DMA_CH8_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH8_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.413 reg_isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B)—Offset 41524h

DMA CH 9 PARAM 5: Device B Packing LSE cropping/Elements

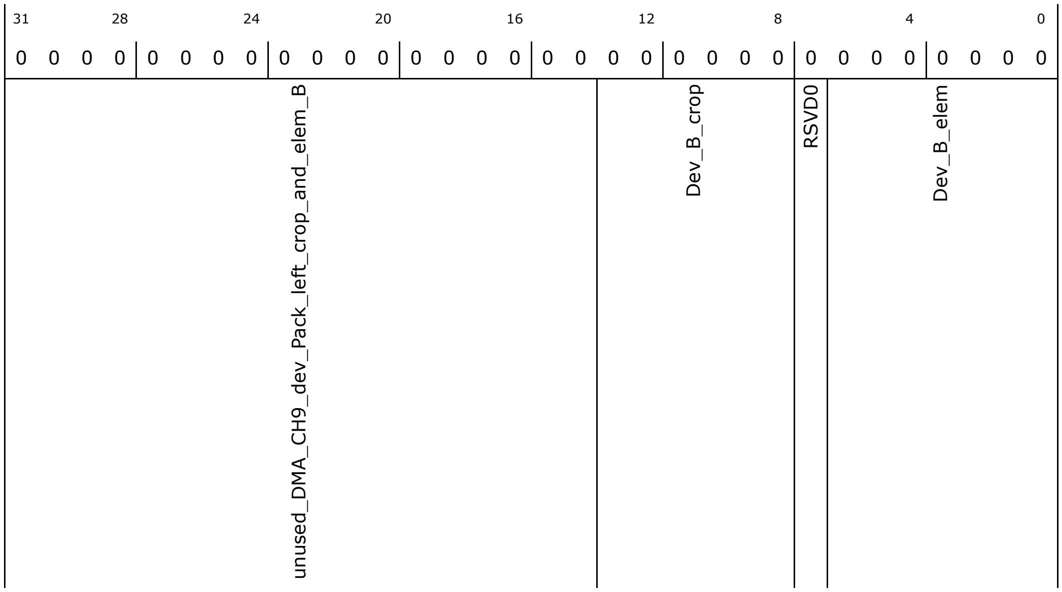
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH9_dev_Pack_left_crop_and_elem_B:
[ISPMMADR] + 41524h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH9_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.414 reg_isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B)—Offset 41528h

DMA CH 10 PARAM 5: Device B Packing LSE cropping/Elements

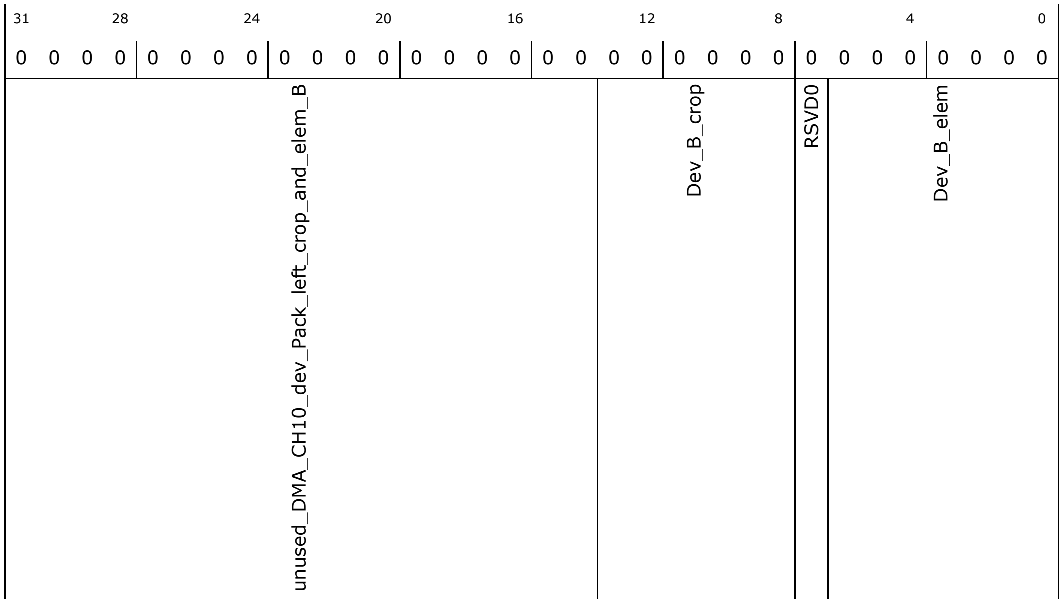
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH10_dev_Pack_left_crop_and_elem_B:
[ISPMMADR] + 41528h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH10_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.415 reg_isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B)—Offset 4152Ch

DMA CH 11 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4152Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH11_dev_Pack_left_crop_and_elem_B																		Dev_B_crop						RSVD0	Dev_B_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH11_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.416 reg_isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B)—Offset 41530h

DMA CH 12 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41530h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH12_dev_Pack_left_crop_and_elem_B

Dev_B_crop

RSVD0

Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH12_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.417 reg_isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B)—Offset 41534h

DMA CH 13 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41534h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH13_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH13_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.418 reg_isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B)—Offset 41538h

DMA CH 14 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41538h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

unused_DMA_CH14_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH14_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.419 reg_isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B)—Offset 4153Ch

DMA CH 15 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4153Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:8	Bit 7	Bits 6:0
unused_DMA_CH15_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH15_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.420 reg_isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B)—Offset 41540h

DMA CH 16 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41540h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0
unused_DMA_CH16_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH16_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.421 reg_isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B)—Offset 41544h

DMA CH 17 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41544h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH17_dev_Pack_left_crop_and_elem_B																		Dev_B_crop						RSVD0	Dev_B_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH17_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.422 reg_isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B)—Offset 41548h

DMA CH 18 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41548h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH18_dev_Pack_left_crop_and_elem_B																		Dev_B_crop						RSVD0	Dev_B_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH18_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.423 reg_isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B)—Offset 4154Ch

DMA CH 19 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH19_dev_Pack_left_crop_and_elem_B:
[ISPMMADR] + 4154Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH19_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH19_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.424 reg_isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B)—Offset 41550h

DMA CH 20 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41550h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH20_dev_Pack_left_crop_and_elem_B | Dev_B_crop | RSVD0 | Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH20_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.425 reg_isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B)—Offset 41554h

DMA CH 21 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41554h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:14	13:8	7	6:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0
unused_DMA_CH21_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH21_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.426 reg_isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B)—Offset 41558h

DMA CH 22 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41558h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:8	Bit 7	Bits 6:0
unused_DMA_CH22_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH22_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.427 reg_isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B)—Offset 4155Ch

DMA CH 23 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4155Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH23_dev_Pack_left_crop_and_elem_B																		Dev_B_crop						RSVD0	Dev_B_elem						

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH23_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.428 reg_isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B)—Offset 41560h

DMA CH 24 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41560h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH24_dev_Pack_left_crop_and_elem_B | Dev_B_crop | RSVD0 | Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH24_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.429 reg_isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B)—Offset 41564h

DMA CH 25 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41564h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH25_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH25_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.430 reg_isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B)—Offset 41568h

DMA CH 26 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41568h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields (bits 31 to 0): unused_DMA_CH26_dev_Pack_left_crop_and_elem_B | Dev_B_crop | RSVD0 | Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH26_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.431 reg_isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B)—Offset 4156Ch

DMA CH 27 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH27_dev_Pack_left_crop_and_elem_B:
[ISPMMADR] + 4156Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:8	Bit 7	Bits 6:0
unused_DMA_CH27_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH27_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.432 reg_isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B)—Offset 41570h

DMA CH 28 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41570h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH28_dev_Pack_left_crop_and_elem_B (31:14), Dev_B_crop (13:8), RSVD0 (7), Dev_B_elem (6:0)

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH28_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.433 reg_isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B)—Offset 41574h

DMA CH 29 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41574h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_DMA_CH29_dev_Pack_left_crop_and_elem_B | Dev_B_crop | RSVD0 | Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH29_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.434 reg_isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B)—Offset 41578h

DMA CH 30 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 41578h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH30_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH30_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.435 reg_isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B_type (isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B)—Offset 4157Ch

DMA CH 31 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_dev_Pack_left_crop_and_elem_B: [ISPMMADR] + 4157Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:14	13:8	7	6:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0
unused_DMA_CH31_dev_Pack_left_crop_and_elem_B	Dev_B_crop	RSVD0	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH31_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0b RO	**RSVD0:** Reserved
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.436 reg_isp_dma_DMA_CH0_Device_Xb_B_type (isp_dma_DMA_CH0_Device_Xb_B)—Offset 41600h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH0_Device_Xb_B: [ISPMMADR] + 41600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH0_Device_Xb_B																DMA_CH0_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH0_Device_Xb_B:** DMA CH 0 PARAM 6: Device B block width (Xb)

15.8.437 reg_isp_dma_DMA_CH1_Device_Xb_B_type (isp_dma_DMA_CH1_Device_Xb_B)—Offset 41604h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH1_Device_Xb_B: [ISPMMADR] + 41604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH1_Device_Xb_B																DMA_CH1_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH1_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH1_Device_Xb_B:** DMA CH 1 PARAM 6: Device B block width (Xb)

15.8.438 reg_isp_dma_DMA_CH2_Device_Xb_B_type (isp_dma_DMA_CH2_Device_Xb_B)—Offset 41608h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_Device_Xb_B: [ISPMMADR] + 41608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH2_Device_Xb_B	DMA_CH2_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH2_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH2_Device_Xb_B:** DMA CH 2 PARAM 6: Device B block width (Xb)

15.8.439 reg_isp_dma_DMA_CH3_Device_Xb_B_type (isp_dma_DMA_CH3_Device_Xb_B)—Offset 4160Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_Device_Xb_B: [ISPMMADR] + 4160Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH3_Device_Xb_B	DMA_CH3_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH3_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH3_Device_Xb_B:** DMA CH 3 PARAM 6: Device B block width (Xb)

15.8.440 reg_isp_dma_DMA_CH4_Device_Xb_B_type (isp_dma_DMA_CH4_Device_Xb_B)—Offset 41610h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH4_Device_Xb_B: [ISPMMADR] + 41610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH4_Device_Xb_B	DMA_CH4_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH4_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH4_Device_Xb_B:** DMA CH 4 PARAM 6: Device B block width (Xb)

15.8.441 reg_isp_dma_DMA_CH5_Device_Xb_B_type (isp_dma_DMA_CH5_Device_Xb_B)—Offset 41614h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_Device_Xb_B: [ISPMMADR] + 41614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH5_Device_Xb_B																DMA_CH5_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH5_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH5_Device_Xb_B:** DMA CH 5 PARAM 6: Device B block width (Xb)

15.8.442 reg_isp_dma_DMA_CH6_Device_Xb_B_type (isp_dma_DMA_CH6_Device_Xb_B)—Offset 41618h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_Device_Xb_B: [ISPMMADR] + 41618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH6_Device_Xb_B	DMA_CH6_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH6_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH6_Device_Xb_B:** DMA CH 6 PARAM 6: Device B block width (Xb)

15.8.443 reg_isp_dma_DMA_CH7_Device_Xb_B_type (isp_dma_DMA_CH7_Device_Xb_B)—Offset 4161Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_Device_Xb_B: [ISPMMADR] + 4161Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH7_Device_Xb_B	DMA_CH7_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH7_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH7_Device_Xb_B:** DMA CH 7 PARAM 6: Device B block width (Xb)

15.8.444 reg_isp_dma_DMA_CH8_Device_Xb_B_type (isp_dma_DMA_CH8_Device_Xb_B)—Offset 41620h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_Device_Xb_B: [ISPMMADR] + 41620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: unused_DMA_CH8_Device_Xb_B
Bits 15:0: DMA_CH8_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH8_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH8_Device_Xb_B:** DMA CH 8 PARAM 6: Device B block width (Xb)

15.8.445 reg_isp_dma_DMA_CH9_Device_Xb_B_type (isp_dma_DMA_CH9_Device_Xb_B)—Offset 41624h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_Device_Xb_B: [ISPMMADR] + 41624h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH9_Device_Xb_B																DMA_CH9_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH9_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH9_Device_Xb_B:** DMA CH 9 PARAM 6: Device B block width (Xb)

15.8.446 reg_isp_dma_DMA_CH10_Device_Xb_B_type (isp_dma_DMA_CH10_Device_Xb_B)—Offset 41628h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH10_Device_Xb_B: [ISPMMADR] + 41628h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH10_Device_Xb_B																DMA_CH10_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH10_Device_Xb_B:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH10_Device_Xb_B:** DMA CH 10 PARAM 6: Device B block width (Xb)

15.8.447 reg_isp_dma_DMA_CH11_Device_Xb_B_type (isp_dma_DMA_CH11_Device_Xb_B)—Offset 4162Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_Device_Xb_B: [ISPMMADR] + 4162Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH11_Device_Xb_B	DMA_CH11_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH11_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH11_Device_Xb_B:** DMA CH 11 PARAM 6: Device B block width (Xb)

15.8.448 reg_isp_dma_DMA_CH12_Device_Xb_B_type (isp_dma_DMA_CH12_Device_Xb_B)—Offset 41630h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_Device_Xb_B: [ISPMMADR] + 41630h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH12_Device_Xb_B	DMA_CH12_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH12_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH12_Device_Xb_B:** DMA CH 12 PARAM 6: Device B block width (Xb)

15.8.449 reg_isp_dma_DMA_CH13_Device_Xb_B_type (isp_dma_DMA_CH13_Device_Xb_B)—Offset 41634h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_Device_Xb_B: [ISPMMADR] + 41634h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH13_Device_Xb_B	DMA_CH13_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH13_Device_Xb_B:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH13_Device_Xb_B:** DMA CH 13 PARAM 6: Device B block width (Xb)

15.8.450 reg_isp_dma_DMA_CH14_Device_Xb_B_type (isp_dma_DMA_CH14_Device_Xb_B)—Offset 41638h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH14_Device_Xb_B: [ISPMMADR] + 41638h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH14_Device_Xb_B	DMA_CH14_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH14_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH14_Device_Xb_B:** DMA CH 14 PARAM 6: Device B block width (Xb)

15.8.451 reg_isp_dma_DMA_CH15_Device_Xb_B_type (isp_dma_DMA_CH15_Device_Xb_B)—Offset 4163Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH15_Device_Xb_B: [ISPMMADR] + 4163Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH15_Device_Xb_B																DMA_CH15_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH15_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH15_Device_Xb_B:** DMA CH 15 PARAM 6: Device B block width (Xb)

15.8.452 reg_isp_dma_DMA_CH16_Device_Xb_B_type (isp_dma_DMA_CH16_Device_Xb_B)—Offset 41640h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH16_Device_Xb_B: [ISPMMADR] + 41640h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH16_Device_Xb_B																DMA_CH16_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH16_Device_Xb_B:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH16_Device_Xb_B:** DMA CH 16 PARAM 6: Device B block width (Xb)

15.8.453 reg_isp_dma_DMA_CH17_Device_Xb_B_type (isp_dma_DMA_CH17_Device_Xb_B)—Offset 41644h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH17_Device_Xb_B: [ISPMMADR] + 41644h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: unused_DMA_CH17_Device_Xb_B
Bits 15:0: DMA_CH17_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH17_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH17_Device_Xb_B:** DMA CH 17 PARAM 6: Device B block width (Xb)

15.8.454 reg_isp_dma_DMA_CH18_Device_Xb_B_type (isp_dma_DMA_CH18_Device_Xb_B)—Offset 41648h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH18_Device_Xb_B: [ISPMMADR] + 41648h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:16	Bits 15:0
unused_DMA_CH18_Device_Xb_B	DMA_CH18_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH18_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH18_Device_Xb_B:** DMA CH 18 PARAM 6: Device B block width (Xb)

15.8.455 reg_isp_dma_DMA_CH19_Device_Xb_B_type (isp_dma_DMA_CH19_Device_Xb_B)—Offset 4164Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_Device_Xb_B: [ISPMMADR] + 4164Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:16	Bits 15:0
unused_DMA_CH19_Device_Xb_B	DMA_CH19_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH19_Device_Xb_B:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH19_Device_Xb_B:** DMA CH 19 PARAM 6: Device B block width (Xb)

15.8.456 reg_isp_dma_DMA_CH20_Device_Xb_B_type (isp_dma_DMA_CH20_Device_Xb_B)—Offset 41650h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH20_Device_Xb_B: [ISPMMADR] + 41650h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH20_Device_Xb_B	DMA_CH20_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH20_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH20_Device_Xb_B:** DMA CH 20 PARAM 6: Device B block width (Xb)

15.8.457 reg_isp_dma_DMA_CH21_Device_Xb_B_type (isp_dma_DMA_CH21_Device_Xb_B)—Offset 41654h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH21_Device_Xb_B: [ISPMMADR] + 41654h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH21_Device_Xb_B																DMA_CH21_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH21_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH21_Device_Xb_B:** DMA CH 21 PARAM 6: Device B block width (Xb)

15.8.458 reg_isp_dma_DMA_CH22_Device_Xb_B_type (isp_dma_DMA_CH22_Device_Xb_B)—Offset 41658h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH22_Device_Xb_B: [ISPMMADR] + 41658h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH22_Device_Xb_B																DMA_CH22_Device_Xb_B															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH22_Device_Xb_B:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH22_Device_Xb_B:** DMA CH 22 PARAM 6: Device B block width (Xb)

15.8.459 reg_isp_dma_DMA_CH23_Device_Xb_B_type (isp_dma_DMA_CH23_Device_Xb_B)—Offset 4165Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH23_Device_Xb_B: [ISPMMADR] + 4165Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: unused_DMA_CH23_Device_Xb_B
Bits 15:0: DMA_CH23_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH23_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH23_Device_Xb_B:** DMA CH 23 PARAM 6: Device B block width (Xb)

15.8.460 reg_isp_dma_DMA_CH24_Device_Xb_B_type (isp_dma_DMA_CH24_Device_Xb_B)—Offset 41660h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH24_Device_Xb_B: [ISPMMADR] + 41660h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH24_Device_Xb_B	DMA_CH24_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH24_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH24_Device_Xb_B:** DMA CH 24 PARAM 6: Device B block width (Xb)

15.8.461 reg_isp_dma_DMA_CH25_Device_Xb_B_type (isp_dma_DMA_CH25_Device_Xb_B)—Offset 41664h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_Device_Xb_B: [ISPMMADR] + 41664h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH25_Device_Xb_B	DMA_CH25_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH25_Device_Xb_B:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH25_Device_Xb_B:** DMA CH 25 PARAM 6: Device B block width (Xb)

15.8.462 reg_isp_dma_DMA_CH26_Device_Xb_B_type (isp_dma_DMA_CH26_Device_Xb_B)—Offset 41668h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH26_Device_Xb_B: [ISPMMADR] + 41668h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH26_Device_Xb_B (bits 31:16)
DMA_CH26_Device_Xb_B (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH26_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH26_Device_Xb_B:** DMA CH 26 PARAM 6: Device B block width (Xb)

15.8.463 reg_isp_dma_DMA_CH27_Device_Xb_B_type (isp_dma_DMA_CH27_Device_Xb_B)—Offset 4166Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH27_Device_Xb_B: [ISPMMADR] + 4166Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH27_Device_Xb_B

DMA_CH27_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH27_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH27_Device_Xb_B:** DMA CH 27 PARAM 6: Device B block width (Xb)

15.8.464 reg_isp_dma_DMA_CH28_Device_Xb_B_type (isp_dma_DMA_CH28_Device_Xb_B)—Offset 41670h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_Device_Xb_B: [ISPMMADR] + 41670h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH28_Device_Xb_B

DMA_CH28_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH28_Device_Xb_B:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_CH28_Device_Xb_B:** DMA CH 28 PARAM 6: Device B block width (Xb)

15.8.465 reg_isp_dma_DMA_CH29_Device_Xb_B_type (isp_dma_DMA_CH29_Device_Xb_B)—Offset 41674h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH29_Device_Xb_B: [ISPMMADR] + 41674h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH29_Device_Xb_B	DMA_CH29_Device_Xb_B

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH29_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH29_Device_Xb_B:** DMA CH 29 PARAM 6: Device B block width (Xb)

15.8.466 reg_isp_dma_DMA_CH31_Device_Xb_B_type (isp_dma_DMA_CH31_Device_Xb_B)—Offset 41678h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH31_Device_Xb_B: [ISPMMADR] + 41678h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH31_Device_Xb_B (31:16) | DMA_CH31_Device_Xb_B (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH31_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH31_Device_Xb_B:** DMA CH 31 PARAM 6: Device B block width (Xb)

15.8.467 reg_isp_dma_DMA_CH0_Yb_type (isp_dma_DMA_CH0_Yb)—Offset 41700h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH0_Yb: [ISPMMADR] + 41700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH0_Yb (31:16) | DMA_CH0_Yb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Yb:** Unused
15:0	0h RO	**DMA_CH0_Yb:** DMA CH 0 PARAM 7: block Height (Yb)

15.8.468 reg_isp_dma_DMA_CH1_Yb_type (isp_dma_DMA_CH1_Yb)—Offset 41704h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH1_Yb: [ISPMMADR] + 41704h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:16	15:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
unused_DMA_CH1_Yb	DMA_CH1_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH1_Yb:** Unused
15:0	0h RO	**DMA_CH1_Yb:** DMA CH 1 PARAM 7: block Height (Yb)

15.8.469 reg_isp_dma_DMA_CH2_Yb_type (isp_dma_DMA_CH2_Yb)—Offset 41708h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH2_Yb: [ISPMMADR] + 41708h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:16	15:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
unused_DMA_CH2_Yb	DMA_CH2_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH2_Yb:** Unused
15:0	0h RO	**DMA_CH2_Yb:** DMA CH 2 PARAM 7: block Height (Yb)

15.8.470 reg_isp_dma_DMA_CH3_Yb_type (isp_dma_DMA_CH3_Yb)—Offset 4170Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_Yb: [ISPMMADR] + 4170Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH3_Yb	DMA_CH3_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH3_Yb:** Unused
15:0	0h RO	**DMA_CH3_Yb:** DMA CH 3 PARAM 7: block Height (Yb)

15.8.471 reg_isp_dma_DMA_CH4_Yb_type (isp_dma_DMA_CH4_Yb)—Offset 41710h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_Yb: [ISPMMADR] + 41710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH4_Yb																DMA_CH4_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH4_Yb:** Unused
15:0	0h RO	**DMA_CH4_Yb:** DMA CH 4 PARAM 7: block Height (Yb)

15.8.472 reg_isp_dma_DMA_CH5_Yb_type (isp_dma_DMA_CH5_Yb)—Offset 41714h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH5_Yb: [ISPMMADR] + 41714h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH5_Yb																DMA_CH5_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH5_Yb:** Unused
15:0	0h RO	**DMA_CH5_Yb:** DMA CH 5 PARAM 7: block Height (Yb)

15.8.473 reg_isp_dma_DMA_CH6_Yb_type (isp_dma_DMA_CH6_Yb)—Offset 41718h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH6_Yb: [ISPMMADR] + 41718h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH6_Yb																DMA_CH6_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH6_Yb:** Unused
15:0	0h RO	**DMA_CH6_Yb:** DMA CH 6 PARAM 7: block Height (Yb)

15.8.474 reg_isp_dma_DMA_CH7_Yb_type (isp_dma_DMA_CH7_Yb)—Offset 4171Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH7_Yb: [ISPMMADR] + 4171Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH7_Yb																DMA_CH7_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH7_Yb:** Unused
15:0	0h RO	**DMA_CH7_Yb:** DMA CH 7 PARAM 7: block Height (Yb)

15.8.475 reg_isp_dma_DMA_CH8_Yb_type (isp_dma_DMA_CH8_Yb)—Offset 41720h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH8_Yb: [ISPMMADR] + 41720h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH8_Yb

DMA_CH8_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH8_Yb:** Unused
15:0	0h RO	**DMA_CH8_Yb:** DMA CH 8 PARAM 7: block Height (Yb)

15.8.476 reg_isp_dma_DMA_CH9_Yb_type (isp_dma_DMA_CH9_Yb)—Offset 41724h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH9_Yb: [ISPMMADR] + 41724h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH9_Yb

DMA_CH9_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH9_Yb:** Unused
15:0	0h RO	**DMA_CH9_Yb:** DMA CH 9 PARAM 7: block Height (Yb)

15.8.477 reg_isp_dma_DMA_CH10_Yb_type (isp_dma_DMA_CH10_Yb)—Offset 41728h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH10_Yb: [ISPMMADR] + 41728h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH10_Yb																DMA_CH10_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH10_Yb:** Unused
15:0	0h RO	**DMA_CH10_Yb:** DMA CH 10 PARAM 7: block Height (Yb)

15.8.478 reg_isp_dma_DMA_CH11_Yb_type (isp_dma_DMA_CH11_Yb)—Offset 4172Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH11_Yb: [ISPMMADR] + 4172Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH11_Yb | DMA_CH11_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH11_Yb:** Unused
15:0	0h RO	**DMA_CH11_Yb:** DMA CH 11 PARAM 7: block Height (Yb)

15.8.479 reg_isp_dma_DMA_CH12_Yb_type (isp_dma_DMA_CH12_Yb)—Offset 41730h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_Yb: [ISPMMADR] + 41730h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH12_Yb | DMA_CH12_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH12_Yb:** Unused
15:0	0h RO	**DMA_CH12_Yb:** DMA CH 12 PARAM 7: block Height (Yb)

15.8.480 reg_isp_dma_DMA_CH13_Yb_type (isp_dma_DMA_CH13_Yb)—Offset 41734h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_Yb: [ISPMMADR] + 41734h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH13_Yb (bits 31:16), DMA_CH13_Yb (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH13_Yb:** Unused
15:0	0h RO	**DMA_CH13_Yb:** DMA CH 13 PARAM 7: block Height (Yb)

15.8.481 reg_isp_dma_DMA_CH14_Yb_type (isp_dma_DMA_CH14_Yb)—Offset 41738h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_Yb: [ISPMMADR] + 41738h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH14_Yb (bits 31:16), DMA_CH14_Yb (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH14_Yb:** Unused
15:0	0h RO	**DMA_CH14_Yb:** DMA CH 14 PARAM 7: block Height (Yb)

15.8.482 reg_isp_dma_DMA_CH15_Yb_type (isp_dma_DMA_CH15_Yb)—Offset 4173Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH15_Yb: [ISPMMADR] + 4173Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:16	15:0
0000 0000 0000 0000	0000 0000 0000 0000
unused_DMA_CH15_Yb	DMA_CH15_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH15_Yb:** Unused
15:0	0h RO	**DMA_CH15_Yb:** DMA CH 15 PARAM 7: block Height (Yb)

15.8.483 reg_isp_dma_DMA_CH16_Yb_type (isp_dma_DMA_CH16_Yb)—Offset 41740h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH16_Yb: [ISPMMADR] + 41740h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:16	15:0
0000 0000 0000 0000	0000 0000 0000 0000
unused_DMA_CH16_Yb	DMA_CH16_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH16_Yb:** Unused
15:0	0h RO	**DMA_CH16_Yb:** DMA CH 16 PARAM 7: block Height (Yb)

15.8.484 reg_isp_dma_DMA_CH17_Yb_type (isp_dma_DMA_CH17_Yb)—Offset 41744h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_Yb: [ISPMMADR] + 41744h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH17_Yb	DMA_CH17_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH17_Yb:** Unused
15:0	0h RO	**DMA_CH17_Yb:** DMA CH 17 PARAM 7: block Height (Yb)

15.8.485 reg_isp_dma_DMA_CH18_Yb_type (isp_dma_DMA_CH18_Yb)—Offset 41748h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_Yb: [ISPMMADR] + 41748h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH18_Yb	DMA_CH18_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH18_Yb:** Unused
15:0	0h RO	**DMA_CH18_Yb:** DMA CH 18 PARAM 7: block Height (Yb)

15.8.486 reg_isp_dma_DMA_CH19_Yb_type (isp_dma_DMA_CH19_Yb)—Offset 4174Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_Yb: [ISPMMADR] + 4174Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
unused_DMA_CH19_Yb	DMA_CH19_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH19_Yb:** Unused
15:0	0h RO	**DMA_CH19_Yb:** DMA CH 19 PARAM 7: block Height (Yb)

15.8.487 reg_isp_dma_DMA_CH20_Yb_type (isp_dma_DMA_CH20_Yb)—Offset 41750h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_Yb: [ISPMMADR] + 41750h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH20_Yb | DMA_CH20_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH20_Yb:** Unused
15:0	0h RO	**DMA_CH20_Yb:** DMA CH 20 PARAM 7: block Height (Yb)

15.8.488 reg_isp_dma_DMA_CH21_Yb_type (isp_dma_DMA_CH21_Yb)—Offset 41754h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_Yb: [ISPMMADR] + 41754h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH21_Yb | DMA_CH21_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH21_Yb:** Unused
15:0	0h RO	**DMA_CH21_Yb:** DMA CH 21 PARAM 7: block Height (Yb)

15.8.489 reg_isp_dma_DMA_CH22_Yb_type (isp_dma_DMA_CH22_Yb)—Offset 41758h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH22_Yb: [ISPMMADR] + 41758h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH22_Yb (bits 31:16) | DMA_CH22_Yb (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH22_Yb:** Unused
15:0	0h RO	**DMA_CH22_Yb:** DMA CH 22 PARAM 7: block Height (Yb)

15.8.490 reg_isp_dma_DMA_CH23_Yb_type (isp_dma_DMA_CH23_Yb)—Offset 4175Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH23_Yb: [ISPMMADR] + 4175Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH23_Yb (bits 31:16) | DMA_CH23_Yb (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH23_Yb:** Unused
15:0	0h RO	**DMA_CH23_Yb:** DMA CH 23 PARAM 7: block Height (Yb)

15.8.491 reg_isp_dma_DMA_CH24_Yb_type (isp_dma_DMA_CH24_Yb)—Offset 41760h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH24_Yb: [ISPMMADR] + 41760h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_CH24_Yb	DMA_CH24_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH24_Yb:** Unused
15:0	0h RO	**DMA_CH24_Yb:** DMA CH 24 PARAM 7: block Height (Yb)

15.8.492 reg_isp_dma_DMA_CH25_Yb_type (isp_dma_DMA_CH25_Yb)—Offset 41764h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_CH25_Yb: [ISPMMADR] + 41764h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH25_Yb																DMA_CH25_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH25_Yb:** Unused
15:0	0h RO	**DMA_CH25_Yb:** DMA CH 25 PARAM 7: block Height (Yb)

15.8.493 reg_isp_dma_DMA_CH26_Yb_type (isp_dma_DMA_CH26_Yb)—Offset 41768h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_Yb: [ISPMMADR] + 41768h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH26_Yb																DMA_CH26_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH26_Yb:** Unused
15:0	0h RO	**DMA_CH26_Yb:** DMA CH 26 PARAM 7: block Height (Yb)

15.8.494 reg_isp_dma_DMA_CH27_Yb_type (isp_dma_DMA_CH27_Yb)—Offset 4176Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_Yb: [ISPMMADR] + 4176Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH27_Yb | DMA_CH27_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH27_Yb:** Unused
15:0	0h RO	**DMA_CH27_Yb:** DMA CH 27 PARAM 7: block Height (Yb)

15.8.495 reg_isp_dma_DMA_CH28_Yb_type (isp_dma_DMA_CH28_Yb)—Offset 41770h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_Yb: [ISPMMADR] + 41770h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH28_Yb | DMA_CH28_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH28_Yb:** Unused
15:0	0h RO	**DMA_CH28_Yb:** DMA CH 28 PARAM 7: block Height (Yb)

15.8.496 reg_isp_dma_DMA_CH29_Yb_type (isp_dma_DMA_CH29_Yb)—Offset 41774h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_Yb: [ISPMMADR] + 41774h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH29_Yb (31:16) | DMA_CH29_Yb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH29_Yb:** Unused
15:0	0h RO	**DMA_CH29_Yb:** DMA CH 29 PARAM 7: block Height (Yb)

15.8.497 reg_isp_dma_DMA_CH31_Yb_type (isp_dma_DMA_CH31_Yb)—Offset 4177Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_Yb: [ISPMMADR] + 4177Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH31_Yb (31:16) | DMA_CH31_Yb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH31_Yb:** Unused
15:0	0h RO	**DMA_CH31_Yb:** DMA CH 31 PARAM 7: block Height (Yb)

15.8.498 reg_isp_dma_DMA_CH0_pending_command_type (isp_dma_DMA_CH0_pending_command)—Offset 41800h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH0_pending_command: [ISPMMADR] + 41800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4: unused_DMA_CH0_pending_command; bits 3:0: DMA_CH0_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH0_pending_command:** Unused
3:0	0h RO	**DMA_CH0_pending_command:** DMA CH 0 PARAM 8: Pending commands which will use channel 0

15.8.499 reg_isp_dma_DMA_CH1_pending_command_type (isp_dma_DMA_CH1_pending_command)—Offset 41804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH1_pending_command: [ISPMMADR] + 41804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH1_pending_command (bits 31:4); DMA_CH1_pending_command (bits 3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH1_pending_command:** Unused
3:0	0h RO	**DMA_CH1_pending_command:** DMA CH 1 PARAM 8: Pending commands which will use channel 1

15.8.500 reg_isp_dma_DMA_CH2_pending_command_type (isp_dma_DMA_CH2_pending_command)—Offset 41808h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH2_pending_command: [ISPMMADR] + 41808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH2_pending_command (bits 31:4); DMA_CH2_pending_command (bits 3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH2_pending_command:** Unused
3:0	0h RO	**DMA_CH2_pending_command:** DMA CH 2 PARAM 8: Pending commands which will use channel 2

15.8.501 reg_isp_dma_DMA_CH3_pending_command_type (isp_dma_DMA_CH3_pending_command)—Offset 4180Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH3_pending_command: [ISPMMADR] + 4180Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH3_pending_command (bits 31:4); DMA_CH3_pending_command (bits 3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH3_pending_command:** Unused
3:0	0h RO	**DMA_CH3_pending_command:** DMA CH 0 PARAM 8: Pending commands which will use channel 3

15.8.502 reg_isp_dma_DMA_CH4_pending_command_type (isp_dma_DMA_CH4_pending_command)—Offset 41810h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH4_pending_command: [ISPMMADR] + 41810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:4	3:0
unused_DMA_CH4_pending_command	DMA_CH4_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH4_pending_command:** Unused
3:0	0h RO	**DMA_CH4_pending_command:** DMA CH 4 PARAM 8: Pending commands which will use channel 4

15.8.503 reg_isp_dma_DMA_CH5_pending_command_type (isp_dma_DMA_CH5_pending_command)—Offset 41814h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH5_pending_command: [ISPMMADR] + 41814h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:4	3:0
unused_DMA_CH5_pending_command	DMA_CH5_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH5_pending_command:** Unused
3:0	0h RO	**DMA_CH5_pending_command:** DMA CH 5 PARAM 8: Pending commands which will use channel 5

15.8.504 reg_isp_dma_DMA_CH6_pending_command_type (isp_dma_DMA_CH6_pending_command)—Offset 41818h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH6_pending_command: [ISPMMADR] + 41818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
unused_DMA_CH6_pending_command	DMA_CH6_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH6_pending_command:** Unused
3:0	0h RO	**DMA_CH6_pending_command:** DMA CH 6 PARAM 8: Pending commands which will use channel 6

15.8.505 reg_isp_dma_DMA_CH7_pending_command_type (isp_dma_DMA_CH7_pending_command)—Offset 4181Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH7_pending_command: [ISPMMADR] + 4181Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH7_pending_command																												DMA_CH7_pending_command			

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH7_pending_command:** Unused
3:0	0h RO	**DMA_CH7_pending_command:** DMA CH 7 PARAM 8: Pending commands which will use channel 7

15.8.506 reg_isp_dma_DMA_CH8_pending_command_type (isp_dma_DMA_CH8_pending_command)—Offset 41820h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH8_pending_command: [ISPMMADR] + 41820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH8_pending_command																												DMA_CH8_pending_command			

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH8_pending_command:** Unused
3:0	0h RO	**DMA_CH8_pending_command:** DMA CH 8 PARAM 8: Pending commands which will use channel 6

15.8.507 reg_isp_dma_DMA_CH9_pending_command_type (isp_dma_DMA_CH9_pending_command)—Offset 41824h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH9_pending_command: [ISPMMADR] + 41824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
unused_DMA_CH9_pending_command	DMA_CH9_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH9_pending_command:** Unused
3:0	0h RO	**DMA_CH9_pending_command:** DMA CH 9 PARAM 8: Pending commands which will use channel 7

15.8.508 reg_isp_dma_DMA_CH10_pending_command_type (isp_dma_DMA_CH10_pending_command)—Offset 41828h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH10_pending_command: [ISPMMADR] + 41828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH10_pending_command (31:4), DMA_CH10_pending_command (3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH10_pending_command:** Unused
3:0	0h RO	**DMA_CH10_pending_command:** DMA CH 10 PARAM 8: Pending commands which will use channel 0

15.8.509 reg_isp_dma_DMA_CH11_pending_command_type (isp_dma_DMA_CH11_pending_command)—Offset 4182Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH11_pending_command: [ISPMMADR] + 4182Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH11_pending_command (31:4), DMA_CH11_pending_command (3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH11_pending_command:** Unused
3:0	0h RO	**DMA_CH11_pending_command:** DMA CH 11 PARAM 8: Pending commands which will use channel 1

15.8.510 reg_isp_dma_DMA_CH12_pending_command_type (isp_dma_DMA_CH12_pending_command)—Offset 41830h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH12_pending_command: [ISPMMADR] + 41830h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH12_pending_command

DMA_CH12_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH12_pending_command:** Unused
3:0	0h RO	**DMA_CH12_pending_command:** DMA CH 12 PARAM 8: Pending commands which will use channel 2

15.8.511 reg_isp_dma_DMA_CH13_pending_command_type (isp_dma_DMA_CH13_pending_command)—Offset 41834h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH13_pending_command: [ISPMMADR] + 41834h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
unused_DMA_CH13_pending_command							DMA_CH13_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH13_pending_command:** Unused
3:0	0h RO	**DMA_CH13_pending_command:** DMA CH 10 PARAM 8: Pending commands which will use channel 3

15.8.512 reg_isp_dma_DMA_CH14_pending_command_type (isp_dma_DMA_CH14_pending_command)—Offset 41838h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH14_pending_command: [ISPMMADR] + 41838h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
unused_DMA_CH14_pending_command							DMA_CH14_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH14_pending_command:** Unused
3:0	0h RO	**DMA_CH14_pending_command:** DMA CH 14 PARAM 8: Pending commands which will use channel 4

15.8.513 reg_isp_dma_DMA_CH15_pending_command_type (isp_dma_DMA_CH15_pending_command)—Offset 4183Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH15_pending_command: [ISPMMADR] + 4183Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH15_pending_command

DMA_CH15_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH15_pending_command:** Unused
3:0	0h RO	**DMA_CH15_pending_command:** DMA CH 15 PARAM 8: Pending commands which will use channel 5

15.8.514 reg_isp_dma_DMA_CH16_pending_command_type (isp_dma_DMA_CH16_pending_command)—Offset 41840h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH16_pending_command: [ISPMMADR] + 41840h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
unused_DMA_CH16_pending_command	DMA_CH16_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH16_pending_command:** Unused
3:0	0h RO	**DMA_CH16_pending_command:** DMA CH 16 PARAM 8: Pending commands which will use channel 6

15.8.515 reg_isp_dma_DMA_CH17_pending_command_type (isp_dma_DMA_CH17_pending_command)—Offset 41844h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH17_pending_command: [ISPMMADR] + 41844h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
unused_DMA_CH17_pending_command	DMA_CH17_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH17_pending_command:** Unused
3:0	0h RO	**DMA_CH17_pending_command:** DMA CH 17 PARAM 8: Pending commands which will use channel 7

15.8.516 reg_isp_dma_DMA_CH18_pending_command_type (isp_dma_DMA_CH18_pending_command)—Offset 41848h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH18_pending_command: [ISPMMADR] + 41848h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
unused_DMA_CH18_pending_command	DMA_CH18_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH18_pending_command:** Unused
3:0	0h RO	**DMA_CH18_pending_command:** DMA CH 18 PARAM 8: Pending commands which will use channel 6

15.8.517 reg_isp_dma_DMA_CH19_pending_command_type (isp_dma_DMA_CH19_pending_command)—Offset 4184Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH19_pending_command: [ISPMMADR] + 4184Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH19_pending_command (31:4), DMA_CH19_pending_command (3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH19_pending_command:** Unused
3:0	0h RO	**DMA_CH19_pending_command:** DMA CH 19 PARAM 8: Pending commands which will use channel 7

15.8.518 reg_isp_dma_DMA_CH20_pending_command_type (isp_dma_DMA_CH20_pending_command)—Offset 41850h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH20_pending_command: [ISPMMADR] + 41850h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH20_pending_command (31:4), DMA_CH20_pending_command (3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH20_pending_command:** Unused
3:0	0h RO	**DMA_CH20_pending_command:** DMA CH 20 PARAM 8: Pending commands which will use channel 0

15.8.519 reg_isp_dma_DMA_CH21_pending_command_type (isp_dma_DMA_CH21_pending_command)—Offset 41854h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH21_pending_command: [ISPMMADR] + 41854h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:4	3:0
Default	0000 0000 0000 0000 0000 0000 0000	0000
Field	unused_DMA_CH21_pending_command	DMA_CH21_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH21_pending_command:** Unused
3:0	0h RO	**DMA_CH21_pending_command:** DMA CH 21 PARAM 8: Pending commands which will use channel 1

15.8.520 reg_isp_dma_DMA_CH22_pending_command_type (isp_dma_DMA_CH22_pending_command)—Offset 41858h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH22_pending_command: [ISPMMADR] + 41858h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH22_pending_command | DMA_CH22_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH22_pending_command:** Unused
3:0	0h RO	**DMA_CH22_pending_command:** DMA CH 22 PARAM 8: Pending commands which will use channel 2

15.8.521 reg_isp_dma_DMA_CH23_pending_command_type (isp_dma_DMA_CH23_pending_command)—Offset 4185Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH23_pending_command: [ISPMMADR] + 4185Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_CH23_pending_command | DMA_CH23_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH23_pending_command:** Unused
3:0	0h RO	**DMA_CH23_pending_command:** DMA CH 20 PARAM 8: Pending commands which will use channel 3

15.8.522 reg_isp_dma_DMA_CH24_pending_command_type (isp_dma_DMA_CH24_pending_command)—Offset 41860h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH24_pending_command: [ISPMMADR] + 41860h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

31:4	3:0
unused_DMA_CH24_pending_command	DMA_CH24_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH24_pending_command:** Unused
3:0	0h RO	**DMA_CH24_pending_command:** DMA CH 24 PARAM 8: Pending commands which will use channel 4

15.8.523 reg_isp_dma_DMA_CH25_pending_command_type (isp_dma_DMA_CH25_pending_command)—Offset 41864h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH25_pending_command: [ISPMMADR] + 41864h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH25_pending_command (bits 31:4), DMA_CH25_pending_command (bits 3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH25_pending_command:** Unused
3:0	0h RO	**DMA_CH25_pending_command:** DMA CH 25 PARAM 8: Pending commands which will use channel 5

15.8.524 reg_isp_dma_DMA_CH26_pending_command_type (isp_dma_DMA_CH26_pending_command)—Offset 41868h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH26_pending_command: [ISPMMADR] + 41868h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_CH26_pending_command (bits 31:4), DMA_CH26_pending_command (bits 3:0)

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH26_pending_command:** Unused
3:0	0h RO	**DMA_CH26_pending_command:** DMA CH 26 PARAM 8: Pending commands which will use channel 6

15.8.525 reg_isp_dma_DMA_CH27_pending_command_type (isp_dma_DMA_CH27_pending_command)—Offset 4186Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH27_pending_command: [ISPMMADR] + 4186Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31–4	3–0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0
unused_DMA_CH27_pending_command	DMA_CH27_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH27_pending_command:** Unused
3:0	0h RO	**DMA_CH27_pending_command:** DMA CH 27 PARAM 8: Pending commands which will use channel 7

15.8.526 reg_isp_dma_DMA_CH28_pending_command_type (isp_dma_DMA_CH28_pending_command)—Offset 41870h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH28_pending_command: [ISPMMADR] + 41870h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
unused_DMA_CH28_pending_command							DMA_CH28_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH28_pending_command:** Unused
3:0	0h RO	**DMA_CH28_pending_command:** DMA CH 28 PARAM 8: Pending commands which will use channel 6

15.8.527 reg_isp_dma_DMA_CH29_pending_command_type (isp_dma_DMA_CH29_pending_command)—Offset 41874h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH29_pending_command: [ISPMMADR] + 41874h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
unused_DMA_CH29_pending_command							DMA_CH29_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH29_pending_command:** Unused
3:0	0h RO	**DMA_CH29_pending_command:** DMA CH 29 PARAM 8: Pending commands which will use channel 7

15.8.528 reg_isp_dma_DMA_CH30_pending_command_type (isp_dma_DMA_CH30_pending_command)—Offset 41878h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH30_pending_command: [ISPMMADR] + 41878h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
unused_DMA_CH30_pending_command	DMA_CH30_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH30_pending_command:** Unused
3:0	0h RO	**DMA_CH30_pending_command:** DMA CH 30 PARAM 8: Pending commands which will use channel 6

15.8.529 reg_isp_dma_DMA_CH31_pending_command_type (isp_dma_DMA_CH31_pending_command)—Offset 4187Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_CH31_pending_command: [ISPMMADR] + 4187Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4: unused_DMA_CH31_pending_command; Bits 3:0: DMA_CH31_pending_command

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH31_pending_command:** Unused
3:0	0h RO	**DMA_CH31_pending_command:** DMA CH 30 PARAM 8: Pending commands which will use channel 7

15.8.530 reg_isp_dma_DMA_command_token_type (isp_dma_DMA_command_token)—Offset 42000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_command_token: [ISPMMADR] + 42000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:0: DMA_command_token

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_token:** Pending or last executed command token

15.8.531 reg_isp_dma_DMA_command_src_addr_type (isp_dma_DMA_command_src_addr)—Offset 42004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_command_src_addr: [ISPMMADR] + 42004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_command_src_addr

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_src_addr:** Source address of the pending or last executed command token

15.8.532 reg_isp_dma_DMA_command_dst_addr_type (isp_dma_DMA_command_dst_addr)—Offset 42008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_command_dst_addr: [ISPMMADR] + 42008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_command_dst_addr

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_dst_addr:** Destination address of the pending or last executed command token

15.8.533 reg_isp_dma_DMA_command_ctrl_id_type (isp_dma_DMA_command_ctrl_id)—Offset 4200Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_command_ctrl_id: [ISPMMADR] + 4200Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1: unused_DMA_command_ctrl_id
Bit 0: DMA_command_ctrl_id

Bit Range	Default & Access	Description
31:1	0h RW	**unused_DMA_command_ctrl_id:** Unused
0	0h RO	**DMA_command_ctrl_id:** Controller id of the pending or last executed command token

15.8.534 reg_isp_dma_DMA_FSM_Ctrl_status_type (isp_dma_DMA_FSM_Ctrl_status)—Offset 42010h

DMA FSM Control state and flags

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_status: [ISPMMADR] + 42010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31	28	24	20	16	12	8	4	0

31:8	7:4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	1
unused_DMA_FSM_Ctrl_status	Ctrl_state	Error_flag	Stall_flag	Run_flag	Idle_flag

Bit Range	Default & Access	Description
31:8	0h RW	**unused_DMA_FSM_Ctrl_status:** Unused
7:4	0h RO	**Ctrl_state:** FSM control state: 0)Idle -- 1)req_rcv -- 2)rcv -- 3)rcv_req -- 4)init
3	0h RO	**Error_flag:** Error flag
2	0h RO	**Stall_flag:** Stall flag
1	0h RO	**Run_flag:** Run flag
0	1h RO	**Idle_flag:** Idle flag

15.8.535 reg_isp_dma_DMA_FSM_Pack_status_type (isp_dma_DMA_FSM_Pack_status)—Offset 42014h

DMA FSM Pack state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Pack_status: [ISPMMADR] + 42014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3	2	1	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	1
unused_DMA_FSM_Pack_status							Error_flag	Stall_flag	Run_flag	Idle_flag

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_FSM_Pack_status:** Unused
3	0h RO	**Error_flag:** Error flag
2	0h RO	**Stall_flag:** Stall flag
1	0h RO	**Run_flag:** Run flag
0	1h RO	**Idle_flag:** Idle flag

15.8.536 reg_isp_dma_DMA_FSM_request_status_type (isp_dma_DMA_FSM_request_status)—Offset 42018h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_request_status: [ISPMMADR] + 42018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–2	1–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0
unused_DMA_FSM_request_status								DMA_FSM_request_status

Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_request_status:** Unused
1:0	0h RO	**DMA_FSM_request_status:** DMA FSM Request state: 0)Idle -- 1)req -- 2)Next line

15.8.537 reg_isp_dma_DMA_FSM_write_status_type (isp_dma_DMA_FSM_write_status)—Offset 4201Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_write_status: [ISPMMADR] + 4201Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_write_status
DMA_FSM_write_status

Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_write_status:** Unused
1:0	0h RO	**DMA_FSM_write_status:** DMA FSM Write state: 0)Idle -- 1)req -- 2)Next line

15.8.538 reg_isp_dma_DMA_FSM_Ctrl_dev_idx_type (isp_dma_DMA_FSM_Ctrl_dev_idx)—Offset 42110h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_dev_idx: [ISPMMADR] + 42110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Ctrl_dev_idx
DMA_FSM_Ctrl_dev_idx

Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_Ctrl_dev_idx:** Unused
1:0	0h RO	**DMA_FSM_Ctrl_dev_idx:** DMA FSM Control request device idx

15.8.539 reg_isp_dma_DMA_FSM_Pack_cnt_Yb_type (isp_dma_DMA_FSM_Pack_cnt_Yb)—Offset 42114h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_Pack_cnt_Yb: [ISPMMADR] + 42114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Pack_cnt_Yb
DMA_FSM_Pack_cnt_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_cnt_Yb:** Unused
15:0	0h RO	**DMA_FSM_Pack_cnt_Yb:** DMA FSM pack counter height (Yb)

15.8.540 reg_isp_dma_DMA_FSM_Request_cnt_Yb_type (isp_dma_DMA_FSM_Request_cnt_Yb)—Offset 42118h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Request_cnt_Yb: [ISPMMADR] + 42118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:16	15:0
Default	0000 0000 0000 0000	0000 0000 0000 0000
Field	unused_DMA_FSM_Request_cnt_Yb	DMA_FSM_Request_cnt_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Request_cnt_Yb:** Unused
15:0	0h RO	**DMA_FSM_Request_cnt_Yb:** DMA FSM request counter height (Yb)

15.8.541 reg_isp_dma_DMA_FSM_Write_cnt_Y_type (isp_dma_DMA_FSM_Write_cnt_Y)—Offset 4211Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Write_cnt_Y: [ISPMMADR] + 4211Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Write_cnt_Y

DMA_FSM_Write_cnt_Y

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Write_cnt_Y:** Unused
15:0	0h RO	**DMA_FSM_Write_cnt_Y:** DMA FSM Write counter height (Yb)

15.8.542 reg_isp_dma_DMA_FSM_Ctrl_req_addr_type (isp_dma_DMA_FSM_Ctrl_req_addr)—Offset 42210h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_req_addr: [ISPMMADR] + 42210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_FSM_Ctrl_req_addr

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_req_addr:** DMA FSM Control request address

15.8.543 reg_isp_dma_DMA_FSM_Pack_req_cnt_Xb_type (isp_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 42214h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_Pack_req_cnt_Xb: [ISPMMADR] + 42214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: unused_DMA_FSM_Pack_req_cnt_Xb
Bits 15:0: DMA_FSM_Pack_req_cnt_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_req_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Pack_req_cnt_Xb:** DMA FSM pack request counter width (Xb)

15.8.544 reg_isp_dma_DMA_FSM_Request_cnt_Xb_type (isp_dma_DMA_FSM_Request_cnt_Xb)—Offset 42218h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_Request_cnt_Xb: [ISPMMADR] + 42218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Request_cnt_Xb																DMA_FSM_Request_cnt_Xb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Request_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Request_cnt_Xb:** DMA FSM Request counter width (Xb)

15.8.545 reg_isp_dma_DMA_FSM_Write_cnt_Xb_type (isp_dma_DMA_FSM_Write_cnt_Xb)—Offset 4221Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_Write_cnt_Xb: [ISPMMADR] + 4221Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Write_cnt_Xb																DMA_FSM_Write_cnt_Xb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Write_cnt_Xb:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_FSM_Write_cnt_Xb:** DMA FSM Write counter width (Xb)

15.8.546 reg_isp_dma_DMA_FSM_Ctrl_req_stride_type (isp_dma_DMA_FSM_Ctrl_req_stride)—Offset 42310h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_req_stride: [ISPMMADR] + 42310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_FSM_Ctrl_req_stride

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_req_stride:** DMA FSM Control request stride

15.8.547 reg_isp_dma_DMA_FSM_Pack_wr_cnt_Xb_type (isp_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 42314h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Pack_wr_cnt_Xb: [ISPMMADR] + 42314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_FSM_Pack_wr_cnt_Xb (31:16), DMA_FSM_Pack_wr_cnt_Xb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_wr_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Pack_wr_cnt_Xb:** DMA FSM pack write counter width (Xb)

15.8.548 reg_isp_dma_DMA_FSM_Req_remining_Xb_type (isp_dma_DMA_FSM_Req_remining_Xb)—Offset 42318h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Req_remining_Xb: [ISPMMADR] + 42318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_FSM_Req_remining_Xb (31:16), DMA_FSM_Req_remining_Xb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Req_remining_Xb:** Unused
15:0	0h RO	**DMA_FSM_Req_remining_Xb:** DMA FSM Request counter remaining word width

15.8.549 reg_isp_dma_DMA_FSM_Wr_remining_Xb_type (isp_dma_DMA_FSM_Wr_remining_Xb)—Offset 4231Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Wr_remining_Xb: [ISPMMADR] + 4231Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Wr_remining_Xb

DMA_FSM_Wr_remining_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Wr_remining_Xb:** Unused
15:0	0h RO	**DMA_FSM_Wr_remining_Xb:** DMA FSM Write counter remaining word width

15.8.550 reg_isp_dma_DMA_FSM_Ctrl_req_Xb_type (isp_dma_DMA_FSM_Ctrl_req_Xb)—Offset 42410h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_req_Xb: [ISPMMADR] + 42410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

31:16	15:0
unused_DMA_FSM_Ctrl_req_Xb	DMA_FSM_Ctrl_req_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_req_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_req_Xb:** DMA FSM Control request width (Xb)

15.8.551 reg_isp_dma_DMA_FSM_Req_burst_cnt_type (isp_dma_DMA_FSM_Req_burst_cnt)—Offset 42418h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Req_burst_cnt: [ISPMMADR] + 42418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1

31:16	15:0
unused_DMA_FSM_Req_burst_cnt	DMA_FSM_Req_burst_cnt

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Req_burst_cnt:** Unused
15:0	FFFFh RO	**DMA_FSM_Req_burst_cnt:** DMA FSM Request word burst counter

15.8.552 reg_isp_dma_DMA_FSM_Wr_burst_cnt_type (isp_dma_DMA_FSM_Wr_burst_cnt)—Offset 4241Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Wr_burst_cnt: [ISPMMADR] + 4241Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

unused_DMA_FSM_Wr_burst_cnt (bits 31:16) | DMA_FSM_Wr_burst_cnt (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Wr_burst_cnt:** Unused
15:0	FFFFh RO	**DMA_FSM_Wr_burst_cnt:** DMA FSM Write word burst counter

15.8.553 reg_isp_dma_DMA_FSM_Ctrl_req_Yb_type (isp_dma_DMA_FSM_Ctrl_req_Yb)—Offset 42510h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_req_Yb: [ISPMMADR] + 42510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Ctrl_req_Yb																DMA_FSM_Ctrl_req_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_req_Yb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_req_Yb:** DMA FSM Control request height (Yb)

15.8.554 reg_isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx_type (isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 42610h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_Pack_req_dev_idx: [ISPMMADR] + 42610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Ctrl_Pack_req_dev_idx																														DMA_FSM_Ctrl_Pack_req_dev_idx	

Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_Ctrl_Pack_req_dev_idx:** Unused
1:0	0h RO	**DMA_FSM_Ctrl_Pack_req_dev_idx:** DMA FSM Control pack request device idx

15.8.555 reg_isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx_type (isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 42710h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx: [ISPMMADR] + 42710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:2: unused_DMA_FSM_Ctrl_Pack_wr_dev_idx
Bits 1:0: DMA_FSM_Ctrl_Pack_wr_dev_idx

Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_Ctrl_Pack_wr_dev_idx:** Unused
1:0	0h RO	**DMA_FSM_Ctrl_Pack_wr_dev_idx:** DMA FSM Control pack write device idx

15.8.556 reg_isp_dma_DMA_FSM_Ctrl_Wr_addr_type (isp_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 42810h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_Wr_addr: [ISPMMADR] + 42810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_FSM_Ctrl_Wr_addr

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_Wr_addr:** DMA FSM Control write address

15.8.557 reg_isp_dma_DMA_FSM_Ctrl_Wr_stride_type (isp_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 42910h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_Wr_stride: [ISPMMADR] + 42910h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_FSM_Ctrl_Wr_stride

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_Wr_stride:** DMA FSM Control write stride

15.8.558 reg_isp_dma_DMA_FSM_Ctrl_pack_req_Xb_type (isp_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 42A10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_req_Xb: [ISPMMADR] + 42A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_FSM_Ctrl_pack_req_Xb (31:16), DMA_FSM_Ctrl_pack_req_Xb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_req_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_req_Xb:** DMA FSM Control FSM Pack request width (Xb)

15.8.559 reg_isp_dma_DMA_FSM_Ctrl_pack_Yb_type (isp_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 42B10h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_Yb: [ISPMMADR] + 42B10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_FSM_Ctrl_pack_Yb (31:16), DMA_FSM_Ctrl_pack_Yb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_Yb:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_FSM_Ctrl_pack_Yb:** DMA FSM Control FSM Pack height (Yb)

15.8.560 reg_isp_dma_DMA_FSM_Ctrl_pack_wr_Xb_type (isp_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 42C10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_wr_Xb: [ISPMMADR] + 42C10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:16	15:0
Default	0000 0000 0000 0000	0000 0000 0000 0000
Field	unused_DMA_FSM_Ctrl_pack_wr_Xb	DMA_FSM_Ctrl_pack_wr_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_wr_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_wr_Xb:** DMA FSM Control FSM Pack write width (Xb)

15.8.561 reg_isp_dma_DMA_FSM_Ctrl_pack_req_elem_type (isp_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 42D10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_req_elem: [ISPMMADR] + 42D10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:7	Bits 6:0
unused_DMA_FSM_Ctrl_pack_req_elem	DMA_FSM_Ctrl_pack_req_elem

Bit Range	Default & Access	Description
31:7	0h RW	**unused_DMA_FSM_Ctrl_pack_req_elem:** Unused
6:0	0h RO	**DMA_FSM_Ctrl_pack_req_elem:** DMA FSM Control pack request element per word

15.8.562 reg_isp_dma_DMA_FSM_Ctrl_pack_wr_elem_type (isp_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 42E10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_wr_elem: [ISPMMADR] + 42E10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:7	Bits 6:0
unused_DMA_FSM_Ctrl_pack_wr_elem	DMA_FSM_Ctrl_pack_wr_elem

Bit Range	Default & Access	Description
31:7	0h RW	**unused_DMA_FSM_Ctrl_pack_wr_elem:** Unused
6:0	0h RO	**DMA_FSM_Ctrl_pack_wr_elem:** DMA FSM Control pack write element per word

15.8.563 reg_isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id_type (isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 42F10h

DMA FSM Control pack element sign zero extension and controller ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id: [ISPMMADR] + 42F10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:5	4	3:1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0	0
Field	unused_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id	ctrl_id	RSVD0	sign

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id:** Unused
4	0h RO	**ctrl_id:** Controller ID
3:1	0b RO	**RSVD0:** Reserved
0	0h RO	**sign:** element sign(1)/zero(0) extension

15.8.564 reg_isp_dma_Dev_Interf_0_req_side_type (isp_dma_Dev_Interf_0_req_side)—Offset 43000h

DMA Device interface 0 internal side status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_Dev_Interf_0_req_side: [ISPMMADR] + 43000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:4	3	2	1	0
Default	0000 0000 0000 0000 0000 0000 0000	0	0	0	0
Field	unused_Dev_Interf_0_req_side	ack_flag	run_flag	we_n_flag	cs_flag

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_0_req_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	0h RO	**run_flag:** Run flag
1	0h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

15.8.565 reg_isp_dma_Dev_Interf_1_req_side_type (isp_dma_Dev_Interf_1_req_side)—Offset 43004h

DMA Device interface 1 internal side status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_Dev_Interf_1_req_side: [ISPMMADR] + 43004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
unused_Dev_Interf_1_req_side																												ack_flag	run_flag	we_n_flag	cs_flag

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_1_req_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	1h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

15.8.566 reg_isp_dma_Dev_Interf_2_req_side_type (isp_dma_Dev_Interf_2_req_side)—Offset 43008h

DMA Device interface 2 internal side status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_2_req_side: [ISPMMADR] + 43008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
unused_Dev_Interf_2_req_side																												ack_flag	run_flag	we_n_flag	cs_flag

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_2_req_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	1h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

15.8.567 reg_isp_dma_Dev_Interf_0_snd_side_type (isp_dma_Dev_Interf_0_snd_side)—Offset 43100h

DMA Device interface 0 output side status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_0_snd_side: [ISPMMADR] + 43100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 31:4	Bit 3	Bit 2	Bit 1	Bit 0
unused_Dev_Interf_0_snd_side	ack_flag	run_flag	we_n_flag	cs_flag

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_0_snd_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	0h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

15.8.568 reg_isp_dma_Dev_Interf_1_snd_side_type (isp_dma_Dev_Interf_1_snd_side)—Offset 43104h

DMA Device interface 1 output side status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_Dev_Interf_1_snd_side: [ISPMMADR] + 43104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
unused_Dev_Interf_1_snd_side																												ack_flag	run_flag	we_n_flag	cs_flag

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_1_snd_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	1h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

15.8.569 reg_isp_dma_Dev_Interf_2_snd_side_type (isp_dma_Dev_Interf_2_snd_side)—Offset 43108h

DMA Device interface 2 output side status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_Dev_Interf_2_snd_side: [ISPMMADR] + 43108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
unused_Dev_Interf_2_snd_side																												ack_flag	run_flag	we_n_flag	cs_flag

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_2_snd_side:** Unused
3	0h RO	**ack_flag:** Ack flag
2	1h RO	**run_flag:** Run flag
1	1h RO	**we_n_flag:** We_n flag
0	0h RO	**cs_flag:** CS flag

15.8.570 reg_isp_dma_Dev_Interf_0_Fifo_status_type (isp_dma_Dev_Interf_0_Fifo_status)—Offset 43200h

Device Interface 0 Fifo status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_0_Fifo_status: [ISPMMADR] + 43200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 31:17	Bits 16:3	Bit 2	Bit 1	Bit 0
unused_Dev_Interf_0_Fifo_status	fifo_w_cnt	is_empty	is_full	will_be_full

Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_0_Fifo_status:** Unused
16:3	0h RO	**fifo_w_cnt:** Fifo word counter
2	1h RO	**is_empty:** Fifo is empty
1	0h RO	**is_full:** Fifo is full
0	0h RO	**will_be_full:** Fifo will be full

15.8.571 reg_isp_dma_Dev_Interf_1_Fifo_status_type (isp_dma_Dev_Interf_1_Fifo_status)—Offset 43204h

Device Interface 1 Fifo status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_1_Fifo_status: [ISPMMADR] + 43204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Fields: unused_Dev_Interf_1_Fifo_status (31:17), fifo_w_cnt (16:3), is_empty (2), is_full (1), will_be_full (0)

Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_1_Fifo_status:** Unused
16:3	0h RO	**fifo_w_cnt:** Fifo word counter
2	1h RO	**is_empty:** Fifo is empty
1	0h RO	**is_full:** Fifo is full
0	0h RO	**will_be_full:** Fifo will be full

15.8.572 reg_isp_dma_Dev_Interf_2_Fifo_status_type (isp_dma_Dev_Interf_2_Fifo_status)—Offset 43208h

Device Interface 2 Fifo status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_dma_Dev_Interf_2_Fifo_status: [ISPMMADR] + 43208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 31:17	Bits 16:3	Bit 2	Bit 1	Bit 0
unused_Dev_Interf_2_Fifo_status	fifo_w_cnt	is_empty	is_full	will_be_full

Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_2_Fifo_status:** Unused
16:3	0h RO	**fifo_w_cnt:** Fifo word counter
2	1h RO	**is_empty:** Fifo is empty
1	0h RO	**is_full:** Fifo is full
0	0h RO	**will_be_full:** Fifo will be full

15.8.573 reg_isp_dma_Dev_Interf_0_Req_complete_bust_type (isp_dma_Dev_Interf_0_Req_complete_bust)—Offset 43300h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_0_Req_complete_bust: [ISPMMADR] + 43300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_Dev_Interf_0_Req_complete_bust (31:1), Dev_Interf_0_Req_complete_bust (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_0_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_0_Req_complete_bust:** DMA Device interface 0 Request only complete burst

15.8.574 reg_isp_dma_Dev_Interf_1_Req_complete_bust_type (isp_dma_Dev_Interf_1_Req_complete_bust)—Offset 43304h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_1_Req_complete_bust: [ISPMMADR] + 43304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_Dev_Interf_1_Req_complete_bust (31:1), Dev_Interf_1_Req_complete_bust (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_1_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_1_Req_complete_bust:** DMA Device interface 1 Request only complete burst

15.8.575 reg_isp_dma_Dev_Interf_2_Req_complete_bust_type (isp_dma_Dev_Interf_2_Req_complete_bust)—Offset 43308h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_2_Req_complete_bust: [ISPMMADR] + 43308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_Dev_Interf_2_Req_complete_bust

Dev_Interf_2_Req_complete_bust

Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_2_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_2_Req_complete_bust:** DMA Device interface 2 Request only complete burst

15.8.576 reg_isp_dma_Dev_Interf_2_Max_burst_Size_type (isp_dma_Dev_Interf_2_Max_burst_Size)—Offset 43408h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_dma_Dev_Interf_2_Max_burst_Size: [ISPMMADR] + 43408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000007Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

unused_Dev_Interf_2_Max_burst_Size (31:8), Dev_Interf_2_Max_burst_Size (7:0)

Bit Range	Default & Access	Description
31:8	0h RW	**unused_Dev_Interf_2_Max_burst_Size:** Unused
7:0	7Fh RW	**Dev_Interf_2_Max_burst_Size:** DMA Device interface 2 max burst size

15.8.577 reg_gdc1_reg0_type (gdc1_reg0)—Offset 50000h

Status register: Current opx, opy, top-level FSM state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_reg0: [ISPMMADR] + 50000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg0 (31:30), OPX (29:17), not_used1 (16:14), OPY (13:2), FSM0_state (1:0)

Bit Range	Default & Access	Description
31:30	0h RW	**unused_reg0:** Unused
29:17	0h RO	**OPX:** OPX value
16:14	0h RO	**not_used1:** N/A

Bit Range	Default & Access	Description
13:2	0h RO	**OPY:** OPY value
1:0	0h RO	**FSM0_state:** FSM0 state: 00=Idle ; 01=Busy-receiving data needed to kick the device ; 10=Busy-wait state ; 11=Busy-run state

15.8.578 reg_gdc1_woi_x_type (gdc1_woi_x)—Offset 50004h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_woi_x: [ISPMMADR] + 50004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_woi_x (bits 31:12), woi_x (bits 11:0)

Bit Range	Default & Access	Description
31:12	0h RW	**unused_woi_x:** Unused
11:0	0h RO	**woi_x:** Configured X dimension of the internal window-of-interest (local memory)

15.8.579 reg_gdc1_woi_y_type (gdc1_woi_y)—Offset 50008h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_woi_y: [ISPMMADR] + 50008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_woi_y (bits 31:6), woi_y (bits 5:0)

Bit Range	Default & Access	Description
31:6	0h RW	**unused_woi_y:** Unused
5:0	0h RO	**woi_y:** Configured Y dimension of the internal window-of-interest (local memory)

15.8.580 reg_gdc1_bpp_type (gdc1_bpp)—Offset 5000Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_bpp: [ISPMMADR] + 5000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_bpp																												bpp			

Bit Range	Default & Access	Description
31:4	0h RW	**unused_bpp:** Unused
3:0	0h RW	**bpp:** Bits per input/output pixel, allowed: 8, 10, 12, 14

15.8.581 reg_gdc1_fryipxfrx_start_type (gdc1_fryipxfrx_start)—Offset 50010h

Fractional component of the starting X and Y position for scaling given in fixed point notation

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_fryipxfrx_start: [ISPMMADR] + 50010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_fryipxfrx_start | fry | ipxfrx

Bit Range	Default & Access	Description
31:26	0h RW	**unused_fryipxfrx_start:** Unused
25:16	0h RW	**fry:** Fractional component of the Y start
15:0	0h RW	**ipxfrx:** Integer (6) and Fractional (10) component of the X start

15.8.582 reg_gdc1_oxdim_type (gdc1_oxdim)—Offset 50014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_oxdim: [ISPMMADR] + 50014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_oxdim | oxdim

Bit Range	Default & Access	Description
31:13	0h RW	**unused_oxdim:** Unused
12:0	0h RW	**oxdim:** Output X dimension of the produced block of pixels

15.8.583 reg_gdc1_oydim_type (gdc1_oydim)—Offset 50018h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_oydim: [ISPMMADR] + 50018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_oydim (31:12), oydim (11:0)

Bit Range	Default & Access	Description
31:12	0h RW	**unused_oydim:** Unused
11:0	0h RW	**oydim:** Output Y dimension of the produced block of pixels

15.8.584 reg_gdc1_src_addr_type (gdc1_src_addr)—Offset 5001Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_src_addr: [ISPMMADR] + 5001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_src_addr (31:25), src_addr (24:0)

Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_addr:** Unused
24:0	0h RW	**src_addr:** Source (input) pixel base address [byte-based]

15.8.585 reg_gdc1_src_end_type (gdc1_src_end)—Offset 50020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_src_end: [ISPMMADR] + 50020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_src_end							src_end																								

Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_end:** Unused
24:0	0h RW	**src_end:** End address. When reached wrap around. [byte-based]

15.8.586 reg_gdc1_src_wrap_type (gdc1_src_wrap)—Offset 50024h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_src_wrap: [ISPMMADR] + 50024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_src_wrap							src_wrap																								

Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_wrap:** Unused
24:0	0h RW	**src_wrap:** Wrap addr. Wrap here when src_end reached [byte-based]

15.8.587 reg_gdc1_src_stride_type (gdc1_src_stride)—Offset 50028h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_src_stride: [ISPMMADR] + 50028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_src_stride | src_stride

Bit Range	Default & Access	Description
31:19	0h RW	**unused_src_stride:** Unused
18:0	0h RW	**src_stride:** Source (input) pixel stride [byte-based]

15.8.588 reg_gdc1_dst_addr_type (gdc1_dst_addr)—Offset 5002Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_dst_addr: [ISPMMADR] + 5002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_dst_addr | dst_addr

Bit Range	Default & Access	Description
31:25	0h RW	**unused_dst_addr:** Unused
24:0	0h RW	**dst_addr:** Destination (output) pixel base address [byte-based]

15.8.589 reg_gdc1_dst_stride_type (gdc1_dst_stride)—Offset 50030h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_dst_stride: [ISPMMADR] + 50030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_dst_stride | dst_stride

Bit Range	Default & Access	Description
31:19	0h RW	**unused_dst_stride:** Unused
18:0	0h RW	**dst_stride:** Destination (output) pixel stride [byte-based]

15.8.590 reg_gdc1_dx_type (gdc1_dx)—Offset 50034h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_dx: [ISPMMADR] + 50034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_dx | dx

Bit Range	Default & Access	Description
31:14	0h RW	**unused_dx:** Unused
13:0	0h RW	**dx:** Scaling only: Horizontal scaling factor

15.8.591 reg_gdc1_dy_type (gdc1_dy)—Offset 50038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_dy: [ISPMMADR] + 50038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_dy																		dy													

Bit Range	Default & Access	Description
31:14	0h RW	**unused_dy:** Unused
13:0	0h RW	**dy:** Scaling only: Vertical scaling factor

15.8.592 reg_gdc1_P0_primX_ixdim_type (gdc1_P0_primX_ixdim)—Offset 5003Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_P0_primX_ixdim: [ISPMMADR] + 5003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_P0_primX_ixdim									P0_primX_ixdim																						

Bit Range	Default & Access	Description
31:23	0h RW	**unused_P0_primX_ixdim:** Unused
22:0	0h RW	**P0_primX_ixdim:** P0(X) Tetragon mode: top-left coordinate (X), Scaling mode: dimension of the input region (X), fixed point notation, 13.10

15.8.593 reg_gdc1_P0_primY_iydim_type (gdc1_P0_primY_iydim)—Offset 50040h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_P0_primY_iydim: [ISPMMADR] + 50040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P0_primY_iydim | P0_primY_iydim

Bit Range	Default & Access	Description
31:22	0h RW	**unused_P0_primY_iydim:** Unused
21:0	0h RW	**P0_primY_iydim:** P0(Y) Tetragon mode: top-left coordinate (Y), Scaling mode: dimension of the input region (Y), fixed point notation, 12.10

15.8.594 reg_gdc1_P1_primX_type (gdc1_P1_primX)—Offset 50044h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_P1_primX: [ISPMMADR] + 50044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P1_primX | P1_primX

Bit Range	Default & Access	Description
31:23	0h RW	**unused_P1_primX:** Unused
22:0	0h RW	**P1_primX:** P1(X) Tetragon mode only: top-right coordinate (X), fixed point notation, 13.10

15.8.595 reg_gdc1_P1_primY_type (gdc1_P1_primY)—Offset 50048h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_P1_primY: [ISPMMADR] + 50048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P1_primY | P1_primY

Bit Range	Default & Access	Description
31:22	0h RW	**unused_P1_primY:** Unused
21:0	0h RW	**P1_primY:** P1(Y) Tetragon mode only: top-right coordinate (Y), fixed point notation, 12.10

15.8.596 reg_gdc1_P2_primX_type (gdc1_P2_primX)—Offset 5004Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_P2_primX: [ISPMMADR] + 5004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P2_primX | P2_primX

Bit Range	Default & Access	Description
31:23	0h RW	**unused_P2_primX:** Unused
22:0	0h RW	**P2_primX:** P2(X) Tetragon mode only: bottom-left coordinate (X), fixed point notation, 13.10

15.8.597 reg_gdc1_P2_primY_type (gdc1_P2_primY)—Offset 50050h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_P2_primY: [ISPMMADR] + 50050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P2_primY (31:22) | P2_primY (21:0)

Bit Range	Default & Access	Description
31:22	0h RW	**unused_P2_primY:** Unused
21:0	0h RW	**P2_primY:** P2(Y) Tetragon mode only: bottom-left coordinate (Y), fixed point notation, 12.10

15.8.598 reg_gdc1_P3_primX_type (gdc1_P3_primX)—Offset 50054h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_P3_primX: [ISPMMADR] + 50054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P3_primX (31:23) | P3_primX (22:0)

Bit Range	Default & Access	Description
31:23	0h RW	**unused_P3_primX:** Unused
22:0	0h RW	**P3_primX:** P3(X) Tetragon mode only: bottom-right coordinate (X), fixed point notation, 13.10

15.8.599 reg_gdc1_P3_primY_type (gdc1_P3_primY)—Offset 50058h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_P3_primY: [ISPMMADR] + 50058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P3_primY (31:22), P3_primY (21:0)

Bit Range	Default & Access	Description
31:22	0h RW	**unused_P3_primY:** Unused
21:0	0h RW	**P3_primY:** P3(Y) Tetragon mode only: bottom-right coordinate (Y), fixed point notation, 12.10

15.8.600 reg_gdc1_perf_mode_type (gdc1_perf_mode)—Offset 5005Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_perf_mode: [ISPMMADR] + 5005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_perf_mode (31:2), perf_mode (1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_perf_mode:** Unused
1:0	0h RW	**perf_mode:** Number and location of pixels produced per clock cycle: 00=1x1 pixels ; 01=2x1 pixels ; 10=1x2 pixels ; 11=2x2 pixels

15.8.601 reg_gdc1_interp_type_type (gdc1_interp_type)—Offset 50060h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_interp_type: [ISPMMADR] + 50060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_interp_type (bits 31:2), interp_type (bits 1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_interp_type:** Unused
1:0	0h RW	**interp_type:** Type of interpolation: 00=NND ; 01=BLI ; 10=BCI ; 11=LUT

15.8.602 reg_gdc1_scan_mode_type (gdc1_scan_mode)—Offset 50064h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc1_scan_mode: [ISPMMADR] + 50064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_scan_mode (bits 31:1), scan_mode (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_scan_mode:** Unused
0	0h RW	**scan_mode:** Scanning mode: 0 = STB (Slide To Bottom) ; 1 = STR (Slide To Right)

15.8.603 reg_gdc1_proc_mode_type (gdc1_proc_mode)—Offset 50068h

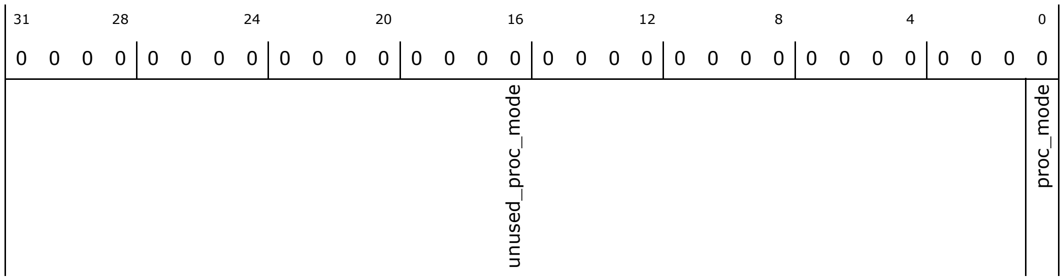
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc1_proc_mode: [ISPMMADR] + 50068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0h RW	**unused_proc_mode:** Unused
0	0h RW	**proc_mode:** Processing mode: 0 = Rectangular-based scaling ; 1 = Tetragon-based scaling

15.8.604 reg_gdc2_reg0_type (gdc2_reg0)—Offset 60000h

Status register: Current opx, opy, top-level FSM state

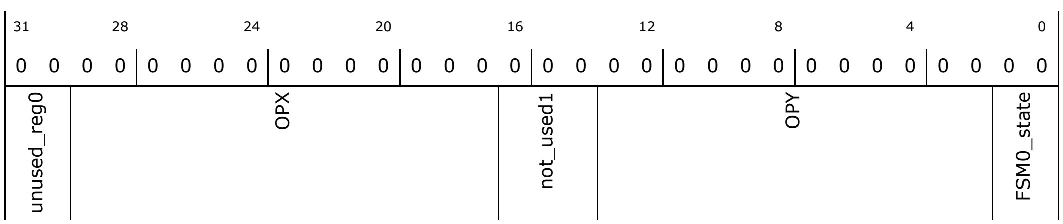
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_reg0: [ISPMMADR] + 60000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**unused_reg0:** Unused
29:17	0h RO	**OPX:** OPX value

Bit Range	Default & Access	Description
16:14	0h RO	**not_used1:** N/A
13:2	0h RO	**OPY:** OPY value
1:0	0h RO	**FSM0_state:** FSM0 state: 00=Idle ; 01=Busy-receiving data needed to kick the device ; 10=Busy-wait state ; 11=Busy-run state

15.8.605 reg_gdc2_woi_x_type (gdc2_woi_x)—Offset 60004h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_woi_x: [ISPMMADR] + 60004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_woi_x (bits 31:12), woi_x (bits 11:0)

Bit Range	Default & Access	Description
31:12	0h RW	**unused_woi_x:** Unused
11:0	0h RO	**woi_x:** Configured X dimension of the internal window-of-interest (local memory)

15.8.606 reg_gdc2_woi_y_type (gdc2_woi_y)—Offset 60008h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_woi_y: [ISPMMADR] + 60008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_woi_y (bits 31:6), woi_y (bits 5:0)

Bit Range	Default & Access	Description
31:6	0h RW	**unused_woi_y:** Unused
5:0	0h RO	**woi_y:** Configured Y dimension of the internal window-of-interest (local memory)

15.8.607 reg_gdc2_bpp_type (gdc2_bpp)—Offset 6000Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_bpp: [ISPMMADR] + 6000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_bpp																												bpp			

Bit Range	Default & Access	Description
31:4	0h RW	**unused_bpp:** Unused
3:0	0h RW	**bpp:** Bits per input/output pixel, allowed: 8, 10, 12, 14

15.8.608 reg_gdc2_fryipxfrx_start_type (gdc2_fryipxfrx_start)—Offset 60010h

Fractional component of the starting X and Y position for scaling given in fixed point notation

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_fryipxfrx_start: [ISPMMADR] + 60010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_fryipxfrx_start	fry	ipxfrx

Bit Range	Default & Access	Description
31:26	0h RW	**unused_fryipxfrx_start:** Unused
25:16	0h RW	**fry:** Fractional component of the Y start
15:0	0h RW	**ipxfrx:** Integer (6) and Fractional (10) component of the X start

15.8.609 reg_gdc2_oxdim_type (gdc2_oxdim)—Offset 60014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_oxdim: [ISPMMADR] + 60014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_oxdim	oxdim

Bit Range	Default & Access	Description
31:13	0h RW	**unused_oxdim:** Unused
12:0	0h RW	**oxdim:** Output X dimension of the produced block of pixels

15.8.610 reg_gdc2_oydim_type (gdc2_oydim)—Offset 60018h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_oydim: [ISPMMADR] + 60018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_oydim (31:12), oydim (11:0)

Bit Range	Default & Access	Description
31:12	0h RW	**unused_oydim:** Unused
11:0	0h RW	**oydim:** Output Y dimension of the produced block of pixels

15.8.611 reg_gdc2_src_addr_type (gdc2_src_addr)—Offset 6001Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_src_addr: [ISPMMADR] + 6001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_src_addr (31:25), src_addr (24:0)

Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_addr:** Unused
24:0	0h RW	**src_addr:** Source (input) pixel base address [byte-based]

15.8.612 reg_gdc2_src_end_type (gdc2_src_end)—Offset 60020h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_src_end: [ISPMMADR] + 60020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_src_end							src_end																								

Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_end:** Unused
24:0	0h RW	**src_end:** End address. When reached wrap around. [byte-based]

15.8.613 reg_gdc2_src_wrap_type (gdc2_src_wrap)—Offset 60024h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_src_wrap: [ISPMMADR] + 60024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_src_wrap							src_wrap																								

Bit Range	Default & Access	Description
31:25	0h RW	**unused_src_wrap:** Unused
24:0	0h RW	**src_wrap:** Wrap addr. Wrap here when src_end reached [byte-based]

15.8.614 reg_gdc2_src_stride_type (gdc2_src_stride)—Offset 60028h

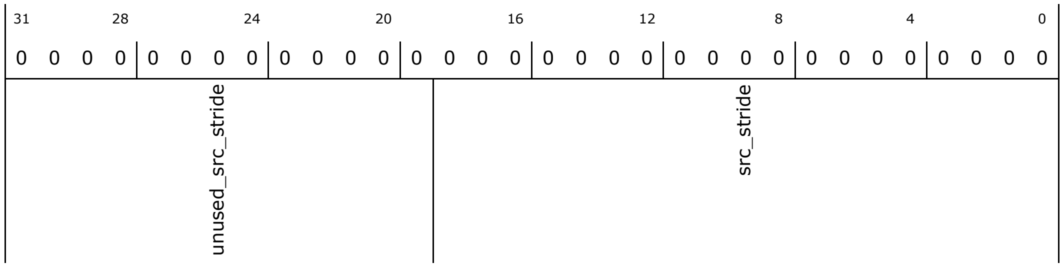
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_src_stride: [ISPMMADR] + 60028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0h RW	**unused_src_stride:** Unused
18:0	0h RW	**src_stride:** Source (input) pixel stride [byte-based]

15.8.615 reg_gdc2_dst_addr_type (gdc2_dst_addr)—Offset 6002Ch

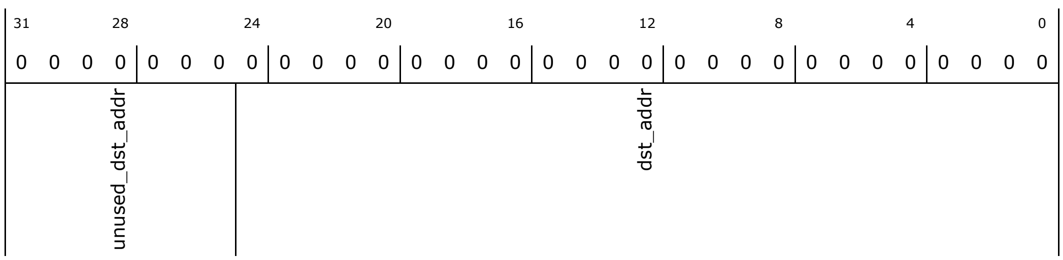
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_dst_addr: [ISPMMADR] + 6002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0h RW	**unused_dst_addr:** Unused
24:0	0h RW	**dst_addr:** Destination (output) pixel base address [byte-based]

15.8.616 reg_gdc2_dst_stride_type (gdc2_dst_stride)—Offset 60030h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_dst_stride: [ISPMMADR] + 60030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_dst_stride | dst_stride

Bit Range	Default & Access	Description
31:19	0h RW	**unused_dst_stride:** Unused
18:0	0h RW	**dst_stride:** Destination (output) pixel stride [byte-based]

15.8.617 reg_gdc2_dx_type (gdc2_dx)—Offset 60034h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_dx: [ISPMMADR] + 60034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_dx | dx

Bit Range	Default & Access	Description
31:14	0h RW	**unused_dx:** Unused
13:0	0h RW	**dx:** Scaling only: Horizontal scaling factor

15.8.618 reg_gdc2_dy_type (gdc2_dy)—Offset 60038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_dy: [ISPMMADR] + 60038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_dy | dy

Bit Range	Default & Access	Description
31:14	0h RW	**unused_dy:** Unused
13:0	0h RW	**dy:** Scaling only: Vertical scaling factor

15.8.619 reg_gdc2_P0_primX_ixdim_type (gdc2_P0_primX_ixdim)—Offset 6003Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P0_primX_ixdim: [ISPMMADR] + 6003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P0_primX_ixdim | P0_primX_ixdim

Bit Range	Default & Access	Description
31:23	0h RW	**unused_P0_primX_ixdim:** Unused
22:0	0h RW	**P0_primX_ixdim:** P0(X) Tetragon mode: top-left coordinate (X), Scaling mode: dimension of the input region (X), fixed point notation, 13.10

15.8.620 reg_gdc2_P0_primY_iydim_type (gdc2_P0_primY_iydim)—Offset 60040h

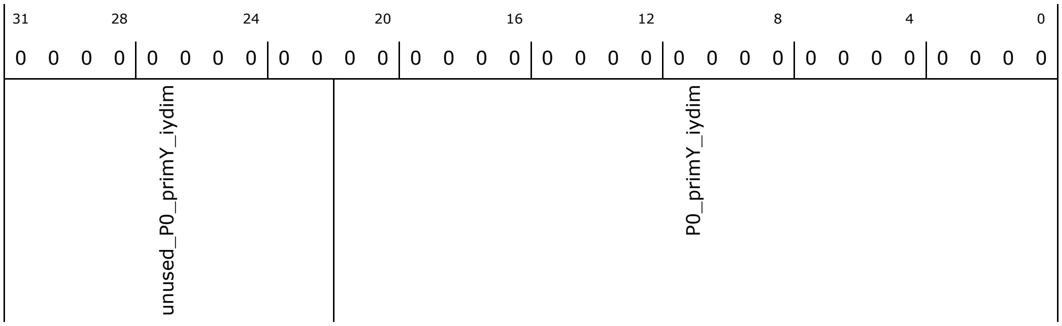
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P0_primY_iydim: [ISPMMADR] + 60040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0h RW	**unused_P0_primY_iydim:** Unused
21:0	0h RW	**P0_primY_iydim:** P0(Y) Tetragon mode: top-left coordinate (Y), Scaling mode: dimension of the input region (Y), fixed point notation, 12.10

15.8.621 reg_gdc2_P1_primX_type (gdc2_P1_primX)—Offset 60044h

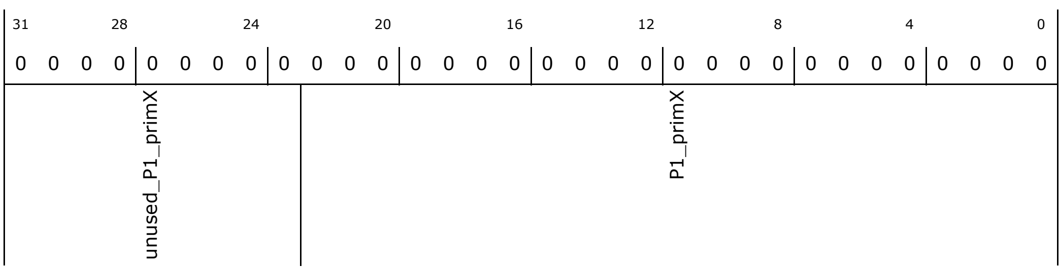
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

gdc2_P1_primX: [ISPMMADR] + 60044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:23	0h RW	**unused_P1_primX:** Unused
22:0	0h RW	**P1_primX:** P1(X) Tetragon mode only: top-right coordinate (X), fixed point notation, 13.10

15.8.622 reg_gdc2_P1_primY_type (gdc2_P1_primY)—Offset 60048h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_P1_primY: [ISPMMADR] + 60048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P1_primY (31:22) | P1_primY (21:0)

Bit Range	Default & Access	Description
31:22	0h RW	**unused_P1_primY:** Unused
21:0	0h RW	**P1_primY:** P1(Y) Tetragon mode only: top-right coordinate (Y), fixed point notation, 12.10

15.8.623 reg_gdc2_P2_primX_type (gdc2_P2_primX)—Offset 6004Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_P2_primX: [ISPMMADR] + 6004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_P2_primX (31:23) | P2_primX (22:0)

Bit Range	Default & Access	Description
31:23	0h RW	**unused_P2_primX:** Unused
22:0	0h RW	**P2_primX:** P2(X) Tetragon mode only: bottom-left coordinate (X), fixed point notation, 13.10

15.8.624 reg_gdc2_P2_primY_type (gdc2_P2_primY)—Offset 60050h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_P2_primY: [ISPMMADR] + 60050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_P2_primY (bits 31:22), P2_primY (bits 21:0)

Bit Range	Default & Access	Description
31:22	0h RW	**unused_P2_primY:** Unused
21:0	0h RW	**P2_primY:** P2(Y) Tetragon mode only: bottom-left coordinate (Y), fixed point notation, 12.10

15.8.625 reg_gdc2_P3_primX_type (gdc2_P3_primX)—Offset 60054h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_P3_primX: [ISPMMADR] + 60054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_P3_primX (bits 31:23), P3_primX (bits 22:0)

Bit Range	Default & Access	Description
31:23	0h RW	**unused_P3_primX:** Unused
22:0	0h RW	**P3_primX:** P3(X) Tetragon mode only: bottom-right coordinate (X), fixed point notation, 13.10

15.8.626 reg_gdc2_P3_primY_type (gdc2_P3_primY)—Offset 60058h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_P3_primY: [ISPMMADR] + 60058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_P3_primY (bits 31:22), P3_primY (bits 21:0)

Bit Range	Default & Access	Description
31:22	0h RW	**unused_P3_primY:** Unused
21:0	0h RW	**P3_primY:** P3(Y) Tetragon mode only: bottom-right coordinate (Y), fixed point notation, 12.10

15.8.627 reg_gdc2_perf_mode_type (gdc2_perf_mode)—Offset 6005Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_perf_mode: [ISPMMADR] + 6005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_perf_mode (bits 31:2), perf_mode (bits 1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_perf_mode:** Unused
1:0	0h RW	**perf_mode:** Number and location of pixels produced per clock cycle: 00=1x1 pixels ; 01=2x1 pixels ; 10=1x2 pixels ; 11=2x2 pixels

15.8.628 reg_gdc2_interp_type_type (gdc2_interp_type)—Offset 60060h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_interp_type: [ISPMMADR] + 60060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_interp_type (31:2), interp_type (1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_interp_type:** Unused
1:0	0h RW	**interp_type:** Type of interpolation: 00=NND ; 01=BLI ; 10=BCI ; 11=LUT

15.8.629 reg_gdc2_scan_mode_type (gdc2_scan_mode)—Offset 60064h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_scan_mode: [ISPMMADR] + 60064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_scan_mode (31:1), scan_mode (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_scan_mode:** Unused
0	0h RW	**scan_mode:** Scanning mode: 0 = STB (Slide To Bottom) ; 1 = STR (Slide To Right)

15.8.630 reg_gdc2_proc_mode_type (gdc2_proc_mode)—Offset 60068h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

gdc2_proc_mode: [ISPMMADR] + 60068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_proc_mode (bits 31:1), proc_mode (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_proc_mode:** Unused
0	0h RW	**proc_mode:** Processing mode: 0 = Rectangular-based scaling ; 1 = Tetragon-based scaling

15.8.631 reg_data_out_sys_c_mmu_MMU_invalidate_cache_type (data_out_sys_c_mmu_MMU_invalidate_cache)—Offset 70000h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

data_out_sys_c_mmu_MMU_invalidate_cache: [ISPMMADR] + 70000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_MMU_invalidate_cache (bits 31:1), MMU_invalidate_cache (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MMU_invalidate_cache:** Unused
0	0h WO	**MMU_invalidate_cache:** MMU invalidate cache. When '1', the MMUs TLB is invalidated.

15.8.632 reg_data_out_sys_c_mmu_MMU_page_table_base_type (data_out_sys_c_mmu_MMU_page_table_base)—Offset 70004h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

data_out_sys_c_mmu_MMU_page_table_base: [ISPMMADR] + 70004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:24	23:0
unused_MMU_page_table_base	MMU_page_table_base

Bit Range	Default & Access	Description
31:24	0h RW	**unused_MMU_page_table_base:** Unused
23:0	0h RW	**MMU_page_table_base:** Defines the physical page number of the page tables

15.8.633 reg_inp_sys_csi_receiver_csi1_dev_ready_type (inp_sys_csi_receiver_csi1_dev_ready)—Offset 80100h

Set after programming operational registers to enable receiver

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi1_dev_ready: [ISPMMADR] + 80100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi1_dev_ready | mask_data_id_err | mask_ecc_double_bit_err | mask_rx_data_timeout_err | mask_sot_sync_err | mask_overrun_err | mask_init_time_out_err | reserved_1 | device_ready

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi1_dev_ready:** Unused
7	0h RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0h RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0h RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0h RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0h RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded
2	0h RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0h RO	**reserved_1:** Reserved
0	0h RW	**device_ready:** Set to indicate that device is ready for reception

15.8.634 reg_inp_sys_csi_receiver_csi1_int_status_type (inp_sys_csi_receiver_csi1_int_status)—Offset 80104h

Interrupt Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_int_status: [ISPMMADR] + 80104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							unused_csi1_int_status								err_line_sync	err_escape	err_data_timeout	err_frame_data	err_frame_sync	err_id	err_crc	no_ecc_err	err_ecc_corr	err_ecc_double	err_control	err_sot_sync_hs	err_sot_hs	sleep_mode_exit	sleep_mode_entry	err_init_timeout	reserved_0

Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi1_int_status:** Unused
16	0h RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0h RW/1C	**err_escape:** Set if an unrecognised escape entry command is received
14	0h RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0h RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0h RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel
11	0h RW/1C	**err_id:** Set if packet header has a unrecognised data id
10	0h RW/1C	**err_crc:** Set if computed CRC differs from received value
9	0h RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0h RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit
7	0h RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits
6	0h RW/1C	**err_control:** Set if DPHY flags a control error
5	0h RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0h RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0h RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state
2	0h RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state
1	0h RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes
0	0h RO	**reserved_0:** Always set to 0

15.8.635 reg_inp_sys_csi_receiver_csi1_int_enable_type (inp_sys_csi_receiver_csi1_int_enable)—Offset 80108h

Interrupt Enable

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_int_enable: [ISPMMADR] + 80108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_csi1_int_enable															err_line_sync	err_escape	err_data_timeout	err_frame_data	err_frame_sync	err_id	err_crc	no_ecc_err	err_ecc_corr	err_ecc_double	err_control	err_sot_sync_hs	err_sot_hs	sleep_mode_exit	sleep_mode_entry	err_init_timeout	overrun

Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi1_int_enable:** Unused
16	0h RW	**err_line_sync:** Enable line sync error interrupt
15	0h RW	**err_escape:** Enable escape entry error interrupt
14	0h RW	**err_data_timeout:** Enable timeout error interrupt
13	0h RW	**err_frame_data:** Enable frame data error interrupt
12	0h RW	**err_frame_sync:** Enable frame sync error interrupt
11	0h RW	**err_id:** Enable data id error interrupt
10	0h RW	**err_crc:** Enable CRC error interrupt
9	0h RW	**no_ecc_err:** Enable no ECC error interrupt
8	0h RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0h RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0h RW	**err_control:** Enable control error interrupt

Bit Range	Default & Access	Description
5	0h RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0h RW	**err_sot_hs:** Enable start of transmission error interrupt
3	0h RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0h RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0h RW	**err_init_timeout:** Enable Initialization timeout error interrupt
0	0h RW	**overrun:** Enable FIFO overrun interrupt: NOT available now, can be discarded

15.8.636 reg_inp_sys_csi_receiver_csi1_func_prg_type (inp_sys_csi_receiver_csi1_func_prg)—Offset 8010Ch

Functional Programming

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_func_prg: [ISPMMADR] + 8010Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
unused_csi1_func_prg													func_prg_reg_2			func_prg_reg_1								func_prg_reg_0							

Bit Range	Default & Access	Description
31:19	0h RW	**unused_csi1_func_prg:** Unused
18:16	7h RW	**func_prg_reg_2:** Byte 2 for functional programming
15:8	FFh RW	**func_prg_reg_1:** Byte 1 for functional programming
7:0	FFh RW	**func_prg_reg_0:** Byte 0 for functional programming

15.8.637 reg_inp_sys_csi_receiver_csi1_init_cnt_type (inp_sys_csi_receiver_csi1_init_cnt)—Offset 80110h

Duration after power up when DPHY lanes will not be observed

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_init_cnt: [ISPMMADR] + 80110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_csi1_init_cnt (31:16), init_timer_reg_1 (15:8), init_timer_reg_0 (7:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi1_init_cnt:** Unused
15:8	0h RW	**init_timer_reg_1:** Byte 1 for power up timer
7:0	0h RW	**init_timer_reg_0:** Byte 0 for power up timer

15.8.638 reg_inp_sys_csi_receiver_csi_backend_fs_ls_type (inp_sys_csi_receiver_csi_backend_fs_ls)—Offset 8011Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_fs_ls: [ISPMMADR] + 8011Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

unused_csi_backend_fs_ls (31:8) | csi_backend_fs_ls (7:0)

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_fs_ls:** Unused
7:0	02h RW	**csi_backend_fs_ls:** Minimum interval between frame start and line start syncs

15.8.639 reg_inp_sys_csi_receiver_csi_backend_ls_dvalid_type (inp_sys_csi_receiver_csi_backend_ls_dvalid)—Offset 80120h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_ls_dvalid: [ISPMMADR] + 80120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

unused_csi_backend_ls_dvalid (31:8) | csi_backend_ls_dvalid (7:0)

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_ls_dvalid:** Unused
7:0	02h RW	**csi_backend_ls_dvalid:** Minimum interval between line start sync and valid data

15.8.640 reg_inp_sys_csi_receiver_csi_backend_dvalid_le_type (inp_sys_csi_receiver_csi_backend_dvalid_le)—Offset 80124h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_dvalid_le: [ISPMMADR] + 80124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31:8: unused_csi_backend_dvalid_le; bits 7:0: csi_backend_dvalid_le

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_dvalid_le:** Unused
7:0	02h RW	**csi_backend_dvalid_le:** Minimum interval between valid data and line end sync

15.8.641 reg_inp_sys_csi_receiver_csi_backend_le_fe_type (inp_sys_csi_receiver_csi_backend_le_fe)—Offset 80128h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_le_fe: [ISPMMADR] + 80128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
unused_csi_backend_le_fe																								csi_backend_le_fe							

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_le_fe:** Unused
7:0	02h RW	**csi_backend_le_fe:** Minimum interval between line end and frame end syncs

15.8.642 reg_inp_sys_csi_receiver_csi_backend_fe_fs_type (inp_sys_csi_receiver_csi_backend_fe_fs)—Offset 8012Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_fe_fs: [ISPMMADR] + 8012Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
unused_csi_backend_fe_fs																								csi_backend_fe_fs							

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_fe_fs:** Unused
7:0	02h RW	**csi_backend_fe_fs:** Minimum interval between frame end and frame start syncs

15.8.643 reg_inp_sys_csi_receiver_csi_backend_le_ls_type (inp_sys_csi_receiver_csi_backend_le_ls)—Offset 80130h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_le_ls: [ISPMMADR] + 80130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 31:8	Bits 7:0
unused_csi_backend_le_ls	csi_backend_le_ls

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_backend_le_ls:** Unused
7:0	04h RW	**csi_backend_le_ls:** Minimum interval between line end and line start syncs

15.8.644 reg_inp_sys_csi_receiver_csi_backend_two_pixel_en_type (inp_sys_csi_receiver_csi_backend_two_pixel_en)—Offset 80134h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_two_pixel_en: [ISPMMADR] + 80134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_csi_backend_two_pixel_en (31:1), csi_backend_two_pixel_en (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_backend_two_pixel_en:** Unused
0	0h RW	**csi_backend_two_pixel_en:** Enable two pixels per clock mode

15.8.645 reg_inp_sys_csi_receiver_csi1_raw16_18_data_id_type (inp_sys_csi_receiver_csi1_raw16_18_data_id)—Offset 80138h

RAW 16 and RAW 18 data ID register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi1_raw16_18_data_id: [ISPMMADR] + 80138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_csi1_raw16_18_data_id (31:16), reserved_1514 (15:14), raw18 (13:8), reserved_76 (7:6), raw16 (5:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi1_raw16_18_data_id:** Unused
15:14	0h RO	**reserved_1514:** Reserved
13:8	0h RW	**raw18:** RAW 18 data ID
7:6	0h RO	**reserved_76:** Reserved
5:0	0h RW	**raw16:** RAW 16 data ID

15.8.646 reg_inp_sys_csi_receiver_csi1_sync_cnt_type (inp_sys_csi_receiver_csi1_sync_cnt)—Offset 8013Ch

Synchronisation count value in terms of MIPI high speed byte clock

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi1_sync_cnt: [ISPMMADR] + 8013Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
sync_cnt_4lane								sync_cnt_3lane								sync_cnt_2lane								sync_cnt_1lane							

Bit Range	Default & Access	Description
31:24	FFh RW	**sync_cnt_4lane:** Synchronisation count value for 4 lane
23:16	FFh RW	**sync_cnt_3lane:** Synchronisation count value for 3 lane
15:8	FFh RW	**sync_cnt_2lane:** Synchronisation count value for 2 lane
7:0	FFh RW	**sync_cnt_1lane:** Synchronisation count value for 1 lane

15.8.647 reg_inp_sys_csi_receiver_csi1_rx_cnt_type (inp_sys_csi_receiver_csi1_rx_cnt)—Offset 80140h

Receive count value in terms of MIPI high speed byte clock

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi1_rx_cnt: [ISPMMADR] + 80140h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: FFFFFFFFh

Bits	31:24	23:16	15:8	7:0
Value	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Field	rx_cnt_4lane	rx_cnt_3lane	rx_cnt_2lane	rx_cnt_1lane

Bit Range	Default & Access	Description
31:24	FFh RW	**rx_cnt_4lane:** Receive count value for 4 lane
23:16	FFh RW	**rx_cnt_3lane:** Receive count value for 3 lane
15:8	FFh RW	**rx_cnt_2lane:** Receive count value for 2 lane
7:0	FFh RW	**rx_cnt_1lane:** Receive count value for 1 lane

15.8.648 reg_inp_sys_csi_receiver_csi_backend_rst_type (inp_sys_csi_receiver_csi_backend_rst)—Offset 80144h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_backend_rst: [ISPMMADR] + 80144h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Field	unused_csi_backend_rst	csi_backend_rst

Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_backend_rst:** Unused

Bit Range	Default & Access	Description
0	0h RW	**csi_backend_rst:** Reset CSI Rx backend block

15.8.649 reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0)—Offset 80148h

Compression and Prediction scheme register 0 for virtual channel 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0: [ISPMMADR] + 80148h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_backend_comp_pred_reg0_vc0	pred_usd_type6	comp_usd_type6	pred_usd_type5	comp_usd_type5	pred_usd_type4	comp_usd_type4	pred_usd_type3	comp_usd_type3	pred_usd_type2	comp_usd_type2	pred_usd_type1	comp_usd_type1

Bit Range	Default & Access	Description
31:30	0h RW	**unused_csi_backend_comp_pred_reg0_vc0:** Unused
29:28	0h RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0h RW	**comp_usd_type6:** compression format for user defined type 6 data: value between 1 to 6
24:23	0h RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0h RW	**comp_usd_type5:** compression format for user defined type 5 data: value between 1 to 6
19:18	0h RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2

Bit Range	Default & Access	Description
17:15	0h RW	**comp_usd_type4:** compression format for user defined type 4 data: value between 1 to 6
14:13	0h RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0h RW	**comp_usd_type3:** compression format for user defined type 3 data: value between 1 to 6
9:8	0h RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type2:** compression format for user defined type 2 data: value between 1 to 6
4:3	0h RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for user defined type 1 data: value between 1 to 6

15.8.650 reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc0_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc0)—Offset 8014Ch

Compression scheme register 1 for virtual channel 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_reg1_vc0: [ISPMMADR] + 8014Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:10	Bits 9:8	Bits 7:5	Bits 4:3	Bits 2:0
unused_csi_backend_comp_reg1_vc0	pred_usd_type8	comp_usd_type8	pred_usd_type7	comp_usd_type7

Bit Range	Default & Access	Description
31:10	0h RW	**unused_csi_backend_comp_reg1_vc0:** Unused

Bit Range	Default & Access	Description
9:8	0h RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type8:** compression format for user defined type 8 data: value between 1 to 6
4:3	0h RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type7:** compression format for user defined type 7 data: value between 1 to 6

15.8.651 reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1)—Offset 80150h

Compression and Prediction scheme register 0 for virtual channel 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1: [ISPMMADR] + 80150h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:30	unused_csi_backend_comp_pred_reg0_vc1
29:28	pred_usd_type6
27:25	comp_usd_type6
24:23	pred_usd_type5
22:20	comp_usd_type5
19:18	pred_usd_type4
17:15	comp_usd_type4
14:13	pred_usd_type3
12:10	comp_usd_type3
9:8	pred_usd_type2
7:5	comp_usd_type2
4:3	pred_usd_type1
2:0	comp_usd_type1

Bit Range	Default & Access	Description
31:30	0h RW	**unused_csi_backend_comp_pred_reg0_vc1:** Unused
29:28	0h RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0h RW	**comp_usd_type6:** compression format for user defined type 6 data: value between 1 to 6

Bit Range	Default & Access	Description
24:23	0h RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0h RW	**comp_usd_type5:** compression format for user defined type 5 data: value between 1 to 6
19:18	0h RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0h RW	**comp_usd_type4:** compression format for user defined type 4 data: value between 1 to 6
14:13	0h RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0h RW	**comp_usd_type3:** compression format for user defined type 3 data: value between 1 to 6
9:8	0h RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type2:** compression format for user defined type 2 data: value between 1 to 6
4:3	0h RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for user defined type 1 data: value between 1 to 6

15.8.652 reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc1_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc1)—Offset 80154h

Compression scheme register 1 for virtual channel 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_reg1_vc1: [ISPMMADR] + 80154h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	

Bits 31:10	Bits 9:8	Bits 7:5	Bits 4:3	Bits 2:0
unused_csi_backend_comp_reg1_vc1	pred_usd_type8	comp_usd_type8	pred_usd_type7	comp_usd_type7

Bit Range	Default & Access	Description
31:10	0h RW	**unused_csi_backend_comp_reg1_vc1:** Unused
9:8	0h RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type8:** compression format for user defined type 8 data: value between 1 to 6
4:3	0h RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type7:** compression format for user defined type 7 data: value between 1 to 6

15.8.653 reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2)—Offset 80158h

Compression and Prediction scheme register 0 for virtual channel 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2: [ISPMMADR] + 80158h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_backend_comp_pred_reg0_vc2	pred_usd_type6	comp_usd_type6	pred_usd_type5	comp_usd_type5	pred_usd_type4	comp_usd_type4	pred_usd_type3	comp_usd_type3	pred_usd_type2	comp_usd_type2	pred_usd_type1	comp_usd_type1

Bit Range	Default & Access	Description
31:30	0h RW	**unused_csi_backend_comp_pred_reg0_vc2:** Unused
29:28	0h RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0h RW	**comp_usd_type6:** compression format for user defined type 6 data: value between 1 to 6
24:23	0h RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0h RW	**comp_usd_type5:** compression format for user defined type 5 data: value between 1 to 6
19:18	0h RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0h RW	**comp_usd_type4:** compression format for user defined type 4 data: value between 1 to 6
14:13	0h RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0h RW	**comp_usd_type3:** compression format for user defined type 3 data: value between 1 to 6
9:8	0h RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type2:** compression format for user defined type 2 data: value between 1 to 6
4:3	0h RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for user defined type 1 data: value between 1 to 6

15.8.654 reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc2_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc2)—Offset 8015Ch

Compression scheme register 1 for virtual channel 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**inp_sys_csi_receiver_csi_backend_comp_reg1_vc2:** [ISPMMADR] + 8015Ch
	ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
	ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:10	Bits 9:8	Bits 7:5	Bits 4:3	Bits 2:0
unused_csi_backend_comp_reg1_vc2	pred_usd_type8	comp_usd_type8	pred_usd_type7	comp_usd_type7

Bit Range	Default & Access	Description
31:10	0h RW	**unused_csi_backend_comp_reg1_vc2:** Unused
9:8	0h RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type8:** compression format for user defined type 8 data: value between 1 to 6
4:3	0h RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type7:** compression format for user defined type 7 data: value between 1 to 6

15.8.655 reg_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3_type (inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3)—Offset 80160h

Compression and Prediction scheme register 0 for virtual channel 3

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3:
[ISPMMADR] + 80160h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:30	29:28	27:25	24:23	22:20	19:18	17:15	14:13	12:10	9:8	7:5	4:3	2:0
Default	00	00	000	00	000	00	000	00	000	00	000	00	000
Field	unused_csi_backend_comp_pred_reg0_vc3	pred_usd_type6	comp_usd_type6	pred_usd_type5	comp_usd_type5	pred_usd_type4	comp_usd_type4	pred_usd_type3	comp_usd_type3	pred_usd_type2	comp_usd_type2	pred_usd_type1	comp_usd_type1

Bit Range	Default & Access	Description
31:30	0h RW	**unused_csi_backend_comp_pred_reg0_vc3:** Unused
29:28	0h RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0h RW	**comp_usd_type6:** compression format for user defined type 6 data: value between 1 to 6
24:23	0h RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0h RW	**comp_usd_type5:** compression format for user defined type 5 data: value between 1 to 6
19:18	0h RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0h RW	**comp_usd_type4:** compression format for user defined type 4 data: value between 1 to 6
14:13	0h RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0h RW	**comp_usd_type3:** compression format for user defined type 3 data: value between 1 to 6
9:8	0h RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type2:** compression format for user defined type 2 data: value between 1 to 6
4:3	0h RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2

Bit Range	Default & Access	Description
2:0	0h RW	**comp_usd_type1:** compression format for user defined type 1 data: value between 1 to 6

15.8.656 reg_inp_sys_csi_receiver_csi_backend_comp_reg1_vc3_type (inp_sys_csi_receiver_csi_backend_comp_reg1_vc3)—Offset 80164h

Compression scheme register 1 for virtual channel 3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_comp_reg1_vc3: [ISPMMADR] + 80164h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:10	9:8	7:5	4:3	2:0
Default	0000 0000 0000 0000 0000 00	00	000	00	000
Field	unused_csi_backend_comp_reg1_vc3	pred_usd_type8	comp_usd_type8	pred_usd_type7	comp_usd_type7

Bit Range	Default & Access	Description
31:10	0h RW	**unused_csi_backend_comp_reg1_vc3:** Unused
9:8	0h RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0h RW	**comp_usd_type8:** compression format for user defined type 8 data: value between 1 to 6
4:3	0h RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0h RW	**comp_usd_type7:** compression format for user defined type 7 data: value between 1 to 6

15.8.657 reg_inp_sys_csi_receiver_csi_backend_raw18_reg_type (inp_sys_csi_receiver_csi_backend_raw18_reg)—Offset 80168h

Configuration register for RAW 18 data type decode

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_raw18_reg: [ISPMMADR] + 80168h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:9	Bit 8	Bits 7:6	Bits 5:0
unused_csi_backend_raw18_reg	format_en	format_option	format_id

Bit Range	Default & Access	Description
31:9	0h RW	**unused_csi_backend_raw18_reg:** Unused
8	0h RW	**format_en:** enable RAW 18 type decode
7:6	0h RW	**format_option:** format option for RAW 18 data type: 3 options possible (1,2,3)
5:0	0h RW	**format_id:** data id for RAW 18

15.8.658 reg_inp_sys_csi_receiver_csi_backend_force_raw8_reg_type (inp_sys_csi_receiver_csi_backend_force_raw8_reg)—Offset 8016Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_force_raw8_reg: [ISPMMADR] + 8016Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_backend_force_raw8_reg

csi_backend_force_raw8_reg

Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_backend_force_raw8_reg:** Unused
0	0h RW	**csi_backend_force_raw8_reg:** Force RAW8(byte) decoding for LONG data packets

15.8.659 reg_inp_sys_csi_receiver_csi_backend_raw16_reg_type (inp_sys_csi_receiver_csi_backend_raw16_reg)—Offset 80170h

Configuration register for RAW 16 data type decode

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_backend_raw16_reg: [ISPMMADR] + 80170h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_backend_raw16_reg

format_en

format_option

format_id

Bit Range	Default & Access	Description
31:9	0h RW	**unused_csi_backend_raw16_reg:** Unused
8	0h RW	**format_en:** enable RAW 16 type decode
7:6	0h RW	**format_option:** format option for RAW 16 data type: ONLY 1 option possible (1)
5:0	0h RW	**format_id:** data id for RAW 16

15.8.660 reg_inp_sys_csi_receiver_csi2_dev_ready_type (inp_sys_csi_receiver_csi2_dev_ready)—Offset 80200h

Set after programming operational registers to enable receiver

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_dev_ready: [ISPMMADR] + 80200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:8	7	6	5	4	3	2	1	0
Default	0000 0000 0000 0000 0000 0000	0	0	0	0	0	0	0	0
Field	unused_csi2_dev_ready	mask_data_id_err	mask_ecc_double_bit_err	mask_rx_data_timeout_err	mask_sot_sync_err	mask_overrun_err	mask_init_time_out_err	reserved_1	device_ready

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi2_dev_ready:** Unused
7	0h RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0h RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0h RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0h RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0h RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded

Bit Range	Default & Access	Description
2	0h RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0h RO	**reserved_1:** Reserved
0	0h RW	**device_ready:** Set to indicate that device is ready for reception

15.8.661 reg_inp_sys_csi_receiver_csi2_int_status_type (inp_sys_csi_receiver_csi2_int_status)—Offset 80204h

Interrupt Status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi2_int_status: [ISPMMADR] + 80204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_csi2_int_status	err_line_sync	err_escape	err_data_timeout	err_frame_data	err_frame_sync	err_id	err_crc	no_ecc_err	err_ecc_corr	err_ecc_double	err_control	err_sot_sync_hs	err_sot_hs	sleep_mode_exit	sleep_mode_entry	err_init_timeout	reserved_10

Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi2_int_status:** Unused
16	0h RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0h RW/1C	**err_escape:** Set if an unrecognised escape entry command is received
14	0h RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0h RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0h RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel
11	0h RW/1C	**err_id:** Set if packet header has a unrecognised data id
10	0h RW/1C	**err_crc:** Set if computed CRC differs from received value

Bit Range	Default & Access	Description
9	0h RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0h RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit
7	0h RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits
6	0h RW/1C	**err_control:** Set if DPHY flags a control error
5	0h RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0h RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0h RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state
2	0h RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state
1	0h RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes
0	0h RO	**reserved_10:** Always set to 0

15.8.662 reg_inp_sys_csi_receiver_csi2_int_enable_type (inp_sys_csi_receiver_csi2_int_enable)—Offset 80208h

Interrupt Enable

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi2_int_enable: [ISPMMADR] + 80208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

31:17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused_csi2_int_enable	err_line_sync	err_escape	err_data_timeout	err_frame_data	err_frame_sync	err_id	err_crc	no_ecc_err	err_ecc_corr	err_ecc_double	err_control	err_sot_sync_hs	err_sot_hs	sleep_mode_exit	sleep_mode_entry	err_init_timeout	overrun

Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi2_int_enable:** Unused

Bit Range	Default & Access	Description
16	0h RW	**err_line_sync:** Enable line sync error interrupt
15	0h RW	**err_escape:** Enable escape entry error interrupt
14	0h RW	**err_data_timeout:** Enable timeout error interrupt
13	0h RW	**err_frame_data:** Enable frame data error interrupt
12	0h RW	**err_frame_sync:** Enable frame sync error interrupt
11	0h RW	**err_id:** Enable data id error interrupt
10	0h RW	**err_crc:** Enable CRC error interrupt
9	0h RW	**no_ecc_err:** Enable no ECC error interrupt
8	0h RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0h RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0h RW	**err_control:** Enable control error interrupt
5	0h RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0h RW	**err_sot_hs:** Enable start of transmission error interrupt
3	0h RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0h RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0h RW	**err_init_timeout:** Enable Initialization timeout error interrupt
0	0h RW	**overrun:** Enable FIFO overrun interrupt: NOT available now, can be discarded

15.8.663 reg_inp_sys_csi_receiver_csi2_func_prg_type (inp_sys_csi_receiver_csi2_func_prg)—Offset 8020Ch

Functional Programming

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi2_func_prg: [ISPMMADR] + 8020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 1 1 1 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1

unused_csi2_func_prg | func_prg_reg_2 | func_prg_reg_1 | func_prg_reg_0

Bit Range	Default & Access	Description
31:19	0h RW	**unused_csi2_func_prg:** Unused
18:16	7h RW	**func_prg_reg_2:** Byte 2 for functional programming
15:8	FFh RW	**func_prg_reg_1:** Byte 1 for functional programming
7:0	FFh RW	**func_prg_reg_0:** Byte 0 for functional programming

15.8.664 reg_inp_sys_csi_receiver_csi2_init_cnt_type (inp_sys_csi_receiver_csi2_init_cnt)—Offset 80210h

Duration after power up when DPHY lanes will not be observed

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi2_init_cnt: [ISPMMADR] + 80210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_csi2_init_cnt | init_timer_reg_1 | init_timer_reg_0

Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi2_init_cnt:** Unused
15:8	0h RW	**init_timer_reg_1:** Byte 1 for power up timer

Bit Range	Default & Access	Description
7:0	0h RW	**init_timer_reg_0:** Byte 0 for power up timer

15.8.665 reg_inp_sys_csi_receiver_csi2_raw16_18_data_id_type (inp_sys_csi_receiver_csi2_raw16_18_data_id)—Offset 80238h

RAW 16 and RAW 18 data ID register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi2_raw16_18_data_id: [ISPMMADR] + 80238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_csi2_raw16_18_data_id																reserved_1514		raw18						reserved_76		raw16					

Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi2_raw16_18_data_id:** Unused
15:14	0h RO	**reserved_1514:** Reserved
13:8	0h RW	**raw18:** RAW 18 data ID
7:6	0h RO	**reserved_76:** Reserved
5:0	0h RW	**raw16:** RAW 16 data ID

15.8.666 reg_inp_sys_csi_receiver_csi2_sync_cnt_type (inp_sys_csi_receiver_csi2_sync_cnt)—Offset 8023Ch

Synchronisation count value in terms of MIPI high speed byte clock

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi2_sync_cnt: [ISPMMADR] + 8023Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000FFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
unused_csi2_sync_cnt																								sync_cnt_1lane							

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi2_sync_cnt:** Unused
7:0	FFh RW	**sync_cnt_1lane:** Synchronisation count value for 1 lane

15.8.667 reg_inp_sys_csi_receiver_csi2_rx_cnt_type (inp_sys_csi_receiver_csi2_rx_cnt)—Offset 80240h

Receive count value in terms of MIPI high speed byte clock

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi2_rx_cnt: [ISPMMADR] + 80240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000FFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
unused_csi2_rx_cnt																								rx_cnt_1lane							

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi2_rx_cnt:** Unused
7:0	FFh RW	**rx_cnt_1lane:** Receive count value for 1 lane

15.8.668 reg_inp_sys_csi_receiver_csi3_dev_ready_type (inp_sys_csi_receiver_csi3_dev_ready)—Offset 80300h

Set after programming operational registers to enable receiver

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**inp_sys_csi_receiver_csi3_dev_ready:** [ISPMMADR] + 80300h **ISPMMADR Type:** PCI Configuration Register (Size: 32 bits) **ISPMMADR Reference:** [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	7	6	5	4	3	2	1	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0		0	0	0	0	0	0	0	0
unused_csi3_dev_ready							mask_data_id_err	mask_ecc_double_bit_err	mask_rx_data_timeout_err	mask_sot_sync_err	mask_overrun_err	mask_init_time_out_err	reserved_1	device_ready

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi3_dev_ready:** Unused
7	0h RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0h RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0h RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0h RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0h RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded
2	0h RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0h RO	**reserved_1:** Reserved
0	0h RW	**device_ready:** Set to indicate that device is ready for reception

15.8.669 reg_inp_sys_csi_receiver_csi3_int_status_type (inp_sys_csi_receiver_csi3_int_status)—Offset 80304h

Interrupt Status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi3_int_status: [ISPMMADR] + 80304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	unused_csi3_int_status	err_line_sync	err_escape	err_data_timeout	err_frame_data	err_frame_sync	err_id	err_crc	no_ecc_err	err_ecc_corr	err_ecc_double	err_control	err_sot_sync_hs	err_sot_hs	sleep_mode_exit	sleep_mode_entry	err_init_timeout	reserved_10

Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi3_int_status:** Unused
16	0h RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0h RW/1C	**err_escape:** Set if an unrecognised escape entry command is received
14	0h RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0h RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0h RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel
11	0h RW/1C	**err_id:** Set if packet header has a unrecognised data id
10	0h RW/1C	**err_crc:** Set if computed CRC differs from received value
9	0h RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0h RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit
7	0h RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits
6	0h RW/1C	**err_control:** Set if DPHY flags a control error
5	0h RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0h RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0h RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state

Bit Range	Default & Access	Description
2	0h RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state
1	0h RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes
0	0h RO	**reserved_10:** Always set to 0

15.8.670 reg_inp_sys_csi_receiver_csi3_int_enable_type (inp_sys_csi_receiver_csi3_int_enable)—Offset 80308h

Interrupt Enable

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_int_enable: [ISPMMADR] + 80308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	unused_csi3_int_enable	err_line_sync	err_escape	err_data_timeout	err_frame_data	err_frame_sync	err_id	err_crc	no_ecc_err	err_ecc_corr	err_ecc_double	err_control	err_sot_sync_hs	err_sot_hs	sleep_mode_exit	sleep_mode_entry	err_init_timeout	overrun

Bit Range	Default & Access	Description
31:17	0h RW	**unused_csi3_int_enable:** Unused
16	0h RW	**err_line_sync:** Enable line sync error interrupt
15	0h RW	**err_escape:** Enable escape entry error interrupt
14	0h RW	**err_data_timeout:** Enable timeout error interrupt
13	0h RW	**err_frame_data:** Enable frame data error interrupt
12	0h RW	**err_frame_sync:** Enable frame sync error interrupt
11	0h RW	**err_id:** Enable data id error interrupt
10	0h RW	**err_crc:** Enable CRC error interrupt

Bit Range	Default & Access	Description
9	0h RW	**no_ecc_err:** Enable no ECC error interrupt
8	0h RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0h RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0h RW	**err_control:** Enable control error interrupt
5	0h RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0h RW	**err_sot_hs:** Enable start of transmission error interrupt
3	0h RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0h RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0h RW	**err_init_timeout:** Enable Initialization timeout error interrupt
0	0h RW	**overrun:** Enable FIFO overrun interrupt: NOT available now, can be discarded

15.8.671 reg_inp_sys_csi_receiver_csi3_func_prg_type (inp_sys_csi_receiver_csi3_func_prg)—Offset 8030Ch

Functional Programming

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi3_func_prg: [ISPMMADR] + 8030Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 1 1 1 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1 | 1 1 1 1

unused_csi3_func_prg | func_prg_reg_2 | func_prg_reg_1 | func_prg_reg_0

Bit Range	Default & Access	Description
31:19	0h RW	**unused_csi3_func_prg:** Unused

Bit Range	Default & Access	Description
18:16	7h RW	**func_prg_reg_2:** Byte 2 for functional programming
15:8	FFh RW	**func_prg_reg_1:** Byte 1 for functional programming
7:0	FFh RW	**func_prg_reg_0:** Byte 0 for functional programming

15.8.672 reg_inp_sys_csi_receiver_csi3_init_cnt_type (inp_sys_csi_receiver_csi3_init_cnt)—Offset 80310h

Duration after power up when DPHY lanes will not be observed

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi3_init_cnt: [ISPMMADR] + 80310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_csi3_init_cnt																init_timer_reg_1								init_timer_reg_0							

Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi3_init_cnt:** Unused
15:8	0h RW	**init_timer_reg_1:** Byte 1 for power up timer
7:0	0h RW	**init_timer_reg_0:** Byte 0 for power up timer

15.8.673 reg_inp_sys_csi_receiver_csi3_raw16_18_data_id_type (inp_sys_csi_receiver_csi3_raw16_18_data_id)—Offset 80338h

RAW 16 and RAW 18 data ID register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_raw16_18_data_id: [ISPMMADR] + 80338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_csi3_raw16_18_data_id (31:16), reserved_1514 (15:14), raw18 (13:8), reserved_76 (7:6), raw16 (5:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi3_raw16_18_data_id:** Unused
15:14	0h RO	**reserved_1514:** Reserved
13:8	0h RW	**raw18:** RAW 18 data ID
7:6	0h RO	**reserved_76:** Reserved
5:0	0h RW	**raw16:** RAW 16 data ID

15.8.674 reg_inp_sys_csi_receiver_csi3_sync_cnt_type (inp_sys_csi_receiver_csi3_sync_cnt)—Offset 8033Ch

Synchronisation count value in terms of MIPI high speed byte clock

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi3_sync_cnt: [ISPMMADR] + 8033Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

31:16	15:8	7:0
unused_csi3_sync_cnt	sync_cnt_2lane	sync_cnt_1lane

Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi3_sync_cnt:** Unused
15:8	FFh RW	**sync_cnt_2lane:** Synchronisation count value for 2 lane
7:0	FFh RW	**sync_cnt_1lane:** Synchronisation count value for 1 lane

15.8.675 reg_inp_sys_csi_receiver_csi3_rx_cnt_type (inp_sys_csi_receiver_csi3_rx_cnt)—Offset 80340h

Receive count value in terms of MIPI high speed byte clock

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi3_rx_cnt: [ISPMMADR] + 80340h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:8	7:0
unused_csi3_rx_cnt	rx_cnt_2lane	rx_cnt_1lane

Bit Range	Default & Access	Description
31:16	0h RW	**unused_csi3_rx_cnt:** Unused
15:8	0h RW	**rx_cnt_2lane:** Receive count value for 2 lane
7:0	0h RW	**rx_cnt_1lane:** Receive count value for 1 lane

15.8.676 reg_inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl_type (inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl)—Offset 80800h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl: [ISPMMADR] + 80800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_csi_be_gen_sh_acc_ovl (bits 31:1), csi_be_gen_sh_acc_ovl (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_be_gen_sh_acc_ovl:** Unused
0	0h RW	**csi_be_gen_sh_acc_ovl:** Allows for overruling the accept signal generated by the generic short packet FIFO, going to the CSI receiver backend.

15.8.677 reg_inp_sys_csi_receiver_csi_sh_be_srst_type (inp_sys_csi_receiver_csi_sh_be_srst)—Offset 80804h

soft reset modules of the SH CSI receiver Back End

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_srst: [ISPMMADR] + 80804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bit	31:8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
Field	unused_csi_sh_be_srst	srst_be_controller	srst_one_2_two_channel	srst_stream_demux	srst_pixel_decoder	srst_stream_mux	srst_pixel_formatter	srst_rate_conversion_fifo	srst_header_extractor

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_sh_be_srst:** Unused
7	0h RW	**srst_be_controller:** Soft resets the backend controller module
6	0h RW	**srst_one_2_two_channel:** Soft resets the one 2 two channel module
5	0h RW	**srst_stream_demux:** Soft resets the stream demux module
4	0h RW	**srst_pixel_decoder:** Soft resets the pixel decoder module
3	0h RW	**srst_stream_mux:** Soft resets the stream mux module
2	0h RW	**srst_pixel_formatter:** Soft resets the pixel formatter module
1	0h RW	**srst_rate_conversion_fifo:** Soft resets the rate conversion FIFO module
0	0h RW	**srst_header_extractor:** Soft resets the header extractor module

15.8.678 reg_inp_sys_csi_receiver_csi_sh_be_two_ppc_type (inp_sys_csi_receiver_csi_sh_be_two_ppc)—Offset 80808h

Sets the output rate of the backend and the precision

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_two_ppc: [ISPMMADR] + 80808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_csi_sh_be_two_ppc | high_precision | use_both_ports

Bit Range	Default & Access	Description
31:2	0h RW	**unused_csi_sh_be_two_ppc:** Unused
1	0h RW	**high_precision:** When '1', (and use_both_ports='1' as well) both ports A and B are used to output one high precision pixel, when '0', high_precision pixels are saturated to fit on one port.
0	0h RW	**use_both_ports:** When '1', both ports A and B are active. When '0' only port A is active

15.8.679 reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0)—Offset 8080Ch

Compression scheme register for virtual channel 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0:
[ISPMMADR] + 8080Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

pred_usd_type8 | comp_usd_type8 | pred_usd_type7 | comp_usd_type7 | pred_usd_type6 | comp_usd_type6 | pred_usd_type5 | comp_usd_type5 | pred_usd_type4 | comp_usd_type4 | pred_usd_type3 | comp_usd_type3 | pred_usd_type2 | comp_usd_type2 | pred_usd_type1 | comp_usd_type1

Bit Range	Default & Access	Description
31	0h RW	**pred_usd_type8:** prediction algorithm for vc=0, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0h RW	**comp_usd_type8:** compression format for vc=0, user defined type 8 data: value between 0 to 6. 0-no compression

Bit Range	Default & Access	Description
27	0h RW	**pred_usd_type7:** prediction algorithm for vc=0, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0h RW	**comp_usd_type7:** compression format for vc=0, user defined type 7 data: value between 0 to 6. 0-no compression
23	0h RW	**pred_usd_type6:** prediction algorithm for vc=0, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0h RW	**comp_usd_type6:** compression format for vc=0, user defined type 6 data: value between 0 to 6. 0-no compression
19	0h RW	**pred_usd_type5:** prediction algorithm for vc=0, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0h RW	**comp_usd_type5:** compression format for vc=0, user defined type 5 data: value between 0 to 6. 0-no compression
15	0h RW	**pred_usd_type4:** prediction algorithm for vc=0, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0h RW	**comp_usd_type4:** compression format for vc=0, user defined type 4 data: value between 0 to 6. 0-no compression
11	0h RW	**pred_usd_type3:** prediction algorithm for vc=0, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0h RW	**comp_usd_type3:** compression format for vc=0, user defined type 3 data: value between 0 to 6. 0-no compression
7	0h RW	**pred_usd_type2:** prediction algorithm for vc=0, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0h RW	**comp_usd_type2:** compression format for vc=0, user defined type 2 data: value between 0 to 6. 0-no compression
3	0h RW	**pred_usd_type1:** prediction algorithm for vc=0, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for vc=0, user defined type 1 data: value between 0 to 6. 0-no compression

15.8.680 reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1)—Offset 80810h

Compression scheme register for virtual channel 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1: [ISPMMADR] + 80810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
pred_usd_type8	comp_usd_type8			pred_usd_type7	comp_usd_type7			pred_usd_type6	comp_usd_type6			pred_usd_type5	comp_usd_type5			pred_usd_type4	comp_usd_type4			pred_usd_type3	comp_usd_type3			pred_usd_type2	comp_usd_type2			pred_usd_type1	comp_usd_type1		

Bit Range	Default & Access	Description
31	0h RW	**pred_usd_type8:** prediction algorithm for vc=1, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0h RW	**comp_usd_type8:** compression format for vc=1, user defined type 8 data: value between 0 to 6. 0-no compression
27	0h RW	**pred_usd_type7:** prediction algorithm for vc=1, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0h RW	**comp_usd_type7:** compression format for vc=1, user defined type 7 data: value between 0 to 6. 0-no compression
23	0h RW	**pred_usd_type6:** prediction algorithm for vc=1, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0h RW	**comp_usd_type6:** compression format for vc=1, user defined type 6 data: value between 0 to 6. 0-no compression
19	0h RW	**pred_usd_type5:** prediction algorithm for vc=1, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0h RW	**comp_usd_type5:** compression format for vc=1, user defined type 5 data: value between 0 to 6. 0-no compression
15	0h RW	**pred_usd_type4:** prediction algorithm for vc=1, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0h RW	**comp_usd_type4:** compression format for vc=1, user defined type 4 data: value between 0 to 6. 0-no compression
11	0h RW	**pred_usd_type3:** prediction algorithm for vc=1, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0h RW	**comp_usd_type3:** compression format for vc=1, user defined type 3 data: value between 0 to 6. 0-no compression
7	0h RW	**pred_usd_type2:** prediction algorithm for vc=1, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0h RW	**comp_usd_type2:** compression format for vc=1, user defined type 2 data: value between 0 to 6. 0-no compression
3	0h RW	**pred_usd_type1:** prediction algorithm for vc=1, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for vc=1, user defined type 1 data: value between 0 to 6. 0-no compression

15.8.681 reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2)—Offset 80814h

Compression scheme register for virtual channel 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2:** [ISPMMADR] + 80814h
	ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
	ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30:28	27	26:24	23	22:20	19	18:16	15	14:12	11	10:8	7	6:4	3	2:0
0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0
pred_usd_type8	comp_usd_type8	pred_usd_type7	comp_usd_type7	pred_usd_type6	comp_usd_type6	pred_usd_type5	comp_usd_type5	pred_usd_type4	comp_usd_type4	pred_usd_type3	comp_usd_type3	pred_usd_type2	comp_usd_type2	pred_usd_type1	comp_usd_type1

Bit Range	Default & Access	Description
31	0h RW	**pred_usd_type8:** prediction algorithm for vc=2, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0h RW	**comp_usd_type8:** compression format for vc=2, user defined type 8 data: value between 0 to 6. 0-no compression
27	0h RW	**pred_usd_type7:** prediction algorithm for vc=2, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0h RW	**comp_usd_type7:** compression format for vc=2, user defined type 7 data: value between 0 to 6. 0-no compression
23	0h RW	**pred_usd_type6:** prediction algorithm for vc=2, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0h RW	**comp_usd_type6:** compression format for vc=2, user defined type 6 data: value between 0 to 6. 0-no compression
19	0h RW	**pred_usd_type5:** prediction algorithm for vc=2, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0h RW	**comp_usd_type5:** compression format for vc=2, user defined type 5 data: value between 0 to 6. 0-no compression
15	0h RW	**pred_usd_type4:** prediction algorithm for vc=2, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0h RW	**comp_usd_type4:** compression format for vc=2, user defined type 4 data: value between 0 to 6. 0-no compression
11	0h RW	**pred_usd_type3:** prediction algorithm for vc=2, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0h RW	**comp_usd_type3:** compression format for vc=2, user defined type 3 data: value between 0 to 6. 0-no compression
7	0h RW	**pred_usd_type2:** prediction algorithm for vc=2, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0h RW	**comp_usd_type2:** compression format for vc=2, user defined type 2 data: value between 0 to 6. 0-no compression
3	0h RW	**pred_usd_type1:** prediction algorithm for vc=2, user defined type 1 data: 0 -) pred1, 1 -) pred2

Bit Range	Default & Access	Description
2:0	0h RW	**comp_usd_type1:** compression format for vc=2, user defined type 1 data: value between 0 to 6. 0-no compression

15.8.682 reg_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3_type (inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3)—Offset 80818h

Compression scheme register for virtual channel 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3: [ISPMMADR] + 80818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31	30:28	27	26:24	23	22:20	19	18:16	15	14:12	11	10:8	7	6:4	3	2:0
Default	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0	0	0 0 0
Field	pred_usd_type8	comp_usd_type8	pred_usd_type7	comp_usd_type7	pred_usd_type6	comp_usd_type6	pred_usd_type5	comp_usd_type5	pred_usd_type4	comp_usd_type4	pred_usd_type3	comp_usd_type3	pred_usd_type2	comp_usd_type2	pred_usd_type1	comp_usd_type1

Bit Range	Default & Access	Description
31	0h RW	**pred_usd_type8:** prediction algorithm for vc=3, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0h RW	**comp_usd_type8:** compression format for vc=3, user defined type 8 data: value between 0 to 6. 0-no compression
27	0h RW	**pred_usd_type7:** prediction algorithm for vc=3, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0h RW	**comp_usd_type7:** compression format for vc=3, user defined type 7 data: value between 0 to 6. 0-no compression
23	0h RW	**pred_usd_type6:** prediction algorithm for vc=3, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0h RW	**comp_usd_type6:** compression format for vc=3, user defined type 6 data: value between 0 to 6. 0-no compression
19	0h RW	**pred_usd_type5:** prediction algorithm for vc=3, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0h RW	**comp_usd_type5:** compression format for vc=3, user defined type 5 data: value between 0 to 6. 0-no compression
15	0h RW	**pred_usd_type4:** prediction algorithm for vc=3, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0h RW	**comp_usd_type4:** compression format for vc=3, user defined type 4 data: value between 0 to 6. 0-no compression

Bit Range	Default & Access	Description
11	0h RW	**pred_usd_type3:** prediction algorithm for vc=3, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0h RW	**comp_usd_type3:** compression format for vc=3, user defined type 3 data: value between 0 to 6. 0-no compression
7	0h RW	**pred_usd_type2:** prediction algorithm for vc=3, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0h RW	**comp_usd_type2:** compression format for vc=3, user defined type 2 data: value between 0 to 6. 0-no compression
3	0h RW	**pred_usd_type1:** prediction algorithm for vc=3, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0h RW	**comp_usd_type1:** compression format for vc=3, user defined type 1 data: value between 0 to 6. 0-no compression

15.8.683 reg_inp_sys_csi_receiver_csi_sh_be_sel_be_type (inp_sys_csi_receiver_csi_sh_be_sel_be)—Offset 8081Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_sel_be: [ISPMMADR] + 8081Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_sh_be_sel_be (bits 31:1); csi_sh_be_sel_be (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_csi_sh_be_sel_be:** Unused
0	0h RW	**csi_sh_be_sel_be:** Selects which CSI Receiver Backend to use 0-Arasan Backend, 1-Silicon Hive Backend

15.8.684 reg_inp_sys_csi_receiver_csi_sh_be_raw16_reg_type (inp_sys_csi_receiver_csi_sh_be_raw16_reg)—Offset 80820h

Configuration register for RAW 16 data type decode

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_raw16_reg: [ISPMMADR] + 80820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_sh_be_raw16_reg | format_en | format_id

Bit Range	Default & Access	Description
31:7	0h RW	**unused_csi_sh_be_raw16_reg:** Unused
6	0h RW	**format_en:** enable RAW 16 type decode
5:0	0h RW	**format_id:** data id for RAW 16

15.8.685 reg_inp_sys_csi_receiver_csi_sh_be_raw18_reg_type (inp_sys_csi_receiver_csi_sh_be_raw18_reg)—Offset 80824h

Configuration register for RAW 18 data type decode

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_raw18_reg: [ISPMMADR] + 80824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_sh_be_raw18_reg | format_en | format_option | format_id

Bit Range	Default & Access	Description
31:9	0h RW	**unused_csi_sh_be_raw18_reg:** Unused
8	0h RW	**format_en:** enable RAW 16 type decode
7:6	0h RW	**format_option:** format option for RAW 18 data type: 3 options possible (1,2,3)
5:0	0h RW	**format_id:** data id for RAW 16

15.8.686 reg_inp_sys_csi_receiver_csi_sh_be_force_raw8_reg_type (inp_sys_csi_receiver_csi_sh_be_force_raw8_reg)—Offset 80828h

Force RAW8(byte) decoding for LONG data packets

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_force_raw8_reg:
[ISPMMADR] + 80828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_sh_be_force_raw8_reg | force_data_id | option_enable

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_sh_be_force_raw8_reg:** Unused
7:2	0h RW	**force_data_id:** Data_id that should be forced to RAW8
1:0	0h RW	**option_enable:** 00-Do not force anything in RAW8 mode. 01-force all data types in RAW8 mode, 11-force only packets with data_id force_data_id to RAW8 mode

15.8.687 reg_inp_sys_csi_receiver_csi_sh_be_irq_stat_reg_type (inp_sys_csi_receiver_csi_sh_be_irq_stat_reg)—Offset 8082Ch

IRQ status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_irq_stat_reg: [ISPMMADR] + 8082Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_csi_sh_be_irq_stat_reg (bits 31:2), irq_premature_sop (bit 1), irq_missing_sop (bit 0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_csi_sh_be_irq_stat_reg:** Unused
1	0h RO	**irq_premature_sop:** If '1', sh_be has detected a premature sop
0	0h RO	**irq_missing_sop:** If '1', sh_be has detected a missing sop

15.8.688 reg_inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg_type (inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg)—Offset 80830h

IRQ status clear register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg:
[ISPMMADR] + 80830h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_csi_sh_be_irq_stat_clear_reg (bits 31:2), irq_premature_sop (bit 1), irq_missing_sop (bit 0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_csi_sh_be_irq_stat_clear_reg:** Unused
1	0h WO	**irq_premature_sop:** A '1' written into this field, clears the premature_sop field to '0'
0	0h WO	**irq_missing_sop:** A '1' written into this field, clears the irq_missing_sop field to '0'

15.8.689 reg_inp_sys_csi_receiver_csi_sh_be_custom_enable_reg_type (inp_sys_csi_receiver_csi_sh_be_custom_enable_reg)—Offset 80834h

Enable custom mode decoding for LONG data packets

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_csi_receiver_csi_sh_be_custom_enable_reg:
[ISPMMADR] + 80834h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_csi_sh_be_custom_enable_reg | custom_data_id | option_enable

Bit Range	Default & Access	Description
31:8	0h RW	**unused_csi_sh_be_custom_enable_reg:** Unused
7:2	0h RW	**custom_data_id:** Data_id that should be processed in custom mode
1:0	0h RW	**option_enable:** 00-Custom mode switched off. 01-all data types in custom mode, 11-only packets with data id custom_data_id are processed in custom mode

15.8.690 reg_inp_sys_capt_unit_a_reg_CaptStartMode_type (inp_sys_capt_unit_a_reg_CaptStartMode)—Offset 81000h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_CaptStartMode: [ISPMMADR] + 81000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_CaptStartMode | reg_CaptStartMode

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_CaptStartMode:** Unused
0	0h RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

15.8.691 reg_inp_sys_capt_unit_a_reg_Capt_Start_Addr_type (inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Start_Addr: [ISPMMADR] + 81004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_Capt_Start_Addr | reg_Capt_Start_Addr

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Start_Addr:** Unused
8:0	0h RW	**reg_Capt_Start_Addr:** Start Address of first memory region

15.8.692 reg_inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size)—Offset 81008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size: [ISPMMADR] + 81008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Fields: unused_reg_Capt_Mem_Region_Size (bits 31:9), reg_Capt_Mem_Region_Size (bits 8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Mem_Region_Size:** Unused
8:0	080h RW	**reg_Capt_Mem_Region_Size:** Memory region size

15.8.693 reg_inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions)—Offset 8100Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions:
[ISPMMADR] + 8100Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Fields: unused_reg_Capt_Num_Mem_Regions (bits 31:9), reg_Capt_Num_Mem_Regions (bits 8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Num_Mem_Regions:** Unused
8:0	003h RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

15.8.694 reg_inp_sys_capt_unit_a_reg_Capt_Init_type (inp_sys_capt_unit_a_reg_Capt_Init)—Offset 81010h

Initialize Capture Unit

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Init: [ISPMMADR] + 81010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_Capt_Init	restart_mem_reg_id	restart_mem_addr	restart	resync	flush	reset_reg

Bit Range	Default & Access	Description
31:22	0h RW	**unused_reg_Capt_Init:** Unused
21:13	0h WO	**restart_mem_reg_id:** Restart Memory Region ID
12:4	0h WO	**restart_mem_addr:** Restart Memory Address
3	0h WO	**restart:** Restart Capture Unit
2	0h WO	**resync:** Resynchronize Capture Unit
1	0h WO	**flush:** Flush Internal Buffers
0	0h WO	**reset_reg:** Reset Status Registers

15.8.695 reg_inp_sys_capt_unit_a_reg_Capt_Start_type (inp_sys_capt_unit_a_reg_Capt_Start)—Offset 81014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Start: [ISPMMADR] + 81014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: bits 31:1 unused_reg_Capt_Start; bit 0 reg_Capt_Start

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Start:** Unused
0	0h WO	**reg_Capt_Start:** Start Capturing

15.8.696 reg_inp_sys_capt_unit_a_reg_Capt_Stop_type (inp_sys_capt_unit_a_reg_Capt_Stop)—Offset 81018h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Stop: [ISPMMADR] + 81018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: bits 31:1 unused_reg_Capt_Stop; bit 0 reg_Capt_Stop

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Stop:** Unused
0	0h WO	**reg_Capt_Stop:** Stop Capturing

15.8.697 reg_inp_sys_capt_unit_a_reg_Capt_Packet_Length_type (inp_sys_capt_unit_a_reg_Capt_Packet_Length)—Offset 8101Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Packet_Length:
[ISPMMADR] + 8101Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Packet_Length

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

15.8.698 reg_inp_sys_capt_unit_a_reg_Capt_Received_Length_type (inp_sys_capt_unit_a_reg_Capt_Received_Length)—Offset 81020h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Received_Length:
[ISPMMADR] + 81020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Length

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

15.8.699 reg_inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets)—Offset 81024h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets:
[ISPMMADR] + 81024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Short_Packets

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

15.8.700 reg_inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets)—Offset 81028h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets:
[ISPMMADR] + 81028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Long_Packets

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

15.8.701 reg_inp_sys_capt_unit_a_reg_Capt_Last_Command_type (inp_sys_capt_unit_a_reg_Capt_Last_Command)—Offset 8102Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Last_Command: [ISPMMADR] + 8102Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Last_Command

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Command:** Last command token accepted

15.8.702 reg_inp_sys_capt_unit_a_reg_Capt_Next_Command_type (inp_sys_capt_unit_a_reg_Capt_Next_Command)—Offset 81030h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Next_Command:
[ISPMMADR] + 81030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Next_Command

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Command:** Next command token to be accepted

15.8.703 reg_inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge)—Offset 81034h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge:
[ISPMMADR] + 81034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Last_Acknowledge

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

15.8.704 reg_inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge)—Offset 81038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge: [ISPMMADR] + 81038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Next_Acknowledge

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

15.8.705 reg_inp_sys_capt_unit_a_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_a_reg_Capt_FSM_State_Info)—Offset 8103Ch

Capture Unit State Machine Information

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_a_reg_Capt_FSM_State_Info: [ISPMMADR] + 8103Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_reg_Capt_FSM_State_Info	synchronizer_fsm_ps	synchronizer_fsm_s	synchronizer_fsm_ns	write2mem_fsm_ps	write2mem_fsm_s	write2mem_fsm_ns

Bit Range	Default & Access	Description
31:15	0h RW	**unused_reg_Capt_FSM_State_Info:** Unused
14:12	0h RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
11:9	0h RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
8:6	0h RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0h RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine
3:2	0h RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine
1:0	0h RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine

15.8.706 reg_inp_sys_capt_unit_b_reg_CaptStartMode_type (inp_sys_capt_unit_b_reg_CaptStartMode)—Offset 82000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_CaptStartMode: [ISPMMADR] + 82000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_CaptStartMode | reg_CaptStartMode

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_CaptStartMode:** Unused
0	0h RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

15.8.707 reg_inp_sys_capt_unit_b_reg_Capt_Start_Addr_type (inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Start_Addr: [ISPMMADR] + 82004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_Capt_Start_Addr | reg_Capt_Start_Addr

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Start_Addr:** Unused
8:0	0h RW	**reg_Capt_Start_Addr:** Start Address of first memory region

15.8.708 reg_inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size)—Offset 82008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size: [ISPMMADR] + 82008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0

Fields: unused_reg_Capt_Mem_Region_Size (bits 31:9); reg_Capt_Mem_Region_Size (bits 8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Mem_Region_Size:** Unused
8:0	080h RW	**reg_Capt_Mem_Region_Size:** Memory region size

15.8.709 reg_inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions)—Offset 8200Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions: [ISPMMADR] + 8200Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h

31	28	24	20	16	12	8	4	0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

unused_reg_Capt_Num_Mem_Regions (31:9) | reg_Capt_Num_Mem_Regions (8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Num_Mem_Regions:** Unused
8:0	003h RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

15.8.710 reg_inp_sys_capt_unit_b_reg_Capt_Init_type (inp_sys_capt_unit_b_reg_Capt_Init)—Offset 82010h

Initialize Capture Unit

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Init: [ISPMMADR] + 82010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

unused_reg_Capt_Init (31:22) | restart_mem_reg_id (21:13) | restart_mem_addr (12:4) | restart (3) | resync (2) | flush (1) | reset_reg (0)

Bit Range	Default & Access	Description
31:22	0h RW	**unused_reg_Capt_Init:** Unused
21:13	0h WO	**restart_mem_reg_id:** Restart Memory Region ID

Bit Range	Default & Access	Description
12:4	0h WO	**restart_mem_addr:** Restart Memory Address
3	0h WO	**restart:** Restart Capture Unit
2	0h WO	**resync:** Resynchronize Capture Unit
1	0h WO	**flush:** Flush Internal Buffers
0	0h WO	**reset_reg:** Reset Status Registers

15.8.711 reg_inp_sys_capt_unit_b_reg_Capt_Start_type (inp_sys_capt_unit_b_reg_Capt_Start)—Offset 82014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Start: [ISPMMADR] + 82014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1: unused_reg_Capt_Start; Bit 0: reg_Capt_Start

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Start:** Unused
0	0h WO	**reg_Capt_Start:** Start Capturing

15.8.712 reg_inp_sys_capt_unit_b_reg_Capt_Stop_type (inp_sys_capt_unit_b_reg_Capt_Stop)—Offset 82018h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Stop: [ISPMMADR] + 82018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_Capt_Stop

reg_Capt_Stop

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Stop:** Unused
0	0h WO	**reg_Capt_Stop:** Stop Capturing

15.8.713 reg_inp_sys_capt_unit_b_reg_Capt_Packet_Length_type (inp_sys_capt_unit_b_reg_Capt_Packet_Length)—Offset 8201Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Packet_Length: [ISPMMADR] + 8201Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Packet_Length

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

15.8.714 reg_inp_sys_capt_unit_b_reg_Capt_Received_Length_type (inp_sys_capt_unit_b_reg_Capt_Received_Length)—Offset 82020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Received_Length: [ISPMMADR] + 82020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Length

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

15.8.715 reg_inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets)—Offset 82024h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets: [ISPMMADR] + 82024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Short_Packets

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

15.8.716 reg_inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets)—Offset 82028h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets: [ISPMMADR] + 82028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Long_Packets

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

15.8.717 reg_inp_sys_capt_unit_b_reg_Capt_Last_Command_type (inp_sys_capt_unit_b_reg_Capt_Last_Command)—Offset 8202Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Last_Command: [ISPMMADR] + 8202Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Last_Command

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Command:** Last command token accepted

15.8.718 reg_inp_sys_capt_unit_b_reg_Capt_Next_Command_type (inp_sys_capt_unit_b_reg_Capt_Next_Command)—Offset 82030h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Next_Command: [ISPMMADR] + 82030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Next_Command

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Command:** Next command token to be accepted

15.8.719 reg_inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge)—Offset 82034h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge:
[ISPMMADR] + 82034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Last_Acknowledge

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

15.8.720 reg_inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge)—Offset 82038h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge:
[ISPMMADR] + 82038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Next_Acknowledge

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

15.8.721 reg_inp_sys_capt_unit_b_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_b_reg_Capt_FSM_State_Info)—Offset 8203Ch

Capture Unit State Machine Information

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_b_reg_Capt_FSM_State_Info: [ISPMMADR] + 8203Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:15	14:12	11:9	8:6	5:4	3:2	1:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0	0 0 0	0 0 0	0 0	0 0	0 0
unused_reg_Capt_FSM_State_Info	synchronizer_fsm_ps	synchronizer_fsm_s	synchronizer_fsm_ns	write2mem_fsm_ps	write2mem_fsm_s	write2mem_fsm_ns

Bit Range	Default & Access	Description
31:15	0h RW	**unused_reg_Capt_FSM_State_Info:** Unused
14:12	0h RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
11:9	0h RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
8:6	0h RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0h RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine
3:2	0h RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine
1:0	0h RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine

15.8.722 reg_inp_sys_capt_unit_c_reg_CaptStartMode_type (inp_sys_capt_unit_c_reg_CaptStartMode)—Offset 83000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_CaptStartMode: [ISPMMADR] + 83000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_CaptStartMode (bits 31:1), reg_CaptStartMode (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_CaptStartMode:** Unused
0	0h RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

15.8.723 reg_inp_sys_capt_unit_c_reg_Capt_Start_Addr_type (inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Start_Addr: [ISPMMADR] + 83004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_Capt_Start_Addr | reg_Capt_Start_Addr

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Start_Addr:** Unused
8:0	0h RW	**reg_Capt_Start_Addr:** Start Address of first memory region

15.8.724 reg_inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size_type (inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size)—Offset 83008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size: [ISPMMADR] + 83008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

unused_reg_Capt_Mem_Region_Size | reg_Capt_Mem_Region_Size

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Mem_Region_Size:** Unused

Bit Range	Default & Access	Description
8:0	080h RW	**reg_Capt_Mem_Region_Size:** Memory region size

15.8.725 reg_inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions_type (inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions)—Offset 8300Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions: [ISPMMADR] + 8300Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Fields: unused_reg_Capt_Num_Mem_Regions (bits 31:9), reg_Capt_Num_Mem_Regions (bits 8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Capt_Num_Mem_Regions:** Unused
8:0	003h RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

15.8.726 reg_inp_sys_capt_unit_c_reg_Capt_Init_type (inp_sys_capt_unit_c_reg_Capt_Init)—Offset 83010h

Initialize Capture Unit

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Init: [ISPMMADR] + 83010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_reg_Capt_Init	restart_mem_reg_id	restart_mem_addr	restart	resync	flush	reset_reg

Bit Range	Default & Access	Description
31:22	0h RW	**unused_reg_Capt_Init:** Unused
21:13	0h WO	**restart_mem_reg_id:** Restart Memory Region ID
12:4	0h WO	**restart_mem_addr:** Restart Memory Address
3	0h WO	**restart:** Restart Capture Unit
2	0h WO	**resync:** Resynchronize Capture Unit
1	0h WO	**flush:** Flush Internal Buffers
0	0h WO	**reset_reg:** Reset Status Registers

15.8.727 reg_inp_sys_capt_unit_c_reg_Capt_Start_type (inp_sys_capt_unit_c_reg_Capt_Start)—Offset 83014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Start: [ISPMMADR] + 83014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_reg_Capt_Start	reg_Capt_Start

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Start:** Unused
0	0h WO	**reg_Capt_Start:** Start Capturing

15.8.728 reg_inp_sys_capt_unit_c_reg_Capt_Stop_type (inp_sys_capt_unit_c_reg_Capt_Stop)—Offset 83018h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Stop: [ISPMMADR] + 83018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_Capt_Stop (bits 31:1)
reg_Capt_Stop (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_Capt_Stop:** Unused
0	0h WO	**reg_Capt_Stop:** Stop Capturing

15.8.729 reg_inp_sys_capt_unit_c_reg_Capt_Packet_Length_type (inp_sys_capt_unit_c_reg_Capt_Packet_Length)—Offset 8301Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Packet_Length:
[ISPMMADR] + 8301Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Packet_Length

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

15.8.730 reg_inp_sys_capt_unit_c_reg_Capt_Received_Length_type (inp_sys_capt_unit_c_reg_Capt_Received_Length)—Offset 83020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Received_Length: [ISPMMADR] + 83020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Length

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

15.8.731 reg_inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets_type (inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets)—Offset 83024h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets: [ISPMMADR] + 83024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Short_Packets

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

15.8.732 reg_inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets_type (inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets)—Offset 83028h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets: [ISPMMADR] + 83028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Capt_Received_Long_Packets

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

15.8.733 reg_inp_sys_capt_unit_c_reg_Capt_Last_Command_type (inp_sys_capt_unit_c_reg_Capt_Last_Command)—Offset 8302Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Last_Command: [ISPMMADR] + 8302Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Last_Command

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Command:** Last command token accepted

15.8.734 reg_inp_sys_capt_unit_c_reg_Capt_Next_Command_type (inp_sys_capt_unit_c_reg_Capt_Next_Command)—Offset 83030h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Next_Command: [ISPMMADR] + 83030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Next_Command

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Command:** Next command token to be accepted

15.8.735 reg_inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge_type (inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge)—Offset 83034h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge: [ISPMMADR] + 83034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Capt_Last_Acknowledge

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

15.8.736 reg_inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge_type (inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge)—Offset 83038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge: [ISPMMADR] + 83038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Fields: bits 31:0 reg_Capt_Next_Acknowledge

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

15.8.737 reg_inp_sys_capt_unit_c_reg_Capt_FSM_State_Info_type (inp_sys_capt_unit_c_reg_Capt_FSM_State_Info)—Offset 8303Ch

Capture Unit State Machine Information

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_capt_unit_c_reg_Capt_FSM_State_Info: [ISPMMADR] + 8303Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_Capt_FSM_State_Info, synchronizer_fsm_ps, synchronizer_fsm_s, synchronizer_fsm_ns, write2mem_fsm_ps, write2mem_fsm_s, write2mem_fsm_ns

Bit Range	Default & Access	Description
31:15	0h RW	**unused_reg_Capt_FSM_State_Info:** Unused
14:12	0h RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
11:9	0h RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
8:6	0h RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0h RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine
3:2	0h RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine
1:0	0h RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine

15.8.738 reg_inp_sys_acq_unit_reg_Acq_Start_Addr_type (inp_sys_acq_unit_reg_Acq_Start_Addr)—Offset 84000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Start_Addr: [ISPMMADR] + 84000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_reg_Acq_Start_Addr | reg_Acq_Start_Addr

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Acq_Start_Addr:** Unused
8:0	0h RW	**reg_Acq_Start_Addr:** Start Address of first memory region

15.8.739 reg_inp_sys_acq_unit_reg_Acq_Mem_Region_Size_type (inp_sys_acq_unit_reg_Acq_Mem_Region_Size)—Offset 84004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Mem_Region_Size: [ISPMMADR] + 84004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fields: bits 31:9 unused_reg_Acq_Mem_Region_Size; bits 8:0 reg_Acq_Mem_Region_Size

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Acq_Mem_Region_Size:** Unused
8:0	080h RW	**reg_Acq_Mem_Region_Size:** Memory region size

15.8.740 reg_inp_sys_acq_unit_reg_Acq_Num_Mem_Regions_type (inp_sys_acq_unit_reg_Acq_Num_Mem_Regions)—Offset 84008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Num_Mem_Regions: [ISPMMADR] + 84008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

unused_reg_Acq_Num_Mem_Regions | reg_Acq_Num_Mem_Regions

Bit Range	Default & Access	Description
31:9	0h RW	**unused_reg_Acq_Num_Mem_Regions:** Unused
8:0	003h RW	**reg_Acq_Num_Mem_Regions:** Number of memory regions

15.8.741 reg_inp_sys_acq_unit_reg_Acq_Init_type (inp_sys_acq_unit_reg_Acq_Init)—Offset 8400Ch

Initialize Acquisition Unit

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Init: [ISPMMADR] + 8400Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_Acq_Init | resync | RSVD0 | reset_reg

Bit Range	Default & Access	Description
31:3	0h RW	**unused_reg_Acq_Init:** Unused
2	0h WO	**resync:** Resynchronize the Acquisition Unit

Bit Range	Default & Access	Description
1	0b RO	**RSVD0:** Reserved
0	0h WO	**reset_reg:** Reset Status Registers

15.8.742 reg_inp_sys_acq_unit_reg_Acq_Received_Short_Packets_type (inp_sys_acq_unit_reg_Acq_Received_Short_Packets)—Offset 84010h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Received_Short_Packets:
[ISPMMADR] + 84010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Acq_Received_Short_Packets

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Acq_Received_Short_Packets:** Number of received short packets

15.8.743 reg_inp_sys_acq_unit_reg_Acq_Received_Long_Packets_type (inp_sys_acq_unit_reg_Acq_Received_Long_Packets)—Offset 84014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Received_Long_Packets:
[ISPMMADR] + 84014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_Acq_Received_Long_Packets

Bit Range	Default & Access	Description
31:0	0h RO	**reg_Acq_Received_Long_Packets:** Number of received long packets

15.8.744 reg_inp_sys_acq_unit_reg_Acq_Last_Command_type (inp_sys_acq_unit_reg_Acq_Last_Command)—Offset 84018h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Last_Command: [ISPMMADR] + 84018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Acq_Last_Command

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Acq_Last_Command:** Last command token accepted

15.8.745 reg_inp_sys_acq_unit_reg_Acq_Next_Command_type (inp_sys_acq_unit_reg_Acq_Next_Command)—Offset 8401Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Next_Command: [ISPMMADR] + 8401Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Acq_Next_Command

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Acq_Next_Command:** Next command token to be accepted

15.8.746 reg_inp_sys_acq_unit_reg_Acq_Last_Acknowledge_type (inp_sys_acq_unit_reg_Acq_Last_Acknowledge)—Offset 84020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Last_Acknowledge: [ISPMMADR] + 84020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Acq_Last_Acknowledge

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Acq_Last_Acknowledge:** Last acknowledge token send

15.8.747 reg_inp_sys_acq_unit_reg_Acq_Next_Acknowledge_type (inp_sys_acq_unit_reg_Acq_Next_Acknowledge)—Offset 84024h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Next_Acknowledge: [ISPMMADR] + 84024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

reg_Acq_Next_Acknowledge

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**reg_Acq_Next_Acknowledge:** Next acknowledge token to be send

15.8.748 reg_inp_sys_acq_unit_reg_Acq_FSM_State_Info_type (inp_sys_acq_unit_reg_Acq_FSM_State_Info)—Offset 84028h

Acquisition unit State Machine information

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_FSM_State_Info: [ISPMMADR] + 84028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_Acq_FSM_State_Info																				synchronizer_fsm_ps		synchronizer_fsm_s		synchronizer_fsm_ns		mem2stream_fsm_ps		mem2stream_fsm_s		mem2stream_fsm_ns	

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_Acq_FSM_State_Info:** Unused
11:10	0h RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
9:8	0h RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
7:6	0h RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0h RO	**mem2stream_fsm_ps:** Previous state of Mem2Stream State Machine
3:2	0h RO	**mem2stream_fsm_s:** Current state of Mem2Stream State Machine
1:0	0h RO	**mem2stream_fsm_ns:** Next state of Mem2Stream State Machine

15.8.749 reg_inp_sys_acq_unit_reg_Acq_Int_Cntr_Info_type (inp_sys_acq_unit_reg_Acq_Int_Cntr_Info)—Offset 8402Ch

Acq_Int_Cntr_Info

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_acq_unit_reg_Acq_Int_Cntr_Info: [ISPMMADR] + 8402Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

unused_reg_Acq_Int_Cntr_Info	transmit_cntr	RSVD0	superword_cntr	RSVD1	mwp_cntr

Bit Range	Default & Access	Description
31	0h RW	**unused_reg_Acq_Int_Cntr_Info:** Unused
30:28	0h RO	**transmit_cntr:** Counter used for determining which word (part of a superword) to be send
27:25	0b RO	**RSVD0:** Reserved
24:16	0h RO	**superword_cntr:** Counts number of superwords read from wide bus (input buffer)
15:14	0b RO	**RSVD1:** Reserved
13:0	0h RO	**mwp_cntr:** Counts words in multi word packet

15.8.750 reg_inp_sys_dma_DMA_FSM_Command_type (inp_sys_dma_DMA_FSM_Command)—Offset 85000h

FSM Command: Last command and State

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_dma_DMA_FSM_Command: [ISPMMADR] + 85000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

state	unused	Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:16	0h RO	**state:** Lower 16 bits of the last command received and processed

Bit Range	Default & Access	Description
15:4	0h RO	**unused:** unused
3	0h RO	**Error:** Error flag
2	0h RO	**Stall:** Stall flag
1	0h RO	**Run:** Run flag
0	0h RO	**Idle:** Idle flag

15.8.751 reg_inp_sys_dma_DMA_CH0_Packing_setup_type (inp_sys_dma_DMA_CH0_Packing_setup)—Offset 86000h

DMA CH 0 PARAM 0: Packing setup

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_Packing_setup: [ISPMMADR] + 86000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH0_Packing_setup																											ext	unused			conn

Bit Range	Default & Access	Description
31:5	0h RW	**unused_DMA_CH0_Packing_setup:** Unused
4	0h RO	**ext:** Zero(0)/Sign(1) extension
3:1	0h RO	**unused:** unused
0	0h RO	**conn:** Connection ID

15.8.752 reg_inp_sys_dma_DMA_CH0_dev_stride_A_type (inp_sys_dma_DMA_CH0_dev_stride_A)—Offset 86100h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_dev_stride_A: [ISPMMADR] + 86100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_CH0_dev_stride_A

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH0_dev_stride_A:** DMA CH 0 PARAM 1: Device A stride

15.8.753 reg_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A_type (inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 86200h

DMA CH 0 PARAM 2: Device A Packing LSE cropping/Elements

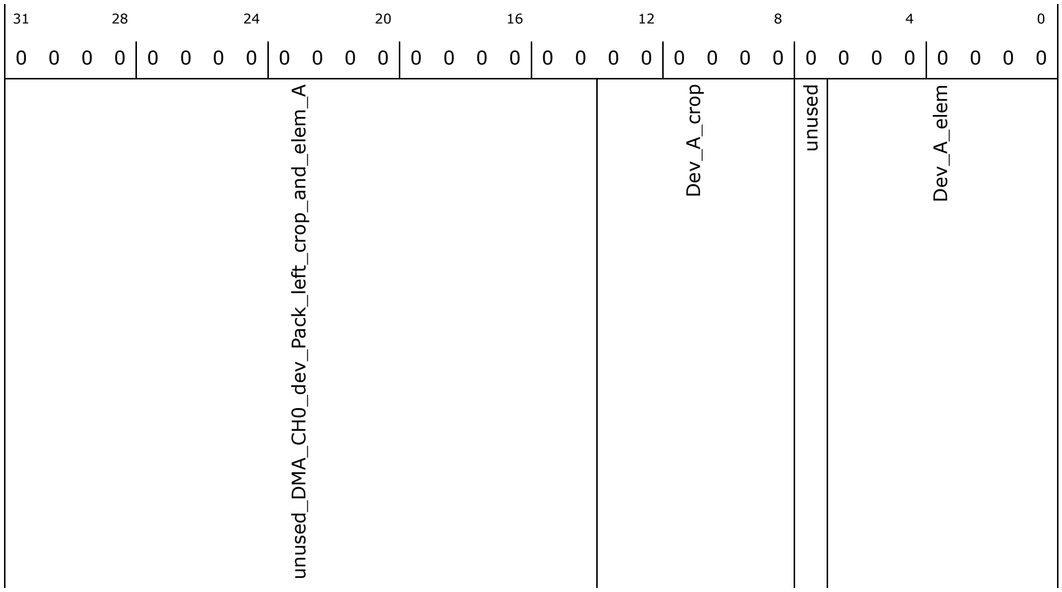
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A: [ISPMMADR] + 86200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH0_dev_Pack_left_crop_and_elem_A:** Unused
13:8	0h RO	**Dev_A_crop:** Device A left element cropping
7	0h RO	**unused:** unused
6:0	0h RO	**Dev_A_elem:** Device A element per word

15.8.754 reg_inp_sys_dma_DMA_CH0_Device_Xb_A_type (inp_sys_dma_DMA_CH0_Device_Xb_A)—Offset 86300h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_Device_Xb_A: [ISPMMADR] + 86300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH0_Device_Xb_A																DMA_CH0_Device_Xb_A															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Device_Xb_A:** Unused
15:0	0h RO	**DMA_CH0_Device_Xb_A:** DMA CH 0 PARAM 3: Device A block width (Xb)

15.8.755 reg_inp_sys_dma_DMA_CH0_dev_stride_B_type (inp_sys_dma_DMA_CH0_dev_stride_B)—Offset 86400h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_dev_stride_B: [ISPMMADR] + 86400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DMA_CH0_dev_stride_B																															

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_CH0_dev_stride_B:** DMA CH 0 PARAM 4: Device B stride

15.8.756 reg_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B_type

(inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 86500h

DMA CH 0 PARAM 5: Device B Packing LSE cropping/Elements

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B : [ISPMMADR] + 86500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:14	13:8	7	6:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0
Field	unused_DMA_CH0_dev_Pack_left_crop_and_elem_B	Dev_B_crop	unused	Dev_B_elem

Bit Range	Default & Access	Description
31:14	0h RW	**unused_DMA_CH0_dev_Pack_left_crop_and_elem_B:** Unused
13:8	0h RO	**Dev_B_crop:** Device B left element cropping
7	0h RO	**unused:** unused
6:0	0h RO	**Dev_B_elem:** Device B element per word

15.8.757 reg_inp_sys_dma_DMA_CH0_Device_Xb_B_type (inp_sys_dma_DMA_CH0_Device_Xb_B)—Offset 86600h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_Device_Xb_B: [ISPMMADR] + 86600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH0_Device_Xb_B (31:16), DMA_CH0_Device_Xb_B (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Device_Xb_B:** Unused
15:0	0h RO	**DMA_CH0_Device_Xb_B:** DMA CH 0 PARAM 6: Device B block width (Xb)

15.8.758 reg_inp_sys_dma_DMA_CH0_Yb_type (inp_sys_dma_DMA_CH0_Yb)—Offset 86700h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_Yb: [ISPMMADR] + 86700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_CH0_Yb (31:16), DMA_CH0_Yb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_CH0_Yb:** Unused
15:0	0h RO	**DMA_CH0_Yb:** DMA CH 0 PARAM 7: block Height (Yb)

15.8.759 reg_inp_sys_dma_DMA_CH0_pending_command_type (inp_sys_dma_DMA_CH0_pending_command)—Offset 86800h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_CH0_pending_command: [ISPMMADR] + 86800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_CH0_pending_command																												DMA_CH0_pending_command			

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_CH0_pending_command:** Unused
3:0	0h RO	**DMA_CH0_pending_command:** DMA CH 0 PARAM 8: Pending commands which will use channel 0

15.8.760 reg_inp_sys_dma_DMA_command_token_type (inp_sys_dma_DMA_command_token)—Offset 87000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_command_token: [ISPMMADR] + 87000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DMA_command_token																															

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_token:** Pending or last executed command token

15.8.761 reg_inp_sys_dma_DMA_command_src_addr_type (inp_sys_dma_DMA_command_src_addr)—Offset 87004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_command_src_addr: [ISPMMADR] + 87004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DMA_command_src_addr																															

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_src_addr:** Source address of the pending or last executed command token

15.8.762 reg_inp_sys_dma_DMA_command_dst_addr_type (inp_sys_dma_DMA_command_dst_addr)—Offset 87008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_command_dst_addr: [ISPMMADR] + 87008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_command_dst_addr

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_command_dst_addr:** Destination address of the pending or last executed command token

15.8.763 reg_inp_sys_dma_DMA_command_ctrl_id_type (inp_sys_dma_DMA_command_ctrl_id)—Offset 8700Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_command_ctrl_id: [ISPMMADR] + 8700Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_command_ctrl_id

DMA_command_ctrl_id

Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_command_ctrl_id:** Unused
1:0	0h RO	**DMA_command_ctrl_id:** Controller id of the pending or last executed command token

15.8.764 reg_inp_sys_dma_DMA_FSM_Ctrl_status_type (inp_sys_dma_DMA_FSM_Ctrl_status)—Offset 87010h

DMA FSM Control state and flags

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_status: [ISPMMADR] + 87010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
unused_DMA_FSM_Ctrl_status																								FSM				Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:8	0h RW	**unused_DMA_FSM_Ctrl_status:** Unused
7:4	0h RO	**FSM:** FSM control state: 0)Idle -- 1)req_rcv -- 2)rcv -- 3)rcv_req -- 4)init
3	0h RO	**Error:** Error flag
2	0h RO	**Stall:** Stall flag
1	0h RO	**Run:** Run flag
0	1h RO	**Idle:** Idle flag

15.8.765 reg_inp_sys_dma_DMA_FSM_Pack_status_type (inp_sys_dma_DMA_FSM_Pack_status)—Offset 87014h

DMA FSM Pack state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Pack_status: [ISPMMADR] + 87014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Pack_status																												Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:4	0h RW	**unused_DMA_FSM_Pack_status:** Unused
3	0h RO	**Error:** Error flag
2	0h RO	**Stall:** Stall flag
1	0h RO	**Run:** Run flag
0	0h RO	**Idle:** Idle flag

15.8.766 reg_inp_sys_dma_DMA_FSM_request_status_type (inp_sys_dma_DMA_FSM_request_status)—Offset 87018h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_request_status: [ISPMMADR] + 87018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_request_status

DMA_FSM_request_status

Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_request_status:** Unused
1:0	0h RO	**DMA_FSM_request_status:** DMA FSM Request state: 0)Idle -- 1)req -- 2)Next line

15.8.767 reg_inp_sys_dma_DMA_FSM_write_status_type (inp_sys_dma_DMA_FSM_write_status)—Offset 8701Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_write_status: [ISPMMADR] + 8701Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_write_status

DMA_FSM_write_status

Bit Range	Default & Access	Description
31:2	0h RW	**unused_DMA_FSM_write_status:** Unused

Bit Range	Default & Access	Description
1:0	0h RO	**DMA_FSM_write_status:** DMA FSM Write state: 0)Idle -- 1)req -- 2)Next line

15.8.768 reg_inp_sys_dma_DMA_FSM_Ctrl_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_dev_idx)—Offset 87110h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_dev_idx: [ISPMMADR] + 87110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Ctrl_dev_idx																															DMA_FSM_Ctrl_dev_idx

Bit Range	Default & Access	Description
31:1	0h RW	**unused_DMA_FSM_Ctrl_dev_idx:** Unused
0	0h RO	**DMA_FSM_Ctrl_dev_idx:** DMA FSM Control request device idx

15.8.769 reg_inp_sys_dma_DMA_FSM_Pack_cnt_Yb_type (inp_sys_dma_DMA_FSM_Pack_cnt_Yb)—Offset 87114h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Pack_cnt_Yb: [ISPMMADR] + 87114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Pack_cnt_Yb																DMA_FSM_Pack_cnt_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_cnt_Yb:** Unused
15:0	0h RO	**DMA_FSM_Pack_cnt_Yb:** DMA FSM pack counter height (Yb)

15.8.770 reg_inp_sys_dma_DMA_FSM_Request_cnt_Yb_type (inp_sys_dma_DMA_FSM_Request_cnt_Yb)—Offset 87118h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Request_cnt_Yb: [ISPMMADR] + 87118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Request_cnt_Yb																DMA_FSM_Request_cnt_Yb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Request_cnt_Yb:** Unused

Bit Range	Default & Access	Description
15:0	0h RO	**DMA_FSM_Request_cnt_Yb:** DMA FSM request counter height (Yb)

15.8.771 reg_inp_sys_dma_DMA_FSM_Write_cnt_Y_type (inp_sys_dma_DMA_FSM_Write_cnt_Y)—Offset 8711Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Write_cnt_Y: [ISPMMADR] + 8711Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_FSM_Write_cnt_Y	DMA_FSM_Write_cnt_Y

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Write_cnt_Y:** Unused
15:0	0h RO	**DMA_FSM_Write_cnt_Y:** DMA FSM Write counter height (Yb)

15.8.772 reg_inp_sys_dma_DMA_FSM_Ctrl_req_addr_type (inp_sys_dma_DMA_FSM_Ctrl_req_addr)—Offset 87210h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_req_addr: [ISPMMADR] + 87210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_FSM_Ctrl_req_addr

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_req_addr:** DMA FSM Control request address

15.8.773 reg_inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb_type (inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 87214h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb: [ISPMMADR] + 87214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Pack_req_cnt_Xb

DMA_FSM_Pack_req_cnt_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_req_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Pack_req_cnt_Xb:** DMA FSM pack request counter width (Xb)

15.8.774 reg_inp_sys_dma_DMA_FSM_Request_cnt_Xb_type (inp_sys_dma_DMA_FSM_Request_cnt_Xb)—Offset 87218h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Request_cnt_Xb: [ISPMMADR] + 87218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: unused_DMA_FSM_Request_cnt_Xb
Bits 15:0: DMA_FSM_Request_cnt_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Request_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Request_cnt_Xb:** DMA FSM Request counter width (Xb)

15.8.775 reg_inp_sys_dma_DMA_FSM_Write_cnt_Xb_type (inp_sys_dma_DMA_FSM_Write_cnt_Xb)—Offset 8721Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Write_cnt_Xb: [ISPMMADR] + 8721Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: unused_DMA_FSM_Write_cnt_Xb; Bits 15:0: DMA_FSM_Write_cnt_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Write_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Write_cnt_Xb:** DMA FSM Write counter width (Xb)

15.8.776 reg_inp_sys_dma_DMA_FSM_Ctrl_req_stride_type (inp_sys_dma_DMA_FSM_Ctrl_req_stride)—Offset 87310h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_req_stride: [ISPMMADR] + 87310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:0: DMA_FSM_Ctrl_req_stride

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_req_stride:** DMA FSM Control request stride

15.8.777 reg_inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb_type (inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 87314h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb: [ISPMMADR] + 87314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_DMA_FSM_Pack_wr_cnt_Xb																DMA_FSM_Pack_wr_cnt_Xb															

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Pack_wr_cnt_Xb:** Unused
15:0	0h RO	**DMA_FSM_Pack_wr_cnt_Xb:** DMA FSM pack write counter width (Xb)

15.8.778 reg_inp_sys_dma_DMA_FSM_Req_remining_Xb_type (inp_sys_dma_DMA_FSM_Req_remining_Xb)—Offset 87318h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Req_remining_Xb: [ISPMMADR] + 87318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_FSM_Req_remining_Xb (31:16)	DMA_FSM_Req_remining_Xb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Req_remining_Xb:** Unused
15:0	0h RO	**DMA_FSM_Req_remining_Xb:** DMA FSM Request counter remaining word width

15.8.779 reg_inp_sys_dma_DMA_FSM_Wr_remining_Xb_type (inp_sys_dma_DMA_FSM_Wr_remining_Xb)—Offset 8731Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Wr_remining_Xb: [ISPMMADR] + 8731Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_DMA_FSM_Wr_remining_Xb (31:16)	DMA_FSM_Wr_remining_Xb (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Wr_remining_Xb:** Unused
15:0	0h RO	**DMA_FSM_Wr_remining_Xb:** DMA FSM Write counter remaining word width

15.8.780 reg_inp_sys_dma_DMA_FSM_Ctrl_req_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_req_Xb)—Offset 87410h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_req_Xb: [ISPMMADR] + 87410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
unused_DMA_FSM_Ctrl_req_Xb	DMA_FSM_Ctrl_req_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_req_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_req_Xb:** DMA FSM Control request width (Xb)

15.8.781 reg_inp_sys_dma_DMA_FSM_Req_burst_cnt_type (inp_sys_dma_DMA_FSM_Req_burst_cnt)—Offset 87418h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Req_burst_cnt: [ISPMMADR] + 87418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

unused_DMA_FSM_Req_burst_cnt (31:16) | DMA_FSM_Req_burst_cnt (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Req_burst_cnt:** Unused
15:0	FFFFh RO	**DMA_FSM_Req_burst_cnt:** DMA FSM Request word burst counter

15.8.782 reg_inp_sys_dma_DMA_FSM_Wr_burst_cnt_type (inp_sys_dma_DMA_FSM_Wr_burst_cnt)—Offset 8741Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Wr_burst_cnt: [ISPMMADR] + 8741Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

unused_DMA_FSM_Wr_burst_cnt (31:16) | DMA_FSM_Wr_burst_cnt (15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Wr_burst_cnt:** Unused

Bit Range	Default & Access	Description
15:0	FFFFh RO	**DMA_FSM_Wr_burst_cnt:** DMA FSM Write word burst counter

15.8.783 reg_inp_sys_dma_DMA_FSM_Ctrl_req_Yb_type (inp_sys_dma_DMA_FSM_Ctrl_req_Yb)—Offset 87510h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_req_Yb: [ISPMMADR] + 87510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: unused_DMA_FSM_Ctrl_req_Yb
Bits 15:0: DMA_FSM_Ctrl_req_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_req_Yb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_req_Yb:** DMA FSM Control request height (Yb)

15.8.784 reg_inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 87610h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx:
[ISPMMADR] + 87610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_FSM_Ctrl_Pack_req_dev_idx (bits 31:1); DMA_FSM_Ctrl_Pack_req_dev_idx (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_DMA_FSM_Ctrl_Pack_req_dev_idx:** Unused
0	0h RO	**DMA_FSM_Ctrl_Pack_req_dev_idx:** DMA FSM Control pack request device idx

15.8.785 reg_inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx_type (inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 87710h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx: [ISPMMADR] + 87710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_FSM_Ctrl_Pack_wr_dev_idx (bits 31:1); DMA_FSM_Ctrl_Pack_wr_dev_idx (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_DMA_FSM_Ctrl_Pack_wr_dev_idx:** Unused
0	0h RO	**DMA_FSM_Ctrl_Pack_wr_dev_idx:** DMA FSM Control pack write device idx

15.8.786 reg_inp_sys_dma_DMA_FSM_Ctrl_Wr_addr_type (inp_sys_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 87810h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_Wr_addr: [ISPMMADR] +
87810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_FSM_Ctrl_Wr_addr

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_Wr_addr:** DMA FSM Control write address

15.8.787 reg_inp_sys_dma_DMA_FSM_Ctrl_Wr_stride_type (inp_sys_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 87910h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_Wr_stride: [ISPMMADR] +
87910h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_FSM_Ctrl_Wr_stride

Bit Range	Default & Access	Description
31:0	0h RO	**DMA_FSM_Ctrl_Wr_stride:** DMA FSM Control write stride

15.8.788 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 87A10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb: [ISPMMADR] + 87A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Ctrl_pack_req_Xb

DMA_FSM_Ctrl_pack_req_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_req_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_req_Xb:** DMA FSM Control FSM Pack request width (Xb)

15.8.789 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_Yb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 87B10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_Yb: [ISPMMADR] + 87B10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: unused_DMA_FSM_Ctrl_pack_Yb
Bits 15:0: DMA_FSM_Ctrl_pack_Yb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_Yb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_Yb:** DMA FSM Control FSM Pack height (Yb)

15.8.790 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb_type (inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 87C10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb: [ISPMMADR] + 87C10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Ctrl_pack_wr_Xb | DMA_FSM_Ctrl_pack_wr_Xb

Bit Range	Default & Access	Description
31:16	0h RW	**unused_DMA_FSM_Ctrl_pack_wr_Xb:** Unused
15:0	0h RO	**DMA_FSM_Ctrl_pack_wr_Xb:** DMA FSM Control FSM Pack write width (Xb)

15.8.791 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem_type (inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 87D10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem: [ISPMMADR] + 87D10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Ctrl_pack_req_elem | DMA_FSM_Ctrl_pack_req_elem

Bit Range	Default & Access	Description
31:7	0h RW	**unused_DMA_FSM_Ctrl_pack_req_elem:** Unused
6:0	0h RO	**DMA_FSM_Ctrl_pack_req_elem:** DMA FSM Control pack request element per word

15.8.792 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem_type (inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 87E10h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem: [ISPMMADR] + 87E10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_DMA_FSM_Ctrl_pack_wr_elem

DMA_FSM_Ctrl_pack_wr_elem

Bit Range	Default & Access	Description
31:7	0h RW	**unused_DMA_FSM_Ctrl_pack_wr_elem:** Unused
6:0	0h RO	**DMA_FSM_Ctrl_pack_wr_elem:** DMA FSM Control pack write element per word

15.8.793 reg_inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id_type (inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 87F10h

DMA FSM Control pack element sign zero extension and controller ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id: [ISPMMADR] + 87F10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id (31:6), ctrlID (5:4), unused (3:1), ext (0)

Bit Range	Default & Access	Description
31:6	0h RW	**unused_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id:** Unused
5:4	0h RO	**ctrlID:** Controller ID
3:1	0h RO	**unused:** unused
0	0h RO	**ext:** element sign(1)/zero(0) extension

15.8.794 reg_inp_sys_dma_Dev_Interf_0_req_side_type (inp_sys_dma_Dev_Interf_0_req_side)—Offset 88000h

DMA Device interface 0 internal side status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_0_req_side: [ISPMMADR] + 88000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_Dev_Interf_0_req_side																												Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_0_req_side:** Unused
3	0h RO	**Error:** Ack flag
2	0h RO	**Stall:** Run flag
1	0h RO	**Run:** We_n flag
0	0h RO	**Idle:** CS flag

15.8.795 reg_inp_sys_dma_Dev_Interf_1_req_side_type (inp_sys_dma_Dev_Interf_1_req_side)—Offset 88004h

DMA Device interface 1 internal side status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_req_side: [ISPMMADR] + 88004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
unused_Dev_Interf_1_req_side																												Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_1_req_side:** Unused
3	0h RO	**Error:** Ack flag
2	1h RO	**Stall:** Run flag
1	1h RO	**Run:** We_n flag
0	0h RO	**Idle:** CS flag

15.8.796 reg_inp_sys_dma_Dev_Interf_0_snd_side_type (inp_sys_dma_Dev_Interf_0_snd_side)—Offset 88100h

DMA Device interface 0 output side status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_0_snd_side: [ISPMMADR] + 88100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h

Bits	31:4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0	0
Field	unused_Dev_Interf_0_snd_side	Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_0_snd_side:** Unused
3	0h RO	**Error:** Ack flag
2	1h RO	**Stall:** Run flag
1	0h RO	**Run:** We_n flag
0	0h RO	**Idle:** CS flag

15.8.797 reg_inp_sys_dma_Dev_Interf_1_snd_side_type (inp_sys_dma_Dev_Interf_1_snd_side)—Offset 88104h

DMA Device interface 1 output side status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_snd_side: [ISPMMADR] + 88104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h

31 28 24 20 16 12 8 4 0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	1	1	0
unused_Dev_Interf_1_snd_side							Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:4	0h RW	**unused_Dev_Interf_1_snd_side:** Unused
3	0h RO	**Error:** Ack flag
2	1h RO	**Stall:** Run flag
1	1h RO	**Run:** We_n flag
0	0h RO	**Idle:** CS flag

15.8.798 reg_inp_sys_dma_Dev_Interf_0_Fifo_status_type (inp_sys_dma_Dev_Interf_0_Fifo_status)—Offset 88200h

Device Interface 0 Fifo Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_0_Fifo_status: [ISPMMADR] + 88200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	31:17	16:3	2	1	0
Field	unused_Dev_Interf_0_Fifo_status	Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_0_Fifo_status:** Unused
16:3	0h RO	**Error:** Fifo word counter
2	1h RO	**Stall:** Fifo is empty
1	0h RO	**Run:** Fifo is full
0	0h RO	**Idle:** Fifo will be full

15.8.799 reg_inp_sys_dma_Dev_Interf_1_Fifo_status_type (inp_sys_dma_Dev_Interf_1_Fifo_status)—Offset 88204h

Device Interface 1 Fifo Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_Fifo_status: [ISPMMADR] + 88204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0

unused_Dev_Interf_1_Fifo_status	Error	Stall	Run	Idle

Bit Range	Default & Access	Description
31:17	0h RW	**unused_Dev_Interf_1_Fifo_status:** Unused
16:3	0h RO	**Error:** Fifo word counter
2	1h RO	**Stall:** Fifo is empty
1	0h RO	**Run:** Fifo is full
0	0h RO	**Idle:** Fifo will be full

15.8.800 reg_inp_sys_dma_Dev_Interf_0_Req_complete_bust_type (inp_sys_dma_Dev_Interf_0_Req_complete_bust)—Offset 88300h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_dma_Dev_Interf_0_Req_complete_bust:
[ISPMMADR] + 88300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_Dev_Interf_0_Req_complete_bust (bits 31:1)
Dev_Interf_0_Req_complete_bust (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_0_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_0_Req_complete_bust:** DMA Device interface 0 Request only complete burst

15.8.801 reg_inp_sys_dma_Dev_Interf_1_Req_complete_bust_type (inp_sys_dma_Dev_Interf_1_Req_complete_bust)—Offset 88304h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_Req_complete_bust: [ISPMMADR] + 88304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_Dev_Interf_1_Req_complete_bust (bits 31:1)
Dev_Interf_1_Req_complete_bust (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_Dev_Interf_1_Req_complete_bust:** Unused
0	0h RW	**Dev_Interf_1_Req_complete_bust:** DMA Device interface 1 Request only complete burst

15.8.802 reg_inp_sys_dma_Dev_Interf_1_Max_burst_Size_type (inp_sys_dma_Dev_Interf_1_Max_burst_Size)—Offset 88400h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_dma_Dev_Interf_1_Max_burst_Size: [ISPMMADR] + 88400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000007Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

unused_Dev_Interf_1_Max_burst_Size (bits 31:8)
Dev_Interf_1_Max_burst_Size (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RW	**unused_Dev_Interf_1_Max_burst_Size:** Unused
7:0	7Fh RW	**Dev_Interf_1_Max_burst_Size:** DMA Device interface 1 max burst size

15.8.803 reg_inp_sys_inp_ctrl_inpsys_captA_start_addr_type (inp_sys_inp_ctrl_inpsys_captA_start_addr)—Offset 89000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captA_start_addr: [ISPMMADR] + 89000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:9	Bits 8:0
unused_inpsys_captA_start_addr	inpsys_captA_start_addr

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captA_start_addr:** Unused
8:0	0h RW	**inpsys_captA_start_addr:** Input System Controller Capt A mem region start address

15.8.804 reg_inp_sys_inp_ctrl_inpsys_captB_start_addr_type (inp_sys_inp_ctrl_inpsys_captB_start_addr)—Offset 89004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captB_start_addr: [ISPMMADR] + 89004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:9	Bits 8:0
unused_inpsys_captB_start_addr	inpsys_captB_start_addr

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captB_start_addr:** Unused

Bit Range	Default & Access	Description
8:0	0h RW	**inpsys_captB_start_addr:** Input System Controller Capt B mem region start address

15.8.805 reg_inp_sys_inp_ctrl_inpsys_captC_start_addr_type (inp_sys_inp_ctrl_inpsys_captC_start_addr)—Offset 89008h

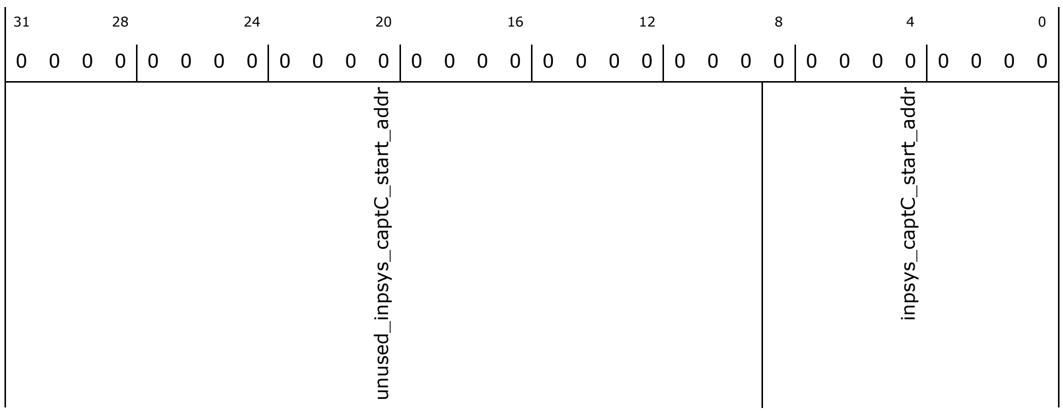
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captC_start_addr: [ISPMMADR] + 89008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captC_start_addr:** Unused
8:0	0h RW	**inpsys_captC_start_addr:** Input System Controller Capt C mem region start address

15.8.806 reg_inp_sys_inp_ctrl_inpsys_captA_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captA_mem_region_size)—Offset 8900Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captA_mem_region_size: [ISPMMADR] + 8900Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 0 0 0 | 0 0 0 0

Bits 31:9	Bits 8:0
unused_inpsys_captA_mem_region_size	inpsys_captA_mem_region_size

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captA_mem_region_size:** Unused
8:0	080h RW	**inpsys_captA_mem_region_size:** Input System Controller Capt A mem region size

15.8.807 reg_inp_sys_inp_ctrl_inpsys_captB_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captB_mem_region_size)—Offset 89010h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captB_mem_region_size: [ISPMMADR] + 89010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 0 0 0 | 0 0 0 0

Bits 31:9	Bits 8:0
unused_inpsys_captB_mem_region_size	inpsys_captB_mem_region_size

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captB_mem_region_size:** Unused
8:0	080h RW	**inpsys_captB_mem_region_size:** Input System Controller Capt B mem region size

15.8.808 reg_inp_sys_inp_ctrl_inpsys_captC_mem_region_size_type (inp_sys_inp_ctrl_inpsys_captC_mem_region_size)—Offset 89014h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captC_mem_region_size: [ISPMMADR] + 89014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fields: unused_inpsys_captC_mem_region_size (bits 31:9), inpsys_captC_mem_region_size (bits 8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captC_mem_region_size:** Unused
8:0	080h RW	**inpsys_captC_mem_region_size:** Input System Controller Capt C mem region size

15.8.809 reg_inp_sys_inp_ctrl_inpsys_captA_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captA_num_mem_regions)—Offset 89018h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captA_num_mem_regions: [ISPMMADR] + 89018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Fields: unused_inpsys_captA_num_mem_regions (31:9); inpsys_captA_num_mem_regions (8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captA_num_mem_regions:** Unused
8:0	003h RW	**inpsys_captA_num_mem_regions:** Input System Controller Capt A number of mem regions

15.8.810 reg_inp_sys_inp_ctrl_inpsys_captB_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captB_num_mem_regions)—Offset 8901Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captB_num_mem_regions: [ISPMMADR] + 8901Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Fields: unused_inpsys_captB_num_mem_regions (bits 31:9), inpsys_captB_num_mem_regions (bits 8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captB_num_mem_regions:** Unused
8:0	003h RW	**inpsys_captB_num_mem_regions:** Input System Controller Capt B number of mem regions

15.8.811 reg_inp_sys_inp_ctrl_inpsys_captC_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_captC_num_mem_regions)—Offset 89020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captC_num_mem_regions: [ISPMMADR] + 89020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)

ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Fields: unused_inpsys_captC_num_mem_regions (bits 31:9), inpsys_captC_num_mem_regions (bits 8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_captC_num_mem_regions:** Unused
8:0	003h RW	**inpsys_captC_num_mem_regions:** Input System Controller Capt C number of mem regions

15.8.812 reg_inp_sys_inp_ctrl_inpsys_acq_start_addr_type (inp_sys_inp_ctrl_inpsys_acq_start_addr)—Offset 89024h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_acq_start_addr: [ISPMMADR] + 89024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:9	Bits 8:0
unused_inpsys_acq_start_addr	inpsys_acq_start_addr

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_acq_start_addr:** Unused
8:0	0h RW	**inpsys_acq_start_addr:** Input System Controller Acquisition mem region start address

15.8.813 reg_inp_sys_inp_ctrl_inpsys_acq_mem_region_size_type (inp_sys_inp_ctrl_inpsys_acq_mem_region_size)—Offset 89028h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_acq_mem_region_size: [ISPMMADR] + 89028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fields: unused_inpsys_acq_mem_region_size (bits 31:9), inpsys_acq_mem_region_size (bits 8:0)

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_acq_mem_region_size:** Unused
8:0	080h RW	**inpsys_acq_mem_region_size:** Input System Controller Acquisition mem region size

15.8.814 reg_inp_sys_inp_ctrl_inpsys_acq_num_mem_regions_type (inp_sys_inp_ctrl_inpsys_acq_num_mem_regions)—Offset 8902Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_acq_num_mem_regions: [ISPMMADR] + 8902Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Fields: unused_inpsys_acq_num_mem_regions, inpsys_acq_num_mem_regions

Bit Range	Default & Access	Description
31:9	0h RW	**unused_inpsys_acq_num_mem_regions:** Unused
8:0	003h RW	**inpsys_acq_num_mem_regions:** Input System Controller Acquisition number of mem regions

15.8.815 reg_inp_sys_inp_ctrl_inpsys_ctrl_init_type (inp_sys_inp_ctrl_inpsys_ctrl_init)—Offset 89030h

Input System Controller initialization register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_inp_ctrl_inpsys_ctrl_init: [ISPMMADR] + 89030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_inpsys_ctrl_init (31:3), reserved (2:1), reset_registers (0)

Bit Range	Default & Access	Description
31:3	0h RW	**unused_inpsys_ctrl_init:** Unused
2:1	0h RW	**reserved:** reserved bits, no action for now
0	0h RW	**reset_registers:** Reset all registers in Input System Controller

15.8.816 reg_inp_sys_inp_ctrl_inpsys_last_cmd_type (inp_sys_inp_ctrl_inpsys_last_cmd)—Offset 89034h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_inp_ctrl_inpsys_last_cmd: [ISPMMADR] + 89034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

inpsys_last_cmd

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**inpsys_last_cmd:** Input System Controller last command register

15.8.817 reg_inp_sys_inp_ctrl_inpsys_next_cmd_type (inp_sys_inp_ctrl_inpsys_next_cmd)—Offset 89038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_next_cmd: [ISPMMADR] + 89038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

inpsys_next_cmd

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**inpsys_next_cmd:** Input System Controller next command register

15.8.818 reg_inp_sys_inp_ctrl_inpsys_last_ack_type (inp_sys_inp_ctrl_inpsys_last_ack)—Offset 8903Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_last_ack: [ISPMMADR] + 8903Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

inpsys_last_ack

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**inpsys_last_ack:** Input System Controller last acknowledge register

15.8.819 reg_inp_sys_inp_ctrl_inpsys_next_ack_type (inp_sys_inp_ctrl_inpsys_next_ack)—Offset 89040h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_next_ack: [ISPMMADR] + 89040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

inpsys_next_ack

Bit Range	Default & Access	Description
31:0	0000000Fh RO	**inpsys_next_ack:** Input System Controller next acknowledge register

15.8.820 reg_inp_sys_inp_ctrl_inpsys_top_fsm_state_type (inp_sys_inp_ctrl_inpsys_top_fsm_state)—Offset 89044h

Input System Controller top-ctrl FSM current and next state info Register (both Cmd/ Ack FSM)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_top_fsm_state: [ISPMMADR] + 89044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
ack_fsm_next_state	ack_fsm_current_state	cmd_fsm_next_state	cmd_fsm_current_state

Bit Range	Default & Access	Description
31:24	0h RW	**ack_fsm_next_state:** Next state of top-ctrl Acknowledge FSM
23:16	0h RW	**ack_fsm_current_state:** Current state of top-ctrl Acknowledge FSM
15:8	0h RW	**cmd_fsm_next_state:** Next state of top-ctrl Command FSM
7:0	0h RW	**cmd_fsm_current_state:** Current state of top-ctrl Command FSM

15.8.821 reg_inp_sys_inp_ctrl_inpsys_captA_fsm_state_type (inp_sys_inp_ctrl_inpsys_captA_fsm_state)—Offset 89048h

Input System Controller captureA sub-ctrl current and next state info Register (FSM and DMA cmd state)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captA_fsm_state: [ISPMMADR] + 89048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:28	27:24	23:12	11:0
0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
dma_cmd_next_state	dma_cmd_current_state	fsm_next_state	fsm_current_state

Bit Range	Default & Access	Description
31:28	0h RW	**dma_cmd_next_state:** Next state of DMA cmd

Bit Range	Default & Access	Description
27:24	0h RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0h RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0h RW	**fsm_current_state:** Current state of sub-ctrl FSM

15.8.822 reg_inp_sys_inp_ctrl_inpsys_captB_fsm_state_type (inp_sys_inp_ctrl_inpsys_captB_fsm_state)—Offset 8904Ch

Input System Controller captureB sub-ctrl current and next state info Register (FSM and DMA cmd state)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captB_fsm_state: [ISPMMADR] + 8904Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31–28	27–24	23–12	11–0
0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
dma_cmd_next_state	dma_cmd_current_state	fsm_next_state	fsm_current_state

Bit Range	Default & Access	Description
31:28	0h RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0h RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0h RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0h RW	**fsm_current_state:** Current state of sub-ctrl FSM

15.8.823 reg_inp_sys_inp_ctrl_inpsys_captC_fsm_state_type (inp_sys_inp_ctrl_inpsys_captC_fsm_state)—Offset 89050h

Input System Controller captureC sub-ctrl current and next state info Register (FSM and DMA cmd state)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_captC_fsm_state: [ISPMMADR] + 89050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
dma_cmd_next_state				dma_cmd_current_state				fsm_next_state												fsm_current_state											

Bit Range	Default & Access	Description
31:28	0h RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0h RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0h RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0h RW	**fsm_current_state:** Current state of sub-ctrl FSM

15.8.824 reg_inp_sys_inp_ctrl_inpsys_acq_fsm_state_type (inp_sys_inp_ctrl_inpsys_acq_fsm_state)—Offset 89054h

Input System Controller acquisition sub-ctrl current and next state info Register (FSM and DMA cmd state)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_inp_ctrl_inpsys_acq_fsm_state: [ISPMMADR] + 89054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:28	27:24	23:12	11:0
0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0
dma_cmd_next_state	dma_cmd_current_state	fsm_next_state	fsm_current_state

Bit Range	Default & Access	Description
31:28	0h RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0h RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0h RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0h RW	**fsm_current_state:** Current state of sub-ctrl FSM

15.8.825 reg_inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region_type (inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region)—Offset 89058h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region:
[ISPMMADR] + 89058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_inpsys_capt_reserve_one_mem_region

inpsys_capt_reserve_one_mem_region

Bit Range	Default & Access	Description
31:1	0h RW	**unused_inpsys_capt_reserve_one_mem_region:** Unused
0	0h RW	**inpsys_capt_reserve_one_mem_region:** Reserve 1 or 0 mem region of capture units in input buffer to avoid overflow of captured data. 0: zero mem region reserved, 1: one mem region reserved

15.8.826 reg_inp_sys_gpreg_str_multicastA_sel_type (inp_sys_gpreg_str_multicastA_sel)—Offset 8A000h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_gpreg_str_multicastA_sel: [ISPMMADR] + 8A000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_str_multicastA_sel

str_multicastA_sel

Bit Range	Default & Access	Description
31:2	0h RW	**unused_str_multicastA_sel:** Unused
1:0	0h RW	**str_multicastA_sel:** StreamMulticastA_select

15.8.827 reg_inp_sys_gpreg_str_multicastB_sel_type (inp_sys_gpreg_str_multicastB_sel)—Offset 8A004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_multicastB_sel: [ISPMMADR] + 8A004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_str_multicastB_sel (bits 31:2); str_multicastB_sel (bits 1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_str_multicastB_sel:** Unused
1:0	0h RW	**str_multicastB_sel:** StreamMulticastB_select

15.8.828 reg_inp_sys_gpreg_str_multicastC_sel_type (inp_sys_gpreg_str_multicastC_sel)—Offset 8A008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_multicastC_sel: [ISPMMADR] + 8A008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_str_multicastC_sel (31:2) | str_multicastC_sel (1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_str_multicastC_sel:** Unused
1:0	0h RW	**str_multicastC_sel:** StreamMulticastC_select

15.8.829 reg_inp_sys_gpreg_str_mux_sel_type (inp_sys_gpreg_str_mux_sel)—Offset 8A00Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_mux_sel: [ISPMMADR] + 8A00Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_str_mux_sel (31:2) | str_mux_sel (1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_str_mux_sel:** Unused
1:0	0h RW	**str_mux_sel:** StreamMux_select

15.8.830 reg_inp_sys_gpreg_str_mon_status_type (inp_sys_gpreg_str_mon_status)—Offset 8A010h

Streaming Monitor Status, [accept,valid] of streaming port

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_gpreg_str_mon_status: [ISPMMADR] + 8A010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:24	unused_str_mon_status
23:22	str_pixelB_deint_stat
21:20	str_pixelA_deint_stat
19:18	str_pixelB_stat
17:16	str_pixelA_stat
15:14	str_ctrl_out_stat
13:12	str_ctrl_in_stat
11:10	str_gensh_fifo_stat
9:8	str_gensh_pkt_stat
7:6	str_mux_stat
5:4	str_captC_stat
3:2	str_captB_stat
1:0	str_captA_stat

Bit Range	Default & Access	Description
31:24	0h RW	**unused_str_mon_status:** Unused
23:22	0h RW	**str_pixelB_deint_stat:** Pixel B streaming output from Stream Deinterleaver
21:20	0h RW	**str_pixelA_deint_stat:** Pixel A streaming output from Stream Deinterleaver
19:18	0h RW	**str_pixelB_stat:** Pixel B streaming output from CSI receiver
17:16	0h RW	**str_pixelA_stat:** Pixel A streaming output from CSI receiver
15:14	0h RW	**str_ctrl_out_stat:** Control streaming output
13:12	0h RW	**str_ctrl_in_stat:** Control streaming input
11:10	0h RW	**str_gensh_fifo_stat:** Generic short FIFO streaming output
9:8	0h RW	**str_gensh_pkt_stat:** Generic short packet streaming output from CSI receiver
7:6	0h RW	**str_mux_stat:** Stream Mux streaming output
5:4	0h RW	**str_captC_stat:** Capture port C streaming output from CSI receiver
3:2	0h RW	**str_captB_stat:** Capture port B streaming output from CSI receiver
1:0	0h RW	**str_captA_stat:** Capture port A streaming output from CSI receiver

15.8.831 reg_inp_sys_gpreg_str_mon_irq_cond_type (inp_sys_gpreg_str_mon_irq_cond)—Offset 8A014h

Streaming Monitor IRQ condition, [accept,valid] for streaming port

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_mon_irq_cond: [ISPMMADR] + 8A014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:24	23:22	21:20	19:18	17:16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
0 0 0 0 0 0 0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
unused_str_mon_irq_cond	str_pixelB_deint_irq_cond	str_pixelA_deint_irq_cond	str_pixelB_irq_cond	str_pixelA_irq_cond	str_ctrl_out_irq_cond	str_ctrl_in_irq_cond	str_gensh_fifo_irq_cond	str_gensh_pkt_irq_cond	str_mux_irq_cond	str_captC_irq_cond	str_captB_irq_cond	str_captA_irq_cond

Bit Range	Default & Access	Description
31:24	0h RW	**unused_str_mon_irq_cond:** Unused
23:22	0h RW	**str_pixelB_deint_irq_cond:** Pixel B streaming output from Stream Deinterleaver
21:20	0h RW	**str_pixelA_deint_irq_cond:** Pixel A streaming output from Stream Deinterleaver
19:18	0h RW	**str_pixelB_irq_cond:** Pixel B streaming output from CSI receiver
17:16	0h RW	**str_pixelA_irq_cond:** Pixel A streaming output from CSI receiver
15:14	0h RW	**str_ctrl_out_irq_cond:** Control streaming output
13:12	0h RW	**str_ctrl_in_irq_cond:** Control streaming input
11:10	0h RW	**str_gensh_fifo_irq_cond:** Generic short FIFO streaming output
9:8	0h RW	**str_gensh_pkt_irq_cond:** Generic short packet streaming output from CSI receiver
7:6	0h RW	**str_mux_irq_cond:** Stream Mux streaming output
5:4	0h RW	**str_captC_irq_cond:** Capture port C streaming output from CSI receiver
3:2	0h RW	**str_captB_irq_cond:** Capture port B streaming output from CSI receiver

Bit Range	Default & Access	Description
1:0	0h RW	**str_captA_irq_cond:** Capture port A streaming output from CSI receiver

15.8.832 reg_inp_sys_gpreg_str_mon_irq_en_type (inp_sys_gpreg_str_mon_irq_en)—Offset 8A018h

Streaming Monitor IRQ enable

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_gpreg_str_mon_irq_en: [ISPMMADR] + 8A018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	unused_str_mon_irq_en	str_pixelB_deint_irq_en	str_pixelA_deint_irq_en	str_pixelB_irq_en	str_pixelA_irq_en	str_ctrl_out_irq_en	str_ctrl_in_irq_en	str_gensh_fifo_irq_en	str_gensh_pkt_irq_en	str_mux_irq_en	str_captC_irq_en	str_captB_irq_en	str_captA_irq_en

Bit Range	Default & Access	Description
31:12	0h RW	**unused_str_mon_irq_en:** Unused
11	0h RW	**str_pixelB_deint_irq_en:** Pixel B streaming output from Stream Deinterleaver
10	0h RW	**str_pixelA_deint_irq_en:** Pixel A streaming output from Stream Deinterleaver
9	0h RW	**str_pixelB_irq_en:** Pixel B streaming output from CSI receiver
8	0h RW	**str_pixelA_irq_en:** Pixel A streaming output from CSI receiver
7	0h RW	**str_ctrl_out_irq_en:** Control streaming output
6	0h RW	**str_ctrl_in_irq_en:** Control streaming input
5	0h RW	**str_gensh_fifo_irq_en:** Generic short FIFO streaming output
4	0h RW	**str_gensh_pkt_irq_en:** Generic short packet streaming output from CSI receiver
3	0h RW	**str_mux_irq_en:** Stream Mux streaming output

Bit Range	Default & Access	Description
2	0h RW	**str_captC_irq_en:** Capture port C streaming output from CSI receiver
1	0h RW	**str_captB_irq_en:** Capture port B streaming output from CSI receiver
0	0h RW	**str_captA_irq_en:** Capture port A streaming output from CSI receiver

15.8.833 reg_inp_sys_gpreg_isys_srst_type (inp_sys_gpreg_isys_srst)—Offset 8A01Ch

Soft resets the modules of the input system. Writing a 1 to a field brings a module in reset, writing a 0 brings that module out of reset

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_gpreg_isys_srst: [ISPMMADR] + 8A01Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bit	Default	Field
31:25	0 0 0 0 0 0 0	unused_isys_srst
24	0	srst_csi_rcv_be_out
23	0	srst_cfifo_acq
22	0	srst_cfifo_cap_c
21	0	srst_cfifo_cap_b
20	0	srst_cfifo_cap_a
19	0	srst_dma
18	0	srst_wide_bus
17	0	srst_gensh_fifo
16	0	srst_cio2ahb
15	0	srst_str_mux
14	0	srst_isys_top_ctrl
13	0	srst_isys_acq_ctrl
12	0	srst_isys_captC_sub_ctrl
11	0	srst_isys_captB_sub_ctrl
10	0	srst_isys_captA_sub_ctrl
9	0	srst_acq
8	0	srst_capt_c
7	0	srst_capt_b
6	0	srst_capt_a
5	0	srst_multi_cast_c
4	0	srst_multi_cast_b
3	0	srst_multi_cast_a
2	0	srst_capt_fifo_c
1	0	srst_capt_fifo_b
0	0	srst_capt_fifo_a

Bit Range	Default & Access	Description
31:25	0h RW	**unused_isys_srst:** Unused
24	0h RW	**srst_csi_rcv_be_out:** Soft resets the output of the csi receiver backend
23	0h RW	**srst_cfifo_acq:** Soft resets the control and acknowledge FIFOs for the acquistion unit
22	0h RW	**srst_cfifo_cap_c:** Soft resets the control and acknowledge FIFOs for capture unit C
21	0h RW	**srst_cfifo_cap_b:** Soft resets the control and acknowledge FIFOs for capture unit B
20	0h RW	**srst_cfifo_cap_a:** Soft resets the control and acknowledge FIFOs for capture unit A
19	0h RW	**srst_dma:** Soft resets the DMA

Bit Range	Default & Access	Description
18	0h RW	**srst_wide_bus:** Soft resets the wide bus including the CIO converter
17	0h RW	**srst_gensh_fifo:** Soft resets the generic short FIFO
16	0h RW	**srst_cio2ahb:** Soft resets the CIO2AHB adapter
15	0h RW	**srst_str_mux:** Soft resets the streaming mux
14	0h RW	**srst_isys_top_ctrl:** Soft resets the input system Top controller
13	0h RW	**srst_isys_acq_ctrl:** Soft resets the input system Acquisition sub-controller (controls data-path from selected captA/captB/captC/dma_acq to acq)
12	0h RW	**srst_isys_captC_sub_ctrl:** Soft resets the input system CaptureC sub-controller (controls data-path from captC to dma_captC)
11	0h RW	**srst_isys_captB_sub_ctrl:** Soft resets the input system CaptureB sub-controller (controls data-path from captB to dma_captB)
10	0h RW	**srst_isys_captA_sub_ctrl:** Soft resets the input system CaptureA sub-controller (controls data-path from captA to dma_captA)
9	0h RW	**srst_acq:** Soft resets the acquision unit
8	0h RW	**srst_capt_c:** Soft resets the capture unit C
7	0h RW	**srst_capt_b:** Soft resets the capture unit B
6	0h RW	**srst_capt_a:** Soft resets the capture unit A
5	0h RW	**srst_multi_cast_c:** Soft resets multi cast C
4	0h RW	**srst_multi_cast_b:** Soft resets multi cast B
3	0h RW	**srst_multi_cast_a:** Soft resets multi cast A
2	0h RW	**srst_capt_fifo_c:** Soft resets the FIFO before multi cast C
1	0h RW	**srst_capt_fifo_b:** Soft resets the FIFO before multi cast B
0	0h RW	**srst_capt_fifo_a:** Soft resets the FIFO before multi cast A

15.8.834 reg_inp_sys_gpreg_isys_slv_reg_srst_type (inp_sys_gpreg_isys_slv_reg_srst)—Offset 8A020h

Soft resets the slave accessible registers of certain input system modules. Writing a 1 to a field brings the registers for a module to their default value, writing a 0 allows them to be overwritten

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_gpreg_isys_slv_reg_srst: [ISPMMADR] + 8A020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:6	5	4	3	2	1	0
0000 0000 0000 0000 0000 0000 00	0	0	0	0	0	0
unused_isys_slv_reg_srst	srst_slv_reg_isys_ctrl	srst_slv_reg_dma	srst_slv_reg_acq	srst_slv_reg_capt_c	srst_slv_reg_capt_b	srst_slv_reg_capt_a

Bit Range	Default & Access	Description
31:6	0h RW	**unused_isys_slv_reg_srst:** Unused
5	0h RW	**srst_slv_reg_isys_ctrl:** Soft resets the slave accessible registers of the input system controller
4	0h RW	**srst_slv_reg_dma:** Soft resets the slave accessible registers of the DMA
3	0h RW	**srst_slv_reg_acq:** Soft resets the slave accessible registers of the acquisition unit
2	0h RW	**srst_slv_reg_capt_c:** Soft resets the slave accessible registers of capture unit C
1	0h RW	**srst_slv_reg_capt_b:** Soft resets the slave accessible registers of capture unit B
0	0h RW	**srst_slv_reg_capt_a:** Soft resets the slave accessible registers of capture unit A

15.8.835 reg_inp_sys_gpreg_str_deint_portA_cnt_type (inp_sys_gpreg_str_deint_portA_cnt)—Offset 8A024h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_gpreg_str_deint_portA_cnt: [ISPMMADR] + 8A024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_str_deint_portA_cnt

str_deint_portA_cnt

Bit Range	Default & Access	Description
31:16	0h RW	**unused_str_deint_portA_cnt:** Unused
15:0	0h RW	**str_deint_portA_cnt:** stream data count for portA of stream deinterleave block

15.8.836 reg_inp_sys_gpreg_str_deint_portB_cnt_type (inp_sys_gpreg_str_deint_portB_cnt)—Offset 8A028h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_gpreg_str_deint_portB_cnt: [ISPMMADR] + 8A028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_str_deint_portB_cnt

str_deint_portB_cnt

Bit Range	Default & Access	Description
31:16	0h RW	**unused_str_deint_portB_cnt:** Unused
15:0	0h RW	**str_deint_portB_cnt:** stream data count for portB of stream deinterleave block

15.8.837 reg_inp_sys_fifo_adapter_CSI_generic_short_packet_available_type

(inp_sys_fifo_adapter_CSI_generic_short_packet_available)—Offset 8B008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_fifo_adapter_CSI_generic_short_packet_available : [ISPMMADR] + 8B008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: unused_CSI_generic_short_packet_available (bits 31:1), CSI_generic_short_packet_available (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_CSI_generic_short_packet_available:** Unused
0	1h RO	**CSI_generic_short_packet_available:** Returns 1 if there is a generic short packet available. Returns 0 is there is no generic short packet available.

15.8.838 reg_inp_sys_irq_ctrl_irq_edge_type (inp_sys_irq_ctrl_irq_edge)—Offset 8C000h

IRQ active edge select per interrupt input. Rising edge: 1, Falling edge: 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_irq_ctrl_irq_edge: [ISPMMADR] + 8C000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:19	18	17	16	15:13	12	11:10	9:8	7:6	5:4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0 0 0	0	0 0	0 0	0 0	0 0	0	0	0	0
Field	unused_irq_edge	strmon_irq	dma_irq	cio2ahb_irq	inpsys_ctrl_irq	acq_irq	captC_irq	captB_irq	captA_irq	csi_irq	csi_pkt_eol	csi_pkt_sol	csi_pkt_eof	csi_pkt_sof

Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_edge:** Unused
18	0h RW	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RW	**acq_irq:** Acquisition unit interrupt request
11:10	0h RW	**captC_irq:** Capture unit C interrupt request
9:8	0h RW	**captB_irq:** Capture unit B interrupt request
7:6	0h RW	**captA_irq:** Capture unit A interrupt request
5:4	0h RW	**csi_irq:** CSI receiver interrupt request
3	0h RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

15.8.839 reg_inp_sys_irq_ctrl_irq_mask_type (inp_sys_irq_ctrl_irq_mask)—Offset 8C004h

IRQ mask per interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_irq_ctrl_irq_mask: [ISPMMADR] + 8C004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:19	18	17	16	15:13	12	11:10	9:8	7:6	5:4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0 0 0	0	0 0	0 0	0 0	0 0	0	0	0	0
unused_irq_mask	strmon_irq	dma_irq	cio2ahb_irq	inpsys_ctrl_irq	acq_irq	captC_irq	captB_irq	captA_irq	csi_irq	csi_pkt_eol	csi_pkt_sol	csi_pkt_eof	csi_pkt_sof

Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_mask:** Unused
18	0h RW	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RW	**acq_irq:** Acquisition unit interrupt request
11:10	0h RW	**captC_irq:** Capture unit C interrupt request
9:8	0h RW	**captB_irq:** Capture unit B interrupt request
7:6	0h RW	**captA_irq:** Capture unit A interrupt request
5:4	0h RW	**csi_irq:** CSI receiver interrupt request
3	0h RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

15.8.840 reg_inp_sys_irq_ctrl_irq_status_type (inp_sys_irq_ctrl_irq_status)—Offset 8C008h

IRQ status for each unmasked interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_irq_ctrl_irq_status: [ISPMMADR] + 8C008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31:19	18	17	16	15:13	12	11:10	9:8	7:6	5:4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0 0 0	0	0 0	0 0	0 0	0 0	0	0	0	0
unused_irq_status	strmon_irq	dma_irq	cio2ahb_irq	inpsys_ctrl_irq	acq_irq	captC_irq	captB_irq	captA_irq	csi_irq	csi_pkt_eol	csi_pkt_sol	csi_pkt_eof	csi_pkt_sof

Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_status:** Unused
18	0h RO	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RO	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RO	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RO	**acq_irq:** Acquisition unit interrupt request
11:10	0h RO	**captC_irq:** Capture unit C interrupt request
9:8	0h RO	**captB_irq:** Capture unit B interrupt request
7:6	0h RO	**captA_irq:** Capture unit A interrupt request
5:4	0h RO	**csi_irq:** CSI receiver interrupt request
3	0h RO	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RO	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RO	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RO	**csi_pkt_sof:** Start of Frame packet from CSI receiver

15.8.841 reg_inp_sys_irq_ctrl_irq_clear_type (inp_sys_irq_ctrl_irq_clear)—Offset 8C00Ch

IRQ clear for interrupt set in irq_status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_irq_ctrl_irq_clear: [ISPMMADR] + 8C00Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_irq_clear | strmon_irq | dma_irq | cio2ahb_irq | inpsys_ctrl_irq | acq_irq | captC_irq | captB_irq | captA_irq | csi_irq | csi_pkt_eol | csi_pkt_sol | csi_pkt_eof | csi_pkt_sof

Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_clear:** Unused
18	0h WO	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h WO	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h WO	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h WO	**acq_irq:** Acquisition unit interrupt request
11:10	0h WO	**captC_irq:** Capture unit C interrupt request
9:8	0h WO	**captB_irq:** Capture unit B interrupt request
7:6	0h WO	**captA_irq:** Capture unit A interrupt request
5:4	0h WO	**csi_irq:** CSI receiver interrupt request
3	0h WO	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h WO	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h WO	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h WO	**csi_pkt_sof:** Start of Frame packet from CSI receiver

15.8.842 reg_inp_sys_irq_ctrl_irq_en_type (inp_sys_irq_ctrl_irq_en)—Offset 8C010h

IRQ enable per interrupt bit

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

inp_sys_irq_ctrl_irq_en: [ISPMMADR] + 8C010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_irq_en													strmon_irq	dma_irq	cio2ahb_irq	inpsys_ctrl_irq			acq_irq	captC_irq		captB_irq		captA_irq		csi_irq		csi_pkt_eol	csi_pkt_sol	csi_pkt_eof	csi_pkt_sof

Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_en:** Unused
18	0h RW	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RW	**acq_irq:** Acquisition unit interrupt request
11:10	0h RW	**captC_irq:** Capture unit C interrupt request
9:8	0h RW	**captB_irq:** Capture unit B interrupt request
7:6	0h RW	**captA_irq:** Capture unit A interrupt request
5:4	0h RW	**csi_irq:** CSI receiver interrupt request
3	0h RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0h RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

15.8.843 reg_inp_sys_irq_ctrl_irq_level_not_pulse_type (inp_sys_irq_ctrl_irq_level_not_pulse)—Offset 8C014h

IRQ setting per interrupt bit for level or pulse irq generation at output pin. Level: 1, Pulse: 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

inp_sys_irq_ctrl_irq_level_not_pulse: [ISPMMADR] + 8C014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_irq_level_not_pulse | strmon_irq | dma_irq | cio2ahb_irq | inpsys_ctrl_irq | acq_irq | captC_irq | captB_irq | captA_irq | csi_irq | csi_pkt_eol | csi_pkt_sol | csi_pkt_eof | csi_pkt_sof

Bit Range	Default & Access	Description
31:19	0h RW	**unused_irq_level_not_pulse:** Unused
18	0h RW	**strmon_irq:** Streaming monitor interrupt request
17	0h RO	**dma_irq:** DMA interrupt request
16	0h RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0h RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0h RW	**acq_irq:** Acquisition unit interrupt request
11:10	0h RW	**captC_irq:** Capture unit C interrupt request
9:8	0h RW	**captB_irq:** Capture unit B interrupt request
7:6	0h RW	**captA_irq:** Capture unit A interrupt request
5:4	0h RW	**csi_irq:** CSI receiver interrupt request
3	0h RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver

Bit Range	Default & Access	Description
2	0h RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0h RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0h RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

15.8.844 reg_isel_gpr_reg_gp_syncgen_enable_type (isel_gpr_reg_gp_syncgen_enable)—Offset 90000h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_syncgen_enable: [ISPMMADR] + 90000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															unused_reg_gp_syncgen_enable																reg_gp_syncgen_enable

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_syncgen_enable:** Unused
0	0h RW	**reg_gp_syncgen_enable:** Enables (value=1) or disables (value=0) the Sync Generator.

15.8.845 reg_isel_gpr_reg_gp_syncgen_free_running_type (isel_gpr_reg_gp_syncgen_free_running)—Offset 90004h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_syncgen_free_running: [ISPMMADR] + 90004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_syncgen_free_running (31:1); reg_gp_syncgen_free_running (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_syncgen_free_running:** Unused
0	0h RW	**reg_gp_syncgen_free_running:** Sets the sync generator in free running mode (value=1) or let it stall in sync with either the PRBS or TPG (value=0)

15.8.846 reg_isel_gpr_reg_gp_syncgen_pause_type (isel_gpr_reg_gp_syncgen_pause)—Offset 90008h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_syncgen_pause: [ISPMMADR] + 90008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_syncgen_pause (31:1); reg_gp_syncgen_pause (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_syncgen_pause:** Unused

Bit Range	Default & Access	Description
0	0h RW	**reg_gp_syncgen_pause:** Sets the sync generator in pause mode (value=1) or not (value=0)

15.8.847 reg_isel_gpr_reg_gp_nr_frames_type (isel_gpr_reg_gp_nr_frames)—Offset 9000Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_nr_frames: [ISPMMADR] + 9000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:0
unused_reg_gp_nr_frames	reg_gp_nr_frames

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_nr_frames:** Unused
13:0	0h RW	**reg_gp_nr_frames:** Sets the sync generator parameter Number of Frames

15.8.848 reg_isel_gpr_reg_gp_syngen_nr_pix_type (isel_gpr_reg_gp_syngen_nr_pix)—Offset 90010h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syngen_nr_pix: [ISPMMADR] + 90010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_syngen_nr_pix

reg_gp_syngen_nr_pix

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syngen_nr_pix:** Unused
13:0	0h RW	**reg_gp_syngen_nr_pix:** Sets the number of active pixels per line in the Sync Generator

15.8.849 reg_isel_gpr_reg_gp_syngen_nr_lines_type (isel_gpr_reg_gp_syngen_nr_lines)—Offset 90014h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syngen_nr_lines: [ISPMMADR] + 90014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_syngen_nr_lines

reg_gp_syngen_nr_lines

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syngen_nr_lines:** Unused
13:0	0h RW	**reg_gp_syngen_nr_lines:** Sets the number of lines per frame in the Sync generator

15.8.850 reg_isel_gpr_reg_gp_syngen_hblank_cycles_type (isel_gpr_reg_gp_syngen_hblank_cycles)—Offset 90018h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syngen_hblank_cycles: [ISPMMADR] + 90018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_syngen_hblank_cycles | reg_gp_syngen_hblank_cycles

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syngen_hblank_cycles:** Unused
13:0	0h RW	**reg_gp_syngen_hblank_cycles:** Sets the number of cycles between the end-of-line and start-of-line pulses.

15.8.851 reg_isel_gpr_reg_gp_syngen_vblank_cycles_type (isel_gpr_reg_gp_syngen_vblank_cycles)—Offset 9001Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syngen_vblank_cycles: [ISPMMADR] + 9001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_syngen_vblank_cycles

reg_gp_syngen_vblank_cycles

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syngen_vblank_cycles:** Unused
13:0	0h RW	**reg_gp_syngen_vblank_cycles:** Sets the number of cycles between the end-of-frame and start-of-frame pulses.

15.8.852 reg_isel_gpr_reg_gp_isel_sof_type (isel_gpr_reg_gp_isel_sof)—Offset 90020h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_sof: [ISPMMADR] + 90020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_sof

reg_gp_isel_sof

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_sof:** Unused
0	0h RW	**reg_gp_isel_sof:** Sets the input selector gp_sof input.

15.8.853 reg_isel_gpr_reg_gp_isel_eof_type (isel_gpr_reg_gp_isel_eof)—Offset 90024h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_eof: [ISPMMADR] + 90024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gp_isel_eof (31:1), reg_gp_isel_eof (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_eof:** Unused
0	0h RW	**reg_gp_isel_eof:** Sets the input selector gp_eof input.

15.8.854 reg_isel_gpr_reg_gp_isel_sol_type (isel_gpr_reg_gp_isel_sol)—Offset 90028h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_sol: [ISPMMADR] + 90028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gp_isel_sol (31:1), reg_gp_isel_sol (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_sol:** Unused
0	0h RW	**reg_gp_isel_sol:** Sets the input selector gp_sol input.

15.8.855 reg_isel_gpr_reg_gp_isel_eol_type (isel_gpr_reg_gp_isel_eol)—Offset 9002Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_eol: [ISPMMADR] + 9002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_eol (bits 31:1)
reg_gp_isel_eol (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_eol:** Unused
0	0h RW	**reg_gp_isel_eol:** Sets the input selector gp_eol input.

15.8.856 reg_isel_gpr_reg_gp_isel_lfsr_enable_type (isel_gpr_reg_gp_isel_lfsr_enable)—Offset 90030h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_lfsr_enable: [ISPMMADR] + 90030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_lfsr_enable

reg_gp_isel_lfsr_enable

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_lfsr_enable:** Unused
0	0h RW	**reg_gp_isel_lfsr_enable:** Enables the PRBS

15.8.857 reg_isel_gpr_reg_gp_isel_lfsr_enable_b_type (isel_gpr_reg_gp_isel_lfsr_enable_b)—Offset 90034h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_lfsr_enable_b: [ISPMMADR] + 90034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_lfsr_enable_b

reg_gp_isel_lfsr_enable_b

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_lfsr_enable_b:** Unused

Bit Range	Default & Access	Description
0	0h RW	**reg_gp_isel_lfsr_enable_b:** Enables the PRBS for port b

15.8.858 reg_isel_gpr_reg_gp_isel_lfsr_reset_value_type (isel_gpr_reg_gp_isel_lfsr_reset_value)—Offset 90038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_lfsr_reset_value: [ISPMMADR] + 90038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	30 … 0
0	000 0000 0000 0000 0000 0000 0000 0000
unused_reg_gp_isel_lfsr_reset_value	reg_gp_isel_lfsr_reset_value

Bit Range	Default & Access	Description
31	0h RW	**unused_reg_gp_isel_lfsr_reset_value:** Unused
30:0	0h RW	**reg_gp_isel_lfsr_reset_value:** Set the reset value of the LFSR in the PRBS of the Input selector

15.8.859 reg_isel_gpr_reg_gp_isel_tpg_enable_type (isel_gpr_reg_gp_isel_tpg_enable)—Offset 9003Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_enable: [ISPMMADR] + 9003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_tpg_enable

reg_gp_isel_tpg_enable

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_tpg_enable:** Unused
0	0h RW	**reg_gp_isel_tpg_enable:** Enables the test pattern generator

15.8.860 reg_isel_gpr_reg_gp_isel_tpg_enable_b_type (isel_gpr_reg_gp_isel_tpg_enable_b)—Offset 90040h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_enable_b: [ISPMMADR] + 90040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_tpg_enable_b

reg_gp_isel_tpg_enable_b

Bit Range	Default & Access	Description
31:1	0h RW	**unused_reg_gp_isel_tpg_enable_b:** Unused

Bit Range	Default & Access	Description
0	0h RW	**reg_gp_isel_tpg_enable_b:** Enables the test pattern generator for port b

15.8.861 reg_isel_gpr_reg_gp_isel_hor_cnt_mask_type (isel_gpr_reg_gp_isel_hor_cnt_mask)—Offset 90044h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_hor_cnt_mask: [ISPMMADR] + 90044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:0
unused_reg_gp_isel_hor_cnt_mask	reg_gp_isel_hor_cnt_mask

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_isel_hor_cnt_mask:** Unused
13:0	0h RW	**reg_gp_isel_hor_cnt_mask:** Sets the horizontal counter mask in the Input selector

15.8.862 reg_isel_gpr_reg_gp_isel_ver_cnt_mask_type (isel_gpr_reg_gp_isel_ver_cnt_mask)—Offset 90048h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_ver_cnt_mask: [ISPMMADR] + 90048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_ver_cnt_mask

reg_gp_isel_ver_cnt_mask

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_isel_ver_cnt_mask:** Unused
13:0	0h RW	**reg_gp_isel_ver_cnt_mask:** Sets the vertical counter mask in the Input selector

15.8.863 reg_isel_gpr_reg_gp_isel_xy_cnt_mask_type (isel_gpr_reg_gp_isel_xy_cnt_mask)—Offset 9004Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_xy_cnt_mask: [ISPMMADR] + 9004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_xy_cnt_mask

reg_gp_isel_xy_cnt_mask

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_xy_cnt_mask:** Unused

Bit Range	Default & Access	Description
11:0	0h RW	**reg_gp_isel_xy_cnt_mask:** Sets the xy counter mask in the Input selector

15.8.864 reg_isel_gpr_reg_gp_isel_hor_cnt_delta_type (isel_gpr_reg_gp_isel_hor_cnt_delta)—Offset 90050h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_hor_cnt_delta: [ISPMMADR] + 90050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
unused_reg_gp_isel_hor_cnt_delta	reg_gp_isel_hor_cnt_delta

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_gp_isel_hor_cnt_delta:** Unused
3:0	0h RW	**reg_gp_isel_hor_cnt_delta:** sets the horizontal counter delta in the Input selector

15.8.865 reg_isel_gpr_reg_gp_isel_ver_cnt_delta_type (isel_gpr_reg_gp_isel_ver_cnt_delta)—Offset 90054h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_ver_cnt_delta: [ISPMMADR] + 90054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_ver_cnt_delta | reg_gp_isel_ver_cnt_delta

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_gp_isel_ver_cnt_delta:** Unused
3:0	0h RW	**reg_gp_isel_ver_cnt_delta:** Sets the vertical counter delta in the Input selector

15.8.866 reg_isel_gpr_reg_gp_isel_tpg_mode_type (isel_gpr_reg_gp_isel_tpg_mode)—Offset 90058h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_mode: [ISPMMADR] + 90058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_tpg_mode | reg_gp_isel_tpg_mode

Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_tpg_mode:** Unused
1:0	0h RW	**reg_gp_isel_tpg_mode:** Sets the mode of the test pattern generator. 'b00-ramp mode, 'b01-checkerboard, 'b10-frame based color

15.8.867 reg_isel_gpr_reg_gp_isel_tpg_red1_type (isel_gpr_reg_gp_isel_tpg_red1)—Offset 9005Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_red1: [ISPMMADR] + 9005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_gp_isel_tpg_red1																				reg_gp_isel_tpg_red1											

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_red1:** Unused
11:0	0h RW	**reg_gp_isel_tpg_red1:** Defines the red1 color for test pattern generator

15.8.868 reg_isel_gpr_reg_gp_isel_tpg_green1_type (isel_gpr_reg_gp_isel_tpg_green1)—Offset 90060h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_green1: [ISPMMADR] + 90060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_reg_gp_isel_tpg_green1	reg_gp_isel_tpg_green1

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_green1:** Unused
11:0	0h RW	**reg_gp_isel_tpg_green1:** Defines the green1 color for test pattern generator

15.8.869 reg_isel_gpr_reg_gp_isel_tpg_blue1_type (isel_gpr_reg_gp_isel_tpg_blue1)—Offset 90064h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_blue1: [ISPMMADR] + 90064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_reg_gp_isel_tpg_blue1	reg_gp_isel_tpg_blue1

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_blue1:** Unused
11:0	0h RW	**reg_gp_isel_tpg_blue1:** Defines the blue1 color for test pattern generator

15.8.870 reg_isel_gpr_reg_gp_isel_tpg_red2_type (isel_gpr_reg_gp_isel_tpg_red2)—Offset 90068h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_red2: [ISPMMADR] + 90068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_reg_gp_isel_tpg_red2	reg_gp_isel_tpg_red2

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_red2:** Unused
11:0	0h RW	**reg_gp_isel_tpg_red2:** Defines the red2 color for test pattern generator

15.8.871 reg_isel_gpr_reg_gp_isel_tpg_green2_type (isel_gpr_reg_gp_isel_tpg_green2)—Offset 9006Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_green2: [ISPMMADR] + 9006Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_gp_isel_tpg_green2																				reg_gp_isel_tpg_green2											

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_green2:** Unused
11:0	0h RW	**reg_gp_isel_tpg_green2:** Defines the green2 color for test pattern generator

15.8.872 reg_isel_gpr_reg_gp_isel_tpg_blue2_type (isel_gpr_reg_gp_isel_tpg_blue2)—Offset 90070h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_tpg_blue2: [ISPMMADR] + 90070h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_gp_isel_tpg_blue2																				reg_gp_isel_tpg_blue2											

Bit Range	Default & Access	Description
31:12	0h RW	**unused_reg_gp_isel_tpg_blue2:** Unused
11:0	0h RW	**reg_gp_isel_tpg_blue2:** Defines the blue2 color for test pattern generator

15.8.873 reg_isel_gpr_reg_gp_isel_ch_id_type (isel_gpr_reg_gp_isel_ch_id)—Offset 90074h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_ch_id: [ISPMMADR] + 90074h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gp_isel_ch_id (bits 31:2), reg_gp_isel_ch_id (bits 1:0)

Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_ch_id:** Unused
1:0	0h RW	**reg_gp_isel_ch_id:** Sets the channel id input for the Input selector

15.8.874 reg_isel_gpr_reg_gp_isel_fmt_type_type (isel_gpr_reg_gp_isel_fmt_type)—Offset 90078h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_fmt_type: [ISPMMADR] + 90078h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gp_isel_fmt_type, reg_gp_isel_fmt_type

Bit Range	Default & Access	Description
31:5	0h RW	**unused_reg_gp_isel_fmt_type:** Unused
4:0	0h RW	**reg_gp_isel_fmt_type:** Sets the format type input for the Input selector

15.8.875 reg_isel_gpr_reg_gp_isel_data_sel_type (isel_gpr_reg_gp_isel_data_sel)—Offset 9007Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_data_sel: [ISPMMADR] + 9007Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_gp_isel_data_sel

reg_gp_isel_data_sel

Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_data_sel:** Unused
1:0	0h RW	**reg_gp_isel_data_sel:** Select value for the data multiplexer in the Input selector

15.8.876 reg_isel_gpr_reg_gp_isel_sband_sel_type (isel_gpr_reg_gp_isel_sband_sel)—Offset 90080h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_isel_sband_sel: [ISPMMADR] + 90080h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:2: unused_reg_gp_isel_sband_sel
Bits 1:0: reg_gp_isel_sband_sel

Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_sband_sel:** Unused
1:0	0h RW	**reg_gp_isel_sband_sel:** Select value for the side band multiplexer in the Input selector

15.8.877 reg_isel_gpr_reg_gp_isel_sync_sel_type (isel_gpr_reg_gp_isel_sync_sel)—Offset 90084h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_isel_sync_sel: [ISPMMADR] + 90084h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:2: unused_reg_gp_isel_sync_sel
Bits 1:0: reg_gp_isel_sync_sel

Bit Range	Default & Access	Description
31:2	0h RW	**unused_reg_gp_isel_sync_sel:** Unused
1:0	0h RW	**reg_gp_isel_sync_sel:** Select value for the sync multiplexer in the Input selector

15.8.878 reg_isel_gpr_reg_gp_syncgen_hor_cnt_type (isel_gpr_reg_gp_syncgen_hor_cnt)—Offset 90088h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_hor_cnt: [ISPMMADR] + 90088h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: unused_reg_gp_syncgen_hor_cnt (bits 31:14), reg_gp_syncgen_hor_cnt (bits 13:0)

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syncgen_hor_cnt:** Unused
13:0	0h RO	**reg_gp_syncgen_hor_cnt:** Returns the value of the horizontal counter in the sync generator

15.8.879 reg_isel_gpr_reg_gp_syncgen_ver_cnt_type (isel_gpr_reg_gp_syncgen_ver_cnt)—Offset 9008Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_ver_cnt: [ISPMMADR] + 9008Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:0
unused_reg_gp_syncgen_ver_cnt	reg_gp_syncgen_ver_cnt

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syncgen_ver_cnt:** Unused
13:0	0h RO	**reg_gp_syncgen_ver_cnt:** Returns the value of the vertical counter in the sync generator

15.8.880 reg_isel_gpr_reg_gp_syncgen_frame_cnt_type (isel_gpr_reg_gp_syncgen_frame_cnt)—Offset 90090h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_gpr_reg_gp_syncgen_frame_cnt: [ISPMMADR] + 90090h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:0
unused_reg_gp_syncgen_frame_cnt	reg_gp_syncgen_frame_cnt

Bit Range	Default & Access	Description
31:14	0h RW	**unused_reg_gp_syncgen_frame_cnt:** Unused

Bit Range	Default & Access	Description
13:0	0h RO	**reg_gp_syncgen_frame_cnt:** Returns the value of the frame counter in the sync generator

15.8.881 reg_isel_gpr_reg_gp_soft_reset_type (isel_gpr_reg_gp_soft_reset)—Offset 90094h

Soft resets the modules in the input selector cluster

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_gpr_reg_gp_soft_reset: [ISPMMADR] + 90094h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
unused_reg_gp_soft_reset																												srst_fifo	srst_tpg	srst_prbs	srst_syncgen

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_gp_soft_reset:** Unused
3	0h RW	**srst_fifo:** If 1, the fifo is held in reset mode. If 0, the fifo is not in reset state.
2	0h RW	**srst_tpg:** If 1, the TPG is held in reset mode. If 0, the TPG is not in reset state.
1	0h RW	**srst_prbs:** If 1, the PRBS is held in reset mode. If 0, the PRBS is not in reset state.
0	0h RW	**srst_syncgen:** If 1, the sync generator is held in reset mode. If 0, the sync generator is not in reset state.

15.8.882 reg_isel_fa_send_to_GP_FIFO_type (isel_fa_send_to_GP_FIFO)—Offset 90100h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_fa_send_to_GP_FIFO: [ISPMMADR] + 90100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_send_to_GP_FIFO

send_to_GP_FIFO

Bit Range	Default & Access	Description
31:26	0h RW	**unused_send_to_GP_FIFO:** Unused
25:0	0h WO	**send_to_GP_FIFO:** Send data to input selector GP FIFO

15.8.883 reg_isel_fa_check_send_to_GP_FIFO_type (isel_fa_check_send_to_GP_FIFO)—Offset 90108h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_fa_check_send_to_GP_FIFO: [ISPMMADR] + 90108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

unused_check_send_to_GP_FIFO

check_send_to_GP_FIFO

Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_send_to_GP_FIFO:** Unused
0	1h WO	**check_send_to_GP_FIFO:** Check for availability of GP FIFO. Returns 1 if a word can be send to the input selector, without it being stalled

15.8.884 reg_isel_irq_ctrl_reg_irq_edge_type (isel_irq_ctrl_reg_irq_edge)—Offset 90200h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_edge: [ISPMMADR] + 90200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:4	3:0
Value	0000 0000 0000 0000 0000 0000 0000	0000
Field	unused_reg_irq_edge	reg_irq_edge

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_edge:** Unused
3:0	0h RW	**reg_irq_edge:** indicates for each bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

15.8.885 reg_isel_irq_ctrl_reg_irq_mask_type (isel_irq_ctrl_reg_irq_mask)—Offset 90204h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_mask: [ISPMMADR] + 90204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:4	3:0
Value	0000 0000 0000 0000 0000 0000 0000	0000
Field	unused_reg_irq_mask	reg_irq_mask

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_mask:** Unused
3:0	0h RW	**reg_irq_mask:** indicates for each bit of irq_di whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

15.8.886 reg_isel_irq_ctrl_reg_irq_status_type (isel_irq_ctrl_reg_irq_status)—Offset 90208h

Indicates for each bit whether a non-masked interrupt has been generated (value='1'). Can be cleared by writing a '1' into the the corresponding bit of the req_irq_clear register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_irq_ctrl_reg_irq_status: [ISPMMADR] + 90208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

Bits	31:4	3	2	1	0
Value	0000 0000 0000 0000 0000 0000 0000	0	0	0	0
Field	unused_reg_irq_status	irq_stat_syncgen_eol	irq_stat_syncgen_sol	irq_stat_syncgen_eof	irq_stat_syncgen_sof

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_status:** Unused
3	0h RO	**irq_stat_syncgen_eol:** Represents the irq status of the eol (end of line) bit generated by the sync generator
2	0h RO	**irq_stat_syncgen_sol:** Represents the irq status of the sol (start of line) bit generated by the sync generator
1	0h RO	**irq_stat_syncgen_eof:** Represents the irq status of the eof (end of frame) bit generated by the sync generator
0	0h RO	**irq_stat_syncgen_sof:** Represents the irq status of the sof (start of frame) bit generated by the sync generator

15.8.887 reg_isel_irq_ctrl_reg_irq_clear_type (isel_irq_ctrl_reg_irq_clear)—Offset 9020Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_irq_ctrl_reg_irq_clear: [ISPMMADR] + 9020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_irq_clear | reg_irq_clear

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_clear:** Unused
3:0	0h WO	**reg_irq_clear:** Clears (set to '0') bits in reg_irq_status. When writing a '1' into a bit of this register, the corresponding bit in the req_irq_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the req_irq_status is not affected.

15.8.888 reg_isel_irq_ctrl_reg_irq_enable_type (isel_irq_ctrl_reg_irq_enable)—Offset 90210h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isel_irq_ctrl_reg_irq_enable: [ISPMMADR] + 90210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_reg_irq_enable | reg_irq_enable

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_enable:** Unused
3:0	0h RW	**reg_irq_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also affects the IRQ pin (value='1') or not (value='0')

15.8.889 reg_isel_irq_ctrl_reg_irq_level_not_pulse_type (isel_irq_ctrl_reg_irq_level_not_pulse)—Offset 90214h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isel_irq_ctrl_reg_irq_level_not_pulse: [ISPMMADR] + 90214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

unused_reg_irq_level_not_pulse

reg_irq_level_not_pulse

Bit Range	Default & Access	Description
31:4	0h RW	**unused_reg_irq_level_not_pulse:** Unused
3:0	0h RW	**reg_irq_level_not_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

15.8.890 reg_icache_out_sys_c_mmu_MMU_invalidate_cache_type (icache_out_sys_c_mmu_MMU_invalidate_cache)—Offset A0000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

icache_out_sys_c_mmu_MMU_invalidate_cache: [ISPMMADR] + A0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MMU_invalidate_cache (bits 31:1), MMU_invalidate_cache (bit 0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_MMU_invalidate_cache:** Unused
0	0h WO	**MMU_invalidate_cache:** MMU invalidate cache. When '1', the MMUs TLB is invalidated.

15.8.891 reg_icache_out_sys_c_mmu_MMU_page_table_base_type (icache_out_sys_c_mmu_MMU_page_table_base)—Offset A0004h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

icache_out_sys_c_mmu_MMU_page_table_base:
[ISPMMADR] + A0004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_MMU_page_table_base (bits 31:24), MMU_page_table_base (bits 23:0)

Bit Range	Default & Access	Description
31:24	0h RW	**unused_MMU_page_table_base:** Unused

Bit Range	Default & Access	Description
23:0	0h RW	**MMU_page_table_base:** Defines the physical page number of the page tables

15.8.892 mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first)—Offset B0000h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first: [ISPMMADR] + B0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

prg_mem_first

Bit Range	Default & Access	Description
63:0	0h RW	**prg_mem_first:** Read Latency of 1 cycles. Write latency of 0 cycles

15.8.893 mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last)—Offset B7FF8h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last: [ISPMMADR] + B7FF8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

prg_mem_last

Bit Range	Default & Access	Description
63:0	0h RW	**prg_mem_last:** Read Latency of 1 cycles. Write latency of 0 cycles

15.8.894 mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1C0000h

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first: [ISPMMADR] + 1C0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0				asp_lut_first											

Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

15.8.895 mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1C0FFEh

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last: [ISPMMADR] + 1C0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0				asp_lut_last											

Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

15.8.896 mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1D0000h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first:
[ISPMMADR] + 1D0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0				asp_lut_first											

Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

15.8.897 mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1D0FFEh

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last:
[ISPMMADR] + 1D0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0				asp_lut_last											

Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

15.8.898 mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1E0000h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first:
[ISPMMADR] + 1E0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0				asp_lut_first											

Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

15.8.899 mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1E0FFEh

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last:
[ISPMMADR] + 1E0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0				asp_lut_last											

Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:0	0h RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

15.8.900 mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first)—Offset 1F0000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first: [ISPMMADR] + 1F0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (31:24), asp_histogram_first (23:0)

Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23:0	0h RW	**asp_histogram_first:** Read Latency of 66 cycles. Write latency of 0 cycles

15.8.901 mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last)—Offset 1F0FFCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last: [ISPMMADR] + 1F0FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | asp_histogram_last

Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23:0	0h RW	**asp_histogram_last:** Read Latency of 66 cycles. Write latency of 0 cycles

15.8.902 mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_first_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_first)—Offset 200000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

isp_base_dmem_data_mem_sl_ipdmem_data_mem_first: [ISPMMADR] + 200000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

data_mem_first

Bit Range	Default & Access	Description
31:0	0h RW	**data_mem_first:** Read Latency of 2 cycles. Write latency of 0 cycles

15.8.903 mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_last_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_last)—Offset 203FFCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

isp_base_dmem_data_mem_sl_ipdmem_data_mem_last: [ISPMMADR] + 203FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

data_mem_last

Bit Range	Default & Access	Description
31:0	0h RW	**data_mem_last:** Read Latency of 2 cycles. Write latency of 0 cycles

15.8.904 mem_scp_dmem_mem_sl_ip_dmem_mem_first_type (scp_dmem_mem_sl_ip_dmem_mem_first)—Offset 300000h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_dmem_mem_sl_ip_dmem_mem_first: [ISPMMADR] + 300000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

mem_first

Bit Range	Default & Access	Description
31:0	0h RW	**mem_first:** Read Latency of 2 cycles. Write latency of 0 cycles

15.8.905 mem_scp_dmem_mem_sl_ip_dmem_mem_last_type (scp_dmem_mem_sl_ip_dmem_mem_last)—Offset 307FFCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

scp_dmem_mem_sl_ip_dmem_mem_last: [ISPMMADR] + 307FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

mem_last

Bit Range	Default & Access	Description
31:0	0h RW	**mem_last:** Read Latency of 2 cycles. Write latency of 0 cycles

15.8.906 reg_fa_sp_isp_send_to_SP_type (fa_sp_isp_send_to_SP)—Offset 380008h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

fa_sp_isp_send_to_SP: [ISPMMADR] + 380008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

send_to_SP

Bit Range	Default & Access	Description
31:0	0h WO	**send_to_SP:** Send data to SP streaming input port

15.8.907 reg_fa_sp_isp_send_to_ISP_type (fa_sp_isp_send_to_ISP)—Offset 38000Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

fa_sp_isp_send_to_ISP: [ISPMMADR] + 38000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

send_to_ISP

Bit Range	Default & Access	Description
31:0	0h WO	**send_to_ISP:** Send data to ISP streaming input port

15.8.908 reg_fa_sp_isp_check_receive_from_SP_type (fa_sp_isp_check_receive_from_SP)—Offset 380010h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

fa_sp_isp_check_receive_from_SP: [ISPMMADR] + 380010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

unused_check_receive_from_SP
check_receive_from_SP

Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_receive_from_SP:** Unused
0	1h RO	**check_receive_from_SP:** Check for potential stalling for receiving data on SP streaming output port. Returns 1 if a receive from SP would lead to a stall. Returns 0 if a token is available from the SP.

15.8.909 reg_fa_sp_isp_check_receive_from_ISP_type (fa_sp_isp_check_receive_from_ISP)—Offset 380014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

fa_sp_isp_check_receive_from_ISP: [ISPMMADR] + 380014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

unused_check_receive_from_ISP (31:1), check_receive_from_ISP (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_receive_from_ISP:** Unused
0	1h RO	**check_receive_from_ISP:** Check for potential stalling for receiving data on ISP streaming output port. Returns 1 if a receive from ISP would lead to a stall. Returns 0 if a token is available from the ISP.

15.8.910 reg_fa_sp_isp_check_send_to_SP_type (fa_sp_isp_check_send_to_SP)—Offset 380018h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

fa_sp_isp_check_send_to_SP: [ISPMMADR] + 380018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_check_send_to_SP (31:1), check_send_to_SP (0)

Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_send_to_SP:** Unused
0	0h RO	**check_send_to_SP:** Check for potential stalling for sending data to SP streaming input port. Returns 1 if a send to SP would lead to a stall. Returns 0 when there is space left in the SP token FIFO

15.8.911 reg_fa_sp_isp_check_send_to_ISP_type (fa_sp_isp_check_send_to_ISP)—Offset 38001Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

fa_sp_isp_check_send_to_ISP: [ISPMMADR] + 38001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

unused_check_send_to_ISP

check_send_to_ISP

Bit Range	Default & Access	Description
31:1	0h RW	**unused_check_send_to_ISP:** Unused
0	0h RO	**check_send_to_ISP:** Check for potential stalling for sending data to ISP streaming input port. Returns 1 if a send to ISP would lead to a stall. Returns 0 when there is space left in the ISP token FIFO

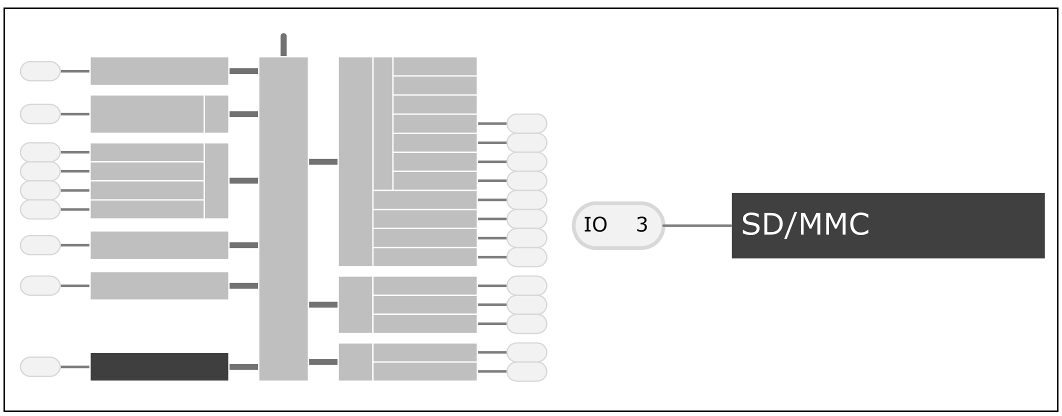
16 Storage Control Cluster (eMMC, SDIO, SD Card)

The Storage Control Cluster (SCC) consists of SDIO, SD Card and eMMC controllers to support mass storage and IO devices.

- One eMMC 4.5 interface
- One SD Card 3.0 interface
- One SDIO 3.0 interface for SDIO-based WIFI

Note: All units in the SCC support both PCI mode and ACPI mode of operation. A level shifter may be needed on the platform for SDIO 3.0 compliance. An eMMC 4.41 controller also exists but shouldn't be used.

Note: eMMC* 5.0 is functional and backward compatible on the Bay Trail platform for features included in eMMC 4.5, with no guarantees the performance is as good as eMMC* 4.5.



16.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 181. eMMC Signals

Signal Name	Direction Power	Description
MMC1_CLK	O V1P8S	**eMMC Clock** The frequency may vary between 400 kHz and 200 MHz.
MMC1_D[7:0]	I/O V1P8S	**eMMC Port Data bits 0 to 7** Bidirectional port used to transfer data to and from eMMC device. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using either D[0]-D[3] or D[0]-D[7], by the MultiMedia Card controller. The MultiMedia Card includes internal pull-ups for data lines D[1]-D[7]. Immediately after entering the 4-bit mode, the card disconnects the internal pull ups of lines D[1], D[2], and D[3]. Correspondingly, immediately after entering to the 8-bit mode the card disconnects the internal pull-ups of lines D[1]-D[7].
MMC1_CMD	I/O V1P8S	**eMMC Port Command** This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.
MMC1_RCOMP	-	**eMMC RCOMP** This signal is used for pre-driver slew rate compensation.
MMC1_RST#	O V1P8S	**eMMC Reset Signals** Active low to reset.

Table 182. SDIO Signals

Signal Name	Direction Power	Description
SD2_CLK	O V1P8S	**SDIO Clock** The frequency may vary between 24 and 50MHz.
SD2_D[2:0]	I/O V1P8S	**SDIO Port Data bits 0 to 2** Bidirectional port used to transfer data to and from SDIO device. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].
SD2_D[3]_CD#	I/O V1P8S	**SDIO Port Data bit 3** Bidirectional port used to transfer data to and from the SDIO device. Also, **Card Detect**. Active low when device is present.
SD2_CMD	I/O V1P8S	**SDIO Port Command** This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.

Table 183. SD Card Signals

Signal Name	Direction Power	Description
SD3_CLK	O VSDIO	**SD Card Clock** The frequency may vary between 24 and 50 MHz.
SD3_D[3:0]	I/O VSDIO	**SD Card Data bits 0 to 3** Bidirectional port used to transfer data to and from SD card. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].
SD3_CD#	I/O V1P8S	**SD Card Detect** Active low when a card is present. Floating (pulled high with internal PU) when a card is not present.
SD3_CMD	I/O VSDIO	**SD Card Command** This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.
SD3_1P8EN	O V1P8S	**SD Card 1.8V Enable** Indicates the voltage of the SD Card to the power delivery subsystem. The default voltage (3.3 V) is requested when this signal is driven low. 1.8 V is requested when this signal is high. This voltage change applies to the SD3_V1P8V3P3_S3 (VSDIO) rail on the SoC.
SD3_RCOMP	-	**SD Card RCOMP** This signal is used for pre-driver slew rate compensation.
SD3_WP	I V1P8S	**SD Card Write Protect** Active high to protect from write.
SD3_PWREN#	O V1P8S	**SD Card Power Enable** This signal is used to enable power on a SD device.

16.2 Features

16.2.1 eMMC Interface Features

- eMMC 4.5 controller supported
- Transfers the data in 1 bit, 4 bit and 8 bit modes.
- Transfers data in the following speed classes: Baseline (1, 4, 8 bit up to 25Mhz), HS SDR/DDR (4, 8 bit up to 50Mhz) and HS200 (4, 8 bit up to 200MHz - 4.5 controller only)
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity.
- Supports MMC Plus and MMC mobile.
- Supports both round-robin and priority-based arbitration for transmit operation.
- Run-time configurabilty of channel ID bits.

16.2.2 SDIO/SD Card Interface Features

- Up to 400Mbits per second data rate using 4 parallel data lines.
- Transfers the data in 1 bit and 4 bit SD modes and SPI mode.
- Transfers the data in following UHS-I modes: HS ,DDR50 and SDR12/25.
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity.
- Designed to work with I/O cards, Read-only cards and Read/Write cards.
- Supports Read wait Control, Suspend/Resume operation.

Note: SDIO only validated with WIFI devices.

16.2.3 Storage Interfaces Overview

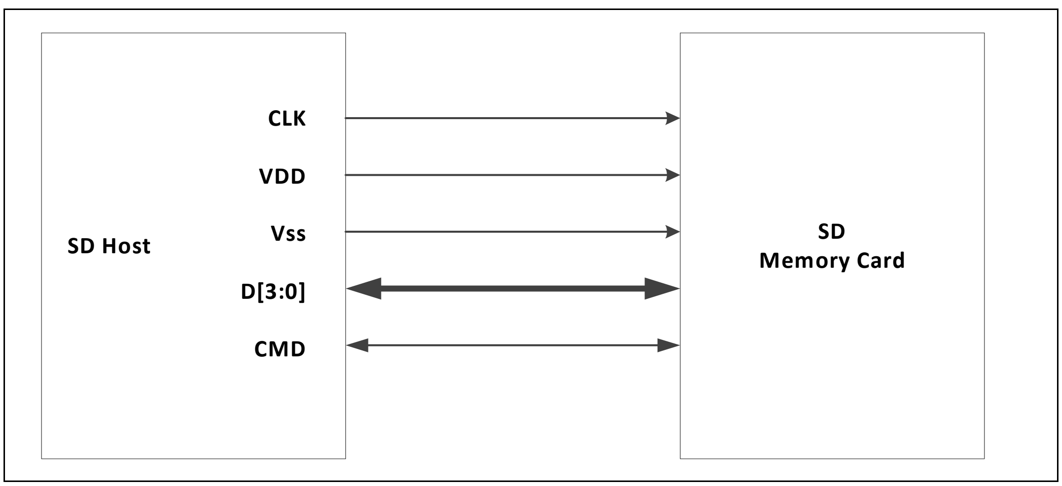
This section provides a very high level overview of the SD, SDIO, eMMC 4.5 specification. Refer to the SD and eMMC specifications for complete details.

16.2.3.1 SD Card 3.0 Bus Interface

The SD Card bus has a single master, single slaves (card), synchronous topology (refer to Figure 98). During initialization process commands are sent to the card, allowing the application to detect the card and assign logical addresses to the physical slot. All data communication in the Card Identification Mode uses the command line (CMD) only.

SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Card will use only SD3_D[0] for data transfer. After initialization the host can change the bus width (number of active data lines). This feature allows easy trade off between hardware cost and system performance. Note that while DAT1-SD3_D[3:1] are not in use, the SoC will tri-state those signals.

Figure 98. SD Memory Card Bus Topology

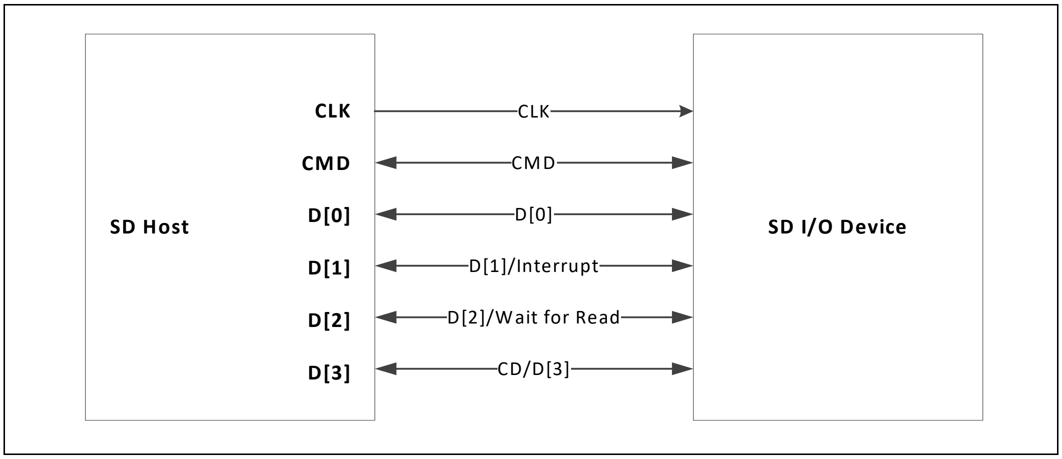


16.2.3.2 SDIO 3.0 Interface

The SDIO interface is the very much like the SD card interface. The SoC supports one SDIO device for wireless devices only (no memory card support).

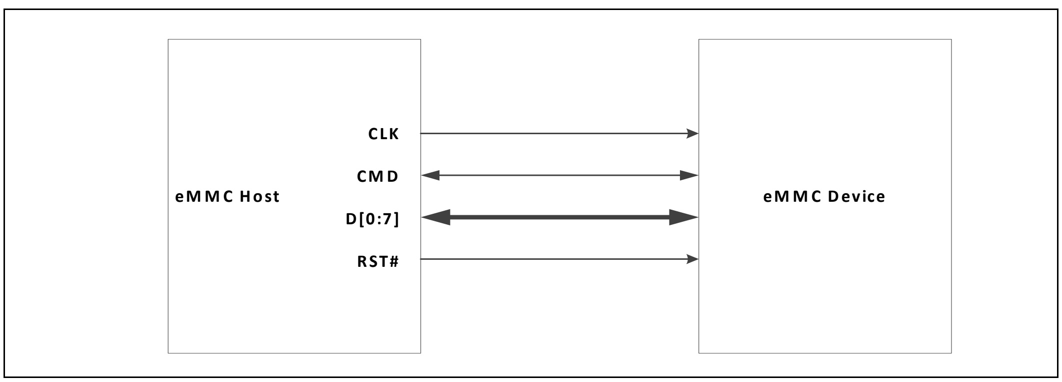
Note: SDIO interface does not support WAKE function.

Figure 99. SDIO Device Bus Topology



16.2.3.3 eMMC4.5 Interface

Figure 100. eMMC Interface



16.3 References

The controller is configured to comply with:

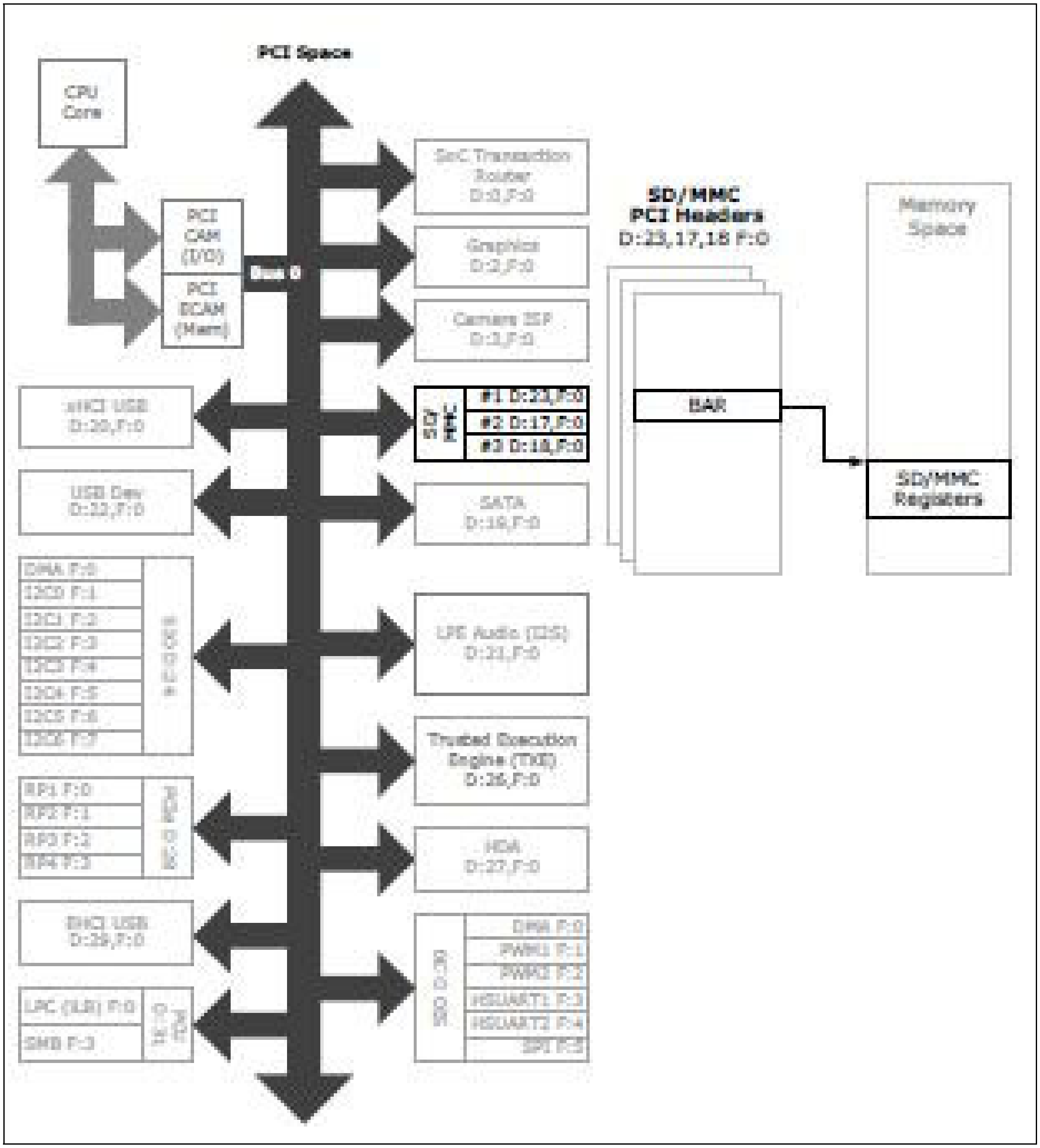
- SD Specification Part 01 Physical Layer Specification version 3.00, April 16, 2009
- SD Specification Part E1 SDIO Specification version 3.00, December 16, 2010
- SD Specification Part A2 SD Host Controller Standard Specification version 3.00, February 18, 2010
- SD Specification Part 03 security Specification version 1.01, April 15, 2001

- Embedded MultiMedia Card (eMMC) Product Standard v4.51, JESD84-A451

16.4 Register Map

Refer to Chapter 3, “Register Access Methods” and Chapter 4, “Mapping Address Spaces” for additional information.

Figure 101.Storage Control Cluster Register Map



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16.5 SDIO for Wifi PCI Configuration Registers

Table 184. Summary of SDIO for Wifi PCI Configuration Registers—0/17/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 1759	00000000h
4–7h	4	"Status and Command Register (STATUSCOMMAND)—Offset 4h" on page 1760	00100000h
8–Bh	4	"Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h" on page 1761	00000000h
C–Fh	4	"Cache Line Size, Latency Timer, and Header Type Register (CLLATHEADERBIST)—Offset Ch" on page 1761	00000000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 1762	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 1763	00000000h
2C–2Fh	4	"Subsystem Vendor ID and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch" on page 1764	00000000h
30–33h	4	"Expansion ROM Base Address Register (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1764	00000000h
34–37h	4	"Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h" on page 1765	00000080h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 1765	00000100h
80–83h	4	"Power Management Capability ID Register (POWERCAPID)—Offset 80h" on page 1766	48030001h
84–87h	4	"Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 1766	00000008h
A0–A3h	4	"General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h" on page 1767	00000000h
A4–A7h	4	"General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h" on page 1768	00000000h
A8–ABh	4	"General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h" on page 1768	00000000h
AC–AFh	4	"General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh" on page 1768	00000000h
C0–C3h	4	"General Purpose Input Register (GEN_INPUT_REGRW)—Offset C0h" on page 1769	00000000h
F8–FBh	4	"Manufacturers ID Register (MANID)—Offset F8h" on page 1769	00000000h

16.5.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	0000h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

16.5.2 Status and Command Register (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:17, F:0] + 4h

Default: 00100000h

31 28 24 20 16 12 8 4 0

Reserved0	RMA	RCA	Reserved1	CAPLIST	INTR_STATUS	Reserved2	Reserved3	INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5	BME	MSE	Reserved6
0 0	0	0	0 0 0 0 0 0 0	1	0	0 0 0	0 0 0 0 0	0	0	0	0 0 0 0 0	0	0	0

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a '1' to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0h RW/1C	**Received Target Abort (RCA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt; i.e., Bridge does not send Interrupt Assert message through the IOSF SideBand Channel. Reset value of this bit is 0.
9	0h RO	**Reserved4:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SERR# Enable (SERR_ENABLE):** This bit controls the sending of DO_SERR messages on IOSF SB.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridges response to downstream memory accesses. When set, accesses to the memory space of the device are enabled. Reset value of this bit is 0.
0	0h RO	**Reserved6:** Reserved.

16.5.3 Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:17, F:0] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CLASS_CODES																								RID							

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** This register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Identifies the revision of a particular AHB device. This is tied to a strap at the top level.

16.5.4 Cache Line Size, Latency Timer, and Header Type Register (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:17, F:0] + Ch

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved0 | MULFNDEV | HEADERTYPE | LATTIMER | CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**Multifunction Device (MULFNDEV):** This bit is always 0 for non-fabric ports. For fabric ports it is driven from the fabric_mult_function strap. A value of 1 indicates a multifunction device; a value of 0 indicates a single function device.
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Doesnt apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesnt apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

16.5.5 Base Address Register (BAR)—Offset 10h

Each AHB device is a single function device with only a single BAR associated with it. Bits 31:4 indicate the Base Address register. Power-up software can determine how much address space the AHB Device requires by writing a value of all 1's to the register and then reading the value back. Bridge will return 0's in all don't-care address bits, effectively specifying the address space required. Unimplemented Base Address registers are hardwired to zero. This is the Size Indicator Read only bits of the register.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

BASEADDR | SIZEINDICATOR | PREFETCHABLE | TYPE | MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1s.

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RO	**Size Indicator (Read Only) (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0s.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this bar is not prefetchable.
2:1	0h RO	**Type (TYPE):** '00' indicates that the BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0 Indicates that this BAR is present in the memory space.

16.5.6 Base Address Register 1 (BAR1)—Offset 14h

Memory accesses to BAR1 region access the PCI configuration space for the LPIO device. BAR1 region is always 4K. However SW accesses through BAR1 should only access the regular PCI configuration space. BAR1 memory accesses which do not access a defined PCI configuration register are treated as accesses to a reserved register.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 14h

Default: 00000000h

Bits	31:12	11:4	3	2:1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0
Field	BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register1 (BASEADDR1):** This field is present if BAR1 is enabled through private config space. If this register is disabled then this is RO and always returns 0.
11:4	00h RO	**Size Indicator1 (SIZEINDICATOR1):** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this bar is not prefetchable.
2:1	0h RO	**Type (TYPE1):** '00' indicates that the BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0 Indicates that this BAR is present in the memory space.

16.5.7 Subsystem Vendor ID and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SUBSYSTEMID (bits 31:16) | SUBSYSTEMVENDORID (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. Th is register makes it possible for the operating environment to distinguish one audio subsystem from the other. This is a Read Write Once register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. This register enables the operating environment to distinguish one subsystem from the other. This is a Read Write Once register.

16.5.8 Expansion ROM Base Address Register (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion ROM Base Address (EXPANSION_ROM_BASE):** Value of all 0s indicates no support for Expansion ROM.

16.5.9 Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:17, F:0] + 34h

Default: 00000080h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
Reserved0						CAPPTR_POWER	

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. When PM capability is disabled, this register is 00h.

16.5.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:17, F:0] + 3Ch

Default: 00000100h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0
MAX_LAT		MIN_GNT		Reserved0	INTPIN	INTLINE	

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates that the device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates that the device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

16.5.11 Power Management Capability ID Register (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 80h

Default: 48030001h

31			28				24				20				16				12				8				4				0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PMESUPPORT					Reserved0								VERSION			NXTCAP								POWER_CAP							

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot. bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

16.5.12 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Reserved0																PMESTATUS	Reserved1						PMEENABLE	Reserved2				NO_SOFT_RESET	Reserved3	POWERSTATE	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit in this register.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for upstream decode on fabric ports.

16.5.13 General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + A0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GEN_REG_RW1

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** capabilities over-ride for the sd/sdio/emmc host controler (bits 31:0)

16.5.14 General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + A4h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

CAP_REG_SEL GEN_REG_RW2

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CAP_REG_SEL:** select if the capabilty will come from the GEN PCI register or from a hard wire
30:0	0h RW	**GEN_REG_RW2:** capabilities over-ride for the sd/sdio/emmc host controler (bits 62:32)

16.5.15 General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + A8h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

GEN_REG_RW3

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** Reserved.

16.5.16 General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + ACh

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

GEN_REG_RW4

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** Reserved.

16.5.17 General Purpose Input Register (GEN_INPUT_REGRW)—Offset C0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + C0h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

GEN_REG_INPUT_RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** Reserved.

16.5.18 Manufacturers ID Register (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + F8h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

16.6 SDIO for Wifi Memory Mapped IO Registers

Table 185. Summary of SDIO for Wifi Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SDMA System Address / Argument 2 Register (SYS_ADR)—Offset 0h" on page 1772	00000000h
4–5h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1773	0000h
6–7h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1774	0000h
8–Bh	4	"Argument 1 Register (ARGUMENT)—Offset 8h" on page 1775	00000000h
C–Dh	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1775	0000h
E–Fh	2	"Command Register (CMD)—Offset Eh" on page 1777	0000h
10–13h	4	"Response Register 0 (RESPONSE0)—Offset 10h" on page 1778	00000000h
14–17h	4	"Response Register 2 (RESPONSE2)—Offset 14h" on page 1779	00000000h
18–1Bh	4	"Response Register 4 (RESPONSE4)—Offset 18h" on page 1779	00000000h
1C–1Fh	4	"Response Register 6 (RESPONSE6)—Offset 1Ch" on page 1780	00000000h
20–23h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1780	00000000h
24–27h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1781	1FFF0000h
28–28h	1	"Host Control 1 Register (HOST_CTL)—Offset 28h" on page 1784	00h
29–29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1785	00h
2A–2Ah	1	"Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah" on page 1786	00h
2B–2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1787	00h
2C–2Dh	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1788	0000h
2E–2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1790	00h
2F–2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1791	00h
30–31h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1792	0000h
32–33h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1795	0000h
34–35h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1797	0000h
36–37h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1799	0000h
38–39h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1800	0000h
3A–3Bh	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1801	0000h
3C–3Fh	4	"Auto CMD12 Error Status Register and Host Control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1803	00000000h
40–43h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1804	00000000h
44–47h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1805	00000000h
48–4Bh	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1805	00000000h
50–51h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1806	0000h

Table 185. Summary of SDIO for Wifi Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
52–53h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1807	0000h
54–54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1808	00h
58–5Bh	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1809	00000000h
70–73h	4	"Boot Timeout Control (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1810	00000000h
74–74h	1	"Debug Selection Register (DEBUG_SEL)—Offset 74h" on page 1811	00h
E0–E3h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1811	00000000h
F0–F0h	1	"SPI Interrupt Support Register (SPI_INT_SUP)—Offset F0h" on page 1813	00h
FC–FDh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1813	0000h
FE–FFh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1814	B502h

16.6.1 SDMA System Address / Argument 2 Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

sys_adr

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SDMA System Address (sys_adr): (1) SDMA System Address** This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at each boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates a DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the uppermost byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. **(2) Argument 2** This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without AMDA, the available block count value is limited by the Block Count register. 65535 blocks is the maximum value in this case.

16.6.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
tx_blk_size_12	boundary			tr_blk_size											

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW	**TX_BLK_SIZE_12 (tx_blk_size_12):** Transfer Block Size 12th bit. This bit is added to support 4Kb Data block transfer.

Bit Range	Default & Access	Field Name (ID): Description
14:12	000b RW	**Host SDMA Buffer Boundary (boundary):** The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at each boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. • 000b = 4K bytes (Detects A11 carry out) • 001b = 8K bytes (Detects A12 carry out) • 010b = 16K Bytes (Detects A13 carry out) • 011b = 32K Bytes (Detects A14 carry out) • 100b = 64K bytes (Detects A15 carry out) • 101b = 128K Bytes (Detects A16 carry out) • 110b = 256K Bytes (Detects A17 carry out) • 111b = 512K Bytes (Detects A18 carry out)
11:0	000h RW	**Transfer Block Size (tr_blk_size):** This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2 *Determining Buffer Block Length*). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. • 0800h = 2048 Bytes • . . . • 0200h = 512 Bytes • 01FFh = 511 Bytes • . . . • 0004h = 4 Bytes • 0003h = 3 Bytes • 0002h = 2 Bytes • 0001h = 1 Byte • 0000h = No data transfer

16.6.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

blk_count

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Blocks Count For Current Transfer (blk_count):** This register is enabled when Block Count Enable in the Transfer Mode register is set to 1, and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1 and the maximum block count. The HC decrements the block count after each block transfer, and stops when the count reaches zero. Setting the block count to 0 results in no data blocks being transferred. This register should be accessed only when no transaction is executing (i.e., after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. When saving transfer context as a result of a Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the HD shall restore the previously saved block count. • 0000h = Stop Count • 0001h = 1 block • 0002h = 2 blocks • . . . • FFFFh = 65535 blocks

16.6.4 Argument 1 Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

argument

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command Argument 1 (argument):** The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

16.6.5 Transfer Mode Register (TX_MODE)—Offset Ch

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data (Refer to Data Present Select in the Command register), or before issuing a Resume command. The Host Driver shall save the value of this register when the data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller shall implement write protection for this register during data transactions. Writes to this register shall be ignored when the Command Inhibit (DAT) in the Present State register is 1.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd							boot_en	spi_mode	cmd_comp_ata	blk_sel	data_tr_dir	auto_cmd_en		blk_count_en	dma_en

Bit Range	Default & Access	Field Name (ID): Description
15:9	00h RO	**Reserved (rsvd):** Reserved.
8	0b RW	**BOOT_EN (boot_en):** To start boot operation for MMC4.3 1 - To start boot mode 0 - Stop the boot read
7	0b RW	**SPI_MODE (spi_mode):** SPI mode enable bit. 1 - SPI mode 0 - SD mode
6	0b RW	**CMD_COMP_ATA (cmd_comp_ata):** Command Completion Signal Enable for CE-ATA Device. ???1??? - Device will send command completion Signal ???0??? - Device will not send command completion Signal
5	0b RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0b RW	**Data Transfer Direction Select (data_tr_dir):** This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller, and it is set to 0 for all other commands. • 1 = Read (Card to Host) • 0 = Write (Host to Card)
3:2	0b RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0b RW	**Block Count Enable (blk_count_en):** This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8). If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. • 1 = Enable • 0 = Disable
0	0b RW	**DMA Enable (dma_en):** This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). • 1 = DMA Data transfer • 0 = No data transfer or Non DMA data transfer

16.6.6 Command Register (CMD)—Offset Eh

The Host Driver shall check the Command Inhibit (DAT) bit and Command Inhibit (CMD) bit in the Present State register before writing to this register. Writing to the upper byte of this register triggers SD command generation. The Host Driver has the responsibility to write this register because the Host Controller does not protect for writing when Command Inhibit (CMD) is set.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd		cmd_index						cmd_type		data_pr_sel	cmd_index_chk_en	cmd_crc_chk_en	reserved	resp_type_sel	

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Rsvd (rsvd):** Reserved.
13:8	0h RW	**Command Index (cmd_index):** These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	00b RW	**Command Type (cmd_type):** There are three types of special commands: Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. **(1) Suspend Command** If the Suspend command succeeds, the Host Controller shall assume the SD Bus has been released and that it is possible to issue the next command, which uses the DAT line. The Host Controller shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the Host Controller shall maintain its current state, and the Host Driver shall restart the transfer by setting Continue Request in the Block Gap Control register. (Refer to 3.12.1 Suspend Sequence). **(2) Resume Command** The Host Driver re-starts the data transfer by restoring the registers in the range of 000-00Dh. (Refer to Figure 1-4 in section 1.6 for the register map.) The Host Controller shall check for busy before starting write transfers. **(3) Abort Command** If this command is set when executing a read transfer, the Host Controller shall stop reads to the buffer. If this command is set when executing a write transfer, the Host Controller shall stop driving the DAT line. After issuing the Abort command, the Host Driver should issue a software reset. (Refer to 3.8 Abort Transaction). • 11b = Abort -- CMD12, CMD52 for writing 'I/O Abort' in CCCR • 10b = Resume -- CMD52 for writing 'Function Select' in CCCR • 01b = Suspend -- CMD52 for writing 'Bus Suspend' in CCCR • 00b = Normal -- Other commands
5	0b RW	**Data Present Select (data_pr_sel):** This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38). (3) Resume command. • 1 = Data Present • 0 = No Data Present

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**Command Index Check Enable (cmd_index_chk_en):** If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. • 1 = Enable • 0 = Disable
3	0b RW	**Command CRC Check Enable (cmd_crc_chk_en):** If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) • 1 = Enable • 0 = Disable
2	0b RO	**Reserved (reserved):** Reserved.
1:0	0h RW	**Response Type Select (resp_type_sel):** • 00 = No Response • 01 = Response Length 136 • 10 = Response Length 48 • 11 = Response Length 48 check Busy after response

16.6.7 Response Register 0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.6.8 Response Register 2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.6.9 Response Register 4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.6.10 Response Register 6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.6.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

buf_data

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Buffer Data (buf_data):** The Host Controller buffer can be accessed through this 32-bit Data Port register. Refer to section 1.7.

16.6.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 1FFF0000h

Bits	Default	Field
31:29	0 0 0	reserved2
28:25	1 1 1 1	dat_sig_lvl
24	1	cmd_ln_sig_lvl
23:20	1 1 1 1	data_ln_sig_lvl
19	1	wr_prot_sw_pin_lvl
18	1	crd_det_pin_lvl
17	1	crd_st_stable
16	1	crd_ins
15:12	0 0 0 0	reserved1
11	0	buf_rd_en
10	0	buf_wr_en
9	0	rd_tx_active
8	0	wr_tx_active
7:3	0 0 0 0 0	reserved
2	0	dat_ln_active
1	0	cmd_inhibit_dat
0	0	cmd_inhibit_cmd

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (reserved2):** Reserved.
28:25	1111b RO	**DAT Line Signal Level (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. • D28 - DAT[7] • D27 - DAT[6] • D26 - DAT[5] • D25 - DAT[4]
24	1b RO	**CMD Line Signal Level (cmd_ln_sig_lvl):** This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	Fh RO	**DAT[3:0] Line Signal Level (data_ln_sig_lvl):** This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. • D23 = DAT[3] • D22 = DAT[2] • D21 = DAT[1] • D20 = DAT[0]
19	1b RO	**Write Protect Switch Pin Level (wr_prot_sw_pin_lvl):** The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP# pin. • 1 = Write enabled (SDWP#=1) • 0 = Write protected (SDWP#=0)
18	1b RO	**Card Detect Pin Level (crd_det_pin_lvl):** This bit reflects the inverse value of the SDCD# pin. Debouncing is not performed on this bit. This bit may be valid when Card State Stable is set to 1, but it is not guaranteed because of propagation delay. Use of this bit is limited to testing since it must be debounced by software. • 1 = Card present (SDCD#=0) • 0 = No card present (SDCD#=1)
17	1b RO	**Card State Stable (crd_st_stable):** This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. No Card state can be detected by this bit being set to 1 while Card Inserted is set to 0. The Software Reset For All in the Software Reset register shall not affect this bit. • 1 = No Card or Inserted • 0 = Reset or Debouncing

Bit Range	Default & Access	Field Name (ID): Description
16	1b RO	**Card Inserted (crd_ins):** This bit indicates whether a card has been inserted. The Host Controller shall debounce this signal so that the Host Driver will not need to wait for it to stabilize. Changing from 0 to 1 generates a Card Insertion interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register shall not affect this bit. If a card is removed while its power is on and its clock is oscillating, the Host Controller shall clear SD Bus Power in the Power Control register (Refer to Section 2.2.11) and SD Clock Enable in the Clock Control register (Refer to Section 2.2.14). When this bit is changed from 1 to 0, the Host Controller shall immediately stop driving CMD and DAT[3:0] (tri-state). In addition, the Host Driver should clear the Host Controller by the Software Reset For All in Software Reset register. The card detect is active regardless of the SD Bus Power. • 1 = Card Inserted • 0 = Reset or Debouncing or No Card
15:12	0h RO	**Reserved1 (reserved1):** Reserved.
11	0b RO	**Buffer Read Enable (buf_rd_en):** This status is used for non-DMA read transfers. The Host Controller may implement multiple buffers to transfer data efficiently. This read only flag indicates that valid data exists in the host side buffer. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when block data is ready in the buffer and generates the Buffer Read Ready interrupt. • 1 = Read enable • 0 = Read disable
10	0b RO	**Buffer Write Enable (buf_wr_en):** This status is used for non-DMA write transfers. The Host Controller can implement multiple buffers to transfer data efficiently. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready interrupt. The Host Controller should neither set Buffer Write Enable nor generate Buffer Write Ready Interrupt after the last block data is written to the Buffer Data Port Register. • 1 = Write enable • 0 = Write disable
9	0b RO	**Read Transfer Active (rd_tx_active):** This status is used for detecting completion of a read transfer. Refer to Section 3.12.3 for sequence details. This bit is set to 1 for either of the following conditions: • After the end bit of the read command. • When read operation is restarted by writing a 1 to Continue Request in the Block Gap Control register. This bit is cleared to 0 for either of the following conditions: • When the last data block as specified by block length is transferred to the System. • In case of ADMA2, end of read operation is designated by Descriptor Table. • When all valid data blocks in the Host Controller have been transferred to the System and no current block transfers are being sent as a result of the Stop At Block Gap Request being set to 1. A Transfer Complete interrupt is generated when this bit changes to 0. • 1 = Transferring data • 0 = No valid data

Bit Range	Default & Access	Field Name (ID): Description
8	0b RO	**Write Transfer Active (wr_tx_active):** This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the Host Controller. Refer to Section 3.12.4 for more details on the sequence of events. This bit is set in either of the following cases: • After the end bit of the write command. • When write operation is restarted by writing a 1 to Continue Request in the Block Gap Control register. This bit is cleared in either of the following cases: • After getting the CRC status of the last data block as specified by the transfer count (Single and Multiple) In case of ADMA2, transfer count is designated by Descriptor Table. • After getting the CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as the result of the Stop At Block Gap Request being set. This status is useful for the Host Driver in determining non DAT line commands can be issued during write busy. • 1 Transferring data • 0 No valid data
7:3	00h RO	**Reserved (reserved):** Reserved.
2	0b RO	**DAT Line Active (dat_ln_active):** This bit indicates whether one of the DAT lines on SD Bus is in use. (a) In the case of read transactions This status indicates whether a read transfer is executing on the SD Bus. Changing this value from 1 to 0 generates a Block Gap Event interrupt in the Normal Interrupt Status register, as the result of the Stop At Block Gap Request being set. Refer to Section 3.12.3 for details on timing. This bit shall be set in either of the following cases: • After the end bit of the read command. • When writing a 1 to Continue Request in the Block Gap Control register to restart a read transfer. This bit shall be cleared in either of the following cases: • When the end bit of the last data block is sent from the SD Bus to the Host Controller. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table. • When a read transfer is stopped at the block gap initiated by a Stop At Block Gap Request. The Host Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Host Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use suspend / resume function. (b) In the case of write transactions This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. Refer to Section 3.12.4 for sequence details. This bit shall be set in either of the following cases: • After the end bit of the write command. • When writing to 1 to Continue Request in the Block Gap Control register to continue a write transfer. This bit shall be cleared in either of the following cases: • When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive 'Not Busy'. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table. • When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request. (c) Command with busy This status indicates whether a command indicates busy (ex. erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command with busy and cleared when busy is de-asserted. Changing this bit from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. Refer Figure 2-11 to Figure 2-13. • 1 = DAT Line Active • 0 = DAT Line Inactive

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Command Inhibit (DAT) (cmd_inhibit_dat):** This status bit is generated if either the DAT Line Active or the Read Transfer Active is set to 1. If this bit is 0, it indicates the Host Controller can issue the next SD Command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal Interrupt Status register. **Note:** The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. • 1 Cannot issue command which uses the DAT line • 0 Can issue command which uses the DAT line
0	0b RO	**Command Inhibit (CMD) (cmd_inhibit_cmd):** Command Inhibit (CMD) If this bit is 0, it indicates the CMD line is not in use and the Host Controller can issue a SD Command using the CMD line. cleared when the command response is received. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register. Even if the Command Inhibit (DAT) is set to 1, commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command Complete Interrupt in the Normal Interrupt Status register. If the Host Controller cannot issue the command because of a command conflict error (Refer to Command CRC Error in Section 2.2.18) or because of Command Not Issued By Auto CMD12 Error (Refer to Section 2.2.23), this bit shall remain 1 and the Command Complete is not set. • 1 Cannot issue command • 0 Can issue command using only CMD line

16.6.13 Host Control 1 Register (HOST_CTL)—Offset 28h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
crd_det_sig_sel	crd_det_tst_lvl	sd8_bit_mode	dma_sel		hi_spd_en	data_tx_wid	led_ctl

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**Card Detect Signal Selection (crd_det_sig_sel):** This bit selects source for the card detection. • 1 = The Card Detect Test Level is selected (for test purposes) • 0 = SDCD# is selected (for normal use) When the source for the card detection is switched, the interrupt should be disabled during the switching period by clearing the Interrupt Status/Signal Enable register in order to mask unexpected interrupt being caused by the glitch. The Interrupt Status/Signal Enable should be disabled during the period of debouncing.

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**Card Detect Test Level (crd_det_tst_lvl):** This bit is enabled while the Card Detect Signal Selection is set to 1, and it indicates whether or not the card is inserted. • 1 = Card Inserted • 0 = No Card
5	0b RW	**SD8 Bit Mode (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	00b RW	**DMA Select (dma_sel):** One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. Use of selected DMA is determined by DMA Enable of the Transfer Mode register. • 00 = SDMA is selected • 01 = Reserved (New assignment is not allowed) • 10 = 32-bit Address ADMA2 is selected • 11 = Reserved (will be modified by Version 4.00)
2	0b RW	**High Speed Enable (hi_spd_en):** This bit is optional. Before setting this bit, the Host Driver shall check the High Speed Support in the Capabilities register. If this bit is set to 0 (default), the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock (up to 25MHz). If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock (up to 50MHz). If Preset Value Enable in the Host Control 2 register is set to 1, Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. • 1 = 4-bit mode • 0 = 1-bit mode
1	0b RW	**Data Transfer Width (data_tx_wid):** Reserved.
0	0b RW	**LED Control (led_ctl):** This bit selects the data width of the Host Controller. The Host Driver shall set it to match the data width of the SD card. • 1 = 4-bit mode • 0 = 1-bit mode

16.6.14 Power Control Register (PWR_CTL)—Offset 29h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd			hw_rst	sd_bus_volt_sel			sd_bus_pwr

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Rsvd (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**HW Reset (hw_rst):** Reserved.
3:1	0h RW	**SD Bus Voltage Select (sd_bus_volt_sel):** By setting these bits, the Host Driver selects the voltage level for the SD card. Before setting this register, the Host Driver shall check the Voltage Support bits in the Capabilities register. If an unsupported voltage is selected, the Host System shall not supply SD Bus voltage. • 111b = 3.3V (Typ.) • 110b = 3.0V (Typ.) • 101b = 1.8V (Typ.) • 100b 000b Reserved
0	0b RW	**SD Bus Power (sd_bus_pwr):** Before setting this bit, the SD Host Driver shall set SD Bus Voltage Select. If the Host Controller detects the No Card state, this bit shall be cleared. If this bit is cleared, the Host Controller shall immediately stop driving CMD and DAT[3:0] (tri-state) and drive SDCLK to low level (Refer to Section 2.2.14) For SD Controller, this bit controls the bus voltage to SDMMC3. For SDIO Controller, power to SDIO device on SDMMC2 is not controlled by this bit. GPIO register and pin can be used to controller the SDIO device power. For eMMC Controller, power to eMMC device on SDMMC1 is not controlled by this bit. GPIO register and pin or alternative solutions can be used. • 1 = Power on • 0 = Power off

16.6.15 Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd			drive_ccsd	int_blk_gap	rd_wait_ctl	cont_req	stp_blk_gap_req

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (rsvd):** Reserved.
4	0b RW	**DRIVE_CCSD (drive_ccsd):** If the driver set this bit (change from ???0??? to ???1???), Host controller will send command completion.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**Interrupt at Block Gap (int_blk_gap):** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. • 1 = Enabled • 0 = Disabled
2	0b RW	**Read Wait Control (rd_wait_ctl):** The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the DAT[2] line. Otherwise, the Host Controller has to stop the SD Clock to hold read data, which restricts commands generation. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1, otherwise DAT line conflict may occur. If this bit is set to 0, Suspend/Resume cannot be supported. • 1 = Enable Read Wait Control • 0 = Disable Read Wait Control
1	0b RW	**Continue Request (cont_req):** This bit is used to restart a transaction, which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At Block Gap Request to 0 and set this bit 1 to restart the transfer. The Host Controller automatically clears this bit in either of the following cases: • In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. • In the case of a write transaction, the Write Transfer Active changes from 0 to 1 as the write transaction restarts. Therefore, it is not necessary for Host Driver to set this bit to 0. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. • 1 = Restart • 0 = Not affect
0	0b RW	**Stop at Block Gap Request (stp_blk_gap_req):** This bit is used to stop executing read and write transaction at the next block gap for non-DMA, SDMA and ADMA transfers. The Host Driver shall leave this bit set Copyright 2002-2011 SD Association SD Host Controller Simplified Specification Version 3.00 44 to 1 until the Transfer Complete is set to 1. Clearing both Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. When Host Controller version is 1.00, the Host Driver can set this bit if the card supports Read Wait Control. When Host Controller version is 2.00 or later, the Host Driver can set this bit regardless of the card supports Read Wait Control. The Host Controller shall stop read transfer by using Read Wait or stopping SD clock. In case of write transfers in which the Host Driver writes data to the Buffer Data Port register, the Host Driver shall set this bit after all block data is written. If this bit is set to 1, the Host Driver shall not write data to Buffer Data Port register. This bit affects Read Transfer Active, Write Transfer Active, DAT Line Active and Command Inhibit (DAT) in the Present State register. Regarding detailed control of bits D01 and D00, refer to Section 3.8 and 3.12. • 1 = Stop • 0 = Transfer

16.6.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is mandatory for the Host Controller, but wakeup functionality depends on the Host Controller system hardware and software. The Host Driver shall maintain voltage on the SD Bus, by setting SD Bus Power to 1 in the Power Control register, when wakeup event via Card Interrupt is desired. Wakeup Event is not supported by Host Controller. Sideband wake via GPIO pin and register shall be used instead. During RTD3, GPIO register is readable and GPIO signal is routed to APIC.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					wakeup_en_sd_rm	wakeup_en_sd_ins	wakeup_en_crd_int

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.
2	0b RW	**Wakeup Event Enable On SD Card Removal (wakeup_en_sd_rm):** This bit enables wakeup event via Card Removal assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. • 1 = Enable • 0 = Disable
1	0b RW	**Wakeup Event Enable On SD Card Insertion (wakeup_en_sd_ins):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. • 1 = Enable • 0 = Disable
0	0b RW	**Wakeup Event Enable On Card Interrupt (wakeup_en_crd_int):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. • 1 = Enable • 0 = Disable

16.6.17 Clock Control Register (CLK_CTL)—Offset 2Ch

At the initialization of the Host Controller, the Host Driver shall set the SDCLK Frequency Select according to the Capabilities register.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sdclk_freq_sel								upper_sdclk_freq_sel		rsvd			sd_clk_en	int_clk_stable	int_clk_en

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**SDCLK Frequency Select (sdclk_freq_sel):** This register is used to select the frequency of the SDCLK pin. The definition of this field is dependent on the Host Controller Version. **(1) 8-bit Divided Clock Mode** This mode is supported by the Host Controller Version 1.00 and 2.00. The frequency is not programmed directly, rather, this register holds the divisor of the Base Clock Frequency For SD Clock in the capabilities register. Only the following settings are allowed. **(1) 8-bit Divided Clock Mode** • 80h = base clock divided by 256 • 40h = base clock divided by 128 • 20h = base clock divided by 64 • 10h = base clock divided by 32 • 08h = base clock divided by 16 • 04h = base clock divided by 8 • 02h = base clock divided by 4 • 01h = base clock divided by 2 • 00h = base clock(10MHz and up) Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor, but it should not be set. The three default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register. • 400KHz divider value • 25MHz divider value • 50MHz divider value According to the Physical Layer Specification, the maximum SD Clock frequency is 25 MHz in normal speed mode and 50MHz in high speed mode, and shall never exceed this limit. The frequency of the SDCLK is set by the following formula: Clock Frequency = (Base Clock) / divisor Thus, choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. For example, if the Base Clock Frequency For SD Clock in the Capabilities register has the value 33MHz, and the target frequency is 25MHz, then choosing the divisor value of 01h will yield 16.5MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400KHz, the divisor value of 40h yields the optimal clock value of 258KHz. **(2) 10-bit Divided Clock Mode** Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits, and all divider values shall be supported. • 3FFh = 1/2046 Divided Clock • N = 1/2N Divided Clock (Duty 50%) • 002h = 1/4 Divided Clock • 001h = 1/2 Divided Clock • 000h = Base Clock (10MHz and up) • 3FFh = Base Clock * M / 1024 • .... • N - 1 = Base Clock * M / N • .... • 002h = Base Clock * M / 3 • 001h = Base Clock * M / 2 • 000h = Base Clock * M This field depends on setting of Preset Value Enable in the Host Control 2 register. If Preset Value Enable = 0, this field is set by Host Driver. If the Preset Value Enable = 1, this field is automatically set to a value specified in one of Preset Value registers.

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Upper Bits of SDCLK Frequency Select (upper_sdclk_freq_sel):** Host Controller Versions 1.00 and 2.00 do not support these bits and they are treated as 00b fixed value (ROC). Host Controller Version 3.00 shall support these bits to expand SDCLK Frequency Select to 10-bit. Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select.
5:3	0h RO	**Rsvd (rsvd):** Reserved.
2	0b RW	**SD Clock Enable (sd_clk_en):** The Host Controller shall stop SDCLK when writing this bit to 0. SDCLK Frequency Select can be changed when this bit is 0. Then, the Host Controller shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK=0). If the Card Inserted in the Present State register is cleared, this bit shall be cleared. • 1 = Enable • 0 = Disable
1	0b RO	**Internal Clock Stable (int_clk_stable):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. **Note:** This is useful when using PLL for a clock oscillator that requires setup time. • 1 = Ready • 0 = Not Ready
0	0b RW	**Internal Clock Enable (int_clk_en):** This bit is set to 0 when the Host Driver is not using the Host Controller, or when the Host Controller awaits a wakeup event. The Host Controller should stop its internal clock to go to a very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the Host Controller shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection. • 1 = Oscillate • 0 = Stop

16.6.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

At the initialization of the Host Controller, the Host Driver shall set the Data Timeout Counter Value according to the Capabilities register.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
reserved				data_timeout_cnt_val			

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Rsvd (reserved):** Reserved.
3:0	0h RW	**Data Timeout Counter Value (data_timeout_cnt_val):** This value determines the interval by which DAT line timeouts are detected. For more information about timeout generation, refer to the Data Timeout Error in the Error Interrupt Status register. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). • 1111b Reserved • 1110b = TMCLK x 2^27 • .... • 0001b = TMCLK x 2^14 • 0000b = TMCLK x 2^13

16.6.19 Software Reset Register (SW_RST)—Offset 2Fh

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					sw_rst_dat_ln	sw_rst_cmd_ln	sw_rst_all

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**Software Reset For DAT Line (sw_rst_dat_ln):** Only part of data circuit is reset. DMA circuit is also reset. The following registers and bits are cleared by this bit: Buffer Data Port register • Buffer is cleared and initialized. Present State register • Buffer Read Enable • Buffer Write Enable • Read Transfer Active • Write Transfer Active • DAT Line Active • Command Inhibit (DAT) Block Gap Control register • Continue Request • Stop At Block Gap Request Normal Interrupt Status register • Buffer Read Ready • Buffer Write Ready • DMA Interrupt • Block Gap Event • Transfer Complete • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.
1	0b RW	**Software Reset For CMD Line (sw_rst_cmd_ln):** Only part of command circuit is reset. The following registers and bits are cleared by this bit: Present State register • Command Inhibit (CMD) Normal Interrupt Status register • Command Complete • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.
0	0b RW	**Software Reset For All (sw_rst_all):** This reset affects the entire Host Controller except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the Host Driver shall set this bit to 1 to reset the Host Controller. The Host Controller shall reset this bit to 0 when Capabilities registers are valid and the Host Driver can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the host driver should issue reset command and reinitialize the SD card. • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.

16.6.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

The Normal Interrupt Status Enable affects reads of this register, but Normal Interrupt Signal Enable does not affect these reads. An interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1. Writing 1 to a bit of RW1C attribute clears it; writing 0 keeps the bit unchanged. Writing 1 to a bit of ROC attribute keeps the bit unchanged. More than one status can be cleared with a single register write. The Card Interrupt is cleared when the card stops asserting the interrupt; that is, when the Card Driver services the interrupt condition.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
err_int	boot_ter_int	boot_ck_rcv	re_tune	int_c	int_b	int_a	crd_int	crd_rm	crd_ins	buf_rd_rdy	buf_wr_rdy	dma_int	blk_gap_event	tx_comp	cmd_comp

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Error Interrupt (err_int):** If any of the bits in the Error Interrupt Status register are set, then this bit is set. Therefore the Host Driver can efficiently test for an error by checking this bit first. This bit is read only. • 1 = Error • 0 = No Error
14	0b RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0b RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0b RO	**Re-Tuning Event (re_tune):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. • 1 Re-Tuning should be performed • 0 Re-Tuning is not required
11	0b RO	**INT_C (int_c):** This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_C is detected • 0 = No interrupt is detected
10	0b RO	**INT_B (int_b):** This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_B is detected • 0 = No interrupt is detected
9	0b RO	**INT_A (int_a):** This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_A is detected • 0 = No interrupt is detected

Bit Range	Default & Access	Field Name (ID): Description
8	0b RO	**Card Interrupt (crd_int):** Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. When this status has been set and the Host Driver needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status Enable register may be set to 0 in order to clear the card interrupt statuses latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (It should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of shared bus, interrupt pins are used to detect interrupts. If 000b is set to Interrupt Pin Select in the Shared Bus Control register, this status is effective. Non-zero value is set to Interrupt Pin Select, INT_A, INT_B or INT_C is then used to device interrupts. • 1 = Generate Card Interrupt • 0 = No Card Interrupt
7	0b RW/1C	**Card Removal (crd_rm):** This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed. Because the card detect state may possibly be changed when the Host Driver clear this bit and interrupt event may not be generated. • 1 = Card removed • 0 = Card state stable or Debouncing
6	0b RW/1C	**Card Insertion (crd_ins):** This status is set if the Card Inserted in the Present State register changes from 0 to 1. When the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed, because the card detect state may possibly be changed when the Host Driver clears this bit and interrupt event may not be generated. • 1 Card inserted • 0 Card state stable or Debouncing
5	0b RW/1C	**Buffer Read Ready (buf_rd_rdy):** This status is set if the Buffer Read Enable changes from 0 to 1. Refer to the Buffer Read Enable in the Present State register. While performing tuning procedure (Execute Tuning is set to 1), Buffer Read Ready is set to 1 for every CMD19 execution. • 1 = Ready to read buffer • 0 = Not ready to read buffer
4	0b RW/1C	**Buffer Write Ready (buf_wr_rdy):** This status is set if the Buffer Write Enable changes from 0 to 1. Refer to the Buffer Write Enable in the Present State register. • 1 = Ready to write buffer • 0 = Not ready to write buffer
3	0b RW/1C	**DMA Interrupt (dma_int):** This status is set if the Host Controller detects the Host SDMA Buffer boundary during transfer. Refer to the Host SDMA Buffer Boundary in the Block Size register. Other DMA interrupt factors may be added in the future. In case of ADMA, by setting Int field in the descriptor table, Host Controller generates this interrupt. Suppose that it is used for debugging. This interrupt shall not be generated after the Transfer Complete. • 1 = DMA Interrupt is generated • 0 = No DMA Interrupt
2	0b RW/1C	**Block Gap Event (blk_gap_event):** If the Stop At Block Gap Request in the Block Gap Control register is set, this bit is set when both a read / write transaction is stopped at a block gap. If Stop At Block Gap Request is not set to 1, this bit is not set to 1. **(1) In the case of a Read Transaction** This bit is set at the falling edge of the DAT Line Active Status, when the transaction is stopped at SD Bus timing. The Read Wait shall be supported in order to use this function. Refer to Section 3.12.3 for timing details. p]**(1) In the case of a Write Transaction** This bit is set at the falling edge of Write Transfer Active Status (after getting CRC status at SD Bus timing). Refer to Section 3.12.4 for more details on the sequence of events. • 1 = Transaction stopped at block gap • 0 = No Block Gap Event

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW/1C	**Transfer Complete (tx_comp):** This bit is set when a read / write transfer and a command with busy is completed. **(1) In the case of a Read Transaction** This bit is set at the falling edge of Read Transfer Active Status. This interrupt is generated in two cases. The first is when a data transfer is completed as specified by data length (After the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the Stop At Block Gap Request in the Block Gap Control register (After valid data has been read to the Host System). Refer to Section 3.12.3 for more details on the sequence of events. **(2) In the case of a Write Transaction** This bit is set at the falling edge of the DAT Line Active Status. This interrupt is generated in two cases. The first is when the last data is written to the SD card as specified by data length and the busy signal released. The second is when data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control register and data transfers completed. (After valid data is written to the SD card and the busy signal released). Refer to Section 3.12.4 for more details on the sequence of events. **(3) In the case of a command with busy** This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit (DAT) in the Present State register. Refer to the spec for the relationship between Transfer Complete and Data Timeout Error. • 1 = Command execution is completed • 0 = Not complete While performing tuning procedure (Execute Tuning is set to 1), Transfer Complete is not set to 1.
0	0b RW/1C	**Command Complete (cmd_comp):** This bit is set when get the end bit of the command response. Auto CMD12 and Auto CMD23 consist of two responses. Command Complete is not generated by the response of CMD12 or CMD23 but generated by the response of a read/write command. Refer to Command Inhibit (CMD) in the Present State register for how to control this bit. Command Timeout Error has higher priority than Command Complete. If both bits are set to 1, it can be considered that the response was not received correctly. For a tabular description of the relationship between these two bits, refer to the description of Command Complete in the spec. • 1 = Command complete • 0 = No command complete

16.6.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Signals defined in this register can be enabled by the Error Interrupt Status Enable register, but not by the Error Interrupt Signal Enable register. The interrupt is generated when the Error Interrupt Signal Enable is enabled and at least one of the statuses is set to 1. Writing to 1 clears the bit, and writing to 0 keeps the bit unchanged. More than one status can be cleared at the one register write.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
vend_spec_err_status	boot_cmd_timeout_err	ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_index_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW	**Vendor Specific Error Status (vend_spec_err_status):** Reserved.
14	0b RW	**Boot Command Timeout Error (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0b RW	**CEATA Error (ceata_err):** Occurs when ATA command termination has occured due to an error condition the device has encountered.
12	0b RW	**Target Response Error (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction).
11:10	0h RO	**Reserved (rsvd):** Reserved.
9	0b RW	**ADMA Error (adma_err):** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. In addition, the Host Controller generates this Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. **ADMA Error State** in the ADMA Error Status indicates that an error occurs in ST_FDS state.The Host Driver may find that Valid bit is not set at the error descriptor. • 0 = error • 1 = no error
8	0b RW	**Auto CMD12 Error (cmd12_err):** Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. • 1 = error • 0 = no error
7	0b RW	**Current Limit Error (cur_limit_err):** By setting the **SD Bus Power** bit in the Power Control register, the Host Controller is requested to supply power for the SD Bus. If the Host Controller supports the Current Limit function, it can be protected from an illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the Host Controller is not supplying power to SD card due to some failure. Reading 0 means that the Host Controller is supplying power and no error has occurred. The Host Controller may require some sampling time to detect the current limit. If the Host Controller does not support this function, this bit shall always be set to 0. • 1 = power fail • 0 = no error
6	0b RW	**Data End Bit Error (data_end_bit_err):** Occurs either when detecting 0 at the end bit position of read data which uses the DAT line or at the end bit position of the CRC Status. • 1 = error • 0 = no error
5	0b RW	**Data CRC Error (data_crc_err):** Occurs when detecting CRC error when transferring read data which uses the **DAT** line or when detecting the Write CRC status having a value of other than 010b.
4	0b RW	**Data Timeout Error (data_timeout_err):** This bit is set when detecting one of following timeout conditions. • Busy timeout for R1b,R5b type • Busy timeout after Write CRC status • Write CRC Status timeout • Read Data timeout • 1 = time out • 0 = no error

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**Command Index Error (cmd_index_err):** This bit is set if a Command Index error occurs in the command response. • 1 = error • 0 = no error
2	0b RW	**Command End Bit Error (cmd_end_bit_err):** This bit is set when detecting that the end bit of a command response is 0. • 1 = End Bit Error generated • 0 = no error
1	0b RW	**Command CRC Error (cmd_crc_err): Command CRC Error** is generated in two cases. If a response is returned and the **Command Timeout Error** is set to 0(indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller shall abort the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict (refer to tabular data in the spec. that explains the relationship between **Command CRC Error** and **Command Timeout Error**). • 1 = CRC Error Generated. • 0 = no error
0	0b RW	**Command Timeout Error (cmd_timeout_err):** This bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict (in which case **Command CRC Error** shall also be set, as shown in tabular data in the spec that explains the relationship between this bit and **Command CRC Error**) this bit shall be set without waiting for 64 SD clock cycles, because the command will be aborted by the Host Controller. • 1 = time out • 0 = no Error

16.6.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Setting to 1 enables Interrupt Status. **Implementation Note:** The Host Controller may sample the card interrupt signal during interrupt period, and may hold its value in the flip-flop. If the **Card Interrupt Status Enable** is set to 0, the Host Controller shall clear all internal signals regarding Card Interrupt.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	rsvd				boot_term_int_en	boot_ack_rcv_en	crd_int_stat_en	crd_rm_stat_en	crd_ins_stat_en	buf_rd_rdy_stat_en	buf_wr_rdy_stat_en	dma_int_stat_en	blk_gap_event_stat_en	tx_comp_stat_en	cmd_comp_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Fixed to 0 (fixed_0):** The Host Driver shall control error interrupts using the Error Interrupt Status Enable register.
14:11	0h RO	**Reserved (rsvd):** Reserved.
10	0b RW	**Boot Term Interrupt Enable (boot_term_int_en):** 0 = Masked.
9	0b RW	**Boot Acknowledge Receive Enable (boot_ack_rcv_en):** 0 = Masked
8	0b RW	**Card Interrupt Status Enable (crd_int_stat_en):** If this bit is set to 0, the Host Controller shall clear interrupt request to the System. The **Card Interrupt** detection is stopped when this bit is cleared, and restarted when this bit is set to 1. The Host Driver may clear the **Card Interrupt Status Enable** before servicing the Card Interrupt, and may set this bit again after all interrupt requests from the card are cleared, to prevent inadvertent interrupts. • 1 = enabled • 0 = masked
7	0b RW	**Card Removal Status Enable (crd_rm_stat_en):** • 1 = enabled • 0 = masked
6	0b RW	**Card Insertion Status Enable (crd_ins_stat_en):** [• 1 = enabled • 0 = masked
5	0b RW	**Buffer Read Ready Status Enable (buf_rd_rdy_stat_en):** • 1 = enabled • 0 = masked
4	0b RW	**Buffer Write Ready Status Enable (buf_wr_rdy_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**DMA Interrupt Status Enable (dma_int_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Block Gap Event Status Enable (blk_gap_event_stat_en):** • 1 = enabled • 0 = masked
1	0b RW	**Transfer Complete Status Enable (tx_comp_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Complete Status Enable (cmd_comp_stat_en):** • 1 = enabled • 0 = masked

16.6.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Setting to 1 enables interrupt status. **Implementation Note:** To detect CMD line conflict, the Host Driver must set both **Command Timeout Error Status Enable** and **Command CRC Error Status Enable to 1**.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_en	tgt_rsp_err_en	rsvd	tune_err_stat_en	adma_err_stat_en	cmd12_err_stat_en	cur_limit_err_stat_en	data_end_bit_err_stat_en	data_crc_err_stat_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15:14	0b RO	**Rsvd0 (rsvd0):** Reserved.
13	0b RW	**CEATA Error Enable (ceata_err_en):** 0 = masked
12	0b RW	**Target Response Error Enable (tgt_rsp_err_en):** 0 = masked
11	0b RO	**Rsvd (rsvd):** Reserved.
10	0b RW	**Tuning Error Status Enable (tune_err_stat_en):** • 1 = enabled • 0 = masked
9	0b RW	**ADMA Error Status Enable (adma_err_stat_en):** • 1 = enabled • 0 = masked
8	0b RW	**Auto CMD12 Error Status Enable (cmd12_err_stat_en):** • 1 = enabled • 0 = masked
7	0b RW	**Current Limit Error Status Enable (cur_limit_err_stat_en):** • 1 = enabled • 0 = masked
6	0b RW	**Data End Bit Error Status Enable (data_end_bit_err_stat_en):** • 1 = enabled • 0 = masked

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**Data CRC Error Status Enable (data_crc_err_stat_en):** • 1 = enabled • 0 = masked
4	0b RW	**Data Timeout Error Status Enable (data_timeout_err_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**Command Index Error Status Enable (cmd_ind_err_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Command End Bit Error Status Enable (cmd_end_bit_err_stat_en):** • 1 = enabled • 0 = masked
1	0b RW	**Command CRC Error Status Enable (cmd_crc_err_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Timeout Error Status Enable (cmd_timeout_err_stat_en):** • 1 = enabled • 0 = masked

16.6.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

This register is used to select which interrupt status is indicated to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	rsvd				boot_term_int_sig_en	boot_ack_rcv_sig_en	crd_int_sig_en	crd_rm_sig_en	crd_ins_sig_en	buf_rd_rdy_sig_en	buf_wr_rdy_sig_en	dma_int_sig_en	blk_gap_event_sig_en	tx_comp_sig_en	cmd_comp_sig_en

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Fixed to 0 (fixed_0):** The Host Driver shall control error interrupts using the Error Interrupt Signal Enable register.
14:11	0h RO	**Reserved (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0b RW	**Boot Terminate Interrupt Signal Enable (boot_term_int_sig_en):** 0 = masked
9	0b RW	**Boot Acknowledge Receive Signal Enable (boot_ack_rcv_sig_en):** 0 = masked
8	0b RW	**Card Interrupt Signal Enable (crd_int_sig_en):** • 1 = enabled • 0 = masked
7	0b RW	**Card Removal Signal Enable (crd_rm_sig_en):** • 1 = enabled • 0 = masked
6	0b RW	**Card Insertion Signal Enable (crd_ins_sig_en):** • 1 = enabled • 0 = masked
5	0b RW	**Buffer Read Ready Signal Enable (buf_rd_rdy_sig_en):** • 1 = enabled • 0 = masked
4	0b RW	**Buffer Write Ready Signal Enable (buf_wr_rdy_sig_en):** • 1 = enabled • 0 = masked
3	0b RW	**DMA Interrupt Signal Enable (dma_int_sig_en):** • 1 = enabled • 0 = masked
2	0b RW	**Block Gap Event Signal Enable (blk_gap_event_sig_en):** • 1 = enabled • 0 = masked
1	0b RW	**Transfer Complete Signal Enable (tx_comp_sig_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Complete Signal Enable (cmd_comp_sig_en):** • 1 = enabled • 0 = masked

16.6.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

This register is used to select which interrupt status is sent to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_sig_en	tgt_err_rsp_sig_en	rsvd	tune_err_sig	adma_err_sig_en	cmd12_err_sig_en	cur_limit_err_sig_en	data_end_bit_err_sig_en	data_crc_err_sig_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15:14	0b RO	**Rsvd0 (rsvd0):** Reserved.
13	0b RW	**CEATA_Error Signal Enable (ceata_err_sig_en):** 0 = masked
12	0b RW	**Target Error Response Signal Enable (tgt_err_rsp_sig_en):** 0 = masked
11	0b RO	**Reserved (rsvd):** Reserved.
10	0b RW	**Tuning Error Signal Enable (tune_err_sig):** • 1 = enabled • 0 = masked
9	0b RW	**ADMA Error Signal Enable (adma_err_sig_en):** • 1 = enabled • 0 = masked
8	0b RW	**Auto CMD12 Error Signal Enable (cmd12_err_sig_en):** • 1 = enabled • 0 = masked
7	0b RW	**Current Limit Error Signal Enable (cur_limit_err_sig_en):** • 1 = enabled • 0 = masked
6	0b RW	**Data End Bit Error Signal Enable (data_end_bit_err_sig_en):** • 1 = enabled • 0 = masked
5	0b RW	**Data CRC Error Signal Enable (data_crc_err_sig_en):** • 1 = enabled • 0 = masked
4	0b RW	**Data Timeout Error Signal Enable (data_timeout_err_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**Command Index Error Signal Enable (cmd_ind_err_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Command End Bit Error Signal Enable (cmd_end_bit_err_stat_en):** • 1 = enabled • 0 = masked

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**Command CRC Error Signal Enable (cmd_crc_err_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Timeout Error Signal Enable (cmd_timeout_err_stat_en):** • 1 = enabled • 0 = masked

16.6.26 Auto CMD12 Error Status Register and Host Control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
preset_value	async_int	RSVD0						sampling_clock	execute_tuning	driver_strength		vl	uhs_mode			rsvd								cmd_not_iss_cmd12_err	rsvd1		cmd12_ind_err	cmd12_end_bit_err	cmd12_crc_err	cmd12_timeout_err	cmd12_not_exe

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Preset Value (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. • 1 = Automatic Selection by Preset Value are Enabled • 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.
30	0b RW	**Asynchronous Interrupt (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. Usage: It is recommended that Synchronous Interrupt mode be used for SDIO Controller by setting this be to '0'. If Asynchronous Interrupt Enable mode is used, it is required that this bit remain '0' until SD initialization sequence is complete. • 1 = Enabled • 0 = Disabled

Bit Range	Default & Access	Field Name (ID): Description
29:24	0b RO	**RSVD0:** Reserved
23	0b RW	**Sampling Clock (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared.
22	0b RW/AC	**Execute Tuning (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0. Refer to the spec for more detail about tuning procedure. • 1 = Execute Tuning • 0 = Not Tuned or Tuning Completed
21:20	0b RW	**Driver Strength (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit.
19	0b RW	**Voltage Regulator Control for I/O Cell (vl):** This bit controls voltage regulator for I/O cell.
18:16	0b RW	**UHS Mode Select (uhs_mode):** This field is used to select one of UHS-I modes.
15:8	0h RO	**Rsvd (rsvd):** Reserved.
7	0b RO	**Command Not Issued By Auto CMD12 Error (cmd_not_iss_cmd12_err):** Reserved.
6:5	0h RO	**Rsvd1 (rsvd1):** Reserved
4	0b RO	**Auto CMD12 Index Error (cmd12_ind_err):** Reserved.
3	0b RO	**Auto CMD12 End Bit Error (cmd12_end_bit_err):** Reserved.
2	0b RO	**Auto CMD12 CRC Error (cmd12_crc_err):** Reserved.
1	0b RO	**Auto CMD12 Timeout Error (cmd12_timeout_err):** Reserved.
0	0b RO	**Auto CMD12 Not Executed (cmd12_not_exe):** Reserved.

16.6.27 Capabilities Register (CAPABILITIES)—Offset 40h

This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initialization.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

capabilities

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**Capabilities (capabilities):** Reserved.

16.6.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

capabilities_2

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**Capabilities 2 (capabilities_2):** Reserved.

16.6.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage. The value is meaningful if Voltage Support is set in the Capabilities register. If this information is supplied by the Host System via another method, all Maximum Current Capabilities register shall be 0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd								max_cur_1p8v								max_cur_3p0v								max_cur_3p3v							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (rsvd):** Reserved.
23:16	00h RO	**Maximum Current for 1.8V (max_cur_1p8v):** Reserved.
15:8	00h RO	**Maximum Current for 3.0V (max_cur_3p0v):** Reserved.
7:0	00h RO	**Maximum Current for 3.3V (max_cur_3p3v):** Reserved.

16.6.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved0								non_cmd12_err	reserved		cmd12_ind_err	cmd12_end_bit_err	cmd12_crc_err	cmd12_timeout_err	cmd12_not_exe

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Reserved 0 (reserved0):** Reserved.
7	0b RW	**Force Event for Command Not Issued By Auto CMD12 Error (non_cmd12_err):** • 1 = Interrupt is generated • 0 = No Interrupt
6:5	00b RO	**Reserved (reserved):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**Force Event for Auto CMD12 Index Error (cmd12_ind_err):** • 1 = Interrupt is generated • 0 = No Interrupt
3	0b RW	**Force Event for Auto CMD12 End Bit Error (cmd12_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
2	0b RW	**Force Event for Auto CMD12 CRC Error (cmd12_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
1	0b RW	**Force Event for Auto CMD12 Timeout Error (cmd12_timeout_err):** • 1 = Interrupt is generated • 0 = No Interrupt
0	0b RW	**Force Event for Auto CMD12 Not Executed (cmd12_not_exe):** • 1 = Interrupt is generated • 0 = No Interrupt

16.6.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Error Interrupt Status register can be written. The effect of a write to this address will be reflected in the Error Interrupt Status Register if the corresponding bit of the Error Interrupt Status Enable Register is set.

- Writing 1 : set each bit of the Error Interrupt Status Register
- Writing 0 : no effect

Note: By setting this register, the Error Interrupt can be set in the Error Interrupt Status register. In order to generate interrupt signal, both the Error Interrupt Status Enable and Error Interrupt Signal Enable shall be set.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_ind_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15:14	00b RO	**Reserved 0 (rsvd0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13	0b RW	**Force Event for CEATA Error (ceata_err):** Reserved.
12	0b RW	**Force Event for Target Response Error (tgt_rsp_err):** Reserved.
11:10	0h RO	**Reserved (rsvd):** Reserved.
9	0b RW	**Force Event for ADMA Error (adma_err):** • 1 = Interrupt is generated • 0 = No Interrupt
8	0b RW	**Force Event for Auto CMD12 Error (cmd12_err):** • 1 = Interrupt is generated • 0 = No Interrupt
7	0b RW	**Force Event for Current Limit Error (cur_limit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
6	0b RW	**Force Event for Data End Bit Error (data_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
5	0b RW	**Event for Data CRC Error (data_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
4	0b RW	**Event for Data Timeout Error (data_timeout_err):** • 1 = Interrupt is generated • 0 = No Interrupt
3	0b RW	**Force Event for Command Index Error (cmd_ind_err):** • 1 = Interrupt is generated • 0 = No Interrupt
2	0b RW	**Force Event for Command End Bit Error (cmd_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
1	0b RW	**Force Event for Command CRC Error (cmd_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
0	0b RW	**Force Event for Command Timeout Error (cmd_timeout_err):** • 1 = Interrupt is generated • 0 No Interrupt

16.6.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

When ADMA Error Interrupt occurs, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address Register holds the address around the error descriptor. To recover from the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows:

- ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address
- ST_FDS: Current location set in the ADMA System Address register is the error descriptor address
- ST_CADR: This sate is never set because do not generate ADMA error in this state.

- ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address

The Host Controller generates the ADMA Error Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. In this case, ADMA Error State indicates that an error occurs at ST_FDS state. The Host Driver may find that the Valid bit is not set in the error descriptor.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					adma_len_mis_err	adma_err_state	

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.
2	0b RO	**ADMA Length Mismatch Error (adma_len_mis_err):** This error occurs in the following 2 cases. • While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. • Total data length can not be divided by the block length. • 1 = Error • 0 = No Error
1:0	00b RO	**ADMA Error State (adma_err_state):** This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates '10' because ADMA never stops in this state. Refer to the spec for tabular information about the relationship between this field and SYS_SDR register.

16.6.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

adma_sys_addr

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ADMA System Address (adma_sys_addr):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000001h RO	**Preset Values (Preset_Values):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
31:0	00010000h RO	**Preset Values (Preset_Values):** Reserved.

16.6.34 Boot Timeout Control (BOOT_TIMEOUT_CTRL)—Offset 70h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

time_cnt_val

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Boot Data Timeout Counter Value (time_cnt_val):** Reserved.

16.6.35 Debug Selection Register (DEBUG_SEL)—Offset 74h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd							debug_sel

Bit Range	Default & Access	Field Name (ID): Description
7:1	00h RO	**Reserved (rsvd):** Reserved.
0	0b WO	**Debug Select (debug_sel):** • 1 = cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out. • 0 = receiver module and fifo_ctrl module signals are probed out

16.6.36 Shared Bus Control Register (SHARED_BUS)—Offset E0h

This register is optional. The devices on shared bus are not intended to be controlled by the Standard Host Driver. This is because shared bus configuration depends on a host system; the devices on shared bus may be controlled by a specific driver of a host system.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0	pwr_ctrl							RSVD1	int_pin			RSVD2	clk_pin			RSVD3	bus_width							RSVD4		num_int_pin		RSVD5	num_clk_pin		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:24	0h RW	**Back-End Power Control (pwr_ctrl):** Each bit of this field controls back-end power supply for an embedded device. Host interface voltage (VDDH) is not controlled by this field. The number of devices supported is specified by **Number of Clock Pins**, and a maximum of 7 devices can be controlled. • D24 Back-end Power Control for Device 1 • D25 Back-end Power Control for Device 2 • D26 Back-end Power Control for Device 3 • D27 Back-end Power Control for Device 4 • D28 Back-end Power Control for Device 5 • D29 Back-end Power Control for Device 6 • D30 Back-end Power Control for Device 7 The function of each bit is defined as follows: • 0 = Back-end Power is Off • 1 = Back-end Power is Supplied Back-End power control is effective for embedded memory devices in the Sleep State that support the Sleep command (CMD14) to reduce power consumption and embedded SDIO devices when IOEx is set to 0.
23	0b RO	**RSVD1:** Reserved
22:20	0h RW	**Interrupt Pin Select (int_pin):** Interrupt pin inputs are enabled by this field. Enable of unsupported interrupt pin is meaningless. • 000b = Interrupt is detected by theInterrupt Cycle. • xx1b = INT_A is enabled • x1xb = INT_B is enabled • 1xxb = INT_C is enabled
19	0b RO	**RSVD2:** Reserved
18:16	0h RW	**Clock Pin Select (clk_pin):** One of clock pin outputs is selected by this field. Selection of unsupported clock pins is meaningless. Refer to Figure 2-38 for the timing of clock outputs. • 000b = Clock Pins are disabled • 001b = CLK[1] is selected • 010b = CLK[2] is selected • . . . • 111b = CLK[7] is Selected
15	0b RO	**RSVD3:** Reserved
14:8	0h RO	**Bus Width Preset (bus_width):** Shared bus supports mixing of 4-bit and 8-bit bus width devices. Each bit of this field specifies the bus width for each embedded device. The number of devices supported is specified by Number of Clock Pins, and a maximum of 7 devices are supported. This field is effective when multiple devices are connected to a shared bus (Slot Type is set to 10b in the Capabilities register). In the other case, Extended Data Transfer Width in the Host Control 1 register is used to select 8-bit bus width. As use of 1-bit mode is not intended for shared bus, Data Transfer Width in the Host Control 1 register should be set to 1. • D24 = Bus width preset for Device 1 • D25 = Bus width preset for Device 2 • D26 = Bus width preset for Device 3 • D27 = Bus width preset for Device 4 • D28 = Bus width preset for Device 5 • D29 = Bus width preset for Device 6 • D30 = Bus width preset for Device 7 The function of each bit is defined as follows: • 0 = 4 bit buswidth mode • 1 = 8 bit buswidth mode
7:6	0b RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RO	**Number of Interrupt Pins (num_int_pin):** This field indicates support of interrupt input pins for shared bus system. Three asynchronous interrupt pins are defined, INT_A#, INT_B# and INT_C#. Which interrupt pin is used is determined by the system. Each one is driven by open drain and then wired OR connection is possible. • 00b = Interrupt Input Pin is not supported • 01b = INTA is Supported • 10b = INTA and INTB are supported • 11b = INTA, INTB and INTC are supported
3	0b RO	**RSVD5:** Reserved
2:0	0h RO	**Number of Clock Pins (num_clk_pin):** This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported. Shared bus is supported by specific system. Then the Standard Host Driver does not support control of these clock pins. • 000b Shared bus is not supported • 001b 1 SDCLK pin is supported • 010b 2 SDCLK pins are supported • . . . • 111b 7 SDCLK pins are supported

16.6.37 SPI Interrupt Support Register (SPI_INT_SUP)—Offset F0h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
spi_int_support							

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**SPI Interrupt Support (spi_int_support):** This bit is set to indicate the assertion of interrupts in the SPI mode at any time, irrespective of the status of thecard select (CS) line. If this bit is zero, then SDIO card can only assert the interrupt line in the SPI mode when the CS line is asserted.

16.6.38 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved								int_sig_slot							

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Reserved (reserved):** Reserved.
7:0	00h RO	**Interrupt Signal For Each Slot (int_sig_slot):** These status bits indicate the logical OR of Interrupt Signal and Wakeup Signal for each slot. A maximum of 8 slots can be defined. If one interrupt signal is associated with multiple slots, the Host Driver can know which interrupt is generated by reading these status bits. By a power on reset or by setting Software Reset For All, the interrupt signal shall be de-asserted and this status shall read 00h. • Bit 00 = Slot 1 • Bit 01 = Slot 2 • Bit 02 = Slot 3 • .... • Bit 07 = Slot 8

16.6.39 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: B502h

15			12				8				4				0
1	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0
vend_ver_num								spec_ver_num							

Bit Range	Default & Access	Field Name (ID): Description
15:8	b5h RO	**Vendor Version Number (vend_ver_num):** This status is reserved for the vendor version number. The Host Driver should not use this status.
7:0	02h RO	**Specification Version Number (spec_ver_num):** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. • 00h = SD Host Specification Version 1.00 • 01h = SD Host Specification Version 2.00, Including the feature of the ADMA and Test Register • 02h = SD Host Specification Version 3.00 • others = Reserved

16.7 SD Card PCI Configuration Registers

Table 186. Summary of SD Card PCI Configuration Registers—0/18/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 1815	00000000h
4–7h	4	"Status and Command Register (STATUSCOMMAND)—Offset 4h" on page 1816	00100000h
8–Bh	4	"Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h" on page 1817	00000000h
C–Fh	4	"Cache Line Size, Latency Timer, and Header Type Register (CLLATHEADERBIST)—Offset Ch" on page 1817	00000000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 1818	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 1819	00000000h
2C–2Fh	4	"Subsystem Vendor ID and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch" on page 1820	00000000h
30–33h	4	"Expansion ROM Base Address Register (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1820	00000000h
34–37h	4	"Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h" on page 1821	00000080h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 1821	00000100h
80–83h	4	"Power Management Capability ID Register (POWERCAPID)—Offset 80h" on page 1822	48030001h
84–87h	4	"Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 1822	00000008h
A0–A3h	4	"General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h" on page 1823	00000000h
A4–A7h	4	"General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h" on page 1824	00000000h
A8–ABh	4	"General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h" on page 1824	00000000h
AC–AFh	4	"General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh" on page 1824	00000000h
C0–C3h	4	"General Purpose Input Register (GEN_INPUT_REGRW)—Offset C0h" on page 1825	00000000h
F8–FBh	4	"Manufacturers ID Register (MANID)—Offset F8h" on page 1825	00000000h

16.7.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 0h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
DEVICEID				VENDORID			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	0000h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

16.7.2 Status and Command Register (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:18, F:0] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0		RMA	RCA	Reserved1							CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a '1' to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0h RW/1C	**Received Target Abort (RCA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt; i.e., Bridge does not send Interrupt Assert message through the IOSF SideBand Channel. Reset value of this bit is 0.
9	0h RO	**Reserved4:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SERR# Enable (SERR_ENABLE):** This bit controls the sending of DO_SERR messages on IOSF SB.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridges response to downstream memory accesses. When set, accesses to the memory space of the device are enabled. Reset value of this bit is 0.
0	0h RO	**Reserved6:** Reserved.

16.7.3 Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 8h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

CLASS_CODES | RID

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** This register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Identifies the revision of a particular AHB device. This is tied to a strap at the top level.

16.7.4 Cache Line Size, Latency Timer, and Header Type Register (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0								MULFNDEV	HEADERTYPE							LATTIMER								CACHELINE_SIZE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**Multifunction Device (MULFNDEV):** This bit is always 0 for non-fabric ports. For fabric ports it is driven from the fabric_mult_function strap. A value of 1 indicates a multifunction device; a value of 0 indicates a single function device.
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Doesnt apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesnt apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

16.7.5 Base Address Register (BAR)—Offset 10h

Each AHB device is a single function device with only a single BAR associated with it. Bits 31:4 indicate the Base Address register. Power-up software can determine how much address space the AHB Device requires by writing a value of all 1's to the register and then reading the value back. Bridge will return 0's in all don't-care address bits, effectively specifying the address space required. Unimplemented Base Address registers are hardwired to zero. This is the Size Indicator Read only bits of the register.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR																				SIZEINDICATOR								PREFETCHABLE	TYPE		MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1s.

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RO	**Size Indicator (Read Only) (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0s.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this bar is not prefetchable.
2:1	0h RO	**Type (TYPE):** '00' indicates that the BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0 Indicates that this BAR is present in the memory space.

16.7.6 Base Address Register 1 (BAR1)—Offset 14h

Memory accesses to BAR1 region access the PCI configuration space for the LPIO device. BAR1 region is always 4K. However SW accesses through BAR1 should only access the regular PCI configuration space. BAR1 memory accesses which do not access a defined PCI configuration register are treated as accesses to a reserved register.

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:18, F:0] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR1																				SIZEINDICATOR1								PREFETCHABLE1	TYPE1		MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register1 (BASEADDR1):** This field is present if BAR1 is enabled through private config space. If this register is disabled then this is RO and always returns 0.
11:4	00h RO	**Size Indicator1 (SIZEINDICATOR1):** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this bar is not prefetchable.
2:1	0h RO	**Type (TYPE1):** '00' indicates that the BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0 Indicates that this BAR is present in the memory space.

16.7.7 Subsystem Vendor ID and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: SUBSYSTEMID (bits 31:16), SUBSYSTEMVENDORID (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. Th is register makes it possible for the operating environment to distinguish one audio subsystem from the other. This is a Read Write Once register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. This register enables the operating environment to distinguish one subsystem from the other. This is a Read Write Once register.

16.7.8 Expansion ROM Base Address Register (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: EXPANSION_ROM_BASE (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion ROM Base Address (EXPANSION_ROM_BASE):** Value of all 0s indicates no support for Expansion ROM.

16.7.9 Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 34h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Reserved0																								CAPPTR_POWER							

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. When PM capability is disabled, this register is 00h.

16.7.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
MAX_LAT								MIN_GNT								Reserved0				INTPIN				INTLINE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates that the device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates that the device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

16.7.11 Power Management Capability ID Register (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)   **Offset:** [B:0, D:18, F:0] + 80h

Default: 48030001h

31			28				24				20				16				12				8				4				0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

PMESUPPORT | Reserved0 | VERSION | NXTCAP | POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot. bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

16.7.12 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)   **Offset:** [B:0, D:18, F:0] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Reserved0 | PMESTATUS | Reserved1 | PMEENABLE | Reserved2 | NO_SOFT_RESET | Reserved3 | POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit in this register.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for upstream decode on fabric ports.

16.7.13 General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:18, F:0] + A0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GEN_REG_RW1

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** capabilities over-ride for the sd/sdio/emmc host controler (bits 31:0)

16.7.14 General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:18, F:0] + A4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAP_REG_SEL | GEN_REG_RW2

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CAP_REG_SEL:** select if the capabilty will come from the GEN PCI register or from a hard wire
30:0	0h RW	**GEN_REG_RW2:** capabilities over-ride for the sd/sdio/emmc host controler (bits 62:32)

16.7.15 General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:18, F:0] + A8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GEN_REG_RW3

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** Reserved.

16.7.16 General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:18, F:0] + ACh

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

GEN_REG_RW4

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** Reserved.

16.7.17 General Purpose Input Register (GEN_INPUT_REGRW)—Offset C0h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:18, F:0] + C0h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

GEN_REG_INPUT_RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** Reserved.

16.7.18 Manufacturers ID Register (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:18, F:0] + F8h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

16.8 SD Card Memory Mapped IO Registers

Table 187. Summary of SD Card Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SDMA System Address / Argument 2 Register (SYS_ADR)—Offset 0h" on page 1828	00000000h
4–5h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1829	0000h
6–7h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1830	0000h
8–Bh	4	"Argument 1 Register (ARGUMENT)—Offset 8h" on page 1831	00000000h
C–Dh	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1831	0000h
E–Fh	2	"Command Register (CMD)—Offset Eh" on page 1833	0000h
10–13h	4	"Response Register 0 (RESPONSE0)—Offset 10h" on page 1834	00000000h
14–17h	4	"Response Register 2 (RESPONSE2)—Offset 14h" on page 1835	00000000h
18–1Bh	4	"Response Register 4 (RESPONSE4)—Offset 18h" on page 1835	00000000h
1C–1Fh	4	"Response Register 6 (RESPONSE6)—Offset 1Ch" on page 1836	00000000h
20–23h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1836	00000000h
24–27h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1837	1FFF0000h
28–28h	1	"Host Control 1 Register (HOST_CTL)—Offset 28h" on page 1840	00h
29–29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1841	00h
2A–2Ah	1	"Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah" on page 1842	00h
2B–2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1843	00h
2C–2Dh	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1844	0000h
2E–2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1846	00h
2F–2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1847	00h
30–31h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1848	0000h
32–33h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1851	0000h
34–35h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1853	0000h
36–37h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1855	0000h
38–39h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1856	0000h
3A–3Bh	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1857	0000h
3C–3Fh	4	"Auto CMD12 Error Status Register and Host Control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1859	00000000h
40–43h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1860	00000000h
44–47h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1861	00000000h
48–4Bh	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1861	00000000h
50–51h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1862	0000h

Table 187. Summary of SD Card Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
52–53h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1863	0000h
54–54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1864	00h
58–5Bh	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1865	00000000h
70–73h	4	"Boot Timeout Control (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1866	00000000h
74–74h	1	"Debug Selection Register (DEBUG_SEL)—Offset 74h" on page 1866	00h
E0–E3h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1867	00000000h
F0–F0h	1	"SPI Interrupt Support Register (SPI_INT_SUP)—Offset F0h" on page 1869	00h
FC–FDh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1869	0000h
FE–FFh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1870	B502h

16.8.1 SDMA System Address / Argument 2 Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

sys_adr

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SDMA System Address (sys_adr): (1) SDMA System Address** This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at each boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates a DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the uppermost byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. **(2) Argument 2** This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without AMDA, the available block count value is limited by the Block Count register. 65535 blocks is the maximum value in this case.

16.8.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
tx_blk_size_12	boundary			tr_blk_size											

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW	**TX_BLK_SIZE_12 (tx_blk_size_12):** Transfer Block Size 12th bit. This bit is added to support 4Kb Data block transfer.

Bit Range	Default & Access	Field Name (ID): Description
14:12	000b RW	**Host SDMA Buffer Boundary (boundary):** The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at each boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. • 000b = 4K bytes (Detects A11 carry out) • 001b = 8K bytes (Detects A12 carry out) • 010b = 16K Bytes (Detects A13 carry out) • 011b = 32K Bytes (Detects A14 carry out) • 100b = 64K bytes (Detects A15 carry out) • 101b = 128K Bytes (Detects A16 carry out) • 110b = 256K Bytes (Detects A17 carry out) • 111b = 512K Bytes (Detects A18 carry out)
11:0	000h RW	**Transfer Block Size (tr_blk_size):** This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2 *Determining Buffer Block Length*). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. • 0800h = 2048 Bytes • . . . • 0200h = 512 Bytes • 01FFh = 511 Bytes • . . . • 0004h = 4 Bytes • 0003h = 3 Bytes • 0002h = 2 Bytes • 0001h = 1 Byte • 0000h = No data transfer

16.8.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

blk_count

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Blocks Count For Current Transfer (blk_count):** This register is enabled when Block Count Enable in the Transfer Mode register is set to 1, and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1 and the maximum block count. The HC decrements the block count after each block transfer, and stops when the count reaches zero. Setting the block count to 0 results in no data blocks being transferred. This register should be accessed only when no transaction is executing (i.e., after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. When saving transfer context as a result of a Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the HD shall restore the previously saved block count. • 0000h = Stop Count • 0001h = 1 block • 0002h = 2 blocks • . . . • FFFFh = 65535 blocks

16.8.4 Argument 1 Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
argument																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command Argument 1 (argument):** The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

16.8.5 Transfer Mode Register (TX_MODE)—Offset Ch

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data (Refer to Data Present Select in the Command register), or before issuing a Resume command. The Host Driver shall save the value of this register when the data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller shall implement write protection for this register during data transactions. Writes to this register shall be ignored when the Command Inhibit (DAT) in the Present State register is 1.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd							boot_en	spi_mode	cmd_comp_ata	blk_sel	data_tr_dir	auto_cmd_en		blk_count_en	dma_en

Bit Range	Default & Access	Field Name (ID): Description
15:9	00h RO	**Reserved (rsvd):** Reserved.
8	0b RW	**BOOT_EN (boot_en):** To start boot operation for MMC4.3 1 - To start boot mode 0 - Stop the boot read
7	0b RW	**SPI_MODE (spi_mode):** SPI mode enable bit. 1 - SPI mode 0 - SD mode
6	0b RW	**CMD_COMP_ATA (cmd_comp_ata):** Command Completion Signal Enable for CE-ATA Device. ???1??? - Device will send command completion Signal ???0??? - Device will not send command completion Signal
5	0b RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0b RW	**Data Transfer Direction Select (data_tr_dir):** This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller, and it is set to 0 for all other commands. • 1 = Read (Card to Host) • 0 = Write (Host to Card)
3:2	0b RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0b RW	**Block Count Enable (blk_count_en):** This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8). If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. • 1 = Enable • 0 = Disable
0	0b RW	**DMA Enable (dma_en):** This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). • 1 = DMA Data transfer • 0 = No data transfer or Non DMA data transfer

16.8.6 Command Register (CMD)—Offset Eh

The Host Driver shall check the Command Inhibit (DAT) bit and Command Inhibit (CMD) bit in the Present State register before writing to this register. Writing to the upper byte of this register triggers SD command generation. The Host Driver has the responsibility to write this register because the Host Controller does not protect for writing when Command Inhibit (CMD) is set.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd		cmd_index						cmd_type		data_pr_sel	cmd_index_chk_en	cmd_crc_chk_en	reserved	resp_type_sel	

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Rsvd (rsvd):** Reserved.
13:8	0h RW	**Command Index (cmd_index):** These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	00b RW	**Command Type (cmd_type):** There are three types of special commands: Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. **(1) Suspend Command** If the Suspend command succeeds, the Host Controller shall assume the SD Bus has been released and that it is possible to issue the next command, which uses the DAT line. The Host Controller shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the Host Controller shall maintain its current state, and the Host Driver shall restart the transfer by setting Continue Request in the Block Gap Control register. (Refer to 3.12.1 Suspend Sequence). **(2) Resume Command** The Host Driver re-starts the data transfer by restoring the registers in the range of 000-00Dh. (Refer to Figure 1-4 in section 1.6 for the register map.) The Host Controller shall check for busy before starting write transfers. **(3) Abort Command** If this command is set when executing a read transfer, the Host Controller shall stop reads to the buffer. If this command is set when executing a write transfer, the Host Controller shall stop driving the DAT line. After issuing the Abort command, the Host Driver should issue a software reset. (Refer to 3.8 Abort Transaction). • 11b = Abort -- CMD12, CMD52 for writing 'I/O Abort' in CCCR • 10b = Resume -- CMD52 for writing 'Function Select' in CCCR • 01b = Suspend -- CMD52 for writing 'Bus Suspend' in CCCR • 00b = Normal -- Other commands
5	0b RW	**Data Present Select (data_pr_sel):** This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38). (3) Resume command. • 1 = Data Present • 0 = No Data Present

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**Command Index Check Enable (cmd_index_chk_en):** If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. • 1 = Enable • 0 = Disable
3	0b RW	**Command CRC Check Enable (cmd_crc_chk_en):** If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) • 1 = Enable • 0 = Disable
2	0b RO	**Reserved (reserved):** Reserved.
1:0	0h RW	**Response Type Select (resp_type_sel):** • 00 = No Response • 01 = Response Length 136 • 10 = Response Length 48 • 11 = Response Length 48 check Busy after response

16.8.7 Response Register 0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.8.8 Response Register 2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.8.9 Response Register 4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.8.10 Response Register 6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.8.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

buf_data

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Buffer Data (buf_data):** The Host Controller buffer can be accessed through this 32-bit Data Port register. Refer to section 1.7.

16.8.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 1FFF0000h

Bits	Default	Field
31:29	0 0 0	reserved2
28:25	1 1 1 1	dat_sig_lvl
24	1	cmd_ln_sig_lvl
23:20	1 1 1 1	data_ln_sig_lvl
19	1	wr_prot_sw_pin_lvl
18	1	crd_det_pin_lvl
17	1	crd_st_stable
16	0	crd_ins
15:12	0 0 0 0	reserved1
11	0	buf_rd_en
10	0	buf_wr_en
9	0	rd_tx_active
8	0	wr_tx_active
7:3	0 0 0 0 0	reserved
2	0	dat_ln_active
1	0	cmd_inhibit_dat
0	0	cmd_inhibit_cmd

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (reserved2):** Reserved.
28:25	1111b RO	**DAT Line Signal Level (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. • D28 - DAT[7] • D27 - DAT[6] • D26 - DAT[5] • D25 - DAT[4]
24	1b RO	**CMD Line Signal Level (cmd_ln_sig_lvl):** This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	Fh RO	**DAT[3:0] Line Signal Level (data_ln_sig_lvl):** This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. • D23 = DAT[3] • D22 = DAT[2] • D21 = DAT[1] • D20 = DAT[0]
19	1b RO	**Write Protect Switch Pin Level (wr_prot_sw_pin_lvl):** The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP# pin. • 1 = Write enabled (SDWP#=1) • 0 = Write protected (SDWP#=0)
18	1b RO	**Card Detect Pin Level (crd_det_pin_lvl):** This bit reflects the inverse value of the SDCD# pin. Debouncing is not performed on this bit. This bit may be valid when Card State Stable is set to 1, but it is not guaranteed because of propagation delay. Use of this bit is limited to testing since it must be debounced by software. • 1 = Card present (SDCD#=0) • 0 = No card present (SDCD#=1)
17	1b RO	**Card State Stable (crd_st_stable):** This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. No Card state can be detected by this bit being set to 1 while Card Inserted is set to 0. The Software Reset For All in the Software Reset register shall not affect this bit. • 1 = No Card or Inserted • 0 = Reset or Debouncing

Bit Range	Default & Access	Field Name (ID): Description
16	1b RO	**Card Inserted (crd_ins):** This bit indicates whether a card has been inserted. The Host Controller shall debounce this signal so that the Host Driver will not need to wait for it to stabilize. Changing from 0 to 1 generates a Card Insertion interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register shall not affect this bit. If a card is removed while its power is on and its clock is oscillating, the Host Controller shall clear SD Bus Power in the Power Control register (Refer to Section 2.2.11) and SD Clock Enable in the Clock Control register (Refer to Section 2.2.14). When this bit is changed from 1 to 0, the Host Controller shall immediately stop driving CMD and DAT[3:0] (tri-state). In addition, the Host Driver should clear the Host Controller by the Software Reset For All in Software Reset register. The card detect is active regardless of the SD Bus Power. • 1 = Card Inserted • 0 = Reset or Debouncing or No Card
15:12	0h RO	**Reserved1 (reserved1):** Reserved.
11	0b RO	**Buffer Read Enable (buf_rd_en):** This status is used for non-DMA read transfers. The Host Controller may implement multiple buffers to transfer data efficiently. This read only flag indicates that valid data exists in the host side buffer. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when block data is ready in the buffer and generates the Buffer Read Ready interrupt. • 1 = Read enable • 0 = Read disable
10	0b RO	**Buffer Write Enable (buf_wr_en):** This status is used for non-DMA write transfers. The Host Controller can implement multiple buffers to transfer data efficiently. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready interrupt. The Host Controller should neither set Buffer Write Enable nor generate Buffer Write Ready Interrupt after the last block data is written to the Buffer Data Port Register. • 1 = Write enable • 0 = Write disable
9	0b RO	**Read Transfer Active (rd_tx_active):** This status is used for detecting completion of a read transfer. Refer to Section 3.12.3 for sequence details. This bit is set to 1 for either of the following conditions: • After the end bit of the read command. • When read operation is restarted by writing a 1 to Continue Request in the Block Gap Control register. This bit is cleared to 0 for either of the following conditions: • When the last data block as specified by block length is transferred to the System. • In case of ADMA2, end of read operation is designated by Descriptor Table. • When all valid data blocks in the Host Controller have been transferred to the System and no current block transfers are being sent as a result of the Stop At Block Gap Request being set to 1. A Transfer Complete interrupt is generated when this bit changes to 0. • 1 = Transferring data • 0 = No valid data

Bit Range	Default & Access	Field Name (ID): Description
8	0b RO	**Write Transfer Active (wr_tx_active):** This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the Host Controller. Refer to Section 3.12.4 for more details on the sequence of events. This bit is set in either of the following cases: • After the end bit of the write command. • When write operation is restarted by writing a 1 to Continue Request in the Block Gap Control register. This bit is cleared in either of the following cases: • After getting the CRC status of the last data block as specified by the transfer count (Single and Multiple) In case of ADMA2, transfer count is designated by Descriptor Table. • After getting the CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as the result of the Stop At Block Gap Request being set. This status is useful for the Host Driver in determining non DAT line commands can be issued during write busy. • 1 Transferring data • 0 No valid data
7:3	00h RO	**Reserved (reserved):** Reserved.
2	0b RO	**DAT Line Active (dat_ln_active):** This bit indicates whether one of the DAT lines on SD Bus is in use. (a) In the case of read transactions This status indicates whether a read transfer is executing on the SD Bus. Changing this value from 1 to 0 generates a Block Gap Event interrupt in the Normal Interrupt Status register, as the result of the Stop At Block Gap Request being set. Refer to Section 3.12.3 for details on timing. This bit shall be set in either of the following cases: • After the end bit of the read command. • When writing a 1 to Continue Request in the Block Gap Control register to restart a read transfer. This bit shall be cleared in either of the following cases: • When the end bit of the last data block is sent from the SD Bus to the Host Controller. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table. • When a read transfer is stopped at the block gap initiated by a Stop At Block Gap Request. The Host Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Host Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use suspend / resume function. (b) In the case of write transactions This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. Refer to Section 3.12.4 for sequence details. This bit shall be set in either of the following cases: • After the end bit of the write command. • When writing to 1 to Continue Request in the Block Gap Control register to continue a write transfer. This bit shall be cleared in either of the following cases: • When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive 'Not Busy'. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table. • When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request. (c) Command with busy This status indicates whether a command indicates busy (ex. erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command with busy and cleared when busy is de-asserted. Changing this bit from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. Refer Figure 2-11 to Figure 2-13. • 1 = DAT Line Active • 0 = DAT Line Inactive

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Command Inhibit (DAT) (cmd_inhibit_dat):** This status bit is generated if either the DAT Line Active or the Read Transfer Active is set to 1. If this bit is 0, it indicates the Host Controller can issue the next SD Command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal Interrupt Status register. **Note:** The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. • 1 Cannot issue command which uses the DAT line • 0 Can issue command which uses the DAT line
0	0b RO	**Command Inhibit (CMD) (cmd_inhibit_cmd):** Command Inhibit (CMD) If this bit is 0, it indicates the CMD line is not in use and the Host Controller can issue a SD Command using the CMD line. cleared when the command response is received. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register. Even if the Command Inhibit (DAT) is set to 1, commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command Complete Interrupt in the Normal Interrupt Status register. If the Host Controller cannot issue the command because of a command conflict error (Refer to Command CRC Error in Section 2.2.18) or because of Command Not Issued By Auto CMD12 Error (Refer to Section 2.2.23), this bit shall remain 1 and the Command Complete is not set. • 1 Cannot issue command • 0 Can issue command using only CMD line

16.8.13 Host Control 1 Register (HOST_CTL)—Offset 28h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
crd_det_sig_sel	crd_det_tst_lvl	sd8_bit_mode	dma_sel		hi_spd_en	data_tx_wid	led_ctl

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**Card Detect Signal Selection (crd_det_sig_sel):** This bit selects source for the card detection. • 1 = The Card Detect Test Level is selected (for test purposes) • 0 = SDCD# is selected (for normal use) When the source for the card detection is switched, the interrupt should be disabled during the switching period by clearing the Interrupt Status/Signal Enable register in order to mask unexpected interrupt being caused by the glitch. The Interrupt Status/ Signal Enable should be disabled during the period of debouncing.

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**Card Detect Test Level (crd_det_tst_lvl):** This bit is enabled while the Card Detect Signal Selection is set to 1, and it indicates whether or not the card is inserted. • 1 = Card Inserted • 0 = No Card
5	0b RW	**SD8 Bit Mode (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	00b RW	**DMA Select (dma_sel):** One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. Use of selected DMA is determined by DMA Enable of the Transfer Mode register. • 00 = SDMA is selected • 01 = Reserved (New assignment is not allowed) • 10 = 32-bit Address ADMA2 is selected • 11 = Reserved (will be modified by Version 4.00)
2	0b RW	**High Speed Enable (hi_spd_en):** This bit is optional. Before setting this bit, the Host Driver shall check the High Speed Support in the Capabilities register. If this bit is set to 0 (default), the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock (up to 25MHz). If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock (up to 50MHz). If Preset Value Enable in the Host Control 2 register is set to 1, Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. • 1 = 4-bit mode • 0 = 1-bit mode
1	0b RW	**Data Transfer Width (data_tx_wid):** Reserved.
0	0b RW	**LED Control (led_ctl):** This bit selects the data width of the Host Controller. The Host Driver shall set it to match the data width of the SD card. • 1 = 4-bit mode • 0 = 1-bit mode

16.8.14 Power Control Register (PWR_CTL)—Offset 29h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd			hw_rst	sd_bus_volt_sel			sd_bus_pwr

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Rsvd (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**HW Reset (hw_rst):** Reserved.
3:1	0h RW	**SD Bus Voltage Select (sd_bus_volt_sel):** By setting these bits, the Host Driver selects the voltage level for the SD card. Before setting this register, the Host Driver shall check the Voltage Support bits in the Capabilities register. If an unsupported voltage is selected, the Host System shall not supply SD Bus voltage. • 111b = 3.3V (Typ.) • 110b = 3.0V (Typ.) • 101b = 1.8V (Typ.) • 100b 000b Reserved
0	0b RW	**SD Bus Power (sd_bus_pwr):** Before setting this bit, the SD Host Driver shall set SD Bus Voltage Select. If the Host Controller detects the No Card state, this bit shall be cleared. If this bit is cleared, the Host Controller shall immediately stop driving CMD and DAT[3:0] (tri-state) and drive SDCLK to low level (Refer to Section 2.2.14) For SD Controller, this bit controls the bus voltage to SDMMC3. For SDIO Controller, power to SDIO device on SDMMC2 is not controlled by this bit. GPIO register and pin can be used to controller the SDIO device power. For eMMC Controller, power to eMMC device on SDMMC1 is not controlled by this bit. GPIO register and pin or alternative solutions can be used. • 1 = Power on • 0 = Power off

16.8.15 Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd			drive_ccsd	int_blk_gap	rd_wait_ctl	cont_req	stp_blk_gap_req

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (rsvd):** Reserved.
4	0b RW	**DRIVE_CCSD (drive_ccsd):** If the driver set this bit (change from ???0??? to ???1???), Host controller will send command completion.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**Interrupt at Block Gap (int_blk_gap):** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. • 1 = Enabled • 0 = Disabled
2	0b RW	**Read Wait Control (rd_wait_ctl):** The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the DAT[2] line. Otherwise, the Host Controller has to stop the SD Clock to hold read data, which restricts commands generation. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1, otherwise DAT line conflict may occur. If this bit is set to 0, Suspend/Resume cannot be supported. • 1 = Enable Read Wait Control • 0 = Disable Read Wait Control
1	0b RW	**Continue Request (cont_req):** This bit is used to restart a transaction, which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At Block Gap Request to 0 and set this bit 1 to restart the transfer. The Host Controller automatically clears this bit in either of the following cases: • In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. • In the case of a write transaction, the Write Transfer Active changes from 0 to 1 as the write transaction restarts. Therefore, it is not necessary for Host Driver to set this bit to 0. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. • 1 = Restart • 0 = Not affect
0	0b RW	**Stop at Block Gap Request (stp_blk_gap_req):** This bit is used to stop executing read and write transaction at the next block gap for non-DMA, SDMA and ADMA transfers. The Host Driver shall leave this bit set Copyright 2002-2011 SD Association SD Host Controller Simplified Specification Version 3.00 44 to 1 until the Transfer Complete is set to 1. Clearing both Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. When Host Controller version is 1.00, the Host Driver can set this bit if the card supports Read Wait Control. When Host Controller version is 2.00 or later, the Host Driver can set this bit regardless of the card supports Read Wait Control. The Host Controller shall stop read transfer by using Read Wait or stopping SD clock. In case of write transfers in which the Host Driver writes data to the Buffer Data Port register, the Host Driver shall set this bit after all block data is written. If this bit is set to 1, the Host Driver shall not write data to Buffer Data Port register. This bit affects Read Transfer Active, Write Transfer Active, DAT Line Active and Command Inhibit (DAT) in the Present State register. Regarding detailed control of bits D01 and D00, refer to Section 3.8 and 3.12. • 1 = Stop • 0 = Transfer

16.8.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is mandatory for the Host Controller, but wakeup functionality depends on the Host Controller system hardware and software. The Host Driver shall maintain voltage on the SD Bus, by setting SD Bus Power to 1 in the Power Control register, when wakeup event via Card Interrupt is desired. Wakeup Event is not supported by Host Controller. Sideband wake via GPIO pin and register shall be used instead. During RTD3, GPIO register is readable and GPIO signal is routed to APIC.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					wakeup_en_sd_rm	wakeup_en_sd_ins	wakeup_en_crd_int

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.
2	0b RW	**Wakeup Event Enable On SD Card Removal (wakeup_en_sd_rm):** This bit enables wakeup event via Card Removal assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. • 1 = Enable • 0 = Disable
1	0b RW	**Wakeup Event Enable On SD Card Insertion (wakeup_en_sd_ins):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. • 1 = Enable • 0 = Disable
0	0b RW	**Wakeup Event Enable On Card Interrupt (wakeup_en_crd_int):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. • 1 = Enable • 0 = Disable

16.8.17 Clock Control Register (CLK_CTL)—Offset 2Ch

At the initialization of the Host Controller, the Host Driver shall set the SDCLK Frequency Select according to the Capabilities register.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sdclk_freq_sel								upper_sdclk_freq_sel		rsvd			sd_clk_en	int_clk_stable	int_clk_en

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**SDCLK Frequency Select (sdclk_freq_sel):** This register is used to select the frequency of the SDCLK pin. The definition of this field is dependent on the Host Controller Version. **(1) 8-bit Divided Clock Mode** This mode is supported by the Host Controller Version 1.00 and 2.00. The frequency is not programmed directly, rather, this register holds the divisor of the Base Clock Frequency For SD Clock in the capabilities register. Only the following settings are allowed. **(1) 8-bit Divided Clock Mode** • 80h = base clock divided by 256 • 40h = base clock divided by 128 • 20h = base clock divided by 64 • 10h = base clock divided by 32 • 08h = base clock divided by 16 • 04h = base clock divided by 8 • 02h = base clock divided by 4 • 01h = base clock divided by 2 • 00h = base clock(10MHz and up) Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor, but it should not be set. The three default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register. • 400KHz divider value • 25MHz divider value • 50MHz divider value According to the Physical Layer Specification, the maximum SD Clock frequency is 25 MHz in normal speed mode and 50MHz in high speed mode, and shall never exceed this limit. The frequency of the SDCLK is set by the following formula: Clock Frequency = (Base Clock) / divisor Thus, choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. For example, if the Base Clock Frequency For SD Clock in the Capabilities register has the value 33MHz, and the target frequency is 25MHz, then choosing the divisor value of 01h will yield 16.5MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400KHz, the divisor value of 40h yields the optimal clock value of 258KHz. **(2) 10-bit Divided Clock Mode** Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits, and all divider values shall be supported. • 3FFh = 1/2046 Divided Clock • N = 1/2N Divided Clock (Duty 50%) • 002h = 1/4 Divided Clock • 001h = 1/2 Divided Clock • 000h = Base Clock (10MHz and up) • 3FFh = Base Clock * M / 1024 • .... • N - 1 = Base Clock * M / N • .... • 002h = Base Clock * M / 3 • 001h = Base Clock * M / 2 • 000h = Base Clock * M This field depends on setting of Preset Value Enable in the Host Control 2 register. If Preset Value Enable = 0, this field is set by Host Driver. If the Preset Value Enable = 1, this field is automatically set to a value specified in one of Preset Value registers.

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Upper Bits of SDCLK Frequency Select (upper_sdclk_freq_sel):** Host Controller Versions 1.00 and 2.00 do not support these bits and they are treated as 00b fixed value (ROC). Host Controller Version 3.00 shall support these bits to expand SDCLK Frequency Select to 10-bit. Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select.
5:3	0h RO	**Rsvd (rsvd):** Reserved.
2	0b RW	**SD Clock Enable (sd_clk_en):** The Host Controller shall stop SDCLK when writing this bit to 0. SDCLK Frequency Select can be changed when this bit is 0. Then, the Host Controller shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK=0). If the Card Inserted in the Present State register is cleared, this bit shall be cleared. • 1 = Enable • 0 = Disable
1	0b RO	**Internal Clock Stable (int_clk_stable):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. **Note:** This is useful when using PLL for a clock oscillator that requires setup time. • 1 = Ready • 0 = Not Ready
0	0b RW	**Internal Clock Enable (int_clk_en):** This bit is set to 0 when the Host Driver is not using the Host Controller, or when the Host Controller awaits a wakeup event. The Host Controller should stop its internal clock to go to a very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the Host Controller shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection. • 1 = Oscillate • 0 = Stop

16.8.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

At the initialization of the Host Controller, the Host Driver shall set the Data Timeout Counter Value according to the Capabilities register.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
reserved				data_timeout_cnt_val			

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Rsvd (reserved):** Reserved.
3:0	0h RW	**Data Timeout Counter Value (data_timeout_cnt_val):** This value determines the interval by which DAT line timeouts are detected. For more information about timeout generation, refer to the Data Timeout Error in the Error Interrupt Status register. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). • 1111b Reserved • 1110b = TMCLK x 2^27 • .... • 0001b = TMCLK x 2^14 • 0000b = TMCLK x 2^13

16.8.19 Software Reset Register (SW_RST)—Offset 2Fh

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					sw_rst_dat_ln	sw_rst_cmd_ln	sw_rst_all

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**Software Reset For DAT Line (sw_rst_dat_ln):** Only part of data circuit is reset. DMA circuit is also reset. The following registers and bits are cleared by this bit: Buffer Data Port register • Buffer is cleared and initialized. Present State register • Buffer Read Enable • Buffer Write Enable • Read Transfer Active • Write Transfer Active • DAT Line Active • Command Inhibit (DAT) Block Gap Control register • Continue Request • Stop At Block Gap Request Normal Interrupt Status register • Buffer Read Ready • Buffer Write Ready • DMA Interrupt • Block Gap Event • Transfer Complete • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.
1	0b RW	**Software Reset For CMD Line (sw_rst_cmd_ln):** Only part of command circuit is reset. The following registers and bits are cleared by this bit: Present State register • Command Inhibit (CMD) Normal Interrupt Status register • Command Complete • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.
0	0b RW	**Software Reset For All (sw_rst_all):** This reset affects the entire Host Controller except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the Host Driver shall set this bit to 1 to reset the Host Controller. The Host Controller shall reset this bit to 0 when Capabilities registers are valid and the Host Driver can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the host driver should issue reset command and reinitialize the SD card. • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.

16.8.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

The Normal Interrupt Status Enable affects reads of this register, but Normal Interrupt Signal Enable does not affect these reads. An interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1. Writing 1 to a bit of RW1C attribute clears it; writing 0 keeps the bit unchanged. Writing 1 to a bit of ROC attribute keeps the bit unchanged. More than one status can be cleared with a single register write. The Card Interrupt is cleared when the card stops asserting the interrupt; that is, when the Card Driver services the interrupt condition.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
err_int	boot_ter_int	boot_ck_rcv	re_tune	int_c	int_b	int_a	crd_int	crd_rm	crd_ins	buf_rd_rdy	buf_wr_rdy	dma_int	blk_gap_event	tx_comp	cmd_comp

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Error Interrupt (err_int):** If any of the bits in the Error Interrupt Status register are set, then this bit is set. Therefore the Host Driver can efficiently test for an error by checking this bit first. This bit is read only. • 1 = Error • 0 = No Error
14	0b RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0b RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0b RO	**Re-Tuning Event (re_tune):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. • 1 Re-Tuning should be performed • 0 Re-Tuning is not required
11	0b RO	**INT_C (int_c):** This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_C is detected • 0 = No interrupt is detected
10	0b RO	**INT_B (int_b):** This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_B is detected • 0 = No interrupt is detected
9	0b RO	**INT_A (int_a):** This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_A is detected • 0 = No interrupt is detected

Bit Range	Default & Access	Field Name (ID): Description
8	0b RO	**Card Interrupt (crd_int):** Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. When this status has been set and the Host Driver needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status Enable register may be set to 0 in order to clear the card interrupt statuses latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (It should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of shared bus, interrupt pins are used to detect interrupts. If 000b is set to Interrupt Pin Select in the Shared Bus Control register, this status is effective. Non-zero value is set to Interrupt Pin Select, INT_A, INT_B or INT_C is then used to device interrupts. • 1 = Generate Card Interrupt • 0 = No Card Interrupt
7	0b RW/1C	**Card Removal (crd_rm):** This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed. Because the card detect state may possibly be changed when the Host Driver clear this bit and interrupt event may not be generated. • 1 = Card removed • 0 = Card state stable or Debouncing
6	0b RW/1C	**Card Insertion (crd_ins):** This status is set if the Card Inserted in the Present State register changes from 0 to 1. When the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed, because the card detect state may possibly be changed when the Host Driver clears this bit and interrupt event may not be generated. • 1 Card inserted • 0 Card state stable or Debouncing
5	0b RW/1C	**Buffer Read Ready (buf_rd_rdy):** This status is set if the Buffer Read Enable changes from 0 to 1. Refer to the Buffer Read Enable in the Present State register. While performing tuning procedure (Execute Tuning is set to 1), Buffer Read Ready is set to 1 for every CMD19 execution. • 1 = Ready to read buffer • 0 = Not ready to read buffer
4	0b RW/1C	**Buffer Write Ready (buf_wr_rdy):** This status is set if the Buffer Write Enable changes from 0 to 1. Refer to the Buffer Write Enable in the Present State register. • 1 = Ready to write buffer • 0 = Not ready to write buffer
3	0b RW/1C	**DMA Interrupt (dma_int):** This status is set if the Host Controller detects the Host SDMA Buffer boundary during transfer. Refer to the Host SDMA Buffer Boundary in the Block Size register. Other DMA interrupt factors may be added in the future. In case of ADMA, by setting Int field in the descriptor table, Host Controller generates this interrupt. Suppose that it is used for debugging. This interrupt shall not be generated after the Transfer Complete. • 1 = DMA Interrupt is generated • 0 = No DMA Interrupt
2	0b RW/1C	**Block Gap Event (blk_gap_event):** If the Stop At Block Gap Request in the Block Gap Control register is set, this bit is set when both a read / write transaction is stopped at a block gap. If Stop At Block Gap Request is not set to 1, this bit is not set to 1. **(1) In the case of a Read Transaction** This bit is set at the falling edge of the DAT Line Active Status, when the transaction is stopped at SD Bus timing. The Read Wait shall be supported in order to use this function. Refer to Section 3.12.3 for timing details. p]**(1) In the case of a Write Transaction** This bit is set at the falling edge of Write Transfer Active Status (after getting CRC status at SD Bus timing). Refer to Section 3.12.4 for more details on the sequence of events. • 1 = Transaction stopped at block gap • 0 = No Block Gap Event

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW/1C	**Transfer Complete (tx_comp):** This bit is set when a read / write transfer and a command with busy is completed. **(1) In the case of a Read Transaction** This bit is set at the falling edge of Read Transfer Active Status. This interrupt is generated in two cases. The first is when a data transfer is completed as specified by data length (After the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the Stop At Block Gap Request in the Block Gap Control register (After valid data has been read to the Host System). Refer to Section 3.12.3 for more details on the sequence of events. **(2) In the case of a Write Transaction** This bit is set at the falling edge of the DAT Line Active Status. This interrupt is generated in two cases. The first is when the last data is written to the SD card as specified by data length and the busy signal released. The second is when data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control register and data transfers completed. (After valid data is written to the SD card and the busy signal released). Refer to Section 3.12.4 for more details on the sequence of events. **(3) In the case of a command with busy** This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit (DAT) in the Present State register. Refer to the spec for the relationship between Transfer Complete and Data Timeout Error. • 1 = Command execution is completed • 0 = Not complete While performing tuning procedure (Execute Tuning is set to 1), Transfer Complete is not set to 1.
0	0b RW/1C	**Command Complete (cmd_comp):** This bit is set when get the end bit of the command response. Auto CMD12 and Auto CMD23 consist of two responses. Command Complete is not generated by the response of CMD12 or CMD23 but generated by the response of a read/write command. Refer to Command Inhibit (CMD) in the Present State register for how to control this bit. Command Timeout Error has higher priority than Command Complete. If both bits are set to 1, it can be considered that the response was not received correctly. For a tabular description of the relationship between these two bits, refer to the description of Command Complete in the spec. • 1 = Command complete • 0 = No command complete

16.8.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Signals defined in this register can be enabled by the Error Interrupt Status Enable register, but not by the Error Interrupt Signal Enable register. The interrupt is generated when the Error Interrupt Signal Enable is enabled and at least one of the statuses is set to 1. Writing to 1 clears the bit, and writing to 0 keeps the bit unchanged. More than one status can be cleared at the one register write.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
vend_spec_err_status	boot_cmd_timeout_err	ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_index_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW	**Vendor Specific Error Status (vend_spec_err_status):** Reserved.
14	0b RW	**Boot Command Timeout Error (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0b RW	**CEATA Error (ceata_err):** Occurs when ATA command termination has occured due to an error condition the device has encountered.
12	0b RW	**Target Response Error (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction).
11:10	0h RO	**Reserved (rsvd):** Reserved.
9	0b RW	**ADMA Error (adma_err):** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. In addition, the Host Controller generates this Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. **ADMA Error State** in the ADMA Error Status indicates that an error occurs in ST_FDS state.The Host Driver may find that Valid bit is not set at the error descriptor. • 0 = error • 1 = no error
8	0b RW	**Auto CMD12 Error (cmd12_err):** Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. • 1 = error • 0 = no error
7	0b RW	**Current Limit Error (cur_limit_err):** By setting the **SD Bus Power** bit in the Power Control register, the Host Controller is requested to supply power for the SD Bus. If the Host Controller supports the Current Limit function, it can be protected from an illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the Host Controller is not supplying power to SD card due to some failure. Reading 0 means that the Host Controller is supplying power and no error has occurred. The Host Controller may require some sampling time to detect the current limit. If the Host Controller does not support this function, this bit shall always be set to 0. • 1 = power fail • 0 = no error
6	0b RW	**Data End Bit Error (data_end_bit_err):** Occurs either when detecting 0 at the end bit position of read data which uses the DAT line or at the end bit position of the CRC Status. • 1 = error • 0 = no error
5	0b RW	**Data CRC Error (data_crc_err):** Occurs when detecting CRC error when transferring read data which uses the **DAT** line or when detecting the Write CRC status having a value of other than 010b.
4	0b RW	**Data Timeout Error (data_timeout_err):** This bit is set when detecting one of following timeout conditions. • Busy timeout for R1b,R5b type • Busy timeout after Write CRC status • Write CRC Status timeout • Read Data timeout • 1 = time out • 0 = no error

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**Command Index Error (cmd_index_err):** This bit is set if a Command Index error occurs in the command response. • 1 = error • 0 = no error
2	0b RW	**Command End Bit Error (cmd_end_bit_err):** This bit is set when detecting that the end bit of a command response is 0. • 1 = End Bit Error generated • 0 = no error
1	0b RW	**Command CRC Error (cmd_crc_err): Command CRC Error** is generated in two cases. If a response is returned and the **Command Timeout Error** is set to 0(indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller shall abort the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict (refer to tabular data in the spec. that explains the relationship between **Command CRC Error** and **Command Timeout Error**). • 1 = CRC Error Generated. • 0 = no error
0	0b RW	**Command Timeout Error (cmd_timeout_err):** This bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict (in which case **Command CRC Error** shall also be set, as shown in tabular data in the spec that explains the relationship between this bit and **Command CRC Error**) this bit shall be set without waiting for 64 SD clock cycles, because the command will be aborted by the Host Controller. • 1 = time out • 0 = no Error

16.8.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Setting to 1 enables Interrupt Status. **Implementation Note:** The Host Controller may sample the card interrupt signal during interrupt period, and may hold its value in the flip-flop. If the **Card Interrupt Status Enable** is set to 0, the Host Controller shall clear all internal signals regarding Card Interrupt.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	rsvd				boot_term_int_en	boot_ack_rcv_en	crd_int_stat_en	crd_rm_stat_en	crd_ins_stat_en	buf_rd_rdy_stat_en	buf_wr_rdy_stat_en	dma_int_stat_en	blk_gap_event_stat_en	tx_comp_stat_en	cmd_comp_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Fixed to 0 (fixed_0):** The Host Driver shall control error interrupts using the Error Interrupt Status Enable register.
14:11	0h RO	**Reserved (rsvd):** Reserved.
10	0b RW	**Boot Term Interrupt Enable (boot_term_int_en):** 0 = Masked.
9	0b RW	**Boot Acknowledge Receive Enable (boot_ack_rcv_en):** 0 = Masked
8	0b RW	**Card Interrupt Status Enable (crd_int_stat_en):** If this bit is set to 0, the Host Controller shall clear interrupt request to the System. The **Card Interrupt** detection is stopped when this bit is cleared, and restarted when this bit is set to 1. The Host Driver may clear the **Card Interrupt Status Enable** before servicing the Card Interrupt, and may set this bit again after all interrupt requests from the card are cleared, to prevent inadvertent interrupts. • 1 = enabled • 0 = masked
7	0b RW	**Card Removal Status Enable (crd_rm_stat_en):** • 1 = enabled • 0 = masked
6	0b RW	**Card Insertion Status Enable (crd_ins_stat_en):** [• 1 = enabled • 0 = masked
5	0b RW	**Buffer Read Ready Status Enable (buf_rd_rdy_stat_en):** • 1 = enabled • 0 = masked
4	0b RW	**Buffer Write Ready Status Enable (buf_wr_rdy_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**DMA Interrupt Status Enable (dma_int_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Block Gap Event Status Enable (blk_gap_event_stat_en):** • 1 = enabled • 0 = masked
1	0b RW	**Transfer Complete Status Enable (tx_comp_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Complete Status Enable (cmd_comp_stat_en):** • 1 = enabled • 0 = masked

16.8.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Setting to 1 enables interrupt status. **Implementation Note:** To detect CMD line conflict, the Host Driver must set both **Command Timeout Error Status Enable** and **Command CRC Error Status Enable to 1**.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_en	tgt_rsp_err_en	rsvd	tune_err_stat_en	adma_err_stat_en	cmd12_err_stat_en	cur_limit_err_stat_en	data_end_bit_err_stat_en	data_crc_err_stat_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15:14	0b RO	**Rsvd0 (rsvd0):** Reserved.
13	0b RW	**CEATA Error Enable (ceata_err_en):** 0 = masked
12	0b RW	**Target Response Error Enable (tgt_rsp_err_en):** 0 = masked
11	0b RO	**Rsvd (rsvd):** Reserved.
10	0b RW	**Tuning Error Status Enable (tune_err_stat_en):** • 1 = enabled • 0 = masked
9	0b RW	**ADMA Error Status Enable (adma_err_stat_en):** • 1 = enabled • 0 = masked
8	0b RW	**Auto CMD12 Error Status Enable (cmd12_err_stat_en):** • 1 = enabled • 0 = masked
7	0b RW	**Current Limit Error Status Enable (cur_limit_err_stat_en):** • 1 = enabled • 0 = masked
6	0b RW	**Data End Bit Error Status Enable (data_end_bit_err_stat_en):** • 1 = enabled • 0 = masked

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**Data CRC Error Status Enable (data_crc_err_stat_en):** • 1 = enabled • 0 = masked
4	0b RW	**Data Timeout Error Status Enable (data_timeout_err_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**Command Index Error Status Enable (cmd_ind_err_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Command End Bit Error Status Enable (cmd_end_bit_err_stat_en):** • 1 = enabled • 0 = masked
1	0b RW	**Command CRC Error Status Enable (cmd_crc_err_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Timeout Error Status Enable (cmd_timeout_err_stat_en):** • 1 = enabled • 0 = masked

16.8.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

This register is used to select which interrupt status is indicated to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	rsvd				boot_term_int_sig_en	boot_ack_rcv_sig_en	crd_int_sig_en	crd_rm_sig_en	crd_ins_sig_en	buf_rd_rdy_sig_en	buf_wr_rdy_sig_en	dma_int_sig_en	blk_gap_event_sig_en	tx_comp_sig_en	cmd_comp_sig_en

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Fixed to 0 (fixed_0):** The Host Driver shall control error interrupts using the Error Interrupt Signal Enable register.
14:11	0h RO	**Reserved (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0b RW	**Boot Terminate Interrupt Signal Enable (boot_term_int_sig_en):** 0 = masked
9	0b RW	**Boot Acknowledge Receive Signal Enable (boot_ack_rcv_sig_en):** 0 = masked
8	0b RW	**Card Interrupt Signal Enable (crd_int_sig_en):** • 1 = enabled • 0 = masked
7	0b RW	**Card Removal Signal Enable (crd_rm_sig_en):** • 1 = enabled • 0 = masked
6	0b RW	**Card Insertion Signal Enable (crd_ins_sig_en):** • 1 = enabled • 0 = masked
5	0b RW	**Buffer Read Ready Signal Enable (buf_rd_rdy_sig_en):** • 1 = enabled • 0 = masked
4	0b RW	**Buffer Write Ready Signal Enable (buf_wr_rdy_sig_en):** • 1 = enabled • 0 = masked
3	0b RW	**DMA Interrupt Signal Enable (dma_int_sig_en):** • 1 = enabled • 0 = masked
2	0b RW	**Block Gap Event Signal Enable (blk_gap_event_sig_en):** • 1 = enabled • 0 = masked
1	0b RW	**Transfer Complete Signal Enable (tx_comp_sig_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Complete Signal Enable (cmd_comp_sig_en):** • 1 = enabled • 0 = masked

16.8.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

This register is used to select which interrupt status is sent to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_sig_en	tgt_err_rsp_sig_en	rsvd	tune_err_sig	adma_err_sig_en	cmd12_err_sig_en	cur_limit_err_sig_en	data_end_bit_err_sig_en	data_crc_err_sig_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15:14	0b RO	**Rsvd0 (rsvd0):** Reserved.
13	0b RW	**CEATA_Error Signal Enable (ceata_err_sig_en):** 0 = masked
12	0b RW	**Target Error Response Signal Enable (tgt_err_rsp_sig_en):** 0 = masked
11	0b RO	**Reserved (rsvd):** Reserved.
10	0b RW	**Tuning Error Signal Enable (tune_err_sig):** • 1 = enabled • 0 = masked
9	0b RW	**ADMA Error Signal Enable (adma_err_sig_en):** • 1 = enabled • 0 = masked
8	0b RW	**Auto CMD12 Error Signal Enable (cmd12_err_sig_en):** • 1 = enabled • 0 = masked
7	0b RW	**Current Limit Error Signal Enable (cur_limit_err_sig_en):** • 1 = enabled • 0 = masked
6	0b RW	**Data End Bit Error Signal Enable (data_end_bit_err_sig_en):** • 1 = enabled • 0 = masked
5	0b RW	**Data CRC Error Signal Enable (data_crc_err_sig_en):** • 1 = enabled • 0 = masked
4	0b RW	**Data Timeout Error Signal Enable (data_timeout_err_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**Command Index Error Signal Enable (cmd_ind_err_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Command End Bit Error Signal Enable (cmd_end_bit_err_stat_en):** • 1 = enabled • 0 = masked

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**Command CRC Error Signal Enable (cmd_crc_err_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Timeout Error Signal Enable (cmd_timeout_err_stat_en):** • 1 = enabled • 0 = masked

16.8.26 Auto CMD12 Error Status Register and Host Control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

Bits	31	30	29:24	23	22	21:20	19	18:16	15:8	7	6:5	4	3	2	1	0
Default	0	0	0 0 0 0 0 0	0	0	0 0	0	0 0 0	0 0 0 0 0 0 0 0	0	0 0	0	0	0	0	0
Field	preset_value	async_int	RSVD0	sampling_clock	execute_tuning	driver_strength	vl	uhs_mode	rsvd	cmd_not_iss_cmd12_err	rsvd1	cmd12_ind_err	cmd12_end_bit_err	cmd12_crc_err	cmd12_timeout_err	cmd12_not_exe

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Preset Value (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. • 1 = Automatic Selection by Preset Value are Enabled • 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.
30	0b RW	**Asynchronous Interrupt (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. Usage: It is recommended that Synchronous Interrupt mode be used for SDIO Controller by setting this be to '0'. If Asynchronous Interrupt Enable mode is used, it is required that this bit remain '0' until SD initialization sequence is complete. • 1 = Enabled • 0 = Disabled

Bit Range	Default & Access	Field Name (ID): Description
29:24	0b RO	**RSVD0:** Reserved
23	0b RW	**Sampling Clock (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared.
22	0b RW/AC	**Execute Tuning (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0. Refer to the spec for more detail about tuning procedure. • 1 = Execute Tuning • 0 = Not Tuned or Tuning Completed
21:20	0b RW	**Driver Strength (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit.
19	0b RW	**Voltage Regulator Control for I/O Cell (vl):** This bit controls voltage regulator for I/O cell.
18:16	0b RW	**UHS Mode Select (uhs_mode):** This field is used to select one of UHS-I modes.
15:8	0h RO	**Rsvd (rsvd):** Reserved.
7	0b RO	**Command Not Issued By Auto CMD12 Error (cmd_not_iss_cmd12_err):** Reserved.
6:5	0h RO	**Rsvd1 (rsvd1):** Reserved
4	0b RO	**Auto CMD12 Index Error (cmd12_ind_err):** Reserved.
3	0b RO	**Auto CMD12 End Bit Error (cmd12_end_bit_err):** Reserved.
2	0b RO	**Auto CMD12 CRC Error (cmd12_crc_err):** Reserved.
1	0b RO	**Auto CMD12 Timeout Error (cmd12_timeout_err):** Reserved.
0	0b RO	**Auto CMD12 Not Executed (cmd12_not_exe):** Reserved.

16.8.27 Capabilities Register (CAPABILITIES)—Offset 40h

This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initialization.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

capabilities

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**Capabilities (capabilities):** Reserved.

16.8.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

capabilities_2

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**Capabilities 2 (capabilities_2):** Reserved.

16.8.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage. The value is meaningful if Voltage Support is set in the Capabilities register. If this information is supplied by the Host System via another method, all Maximum Current Capabilities register shall be 0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

Bits	31:24	23:16	15:8	7:0
Field	rsvd	max_cur_1p8v	max_cur_3p0v	max_cur_3p3v
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (rsvd):** Reserved.
23:16	00h RO	**Maximum Current for 1.8V (max_cur_1p8v):** Reserved.
15:8	00h RO	**Maximum Current for 3.0V (max_cur_3p0v):** Reserved.
7:0	00h RO	**Maximum Current for 3.3V (max_cur_3p3v):** Reserved.

16.8.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

Bits	15:8	7	6:5	4	3	2	1	0
Field	reserved0	non_cmd12_err	reserved	cmd12_ind_err	cmd12_end_bit_err	cmd12_crc_err	cmd12_timeout_err	cmd12_not_exe
Default	0 0 0 0 0 0 0 0	0	0 0	0	0	0	0	0

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Reserved 0 (reserved0):** Reserved.
7	0b RW	**Force Event for Command Not Issued By Auto CMD12 Error (non_cmd12_err):** • 1 = Interrupt is generated • 0 = No Interrupt
6:5	00b RO	**Reserved (reserved):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**Force Event for Auto CMD12 Index Error (cmd12_ind_err):** • 1 = Interrupt is generated • 0 = No Interrupt
3	0b RW	**Force Event for Auto CMD12 End Bit Error (cmd12_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
2	0b RW	**Force Event for Auto CMD12 CRC Error (cmd12_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
1	0b RW	**Force Event for Auto CMD12 Timeout Error (cmd12_timeout_err):** • 1 = Interrupt is generated • 0 = No Interrupt
0	0b RW	**Force Event for Auto CMD12 Not Executed (cmd12_not_exe):** • 1 = Interrupt is generated • 0 = No Interrupt

16.8.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Error Interrupt Status register can be written. The effect of a write to this address will be reflected in the Error Interrupt Status Register if the corresponding bit of the Error Interrupt Status Enable Register is set.

- Writing 1 : set each bit of the Error Interrupt Status Register
- Writing 0 : no effect

Note: By setting this register, the Error Interrupt can be set in the Error Interrupt Status register. In order to generate interrupt signal, both the Error Interrupt Status Enable and Error Interrupt Signal Enable shall be set.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_ind_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15:14	00b RO	**Reserved 0 (rsvd0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13	0b RW	**Force Event for CEATA Error (ceata_err):** Reserved.
12	0b RW	**Force Event for Target Response Error (tgt_rsp_err):** Reserved.
11:10	0h RO	**Reserved (rsvd):** Reserved.
9	0b RW	**Force Event for ADMA Error (adma_err):** • 1 = Interrupt is generated • 0 = No Interrupt
8	0b RW	**Force Event for Auto CMD12 Error (cmd12_err):** • 1 = Interrupt is generated • 0 = No Interrupt
7	0b RW	**Force Event for Current Limit Error (cur_limit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
6	0b RW	**Force Event for Data End Bit Error (data_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
5	0b RW	**Event for Data CRC Error (data_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
4	0b RW	**Event for Data Timeout Error (data_timeout_err):** • 1 = Interrupt is generated • 0 = No Interrupt
3	0b RW	**Force Event for Command Index Error (cmd_ind_err):** • 1 = Interrupt is generated • 0 = No Interrupt
2	0b RW	**Force Event for Command End Bit Error (cmd_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
1	0b RW	**Force Event for Command CRC Error (cmd_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
0	0b RW	**Force Event for Command Timeout Error (cmd_timeout_err):** • 1 = Interrupt is generated • 0 No Interrupt

16.8.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

When ADMA Error Interrupt occurs, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address Register holds the address around the error descriptor. To recover from the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows:

- ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address
- ST_FDS: Current location set in the ADMA System Address register is the error descriptor address
- ST_CADR: This sate is never set because do not generate ADMA error in this state.

- ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address

The Host Controller generates the ADMA Error Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. In this case, ADMA Error State indicates that an error occurs at ST_FDS state. The Host Driver may find that the Valid bit is not set in the error descriptor.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					adma_len_mis_err	adma_err_state	

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.
2	0b RO	**ADMA Length Mismatch Error (adma_len_mis_err):** This error occurs in the following 2 cases. • While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. • Total data length can not be divided by the block length. • 1 = Error • 0 = No Error
1:0	00b RO	**ADMA Error State (adma_err_state):** This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates '10' because ADMA never stops in this state. Refer to the spec for tabular information about the relationship between this field and SYS_SDR register.

16.8.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

adma_sys_addr

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ADMA System Address (adma_sys_addr):** Reserved.

16.8.34 Boot Timeout Control (BOOT_TIMEOUT_CTRL)—Offset 70h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

time_cnt_val

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Boot Data Timeout Counter Value (time_cnt_val):** Reserved.

16.8.35 Debug Selection Register (DEBUG_SEL)—Offset 74h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd							debug_sel

Bit Range	Default & Access	Field Name (ID): Description
7:1	00h RO	**Reserved (rsvd):** Reserved.
0	0b WO	**Debug Select (debug_sel):** • 1 = cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out. • 0 = receiver module and fifo_ctrl module signals are probed out

16.8.36 Shared Bus Control Register (SHARED_BUS)—Offset E0h

This register is optional. The devices on shared bus are not intended to be controlled by the Standard Host Driver. This is because shared bus configuration depends on a host system; the devices on shared bus may be controlled by a specific driver of a host system.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h

Bit positions: 31, 28, 24, 20, 16, 12, 8, 4, 0

RSVD0	pwr_ctrl	RSVD1	int_pin	RSVD2	clk_pin	RSVD3	bus_width	RSVD4	num_int_pin	RSVD5	num_clk_pin
0	0 0 0 0 0 0 0	0	0 0 0	0	0 0 0	0	0 0 0 0 0 0 0	0	0 0 0	0	0 0 0

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**RSVD0:** Reserved
30:24	0h RW	**Back-End Power Control (pwr_ctrl):** Each bit of this field controls back-end power supply for an embedded device. Host interface voltage (VDDH) is not controlled by this field. The number of devices supported is specified by **Number of Clock Pins**, and a maximum of 7 devices can be controlled. • D24 Back-end Power Control for Device 1 • D25 Back-end Power Control for Device 2 • D26 Back-end Power Control for Device 3 • D27 Back-end Power Control for Device 4 • D28 Back-end Power Control for Device 5 • D29 Back-end Power Control for Device 6 • D30 Back-end Power Control for Device 7 The function of each bit is defined as follows: • 0 = Back-end Power is Off • 1 = Back-end Power is Supplied Back-End power control is effective for embedded memory devices in the Sleep State that support the Sleep command (CMD14) to reduce power consumption and embedded SDIO devices when IOEx is set to 0.
23	0b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22:20	0h RW	**Interrupt Pin Select (int_pin):** Interrupt pin inputs are enabled by this field. Enable of unsupported interrupt pin is meaningless. • 000b = Interrupt is detected by theInterrupt Cycle. • xx1b = INT_A is enabled • x1xb = INT_B is enabled • 1xxb = INT_C is enabled
19	0b RO	**RSVD2:** Reserved
18:16	0h RW	**Clock Pin Select (clk_pin):** One of clock pin outputs is selected by this field. Selection of unsupported clock pins is meaningless. Refer to Figure 2-38 for the timing of clock outputs. • 000b = Clock Pins are disabled • 001b = CLK[1] is selected • 010b = CLK[2] is selected • . . . • 111b = CLK[7] is Selected
15	0b RO	**RSVD3:** Reserved
14:8	0h RO	**Bus Width Preset (bus_width):** Shared bus supports mixing of 4-bit and 8-bit bus width devices. Each bit of this field specifies the bus width for each embedded device. The number of devices supported is specified by Number of Clock Pins, and a maximum of 7 devices are supported. This field is effective when multiple devices are connected to a shared bus (Slot Type is set to 10b in the Capabilities register). In the other case, Extended Data Transfer Width in the Host Control 1 register is used to select 8-bit bus width. As use of 1-bit mode is not intended for shared bus, Data Transfer Width in the Host Control 1 register should be set to 1. • D24 = Bus width preset for Device 1 • D25 = Bus width preset for Device 2 • D26 = Bus width preset for Device 3 • D27 = Bus width preset for Device 4 • D28 = Bus width preset for Device 5 • D29 = Bus width preset for Device 6 • D30 = Bus width preset for Device 7 The function of each bit is defined as follows: • 0 = 4 bit buswidth mode • 1 = 8 bit buswidth mode
7:6	0b RO	**RSVD4:** Reserved
5:4	0h RO	**Number of Interrupt Pins (num_int_pin):** This field indicates support of interrupt input pins for shared bus system. Three asynchronous interrupt pins are defined, INT_A#, INT_B# and INT_C#. Which interrupt pin is used is determined by the system. Each one is driven by open drain and then wired OR connection is possible. • 00b = Interrupt Input Pin is not supported • 01b = INTA is Supported • 10b = INTA and INTB are supported • 11b = INTA, INTB and INTC are supported
3	0b RO	**RSVD5:** Reserved
2:0	0h RO	**Number of Clock Pins (num_clk_pin):** This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported. Shared bus is supported by specific system. Then the Standard Host Driver does not support control of these clock pins. • 000b Shared bus is not supported • 001b 1 SDCLK pin is supported • 010b 2 SDCLK pins are supported • . . . • 111b 7 SDCLK pins are supported

16.8.37 SPI Interrupt Support Register (SPI_INT_SUP)—Offset F0h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
spi_int_support							

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**SPI Interrupt Support (spi_int_support):** This bit is set to indicate the assertion of interrupts in the SPI mode at any time, irrespective of the status of thecard select (CS) line. If this bit is zero, then SDIO card can only assert the interrupt line in the SPI mode when the CS line is asserted.

16.8.38 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved								int_sig_slot							

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Reserved (reserved):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Interrupt Signal For Each Slot (int_sig_slot):** These status bits indicate the logical OR of Interrupt Signal and Wakeup Signal for each slot. A maximum of 8 slots can be defined. If one interrupt signal is associated with multiple slots, the Host Driver can know which interrupt is generated by reading these status bits. By a power on reset or by setting Software Reset For All, the interrupt signal shall be de-asserted and this status shall read 00h. • Bit 00 = Slot 1 • Bit 01 = Slot 2 • Bit 02 = Slot 3 • .... • Bit 07 = Slot 8

16.8.39 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: B502h

15			12				8				4				0
1	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0
vend_ver_num								spec_ver_num							

Bit Range	Default & Access	Field Name (ID): Description
15:8	b5h RO	**Vendor Version Number (vend_ver_num):** This status is reserved for the vendor version number. The Host Driver should not use this status.
7:0	02h RO	**Specification Version Number (spec_ver_num):** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. • 00h = SD Host Specification Version 1.00 • 01h = SD Host Specification Version 2.00, Including the feature of the ADMA and Test Register • 02h = SD Host Specification Version 3.00 • others = Reserved

16.9 eMMC 4.5 PCI Configuration Registers

Table 188. Summary of eMMC 4.5 PCI Configuration Registers—0/23/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 1871	00000000h
4–7h	4	"Status and Command Register (STATUSCOMMAND)—Offset 4h" on page 1872	00100000h
8–Bh	4	"Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h" on page 1873	00000000h
C–Fh	4	"Cache Line Size, Latency Timer, and Header Type Register (CLLATHEADERBIST)—Offset Ch" on page 1873	00000000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 1874	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 1875	00000000h
2C–2Fh	4	"Subsystem Vendor ID and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch" on page 1876	00000000h
30–33h	4	"Expansion ROM Base Address Register (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1876	00000000h
34–37h	4	"Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h" on page 1877	00000080h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 1877	00000100h
80–83h	4	"Power Management Capability ID Register (POWERCAPID)—Offset 80h" on page 1878	48030001h
84–87h	4	"Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 1878	00000008h
A0–A3h	4	"General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h" on page 1879	00000000h
A4–A7h	4	"General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h" on page 1880	00000000h
A8–ABh	4	"General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h" on page 1880	00000000h
AC–AFh	4	"General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh" on page 1880	00000000h
C0–C3h	4	"General Purpose Input Register (GEN_INPUT_REGRW)—Offset C0h" on page 1881	00000000h
F8–FBh	4	"Manufacturers ID Register (MANID)—Offset F8h" on page 1881	00000000h

16.9.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:23, F:0] + 0h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
DEVICEID				VENDORID				

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	0000h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

16.9.2 Status and Command Register (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:23, F:0] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0		RMA	RCA	Reserved1							CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a '1' to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0h RW/1C	**Received Target Abort (RCA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt; i.e., Bridge does not send Interrupt Assert message through the IOSF SideBand Channel. Reset value of this bit is 0.
9	0h RO	**Reserved4:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SERR# Enable (SERR_ENABLE):** This bit controls the sending of DO_SERR messages on IOSF SB.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridges response to downstream memory accesses. When set, accesses to the memory space of the device are enabled. Reset value of this bit is 0.
0	0h RO	**Reserved6:** Reserved.

16.9.3 Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
											CLASS_CODES																RID				

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** This register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Identifies the revision of a particular AHB device. This is tied to a strap at the top level.

16.9.4 Cache Line Size, Latency Timer, and Header Type Register (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:24	Bit 23	Bits 22:16	Bits 15:8	Bits 7:0
Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**Multifunction Device (MULFNDEV):** This bit is always 0 for non-fabric ports. For fabric ports it is driven from the fabric_mult_function strap. A value of 1 indicates a multifunction device; a value of 0 indicates a single function device.
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Doesnt apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesnt apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

16.9.5 Base Address Register (BAR)—Offset 10h

Each AHB device is a single function device with only a single BAR associated with it. Bits 31:4 indicate the Base Address register. Power-up software can determine how much address space the AHB Device requires by writing a value of all 1's to the register and then reading the value back. Bridge will return 0's in all don't-care address bits, effectively specifying the address space required. Unimplemented Base Address registers are hardwired to zero. This is the Size Indicator Read only bits of the register.

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:23, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:12	Bits 11:4	Bit 3	Bits 2:1	Bit 0
BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1s.

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RO	**Size Indicator (Read Only) (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0s.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this bar is not prefetchable.
2:1	0h RO	**Type (TYPE):** '00' indicates that the BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0 Indicates that this BAR is present in the memory space.

16.9.6 Base Address Register 1 (BAR1)—Offset 14h

Memory accesses to BAR1 region access the PCI configuration space for the LPIO device. BAR1 region is always 4K. However SW accesses through BAR1 should only access the regular PCI configuration space. BAR1 memory accesses which do not access a defined PCI configuration register are treated as accesses to a reserved register.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + 14h

Default: 00000000h

Bits	31:12	11:4	3	2:1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0
Field	BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register1 (BASEADDR1):** This field is present if BAR1 is enabled through private config space. If this register is disabled then this is RO and always returns 0.
11:4	00h RO	**Size Indicator1 (SIZEINDICATOR1):** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this bar is not prefetchable.
2:1	0h RO	**Type (TYPE1):** '00' indicates that the BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0 Indicates that this BAR is present in the memory space.

16.9.7 Subsystem Vendor ID and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. Th is register makes it possible for the operating environment to distinguish one audio subsystem from the other. This is a Read Write Once register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. This register enables the operating environment to distinguish one subsystem from the other. This is a Read Write Once register.

16.9.8 Expansion ROM Base Address Register (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
EXPANSION_ROM_BASE																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Expansion ROM Base Address (EXPANSION_ROM_BASE):** Value of all 0s indicates no support for Expansion ROM.

16.9.9 Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + 34h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Reserved0																								CAPPTR_POWER							

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. When PM capability is disabled, this register is 00h.

16.9.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
MAX_LAT								MIN_GNT								Reserved0				INTPIN				INTLINE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates that the device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates that the device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

16.9.11 Power Management Capability ID Register (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:23, F:0] + 80h

Default: 48030001h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 1 0 0	1 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Fields: PMESUPPORT, Reserved0, VERSION, NXTCAP, POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot. bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

16.9.12 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:23, F:0] + 84h

Default: 00000008h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0

Fields: Reserved0, PMESTATUS, Reserved1, PMEENABLE, Reserved2, NO_SOFT_RESET, Reserved3, POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit in this register.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for upstream decode on fabric ports.

16.9.13 General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:23, F:0] + A0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GEN_REG_RW1

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW1:** capabilities over-ride for the sd/sdio/emmc host controler (bits 31:0)

16.9.14 General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + A4h

Default: 00000000h

31	30:0
0	000 0000 0000 0000 0000 0000 0000 0000
CAP_REG_SEL	GEN_REG_RW2

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CAP_REG_SEL:** select if the capabilty will come from the GEN PCI register or from a hard wire
30:0	0h RW	**GEN_REG_RW2:** capabilities over-ride for the sd/sdio/emmc host controler (bits 62:32)

16.9.15 General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + A8h

Default: 00000000h

31:0
0000 0000 0000 0000 0000 0000 0000 0000
GEN_REG_RW3

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW3:** Reserved.

16.9.16 General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:23, F:0] + ACh

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GEN_REG_RW4

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GEN_REG_RW4:** Reserved.

16.9.17 General Purpose Input Register (GEN_INPUT_REGRW)—Offset C0h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:23, F:0] + C0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GEN_REG_INPUT_RW

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**GEN_REG_INPUT_RW:** Reserved.

16.9.18 Manufacturers ID Register (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:23, F:0] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

16.10 eMMC 4.5 Memory Mapped IO Registers

Table 189. Summary of eMMC 4.5 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SDMA System Address / Argument 2 Register (SYS_ADR)—Offset 0h" on page 1884	00000000h
4–5h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1885	0000h
6–7h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1886	0000h
8–Bh	4	"Argument 1 Register (ARGUMENT)—Offset 8h" on page 1887	00000000h
C–Dh	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1887	0000h
E–Fh	2	"Command Register (CMD)—Offset Eh" on page 1889	0000h
10–13h	4	"Response Register 0 (RESPONSE0)—Offset 10h" on page 1890	00000000h
14–17h	4	"Response Register 2 (RESPONSE2)—Offset 14h" on page 1891	00000000h
18–1Bh	4	"Response Register 4 (RESPONSE4)—Offset 18h" on page 1891	00000000h
1C–1Fh	4	"Response Register 6 (RESPONSE6)—Offset 1Ch" on page 1892	00000000h
20–23h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1892	00000000h
24–27h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1893	1FFF0000h
28–28h	1	"Host Control 1 Register (HOST_CTL)—Offset 28h" on page 1896	00h
29–29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1897	00h
2A–2Ah	1	"Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah" on page 1898	00h
2B–2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1899	00h
2C–2Dh	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1900	0000h
2E–2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1902	00h
2F–2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1903	00h
30–31h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1904	0000h
32–33h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1907	0000h
34–35h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1909	0000h
36–37h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1911	0000h
38–39h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1912	0000h
3A–3Bh	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1913	0000h
3C–3Fh	4	"Auto CMD12 Error Status Register and Host Control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1915	00000000h
40–43h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1916	00000000h
44–47h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1917	00000000h
48–4Bh	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1917	00000000h
50–51h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1918	0000h

Table 189. Summary of eMMC 4.5 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
52–53h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1919	0000h
54–54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1920	00h
58–5Bh	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1921	00000000h
70–73h	4	"Boot Timeout Control (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1922	00000000h
74–74h	1	"Debug Selection Register (DEBUG_SEL)—Offset 74h" on page 1922	00h
E0–E3h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1923	00000000h
F0–F0h	1	"SPI Interrupt Support Register (SPI_INT_SUP)—Offset F0h" on page 1925	00h
FC–FDh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1925	0000h
FE–FFh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1926	B502h

16.10.1 SDMA System Address / Argument 2 Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

sys_adr

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SDMA System Address (sys_adr): (1) SDMA System Address** This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at each boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates a DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the uppermost byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. **(2) Argument 2** This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without AMDA, the available block count value is limited by the Block Count register. 65535 blocks is the maximum value in this case.

16.10.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
tx_blk_size_12	boundary			tr_blk_size											

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW	**TX_BLK_SIZE_12 (tx_blk_size_12):** Transfer Block Size 12th bit. This bit is added to support 4Kb Data block transfer.

Bit Range	Default & Access	Field Name (ID): Description
14:12	000b RW	**Host SDMA Buffer Boundary (boundary):** The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at each boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. • 000b = 4K bytes (Detects A11 carry out) • 001b = 8K bytes (Detects A12 carry out) • 010b = 16K Bytes (Detects A13 carry out) • 011b = 32K Bytes (Detects A14 carry out) • 100b = 64K bytes (Detects A15 carry out) • 101b = 128K Bytes (Detects A16 carry out) • 110b = 256K Bytes (Detects A17 carry out) • 111b = 512K Bytes (Detects A18 carry out)
11:0	000h RW	**Transfer Block Size (tr_blk_size):** This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2 *Determining Buffer Block Length*). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. • 0800h = 2048 Bytes • . . . • 0200h = 512 Bytes • 01FFh = 511 Bytes • . . . • 0004h = 4 Bytes • 0003h = 3 Bytes • 0002h = 2 Bytes • 0001h = 1 Byte • 0000h = No data transfer

16.10.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
blk_count															

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Blocks Count For Current Transfer (blk_count):** This register is enabled when Block Count Enable in the Transfer Mode register is set to 1, and is valid only for multiple block transfers. The Host Driver shall set this register to a value between 1 and the maximum block count. The HC decrements the block count after each block transfer, and stops when the count reaches zero. Setting the block count to 0 results in no data blocks being transferred. This register should be accessed only when no transaction is executing (i.e., after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored. When saving transfer context as a result of a Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the HD shall restore the previously saved block count. • 0000h = Stop Count • 0001h = 1 block • 0002h = 2 blocks • . . . • FFFFh = 65535 blocks

16.10.4 Argument 1 Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

argument

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command Argument 1 (argument):** The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

16.10.5 Transfer Mode Register (TX_MODE)—Offset Ch

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data (Refer to Data Present Select in the Command register), or before issuing a Resume command. The Host Driver shall save the value of this register when the data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller shall implement write protection for this register during data transactions. Writes to this register shall be ignored when the Command Inhibit (DAT) in the Present State register is 1.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd							boot_en	spi_mode	cmd_comp_ata	blk_sel	data_tr_dir	auto_cmd_en		blk_count_en	dma_en

Bit Range	Default & Access	Field Name (ID): Description
15:9	00h RO	**Reserved (rsvd):** Reserved.
8	0b RW	**BOOT_EN (boot_en):** To start boot operation for MMC4.3 1 - To start boot mode 0 - Stop the boot read
7	0b RW	**SPI_MODE (spi_mode):** SPI mode enable bit. 1 - SPI mode 0 - SD mode
6	0b RW	**CMD_COMP_ATA (cmd_comp_ata):** Command Completion Signal Enable for CE-ATA Device. ???1??? - Device will send command completion Signal ???0??? - Device will not send command completion Signal
5	0b RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0b RW	**Data Transfer Direction Select (data_tr_dir):** This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller, and it is set to 0 for all other commands. • 1 = Read (Card to Host) • 0 = Write (Host to Card)
3:2	0b RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0b RW	**Block Count Enable (blk_count_en):** This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8). If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. • 1 = Enable • 0 = Disable
0	0b RW	**DMA Enable (dma_en):** This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). • 1 = DMA Data transfer • 0 = No data transfer or Non DMA data transfer

16.10.6 Command Register (CMD)—Offset Eh

The Host Driver shall check the Command Inhibit (DAT) bit and Command Inhibit (CMD) bit in the Present State register before writing to this register. Writing to the upper byte of this register triggers SD command generation. The Host Driver has the responsibility to write this register because the Host Controller does not protect for writing when Command Inhibit (CMD) is set.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd		cmd_index						cmd_type		data_pr_sel	cmd_index_chk_en	cmd_crc_chk_en	reserved	resp_type_sel	

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Rsvd (rsvd):** Reserved.
13:8	0h RW	**Command Index (cmd_index):** These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	00b RW	**Command Type (cmd_type):** There are three types of special commands: Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. **(1) Suspend Command** If the Suspend command succeeds, the Host Controller shall assume the SD Bus has been released and that it is possible to issue the next command, which uses the DAT line. The Host Controller shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the Host Controller shall maintain its current state, and the Host Driver shall restart the transfer by setting Continue Request in the Block Gap Control register. (Refer to 3.12.1 Suspend Sequence). **(2) Resume Command** The Host Driver re-starts the data transfer by restoring the registers in the range of 000-00Dh. (Refer to Figure 1-4 in section 1.6 for the register map.) The Host Controller shall check for busy before starting write transfers. **(3) Abort Command** If this command is set when executing a read transfer, the Host Controller shall stop reads to the buffer. If this command is set when executing a write transfer, the Host Controller shall stop driving the DAT line. After issuing the Abort command, the Host Driver should issue a software reset. (Refer to 3.8 Abort Transaction). • 11b = Abort -- CMD12, CMD52 for writing 'I/O Abort' in CCCR • 10b = Resume -- CMD52 for writing 'Function Select' in CCCR • 01b = Suspend -- CMD52 for writing 'Bus Suspend' in CCCR • 00b = Normal -- Other commands
5	0b RW	**Data Present Select (data_pr_sel):** This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38). (3) Resume command. • 1 = Data Present • 0 = No Data Present

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**Command Index Check Enable (cmd_index_chk_en):** If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. • 1 = Enable • 0 = Disable
3	0b RW	**Command CRC Check Enable (cmd_crc_chk_en):** If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) • 1 = Enable • 0 = Disable
2	0b RO	**Reserved (reserved):** Reserved.
1:0	0h RW	**Response Type Select (resp_type_sel):** • 00 = No Response • 01 = Response Length 136 • 10 = Response Length 48 • 11 = Response Length 48 check Busy after response

16.10.7 Response Register 0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.10.8 Response Register 2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0 0 0	0	0 0 0		0	0 0 0			0	0 0 0			0	0 0 0			0	0 0 0			0	0 0 0			0	0 0 0			0

cmd_resp (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.10.9 Response Register 4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0 0 0	0	0 0 0		0	0 0 0			0	0 0 0			0	0 0 0			0	0 0 0			0	0 0 0			0	0 0 0			0

cmd_resp (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.10.10 Response Register 6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

cmd_resp

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Command Response (cmd_resp):** The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

16.10.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

buf_data

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Buffer Data (buf_data):** The Host Controller buffer can be accessed through this 32-bit Data Port register. Refer to section 1.7.

16.10.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 1FFF0000h

31			28				24				20				16				12				8				4				0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved2			dat_sig_lvl				cmd_ln_sig_lvl	data_ln_sig_lvl				wr_prot_sw_pin_lvl	crd_det_pin_lvl	crd_st_stable	crd_ins	reserved1				buf_rd_en	buf_wr_en	rd_tx_active	wr_tx_active	reserved					dat_ln_active	cmd_inhibit_dat	cmd_inhibit_cmd

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (reserved2):** Reserved.
28:25	1111b RO	**DAT Line Signal Level (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. • D28 - DAT[7] • D27 - DAT[6] • D26 - DAT[5] • D25 - DAT[4]
24	1b RO	**CMD Line Signal Level (cmd_ln_sig_lvl):** This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	Fh RO	**DAT[3:0] Line Signal Level (data_ln_sig_lvl):** This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. • D23 = DAT[3] • D22 = DAT[2] • D21 = DAT[1] • D20 = DAT[0]
19	1b RO	**Write Protect Switch Pin Level (wr_prot_sw_pin_lvl):** The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP# pin. • 1 = Write enabled (SDWP#=1) • 0 = Write protected (SDWP#=0)
18	1b RO	**Card Detect Pin Level (crd_det_pin_lvl):** This bit reflects the inverse value of the SDCD# pin. Debouncing is not performed on this bit. This bit may be valid when Card State Stable is set to 1, but it is not guaranteed because of propagation delay. Use of this bit is limited to testing since it must be debounced by software. • 1 = Card present (SDCD#=0) • 0 = No card present (SDCD#=1)
17	1b RO	**Card State Stable (crd_st_stable):** This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. No Card state can be detected by this bit being set to 1 while Card Inserted is set to 0. The Software Reset For All in the Software Reset register shall not affect this bit. • 1 = No Card or Inserted • 0 = Reset or Debouncing

Bit Range	Default & Access	Field Name (ID): Description
16	1b RO	**Card Inserted (crd_ins):** This bit indicates whether a card has been inserted. The Host Controller shall debounce this signal so that the Host Driver will not need to wait for it to stabilize. Changing from 0 to 1 generates a Card Insertion interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register shall not affect this bit. If a card is removed while its power is on and its clock is oscillating, the Host Controller shall clear SD Bus Power in the Power Control register (Refer to Section 2.2.11) and SD Clock Enable in the Clock Control register (Refer to Section 2.2.14). When this bit is changed from 1 to 0, the Host Controller shall immediately stop driving CMD and DAT[3:0] (tri-state). In addition, the Host Driver should clear the Host Controller by the Software Reset For All in Software Reset register. The card detect is active regardless of the SD Bus Power. • 1 = Card Inserted • 0 = Reset or Debouncing or No Card
15:12	0h RO	**Reserved1 (reserved1):** Reserved.
11	0b RO	**Buffer Read Enable (buf_rd_en):** This status is used for non-DMA read transfers. The Host Controller may implement multiple buffers to transfer data efficiently. This read only flag indicates that valid data exists in the host side buffer. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when block data is ready in the buffer and generates the Buffer Read Ready interrupt. • 1 = Read enable • 0 = Read disable
10	0b RO	**Buffer Write Enable (buf_wr_en):** This status is used for non-DMA write transfers. The Host Controller can implement multiple buffers to transfer data efficiently. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready interrupt. The Host Controller should neither set Buffer Write Enable nor generate Buffer Write Ready Interrupt after the last block data is written to the Buffer Data Port Register. • 1 = Write enable • 0 = Write disable
9	0b RO	**Read Transfer Active (rd_tx_active):** This status is used for detecting completion of a read transfer. Refer to Section 3.12.3 for sequence details. This bit is set to 1 for either of the following conditions: • After the end bit of the read command. • When read operation is restarted by writing a 1 to Continue Request in the Block Gap Control register. This bit is cleared to 0 for either of the following conditions: • When the last data block as specified by block length is transferred to the System. • In case of ADMA2, end of read operation is designated by Descriptor Table. • When all valid data blocks in the Host Controller have been transferred to the System and no current block transfers are being sent as a result of the Stop At Block Gap Request being set to 1. A Transfer Complete interrupt is generated when this bit changes to 0. • 1 = Transferring data • 0 = No valid data

Bit Range	Default & Access	Field Name (ID): Description
8	0b RO	**Write Transfer Active (wr_tx_active):** This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the Host Controller. Refer to Section 3.12.4 for more details on the sequence of events. This bit is set in either of the following cases: • After the end bit of the write command. • When write operation is restarted by writing a 1 to Continue Request in the Block Gap Control register. This bit is cleared in either of the following cases: • After getting the CRC status of the last data block as specified by the transfer count (Single and Multiple) In case of ADMA2, transfer count is designated by Descriptor Table. • After getting the CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as the result of the Stop At Block Gap Request being set. This status is useful for the Host Driver in determining non DAT line commands can be issued during write busy. • 1 Transferring data • 0 No valid data
7:3	00h RO	**Reserved (reserved):** Reserved.
2	0b RO	**DAT Line Active (dat_ln_active):** This bit indicates whether one of the DAT lines on SD Bus is in use. (a) In the case of read transactions This status indicates whether a read transfer is executing on the SD Bus. Changing this value from 1 to 0 generates a Block Gap Event interrupt in the Normal Interrupt Status register, as the result of the Stop At Block Gap Request being set. Refer to Section 3.12.3 for details on timing. This bit shall be set in either of the following cases: • After the end bit of the read command. • When writing a 1 to Continue Request in the Block Gap Control register to restart a read transfer. This bit shall be cleared in either of the following cases: • When the end bit of the last data block is sent from the SD Bus to the Host Controller. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table. • When a read transfer is stopped at the block gap initiated by a Stop At Block Gap Request. The Host Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Host Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use suspend / resume function. (b) In the case of write transactions This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. Refer to Section 3.12.4 for sequence details. This bit shall be set in either of the following cases: • After the end bit of the write command. • When writing to 1 to Continue Request in the Block Gap Control register to continue a write transfer. This bit shall be cleared in either of the following cases: • When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive 'Not Busy'. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table. • When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request. (c) Command with busy This status indicates whether a command indicates busy (ex. erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command with busy and cleared when busy is de-asserted. Changing this bit from 1 to 0 generate a Transfer Complete interrupt in the Normal Interrupt Status register. Refer Figure 2-11 to Figure 2-13. • 1 = DAT Line Active • 0 = DAT Line Inactive

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Command Inhibit (DAT) (cmd_inhibit_dat):** This status bit is generated if either the DAT Line Active or the Read Transfer Active is set to 1. If this bit is 0, it indicates the Host Controller can issue the next SD Command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal Interrupt Status register. **Note:** The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. • 1 Cannot issue command which uses the DAT line • 0 Can issue command which uses the DAT line
0	0b RO	**Command Inhibit (CMD) (cmd_inhibit_cmd):** Command Inhibit (CMD) If this bit is 0, it indicates the CMD line is not in use and the Host Controller can issue a SD Command using the CMD line. cleared when the command response is received. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register. Even if the Command Inhibit (DAT) is set to 1, commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command Complete Interrupt in the Normal Interrupt Status register. If the Host Controller cannot issue the command because of a command conflict error (Refer to Command CRC Error in Section 2.2.18) or because of Command Not Issued By Auto CMD12 Error (Refer to Section 2.2.23), this bit shall remain 1 and the Command Complete is not set. • 1 Cannot issue command • 0 Can issue command using only CMD line

16.10.13 Host Control 1 Register (HOST_CTL)—Offset 28h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
crd_det_sig_sel	crd_det_tst_lvl	sd8_bit_mode	dma_sel		hi_spd_en	data_tx_wid	led_ctl

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**Card Detect Signal Selection (crd_det_sig_sel):** This bit selects source for the card detection. • 1 = The Card Detect Test Level is selected (for test purposes) • 0 = SDCD# is selected (for normal use) When the source for the card detection is switched, the interrupt should be disabled during the switching period by clearing the Interrupt Status/Signal Enable register in order to mask unexpected interrupt being caused by the glitch. The Interrupt Status/ Signal Enable should be disabled during the period of debouncing.

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**Card Detect Test Level (crd_det_tst_lvl):** This bit is enabled while the Card Detect Signal Selection is set to 1, and it indicates whether or not the card is inserted. • 1 = Card Inserted • 0 = No Card
5	0b RW	**SD8 Bit Mode (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	00b RW	**DMA Select (dma_sel):** One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. Use of selected DMA is determined by DMA Enable of the Transfer Mode register. • 00 = SDMA is selected • 01 = Reserved (New assignment is not allowed) • 10 = 32-bit Address ADMA2 is selected • 11 = Reserved (will be modified by Version 4.00)
2	0b RW	**High Speed Enable (hi_spd_en):** This bit is optional. Before setting this bit, the Host Driver shall check the High Speed Support in the Capabilities register. If this bit is set to 0 (default), the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock (up to 25MHz). If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock (up to 50MHz). If Preset Value Enable in the Host Control 2 register is set to 1, Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. • 1 = 4-bit mode • 0 = 1-bit mode
1	0b RW	**Data Transfer Width (data_tx_wid):** Reserved.
0	0b RW	**LED Control (led_ctl):** This bit selects the data width of the Host Controller. The Host Driver shall set it to match the data width of the SD card. • 1 = 4-bit mode • 0 = 1-bit mode

16.10.14 Power Control Register (PWR_CTL)—Offset 29h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd			hw_rst	sd_bus_volt_sel			sd_bus_pwr

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Rsvd (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**HW Reset (hw_rst):** Reserved.
3:1	0h RW	**SD Bus Voltage Select (sd_bus_volt_sel):** By setting these bits, the Host Driver selects the voltage level for the SD card. Before setting this register, the Host Driver shall check the Voltage Support bits in the Capabilities register. If an unsupported voltage is selected, the Host System shall not supply SD Bus voltage. • 111b = 3.3V (Typ.) • 110b = 3.0V (Typ.) • 101b = 1.8V (Typ.) • 100b 000b Reserved
0	0b RW	**SD Bus Power (sd_bus_pwr):** Before setting this bit, the SD Host Driver shall set SD Bus Voltage Select. If the Host Controller detects the No Card state, this bit shall be cleared. If this bit is cleared, the Host Controller shall immediately stop driving CMD and DAT[3:0] (tri-state) and drive SDCLK to low level (Refer to Section 2.2.14) For SD Controller, this bit controls the bus voltage to SDMMC3. For SDIO Controller, power to SDIO device on SDMMC2 is not controlled by this bit. GPIO register and pin can be used to controller the SDIO device power. For eMMC Controller, power to eMMC device on SDMMC1 is not controlled by this bit. GPIO register and pin or alternative solutions can be used. • 1 = Power on • 0 = Power off

16.10.15 Block Gap Control Register (_BLK_GAP_CTL)—Offset 2Ah

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd			drive_ccsd	int_blk_gap	rd_wait_ctl	cont_req	stp_blk_gap_req

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (rsvd):** Reserved.
4	0b RW	**DRIVE_CCSD (drive_ccsd):** If the driver set this bit (change from ???0??? to ???1???), Host controller will send command completion.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**Interrupt at Block Gap (int_blk_gap):** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. • 1 = Enabled • 0 = Disabled
2	0b RW	**Read Wait Control (rd_wait_ctl):** The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the DAT[2] line. Otherwise, the Host Controller has to stop the SD Clock to hold read data, which restricts commands generation. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1, otherwise DAT line conflict may occur. If this bit is set to 0, Suspend/Resume cannot be supported. • 1 = Enable Read Wait Control • 0 = Disable Read Wait Control
1	0b RW	**Continue Request (cont_req):** This bit is used to restart a transaction, which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At Block Gap Request to 0 and set this bit 1 to restart the transfer. The Host Controller automatically clears this bit in either of the following cases: • In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. • In the case of a write transaction, the Write Transfer Active changes from 0 to 1 as the write transaction restarts. Therefore, it is not necessary for Host Driver to set this bit to 0. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. • 1 = Restart • 0 = Not affect
0	0b RW	**Stop at Block Gap Request (stp_blk_gap_req):** This bit is used to stop executing read and write transaction at the next block gap for non-DMA, SDMA and ADMA transfers. The Host Driver shall leave this bit set Copyright 2002-2011 SD Association SD Host Controller Simplified Specification Version 3.00 44 to 1 until the Transfer Complete is set to 1. Clearing both Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. When Host Controller version is 1.00, the Host Driver can set this bit if the card supports Read Wait Control. When Host Controller version is 2.00 or later, the Host Driver can set this bit regardless of the card supports Read Wait Control. The Host Controller shall stop read transfer by using Read Wait or stopping SD clock. In case of write transfers in which the Host Driver writes data to the Buffer Data Port register, the Host Driver shall set this bit after all block data is written. If this bit is set to 1, the Host Driver shall not write data to Buffer Data Port register. This bit affects Read Transfer Active, Write Transfer Active, DAT Line Active and Command Inhibit (DAT) in the Present State register. Regarding detailed control of bits D01 and D00, refer to Section 3.8 and 3.12. • 1 = Stop • 0 = Transfer

16.10.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is mandatory for the Host Controller, but wakeup functionality depends on the Host Controller system hardware and software. The Host Driver shall maintain voltage on the SD Bus, by setting SD Bus Power to 1 in the Power Control register, when wakeup event via Card Interrupt is desired. Wakeup Event is not supported by Host Controller. Sideband wake via GPIO pin and register shall be used instead. During RTD3, GPIO register is readable and GPIO signal is routed to APIC.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					wakeup_en_sd_rm	wakeup_en_sd_ins	wakeup_en_crd_int

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.
2	0b RW	**Wakeup Event Enable On SD Card Removal (wakeup_en_sd_rm):** This bit enables wakeup event via Card Removal assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. • 1 = Enable • 0 = Disable
1	0b RW	**Wakeup Event Enable On SD Card Insertion (wakeup_en_sd_ins):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake Up Support) in CIS does not affect this bit. • 1 = Enable • 0 = Disable
0	0b RW	**Wakeup Event Enable On Card Interrupt (wakeup_en_crd_int):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. • 1 = Enable • 0 = Disable

16.10.17 Clock Control Register (CLK_CTL)—Offset 2Ch

At the initialization of the Host Controller, the Host Driver shall set the SDCLK Frequency Select according to the Capabilities register.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sdclk_freq_sel								upper_sdclk_freq_sel		rsvd			sd_clk_en	int_clk_stable	int_clk_en

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**SDCLK Frequency Select (sdclk_freq_sel):** This register is used to select the frequency of the SDCLK pin. The definition of this field is dependent on the Host Controller Version. **(1) 8-bit Divided Clock Mode** This mode is supported by the Host Controller Version 1.00 and 2.00. The frequency is not programmed directly, rather, this register holds the divisor of the Base Clock Frequency For SD Clock in the capabilities register. Only the following settings are allowed. **(1) 8-bit Divided Clock Mode** • 80h = base clock divided by 256 • 40h = base clock divided by 128 • 20h = base clock divided by 64 • 10h = base clock divided by 32 • 08h = base clock divided by 16 • 04h = base clock divided by 8 • 02h = base clock divided by 4 • 01h = base clock divided by 2 • 00h = base clock(10MHz and up) Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor, but it should not be set. The three default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register. • 400KHz divider value • 25MHz divider value • 50MHz divider value According to the Physical Layer Specification, the maximum SD Clock frequency is 25 MHz in normal speed mode and 50MHz in high speed mode, and shall never exceed this limit. The frequency of the SDCLK is set by the following formula: Clock Frequency = (Base Clock) / divisor Thus, choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. For example, if the Base Clock Frequency For SD Clock in the Capabilities register has the value 33MHz, and the target frequency is 25MHz, then choosing the divisor value of 01h will yield 16.5MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400KHz, the divisor value of 40h yields the optimal clock value of 258KHz. **(2) 10-bit Divided Clock Mode** Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits, and all divider values shall be supported. • 3FFh = 1/2046 Divided Clock • N = 1/2N Divided Clock (Duty 50%) • 002h = 1/4 Divided Clock • 001h = 1/2 Divided Clock • 000h = Base Clock (10MHz and up) • 3FFh = Base Clock * M / 1024 • .... • N - 1 = Base Clock * M / N • .... • 002h = Base Clock * M / 3 • 001h = Base Clock * M / 2 • 000h = Base Clock * M This field depends on setting of Preset Value Enable in the Host Control 2 register. If Preset Value Enable = 0, this field is set by Host Driver. If the Preset Value Enable = 1, this field is automatically set to a value specified in one of Preset Value registers.

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Upper Bits of SDCLK Frequency Select (upper_sdclk_freq_sel):** Host Controller Versions 1.00 and 2.00 do not support these bits and they are treated as 00b fixed value (ROC). Host Controller Version 3.00 shall support these bits to expand SDCLK Frequency Select to 10-bit. Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select.
5:3	0h RO	**Rsvd (rsvd):** Reserved.
2	0b RW	**SD Clock Enable (sd_clk_en):** The Host Controller shall stop SDCLK when writing this bit to 0. SDCLK Frequency Select can be changed when this bit is 0. Then, the Host Controller shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK=0). If the Card Inserted in the Present State register is cleared, this bit shall be cleared. • 1 = Enable • 0 = Disable
1	0b RO	**Internal Clock Stable (int_clk_stable):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. **Note:** This is useful when using PLL for a clock oscillator that requires setup time. • 1 = Ready • 0 = Not Ready
0	0b RW	**Internal Clock Enable (int_clk_en):** This bit is set to 0 when the Host Driver is not using the Host Controller, or when the Host Controller awaits a wakeup event. The Host Controller should stop its internal clock to go to a very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the Host Controller shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection. • 1 = Oscillate • 0 = Stop

16.10.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

At the initialization of the Host Controller, the Host Driver shall set the Data Timeout Counter Value according to the Capabilities register.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
reserved				data_timeout_cnt_val			

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Rsvd (reserved):** Reserved.
3:0	0h RW	**Data Timeout Counter Value (data_timeout_cnt_val):** This value determines the interval by which DAT line timeouts are detected. For more information about timeout generation, refer to the Data Timeout Error in the Error Interrupt Status register. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). • 1111b Reserved • 1110b = TMCLK x 2^27 • .... • 0001b = TMCLK x 2^14 • 0000b = TMCLK x 2^13

16.10.19 Software Reset Register (SW_RST)—Offset 2Fh

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					sw_rst_dat_ln	sw_rst_cmd_ln	sw_rst_all

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**Software Reset For DAT Line (sw_rst_dat_ln):** Only part of data circuit is reset. DMA circuit is also reset. The following registers and bits are cleared by this bit: Buffer Data Port register • Buffer is cleared and initialized. Present State register • Buffer Read Enable • Buffer Write Enable • Read Transfer Active • Write Transfer Active • DAT Line Active • Command Inhibit (DAT) Block Gap Control register • Continue Request • Stop At Block Gap Request Normal Interrupt Status register • Buffer Read Ready • Buffer Write Ready • DMA Interrupt • Block Gap Event • Transfer Complete • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.
1	0b RW	**Software Reset For CMD Line (sw_rst_cmd_ln):** Only part of command circuit is reset. The following registers and bits are cleared by this bit: Present State register • Command Inhibit (CMD) Normal Interrupt Status register • Command Complete • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.
0	0b RW	**Software Reset For All (sw_rst_all):** This reset affects the entire Host Controller except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the Host Driver shall set this bit to 1 to reset the Host Controller. The Host Controller shall reset this bit to 0 when Capabilities registers are valid and the Host Driver can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the host driver should issue reset command and reinitialize the SD card. • 1 = Reset • 0 = Work When Auto or Dynamic Clock Gating is enabled for this controller, the Software Reset bit may require several reads before the bit clears.

16.10.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

The Normal Interrupt Status Enable affects reads of this register, but Normal Interrupt Signal Enable does not affect these reads. An interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1. Writing 1 to a bit of RW1C attribute clears it; writing 0 keeps the bit unchanged. Writing 1 to a bit of ROC attribute keeps the bit unchanged. More than one status can be cleared with a single register write. The Card Interrupt is cleared when the card stops asserting the interrupt; that is, when the Card Driver services the interrupt condition.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
err_int	boot_ter_int	boot_ck_rcv	re_tune	int_c	int_b	int_a	crd_int	crd_rm	crd_ins	buf_rd_rdy	buf_wr_rdy	dma_int	blk_gap_event	tx_comp	cmd_comp

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Error Interrupt (err_int):** If any of the bits in the Error Interrupt Status register are set, then this bit is set. Therefore the Host Driver can efficiently test for an error by checking this bit first. This bit is read only. • 1 = Error • 0 = No Error
14	0b RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0b RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0b RO	**Re-Tuning Event (re_tune):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. • 1 Re-Tuning should be performed • 0 Re-Tuning is not required
11	0b RO	**INT_C (int_c):** This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_C is detected • 0 = No interrupt is detected
10	0b RO	**INT_B (int_b):** This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_B is detected • 0 = No interrupt is detected
9	0b RO	**INT_A (int_a):** This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor. Refer to the Shared Bus Control register. • 1 = INT_A is detected • 0 = No interrupt is detected

Bit Range	Default & Access	Field Name (ID): Description
8	0b RO	**Card Interrupt (crd_int):** Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. When this status has been set and the Host Driver needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status Enable register may be set to 0 in order to clear the card interrupt statuses latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (It should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of shared bus, interrupt pins are used to detect interrupts. If 000b is set to Interrupt Pin Select in the Shared Bus Control register, this status is effective. Non-zero value is set to Interrupt Pin Select, INT_A, INT_B or INT_C is then used to device interrupts. • 1 = Generate Card Interrupt • 0 = No Card Interrupt
7	0b RW/1C	**Card Removal (crd_rm):** This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed. Because the card detect state may possibly be changed when the Host Driver clear this bit and interrupt event may not be generated. • 1 = Card removed • 0 = Card state stable or Debouncing
6	0b RW/1C	**Card Insertion (crd_ins):** This status is set if the Card Inserted in the Present State register changes from 0 to 1. When the Host Driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed, because the card detect state may possibly be changed when the Host Driver clears this bit and interrupt event may not be generated. • 1 Card inserted • 0 Card state stable or Debouncing
5	0b RW/1C	**Buffer Read Ready (buf_rd_rdy):** This status is set if the Buffer Read Enable changes from 0 to 1. Refer to the Buffer Read Enable in the Present State register. While performing tuning procedure (Execute Tuning is set to 1), Buffer Read Ready is set to 1 for every CMD19 execution. • 1 = Ready to read buffer • 0 = Not ready to read buffer
4	0b RW/1C	**Buffer Write Ready (buf_wr_rdy):** This status is set if the Buffer Write Enable changes from 0 to 1. Refer to the Buffer Write Enable in the Present State register. • 1 = Ready to write buffer • 0 = Not ready to write buffer
3	0b RW/1C	**DMA Interrupt (dma_int):** This status is set if the Host Controller detects the Host SDMA Buffer boundary during transfer. Refer to the Host SDMA Buffer Boundary in the Block Size register. Other DMA interrupt factors may be added in the future. In case of ADMA, by setting Int field in the descriptor table, Host Controller generates this interrupt. Suppose that it is used for debugging. This interrupt shall not be generated after the Transfer Complete. • 1 = DMA Interrupt is generated • 0 = No DMA Interrupt
2	0b RW/1C	**Block Gap Event (blk_gap_event):** If the Stop At Block Gap Request in the Block Gap Control register is set, this bit is set when both a read / write transaction is stopped at a block gap. If Stop At Block Gap Request is not set to 1, this bit is not set to 1. **(1) In the case of a Read Transaction** This bit is set at the falling edge of the DAT Line Active Status, when the transaction is stopped at SD Bus timing. The Read Wait shall be supported in order to use this function. Refer to Section 3.12.3 for timing details. p]**(1) In the case of a Write Transaction** This bit is set at the falling edge of Write Transfer Active Status (after getting CRC status at SD Bus timing). Refer to Section 3.12.4 for more details on the sequence of events. • 1 = Transaction stopped at block gap • 0 = No Block Gap Event

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW/1C	**Transfer Complete (tx_comp):** This bit is set when a read / write transfer and a command with busy is completed. **(1) In the case of a Read Transaction** This bit is set at the falling edge of Read Transfer Active Status. This interrupt is generated in two cases. The first is when a data transfer is completed as specified by data length (After the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the Stop At Block Gap Request in the Block Gap Control register (After valid data has been read to the Host System). Refer to Section 3.12.3 for more details on the sequence of events. **(2) In the case of a Write Transaction** This bit is set at the falling edge of the DAT Line Active Status. This interrupt is generated in two cases. The first is when the last data is written to the SD card as specified by data length and the busy signal released. The second is when data transfers are stopped at the block gap by setting Stop At Block Gap Request in the Block Gap Control register and data transfers completed. (After valid data is written to the SD card and the busy signal released). Refer to Section 3.12.4 for more details on the sequence of events. **(3) In the case of a command with busy** This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit (DAT) in the Present State register. Refer to the spec for the relationship between Transfer Complete and Data Timeout Error. • 1 = Command execution is completed • 0 = Not complete While performing tuning procedure (Execute Tuning is set to 1), Transfer Complete is not set to 1.
0	0b RW/1C	**Command Complete (cmd_comp):** This bit is set when get the end bit of the command response. Auto CMD12 and Auto CMD23 consist of two responses. Command Complete is not generated by the response of CMD12 or CMD23 but generated by the response of a read/write command. Refer to Command Inhibit (CMD) in the Present State register for how to control this bit. Command Timeout Error has higher priority than Command Complete. If both bits are set to 1, it can be considered that the response was not received correctly. For a tabular description of the relationship between these two bits, refer to the description of Command Complete in the spec. • 1 = Command complete • 0 = No command complete

16.10.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Signals defined in this register can be enabled by the Error Interrupt Status Enable register, but not by the Error Interrupt Signal Enable register. The interrupt is generated when the Error Interrupt Signal Enable is enabled and at least one of the statuses is set to 1. Writing to 1 clears the bit, and writing to 0 keeps the bit unchanged. More than one status can be cleared at the one register write.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
vend_spec_err_status	boot_cmd_timeout_err	ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_index_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW	**Vendor Specific Error Status (vend_spec_err_status):** Reserved.
14	0b RW	**Boot Command Timeout Error (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0b RW	**CEATA Error (ceata_err):** Occurs when ATA command termination has occured due to an error condition the device has encountered.
12	0b RW	**Target Response Error (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction).
11:10	0h RO	**Reserved (rsvd):** Reserved.
9	0b RW	**ADMA Error (adma_err):** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. In addition, the Host Controller generates this Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. **ADMA Error State** in the ADMA Error Status indicates that an error occurs in ST_FDS state.The Host Driver may find that Valid bit is not set at the error descriptor. • 0 = error • 1 = no error
8	0b RW	**Auto CMD12 Error (cmd12_err):** Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. • 1 = error • 0 = no error
7	0b RW	**Current Limit Error (cur_limit_err):** By setting the **SD Bus Power** bit in the Power Control register, the Host Controller is requested to supply power for the SD Bus. If the Host Controller supports the Current Limit function, it can be protected from an illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the Host Controller is not supplying power to SD card due to some failure. Reading 0 means that the Host Controller is supplying power and no error has occurred. The Host Controller may require some sampling time to detect the current limit. If the Host Controller does not support this function, this bit shall always be set to 0. • 1 = power fail • 0 = no error
6	0b RW	**Data End Bit Error (data_end_bit_err):** Occurs either when detecting 0 at the end bit position of read data which uses the DAT line or at the end bit position of the CRC Status. • 1 = error • 0 = no error
5	0b RW	**Data CRC Error (data_crc_err):** Occurs when detecting CRC error when transferring read data which uses the **DAT** line or when detecting the Write CRC status having a value of other than 010b.
4	0b RW	**Data Timeout Error (data_timeout_err):** This bit is set when detecting one of following timeout conditions. • Busy timeout for R1b,R5b type • Busy timeout after Write CRC status • Write CRC Status timeout • Read Data timeout • 1 = time out • 0 = no error

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**Command Index Error (cmd_index_err):** This bit is set if a Command Index error occurs in the command response. • 1 = error • 0 = no error
2	0b RW	**Command End Bit Error (cmd_end_bit_err):** This bit is set when detecting that the end bit of a command response is 0. • 1 = End Bit Error generated • 0 = no error
1	0b RW	**Command CRC Error (cmd_crc_err): Command CRC Error** is generated in two cases. If a response is returned and the **Command Timeout Error** is set to 0(indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller shall abort the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict (refer to tabular data in the spec. that explains the relationship between **Command CRC Error** and **Command Timeout Error**). • 1 = CRC Error Generated. • 0 = no error
0	0b RW	**Command Timeout Error (cmd_timeout_err):** This bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict (in which case **Command CRC Error** shall also be set, as shown in tabular data in the spec that explains the relationship between this bit and **Command CRC Error**) this bit shall be set without waiting for 64 SD clock cycles, because the command will be aborted by the Host Controller. • 1 = time out • 0 = no Error

16.10.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Setting to 1 enables Interrupt Status. **Implementation Note:** The Host Controller may sample the card interrupt signal during interrupt period, and may hold its value in the flip-flop. If the **Card Interrupt Status Enable** is set to 0, the Host Controller shall clear all internal signals regarding Card Interrupt.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

Bit	Default	Field
15	0	fixed_0
14:11	0 0 0 0	rsvd
10	0	boot_term_int_en
9	0	boot_ack_rcv_en
8	0	crd_int_stat_en
7	0	crd_rm_stat_en
6	0	crd_ins_stat_en
5	0	buf_rd_rdy_stat_en
4	0	buf_wr_rdy_stat_en
3	0	dma_int_stat_en
2	0	blk_gap_event_stat_en
1	0	tx_comp_stat_en
0	0	cmd_comp_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Fixed to 0 (fixed_0):** The Host Driver shall control error interrupts using the Error Interrupt Status Enable register.
14:11	0h RO	**Reserved (rsvd):** Reserved.
10	0b RW	**Boot Term Interrupt Enable (boot_term_int_en):** 0 = Masked.
9	0b RW	**Boot Acknowledge Receive Enable (boot_ack_rcv_en):** 0 = Masked
8	0b RW	**Card Interrupt Status Enable (crd_int_stat_en):** If this bit is set to 0, the Host Controller shall clear interrupt request to the System. The **Card Interrupt** detection is stopped when this bit is cleared, and restarted when this bit is set to 1. The Host Driver may clear the **Card Interrupt Status Enable** before servicing the Card Interrupt, and may set this bit again after all interrupt requests from the card are cleared, to prevent inadvertent interrupts. • 1 = enabled • 0 = masked
7	0b RW	**Card Removal Status Enable (crd_rm_stat_en):** • 1 = enabled • 0 = masked
6	0b RW	**Card Insertion Status Enable (crd_ins_stat_en):** [• 1 = enabled • 0 = masked
5	0b RW	**Buffer Read Ready Status Enable (buf_rd_rdy_stat_en):** • 1 = enabled • 0 = masked
4	0b RW	**Buffer Write Ready Status Enable (buf_wr_rdy_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**DMA Interrupt Status Enable (dma_int_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Block Gap Event Status Enable (blk_gap_event_stat_en):** • 1 = enabled • 0 = masked
1	0b RW	**Transfer Complete Status Enable (tx_comp_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Complete Status Enable (cmd_comp_stat_en):** • 1 = enabled • 0 = masked

16.10.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Setting to 1 enables interrupt status. **Implementation Note:** To detect CMD line conflict, the Host Driver must set both **Command Timeout Error Status Enable** and **Command CRC Error Status Enable to 1**.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_en	tgt_rsp_err_en	rsvd	tune_err_stat_en	adma_err_stat_en	cmd12_err_stat_en	cur_limit_err_stat_en	data_end_bit_err_stat_en	data_crc_err_stat_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15:14	0b RO	**Rsvd0 (rsvd0):** Reserved.
13	0b RW	**CEATA Error Enable (ceata_err_en):** 0 = masked
12	0b RW	**Target Response Error Enable (tgt_rsp_err_en):** 0 = masked
11	0b RO	**Rsvd (rsvd):** Reserved.
10	0b RW	**Tuning Error Status Enable (tune_err_stat_en):** • 1 = enabled • 0 = masked
9	0b RW	**ADMA Error Status Enable (adma_err_stat_en):** • 1 = enabled • 0 = masked
8	0b RW	**Auto CMD12 Error Status Enable (cmd12_err_stat_en):** • 1 = enabled • 0 = masked
7	0b RW	**Current Limit Error Status Enable (cur_limit_err_stat_en):** • 1 = enabled • 0 = masked
6	0b RW	**Data End Bit Error Status Enable (data_end_bit_err_stat_en):** • 1 = enabled • 0 = masked

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**Data CRC Error Status Enable (data_crc_err_stat_en):** • 1 = enabled • 0 = masked
4	0b RW	**Data Timeout Error Status Enable (data_timeout_err_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**Command Index Error Status Enable (cmd_ind_err_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Command End Bit Error Status Enable (cmd_end_bit_err_stat_en):** • 1 = enabled • 0 = masked
1	0b RW	**Command CRC Error Status Enable (cmd_crc_err_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Timeout Error Status Enable (cmd_timeout_err_stat_en):** • 1 = enabled • 0 = masked

16.10.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

This register is used to select which interrupt status is indicated to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	rsvd				boot_term_int_sig_en	boot_ack_rcv_sig_en	crd_int_sig_en	crd_rm_sig_en	crd_ins_sig_en	buf_rd_rdy_sig_en	buf_wr_rdy_sig_en	dma_int_sig_en	blk_gap_event_sig_en	tx_comp_sig_en	cmd_comp_sig_en

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Fixed to 0 (fixed_0):** The Host Driver shall control error interrupts using the Error Interrupt Signal Enable register.
14:11	0h RO	**Reserved (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0b RW	**Boot Terminate Interrupt Signal Enable (boot_term_int_sig_en):** 0 = masked
9	0b RW	**Boot Acknowledge Receive Signal Enable (boot_ack_rcv_sig_en):** 0 = masked
8	0b RW	**Card Interrupt Signal Enable (crd_int_sig_en):** • 1 = enabled • 0 = masked
7	0b RW	**Card Removal Signal Enable (crd_rm_sig_en):** • 1 = enabled • 0 = masked
6	0b RW	**Card Insertion Signal Enable (crd_ins_sig_en):** • 1 = enabled • 0 = masked
5	0b RW	**Buffer Read Ready Signal Enable (buf_rd_rdy_sig_en):** • 1 = enabled • 0 = masked
4	0b RW	**Buffer Write Ready Signal Enable (buf_wr_rdy_sig_en):** • 1 = enabled • 0 = masked
3	0b RW	**DMA Interrupt Signal Enable (dma_int_sig_en):** • 1 = enabled • 0 = masked
2	0b RW	**Block Gap Event Signal Enable (blk_gap_event_sig_en):** • 1 = enabled • 0 = masked
1	0b RW	**Transfer Complete Signal Enable (tx_comp_sig_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Complete Signal Enable (cmd_comp_sig_en):** • 1 = enabled • 0 = masked

16.10.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

This register is used to select which interrupt status is sent to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err_sig_en	tgt_err_rsp_sig_en	rsvd	tune_err_sig	adma_err_sig_en	cmd12_err_sig_en	cur_limit_err_sig_en	data_end_bit_err_sig_en	data_crc_err_sig_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15:14	0b RO	**Rsvd0 (rsvd0):** Reserved.
13	0b RW	**CEATA_Error Signal Enable (ceata_err_sig_en):** 0 = masked
12	0b RW	**Target Error Response Signal Enable (tgt_err_rsp_sig_en):** 0 = masked
11	0b RO	**Reserved (rsvd):** Reserved.
10	0b RW	**Tuning Error Signal Enable (tune_err_sig):** • 1 = enabled • 0 = masked
9	0b RW	**ADMA Error Signal Enable (adma_err_sig_en):** • 1 = enabled • 0 = masked
8	0b RW	**Auto CMD12 Error Signal Enable (cmd12_err_sig_en):** • 1 = enabled • 0 = masked
7	0b RW	**Current Limit Error Signal Enable (cur_limit_err_sig_en):** • 1 = enabled • 0 = masked
6	0b RW	**Data End Bit Error Signal Enable (data_end_bit_err_sig_en):** • 1 = enabled • 0 = masked
5	0b RW	**Data CRC Error Signal Enable (data_crc_err_sig_en):** • 1 = enabled • 0 = masked
4	0b RW	**Data Timeout Error Signal Enable (data_timeout_err_stat_en):** • 1 = enabled • 0 = masked
3	0b RW	**Command Index Error Signal Enable (cmd_ind_err_stat_en):** • 1 = enabled • 0 = masked
2	0b RW	**Command End Bit Error Signal Enable (cmd_end_bit_err_stat_en):** • 1 = enabled • 0 = masked

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**Command CRC Error Signal Enable (cmd_crc_err_stat_en):** • 1 = enabled • 0 = masked
0	0b RW	**Command Timeout Error Signal Enable (cmd_timeout_err_stat_en):** • 1 = enabled • 0 = masked

16.10.26 Auto CMD12 Error Status Register and Host Control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

Bits	Default	Field
31	0	preset_value
30	0	async_int
29:24	0 0 0 0 0 0	RSVD0
23	0	sampling_clock
22	0	execute_tuning
21:20	0 0	driver_strength
19	0	vl
18:16	0 0 0	uhs_mode
15:8	0 0 0 0 0 0 0 0	rsvd
7	0	cmd_not_iss_cmd12_err
6:5	0 0	rsvd1
4	0	cmd12_ind_err
3	0	cmd12_end_bit_err
2	0	cmd12_crc_err
1	0	cmd12_timeout_err
0	0	cmd12_not_exe

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Preset Value (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. • 1 = Automatic Selection by Preset Value are Enabled • 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.
30	0b RW	**Asynchronous Interrupt (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. Usage: It is recommended that Synchronous Interrupt mode be used for SDIO Controller by setting this be to '0'. If Asynchronous Interrupt Enable mode is used, it is required that this bit remain '0' until SD initialization sequence is complete. • 1 = Enabled • 0 = Disabled

Bit Range	Default & Access	Field Name (ID): Description
29:24	0b RO	**RSVD0:** Reserved
23	0b RW	**Sampling Clock (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared.
22	0b RW/AC	**Execute Tuning (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0. Refer to the spec for more detail about tuning procedure. • 1 = Execute Tuning • 0 = Not Tuned or Tuning Completed
21:20	0b RW	**Driver Strength (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit.
19	0b RW	**Voltage Regulator Control for I/O Cell (vl):** This bit controls voltage regulator for I/O cell.
18:16	0b RW	**UHS Mode Select (uhs_mode):** This field is used to select one of UHS-I modes.
15:8	0h RO	**Rsvd (rsvd):** Reserved.
7	0b RO	**Command Not Issued By Auto CMD12 Error (cmd_not_iss_cmd12_err):** Reserved.
6:5	0h RO	**Rsvd1 (rsvd1):** Reserved
4	0b RO	**Auto CMD12 Index Error (cmd12_ind_err):** Reserved.
3	0b RO	**Auto CMD12 End Bit Error (cmd12_end_bit_err):** Reserved.
2	0b RO	**Auto CMD12 CRC Error (cmd12_crc_err):** Reserved.
1	0b RO	**Auto CMD12 Timeout Error (cmd12_timeout_err):** Reserved.
0	0b RO	**Auto CMD12 Not Executed (cmd12_not_exe):** Reserved.

16.10.27 Capabilities Register (CAPABILITIES)—Offset 40h

This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initialization.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

capabilities

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**Capabilities (capabilities):** Reserved.

16.10.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

capabilities_2

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RO	**Capabilities 2 (capabilities_2):** Reserved.

16.10.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage. The value is meaningful if Voltage Support is set in the Capabilities register. If this information is supplied by the Host System via another method, all Maximum Current Capabilities register shall be 0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

rsvd	max_cur_1p8v	max_cur_3p0v	max_cur_3p3v

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (rsvd):** Reserved.
23:16	00h RO	**Maximum Current for 1.8V (max_cur_1p8v):** Reserved.
15:8	00h RO	**Maximum Current for 3.0V (max_cur_3p0v):** Reserved.
7:0	00h RO	**Maximum Current for 3.3V (max_cur_3p3v):** Reserved.

16.10.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved0	non_cmd12_err	reserved	cmd12_ind_err	cmd12_end_bit_err	cmd12_crc_err	cmd12_timeout_err	cmd12_not_exe

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Reserved 0 (reserved0):** Reserved.
7	0b RW	**Force Event for Command Not Issued By Auto CMD12 Error (non_cmd12_err):** • 1 = Interrupt is generated • 0 = No Interrupt
6:5	00b RO	**Reserved (reserved):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**Force Event for Auto CMD12 Index Error (cmd12_ind_err):** • 1 = Interrupt is generated • 0 = No Interrupt
3	0b RW	**Force Event for Auto CMD12 End Bit Error (cmd12_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
2	0b RW	**Force Event for Auto CMD12 CRC Error (cmd12_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
1	0b RW	**Force Event for Auto CMD12 Timeout Error (cmd12_timeout_err):** • 1 = Interrupt is generated • 0 = No Interrupt
0	0b RW	**Force Event for Auto CMD12 Not Executed (cmd12_not_exe):** • 1 = Interrupt is generated • 0 = No Interrupt

16.10.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Error Interrupt Status register can be written. The effect of a write to this address will be reflected in the Error Interrupt Status Register if the corresponding bit of the Error Interrupt Status Enable Register is set.

- Writing 1 : set each bit of the Error Interrupt Status Register
- Writing 0 : no effect

Note: By setting this register, the Error Interrupt can be set in the Error Interrupt Status register. In order to generate interrupt signal, both the Error Interrupt Status Enable and Error Interrupt Signal Enable shall be set.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_ind_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15:14	00b RO	**Reserved 0 (rsvd0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13	0b RW	**Force Event for CEATA Error (ceata_err):** Reserved.
12	0b RW	**Force Event for Target Response Error (tgt_rsp_err):** Reserved.
11:10	0h RO	**Reserved (rsvd):** Reserved.
9	0b RW	**Force Event for ADMA Error (adma_err):** • 1 = Interrupt is generated • 0 = No Interrupt
8	0b RW	**Force Event for Auto CMD12 Error (cmd12_err):** • 1 = Interrupt is generated • 0 = No Interrupt
7	0b RW	**Force Event for Current Limit Error (cur_limit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
6	0b RW	**Force Event for Data End Bit Error (data_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
5	0b RW	**Event for Data CRC Error (data_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
4	0b RW	**Event for Data Timeout Error (data_timeout_err):** • 1 = Interrupt is generated • 0 = No Interrupt
3	0b RW	**Force Event for Command Index Error (cmd_ind_err):** • 1 = Interrupt is generated • 0 = No Interrupt
2	0b RW	**Force Event for Command End Bit Error (cmd_end_bit_err):** • 1 = Interrupt is generated • 0 = No Interrupt
1	0b RW	**Force Event for Command CRC Error (cmd_crc_err):** • 1 = Interrupt is generated • 0 = No Interrupt
0	0b RW	**Force Event for Command Timeout Error (cmd_timeout_err):** • 1 = Interrupt is generated • 0 No Interrupt

16.10.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

When ADMA Error Interrupt occurs, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address Register holds the address around the error descriptor. To recover from the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows:

- ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address
- ST_FDS: Current location set in the ADMA System Address register is the error descriptor address
- ST_CADR: This sate is never set because do not generate ADMA error in this state.

- ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address

The Host Controller generates the ADMA Error Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. In this case, ADMA Error State indicates that an error occurs at ST_FDS state. The Host Driver may find that the Valid bit is not set in the error descriptor.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					adma_len_mis_err	adma_err_state	

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (rsvd):** Reserved.
2	0b RO	**ADMA Length Mismatch Error (adma_len_mis_err):** This error occurs in the following 2 cases. • While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. • Total data length can not be divided by the block length. • 1 = Error • 0 = No Error
1:0	00b RO	**ADMA Error State (adma_err_state):** This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates '10' because ADMA never stops in this state. Refer to the spec for tabular information about the relationship between this field and SYS_SDR register.

16.10.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

adma_sys_addr

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ADMA System Address (adma_sys_addr):** Reserved.

16.10.34 Boot Timeout Control (BOOT_TIMEOUT_CTRL)—Offset 70h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

time_cnt_val

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Boot Data Timeout Counter Value (time_cnt_val):** Reserved.

16.10.35 Debug Selection Register (DEBUG_SEL)—Offset 74h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd							debug_sel

Bit Range	Default & Access	Field Name (ID): Description
7:1	00h RO	**Reserved (rsvd):** Reserved.
0	0b WO	**Debug Select (debug_sel):** • 1 = cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out. • 0 = receiver module and fifo_ctrl module signals are probed out

16.10.36 Shared Bus Control Register (SHARED_BUS)—Offset E0h

This register is optional. The devices on shared bus are not intended to be controlled by the Standard Host Driver. This is because shared bus configuration depends on a host system; the devices on shared bus may be controlled by a specific driver of a host system.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0	pwr_ctrl							RSVD1	int_pin			RSVD2	clk_pin			RSVD3	bus_width							RSVD4		num_int_pin		RSVD5	num_clk_pin		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**RSVD0:** Reserved
30:24	0h RW	**Back-End Power Control (pwr_ctrl):** Each bit of this field controls back-end power supply for an embedded device. Host interface voltage (VDDH) is not controlled by this field. The number of devices supported is specified by **Number of Clock Pins**, and a maximum of 7 devices can be controlled. • D24 Back-end Power Control for Device 1 • D25 Back-end Power Control for Device 2 • D26 Back-end Power Control for Device 3 • D27 Back-end Power Control for Device 4 • D28 Back-end Power Control for Device 5 • D29 Back-end Power Control for Device 6 • D30 Back-end Power Control for Device 7 The function of each bit is defined as follows: • 0 = Back-end Power is Off • 1 = Back-end Power is Supplied Back-End power control is effective for embedded memory devices in the Sleep State that support the Sleep command (CMD14) to reduce power consumption and embedded SDIO devices when IOEx is set to 0.
23	0b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22:20	0h RW	**Interrupt Pin Select (int_pin):** Interrupt pin inputs are enabled by this field. Enable of unsupported interrupt pin is meaningless. • 000b = Interrupt is detected by theInterrupt Cycle. • xx1b = INT_A is enabled • x1xb = INT_B is enabled • 1xxb = INT_C is enabled
19	0b RO	**RSVD2:** Reserved
18:16	0h RW	**Clock Pin Select (clk_pin):** One of clock pin outputs is selected by this field. Selection of unsupported clock pins is meaningless. Refer to Figure 2-38 for the timing of clock outputs. • 000b = Clock Pins are disabled • 001b = CLK[1] is selected • 010b = CLK[2] is selected • . . . • 111b = CLK[7] is Selected
15	0b RO	**RSVD3:** Reserved
14:8	0h RO	**Bus Width Preset (bus_width):** Shared bus supports mixing of 4-bit and 8-bit bus width devices. Each bit of this field specifies the bus width for each embedded device. The number of devices supported is specified by Number of Clock Pins, and a maximum of 7 devices are supported. This field is effective when multiple devices are connected to a shared bus (Slot Type is set to 10b in the Capabilities register). In the other case, Extended Data Transfer Width in the Host Control 1 register is used to select 8-bit bus width. As use of 1-bit mode is not intended for shared bus, Data Transfer Width in the Host Control 1 register should be set to 1. • D24 = Bus width preset for Device 1 • D25 = Bus width preset for Device 2 • D26 = Bus width preset for Device 3 • D27 = Bus width preset for Device 4 • D28 = Bus width preset for Device 5 • D29 = Bus width preset for Device 6 • D30 = Bus width preset for Device 7 The function of each bit is defined as follows: • 0 = 4 bit buswidth mode • 1 = 8 bit buswidth mode
7:6	0b RO	**RSVD4:** Reserved
5:4	0h RO	**Number of Interrupt Pins (num_int_pin):** This field indicates support of interrupt input pins for shared bus system. Three asynchronous interrupt pins are defined, INT_A#, INT_B# and INT_C#. Which interrupt pin is used is determined by the system. Each one is driven by open drain and then wired OR connection is possible. • 00b = Interrupt Input Pin is not supported • 01b = INTA is Supported • 10b = INTA and INTB are supported • 11b = INTA, INTB and INTC are supported
3	0b RO	**RSVD5:** Reserved
2:0	0h RO	**Number of Clock Pins (num_clk_pin):** This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported. Shared bus is supported by specific system. Then the Standard Host Driver does not support control of these clock pins. • 000b Shared bus is not supported • 001b 1 SDCLK pin is supported • 010b 2 SDCLK pins are supported • . . . • 111b 7 SDCLK pins are supported

16.10.37 SPI Interrupt Support Register (SPI_INT_SUP)—Offset F0h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
spi_int_support							

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**SPI Interrupt Support (spi_int_support):** This bit is set to indicate the assertion of interrupts in the SPI mode at any time, irrespective of the status of thecard select (CS) line. If this bit is zero, then SDIO card can only assert the interrupt line in the SPI mode when the CS line is asserted.

16.10.38 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved								int_sig_slot							

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Reserved (reserved):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Interrupt Signal For Each Slot (int_sig_slot):** These status bits indicate the logical OR of Interrupt Signal and Wakeup Signal for each slot. A maximum of 8 slots can be defined. If one interrupt signal is associated with multiple slots, the Host Driver can know which interrupt is generated by reading these status bits. By a power on reset or by setting Software Reset For All, the interrupt signal shall be de-asserted and this status shall read 00h. • Bit 00 = Slot 1 • Bit 01 = Slot 2 • Bit 02 = Slot 3 • .... • Bit 07 = Slot 8

16.10.39 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:23, F:0] + 10h

Default: B502h

15			12				8				4				0
1	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0
vend_ver_num								spec_ver_num							

Bit Range	Default & Access	Field Name (ID): Description
15:8	b5h RO	**Vendor Version Number (vend_ver_num):** This status is reserved for the vendor version number. The Host Driver should not use this status.
7:0	02h RO	**Specification Version Number (spec_ver_num):** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. • 00h = SD Host Specification Version 1.00 • 01h = SD Host Specification Version 2.00, Including the feature of the ADMA and Test Register • 02h = SD Host Specification Version 3.00 • others = Reserved

17 Serial ATA (SATA)

The SoC has one integrated SATA host controller that supports independent DMA operation on up to 2 ports and supports data transfer rates of 1.5 Gb/s (150 MB/s) and 3.0 Gb/s (300 MB/s). The SATA controller contains two modes of operation—a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities.

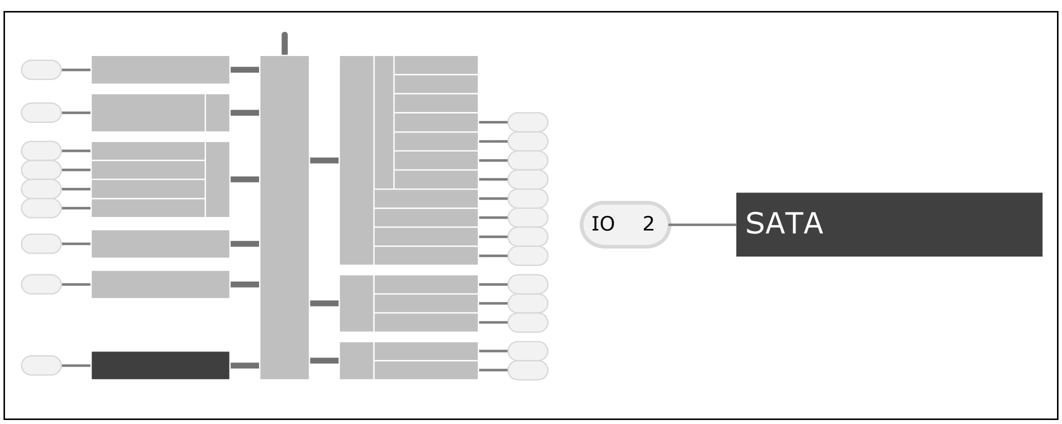
The SoC supports the Serial ATA Specification, Revision 2.6. The SoC also supports several optional sections of the SATA Revision 2.0 Specifications: Extensions to Serial ATA 1.0 Specification, Revision 1.0 (AHCI support is required for some elements).

The SATA controllers feature two sets of interface signals (ports) that can be independently enabled or disabled (they cannot be tri-stated or driven low). Each interface is supported by an independent DMA controller.

The SATA controllers interact with an attached mass storage device through a register interface that is equivalent to that presented by a traditional IDE host adapter. The host software follows existing standards and conventions when accessing the register interface and follows standard command protocol conventions.

Note 1. SATA DevSlp (**Device Sleep**) is not part of revision 2.6 of the SATA specification, with which this processor is compliant. As such, any DEVSLP functionality of this processor is not specification compliant and should not be used.

Note 2. SATA interface transfer rates are independent of UDMA mode settings. SATA interface transfer rates will operate at the bus's maximum speed, regardless of the UDMA mode reported by the SATA device or the system BIOS.



17.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 190. Signals

Signal Name	Direction Plat. Power	Description
SATA_GP[0]	I V1P8S	**Serial ATA 0 General Purpose:** This is an input pin which can be configured as an interlock switch or as a general purpose I/O, depending on the platform. When used as an interlock switch status indication, this signal should be driven to '0' to indicate that the switch is closed, and to '1' to indicate that the switch is open.
SATA_GP[1]	I V1P8S	**Serial ATA 1 General Purpose:** Same as above.
SATA_LED#	O V1P8S	**Serial ATA LED:** This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tristated, the LED is off.
SATA_TXP[1:0] SATA_TXN[1:0]	O VPCIESATA	**Serial ATA Port 1 and 0:** These are outbound high-speed differential signals to Port 1 and 0.
SATA_RXP[1:0] SATA_RXN[1:0]	I VPCIESATA	**Serial ATA Port 1 and 0:** These are inbound high-speed differential signals to Port 1 and 0.
SATA_RCOMP_P SATA_RCOMP_N	O	These pins are used to connect the external resistors used for Rcomp. Please contact your Intel representative for details.

17.2 Features

17.2.1 Supported Features

Table 191. SATA Feature List (Sheet 1 of 2)

Feature	Description
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers
Auto Activate for DMA	Collapses a DMA Setup then DMA Activate sequence into a DMA Setup only
Hot Plug Support	Allows for device detection without power being applied and ability to connect and disconnect devices without prior notification to the system
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot plug
3 Gb/s Transfer Rate	Capable of data transfers up to 3 Gb/s
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention

Table 191. SATA Feature List (Sheet 2 of 2)

Feature	Description
Host & Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states
Staggered Spin-Up	Enables the host to spin up hard drives sequentially to prevent power load problems on boot
Command Completion Coalescing	Reduces interrupt and completion overhead by allowing a specified number of commands to complete and then generating an interrupt to process the commands

Table 192. SATA/AHCI Feature Matrix

Feature	AHCI Disabled	AHCI Enabled
Native Command Queuing (NCQ)	N/A	Supported
Auto Activate for DMA	N/A	Supported
Hot Plug Support	N/A	Supported
Asynchronous Signal Recovery	N/A	Supported
3 Gb/s Transfer Rate	Supported	Supported
ATAPI Asynchronous Notification	N/A	Supported
Host & Link Initiated Power Management	N/A	Supported
Staggered Spin-Up	Supported	Supported
Command Completion Coalescing	N/A	N/A

17.2.2 Theory of Operation

17.2.2.1 Standard ATA Emulation

The SoC contains a set of registers that shadow the contents of the legacy IDE registers. The behavior of the Command and Control Block registers, PIO, and DMA data transfers, resets, and interrupts are all emulated.

Note: The SoC will assert INTR when the master device completes the EDD command regardless of the command completion status of the slave device. If the master completes EDD first, an INTR is generated and BSY will remain '1' until the slave completes the command. If the slave completes EDD first, BSY will be '0' when the master completes the EDD command and asserts INTR. Software must wait for busy to clear (0) before completing an EDD command, as required by the ATA5 through ATA7 (T13) industry standards.

17.2.2.2 48-Bit LBA Operation

The SATA host controller supports 48-bit LBA through the host-to-device register FIS when accesses are performed using writes to the task file. The SATA host controller will ensure that the correct data is put into the correct byte of the host-to-device FIS.

There are special considerations when reading from the task file to support 48-bit LBA operation. Software may need to read all 16-bits. Since the registers are only 8-bits wide and act as a FIFO, a bit must be set in the device/control register, which is at offset 3F6h for primary and 376h for secondary (or their native counterparts).

If software clears Bit 7 of the control register before performing a read, the last item written will be returned from the FIFO. If software sets Bit 7 of the control register before performing a read, the first item written will be returned from the FIFO.

17.2.3 AHCI Operation

The SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers developed through a joint industry effort. AHCI defines transactions between the SATA controller and software and enables advanced performance and usability with SATA. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (such as, an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

The SoC supports all of the mandatory features of the *Serial ATA Advanced Host Controller Interface Specification*, Revision 1.3 and many optional features, such as hardware assisted native command queuing, aggressive power management, LED indicator support, and Hot-Plug through the use of interlock switch support (additional platform hardware and software may be required depending upon the implementation).

Note: For reliable device removal notification while in AHCI operation without the use of interlock switches (surprise removal), interface power management should be disabled for the associated port.

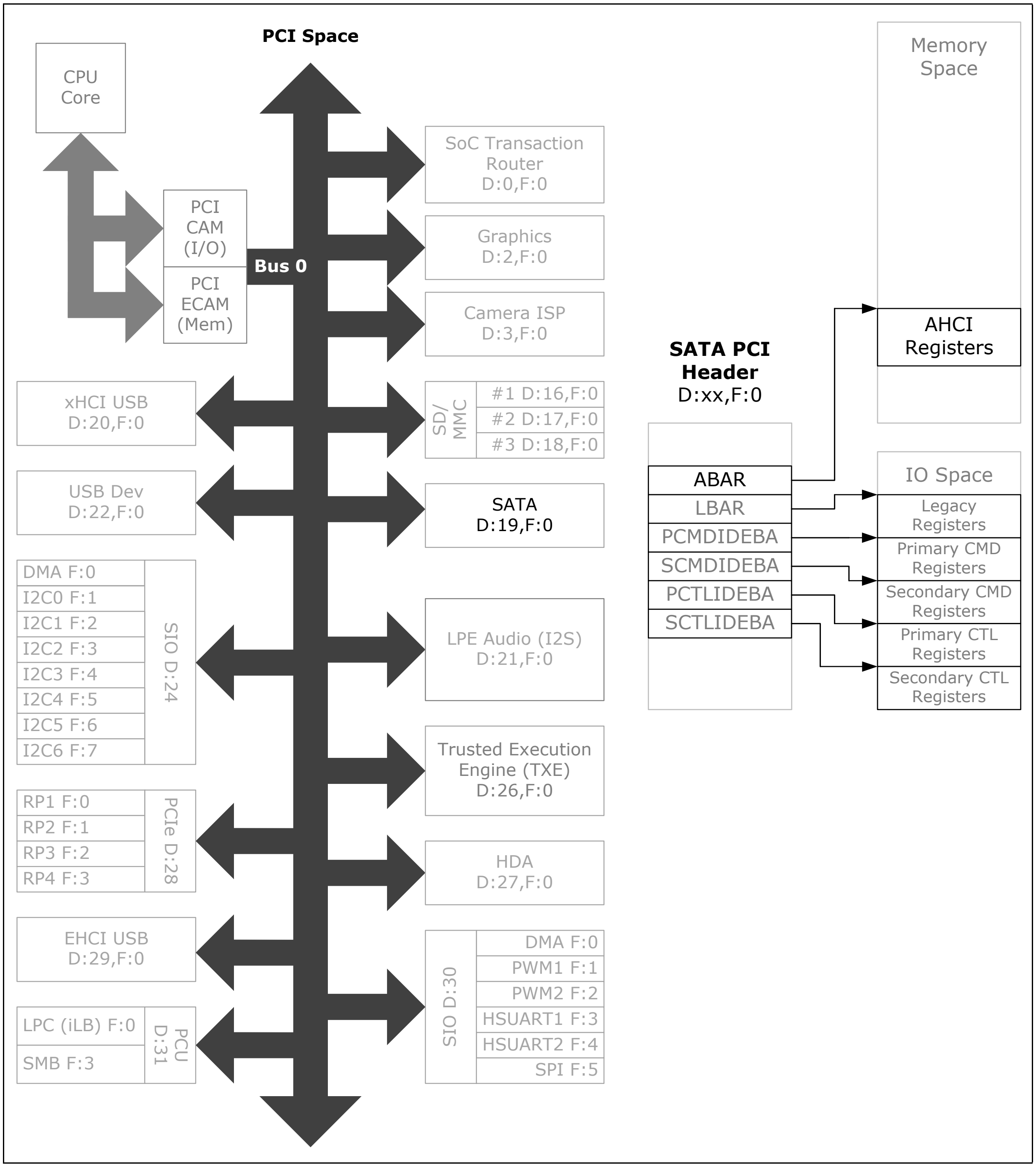
17.3 References

- Serial ATA Specification rev 2.6
- Serial ATA Advanced Host Controller Interface (AHCI) Specification rev 1.3
- Serial ATA II: Extensions to Serial ATA 1.0 Specification, Revision 1.0

17.4 Register Map

See Chapters 3 and 4 for additional information.

Figure 102. SATA Register Map



17.5 SATA PCI Configuration Registers

Table 193. Summary of SATA PCI Configuration Registers—0/19/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Identifiers (ID)—Offset 0h" on page 1933	0F208086h
4h	2	"Command (CMD)—Offset 4h" on page 1933	0000h
6h	2	"Device Status (STS)—Offset 6h" on page 1934	02B0h
8h	1	"Revision ID (RID)—Offset 8h" on page 1935	00h
9h	1	"Programming Interface (PI)—Offset 9h" on page 1936	8Ah
Ah	2	"Class Code (CC)—Offset Ah" on page 1936	0106h
Ch	1	"Cache Line Size (CLS)—Offset Ch" on page 1937	00h
Dh	1	"Master Latency Timer (MLT)—Offset Dh" on page 1937	00h
Eh	1	"Header Type (HTYPE)—Offset Eh" on page 1937	00h
10h	4	"Primary Command Block Base Address (PCMDBA)—Offset 10h" on page 1938	00000001h
14h	4	"Primary Control Block Base Address (PCTLBA)—Offset 14h" on page 1938	00000001h
18h	4	"Secondary Command Block Base Address (SCMDBA)—Offset 18h" on page 1939	00000001h
1Ch	4	"Secondary Control Block Base Address (SCTLBA)—Offset 1Ch" on page 1940	00000001h
20h	4	"Legacy IDE Base Address / AHCI Index Data Pair Base Address (LBAR)—Offset 20h" on page 1940	00000001h
24h	4	"AHCI Base Address/Serial ATA Index Data Pair Base Address (ABAR)—Offset 24h" on page 1941	00000000h
2Ch	4	"Sub System Identifiers (SS)—Offset 2Ch" on page 1942	00000000h
34h	1	"Capabilities Pointer (CAP)—Offset 34h" on page 1942	80h
3Ch	2	"Interrupt Information (INTR)—Offset 3Ch" on page 1942	0100h
3Eh	1	"Minimum Grant (MGNT)—Offset 3Eh" on page 1943	00h
3Fh	1	"Maximum Latency (MLAT)—Offset 3Fh" on page 1943	00h
40h	2	"Primary Timing (PTIM)—Offset 40h" on page 1944	0000h
42h	2	"Secondary Timing (STIM)—Offset 42h" on page 1945	0000h
44h	1	"Device 1 IDE Timing (D1TIM)—Offset 44h" on page 1946	00h
48h	1	"Synchronous DMA Control (Synchronous_DMA_Control)—Offset 48h" on page 1946	00h
4Ah	2	"Synchronous_DMA_Timing—Offset 4Ah" on page 1946	0000h
54h	4	"IDE I/O Configuration (IIOC)—Offset 54h" on page 1947	00000000h
70h	2	"PCI Power Management Capability ID (PID)—Offset 70h" on page 1947	A801h
72h	2	"Primary Command Block Base Address (PCMDBA)—Offset 10h" on page 1938	4003h
74h	2	"PCI Power Management Control and Status (PMCS)—Offset 74h" on page 1948	0008h
80h	2	"Message Signaled Interrupt Identifier (MID)—Offset 80h" on page 1949	7005h
82h	2	"Message Signaled Interrupt Message Control (MC)—Offset 82h" on page 1949	0000h
84h	4	"Message Signaled Interrupt Message Address (MA)—Offset 84h" on page 1950	00000000h
88h	2	"Message Signaled Interrupt Message Data (MD)—Offset 88h" on page 1950	0000h
90h	2	"Port Mapping Register (MAP)—Offset 90h" on page 1951	0420h

Table 193. Summary of SATA PCI Configuration Registers—0/19/0 (Continued)

Offset	Size	Register ID—Description	Default Value
92h	2	"Port Control and Status (PCS)—Offset 92h" on page 1952	0000h
94h	4	"Test Mode Register (TM)—Offset 94h" on page 1953	00000000h
9Ch	4	"SATA General Configuration (SATAGC)—Offset 9Ch" on page 1953	00000000h
A0h	1	"SATA Initialization Register Index (SIRI)—Offset A0h" on page 1955	00h
A4h	4	"SATA Initialization Register Data (SIRD)—Offset A4h" on page 1955	00000000h
A8h	4	"Serial ATA Capability Register 0 (SATACR0)—Offset A8h" on page 1955	00100012h
ACh	4	"Serial ATA Capability Register 1 (SATACR1)—Offset ACh" on page 1956	00000048h
B0h	2	"FLR Capability ID (FLRCID)—Offset B0h" on page 1957	0000h
B4h	2	"FLR Control (FLRCTL)—Offset B4h" on page 1957	0000h
D0h	4	"Scratch Pad (SP)—Offset D0h" on page 1957	00000000h
E0h	4	"BIST FIS Control/Status (BFCS)—Offset E0h" on page 1958	00000000h
E4h	4	"BIST FIS Transmit Data 1 (BFTD1)—Offset E4h" on page 1958	00000000h
E8h	4	"BIST FIS Transmit Data 2 (BFTD2)—Offset E8h" on page 1959	00000000h
F8h	4	"Manufacturing ID (MFID)—Offset F8h" on page 1959	08000FB1h

17.5.1 Identifiers (ID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **ID:** [B:0, D:19, F:0] + 0h

Default: 0F208086h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DID																VID															

Bit Range	Default & Access	Description
31:16	0F20h RO	**Device ID (DID):** The specific value is dependent on config bits and fuses. The value is product specific. VLV SATA DID can be within the range of 0F20-0F27 and 0F2E and 0F2F. However, since VLV SATA does not support RAID, DID can be either 0F20 or OF22.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel.

17.5.2 Command (CMD)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 16 bits) **CMD:** [B:0, D:19, F:0] + 4h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0					ID	FBE	SEE	WCC	PEE	VGA	MWIE	SCE	BME	MSE	IOSE

Bit Range	Default & Access	Description
15:11	0b RO	**RSVD0:** Reserved
10	0h RW	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# will not be generated. When cleared, internal INTx# is generated if there is an interrupt and MSI is not enabled.
9	0h RO	**Fast Back-to-Back Enable (FBE):** Reserved.
8	0h RW	**SERR# Enable (SEE):** When set to 1, the HBA is allowed to generate SERR# on DPD or SATAGC.URD event that is enabled for SERR# generation. When cleared to 0, it is not.
7	0h RO	**Wait Cycle Enable (WCC):** Reserved.
6	0h RW	**Parity Error Response Enable (PEE):** When set, the SATA Controller will corrupt the outbound DATA FIS CRC if a forwarded data parity error is indicated.
5	0h RO	**VGA Palette Snooping Enable (VGA):** Reserved.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved.
3	0h RO	**Special Cycle Enable (SCE):** Reserved.
2	0h RW	**Bus Master Enable (BME):** Controls the SATA Controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the SATA Controller's target memory space (for AHCI).
0	0h RW	**I/O Space Enable (IOSE):** Controls access to the SATA Controller's target I/O space.

17.5.3 Device Status (STS)—Offset 6h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

STS: [B:0, D:19, F:0] + 6h

Default: 02B0h

15			12				8				4				0
0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		DPD	FBC	RSVD0	RSV	CL	IS	RSVD1		

Bit Range	Default & Access	Description
15	0h RW/1C	**Detected Parity Error (DPE):** Set when the SATA Controller detects a parity error on its interface.
14	0h RW/1C	**Signaled System Error (SSE):** Set when SATA Controller generates an SERR#.
13	0h RW/1C	**Received Master-Abort Status (RMA):** Set when the SATA Controller receives a master abort to a cycle it generated.
12	0h RW/1C	**Received Target-Abort Status (RTA):** Set when the SATA Controller receives a target abort to a cycle it generated.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** Controls the device select time for the SATA Controller's PCI interface.
8	0h RW/1C	**Master Data Parity Error Detected (DPD):** Set when the SATA Controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set. This bit can only be set on read completions received from the backbone where there is a parity error.
7	1h RO	**Fast Back-to-Back Capable (FBC):** Reserved.
6	0b RO	**RSVD0:** Reserved
5	1h RO	**66 MHz Capable (RSV):** Reserved.
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA Controller.
3	0h RO	**Interrupt Status (IS):** Reflects the state of INTx# messages, IRQ14 or IRQ15. This bit is set when the interrupt is to be asserted. This bit is a 0 after the interrupt is cleared
2:0	0b RO	**RSVD1:** Reserved

17.5.4 Revision ID (RID)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

RID: [B:0, D:19, F:0] + 8h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Description
7:0	00h RO	**Revision ID (RID):** Indicates stepping of the host controller hardware.

17.5.5 Programming Interface (PI)—Offset 9h

This register definition depends on the CC.SCC field. When the CC.SCC is 01h(IDE mode), register definition corresponds to 1st table. When CC.SCC is 06h(AHCI mode), register definition follows the 2nd table.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PI: [B:0, D:19, F:0] + 9h

Default: 8Ah

7			4				0
1	0	0	0	1	0	1	0
BMS	RSVD0			SNC	SNE	PNC	PNE

Bit Range	Default & Access	Description
7	1h RO	**Bus Master Support (BMS):** Indicates the SATA Controller supports bus master operation.
6:4	0b RO	**RSVD0:** Reserved
3	1h RO	**Secondary Mode Native Capable (SNC):** Indicates that the secondary controller supports both legacy and native modes.
2	0h RW	**Secondary Mode Native Enable (SNE):** Determines the mode that the secondary channel is operating in. 0 corresponds to 'compatibility', 1 means PCI native. If this bit is set by SW, then the PNE bit must also be set by SW. While in theory these bits can be programmed separately, such a configuration is not supported by today's software and is not supported by this hardware. If this bit is left unchanged before switching, the result is indeterminate.
1	1h RO	**Primary Mode Native Capable (PNC):** Indicates that the primary controller supports both legacy and native modes.
0	0h RW	**Primary Mode Native Enable (PNE):** Determines the mode that the primary channel is operating in. 0 corresponds to 'compatibility', 1 means PCI native. If this bit is set by SW, then the SNE bit must also be set by SW. While in theory these bits can be programmed separately, such a configuration is not supported by today's software and is not supported by this hardware. If this bit is left unchanged before switching, the result is indeterminate.

17.5.6 Class Code (CC)—Offset Ah

Access Method

Type: PCI Configuration Register (Size: 16 bits)

CC: [B:0, D:19, F:0] + Ah

Default: 0106h

15			12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0
BCC								SCC							

Bit Range	Default & Access	Description
15:8	01h RO	**Base Class Code (BCC):** Indicates that this is a mass storage device.
7:0	06h RO	**Sub Class Code (SCC):** The value reported in this field is dependent on MAP.SMS and various fuses and configuration bits. The value is product specific. For VLV this field may read 01h (IDE) or 06h (AHCI).

17.5.7 Cache Line Size (CLS)—Offset Ch

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

CLS: [B:0, D:19, F:0] + Ch

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CLS							

Bit Range	Default & Access	Description
7:0	00h RO	**Cache Line Size (CLS):** This register has no meaning for the SATA controller.

17.5.8 Master Latency Timer (MLT)—Offset Dh

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

MLT: [B:0, D:19, F:0] + Dh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MLT							

Bit Range	Default & Access	Description
7:0	00h RO	**Master Latency Timer (MLT):** This register has no meaning for the SATA controller.

17.5.9 Header Type (HTYPE)—Offset Eh

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

HTYPE: [B:0, D:19, F:0] + Eh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MFD	HL						

Bit Range	Default & Access	Description
7	0h RO	**Multi-function Device (MFD):** Indicates this controller is not part of a multi-function device.
6:0	00h RO	**Header Layout (HL):** Indicates that the controller uses a target device layout.

17.5.10 Primary Command Block Base Address (PCMDBA)—Offset 10h

This 8-byte I/O space is used in Native Mode for the Primary Controller's Command Block.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCMDBA: [B:0, D:19, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
RSVD0																BAR													RSVD1		RTE

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:3	0h RW	**Base Address (BAR):** Base address of the I/O space (8 consecutive I/O locations).
2:1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

17.5.11 Primary Control Block Base Address (PCTLBA)—Offset 14h

This 4-byte I/O space is used in Native Mode for the Primary Controller's Control Block.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCTLBA: [B:0, D:19, F:0] + 14h

Default: 00000001h

31	28	24	20	16	12	8	4	0
0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

RSVD0 | BAR | RSVD1 | RTE

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:2	0h RW	**Base Address (BAR):** Base address of the I/O space (4 consecutive I/O locations).
1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

17.5.12 Secondary Command Block Base Address (SCMDBA)—Offset 18h

This 8-byte I/O space is used in Native Mode for the Secondary Controller's Command Block.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SCMDBA: [B:0, D:19, F:0] + 18h

Default: 00000001h

31	28	24	20	16	12	8	4	0
0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

RSVD0 | BAR | RSVD1 | RTE

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:3	0h RW	**Base Address (BAR):** Base address of the I/O space (8 consecutive I/O locations).
2:1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

17.5.13 Secondary Control Block Base Address (SCTLBA)—Offset 1Ch

This 4-byte I/O space is used in Native Mode for the Secondary Controller's Control Block.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SCTLBA: [B:0, D:19, F:0] + 1Ch

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

31:16	15:2	1	0
RSVD0	BAR	RSVD1	RTE

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:2	0h RW	**Base Address (BAR):** Base address of the I/O space (4 consecutive I/O locations).
1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

17.5.14 Legacy IDE Base Address / AHCI Index Data Pair Base Address (LBAR)—Offset 20h

This BAR is used to allocate I/O space for the SFF-8038i mode of operation (aka Bus Master IDE) and if CC.SCC is not 01h, it is used to allocate I/O space for the AHCI index/data pair mechanism as well. Note that hardware does not clear the BA bits (including BA4) when switching from IDE mode to non-IDE mode or vice versa. BIOS is responsible for clearing those bits to 0 since the number of writable bits changes after mode switching.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

LBAR: [B:0, D:19, F:0] + 20h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

31:16	15:4	3:1	0
RSVD0	BA	RSVD1	RTE

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
15:4	0h RW	**Base Address (BA):** Base address of the I/O space. Note for Base Address bit 4: When CC.SCC is 01h, this bit will be RW resulting in requesting 16B of I/O space. When CC.SCC is not 01h, this bit will be RO=0 resulting in requesting 32B of I/O space.
3:1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

17.5.15 AHCI Base Address/Serial ATA Index Data Pair Base Address (ABAR)—Offset 24h

When the programming interface is not IDE (i.e. CC.SCC is not 01h), this register is named ABAR. When the programming interface is IDE, this register becomes SIDPBA. Note that hardware does not clear those BA bits when switching from IDE SKU to non-IDE SKU or vice versa. BIOS is responsible for clearing those bits to 0 since the number of writable bits changes after SKU switching (as indicated by a change in CC.SCC). In the case, this register will then have to be re-programmed to a proper value. When the programming interface is not IDE, the register represents a memory BAR allocating space for the AHCI memory registers. Note that bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (i.e. ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted. When the programming interface is IDE, the register becomes an I/O BAR allocating 16 bytes of I/O space for the I/O mapped registers defined in Memory Registers. Note that although 16 bytes of locations are allocated, only 8 bytes are used as SINDX and SDATA registers; with the remaining 8 bytes preserved for future enhancement.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ABAR: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BA																												PF	TP		RTE

Bit Range	Default & Access	Description
31:4	0h RW	**Base Address (BA):** When programming interface is non IDE, this is base address of register memory space (aligned to 2 KB). Bits 31:11 are RW, bits 10:4 are RO of 0; When programming interface is IDE, this is base address of the I/O space. Bits 31:16 are RO of 0, bits 15:4 are RW
3	0h RO	**Prefetchable (PF):** When programming interface is non IDE, this indicates that this range is not prefetch-able
2:1	0h RO	**Type (TP):** When programming interface is non IDE, this indicates that this range can be mapped anywhere in 32-bit address space
0	0h RO	**Resource Type Indicator (RTE):** When programming interface is non IDE, this indicates a request for register memory space; When programming interface is IDE, this indicates a request for IO space.

17.5.16 Sub System Identifiers (SS)—Offset 2Ch

This register is initialized to logic 0 by the assertion of Backbone Reset. This register can be written only once after Backbone Reset de-assertion.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SS: [B:0, D:19, F:0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSID																SSVID															

Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

17.5.17 Capabilities Pointer (CAP)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

CAP: [B:0, D:19, F:0] + 34h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
CP							

Bit Range	Default & Access	Description
7:0	80h RW/L	**Capability Pointer (CP):** Indicates that the first capability pointer offset is offset 80h (the Message Signaled Interrupt capability). The following capability structures are linked by default which is meant for non-IDE mode: CAP.CP - 80h (MSI) - 70h (PCI Power) - A8h (SATA) - 00h end. BIOS may alter the capability structure list above (by programming a leading capability structure's Next Pointer field) if BIOS wants to bypass any specific capability.[Br] If BIOS intends to operate in IDE mode, BIOS is requested to program this field to 70h and the subsequent capability list as such: CAP.CP - 70h (PCI Power) - end. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO.

17.5.18 Interrupt Information (INTR)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 16 bits)

INTR: [B:0, D:19, F:0] + 3Ch

Default: 0100h

15			12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
IPIN								ILINE							

Bit Range	Default & Access	Description
15:8	01h RO	**Interrupt Pin (IPIN):** This register tells which interrupt pin the device function uses. A value of 1 corresponds to INTA#. A value of 2 corresponds to INTB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#.
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

17.5.19 Minimum Grant (MGNT)—Offset 3Eh

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

MGNT: [B:0, D:19, F:0] + 3Eh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MGNT							

Bit Range	Default & Access	Description
7:0	00h RO	**MGNT:** Minimum Grant

17.5.20 Maximum Latency (MLAT)—Offset 3Fh

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

MLAT: [B:0, D:19, F:0] + 3Fh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MLAT							

Bit Range	Default & Access	Description
7:0	00h RO	**MLAT:** Maximum Latency

17.5.21 Primary Timing (PTIM)—Offset 40h

This controls the timings driven on the parallel cable.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PTIM: [B:0, D:19, F:0] + 40h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DE	D1STE	ISP		RSVD0		RCT		DTE1	PPE1	IE1	TIM1	DTE0	PPE0	IE0	TIM0

Bit Range	Default & Access	Description
15	0h RW	**Decode Enable (DE):** Enables the SATA Controller to decode the Command Blocks (1F0-1F7h for primary, 170-177h for secondary or their native BAR equivalents) and Control Block (3F6h for primary and 376h for secondary or their native BAR equivalents). This bit still has functionality in SATA - if this bit is not set, the port that is mapped to this range will not be decoded.
14	0h RW	**Device 1 Separate Timing Enable (D1STE):** This register is not used by SATA controller.
13:12	0h RW	**IORDY Sample Point (ISP):** This register is not used by SATA controller.
11:10	0b RO	**RSVD0:** Reserved
9:8	0h RW	**Recovery Time (RCT):** This register is not used by SATA controller.
7	0h RW	**Device 1 DMA Timing Enable (DTE1):** This register is not used by SATA controller.
6	0h RW	**Device 1 Prefetch/Posting Enable (PPE1):** This register is not used by SATA controller.
5	0h RW	**Device 1 IORDY Sample Point Enable (IE1):** This register is not used by SATA controller.
4	0h RW	**Device 1 Fast Timing Bank (TIM1):** This register is not used by SATA controller.
3	0h RW	**Device 0 DMA Timing Enable (DTE0):** This register is not used by SATA controller.
2	0h RW	**Device 0 Prefetch/Posting Enable (PPE0):** This register is not used by SATA controller.
1	0h RW	**Device 0 IORDY Sample Point Enable (IE0):** This register is not used by SATA controller.
0	0h RW	**Device 0 Fast Timing Bank (TIM0):** This register is not used by SATA controller.

17.5.22 Secondary Timing (STIM)—Offset 42h

This controls the timings driven on the parallel cable.

Access Method

Type: PCI Configuration Register (Size: 16 bits)	**STIM:** [B:0, D:19, F:0] + 42h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DE	D1STE	ISP		RSVD0		RCT		DTE1	PPE1	IE1	TIM1	DTE0	PPE0	IE0	TIM0

Bit Range	Default & Access	Description
15	0h RW	**Decode Enable (DE):** Enables the SATA Controller to decode the Command Blocks (1F0-1F7h for primary, 170-177h for secondary or their native BAR equivalents) and Control Block (3F6h for primary and 376h for secondary or their native BAR equivalents). This bit still has functionality in SATA - if this bit is not set, the port that is mapped to this range will not be decoded.
14	0h RW	**Device 1 Separate Timing Enable (D1STE):** This register is not used by SATA controller.
13:12	0h RW	**IORDY Sample Point (ISP):** This register is not used by SATA controller.
11:10	0b RO	**RSVD0:** Reserved
9:8	0h RW	**Recovery Time (RCT):** This register is not used by SATA controller.
7	0h RW	**Device 1 DMA Timing Enable (DTE1):** This register is not used by SATA controller.
6	0h RW	**Device 1 Prefetch/Posting Enable (PPE1):** This register is not used by SATA controller.
5	0h RW	**Device 1 IORDY Sample Point Enable (IE1):** This register is not used by SATA controller.
4	0h RW	**Device 1 Fast Timing Bank (TIM1):** This register is not used by SATA controller.
3	0h RW	**Device 0 DMA Timing Enable (DTE0):** This register is not used by SATA controller.
2	0h RW	**Device 0 Prefetch/Posting Enable (PPE0):** This register is not used by SATA controller.
1	0h RW	**Device 0 IORDY Sample Point Enable (IE0):** This register is not used by SATA controller.
0	0h RW	**Device 0 Fast Timing Bank (TIM0):** This register is not used by SATA controller.

17.5.23 Device 1 IDE Timing (D1TIM)—Offset 44h

This register is not used by SATA controller.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

D1TIM: [B:0, D:19, F:0] + 44h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD							

Bit Range	Default & Access	Description
7:0	0h RW	**RSVD:** Reserved

17.5.24 Synchronous DMA Control (Synchronous_DMA_Control)—Offset 48h

This register is not used by SATA controller.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Synchronous_DMA_Control: [B:0, D:19, F:0] + 48h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD							

Bit Range	Default & Access	Description
7:0	0h RW	**RSVD:** Reserved

17.5.25 Synchronous_DMA_Timing—Offset 4Ah

This register is not used by SATA controller.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Synchronous_DMA_Timing: [B:0, D:19, F:0] + 4Ah

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD															

Bit Range	Default & Access	Description
15:0	0h RW	**RSVD:** Reserved

17.5.26 IDE I/O Configuration (IIOC)—Offset 54h

This register is not used by SATA controller.

Access Method

Type: PCI Configuration Register (Size: 32 bits) **IIOC:** [B:0, D:19, F:0] + 54h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																															

Bit Range	Default & Access	Description
31:0	0h RW	**RSVD:** Reserved

17.5.27 PCI Power Management Capability ID (PID)—Offset 70h

Access Method

Type: PCI Configuration Register (Size: 16 bits) **PID:** [B:0, D:19, F:0] + 70h

Default: A801h

15			12				8				4				0
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1
NEXT								CID							

Bit Range	Default & Access	Description
15:8	A8h RW/L	**Next Capability (NEXT):** A8h is location of the Serial ATA Capability structure. This is recommended for non-IDE mode. If the controller is to operate in IDE mode, BIOS is requested to program this field to 00h indicating the end (recommended setting). The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO.
7:0	01h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management capability.

17.5.28 PCI Power Management Capabilities (PC)—Offset 72h

Access Method

Type: PCI Configuration Register (Size: 16 bits) **PC:** [B:0, D:19, F:0] + 72h

Default: 4003h

15			12				8				4				0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
PME_Support					D2_Support	D1_Support	Aux_Current			DSI	RSVD0	PMEC	VS		

Bit Range	Default & Access	Description
15:11	08h RO	**PME_Support:** By default with CC.SCC=01h, the default value is 00000 which indicates no PME Support in IDE mode. When CC.SCC is not 01h in non-IDE mode, the default value is 01000 which indicates PME# can be generated from the D3HOT state in the SATA controller.
10	0h RO	**D2_Support:** The D2 state is not supported.
9	0h RO	**D1_Support:** The D1 state is not supported.
8:6	0h RO	**Aux_Current:** PME# from D3COLD state is not supported, therefore this field is 000b.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0b RO	**RSVD0:** Reserved
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

17.5.29 PCI Power Management Control and Status (PMCS)—Offset 74h

Access Method

Type: PCI Configuration Register (Size: 16 bits) **PMCS:** [B:0, D:19, F:0] + 74h

Default: 0008h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
PMES	RSVD0						PMEE	RSVD1				NSFRST	RSVD2	PS	

Bit Range	Default & Access	Description
15	0h RW	**PME Status (PMES):** This bit is set when a PME event is to be requested, and if this bit is set and PMEE is set, a PME# will be generated. -Note: Whenever CC.SCC=01h either by default or just being updated, hardware shall automatically change the attribute to RO of 0.
14:9	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
8	0h RW	**PME Enable (PMEE):** When CC.SCC is not 01h, this bit is RW. When set, the SATA controller generates PME# from D3HOT on a wake event. Whenever CC.SCC=01h either by default or just being updated, hardware shall automatically change the attribute to RO of 0 since there is no PME Support in IDE mode. Note: Software is advised to clear PMEE together with PMES prior to changing CC.SCC thru MAP.SMS.
7:4	0b RO	**RSVD1:** Reserved
3	1h RO	**No Soft Reset (NSFRST):** A 1 indicates that devices transitioning from D3hot to D0 because of Power_State commands do not perform an internal reset. Configuration context is preserved. Upon transition from the D3hot to the D0 initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the Power_State bits. Regardless of this bit, the controller transition from D3hot to the D0 by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0b RO	**RSVD2:** Reserved
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the SATA Controller and to set a new power state. The values are: 00 = D0 state; 11 = D3HOT state. When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a 10 or 01 to these bits, the write will be ignored. Refer to PCI PM specification section 8.2.2. on software requirements in ensuring I/O space, memory space and Bus Master are disabled prior to entering D3 state.

17.5.30 Message Signaled Interrupt Identifier (MID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MID: [B:0, D:19, F:0] + 80h

Default: 7005h

15			12				8				4				0
0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1
NEXT								CID							

Bit Range	Default & Access	Description
15:8	70h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list is the PCI power management pointer. This is the recommended value. BIOS may program this field to A8h indicating that the next item is Serial ATA Capability structure. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO.
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

17.5.31 Message Signaled Interrupt Message Control (MC)—Offset 82h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MC: [B:0, D:19, F:0] + 82h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0								C64	MME			MMC			MSIE

Bit Range	Default & Access	Description
15:8	0b RO	**RSVD0:** Reserved
7	0h RO	**64 Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RO	**Multiple Message Enable (MME):** When this field is cleared to 000 (and MSIE is set), only a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
3:1	0h RO	**Multiple Message Capable (MMC):** Not supported.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note that CMD.ID bit has not effect on MSI. Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field. Software must also make sure this bit is cleared to 0 when operating in legacy mode (for AHCI SKUs when GHC.AE = 0). This bit is RW when CC.SCC is not 01h and is read-only 0 when CC.SCC is 01h.

17.5.32 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MA: [B:0, D:19, F:0] + 84h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADDR																														RSVD0	

Bit Range	Default & Access	Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	0b RO	**RSVD0:** Reserved

17.5.33 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MD: [B:0, D:19, F:0] + 88h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA															

Bit Range	Default & Access	Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction.

17.5.34 Port Mapping Register (MAP)—Offset 90h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MAP: [B:0, D:19, F:0] + 90h

Default: 0420h

15			12				8				4				0
0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
RSVD0				SPD0		SPD		SMS		SC	RSVD1			MV	

Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:10	1h RO	**SATA Port Disable (SPD0):** A 1 in a bit position corresponding to the SATA port prevents the SATA port from being enabled via config PCS.PxE. Write of 1 to PCS.PxE has no effect when the corresponding SPD[x] bit is 1. In preventing a port(s) from being enabled, BIOS shall first configure MAP.SPD. And only then BIOS configures the PCS.PxE.
9:8	0h RO	**SATA Port Disable (SPD):** A 1 in a bit position corresponding to the SATA port prevents the SATA port from being enabled via config PCS.PxE. Write of 1 to PCS.PxE has no effect when the corresponding SPD[x] bit is 1. In preventing a port(s) from being enabled, BIOS shall first configure MAP.SPD. And only then BIOS configures the PCS.PxE.
7:6	0h RW	**SATA Mode Select (SMS):** Software (SW) programs these bits to control the mode in which the SATA HBA should operate: 00b = IDE mode which requires LBC01.LBGE=1 (refer to LBC01, LBC23 and LBC45 register in SIR register space); 01b = AHCI mode; 10b = RAID mode; 11b = Reserved. Notes : SW shall not manipulate MAP.SMS during runtime operation; i.e. the OS will not do this. The BIOS may choose to switch from one mode to another during POST. IDE mode can be selected when AHCI and/or RAID are enabled. After switching from AHCI/RAID back to IDE mode, the number of usable ports on SATA Controller 1 shall be reduced to 4, dependent on SKUs. AHCI mode may only be selected when MV = 00b. AHCI mode may be selected when RAID feature is enabled by fuse. VLV does not support RAID mode. Programming these bits with values that are illegal will result in in-deterministic behavior by the HW.

Bit Range	Default & Access	Description
5	1h RW	**SATA Port-to-Controller Configuration (SC):** This bit changes number of SATA port availability within each SATA controller. When MAP.SPD[5] is 1 and MAP.SPD[4] is 1, this bit is reserved and is read-only 1 else it's RW-zero. When this bit is 0: Up to 2 SATA ports are available in the SATA controller 1 with port[1:0]. When this bit to 1: Up to 2 SATA ports are available in the SATA controller 1 with port [1:0]. For SMS=IDE mode, this bit should be 0 (note that this irrespective of the number of SATA ports). The number of port availability in this controller shall be discoverable thru this controller's config PCS.PxE, AHCI CAP.NP and AHCI PI[x] register fields. Prior to changing the state of this bit, all ports must be in quiescent state with no commands outstanding. Refer to Single and Dual Controller Switching Requirement for additional software and hardware requirements.
4:2	0b RO	**RSVD1:** Reserved
1:0	0h RO	**Map Value (MV):** This register is reserved.

17.5.35 Port Control and Status (PCS)—Offset 92h

By default, the SATA ports are set (by hardware) to the disabled state (e.g. bits[5:0] == 0) as a result of an initial power on reset. When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. Note: AHCI specific notes: If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL.DET and PxCMD.SUD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to 1 prior to booting the OS, regardless as to whether or not a device is currently on the port.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCS: [B:0, D:19, F:0] + 92h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ORM	RSVD0	RSVD				P1P	P0P	RSVD1						P1E	P0E

Bit Range	Default & Access	Description
15	0h RW	**OOB Retry Mode (ORM):** When cleared, the SATA controller will not retry after an OOB failure. When set, the SATA controller will continue to retry after an OOB failure until successful (infinite retry). BIOS is requested to program this field to 1.
14	0b RO	**RSVD0:** Reserved
13:10	0h RO	**RSVD:** Reserved
9	0h RO	**Port 1 Present (P1P):** Same as P0P, except for port 1.

Bit Range	Default & Access	Description
8	0h RO	**Port 0 Present (P0P):** When set, the SATA controller has detected the presence of a device on port 0. It may change at any time. Clearing P0E bit leads to clearing of this bit after implementation delay. Note: For system software that intends to clear all PCS.PxE bits that are previously 1 to 0 and then to 1 again in two consecutive write cycles, software shall poll on this bit being 0 before setting P0E bit to 1.
7:2	0b RO	**RSVD1:** Reserved
1	0h RW	**Port 1 Enabled (P1E):** When MAP.SPD[1] is 1, this bit is reserved and read-only 0. Otherwise if none of the above is true, this bit is RW and same as P0E but for port 1 and takes precedence over P1CMD.SUD.
0	0h RW	**Port 0 Enabled (P0E):** When MAP.SPD[0] is 1, this bit is reserved and read-only 0. When set, the port is enabled. When cleared, the port is disabled. When enabled, the port can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. This bit takes precedence over P0CMD.SUD. Note: The recommendation for software code that intends to clear all PCS.PxE bits that are previously 1 to 0 and then to 1 again immediately shall refer to the polling requirement as described in P0P register bit. At any time that BIOS or software is clearing PCS.PxE from 1 to 0, due to time needed for port staggering hardware process (up to 2 ports) to complete, BIOS and software shall delay the write to set the TM.PCD register by 1.4us.

17.5.36 Test Mode Register (TM)—Offset 94h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

TM: [B:0, D:19, F:0] + 94h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (31:26)	PCD (25:24)	RSVD0 (23:0)

Bit Range	Default & Access	Description
31:26	0h RO	**Reserved (RSVD):** Reserved.
25:24	0h RW	**Port Clock Disable (PCD):** When any of these bits is set to 1, the backbone clock driven to the associated port logic is gated and will not toggle. When this bit is cleared to 0, all clocks to the associated port logic will operate normally.
23:0	0b RO	**RSVD0:** Reserved

17.5.37 SATA General Configuration (SATAGC)—Offset 9Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

SATAGC: [B:0, D:19, F:0] + 9Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

REGLOCK	RSVD0	WRRSELMPS	RSVD1	URRE	URD	AIE	DEVIDSEL	FLRCSSEL	RSVD2

Bit Range	Default & Access	Description
31	0h RW/O	**Register Lock (REGLOCK):** BIOS can set this bit to 1 to lock the following registers with RW/L attribute: CAP,CP, MID.NEXT, PIE.NEXT, SATACR0.NEXT. Once locked the register attribute of above list changes from RW/L to RO holding the existing value. BIOS is requested to program this field to 1 prior to handle off to OS. If BIOS needs the SATA host controller to change operation a few times (i.e. changing CC.SCC mode) and need different capability structures for each specific operation mode, BIOS need not activate the lock until BIOS is ready to hand off to OS. BIOS may need to separate write access to this byte offset (x9Fh) from write to the lower 3-byte of the dword (x9C-9Eh) if there is a need to program the lower 3-byte dword location early during boot process.
30:15	0b RO	**RSVD0:** Reserved
14:12	0h RW	**Write Request_Size Select/Max_Payload_Size (WRRSELMPS):** These two bits select the max write request size that SATA host controller will initiate for DMA write to memory. SATA host controller will internally break up larger write request based on these bits. The request is address-aligned to the selected size. Defined encodings for this field are: 000b = 128 address aligned bytes max payload size; 111b = 64 address aligned bytes max payload size. All other values are reserved for SATA host controller.
11:10	0b RO	**RSVD1:** Reserved
9	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error. If both URRE and PCI configuration SERR# Enable registers are set to a 1, then the agent must set the Signaled System Error bit in the PCI Status register and send a DO_SERR message in IOSF-SB interface.
8	0h RW/1C	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW.
7	0h RW/O	**Alternate ID Enable (AIE):** When programmed to 0, HW will report the following device id's: 2822h for desktop or 282Ah for mobile. When programmed to a 1, HW will not report these device id's. The value is product specific. Note: Programming this bit to a 1 will prevent the Windows in-box version of the Intel AHCI driver from loading on the platform - will require that the user perform an 'F6' install of the Intel driver that is appropriate for the reported DID. This field is applicable when the AHCI is configured for RAID mode of operation. It has no impact for AHCI and IDE modes of operation. Note: BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by Backbone Reset and BIOS is required to reprogram the value (either 0 or 1) after resuming from S3, S4 or S5. This insures that the value is properly and cannot be changed during runtime.
6	0h RW/O	**AIE0 DevID Selection (DEVIDSEL):** This register allows BIOS to select Device ID when AIE=0 and Server Feature Disable Fuse 7 =0. This bit only has effect in Desktop SKU. In Mobile SKU this bit has no effect at all. Refer to config register offset 09h PI for usage. 0 : 2822h; 1 : 2826h. NOTE: When Server Feature (SATA AIE DEVIDSEL) Disable Fuse 7 is programmed to 1, this disables the writeability of this DEVIDSEL register bit, and becomes RO with a value of 0, which only allows a choice of 2822h.
5	0h RW/O	**FLR Capability Selection (FLRCSSEL):** This allows the FLR Capability to be bypassed. Refer to config offset B0h. BIOS is requested to program this bit to 1 and config offset A8h SATACR0.NEXT to 00h.
4:0	0b RO	**RSVD2:** Reserved

17.5.38 SATA Initialization Register Index (SIRI)—Offset A0h

Access Method

Type: PCI Configuration Register (Size: 8 bits)   **SIRI:** [B:0, D:19, F:0] + A0h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IDX						RSVD0	

Bit Range	Default & Access	Description
7:2	00h RW	**Index (IDX):** 6-bit index pointer into the 256-byte space. Data is written into the SIRD register and read from the SIRD register. This point to a DWord register. The byte enables on the SIRD register affect what will be written. Note that this 256-byte register space setting is applicable to all ports in both SATA controllers 1 and 2 (if supported). Refer to SATA Initialization Register section for detail of the register space.
1:0	0b RO	**RSVD0:** Reserved

17.5.39 SATA Initialization Register Data (SIRD)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)   **SIRD:** [B:0, D:19, F:0] + A4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DTA																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**Data (DTA):** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.

17.5.40 Serial ATA Capability Register 0 (SATACR0)—Offset A8h

This register shall be read-only 0 when CC.SCC is 01h. Note that the SATACR0.NEXT is not changed from RO to become RWO because there is an existing method (SATAGC.FLRCSSEL bit) to bypass the FLR Capability structure. And FLR Capability ID.NEXT is already indicating end of capability structure, it does not need change to be RWO.

Access Method

Type: PCI Configuration Register (Size: 32 bits)   **SATACR0:** [B:0, D:19, F:0] + A8h

Default: 00100012h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
RSVD0								MAJREV				MINREV				NEXT								CAP							

Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23:20	1h RO	**Major Revision (MAJREV):** Major revision number of the SATA Capability Pointer implemented.
19:16	0h RO	**Minor Revision (MINREV):** Minor revision number of the SATA Capability Pointer implemented.
15:8	00h RW/L	**Next Capability Pointer (NEXT):** 00h indicating the final item in the Capability List. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO.
7:0	12h RO	**Capability ID (CAP):** The value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

17.5.41 Serial ATA Capability Register 1 (SATACR1)—Offset ACh

This register shall be read-only 0 when CC.SCC is 01h.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SATACR1: [B:0, D:19, F:0] + ACh

Default: 00000048h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0
RSVD0																BAROFST												BARLOC			

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:4	004h RO	**BAR Offset (BAROFST):** Indicates the offset into the BAR where the AHCI Index/Data pair are located (in Dword granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR (BAR4). A value of 004h indicates offset 10h. 000h = 0h offset; 001h = 4h offset; 002h = 8h offset; 003h = Ch offset; 004h = 10h offset ... FFFh = 3FFFh offset (max 16 KB)
3:0	8h RO	**BAR Location (BARLOC):** Indicates the absolute PCI Configuration Register address of the BAR containing the Index/Data pair (in Dword granularity). The Index and Data I/O registers reside within the space defined by LBAR (BAR4) in the SATA controller. A value of 8h indicates offset 20h, which is LBAR (BAR4). 0000 - 0011b = reserved; 0100b = 10h =) BAR0; 0101b = 14h =) BAR1; 0110b = 18h =) BAR2; 0111b = 1Ch =) BAR3; 1000b = 20h =) LBAR; 1001b = 24h =) BAR5; 1010 - 1110b = reserved; 1111b = Index/Data pair in PCI Configuration space which is not supported.

17.5.42 FLR Capability ID (FLRCID)—Offset B0h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

FLRCID: [B:0, D:19, F:0] + B0h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NEXT								CID							

Bit Range	Default & Access	Description
15:8	00h RO	**Next Capability (NEXT):** 00h indicating the final item in the Capability List.
7:0	00h RO	**Capability ID (CID):** The value of this field depends on the FLRCSSEL bit. SATAGC.FLRCSSEL = 0, Capability ID = 13h; SATAGC.FLRCSSEL = 1, Capability ID = 00h (capability is bypassed).

17.5.43 FLR Control (FLRCTL)—Offset B4h

This register shall be read-only 0 when SATAGC.FLRCSSEL=1.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

FLRCTL: [B:0, D:19, F:0] + B4h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD															

Bit Range	Default & Access	Description
15:0	0h RO	**RSVD:** Reserved

17.5.44 Scratch Pad (SP)—Offset D0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SP: [B:0, D:19, F:0] + D0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DT																															

Bit Range	Default & Access	Description
31:0	0h RW	**Data (DT):** This is a read/write register that is available for software to use. No hardware action is taken on this register.

17.5.45 BIST FIS Control/Status (BFCS)—Offset E0h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

BFCS: [B:0, D:19, F:0] + E0h

Default: 00000000h

31:12	11	10	9	8	7:2	1:0
0000 0000 0000 0000 0000	0	0	0	0	0000 00	00
RSVD0	BFS	BFF	P1BFI	P0BFI	BFP	RSVD1

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0h RW	**BIST FIS Successful (BFS):** This bit is set any time that a BIST FIS transmitted by the SATA controller receives an R_OK completion status from the device
10	0h RW	**BIST FIS Failed (BFF):** This bit is set any time that a BIST FIS transmitted by the SATA controller receives an R_ERR completion status from the device
9	0h RW	**Port 1 BIST FIS Initiate (P1BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 1, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P1E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS.
8	0h RW	**Port 0 BIST FIS Initiate (P0BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 0, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P0E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS.
7:2	0h RW	**BIST FIS Parameters (BFP):** These bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in the BIST FIS transmitted by the SATA controller. This field is not port specific - its contents will be used for any BIST FIS initiated on the SATA controller. The specific bit definitions are: Bit 7 (T) Far End Transmit mode; bit 6 (A) Align Bypass mode; bit 5 (S) Bypass Scrambling; bit 4 (L) Far End Retimed Loopback; bit 3 (F) Far End Analog Loopback; bit 2 (P) Primitive bit for use with Transmit mode.
1:0	0b RO	**RSVD1:** Reserved

17.5.46 BIST FIS Transmit Data 1 (BFTD1)—Offset E4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

BFTD1: [B:0, D:19, F:0] + E4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA

Bit Range	Default & Access	Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the second DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the T bit is indicated in the BFCS register.

17.5.47 BIST FIS Transmit Data 2 (BFTD2)—Offset E8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BFTD2: [B:0, D:19, F:0] + E8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA

Bit Range	Default & Access	Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the third DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the T bit is set in the BFCS register.

17.5.48 Manufacturing ID (MFID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MFID: [B:0, D:19, F:0] + F8h

Default: 08000FB1h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0	1

RSVD0 | DPID | SID | MID | PID

Bit Range	Default & Access	Description
31:28	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
27:24	8h RO	**Dot portion of Process ID (DPID):** Indicates the dot. Process is reflected in bits [7:0]. The value is product specific.
23:16	0h RO	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. The value is product specific.
15:8	0Fh RO	**Manufacturer Identifier (MID):** Indicates Intel.
7:0	B1h RO	**Process/Dot Identifier (PID):** Indicates the Process. Dot is reflected in bits [27:24]. The value is product specific.

17.6 SATA Legacy IO Registers

Table 194. Summary of SATA Legacy I/O Registers—LBAR

Offset	Size	Register ID—Description	Default Value
0h	1	"Primary Command (PCMD)—Offset 0h" on page 1961	00h
2h	1	"Primary Status (PSTS)—Offset 2h" on page 1962	00h
4h	4	"Primary Descriptor Table Pointer (PDTP)—Offset 4h" on page 1962	00000000h
8h	1	"Secondary Command (SCMD)—Offset 8h" on page 1963	00h
Ah	1	"Secondary Status (SSTS)—Offset Ah" on page 1963	00h
Ch	4	"Secondary Descriptor Table Pointer (SDTP)—Offset Ch" on page 1964	00000000h
10h	4	"AHCI Index Register (INDEX)—Offset 10h" on page 1965	00000000h
14h	4	"AHCI Data Register (DATA)—Offset 14h" on page 1966	00000000h

17.6.1 Primary Command (PCMD)—Offset 0h

Access Method

Type: I/O Register
(Size: 8 bits)

PCMD: [LBAR] + 0h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0				RWC	RSVD1		START

Bit Range	Default & Access	Description
7:4	0b RO	**RSVD0:** Reserved
3	0h RW	**Read / Write Control (RWC):** Sets the direction of the bus master transfer: 0 = memory to device, 1 = device to memory. This bit must not be changed when the bus master function is active.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**Start/Stop Bus Master (START):** Setting this bit enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit in PCI configuration space is also set. Clearing it halts bus master operation. All state information is lost when this bit is written to 0; Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active and the device has not yet finished its data transfer, the bus master command is said to be aborted. If this bit is cleared to 0 prior to the DMA data transfer being initiated by the drive in a device to memory data transfer, then not DMAT will be sent to terminate the data transfer. SW intervention (e.g. sending SRST) is required to reset the interface in this condition. This bit is intended to be cleared by software after the data transfer is completed - as indicated by either the ACT bit being cleared in the status register, or the I bit being set in the status register, or both.

17.6.2 Primary Status (PSTS)—Offset 2h

Access Method

Type: I/O Register
(Size: 8 bits)

PSTS: [LBAR] + 2h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S	D1DC	D0DC	RSVD0		I	ERR	ACT

Bit Range	Default & Access	Description
7	0h RO	**Simplex Only (S):** This read-only bit indicates whether or not I both bus master channels (primary and secondary) can be operated at the same time. If the bit is a 0, then the channels operate independently and can be used at the same time. If the bit is a 1, then only one channel may be used at a time.
6	0h RW	**Device 1 DMA Capable (D1DC):** A scratchpad bit set by SW to indicate that device 1 of this channel is capable of DMA transfers. This bit has no effect on the hardware.
5	0h RW	**Device 0 DMA Capable (D0DC):** A scratchpad bit set by SW to indicate that device 0 of this channel is capable of DMA transfers. This bit has no effect on the hardware.
4:3	0b RO	**RSVD0:** Reserved
2	0h RW/1C	**Interrupt (I):** This bit is set when a device FIS is received with the I bit has been set provided that software has not disabled interrupt via the nIEN bit of Device Control Register.
1	0h RW/1C	**Error (ERR):** This bit is set when the controller encounters an error during the transfer and must stop the transfer. See Error Handling for the list of errors that set this bit.
0	0h RO	**Active (ACT):** Set by the host when the START bit is written to the Command register, and cleared by the host when the last transfer for a region is performed, where EOT for that region is set in the region descriptor, and when the START bit is cleared in the Command register and the controller has returned to an idle condition.

17.6.3 Primary Descriptor Table Pointer (PDTP)—Offset 4h

Access Method

Type: I/O Register
(Size: 32 bits)

PDTP: [LBAR] + 4h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
DBA								RSVD0

Bit Range	Default & Access	Description
31:2	00000000h RW	**Descriptor Base Address (DBA):** Corresponds to A[31:2]. This table must not cross a 64K boundary in memory. When read, the current value of the pointer is returned
1:0	0b RO	**RSVD0:** Reserved

17.6.4 Secondary Command (SCMD)—Offset 8h

Access Method

Type: I/O Register
(Size: 8 bits)

SCMD: [LBAR] + 8h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0				RWC	RSVD1		START

Bit Range	Default & Access	Description
7:4	0b RO	**RSVD0:** Reserved
3	0h RW	**Read / Write Control (RWC):** Sets the direction of the bus master transfer: 0 = memory to device, 1 = device to memory. This bit must not be changed when the bus master function is active.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**Start/Stop Bus Master (START):** Setting this bit enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit in PCI configuration space is also set. Clearing it halts bus master operation.

17.6.5 Secondary Status (SSTS)—Offset Ah

Access Method

Type: I/O Register
(Size: 8 bits)

SSTS: [LBAR] + Ah

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S	D1DC	D0DC	RSVD0		I	ERR	ACT

Bit Range	Default & Access	Description
7	0h RO	**Simplex Only (S):** This read-only bit indicates whether or not I both bus master channels (primary and secondary) can be operated at the same time. If the bit is a 0, then the channels operate independently and can be used at the same time. If the bit is a 1, then only one channel may be used at a time.
6	0h RW	**Device 1 DMA Capable (D1DC):** A scratchpad bit set by SW to indicate that device 1 of this channel is capable of DMA transfers. This bit has no effect on the hardware.
5	0h RW	**Device 0 DMA Capable (D0DC):** A scratchpad bit set by SW to indicate that device 0 of this channel is capable of DMA transfers. This bit has no effect on the hardware.
4:3	0b RO	**RSVD0:** Reserved
2	0h RW/1C	**Interrupt (I):** This bit is set when a device FIS is received with the I bit has been set provided that software has not disabled interrupt via the nIEN bit of Device Control Register.
1	0h RW/1C	**Error (ERR):** This bit is set when the controller encounters an error during the transfer and must stop the transfer. See Error Handling for the list of errors that set this bit.
0	0h RO	**Active (ACT):** Set by the host when the START bit is written to the Command register, and cleared by the host when the last transfer for a region is performed, where EOT for that region is set in the region descriptor, and when the START bit is cleared in the Command register and the controller has returned to an idle condition.

17.6.6 Secondary Descriptor Table Pointer (SDTP)—Offset Ch

Access Method

Type: I/O Register
(Size: 32 bits)

SDTP: [LBAR] + Ch

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															DBA																RSVD0

Bit Range	Default & Access	Description
31:2	00000000h RW	**Descriptor Base Address (DBA):** Corresponds to A[31:2]. This table must not cross a 64K boundary in memory. When read, the current value of the pointer is returned
1:0	0b RO	**RSVD0:** Reserved

17.6.7 AHCI Index Register (INDEX)—Offset 10h

This registers are only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/ SDATA register pair shall be used to index into a subset of the memory registers defined in (See Memory Registers for more information on which registers could be indexed).

Access Method

Type: I/O Register
(Size: 32 bits)

INDEX: [LBAR] + 10h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																					INDEX									RSVD1	

Bit Range	Default & Access	Description
31:11	0b RO	**RSVD0:** Reserved
10:2	000h RO	**Index (INDEX):** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	0b RO	**RSVD1:** Reserved

17.6.8 AHCI Data Register (DATA)—Offset 14h

This registers are only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/ SDATA register pair shall be used to index into a subset of the memory registers defined in (See Memory Registers for more information on which registers could be indexed).

Access Method

Type: I/O Register
(Size: 32 bits)

DATA: [LBAR] + 14h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**Data (DATA):** This Data register is a window through which data is read or written to the memory mapped register pointed to by the Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Index.

17.7 SATA Index Pair IO Registers

Table 195. Summary of SATA Index Pair I/O Registers—ABAR

Offset	Size	Register ID—Description	Default Value
0h	4	“Serial ATA Index (SINDX)—Offset 0h” on page 1967	00000000h
4h	4	“Serial ATA Data (SDATA)—Offset 4h” on page 1968	00000000h

17.7.1 Serial ATA Index (SINDX)—Offset 0h

All of these I/O registers are in the core well. They are exposed only when CC.SCC is 01h (i.e. IDE programming interface). These are Index/Data Pair registers that are used to access the SerialATA superset registers (SerialATA Status, SerialATA Control and SerialATA Error). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software write operations to the reserved locations shall have no effect while software read operations to the reserved locations shall return 0. Refer to Serial ATA Index/Data Pair Superset Registers for more details.

Access Method

Type: I/O Register
(Size: 32 bits)

SINDX: [ABAR] + 0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

Bits	31:16	15:8	7:0
Default	0000 0000 0000 0000	0000 0000	0000 0000
Field	RSVD0	PIDX	RIDX

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RW	**Port Index (PIDX):** This index field is used to specify the port of the SATA controller that the port specific SerialATA Status (SSTS), SerialATA Control (SCTL) and SerialATA Error (SERR) registers are to be read from or write to. 00h = Primary Master (Port 0); 01h = Primary Slave (Port 2); 02h = Secondary Master (Port 1); 03h = Secondary Slave (Port 3).
7:0	00h RW	**Register Index (RIDX):** This index field is used to specify one out of three registers currently being indexed into. These three registers are the Serial ATA superset SStatus, SControl and SError memory registers and are port specific, hence for this SATA controller, there are four sets of these registers. Refer to Offset 128h, 1A8h, 228h, 2A8h, 328h, 3A8h: PxSSTS - Port [0-5] Serial ATA Status, Offset 12Ch, 1ACh, 22Ch, 2ACh, 32Ch, 3ACh: PxSCTL - Port [0-5] Serial ATA Control, and Offset 130h, 1B0h, 230h, 2B0h, 330h, 3B0h: PxSERR - Port [0-5] Serial ATA Error for definitions of the SStatus, SControl and SError registers. 00h = SSTS; 01h = SCTL; 02h = SERR.

17.7.2 Serial ATA Data (SDATA)—Offset 4h

All of these I/O registers are in the core well. They are exposed only when CC.SCC is 01h (i.e. IDE programming interface). These are Index/Data Pair registers that are used to access the SerialATA superset registers (SerialATA Status, SerialATA Control and SerialATA Error). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software write operations to the reserved locations shall have no effect while software read operations to the reserved locations shall return 0. Refer to Serial ATA Index/Data Pair Superset Registers for more details.

Access Method

Type: I/O Register
(Size: 32 bits)

SDATA: [ABAR] + 4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**Data (DATA):** This Data register is a window through which data is read or written to from the register pointed to by the Serial ATA Index (SINDX) register above. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by SINDX.RIDX field.

17.8 SATA AHCI Memory Mapped IO Registers

Table 196. Summary of SATA AHCI Memory Mapped I/O Registers—ABAR

Offset	Size	Register ID—Description	Default Value
0h	4	"HBA Capabilities (GHC_CAP)—Offset 0h" on page 1970	DF20FF02h
4h	4	"HBA Capabilities (GHC_CAP)—Offset 0h" on page 1970	00000000h
8h	4	"Interrupt Status (IS)—Offset 8h" on page 1973	00000000h
Ch	4	"Ports Implemented (GHC_PI)—Offset Ch" on page 1973	00000000h
10h	4	"AHCI Version (VS)—Offset 10h" on page 1974	00010300h
24h	4	"HBA Capabilities Extended (GHC_CAP2)—Offset 24h" on page 1974	0000003Ch
A0h	4	"Vendor Specific (VSP)—Offset A0h" on page 1975	00000048h
A4h	4	"Vendor Specific Capabilities (VS_CAP)—Offset A4h" on page 1976	018002FEh
C4h	2	"Premium Feature Block (PFB)—Offset C4h" on page 1977	0000h
C8h	2	"SW Feature Mask (SFM)—Offset C8h" on page 1978	003Fh
100h	4	"Port-Command List Base Address (PxCLB0)—Offset 100h" on page 1979	00000000h
104h	4	"Port-Command List Base Address Upper 32-bits (PxCLBU0)—Offset 104h" on page 1979	00000000h
108h	4	"Port-FIS Base Address (PxFB0)—Offset 108h" on page 1980	00000000h
10Ch	4	"Port-FIS Base Address Upper 32-bits (PxFBU0)—Offset 10Ch" on page 1980	00000000h
110h	4	"Port-Interrupt Status (PxIS0)—Offset 110h" on page 1980	00000000h
114h	4	"Port-Interrupt Enable (PxIE0)—Offset 114h" on page 1982	00000000h
118h	4	"Port-Command (PxCMD0)—Offset 118h" on page 1984	00000004h
120h	4	"Port-Task File Data (PxTFD0)—Offset 120h" on page 1986	0000007Fh
124h	4	"Port-Signature (PxSIG0)—Offset 124h" on page 1987	FFFFFFFFh
128h	4	"Port-Serial ATA Status (PxSSTS0)—Offset 128h" on page 1987	00000000h
12Ch	4	"Port-Serial ATA Control (PxSCTL0)—Offset 12Ch" on page 1988	00000000h
130h	4	"Port-Serial ATA Error (PxSERR0)—Offset 130h" on page 1989	00000000h
134h	4	"Port-Serial ATA Active (PxSACT0)—Offset 134h" on page 1990	00000000h
138h	4	"Port-Commands Issued (PxCI0)—Offset 138h" on page 1990	00000000h
144h	4	"Port-Device Sleep (PxDEVSLP0)—Offset 144h" on page 1991	1E022852h
180h	4	"Port-Command List Base Address (PxCLB1)—Offset 180h" on page 1992	00000000h
184h	4	"Port-Command List Base Address Upper 32-bits (PxCLBU1)—Offset 184h" on page 1992	00000000h
188h	4	"Port-FIS Base Address (PxFB1)—Offset 188h" on page 1992	00000000h
18Ch	4	"Port-FIS Base Address Upper 32-bits (PxFBU1)—Offset 18Ch" on page 1993	00000000h
190h	4	"Port-Interrupt Status (PxIS1)—Offset 190h" on page 1993	00000000h
194h	4	"Port-Interrupt Enable (PxIE1)—Offset 194h" on page 1995	00000000h
198h	4	"Port-Command (PxCMD1)—Offset 198h" on page 1996	00000004h
1A0h	4	"Port-Task File Data (PxTFD1)—Offset 1A0h" on page 1999	0000007Fh
1A4h	4	"Port-Signature (PxSIG1)—Offset 1A4h" on page 1999	FFFFFFFFh
1A8h	4	"Port-Serial ATA Status (PxSSTS1)—Offset 1A8h" on page 2000	00000000h

Table 196. Summary of SATA AHCI Memory Mapped I/O Registers—ABAR (Continued)

Offset	Size	Register ID—Description	Default Value
1ACh	4	"Port-Serial ATA Control (PxSCTL1)—Offset 1ACh" on page 2001	00000000h
1B0h	4	"Port-Serial ATA Error (PxSERR1)—Offset 1B0h" on page 2001	00000000h
1B4h	4	"Port-Serial ATA Active (PxSACT1)—Offset 1B4h" on page 2003	00000000h
1B8h	4	"Port-Commands Issued (PxCI1)—Offset 1B8h" on page 2003	00000000h
1C4h	4	"Port-Device Sleep (PxDEVSLP1)—Offset 1C4h" on page 2003	1E022852h
580h	4	"Enclosure Management Message Format (EM_MF)—Offset 580h" on page 2004	00000000h
584h	4	"Enclosure Management LED (EM_LED)—Offset 584h" on page 2005	00000000h

17.8.1 HBA Capabilities (GHC_CAP)—Offset 0h

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon Backbone Reset.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHC_CAP: [ABAR] + 0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: DF20FF02h

31			28				24				20				16				12				8				4				0
1	1	0	1	1	1	1	1	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0
S64A	SCQA	SSNTF	SMPS	SSS	SALP	SAL	SCLO	ISS				SNZO	SAM	SMP	FBSS	PMD	SSC	PSC	NCS					CCCS	EMS	SXS	NP				

Bit Range	Default & Access	Description
31	1h RW/O	**Supports 64-bit Addressing (S64A):** Indicates the S-ATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	1h RW/O	**Supports Native Command Queuing Acceleration (SCQA):** Indicates the SATA controller supports Serial-ATA Native Command Queuing. The HBA will handle DMA Setup FISes in hardware, including support for auto-activate optimization through the FIS.
29	0h RO	**Supports SNotification Register (SSNTF):** When set to 1, indicates that the HBA supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0, the HBA does not support the PxSNTF (SNotification) register and its associated functionality.
28	1h RW/O	**Supports Mechanical Presence Switch (SMPS):** When set to 1, the HBA supports mechanical presence switches on its ports for use in hot plug operations. When cleared to 0, this function is not supported. This value is loaded by the BIOS prior to OS initialization.
27	1h RW/O	**Supports Staggered Spin-up (SSS):** Indicates whether the S-ATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization.
26	1h RW/O	**Supports Aggressive Link Power Management (SALP):** Indicates the S-ATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process. When cleared to 0, software shall treat the PxCMD.ALPE and PxCMD.ASP bits as reserved.

Bit Range	Default & Access	Description
25	1h RW/O	**Supports Activity LED (SAL):** Indicates the S-ATA controller supports a single output pin (SATALED#) which indicates activity.
24	1h RW/O	**Supports Command List Override (SCLO):** When set to 1, indicates that the HBA supports the PxCMD.CLO bit and its associated function. When cleared to 0, The HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue software reset if these bits are still set from a previous operation.
23:20	2h RW/O	**Interface Speed Support (ISS):** Indicates the maximum speed the S-ATA controller can support on its ports. These encodings match the system software programmable PxSCTL.DET.SPD field. 0000 = Reserved; 0001 = Gen 1 (1.5 Gbps); 0010 = Gen 2 (3 Gbps); 0011 = Gen 3 (6 Gbps); 0100 - 1111 = Reserved.
19	0h RO	**Supports Non-Zero DMA Offsets (SNZO):** Reserved as per AHCI 1.3
18	0h RW/O	**Supports AHCI mode only (SAM):** The SATA controller may optionally support AHCI access mechanism only. A value of 0 indicates that in addition to the native AHCI mechanism (via ABAR), the SATA controller implements a legacy, task-file based register interface such as SFF-8038i. A value of 1 indicates that the SATA controller does not implement a legacy, task-file based register interface.
17	0h RO	**Supports Port Multiplier (SMP):** Not supported.
16	0h RO	**FIS-based Switching Supported (FBSS):** Not supported.
15	1h RO	**PIO Multiple DRQ Block (PMD):** If set to 1, the HBA supports multiple DRQ block data transfers for the PIO command protocol.
14	1h RW/O	**Slumber State Capable (SSC):** The SATA controller supports the slumber state.
13	1h RW/O	**Partial State Capable (PSC):** The SATA controller supports the partial state.
12:8	1Fh RO	**Number of Command Slots (NCS):** 1Fh indicating support for 32 slots.
7	0h RO	**Command Completion Coalescing Supported (CCCS):** When set to 1, indicates that the HBA supports command completion coalescing. When command completion coalescing is supported, the HBA has implemented the CCC_CTL and the CCC_PORTS global HBA registers. When cleared to 0, indicates that the HBA does not support command completion coalescing and the CCC_CTL and CCC_PORTS global HBA registers are not implemented.
6	0h RO	**Enclosure Management Supported (EMS):** Not supported
5	0h RW/O	**Supports External SATA (SXS):** When set to 1, indicates that the HBA has one or more Serial ATA ports that has a signal only connector that is externally accessible. If this bit is set, software may refer to the PxCMD.ESP bit to determine whether a specific port has its signal connector externally accessible as a signal only connector (i.e. power is not part of that connector). When the bit is cleared to 0, indicates that the HBA has no Serial ATA ports that have a signal only connector externally accessible.
4:0	02h RO	**Number of Ports (NP):** 0's based value indicating the maximum number of ports supported. Note that the number of ports indicated in this field may be more than the number of ports indicated in the PI register. Number of ports shall be dependent on MAP.SC and PCIe/SATA muxing configuration where if ANY of these parameter disable a particular port then that port is disabled and not counted. The maximum number of ports supported by SIP is 2 and the least is 0 (i.e. Function Disable). In the case of 0 port configuration, the value of NP is a don't care (while implementation has it fixed as 07h). Any combination in between is supported by SATA host controller. Indicates the number of supported ports.

17.8.2 Global HBA Control (GHC)—Offset 4h

This register controls various global actions of the HBA.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHC: [ABAR] + 4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

Bits	31	30:3	2	1	0
Default	0	0000 0000 0000 0000 0000 0000 0000	0	0	0
Field	AE	RSVD0	MRSM	IE	HR

Bit Range	Default & Access	Description
31	0h RW	**AHCI Enable (AE):** When set, indicates that an AHCI driver is loaded and communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. When set, software shall only talk to the HBA using AHCI. The HBA will not have to allow command processing via both AHCI and legacy mechanisms. When cleared, software will only communicate with the HBA using legacy mechanisms. Software shall set this bit to 1 before accessing other AHCI registers. Note: The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is 0, then GHC.AE should be RW and shall have a reset value of 0. If CAP.SAM is 1, then AE shall be read only and shall have a reset value of 1.
30:3	0b RO	**RSVD0:** Reserved
2	0h RO	**MSI Revert to Single Message (MRSM):** When set to 1 by hardware, indicates that the HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the HBA has not reverted to single MSI mode (i.e. hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME (MC.MMC). The HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: MC.MSIE = 1 (MSI is enabled); MC.MMC) 0 (multiple messages requested); MC.MME) 0 (more than one message allocated); MC.MME != MC.MMC (messages allocated not equal to number requested). When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not reverting to that mode. The HBA shall always revert to single MSI mode when the number of vectors allocated by the host is leass than the number requested. Value of MRSM is a don't care when GHC.HR=1.
1	0h RW	**Interrupt Enable (IE):** This global bit enables interrupts from the HBA. When cleared (reset default), all interrupt sources from all ports are disabled. When set, interrupts are enabled.
0	0h RW/1S	**HBA Reset (HR):** When set by SW, this bit causes an internal reset of the HBA. All state machines that relate to data transfers and native command queuing will return to an idle condition, and all ports will be re-initialized via COMRESET. When the HBA has performed the reset action, it will reset this bit to 0. A software write of 0 will have no effect. For a description on which bits are reset when this bit is set, see the AHCI specification, section 10.3.3.

17.8.3 Interrupt Status (IS)—Offset 8h

This register indicates which of the ports within the controller have an interrupt pending and require service.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

IS: [ABAR] + 8h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31:2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0
RSVD0	IPS1	IPS0

Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	0h RW/1C	**Interrupt Pending Status Port 1 (IPS1):** If set, indicates that port 1 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s): That has port 1 physically.
0	0h RW/1C	**Interrupt Pending Status Port 0 (IPS0):** If set, indicates that port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s): That has port 0 physically.

17.8.4 Ports Implemented (GHC_PI)—Offset Ch

This register indicates which ports are exposed to the HBA. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. Any available port may not be implemented. There is BIOS programming requirement on the PI register. Please refer to section 7.9.13.1.1 for details.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHC_PI: [ABAR] + Ch

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31:2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0
RSVD0	PI1	PI0

Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
1	0h RW/O	**Port 1 Implemented (PI1):** If set, then port 1 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 1 is not available.
0	0h RW/O	**Port 0 Implemented (PI0):** If set, then port 0 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 0 is not available.

17.8.5 AHCI Version (VS)—Offset 10h

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VS: [ABAR] + 10h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00010300h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
MJR																MNR															

Bit Range	Default & Access	Description
31:16	0001h RO	**Major Version Number (MJR):** Indicates the major version is 1
15:0	0300h RO	**Minor Version Number (MNR):** Indicates the minor version is 30

17.8.6 HBA Capabilities Extended (GHC_CAP2)—Offset 24h

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon Backbone Reset.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHC_CAP2: [ABAR] + 24h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 0000003Ch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
RSVD0																										DESO	SADM	SDS	APST	RSVD1	BOH

Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	1h RW/O	**DEVSLP Entrance from Slumber Only (DESO):** This field specifies that the HBA shall only assert DEVSLP if the interface is in Slumber. When this bit is set to 1, the HBA shall ignore software directed entrance to DEVSLP via PxCMD.ICC unless PxSSTS.IPM = 6h. When this bit is cleared to 0, the HBA may enter DEVSLP from any link state (active, Partial, or Slumber). BIOS is requested to program this field to 1.
4	1h RW/O	**Supports Aggressive DEVSLP Management (SADM):** When set to 1, the HBA supports hardware assertion of the DEVSLP signal after the idle timeout expires. When cleared to 0, this function is not supported and software shall treat the PxDEVSLP.ADSE field as reserved. Note: If PHY IO PM Disable Fuse is 1, this register will read 0. Else this register will read 1 with RWO attribute.
3	1h RW/O	**Supports DEVSLP (SDS):** When set to 1, the HBA supports the DEVSLP feature. When cleared to 0, DEVSLP is not supported. Note: If PHY IO PM Disable Fuse is 1, this register will read 0. Else this register will read 1 with RWO attribute.
2	1h RW/O	**Automatic Partial to Slumber Transitions (APST):** When set to 1, the HBA supports Automatic Partial to Slumber Transitions. When cleared to 0, Automatic Partial to Slumber Transition is not supported. Note: If SATA PHY PM Disable Fuse is 1, this register will read only 0. Else this register will read 1 with RWO attribute.
1	0b RO	**RSVD1:** Reserved
0	0h RO	**BIOS/OS Handoff (BOH):** Not supported.

17.8.7 Vendor Specific (VSP)—Offset A0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VSP: [ABAR] + A0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000048h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0
RSVD0																									SFMS	PFS	PT	SRPIR	RSVD1		

Bit Range	Default & Access	Description
31:7	0b RO	**RSVD0:** Reserved
6	1h RO	**Software Feature Mask Supported (SFMS):** Set to 1 if the platform is enabled for premium storage features mask (SFM) as described in VS MMIO space at offset ABAR[RPID.(OFST*4)+4].
5	0h RO	**Premium Features Supported (PFS):** Set to 1 if the platform is enabled for premium storage features (PFB) as described in VS MMIO space at offset ABAR[RPID.OFST*4]. Set to 0 if the platform is not enabled for premium storage features.
4	0h RO	**Platform Type (PT):** Set to 1 if mobile platform. Clear (0) if desktop.

Bit Range	Default & Access	Description
3	1h RO	**Supports RAID Platform ID Reporting (SRPIR):** If set to 1, then indicates that the RAID Platform ID is reported via ABAR + C0h. Set to 0 if this ID is not reported via MMIO space.
2:0	0b RO	**RSVD1:** Reserved

17.8.8 Vendor Specific Capabilities (VS_CAP)—Offset A4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

VS_CAP: [ABAR] + A4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 018002FEh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	0

Bits 31:16	Bits 15:12	Bits 11:1	Bit 0
PNRRO	RSVD0	MSL	PNMBRE

Bit Range	Default & Access	Description
31:16	0180h RO	**PCIe NAND Remapped Register Offset (PNRRO):** Specifies the DWORD offset within ABAR as to where the PCIe NAND AHCI BAR register space is remapped. Only valid when PNABRE = 1. This places the start of the PCIe NAND AHCI BAR register space at ABAR + 600h
15:12	0b RO	**RSVD0:** Reserved
11:1	17Fh RW	**Memory Space Limit. (MSL):** This field specifies the size of the remapped memory space for the PCIe NAND device. It is a 0-based field. Memory BAR offset from 0 to MSL of the PCIe NAND device are remapped under the integrated AHCI controller memory space. The remapped offset into the AHCI memory space and the value programmed in this field must not exceed the allocated 2k AHCI memory space of the integrated AHCI controller. The reset default of this field is 17Fh (i.e. bit[11:1] = 00101111111b) which specifies the size of the remapped memory space as 384 bytes.
0	0h RW/O	**PCIe NAND Memory BAR Remapped Enable (PNMBRE):** Set to 1 if a PCIe NAND device is present and remapping of its memory BAR register space is enabled. Cleared to 0 if there is no PCIe NAND device present or the remapping of its memory BAR register space is disabled.

17.8.9 RAID Platform ID (RPID)—Offset C0h

This register is used by the Intel Matrix Storage Manager OROM to match the features supported by the OROM with the platform on which the OROM is executing. This prevents the use of an OROM designed for newer chipsets from being use on older chipsets as this could reduce up-sell potential.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RPID: [ABAR] + C0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00311C02h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0
OFST																RPID															

Bit Range	Default & Access	Description
31:16	0031h RO	**Offset (OFST):** The offset of the Premium Feature Block (PFB) in DWords from the beginning of the ABAR. SFM follows directly after PFB.
15:0	1C02h RO	**RAID Platform ID (RPID):** Specifies the DID value that has been assigned to the platform. This is the same DID that is reported by the SATA controller when SATAGC.AIE is set to 1 except that the DID is always reported through this register, regardless if the programming of SATAGC.AIE.

17.8.10 Premium Feature Block (PFB)—Offset C4h

These registers indicate to the Intel Rapid Storage Technology AHCI driver that those premium RAID features that can be supported on the platform.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

PFB: [ABAR] + C4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0											RSVD_1	RSVD_2	RSVD_3	SEA	SOI

Bit Range	Default & Access	Description
15:5	0b RO	**RSVD0:** Reserved
4	0h RO	**Reserved (RSVD_1):** Read value is the same as VSP.PFS.
3	0h RO	**Reserved (RSVD_2):** Read value is the same as VSP.PFS.
2	0h RO	**Reserved (RSVD_3):** Read value is the same as VSP.PFS.
1	0h RO	**Supports Email Alert (SEA):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.
0	0h RO	**Supports OEM IOCTL (SOI):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.

17.8.11 SW Feature Mask (SFM)—Offset C8h

The following will be programmed by the BIOS when VS_CAP.SFMS == 1. The feature mask is used by SW to determine which non-premium features shall be supported by SW.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

SFM: [ABAR] + C8h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 003Fh

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
RSVD0				OROM_UI_Normal_Delay		Smart_Response_Technology	IRRT_Only_on_ESATA	LED_Locate	HDDUNLOCK	OROM_UI_and_BANNER	IRRT	R5	R10	R1	R0

Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:10	0h RW/O	**OROM UI Normal Delay. (OROM_UI_Normal_Delay):** Values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 secs (default and previous value); 01 = 4 secs; 10 = 6 secs; 11 = 8 secs. If bit 5 == 0, then these values are disregarded.
9	0h RW/O	**Smart Response Technology. (Smart_Response_Technology):** If set to 1, then Smart Response Technology is enabled. If cleared to 0, the feature is disabled.
8	0h RW/O	**RRT Only on ESATA (IRRT_Only_on_ESATA):** If set to 1, then only RRT volumes can span internal and external SATA ports. If cleared to 0, then any RAID volume can span internal and external SATA ports.
7	0h RW/O	**LED Locate (LED_Locate):** If set to 1, then LED/SGPIO hardware is attached and the ping to locate feature is enabled in the OS.
6	0h RW/O	**HDDUNLOCK:** If set to 1, then HDD password unlock is enabled in the OS.
5	1h RW/O	**OROM UI and BANNER (OROM_UI_and_BANNER):** If set to 1, then the OROM UI is displayed. When cleared to 0, the OROM UI and BANNER are not displayed if all disks and volumes have a normal status.
4	1h RW/O	**RRT (IRRT):** If set to 1, then Rapid Recovery Technology is enabled.
3	1h RW/O	**R5:** If set to 1, then RAID5 is enabled
2	1h RW/O	**R10:** If set to 1, then RAID10 is enabled

Bit Range	Default & Access	Description
1	1h RW/O	**R1:** If set to 1, then RAID1 is enabled
0	1h RW/O	**R0:** If set to 1, then RAID0 is enabled

17.8.12 Port-Command List Base Address (PxCLB0)—Offset 100h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxCLB0: [ABAR] + 100h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: CLB (bits 31:10), RSVD0 (bits 9:0)

Bit Range	Default & Access	Description
31:10	000000h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0b RO	**RSVD0:** Reserved

17.8.13 Port-Command List Base Address Upper 32-bits (PxCLBU0)—Offset 104h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxCLBU0: [ABAR] + 104h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: CLBU (bits 31:0)

Bit Range	Default & Access	Description
31:0	00000000h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

17.8.14 Port-FIS Base Address (PxFB0)—Offset 108h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxFB0: [ABAR] + 108h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: FB (bits 31:8), RSVD0 (bits 7:0)

Bit Range	Default & Access	Description
31:8	0000000h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0b RO	**RSVD0:** Reserved

17.8.15 Port-FIS Base Address Upper 32-bits (PxFBU0)—Offset 10Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxFBU0: [ABAR] + 10Ch

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: FBU (bits 31:0)

Bit Range	Default & Access	Description
31:0	00000000h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

17.8.16 Port-Interrupt Status (PxIS0)—Offset 110h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxIS0: [ABAR] + 110h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21:8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
CPDS	TFES	HBFS	HBDS	IFS	INFS	RSVD0	OFS	IPMS	PRCS	RSVD1	DMPS	PCS	DPS	UFS	SDBS	DSS	PSS	DHRS

Bit Range	Default & Access	Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h RW/1C	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0b RO	**RSVD0:** Reserved
24	0h RW/1C	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C	**Incorrect Port Multiplier Status (IPMS):** Not supported
22	0h RO	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0b RO	**RSVD1:** Reserved
7	0h RW/1C	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).
6	0h RO	**Port Connect Change Status (PCS):** 1=Change in Current Connect Status. 0=No change in Current Connect Status. This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared.
5	0h RW/1C	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.
4	0h RO	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.
2	0h RW/1C	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.

Bit Range	Default & Access	Description
1	0h RW/1C	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

17.8.17 Port-Interrupt Enable (PxIE0)—Offset 114h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxIE0: [ABAR] + 114h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CPDS	TFEE	HBFE	HBDE	IFE	INFE	RSVD0	OFE	IPME	PRCE	RSVD1														DMPE	PCE	DPE	UFE	SDBE	DSE	PSE	DHRE

Bit Range	Default & Access	Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** When set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0b RO	**RSVD0:** Reserved
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interrupt.
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interrupt.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
21:8	0b RO	**RSVD1:** Reserved
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.

Bit Range	Default & Access	Description
6	0h RW	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

17.8.18 Port-Command (PxCMD0)—Offset 118h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxCMD0: [ABAR] + 118h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
ICC				ASP	ALPE	DLAE	ATAPI	APSTE	FBSCP	ESP	CPD	MPSP	HPCP	PMA	RSVD0	CR	FR	MPSS	CCS					RSVD1	PSP	APSE	FRE	CLO	POD	SUD	ST

Bit Range	Default & Access	Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four bit field which can be used to control reset and power states of the interface. If the Link layer is currently in the L_IDLE state, writes to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writes to this field shall have no effect. Fh -9h Reserved. 8h DEVSLP: This shall cause the HBA to assert the DEVSLP signal associated with the port; the HBA shall ignore the DEVSLP Idle Timeout value specified by PxDEVSLP.DITO. Software shall only request DEVSLP when the interface is in an idle state (i.e. PxCI is cleared to 0h and PxSACT is cleared to 0h); if the interface is not idle at the time the register is written, then the HBA takes no action and the interface remains in its current state. If PxCAP2.DESO is set to '1' and PxSSTS.IPM is not set to '6h', then the HBA takes no action and the interface remains in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion). 7h Reserved 6h Slumber: This shall cause the HBA to request a transition of the interface to the Slumber state. The SATA device may reject the request and the interface shall remain in its current state. 5h-3h Reserved. 2h Partial: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state. 1h Active: This shall cause the HBA to request a transition of the interface into the active state. If the requested transition is from the DEVSLP state, then the HBA shall wait until PxDEVSLP.DMAT has expired before de-asserting the DEVSLP signal. 0h No-Op / Idle: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and the software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state (with the exception of DEVSLP). The transition to DEVSLP may occur from any other state if CAP2.DESO is cleared to '0'. If CAP2.DESO is set to '1', then DEVSLP may only be transitioned to if the link is in Slumber.
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter Partial state when it clears a bit in the PxCI or PxSACT register and the register values are both 0h. If CAP.SALP is cleard to 0, software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0. This bit is set by software

Bit Range	Default & Access	Description
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** When set to 1, the HBA may perform Automatic Partial to Slumber Transitions. When cleared to 0 - the port shall not perform Automatic Partial to Slumber Transitions. Software shall only set this bit to 1 - if CAP2.APST is set to 1; if CAP2.APST is cleared to 0 - software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.
21	0h RW/O	**External SATA Port (ESP):** When set to 1, indicates that this port is routed externally and will be used with an external SATA device. When set to 1, CAP.SXS must also be set to 1. When cleared (0), indicates that this port is not routed externally and supports internal SATA devices only. If ESP is set to 1, then the port may experience hot plug events.
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user.
17	0h RO	**Port Multiplier Attached (PMA):** Not supported
16	0b RO	**RSVD0:** Reserved
15	0h RO	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running.
13	0h RO	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.
12:8	00h RO	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7	0b RO	**RSVD1:** Reserved
6	0h RO	**PHYSLP Present (PSP):** If set to 1, the platform supports PHYSLP on this port. If cleared to 0, the platform does not support PHYSLP on this port. This bit may only be set to 1 if CAP2.SPS is set to 1.

Bit Range	Default & Access	Description
5	0h RW	**Aggressive PHYSLP Enable (APSE):** This bit is read/write for HBAs that support aggressive PHYSLP management (CAP2.SAPM == 1). This bit is read-only for HBAs that do not support aggressive PHYSLP management (CAP2.SPS == 0). When this bit is set to 1, the HBA shall assert the PHYSLP signal after the port has been idle (PxCI == 0h and PxSACT == 0h) for the amount of time specified by the GHC.PITO register. When this bit is cleared to 0, the HBA does not enter PHYSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxCMD.PSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the PHYSLP signal if asserted.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW	**Spin-Up Device (SUD):** This bit is read/write for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1 for HBAs that do not support staggered spin-up. On an edge detect from 0 to 1, the HBA shall start a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

17.8.19 Port-Task File Data (PxTFD0)—Offset 120h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxTFD0: [ABAR] + 120h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 0000007Fh

Bits	31:16	15:8	7	6:4	3	2:1	0
Default	0000 0000 0000 0000	0000 0000	0	111	1	11	1
Field	RSVD0	ERR	STS_BSY	STS_RSVD0	STS_DRQ	STS_RSVD1	STS_ERR

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RO	**Error (ERR):** Contains the latest copy of the task file error register.

Bit Range	Default & Access	Description
7	0h RO	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	7h RO	**Status Rsvd0 (STS_RSVD0):** Status - Not Applicable.
3	1h RO	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	3h RO	**Status Rsvd1 (STS_RSVD1):** Status - Not Applicable.
0	1h RO	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

17.8.20 Port-Signature (PxSIG0)—Offset 124h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSIG0: [ABAR] + 124h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SIG																															

Bit Range	Default & Access	Description
31:0	FFFFFFFFh RO	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS.

17.8.21 Port-Serial ATA Status (PxSSTS0)—Offset 128h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSSTS0: [ABAR] + 128h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																				IPM				SPD				DET			

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
11:8	0h RO	**Interface Power Management (IPM):** Indicates the current interface state 0h = Device not present or communication not established. 1h = Interface in active state. 2h = Interface in PARTIAL power management state. 6h = Interface in SLUMBER power management state. 8h = PHYSLP asserted. All other values reserved. This field reflects the interface power management state for both device and host initiated power management. Note: If an automatic partial to slumber transition occurs, PxSSTS.IPM shall reflect that the host has entered slumber (PxSSTS.IPM = 6h.)
7:4	0h RO	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed. 0h = Device not present or communication not established. 1h = Generation 1 communication rate negotiated. 2h = Generation 2 communication rate negotiated. 3h = Generation 3 communication rate negotiated. All other values reserved
3:0	0h RO	**Device Detection (DET):** Indicates the interface device detection and Phy state. 0h = No device detected and Phy communication not established. 1h = Device presence detected but Phy communication not established. 3h = Device presence detected and Phy communication established. 4h = Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved. Note that, while the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. Note: The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.

17.8.22 Port-Serial ATA Control (PxSCTL0)—Offset 12Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSCTL0: [ABAR] + 12Ch

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0												PMP				SPM				IPM				SPD				DET			

Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKP any request from the device to enter that state. 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3hTransitions to both PARTIAL and SLUMBER states disabled 4h Transitions to the DEVSLP power management state are disabled 5h Transitions to the Partial and DEVSLP power management states are disabled 6h Transitions to the Slumber and DEVSLP power management states are disabled 7h Transitions to the Partial, Slumber and DEVSLP power management states are disabled All other values reserved

Bit Range	Default & Access	Description
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface. 0h No speed negotiation restrictions. 1h Limit speed negotiation to Generation 1 communication rate. 2h Limit speed negotiation to a rate not greater than Generation 2 communication rate. 3h Limit speed negotiation to a rate not greater than Generation 3 communication rate. All other values reserved. Note: If software changes SPD after port has been enabled, software is required to perform a port reset via DET=1h.
3:0	0h RW	**Device Detection Initialization (DET):** Controls HBA's device detection and interface initialization. 0h No device detection or initialization action requested. 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is continuously transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h Disable the Serial ATA interface and put Phy in offline mode. All other values reserved. This field may only be changed when PxCMD.ST is '0'. Changing this field while the HBA is running results in undefined behavior. When PxCMD.ST is set to '1', this field should have a value of 0h. It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when PxSCTL.DET = 1h

17.8.23 Port-Serial ATA Error (PxSERR0)—Offset 130h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSERR0: [ABAR] + 130h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DIAG																ERR															

Bit Range	Default & Access	Description
31:16	0000h RW/1C	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bit Field 31:27 Reserved 26 Exchanged (X): When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. The means by which the implementation determines that the device presence has changed is vendor specific. This bit shall always be set to one anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit. 25 Unrecognized FIS Type (F): Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized. 24 Transport state transition error (T): Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. 23 Link Sequence Error (S): Indicates that one or more Link state machine error conditions were encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. 22 Handshake Error (H): Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 CRC Error (C): Indicates that one or more CRC errors occurred with the Link Layer. 20 Disparity Error (D): This field is not used by AHCI. 19 10B to 8B Decode Error (B): Indicates that one or more 10B to 8B decoding errors occurred. 18 Comm Wake (W): Indicates that a Comm Wake signal was detected by the Phy. 17 Phy Internal Error (I): Indicates that the Phy detected some internal error. 16 PhyRdy Change (N): When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. The state of this bit is reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled.

Bit Range	Default & Access	Description
15:0	0000h RW/1C	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. 15:12 Reserved 11 Internal Error (E): The SATA controller failed due to a master or target abort when attempting to access system memory. 10 Protocol Error (P): A violation of the Serial ATA protocol was detected. 9 Persistent Communication or Data Integrity Error (C): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 Transient Data Integrity Error (T): A data integrity error occurred that was not recovered by the interface. 7:2 Reserved 1 Recovered Communications Error (M): Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 Recovered Data Integrity Error (I): A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

17.8.24 Port-Serial ATA Active (PxSACT0)—Offset 134h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSACT0: [ABAR] + 134h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DS

Bit Range	Default & Access	Description
31:0	00000000h RW/1S	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS.

17.8.25 Port-Commands Issued (PxCI0)—Offset 138h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCI0: [ABAR] + 138h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CI

Bit Range	Default & Access	Description
31:0	00000000h RW	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST is set to 1.

17.8.26 Port-Device Sleep (PxDEVSLP0)—Offset 144h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxDEVSLP0: [ABAR] + 144h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 1E022852h

31			28				24				20				16				12				8				4				0
0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0
RSVD0			DM				DITO										MDAT					DETO								DSP	ADSE

Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:25	Fh RW/O	**DITO Multiplier (DM):** 0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITO actual = DITO * DM).
24:15	004h RW	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal.
14:10	0Ah RW	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granularity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The nominal value is 10ms and the minimum is 1ms depending on device identification information.
9:2	14h RW	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20ms while the max value is 255ms depending on device identification information.
1	1h RW/O	**DEVSLP Present (DSP):** If set to 1, the platform supports DEVSLP on this port. If cleared to 0, the platform does not support DEVSLP on this port.
0	0h RW	**Aggressive DEVSLP Enable (ADSE):** When this bit is cleared to 0, the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxDEVSLP.DSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the DEVSLP signal if asserted.

17.8.27 Port-Command List Base Address (PxCLB1)—Offset 180h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCLB1: [ABAR] + 180h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CLB																						RSVD0									

Bit Range	Default & Access	Description
31:10	000000h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0b RO	**RSVD0:** Reserved

17.8.28 Port-Command List Base Address Upper 32-bits (PxCLBU1)—Offset 184h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCLBU1: [ABAR] + 184h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CLBU																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

17.8.29 Port-FIS Base Address (PxFB1)—Offset 188h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxFB1: [ABAR] + 188h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FB																								RSVD0							

Bit Range	Default & Access	Description
31:8	0000000h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0b RO	**RSVD0:** Reserved

17.8.30 Port-FIS Base Address Upper 32-bits (PxFBU1)—Offset 18Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxFBU1: [ABAR] + 18Ch

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FBU																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

17.8.31 Port-Interrupt Status (PxIS1)—Offset 190h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxIS1: [ABAR] + 190h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CPDS	TFES	HBFS	HBDS	IFS	INFS	RSVD0	OFS	IPMS	PRCS	RSVD1														DMPS	PCS	DPS	UFS	SDBS	DSS	PSS	DHRS

Bit Range	Default & Access	Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h RW/1C	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0b RO	**RSVD0:** Reserved
24	0h RW/1C	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C	**Incorrect Port Multiplier Status (IPMS):** Not supported
22	0h RO	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0b RO	**RSVD1:** Reserved
7	0h RW/1C	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).
6	0h RO	**Port Connect Change Status (PCS):** 1=Change in Current Connect Status. 0=No change in Current Connect Status. This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared.
5	0h RW/1C	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.
4	0h RO	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.
2	0h RW/1C	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.
1	0h RW/1C	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

17.8.32 Port-Interrupt Enable (PxIE1)—Offset 194h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxIE1: [ABAR] + 194h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CPDS	TFEE	HBFE	HBDE	IFE	INFE	RSVD0	OFE	IPME	PRCE	RSVD1														DMPE	PCE	DPE	UFE	SDBE	DSE	PSE	DHRE

Bit Range	Default & Access	Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** When set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0b RO	**RSVD0:** Reserved
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interrupt.
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interrupt.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
21:8	0b RO	**RSVD1:** Reserved
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h RW	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.

Bit Range	Default & Access	Description
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

17.8.33 Port-Command (PxCMD1)—Offset 198h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxCMD1: [ABAR] + 198h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
ICC				ASP	ALPE	DLAE	ATAPI	APSTE	FBSCP	ESP	CPD	MPSP	HPCP	PMA	RSVD0	CR	FR	MPSS	CCS					RSVD1	PSP	APSE	FRE	CLO	POD	SUD	ST

Bit Range	Default & Access	Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four bit field which can be used to control reset and power states of the interface. If the Link layer is currently in the L_IDLE state, writes to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writes to this field shall have no effect. Fh -9h Reserved. 8h DEVSLP: This shall cause the HBA to assert the DEVSLP signal associated with the port; the HBA shall ignore the DEVSLP Idle Timeout value specified by PxDEVSLP.DITO. Software shall only request DEVSLP when the interface is in an idle state (i.e. PxCI is cleared to 0h and PxSACT is cleared to 0h); if the interface is not idle at the time the register is written, then the HBA takes no action and the interface remains in its current state. If PxCAP2.DESO is set to '1' and PxSSTS.IPM is not set to '6h', then the HBA takes no action and the interface remains in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion). 7h Reserved 6h Slumber: This shall cause the HBA to request a transition of the interface to the Slumber state. The SATA device may reject the request and the interface shall remain in its current state. 5h-3h Reserved. 2h Partial: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state. 1h Active: This shall cause the HBA to request a transition of the interface into the active state. If the requested transition is from the DEVSLP state, then the HBA shall wait until PxDEVSLP.DMAT has expired before de-asserting the DEVSLP signal. 0h No-Op / Idle: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and the software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state (with the exception of DEVSLP). The transition to DEVSLP may occur from any other state if CAP2.DESO is cleared to '0'. If CAP2.DESO is set to '1', then DEVSLP may only be transitioned to if the link is in Slumber.

Bit Range	Default & Access	Description
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter Partial state when it clears a bit in the PxCI or PxSACT register and the register values are both 0h. If CAP.SALP is cleard to 0, software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0. This bit is set by software
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** When set to 1, the HBA may perform Automatic Partial to Slumber Transitions. When cleared to 0 - the port shall not perform Automatic Partial to Slumber Transitions. Software shall only set this bit to 1 - if CAP2.APST is set to 1; if CAP2.APST is cleared to 0 - software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.
21	0h RW/O	**External SATA Port (ESP):** When set to 1, indicates that this port is routed externally and will be used with an external SATA device. When set to 1, CAP.SXS must also be set to 1. When cleared (0), indicates that this port is not routed externally and supports internal SATA devices only. If ESP is set to 1, then the port may experience hot plug events.
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user.
17	0h RO	**Port Multiplier Attached (PMA):** Not supported
16	0b RO	**RSVD0:** Reserved
15	0h RO	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running.
13	0h RO	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.

Bit Range	Default & Access	Description
12:8	00h RO	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7	0b RO	**RSVD1:** Reserved
6	0h RO	**PHYSLP Present (PSP):** If set to 1, the platform supports PHYSLP on this port. If cleared to 0, the platform does not support PHYSLP on this port. This bit may only be set to 1 if CAP2.SPS is set to 1.
5	0h RW	**Aggressive PHYSLP Enable (APSE):** This bit is read/write for HBAs that support aggressive PHYSLP management (CAP2.SAPM == 1). This bit is read-only for HBAs that do not support aggressive PHYSLP management (CAP2.SPS == 0). When this bit is set to 1, the HBA shall assert the PHYSLP signal after the port has been idle (PxCI == 0h and PxSACT == 0h) for the amount of time specified by the GHC.PITO register. When this bit is cleared to 0, the HBA does not enter PHYSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxCMD.PSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the PHYSLP signal if asserted.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW	**Spin-Up Device (SUD):** This bit is read/write for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1 for HBAs that do not support staggered spin-up. On an edge detect from 0 to 1, the HBA shall start a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

17.8.34 Port-Task File Data (PxTFD1)—Offset 1A0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxTFD1: [ABAR] + 1A0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 0000007Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
RSVD0																ERR								STS_BSY	STS_RSVD0			STS_DRQ	STS_RSVD1		STS_ERR

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RO	**Error (ERR):** Contains the latest copy of the task file error register.
7	0h RO	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	7h RO	**Status Rsvd0 (STS_RSVD0):** Status - Not Applicable.
3	1h RO	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	3h RO	**Status Rsvd1 (STS_RSVD1):** Status - Not Applicable.
0	1h RO	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

17.8.35 Port-Signature (PxSIG1)—Offset 1A4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSIG1: [ABAR] + 1A4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SIG																															

Bit Range	Default & Access	Description
31:0	FFFFFFFFh RO	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS.

17.8.36 Port-Serial ATA Status (PxSSTS1)—Offset 1A8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSSTS1: [ABAR] + 1A8h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
RSVD0					IPM	SPD	DET	

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11:8	0h RO	**Interface Power Management (IPM):** Indicates the current interface state 0h = Device not present or communication not established. 1h = Interface in active state. 2h = Interface in PARTIAL power management state. 6h = Interface in SLUMBER power management state. 8h = PHYSLP asserted. All other values reserved. This field reflects the interface power management state for both device and host initiated power management. Note: If an automatic partial to slumber transition occurs, PxSSTS.IPM shall reflect that the host has entered slumber (PxSSTS.IPM = 6h.)
7:4	0h RO	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed. 0h = Device not present or communication not established. 1h = Generation 1 communication rate negotiated. 2h = Generation 2 communication rate negotiated. 3h = Generation 3 communication rate negotiated. All other values reserved
3:0	0h RO	**Device Detection (DET):** Indicates the interface device detection and Phy state. 0h = No device detected and Phy communication not established. 1h = Device presence detected but Phy communication not established. 3h = Device presence detected and Phy communication established. 4h = Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved. Note that, while the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. Note: The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.

17.8.37 Port-Serial ATA Control (PxSCTL1)—Offset 1ACh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSCTL1: [ABAR] + 1ACh

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0												PMP				SPM				IPM				SPD				DET			

Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKP any request from the device to enter that state. 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3hTransitions to both PARTIAL and SLUMBER states disabled 4h Transitions to the DEVSLP power management state are disabled 5h Transitions to the Partial and DEVSLP power management states are disabled 6h Transitions to the Slumber and DEVSLP power management states are disabled 7h Transitions to the Partial, Slumber and DEVSLP power management states are disabled All other values reserved
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface. 0h No speed negotiation restrictions. 1h Limit speed negotiation to Generation 1 communication rate. 2h Limit speed negotiation to a rate not greater than Generation 2 communication rate. 3h Limit speed negotiation to a rate not greater than Generation 3 communication rate. All other values reserved. Note: If software changes SPD after port has been enabled, software is required to perform a port reset via DET=1h.
3:0	0h RW	**Device Detection Initialization (DET):** Controls HBA's device detection and interface initialization. 0h No device detection or initialization action requested. 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is continuously transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h Disable the Serial ATA interface and put Phy in offline mode. All other values reserved. This field may only be changed when PxCMD.ST is '0'. Changing this field while the HBA is running results in undefined behavior. When PxCMD.ST is set to '1', this field should have a value of 0h. It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when PxSCTL.DET = 1h

17.8.38 Port-Serial ATA Error (PxSERR1)—Offset 1B0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSERR1: [ABAR] + 1B0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DIAG																ERR															

Bit Range	Default & Access	Description
31:16	0000h RW/1C	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bit Field 31:27 Reserved 26 Exchanged (X): When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. The means by which the implementation determines that the device presence has changed is vendor specific. This bit shall always be set to one anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit. 25 Unrecognized FIS Type (F): Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized. 24 Transport state transition error (T): Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. 23 Link Sequence Error (S): Indicates that one or more Link state machine error conditions were encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. 22 Handshake Error (H): Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 CRC Error (C): Indicates that one or more CRC errors occurred with the Link Layer. 20 Disparity Error (D): This field is not used by AHCI. 19 10B to 8B Decode Error (B): Indicates that one or more 10B to 8B decoding errors occurred. 18 Comm Wake (W): Indicates that a Comm Wake signal was detected by the Phy. 17 Phy Internal Error (I): Indicates that the Phy detected some internal error. 16 PhyRdy Change (N): When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. The state of this bit is reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled.
15:0	0000h RW/1C	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. 15:12 Reserved 11 Internal Error (E): The SATA controller failed due to a master or target abort when attempting to access system memory. 10 Protocol Error (P): A violation of the Serial ATA protocol was detected. 9 Persistent Communication or Data Integrity Error (C): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 Transient Data Integrity Error (T): A data integrity error occurred that was not recovered by the interface. 7:2 Reserved 1 Recovered Communications Error (M): Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 Recovered Data Integrity Error (I): A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

17.8.39 Port-Serial ATA Active (PxSACT1)—Offset 1B4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxSACT1: [ABAR] + 1B4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DS

Bit Range	Default & Access	Description
31:0	00000000h RW/1S	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS.

17.8.40 Port-Commands Issued (PxCI1)—Offset 1B8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxCI1: [ABAR] + 1B8h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CI

Bit Range	Default & Access	Description
31:0	00000000h RW	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST is set to 1.

17.8.41 Port-Device Sleep (PxDEVSLP1)—Offset 1C4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PxDEVSLP1: [ABAR] + 1C4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 1E022852h

31			28				24				20				16				12				8				4				0
0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0
RSVD0			DM				DITO										MDAT					DETO								DSP	ADSE

Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:25	Fh RW/O	**DITO Multiplier (DM):** 0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITO actual = DITO * DM).
24:15	004h RW	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal.
14:10	0Ah RW	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granularity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The nominal value is 10ms and the minimum is 1ms depending on device identification information.
9:2	14h RW	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20ms while the max value is 255ms depending on device identification information.
1	1h RW/O	**DEVSLP Present (DSP):** If set to 1, the platform supports DEVSLP on this port. If cleared to 0, the platform does not support DEVSLP on this port.
0	0h RW	**Aggressive DEVSLP Enable (ADSE):** When this bit is cleared to 0, the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxDEVSLP.DSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the DEVSLP signal if asserted.

17.8.42 Enclosure Management Message Format (EM_MF)—Offset 580h

This register is not implemented in VLV.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

EM_MF: [ABAR] + 580h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																															

Bit Range	Default & Access	Description
31:0	0h RO	**RSVD:** Reserved.

17.8.43 Enclosure Management LED (EM_LED)—Offset 584h

This register is not implemented in VLV.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

EM_LED: [ABAR] + 584h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD

Bit Range	Default & Access	Description
31:0	0h RO	**RSVD:** Reserved.

17.9 SATA Primary Read Command IO Registers

Table 197. Summary of SATA Primary Read Command I/O Registers—PCMDIDEBA

Offset	Size	Register ID—Description	Default Value
1h	1	"Primary Channel Error register (P_ERROR)—Offset 1h" on page 2006	00h
2h	1	"Primary Channel Sector Count register (P_SECTOR_COUNT)—Offset 2h" on page 2006	00h
3h	1	"Primary Channel Sector Number register (P_SECTOR_NUMBER)—Offset 3h" on page 2007	00h
4h	1	"Primary Channel Cylinder Low register (P_CYL_LOW)—Offset 4h" on page 2008	00h
5h	1	"Primary Channel Cylinder High register (P_CYL_HIGH)—Offset 5h" on page 2008	00h
6h	1	"Primary Channel Device register (P_DRIVE_HEAD)—Offset 6h" on page 2009	00h
7h	1	"Primary Channel Status register (P_STATUS)—Offset 7h" on page 2009	00h

17.9.1 Primary Channel Error register (P_ERROR)—Offset 1h

Access Method

Type: I/O Register
(Size: 8 bits)

P_ERROR: [PCMDIDEBA] + 1h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0

P_ERROR_1

Bit Range	Default & Access	Description
7:0	00h RW	**Error (P_ERROR_1):** Error.

17.9.2 Primary Channel Sector Count register (P_SECTOR_COUNT)—Offset 2h

Access Method

Type: I/O Register
(Size: 8 bits)

P_SECTOR_COUNT: [PCMDIDEBA] + 2h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
P_SECTOR_COUNT_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Sector Count (P_SECTOR_COUNT_1):** Sector Count.

17.9.3 Primary Channel Sector Number register (P_SECTOR_NUMBER)—Offset 3h

Access Method

Type: I/O Register
(Size: 8 bits)

P_SECTOR_NUMBER: [PCMDIDEBA] + 3h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
P_SECTOR_NUMBER_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Sector Number (P_SECTOR_NUMBER_1):** Sector Number.

17.9.4 Primary Channel Cylinder Low register (P_CYL_LOW)—Offset 4h

Access Method

Type: I/O Register
(Size: 8 bits)

P_CYL_LOW: [PCMDIDEBA] + 4h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
P_CYL_LOW_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Cylinder Low (P_CYL_LOW_1):** Cylinder Low.

17.9.5 Primary Channel Cylinder High register (P_CYL_HIGH)—Offset 5h

Access Method

Type: I/O Register
(Size: 8 bits)

P_CYL_HIGH: [PCMDIDEBA] + 5h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
P_CYL_HIGH_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Cylinder High (P_CYL_HIGH_1):** Cylinder High.

17.9.6 Primary Channel Device register (P_DRIVE_HEAD)—Offset 6h

Access Method

Type: I/O Register
(Size: 8 bits)

P_DRIVE_HEAD: [PCMDIDEBA] + 6h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0			P_DRIVE_HEAD_1	RSVD1			

Bit Range	Default & Access	Description
7:5	0b RO	**RSVD0:** Reserved
4	0h RW	**Device (P_DRIVE_HEAD_1):** Device.
3:0	0b RO	**RSVD1:** Reserved

17.9.7 Primary Channel Status register (P_STATUS)—Offset 7h

Access Method

Type: I/O Register
(Size: 8 bits)

P_STATUS: [PCMDIDEBA] + 7h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
P_STATUS_BSY	P_STATUS_DRDY	P_STATUS_DF	RSVD0	P_STATUS_DRQ	RSVD1		P_STATUS_ERR_CHK

Bit Range	Default & Access	Description
7	0h RW	**BUSY (P_STATUS_BSY):** BUSY.

Bit Range	Default & Access	Description
6	0h RW	**Device Ready (P_STATUS_DRDY):** Device Ready.
5	0h RW	**Device Fault/Stream Error (P_STATUS_DF):** Device Fault/Stream Error.
4	0b RO	**RSVD0:** Reserved
3	0h RW	**Data Request (P_STATUS_DRQ):** Data Request.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**ERR/CHK (P_STATUS_ERR_CHK):** ERR/CHK.

17.10 SATA Primary Write Control IO Registers

Table 198. Summary of SATA Primary Write Control I/O Registers—PCTLIDEBA

Offset	Size	Register ID—Description	Default Value
2h	1	"Primary Channel Device Control register (P_DEVICE_CTRL)—Offset 2h" on page 2011	00h

17.10.1 Primary Channel Device Control register (P_DEVICE_CTRL)—Offset 2h

Access Method

Type: I/O Register
(Size: 8 bits)

P_DEVICE_CTRL: [PCTLIDEBA] + 2h

PCTLIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCTLIDEBA Reference: [B:0, D:19, F:0] + 104h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0					P_DEVICE_CTRL_SRST	P_DEVICE_CTRL_nIEN	RSVD1

Bit Range	Default & Access	Description
7:3	0b RO	**RSVD0:** Reserved
2	0h RW	**Soft Reset (P_DEVICE_CTRL_SRST):** Soft Reset.
1	0h RW	**Interrupt Enable, Negative Logic (P_DEVICE_CTRL_nIEN):** Interrupt Enable, Negative Logic.
0	0b RO	**RSVD1:** Reserved

17.11 SATA Primary Read Control IO Registers

Table 199. Summary of SATA Primary Read Control I/O Registers—PCTLIDEBA

Offset	Size	Register ID—Description	Default Value
2h	1	"Primary Channel Alternate Status register (P_ALT_STATUS)—Offset 2h" on page 2012	00h

17.11.1 Primary Channel Alternate Status register (P_ALT_STATUS)—Offset 2h

Access Method

Type: I/O Register
(Size: 8 bits)

P_ALT_STATUS: [PCTLIDEBA] + 2h

PCTLIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCTLIDEBA Reference: [B:0, D:19, F:0] + 104h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
P_ALT_STATUS_BSY	P_ALT_STATUS_DRDY	P_ALT_STATUS_DF	RSVD0	P_ALT_STATUS_DRQ	RSVD1		P_ALT_STATUS_ERR_CHK

Bit Range	Default & Access	Description
7	0h RW	**BUSY (P_ALT_STATUS_BSY):** BUSY.
6	0h RW	**Device Ready (P_ALT_STATUS_DRDY):** Device Ready.
5	0h RW	**Device Fault/Stream Error (P_ALT_STATUS_DF):** Device Fault/Stream Error.
4	0b RO	**RSVD0:** Reserved
3	0h RW	**Data Request (P_ALT_STATUS_DRQ):** Data Request.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**ERR/CHK (P_ALT_STATUS_ERR_CHK):** ERR/CHK.

17.12 SATA Primary Write Control IO Registers

Table 200. Summary of SATA Primary Write Control I/O Registers—PCTLIDEBA

Offset	Size	Register ID—Description	Default Value
2h	1	"Primary Channel Device Control register (P_DEVICE_CTRL)—Offset 2h" on page 2013	00h

17.12.1 Primary Channel Device Control register (P_DEVICE_CTRL)—Offset 2h

Access Method

Type: I/O Register
(Size: 8 bits)

P_DEVICE_CTRL: [PCTLIDEBA] + 2h

PCTLIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCTLIDEBA Reference: [B:0, D:19, F:0] + 104h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0					P_DEVICE_CTRL_SRST	P_DEVICE_CTRL_nIEN	RSVD1

Bit Range	Default & Access	Description
7:3	0b RO	**RSVD0:** Reserved
2	0h RW	**Soft Reset (P_DEVICE_CTRL_SRST):** Soft Reset.
1	0h RW	**Interrupt Enable, Negative Logic (P_DEVICE_CTRL_nIEN):** Interrupt Enable, Negative Logic.
0	0b RO	**RSVD1:** Reserved

17.13 SATA Secondary Read Command IO Registers

Table 201. Summary of SATA Secondary Read Command I/O Registers—SCMDIDEBA

Offset	Size	Register ID—Description	Default Value
1h	1	"Secondary Channel Error register (S_ERROR)—Offset 1h" on page 2014	00h
2h	1	"Secondary Channel Sector Count register (S_SECTOR_COUNT)—Offset 2h" on page 2015	00h
3h	1	"Secondary Channel Sector Number register (S_SECTOR_NUMBER)—Offset 3h" on page 2015	00h
4h	1	"Secondary Channel Cylinder Low register (S_CYL_LOW)—Offset 4h" on page 2016	00h
5h	1	"Secondary Channel Cylinder High register (S_CYL_HIGH)—Offset 5h" on page 2016	00h
6h	1	"Secondary Channel Device register (S_DRIVE_HEAD)—Offset 6h" on page 2017	00h
7h	1	"Secondary Channel Status register (S_STATUS)—Offset 7h" on page 2018	00h

17.13.1 Secondary Channel Error register (S_ERROR)—Offset 1h

Access Method

Type: I/O Register
(Size: 8 bits)

S_ERROR: [SCMDIDEBA] + 1h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_ERROR_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Error (S_ERROR_1):** Error.

17.13.2 Secondary Channel Sector Count register (S_SECTOR_COUNT)—Offset 2h

Access Method

Type: I/O Register
(Size: 8 bits)

S_SECTOR_COUNT: [SCMDIDEBA] + 2h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_SECTOR_COUNT_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Sector Count (S_SECTOR_COUNT_1):** Sector Count.

17.13.3 Secondary Channel Sector Number register (S_SECTOR_NUMBER)—Offset 3h

Access Method

Type: I/O Register
(Size: 8 bits)

S_SECTOR_NUMBER: [SCMDIDEBA] + 3h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_SECTOR_NUMBER_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Sector Number (S_SECTOR_NUMBER_1):** Sector Number.

17.13.4 Secondary Channel Cylinder Low register (S_CYL_LOW)—Offset 4h

Access Method

Type: I/O Register
(Size: 8 bits)

S_CYL_LOW: [SCMDIDEBA] + 4h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_CYL_LOW_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Cylinder Low (S_CYL_LOW_1):** Cylinder Low.

17.13.5 Secondary Channel Cylinder High register (S_CYL_HIGH)—Offset 5h

Access Method

Type: I/O Register
(Size: 8 bits)

S_CYL_HIGH: [SCMDIDEBA] + 5h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_CYL_HIGH_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Cylinder High (S_CYL_HIGH_1):** Cylinder High.

17.13.6 Secondary Channel Device register (S_DRIVE_HEAD)—Offset 6h

Access Method

Type: I/O Register
(Size: 8 bits)

S_DRIVE_HEAD: [SCMDIDEBA] + 6h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0			S_DRIVE_HEAD_1	RSVD1			

Bit Range	Default & Access	Description
7:5	0b RO	**RSVD0:** Reserved
4	0h RW	**Device (S_DRIVE_HEAD_1):** Device.
3:0	0b RO	**RSVD1:** Reserved

17.13.7 Secondary Channel Status register (S_STATUS)—Offset 7h

Access Method

Type: I/O Register
(Size: 8 bits)

S_STATUS: [SCMDIDEBA] + 7h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_STATUS_BSY	S_STATUS_DRDY	S_STATUS_DF	RSVD0	S_STATUS_DRQ	RSVD1		S_STATUS_ERR_CHK

Bit Range	Default & Access	Description
7	0h RW	**BUSY (S_STATUS_BSY):** BUSY.
6	0h RW	**Device Ready (S_STATUS_DRDY):** Device Ready.
5	0h RW	**Device Fault/Stream Error (S_STATUS_DF):** Device Fault/Stream Error.
4	0b RO	**RSVD0:** Reserved
3	0h RW	**Data Request (S_STATUS_DRQ):** Data Request.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**ERR/CHK (S_STATUS_ERR_CHK):** ERR/CHK.

17.14 SATA Secondary Write Command IO Registers

Table 202. Summary of SATA Secondary Write Command I/O Registers—SCMDIDEBA

Offset	Size	Register ID—Description	Default Value
1h	1	"Secondary Channel Features register (S_FEATURES)—Offset 1h" on page 2019	00h
7h	1	"Secondary Channel Command register (S_COMMAND)—Offset 7h" on page 2020	00h

17.14.1 Secondary Channel Features register (S_FEATURES)—Offset 1h

Access Method

Type: I/O Register
(Size: 8 bits)

S_FEATURES: [SCMDIDEBA] + 1h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0

S_FEATURES_1

Bit Range	Default & Access	Description
7:0	00h RW	**Features (S_FEATURES_1):** Features.

17.14.2 Secondary Channel Command register (S_COMMAND)—Offset 7h

Access Method

Type: I/O Register
(Size: 8 bits)

S_COMMAND: [SCMDIDEBA] + 7h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_COMMAND_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Command (S_COMMAND_1):** Command.

17.15 SATA Secondary Read Control IO Registers

Table 203. Summary of SATA Secondary Read Control I/O Registers—SCTLIDEBA

Offset	Size	Register ID—Description	Default Value
2h	1	"Secondary Channel Alternate Status register (S_ALT_STATUS)—Offset 2h" on page 2021	00h

17.15.1 Secondary Channel Alternate Status register (S_ALT_STATUS)—Offset 2h

Access Method

Type: I/O Register
(Size: 8 bits)

S_ALT_STATUS: [SCTLIDEBA] + 2h

SCTLIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCTLIDEBA Reference: [B:0, D:19, F:0] + 108h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_ALT_STATUS_BSY	S_ALT_STATUS_DRDY	S_ALT_STATUS_DF	RSVD0	S_ALT_STATUS_DRQ	RSVD1		S_ALT_STATUS_ERR_CHK

Bit Range	Default & Access	Description
7	0h RW	**BUSY (S_ALT_STATUS_BSY):** BUSY.
6	0h RW	**Device Ready (S_ALT_STATUS_DRDY):** Device Ready.
5	0h RW	**Device Fault/Stream Error (S_ALT_STATUS_DF):** Device Fault/Stream Error.
4	0b RO	**RSVD0:** Reserved
3	0h RW	**Data Request (S_ALT_STATUS_DRQ):** Data Request.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**ERR/CHK (S_ALT_STATUS_ERR_CHK):** ERR/CHK.

17.16 SATA Secondary Write Command IO Registers

Table 204. Summary of SATA Secondary Write Command I/O Registers—SCMDIDEBA

Offset	Size	Register ID—Description	Default Value
1h	1	"Secondary Channel Features register (S_FEATURES)—Offset 1h" on page 2022	00h
7h	1	"Secondary Channel Command register (S_COMMAND)—Offset 7h" on page 2023	00h

17.16.1 Secondary Channel Features register (S_FEATURES)—Offset 1h

Access Method

Type: I/O Register
(Size: 8 bits)

S_FEATURES: [SCMDIDEBA] + 1h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_FEATURES_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Features (S_FEATURES_1):** Features.

17.16.2 Secondary Channel Command register (S_COMMAND)—Offset 7h

Access Method

Type: I/O Register
(Size: 8 bits)

S_COMMAND: [SCMDIDEBA] + 7h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
S_COMMAND_1							

Bit Range	Default & Access	Description
7:0	00h RW	**Command (S_COMMAND_1):** Command.

17.17 SATA Lane 0 Electrical Register Address Map

Table 205. Summary of SATA Lane 0 Electrical Message Bus Registers—0xA3 (Global Offset 2200h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 2026	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 2028	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 2029	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 2030	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 2031	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 2032	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 2033	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 2034	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 2035	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 2036	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 2038	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 2039	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 2041	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 2042	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 2042	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 2044	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 2045	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 2047	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 2048	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 2049	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 2050	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 2051	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 2052	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 2053	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 2053	0001C020h

17.17.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword0: [Port: 0xA3] + (2200h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 00010080h

Bits	Default	Field
31:28	0 0 0 0	reg_txcfgchange_valid_delay_3_0
27:24	0 0 0 0	reg_txcfgchange_rst_delay_3_0
23	0	reserved500
22:18	0 0 0 0 0	reg_txcfgchange_width_4_0
17	0	reg_txcfgchange_ovrride
16	1	reg_tx2_soft_reset_n
15	0	reg_txswng_clksel
14	0	reg_rcvdetect_ovrd
13	0	reg_rcvdetected
12	0	reg_rcvdetectfinished
11	0	reg_rcvdetect_pulse_width_ovrd
10:8	0 0 0	reg_rcvdetect_pulse_width_2_0
7	1	reg_tx1_soft_reset_n
6	0	reg_tx_8b10b_bypass
5	0	reg_tx_laneup
4	0	reg_left_txfifo_rst_master2
3	0	reg_right_txfifo_rst_master2
2	0	reg_plllinksynch_ovrden
1	0	reg_plllinksynch_ovrd
0	0	reg_tx1_cmmdisparity

Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd______________________:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected_________________________:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished__________________:** override for rcvdetectfinished

Bit Range	Default & Access	Description
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

17.17.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword1: [Port: 0xA3] + (2200h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 00600060h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	reg_txfsm_4us_delay_7_0
23	0	reg_softreset_enable
22	1	cri_rxeb_eiosenable
21	1	cri_rxdigfiltsq_enable
20	0	reg_txfsm_delay_ovrd
19:16	0 0 0 0	reg_txfsm_4us_delay_11_8
15:14	0 0	reg_pclk_rate_1_0
13:12	0 0	reg_rate_1_0
11:9	0 0 0	reg_phymode_2_0
8	0	reg_modeovren
7:6	0 1	reg_datawidth
5	1	soft_reset_n
4	0	reg_diginelben
3	0	reg_digifelben
2	0	reg_strapgroup_ovrden
1	0	reg_yank_timer_done_b_ovrd
0	0	reg_yank_timer_done_b_ovrd_en

Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width

Bit Range	Default & Access	Description
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

17.17.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword2: [Port: 0xA3] + (2200h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	Default	Field
31:28	0 0 0 0	reg_rxpwrfsm_pibiasoff_delay_3_0
27:24	0 0 0 0	cri_sqdbexittimer_override_3_0
23:18	0 0 0 0 0 0	cri_sqdbentrytimer_override_5_0
17:16	0 0	reg_rxdrcgtsqsel_1_0
15	0	cri_reut_SlaveSideDataCheckingEn
14	0	cri_sqdbtimer_ovren
13	0	cri_rxpwrfsm_timer_ovren
12	0	reg_rxidle
11	0	cri_rxrawdata_sel
10	0	cri_dynkalign_eco3302703_mode
9	0	cri_dynkalign_eco3302703_ovren
8	0	reg_rxpwrfsm_pibiasoff_ovrride
7	0	cri_reset_kalignlck
6	0	cri_ebptrrst
5	0	cri_comdispfix
4	0	cri_forcebankhit
3:2	0 0	cri_kalignmode_1_0
1	0	cri_skpprocdis
0	0	cri_elasticbuffer_maskdis

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select

Bit Range	Default & Access	Description
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

17.17.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA3] + (2200h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 5515ACAAh

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0

cri_dfx_patbuf_55_48	cri_dfx_patbuf_63_56	cri_dfx_patbuf_71_64	cri_dfx_patbuf_79_72

Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

17.17.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword4: [Port: 0xA3] + (2200h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	0	0	0	0	0	1

cri_dfx_patbuf_23_16	cri_dfx_patbuf_31_24	cri_dfx_patbuf_39_32	cri_dfx_patbuf_47_40

Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

Bit Range	Default & Access	Description
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

17.17.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword5: [Port: 0xA3] + (2200h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00003E63h

Bits	31	30:28	27:26	25	24	23	22	21	20	19	18	17	16	15:8	7:0
Default	0	000	00	0	0	0	0	0	0	0	0	0	0	0011 1110	0110 0011
Field	cri_dfx_patbuftrain	cri_dfx_prbspoly_2_0	cri_dfx_patbufsize_1_0	cri_dfx_patbufloop	cri_dfx_patbufdwidth	cri_dfx_patbuftrainovr	cri_dfx_marginmode	cri_dfx_chk_sel	cri_dfx_patchken	cri_dfx_patgenen	cri_dfx_clrerrcnt	cri_dfx_lcereset	cri_dfx_lcestart	cri_dfx_patbuf_15_8	cri_dfx_patbuf_7_0

Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training

Bit Range	Default & Access	Description
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

17.17.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA3] + (2200h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: FFFFFFFFh

31:24	23:16	15:8	7:0
1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
cri_dfx_prbsseed_7_0	cri_dfx_prbsseed_15_8	cri_dfx_prbsseed_23_16	cri_dfx_prbsseed_31_24

Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.

Bit Range	Default & Access	Description
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

17.17.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword7: [Port: 0xA3] + (2200h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000009h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 1

Bits	Field
31:24	dfx_cri_errcnt_7_0
23:16	dfx_cri_errcnt_15_8
15	i_rxcaldone
14	dfx_cri_lcemgnerr
13	cri_dfx_patgen2active
12	dfx_cri_patbufallfail
11	dfx_cri_patchkactive
10	dfx_cri_patgenactive
9	dfx_cri_lcetraindone
8	dfx_cri_lcetrainactive
7	reserved501
6	cri_dfx_patgen2en
5:4	cri_dfx_maxerrcnt_1_0
3:0	cri_dfx_prbstraincnt_3_0

Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).

Bit Range	Default & Access	Description
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

17.17.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA3] + (2200h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 000000C4h

Bits	Default	Field
31	0	reg_partial
30	0	reg_slumber
29:27	000	reg_tx2_cdr_override_2_0
26:24	000	reg_cdr_override_2_0
23	0	reg_ebuffmode
22:21	00	reg_usedclockchannel_1_0
20	0	reg_usedclockchannel_ovrride
19	0	reg_gbl_ovrride
18	0	reg_tx1_pclkon_inp2
17	0	reg_tx2_pclkon_inp2
16	0	reg_tx2_txenable
15:12	0000	cri_rxeb_ptr_init_3_0
11	0	reg_powerfsm_ovrride
10	0	reg_suspend
9	0	reg_pclkcfginput
8	0	reg_useqclock
7:4	1100	cri_rxeb_hiwater_3_0
3:0	0100	cri_rxeb_lowater_3_0

Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2

Bit Range	Default & Access	Description
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

17.17.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

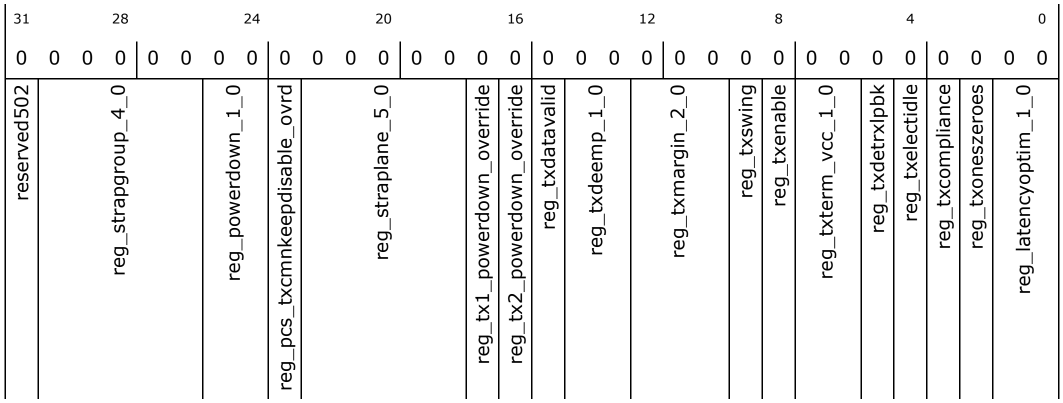
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA3] + (2200h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance

Bit Range	Default & Access	Description
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

17.17.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword10: [Port: 0xA3] + (2200h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:8	7	6	5	4	3	2	1	0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
Field	reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0	reg_rxpwrfsm_timer_ENABLE_RX_3_0	reg_rxpwrfsm_timer_RX_SQEN_3_0	reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0	reg_clk_valid_cnt_7_0	reg_rxterm	reg_rxpolarity	reg_rxeqtrain	reg_rxsquelchen	cri_rxpwrfsm_sqentimer_ovrden	reg_rxintfltren_override	reg_rxintfltren_l	reg_clk_valid_cnt_ovrd

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity

Bit Range	Default & Access	Description
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

17.17.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword11: [Port: 0xA3] + (2200h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0F000000h

Bits	Default	Field
31:30	0 0	reserved505
29	0	reserved506
28:24	0 1 1 1 1	reg_tx2_stagger_mask_4_0
23	0	i_clkbuf_iclken_ovrd
22	0	i_clkbuf_qclken_ovrd
21	0	reserved503
20	0	i_clkbuf_txclkmuxen_ovrd
19	0	reserved504
18	0	reg_tx2_cmmdisparity
17	0	reg_tx1_ctrl_override
16	0	reg_tx2_ctrl_override
15	0	reg_tx2_txterm_vcc_1
14	0	reg_tx2_txterm_vcc_0
13	0	reg_tx2_txdetrxlpbk
12	0	reg_tx2_txelectidle
11	0	reg_tx2_txcompliance
10	0	reg_tx2_txoneszeroes
9:8	0 0	reg_tx2_powerdown_1_0
7	0	o_captesten_h
6	0	i_captestout
5	0	fuse_override
4	0	i_clkbuf_ibiasen_ovrd
3	0	reg_lanedeskew_strap_ovrd
2	0	reg_lane_reverse
1	0	reg_left_txfifo_rst_master
0	0	reg_right_txfifo_rst_master

Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2

Bit Range	Default & Access	Description
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd______________:** reserved
2	0h RW	**reg_lane_reverse________________________:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____________:** reserved
0	0h RW	**reg_right_txfifo_rst_master___________:** reserved

17.17.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword12: [Port: 0xA3] + (2200h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00250F00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Field
31	reg_txfsm_200ns_ovrd
30:24	reg_txfsm_200ns_delay_6_0
23	reg_loadgen2txen_fall_ovrd
22:20	reg_tx2_stagger_mult_2_0
19	reg_lanestagger_by_group
18:16	reg_tx1_stagger_mult_2_0
15:14	reserved509
13	reserved510
12:8	reg_tx1_stagger_mask_4_0
7	reserved507
6	reg_lanestagger_strap_ovrd
5	reserved508
4:0	reg_lanestagger_strap_4_0

Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved

Bit Range	Default & Access	Description
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

17.17.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword13: [Port: 0xA3] + (2200h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31	30:29	28:24	23:16	15	14:13	12:8	7:0
Default	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0
Field	visa_en	reserved512	visa_clk_sel1_4_0	visa_lane_sel1_7_0	visa_bypass	reserved511	visa_clk_sel0_4_0	visa_lane_sel0_7_0

Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

17.17.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword14: [Port: 0xA3] + (2200h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 007A0018h

31	30	29	28:24	23:20	19:16	15:12	11:8	7	6	5	4	3	2:0
0	0	0	0 0 0 0 0	0 1 1 1	1 0 1 0	0 0 0 0	0 0 0 0	0	0	0	1	1	0 0 0
reg_clkbuf_stagger_ovrd	reg_clkbuf_stagger_cnt_10	reg_slowclk_ovrden	reg_txloadgenen2txen_fall_delay_4_0	o_cmlmuxsthsel_3_0	o_cmlsthsel_3_0	o_pcisel_3_0	o_pcqsel_3_0	o_phaseicen	o_phaseqcen	o_pcbypass	o_slowclocken	o_sclk250en	cri_kalign_com_cnt

Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

17.17.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword15: [Port: 0xA3] + (2200h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 04100300h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Field
31:29	reg_powermode_del_cfg_fifoptrgen_2_0
28	reg_clkbuf_en_ovrd
27	o_deskewen
26	reserved514
25	reserved515
24	reserved516
23	o_obsselectlocaldown_h
22	o_obsselectlocalup
21	o_obsselectm1datadown
20	o_obsselectm1dataup
19:18	o_obsselecttom2_1_0
17:16	o_obsselecttom1_1_0
15:14	reg_clkbuf_stagger_cnt_1_0
13:8	reserved513
7:0	reg_clkbuf_stagger_cnt_9_2

Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)

Bit Range	Default & Access	Description
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

17.17.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA3] + (2200h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

31	30:28 (28)	27	26	25	24	23:18 (20)	17:16 (16)	15:12 (12)	11:10	9:8 (8)	7:6	5:4 (4)	3	2	1	0
0	0 0 0	0	0	0	1	0 0 0 0 0 0	0 0	0 0 0 0	0 0	0 0	0 0	0 0	0	0	0	1
squelch_shunt_ovrd_en	squelch_shunt_cnt_2_0	reserved520	i_rxsqfsm_timersel	i_rxsq_asyncmode_h	i_rxsquelchstby_h	reserved519	cri_dfx_evenoddmask_1_0	reserved518	cri_dfx_lce2patsrc_1_0	cri_dfx_lcepatsrc_1_0	reserved517	txloadgen_ctr_val	cri_txhighpowerei_ovrden	cri_tx1highpowerei_ovrdval	cri_tx2highpowerei_ovrdval	p2_fast_exit_en

Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.

Bit Range	Default & Access	Description
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

17.17.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA3] + (2200h + 44h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

Bits	Default	Field
31:30	0 0	oirefdfxsel_1_0
29	0	iopampsfpen_h
28	0	iopampsfnen_h
27	0	iopamppen_h
26	0	iopampnen_h
25	0	monanapgen
24	1	monubufbypassen
23:22	0 0	reserved522
21	0	reg_ivrefen
20	0	ivrefen_ovrd
19:17	0 0 0	reserved523
16	0	oirefcurmonsel
15	0	lrcdisable
14:12	0 0 0	reserved521
11	0	lrc_rdy_pulsegen
10:9	0 0	lrc_rdy_target_1_0
8	0	lrc_rdy_ovd
7	0	rxtermpmrcen
6	0	rxvgapmrcen
5	0	txpmrcen
4	0	irefpmrcen
3	0	rxtermperrcen
2	0	rxvgaperrcen
1	0	txperrcen
0	1	irefperrcen

Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved

Bit Range	Default & Access	Description
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

17.17.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword18: [Port: 0xA3] + (2200h + 48h)

Op Codes:
0h - Read, 1h - Write

Default: 00008080h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Fields: reserved524 (31:27), reg_lrc_calcsonly (26), adcout_9_8 (25:24), adcout_7_0 (23:16), adc2_9_2 (15:8), adc1_9_2 (7:0)

Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimination filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimination filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

17.17.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA3] + (2200h + 4Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00004F10h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0

Fields: iamp0calcode_7_0 (31:24), cal_num (23:20), cal_start (19), cal_type (18), cal_inv (17), cal_rst (16), calclkdivsel_1_0 (15:14), reserved525 (13), calib_done (12), cal_fb_count (11:8), adc_acctime_1_0 (7:6), adc_clksel_1_0 (5:4), adcmuxsel_2_0 (3:1), adcstart (0)

Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [lyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

17.17.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA3] + (2200h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
rxvgarccode_7_0								rxtermrccode_7_0								txrccode_7_0								irefrccode_7_0							

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

17.17.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA3] + (2200h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
rxvgarcscale_7_0								rxtermrcscale_7_0								txrcscale_7_0								irefrcscale_7_0							

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

17.17.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword22: [Port: 0xA3] + (2200h + 58h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

rxvgarcoffset_7_0	rxtermrcoffset_7_0	txrcoffset_7_0	irefrcoffset_7_0

Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

17.17.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA3] + (2200h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
iclkqcfg_spare_7_0								iclkicfg_spare_7	iclkicfg_spare_6_3				iclkicfg_spare_2_0			reserved526				i_drvcfg_3_0				i_ploadcfg_3_0				ipbiasctrl_3_0			

Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

17.17.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword24: [Port: 0xA3] + (2200h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
reserved528								reserved527							cri_lanereset_clkgatectl	cri_lanereqforce	cri_susclkdisable_delay_4_0					cri_data_dynclkgate_mode_1_0		cri_eios_waittime_ovren	cri_eios_waittime_6_0						

Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (i.e. 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay .... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

17.18 PCI Express* Lane 0 Electrical Address Map

Table 206. Summary of PCI Express* Lane 0 Electrical Message Bus Registers—0xA6 (Global Offset 280h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 2055	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 2056	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 2057	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 2058	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 2059	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 2060	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 2060	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 2061	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 2062	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 2063	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 2064	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 2065	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 2067	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 2068	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 2069	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 2070	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 2071	00008A00h

17.18.1 TX_DWORD0 (tx_dword0)—Offset 0h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword0: [Port: 0xA6] + (280h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah

31			28				24				20				16				12				8				4				0
0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0
reserved504	ofrcr1main3_6_0							reserved503	reserved502							reserved501	reserved500							ofrcdrvr1r2	ofrcr1main0_6_0						

Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

17.18.2 TX_DWORD1 (tx_dword1)—Offset 4h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword1: [Port: 0xA6] + (280h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved510		ofrcr2short3_5_0						reserved509		reserved508						reserved507		reserved506						reserved505		ofrcr2short0_5_0					

Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

17.18.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (280h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 5580983Ah

31 28 24	23 20 16	15 12 8	7	6 4 0
0 1 0 1 0 1 0 1	1 0 0 0 0 0 0 0	1 0 0 1 1 0 0 0	0	0 1 1 1 0 1 0
omargin010_7_0	omargin000_7_0	ouniqtranscale_7_0	reserved511	ofrcslices_6_0

Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

17.18.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword3: [Port: 0xA6] + (280h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0C782040h

31	30	29:28	27:26	25	24	23:16	15:8	7:0
0	0	0 0	1 1	0	0	0 1 1 1 1 0 0 0	0 0 1 0 0 0 0 0	0 1 0 0 0 0 0 0
opisorate8b_h	obeacondivratio	ouniqetrangenmethod_1_0	oscaledcompmethod_1_0	odeemswinggenmethod	odownscaleampmethod	omargin101_7_0	omargin100_7_0	omargin011_7_0

Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p

Bit Range	Default & Access	Description
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

17.18.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword4: [Port: 0xA6] + (280h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 2B404D55h

31			28				24				20				16				12				8				4				0
0	0	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1
ow2tapdeemph9p5_7_0								ow2tapdeemph6p0_7_0								ow2tapgen2deemph3p5_7_0								ow2tapgen1deemph3p5_7_0							

Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

17.18.6 TX_DWORD5 (tx_dword5)—Offset 14h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (280h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ocalcinit	reserved515							reserved514								reserved513								reserved512							

Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

17.18.7 TX_DWORD6 (tx_dword6)—Offset 18h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword6: [Port: 0xA6] + (280h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved520	onswbypass_6_0							reserved519	opswbypass_6_0							reserved518	reserved517							ocalccont	reserved516						

Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved

Bit Range	Default & Access	Description
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

17.18.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA6] + (280h + 1Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0038383Fh

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 1 1 | 1 0 0 0 | 0 0 1 1 | 1 0 0 0 | 0 0 1 1 | 1 1 1 1

reserved527 | reserved526 | reserved525 | reserved524 | reserved523 | oslrctrlr2_l_2_0 | oslrctrlr2_h_2_0 | reserved522 | oslrctrl_l_2_0 | oslrctrl_h_2_0 | reserved521 | or2bypass_5_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved

Bit Range	Default & Access	Description
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

17.18.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword8: [Port: 0xA6] + (280h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 0600AA80h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0

Fields (bits 31 to 0): ontlpdtime_7_0 | ofrcdccoup_1_0 | obypbycomp | obypdftmode_4_0 | odftpisodata1_7_0 | odftpisodata0_1_0 | reserved529 | reserved528

Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG

Bit Range	Default & Access	Description
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

17.18.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA6] + (280h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00430C06h

31	30	29:27	26:24	23:22	21:20	19:18	17:16	15:8	7:0
0	0	000	000	01	00	00	11	00001100	00000110
ontlstrongpulling	ontlen	ontllowrefsel_2_0	ontlhighrefsel_2_0	ofrcsatamode_1_0	otxsusclkfreq_1_0	reserved530	orcvdtctrefselnosus_1_0	orcvdtctputime_7_0	ontlputime_7_0

Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active

Bit Range	Default & Access	Description
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

17.18.11 TX_DWORD10 (tx_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword10: [Port: 0xA6] + (280h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ispareread_7_0	reserved532	reserved531	ircvdtctcmpout	idftcaptestsig	idftrcvdetectedtxn	idftrcvdetectedtxp	idftrcvdetectfinished	intlfinished	intlpass_3_0

Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

17.18.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA6] + (280h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00001000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

oselsparetxclkin_2_0	ofrcdotprocess_2_0	ofrcgohighzdis	ofrcgohighzen	ofrcstrongpddis	ofrcstrongpden	ofrctxclkrootdis	ofrctxclkrooten	reserved537	ofrcpwrmodel1	ofrcpwrmodel0s	ofrcpwrmodel0	ofrccmkeeppadnen	ofrccmkeeppadpen	ofrccmkeeppadndis	ofrccmkeeppadpdis	omakedeeperfifo	ofrclatencyoptim_2_0	reserved536	ofrcrcvdtcten	otxrcvdtctclkrate_1_0	reserved535	reserved534	reserved533	oneloopbacken

Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

17.18.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA6] + (280h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31:30	29:27	26	25	24	23	22	21:20	19:18	17:16	15:12	11:8	7:4	3:0
Default	0 0	0 0 0	0	0	0	0	0	0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Field	otxclkbypsel_1_0	ofrcdataratefit_2_0	odistxfelbpin	otxclkampbypsn	otxclkampbypsp	reserved539	odfxanamuxen	odfxanamuxsel_1_0	obs_tx_gated_supply_1_0	reserved538	oobsdigselectupn_3_0	oobsdigselectupp_3_0	oobsdigselectdownn_3_0	oobsdigselectdownp_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - dataratefit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - dataratefit must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]

Bit Range	Default & Access	Description
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

17.18.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword13: [Port: 0xA6] + (280h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved543		ir2short3_5_0						reserved542		ir2short0_5_0						reserved541	ir1main3_6_0							reserved540	ir1main0_6_0						

Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

17.18.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (280h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 00400000h

Bits	31:30	29	28	27	26	25	24	23	22	21:19	18:16	15	14:12	11:8	7	6:4	3:0
Default	0 0	0	0	0	0	0	0	0	1	0 0 0	0 0 0	0	0 0 0	0 0 0 0	0	0 0 0	0 0 0 0
Field	ospare1_1_0	osimmode	ontlmodepin2pin	ofrcdatapathdis	ofrcdatapathen	ofrcdrvbypdis	ofrcdrvbypen	odfttxclkcaptesten	otxdccbyps_l	ofrcnmos32idv_2_0	ofrcpmos32idv_2_0	visa_en	ovisa1_clksel_2_0	ovisa1_lanesel_3_0	ovisa_bypass	ovisa0_clksel_2_0	ovisa0_lanesel_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

17.18.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (280h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

reserved551 | reserved550 | reserved549 | reserved548 | reserved547 | reserved546 | reserved545 | reserved544

Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

17.18.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword16: [Port: 0xA6] + (280h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 00008A00h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

Bits	Field
31:24	reserved554
23:16	reserved553
15:13	ocurconp0ei_2_0
12	reserved552
11:10	omediumcmpadn_1_0
9:8	omediumcmpadp_1_0
7:4	ospare3_3_0
3:0	ospare2_3_0

Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

17.19 SATA Lane 1 Electrical Register Address Map

Table 207. Summary of SATA Lane 1 Electrical Message Bus Registers—0xA3 (Global Offset 2400h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 2072	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 2074	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 2075	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 2077	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 2078	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 2078	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 2080	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 2080	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 2081	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 2083	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 2084	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 2085	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 2087	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 2088	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 2089	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 2090	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 2092	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 2093	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 2095	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 2096	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 2097	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 2098	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 2099	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 2099	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 2100	0001C020h

17.19.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword0: [Port: 0xA3] + (2400h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 00010080h

Bits	31:28	27:24	23	22:18	17	16	15	14	13	12	11	10:8	7	6	5	4	3	2	1	0
Default	0 0 0 0	0 0 0 0	0	0 0 0 0 0	0	1	0	0	0	0	0	0 0 0	1	0	0	0	0	0	0	0
Field	reg_txcfgchange_valid_delay_3_0	reg_txcfgchange_rst_delay_3_0	reserved500	reg_txcfgchange_width_4_0	reg_txcfgchange_ovrride	reg_tx2_soft_reset_n	reg_txswng_clksel	reg_rcvdetect_ovrd___	reg_rcvdetected___	reg_rcvdetectfinished___	reg_rcvdetect_pulse_width_ovrd	reg_rcvdetect_pulse_width_2_0	reg_tx1_soft_reset_n	reg_tx_8b10b_bypass	reg_tx_laneup	reg_left_txfifo_rst_master2	reg_right_txfifo_rst_master2	reg_plllinksynch_ovrden	reg_plllinksynch_ovrd	reg_tx1_cmmdisparity

Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd_______________________:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected___________________________:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished___________________:** override for rcvdetectfinished
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass

Bit Range	Default & Access	Description
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

17.19.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA3] + (2400h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 00600060h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	reg_txfsm_4us_delay_7_0
23	0	reg_softreset_enable
22	1	cri_rxeb_eiosenable
21	1	cri_rxdigfiltsq_enable
20	0	reg_txfsm_delay_ovrd
19:16	0 0 0 0	reg_txfsm_4us_delay_11_8
15:14	0 0	reg_pclk_rate_1_0
13:12	0 0	reg_rate_1_0
11:9	0 0 0	reg_phymode_2_0
8	0	reg_modeovren
7:6	0 1	reg_datawidth
5	1	soft_reset_n
4	0	reg_diginelben
3	0	reg_digifelben
2	0	reg_strapgroup_ovrden
1	0	reg_yank_timer_done_b_ovrd
0	0	reg_yank_timer_done_b_ovrd_en

Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down

Bit Range	Default & Access	Description
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

17.19.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword2: [Port: 0xA3] + (2400h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:28	reg_rxpwrfsm_pibiasoff_delay_3_0
27:24	cri_sqdbexittimer_override_3_0
23:18	cri_sqdbentrytimer_override_5_0
17:16	reg_rxdrcgtsqsel_1_0
15	cri_reut_SlaveSideDataCheckingEn
14	cri_sqdbtimer_ovren
13	cri_rxpwrfsm_timer_ovren
12	reg_rxidle
11	cri_rxrawdata_sel
10	cri_dynkalign_eco3302703_mode
9	cri_dynkalign_eco3302703_ovren
8	reg_rxpwrfsm_pibiasoff_ovrride
7	cri_reset_kalignlck
6	cri_ebptrrst
5	cri_comdispfix
4	cri_forcebankhit
3:2	cri_kalignmode_1_0
1	cri_skpprocdis
0	cri_elasticbuffer_maskdis

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode

Bit Range	Default & Access	Description
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

17.19.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA3] + (2400h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 5515ACAAh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
cri_dfx_patbuf_55_48								cri_dfx_patbuf_63_56								cri_dfx_patbuf_71_64								cri_dfx_patbuf_79_72							

Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

17.19.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword4: [Port: 0xA3] + (2400h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 1 0 1	0 1 1 1	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	1 1 0 0	0 0 0 1

31:24	23:16	15:8	7:0
cri_dfx_patbuf_23_16	cri_dfx_patbuf_31_24	cri_dfx_patbuf_39_32	cri_dfx_patbuf_47_40

Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

17.19.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword5: [Port: 0xA3] + (2400h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00003E63h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	1 1 1 0	0 1 1 0	0 0 1 1

31	30:28	27:26	25	24	23	22	21	20	19	18	17	16	15:8	7:0
cri_dfx_patbuftrain	cri_dfx_prbspoly_2_0	cri_dfx_patbufsize_1_0	cri_dfx_patbufloop	cri_dfx_patbufdwidth	cri_dfx_patbuftrainovr	cri_dfx_marginmode	cri_dfx_chk_sel	cri_dfx_patchken	cri_dfx_patgenen	cri_dfx_clrerrcnt	cri_dfx_lcereset	cri_dfx_lcestart	cri_dfx_patbuf_7_0	cri_dfx_patbuf_15_8

Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

17.19.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword6: [Port: 0xA3] + (2400h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: FFFFFFFFh

Bits	31:24	23:16	15:8	7:0
Default	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Field	cri_dfx_prbsseed_7_0	cri_dfx_prbsseed_15_8	cri_dfx_prbsseed_23_16	cri_dfx_prbsseed_31_24

Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

17.19.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword7: [Port: 0xA3] + (2400h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000009h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	dfx_cri_errcnt_7_0
23:16	0 0 0 0 0 0 0 0	dfx_cri_errcnt_15_8
15	0	i_rxcaldone
14	0	dfx_cri_lcemgnerr
13	0	cri_dfx_patgen2active
12	0	dfx_cri_patbufallfail
11	0	dfx_cri_patchkactive
10	0	dfx_cri_patgenactive
9	0	dfx_cri_lcetraindone
8	0	dfx_cri_lcetrainactive
7	0	reserved501
6	0	cri_dfx_patgen2en
5:4	0 0	cri_dfx_maxerrcnt_1_0
3:0	1 0 0 1	cri_dfx_prbstraincnt_3_0

Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

17.19.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA3] + (2400h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 000000C4h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0
reg_partial	reg_slumber	reg_tx2_cdr_override_2_0			reg_cdr_override_2_0			reg_ebuffmode	reg_usedclockchannel_1_0		reg_usedclockchannel_ovrride	reg_gbl_ovrride	reg_tx1_pclkon_inp2	reg_tx2_pclkon_inp2	reg_tx2_txenable	cri_rxeb_ptr_init_3_0				reg_powerfsm_ovrride	reg_suspend	reg_pclkcfginput	reg_useqclock	cri_rxeb_hiwater_3_0				cri_rxeb_lowater_3_0			

Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed

Bit Range	Default & Access	Description
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

17.19.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword9: [Port: 0xA3] + (2400h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved502 | reg_strapgroup_4_0 | reg_powerdown_1_0 | reg_pcs_txcmnkeepdisable_ovrd | reg_straplane_5_0 | reg_tx1_powerdown_override | reg_tx2_powerdown_override | reg_txdatavalid | reg_txdeemp_1_0 | reg_txmargin_2_0 | reg_txswing | reg_txenable | reg_txterm_vcc_1_0 | reg_txdetrxlpbk | reg_txelectidle | reg_txcompliance | reg_txoneszeroes | reg_latencyoptim_1_0

Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph

Bit Range	Default & Access	Description
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

17.19.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword10: [Port: 0xA3] + (2400h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:8	7	6	5	4	3	2	1	0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
Field	reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0	reg_rxpwrfsm_timer_ENABLE_RX_3_0	reg_rxpwrfsm_timer_RX_SQEN_3_0	reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0	reg_clk_valid_cnt_7_0	reg_rxterm	reg_rxpolarity	reg_rxeqtrain	reg_rxsquelchen	cri_rxpwrfsm_sqentimer_ovrden	reg_rxintfltren_override	reg_rxintfltren_l	reg_clk_valid_cnt_ovrd

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

17.19.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword11: [Port: 0xA3] + (2400h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0F000000h

Bits	Default	Field
31:30	0 0	reserved505
29	0	reserved506
28:24	0 1 1 1 1	reg_tx2_stagger_mask_4_0
23	0	i_clkbuf_iclken_ovrd
22	0	i_clkbuf_qclken_ovrd
21	0	reserved503
20	0	i_clkbuf_txclkmuxen_ovrd
19	0	reserved504
18	0	reg_tx2_cmmdisparity
17	0	reg_tx1_ctrl_override
16	0	reg_tx2_ctrl_override
15	0	reg_tx2_txterm_vcc_1
14	0	reg_tx2_txterm_vcc_0
13	0	reg_tx2_txdetrxlpbk
12	0	reg_tx2_txelectidle
11	0	reg_tx2_txcompliance
10	0	reg_tx2_txoneszeroes
9:8	0 0	reg_tx2_powerdown_1_0
7	0	o_captesten_h
6	0	i_captestout
5	0	fuse_override
4	0	i_clkbuf_ibiasen_ovrd
3	0	reg_lanedeskew_strap_ovrd
2	0	reg_lane_reverse
1	0	reg_left_txfifo_rst_master
0	0	reg_right_txfifo_rst_master

Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2

Bit Range	Default & Access	Description
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd______________:** reserved
2	0h RW	**reg_lane_reverse________________________:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____________:** reserved
0	0h RW	**reg_right_txfifo_rst_master____________:** reserved

17.19.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword12: [Port: 0xA3] + (2400h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00250F00h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Field
31	reg_txfsm_200ns_ovrd
30:24	reg_txfsm_200ns_delay_6_0
23	reg_loadgen2txen_fall_ovrd
22:20	reg_tx2_stagger_mult_2_0
19	reg_lanestagger_by_group
18:16	reg_tx1_stagger_mult_2_0
15:14	reserved509
13	reserved510
12:8	reg_tx1_stagger_mask_4_0
7	reserved507
6	reg_lanestagger_strap_ovrd
5	reserved508
4:0	reg_lanestagger_strap_4_0

Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

17.19.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA3] + (2400h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31	30:29	28:24	23:16	15	14:13	12:8	7:0
Default	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0
Field	visa_en	reserved512	visa_clk_sel1_4_0	visa_lane_sel1_7_0	visa_bypass	reserved511	visa_clk_sel0_4_0	visa_lane_sel0_7_0

Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

17.19.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword14: [Port: 0xA3] + (2400h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 007A0018h

Bits	Default	Field
31	0	reg_clkbuf_stagger_ovrd
30	0	reg_clkbuf_stagger_cnt_10
29	0	reg_slowclk_ovrden
28:24	0 0 0 0 0	reg_txloadgenen2txen_fall_delay_4_0
23:20	0 1 1 1	o_cmlmuxsthsel_3_0
19:16	1 0 1 0	o_cmlsthsel_3_0
15:12	0 0 0 0	o_pcisel_3_0
11:8	0 0 0 0	o_pcqsel_3_0
7	0	o_phaseicen
6	0	o_phaseqcen
5	0	o_pcbypass
4	1	o_slowclocken
3	1	o_sclk250en
2:0	0 0 0	cri_kalign_com_cnt

Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

17.19.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword15: [Port: 0xA3] + (2400h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 04100300h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
reg_powermode_del_cfg_fifoptrgen_2_0			reg_clkbuf_en_ovrd	o_deskewen	reserved514	reserved515	reserved516	o_obsselectlocaldown_h	o_obsselectlocalup	o_obsselectm1datadown	o_obsselectm1dataup	o_obsselecttom2_1_0		o_obsselecttom1_1_0		reg_clkbuf_stagger_cnt_1_0		reserved513						reg_clkbuf_stagger_cnt_9_2							

Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

17.19.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA3] + (2400h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

Bits	Default	Field
31	0	squelch_shunt_ovrd_en
30:28	0 0 0	squelch_shunt_cnt_2_0
27	0	reserved520
26	0	i_rxsqfsm_timersel
25	0	i_rxsq_asyncmode_h
24	1	i_rxsquelchstby_h
23:18	0 0 0 0 0 0	reserved519
17:16	0 0	cri_dfx_evenoddmask_1_0
15:12	0 0 0 0	reserved518
11:10	0 0	cri_dfx_lce2patsrc_1_0
9:8	0 0	cri_dfx_lcepatsrc_1_0
7:6	0 0	reserved517
5:4	0 0	txloadgen_ctr_val
3	0	cri_txhighpowerei_ovrden
2	0	cri_tx1highpowerei_ovrdval
1	0	cri_tx2highpowerei_ovrdval
0	1	p2_fast_exit_en

Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.

Bit Range	Default & Access	Description
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

17.19.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword17: [Port: 0xA3] + (2400h + 44h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

oirefdfxsel_1_0	iopampsfpen_h	iopampsfnen_h	iopamppen_h	iopampnen_h	monanapgen	monubufbypassen	reserved522	reg_ivrefen	ivrefen_ovrd	reserved523	oirefcurmonsel	lrcdisable	reserved521	lrc_rdy_pulsegen	lrc_rdy_target_1_0	lrc_rdy_ovd	rxtermpmrcen	rxvgapmrcen	txpmrcen	irefpmrcen	rxtermperrcen	rxvgaperrcen	txperrcen	irefperrcen

Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode

Bit Range	Default & Access	Description
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

17.19.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA3] + (2400h + 48h)

Op Codes:
0h - Read, 1h - Write

Default: 00008080h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Field
31:27	reserved524
26	reg_lrc_calcsonly
25:24	adcout_9_8
23:16	adcout_7_0
15:8	adc2_9_2
7:0	adc1_9_2

Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimination filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimination filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

17.19.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA3] + (2400h + 4Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00004F10h

Bits	31:24	23:20	19	18	17	16	15:14	13	12	11:8	7:6	5:4	3:1	0
Value	0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	0	0 1	0	0	1 1 1 1	0 0	0 1	0 0 0	0
Field	iamp0calcode_7_0	cal_num	cal_start	cal_type	cal_inv	cal_rst	calclkdivsel_1_0	reserved525	calib_done	cal_fb_count	adc_acctime_1_0	adc_clksel_1_0	adcmuxsel_2_0	adcstart

Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [lyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single

Bit Range	Default & Access	Description
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

17.19.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA3] + (2400h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

rxvgarccode_7_0 | rxtermrccode_7_0 | txrccode_7_0 | irefrccode_7_0

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

17.19.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA3] + (2400h + 54h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
rxvgarcscale_7_0								rxtermrcscale_7_0								txrcscale_7_0								irefrcscale_7_0							

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

17.19.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA3] + (2400h + 58h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
rxvgarcoffset_7_0	rxtermrcoffset_7_0	txrcoffset_7_0	irefrcoffset_7_0

Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

17.19.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA3] + (2400h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h

31:24	23	22:19	18:16	15:12	11:8	7:4	3:0
0 0 0 0 0 0 0 0	0	0 0 1 1	0 0 0	0 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0
iclkqcfg_spare_7_0	iclkicfg_spare_7	iclkicfg_spare_6_3	iclkicfg_spare_2_0	reserved526	i_drvcfg_3_0	i_ploadcfg_3_0	ipbiasctrl_3_0

Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

17.19.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword24: [Port: 0xA3] + (2400h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h

31:24	23:17	16	15	14:10	9:8	7	6:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1	1	1 0 0 0 0	0 0	0	0 1 0 0 0 0 0
reserved528	reserved527	cri_lanereset_clkgatectl	cri_lanereqforce	cri_susclkdisable_delay_4_0	cri_data_dynclkgate_mode_1_0	cri_eios_waittime_ovren	cri_eios_waittime_6_0

Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved

Bit Range	Default & Access	Description
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (i.e. 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay .... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

17.20 SATA Lane 1 Electrical Register Address Map

Table 208. Summary of SATA Lane 1 Electrical Message Bus Registers—0xA3 (Global Offset 2480h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 2102	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 2103	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 2104	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 2104	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 2106	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 2107	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 2107	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 2108	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 2109	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 2110	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 2111	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 2112	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 2113	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 2115	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 2116	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 2117	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 2118	00008A00h

17.20.1 TX_DWORD0 (tx_dword0)—Offset 0h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword0: [Port: 0xA3] + (2480h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah

Bits	Default	Field
31	0	reserved504
30:24	0 1 0 0 1 1 0	ofrcr1main3_6_0
23	0	reserved503
22:16	0 0 0 0 0 0 0	reserved502
15	0	reserved501
14:8	0 0 0 0 0 0 0	reserved500
7	0	ofrcdrvr1r2
6:0	0 1 1 1 0 1 0	ofrcr1main0_6_0

Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

17.20.2 TX_DWORD1 (tx_dword1)—Offset 4h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA3] + (2480h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved510		ofrcr2short3_5_0						reserved509		reserved508						reserved507		reserved506						reserved505		ofrcr2short0_5_0					

Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

17.20.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword2: [Port: 0xA3] + (2480h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 5580983Ah

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	1	1	0	1	0
omargin010_7_0								omargin000_7_0								ouniqtranscale_7_0								reserved511	ofrcslices_6_0						

Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

17.20.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword3: [Port: 0xA3] + (2480h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0C782040h

Bit	31	30	29:28	27:26	25	24	23:16	15:8	7:0
Default	0	0	0 0	1 1	0	0	0 1 1 1 1 0 0 0	0 0 1 0 0 0 0 0	0 1 0 0 0 0 0 0
Field	opisorate8b_h	obeacondivratio	ouniqetrangenmethod_1_0	oscaledcompmethod_1_0	odeemswinggenmethod	odownscaleampmethod	omargin101_7_0	omargin100_7_0	omargin011_7_0

Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

17.20.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

Type: Message Bus Register (Size: 32 bits)	**tx_dword4:** [Port: 0xA3] + (2480h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 2B404D55h

31:24	23:16	15:8	7:0
0 0 1 0 1 0 1 1	0 1 0 0 0 0 0 0	0 1 0 0 1 1 0 1	0 1 0 1 0 1 0 1
ow2tapdeemph9p5_7_0	ow2tapdeemph6p0_7_0	ow2tapgen2deemph3p5_7_0	ow2tapgen1deemph3p5_7_0

Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

17.20.6 TX_DWORD5 (tx_dword5)—Offset 14h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword5: [Port: 0xA3] + (2480h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bit	31	30:24	23:16	15:8	7:0
Default	0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	ocalcinit	reserved515	reserved514	reserved513	reserved512

Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

17.20.7 TX_DWORD6 (tx_dword6)—Offset 18h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword6: [Port: 0xA3] + (2480h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h

Bit	31	30:24	23	22:16	15	14:8	7	6:0
Default	0	0 0 1 1 1 1 1	0	0 1 0 0 0 0 0	0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0
Field	reserved520	onswbypass_6_0	reserved519	opswbypass_6_0	reserved518	reserved517	ocalccont	reserved516

Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved

Bit Range	Default & Access	Description
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

17.20.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword7: [Port: 0xA3] + (2480h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	1

reserved527, reserved526, reserved525, reserved524, reserved523, oslrctrlr2_l_2_0, oslrctrlr2_h_2_0, reserved522, oslrctrl_l_2_0, oslrctrl_h_2_0, reserved521, or2bypass_5_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved

Bit Range	Default & Access	Description
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

17.20.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword8: [Port: 0xA3] + (2480h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 0600AA80h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
ontlpdtime_7_0								ofrcdccoup_1_0		obypbycomp	obypdftmode_4_0					odftpisodata1_7_0								odftpisodata0_1_0		reserved529			reserved528		

Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG

Bit Range	Default & Access	Description
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

17.20.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA3] + (2480h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00430C06h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0
ontlstrongpulling	ontlen	ontllowrefsel_2_0			ontlhighrefsel_2_0			ofrcsatamode_1_0		otxsusclkfreq_1_0		reserved530		orcvdtctrefselnosus_1_0		orcvdtctputime_7_0								ontlputime_7_0							

Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active

Bit Range	Default & Access	Description
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

17.20.11 TX_DWORD10 (tx_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword10: [Port: 0xA3] + (2480h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:24	ispareread_7_0
23:16	reserved532
15:10	reserved531
9	ircvdtctcmpout
8	idftcaptestsig
7	idftrcvdetectedtxn
6	idftrcvdetectedtxp
5	idftrcvdetectfinished
4	intlfinished
3:0	intlpass_3_0

Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

17.20.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword11: [Port: 0xA3] + (2480h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00001000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

oselsparetxclkin_2_0 | ofrcdotprocess_2_0 | ofrcgohighzdis | ofrcgohighzen | ofrcstrongpddis | ofrcstrongpden | ofrctxclkrootdis | ofrctxclkrooten | reserved537 | ofrcpwrmodel1 | ofrcpwrmodel0s | ofrcpwrmodel0 | ofrccmkeeppadnen | ofrccmkeeppadpen | ofrccmkeeppadndis | ofrccmkeeppadpdis | omakedeeperfifo | ofrclatencyoptim_2_0 | reserved536 | ofrcrcvdtcten | otxrcvdtctclkrate_1_0 | reserved535 | reserved534 | reserved533 | oneloopbacken

Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

17.20.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA3] + (2480h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31:30	29:27	26	25	24	23	22	21:20	19:18	17:16	15:12	11:8	7:4	3:0
Default	0 0	0 0 0	0	0	0	0	0	0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Field	otxclkbypsel_1_0	ofrcdataratefit_2_0	odistxfelbpin	otxclkampbypsn	otxclkampbypsp	reserved539	odfxanamuxen	odfxanamuxsel_1_0	obs_tx_gated_supply_1_0	reserved538	oobsdigselectupn_3_0	oobsdigselectupp_3_0	oobsdigselectdownn_3_0	oobsdigselectdownp_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - dataratefit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - dataratefit must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

17.20.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA3] + (2480h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31:30	29:24	23:22	21:16	15	14:8	7	6:0
0 0	0 0 0 0 0 0	0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0
reserved543	ir2short3_5_0	reserved542	ir2short0_5_0	reserved541	ir1main3_6_0	reserved540	ir1main0_6_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

17.20.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA3] + (2480h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 00400000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ospare1_1_0		osimmode	ontlmodepin2pin	ofrcdatapathdis	ofrcdatapathen	ofrcdrvbypdis	ofrcdrvbypen	odfttxclkcaptesten	otxdccbyps_l	ofrcnmos32idv_2_0			ofrcpmos32idv_2_0			visa_en	ovisa1_clksel_2_0			ovisa1_lanesel_3_0				ovisa_bypass	ovisa0_clksel_2_0			ovisa0_lanesel_3_0			

Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

17.20.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA3] + (2480h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31:30	29:24	23:22	21:16	15	14:8	7	6:0
0 0	0 0 0 0 0 0	0 0	0 0 0 0 0 0	0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0
reserved551	reserved550	reserved549	reserved548	reserved547	reserved546	reserved545	reserved544

Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

17.20.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword16: [Port: 0xA3] + (2480h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 00008A00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
reserved554								reserved553								ocurconp0ei_2_0			reserved552	omediumcmpadn_1_0		omediumcmpadp_1_0		ospare3_3_0				ospare2_3_0			

Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

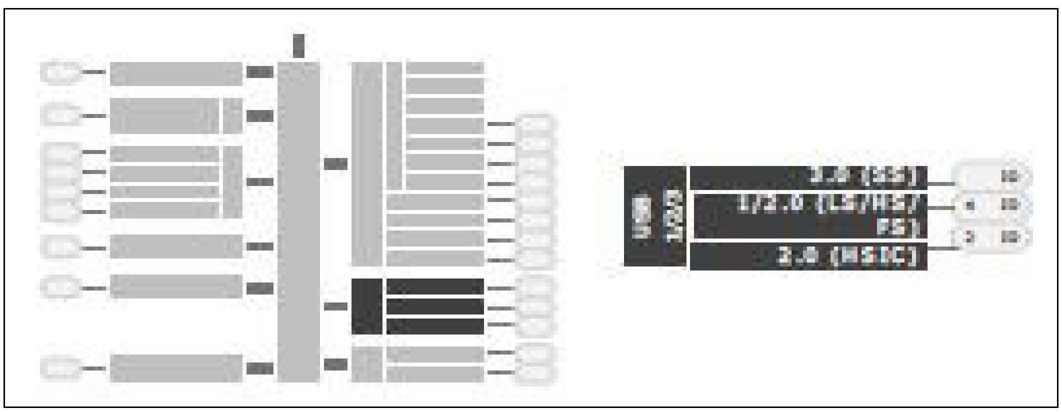
18 USB Host Controller Interfaces (xHCI, EHCI)

The USB Host Controllers (xHCI, EHCI) supports:

- One (1) Super Speed (SS) port on xHCI
- Four (4) Low Speed (LS)/Full Speed (FS)/High Speed (HS) ports on xHCI or EHCI
- Two (2) High Speed (HS) High Speed Inter-Chip (HSIC) ports on xHCI

Note: The SS port must share a LS/FS/HS port to have a full SS connector leaving three LS/FS/HS ports available.

Note: Only one host controller (either xHCI or EHCI) can be used. To enable HSIC and SS ports, xHCI must be used.



18.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 209. USB 3 SS Signals

Signal Name	Direction Plat Power	Description
USB3_TXP/N[0]	O V1P0A	**Data Out:** High speed serialized data outputs. Used for debug mode in xHCI operation.
USB3_RXP/N[0]	I V1P0A	**Data In:** High speed serialized data inputs. Used for debug mode in xHCI operation.
USB3_REXT[0]	I	**Resistor Compensation:** An external resistor must be connected between this pin and package ground. Contact your Intel representative for details.

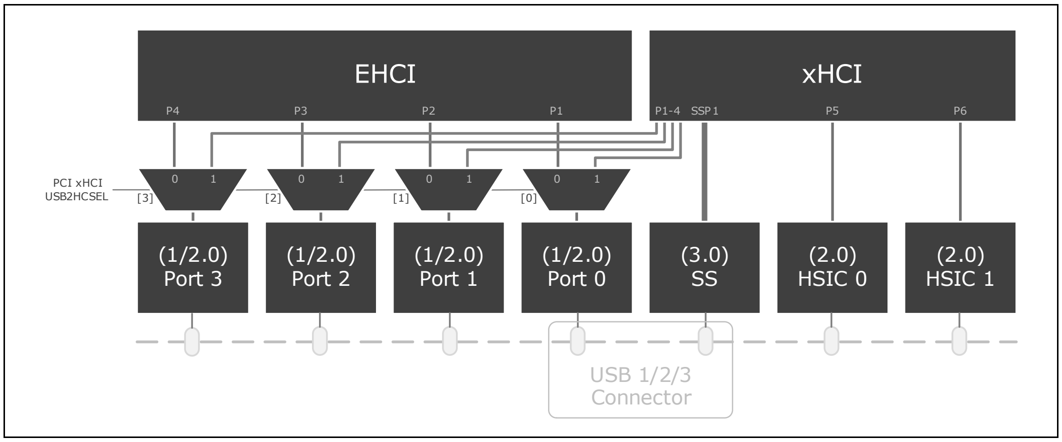
Table 210. USB 2 FS/HS Signals

Signal Name	Direction Plat. Power	Description
USB_DP/N[0:3]	I/O VUSB2	**USB Data:** High speed serialized data I/O. **Note:** USB_DP/N[1] used for debug mode in EHCI operation only. SS port must be implemented to have debug mode during xHCI operation.
USB_OC[0:1]#	I V1P8A	**Over-Current Protection:** Over-current notification for all USB ports (SS/FS/HS/LS).
USB_RCOMPI	I	**Resistor Compensation:** An external resistor must be connected. Contact your Intel representative for details.
USB_RCOMPO	O	**Resistor Compensation:** An external resistor must be connected. Contact your Intel representative for details.

Table 211. USB 2 HSIC Signals

Signal Name	Direction Plat. Power	Description
USB_HSIC[0:1]_DATA	I/O V1P24A	**HSIC Data:** High speed serialized data.
USB_HSIC[0:1]_STROBE	I/O V1P24A	**HSIC Strobe:** Strobe reference for data.
USB_HSIC_RCOMP	I	**Resistor Compensation:** An external resistor must be connected. Contact your Intel representative for details.

Figure 103.xHCI and EHCI Port Mapping



Note: xHCI (3.0) SS is the debug port for xHCI controller.
Note: EHCI (1/2.0) Port 1 is the debug port of the EHCI controller

18.2 USB 3.0 xHCI (Extensible Host Controller Interface)

The xHCI compliant host controller can control up to 7 USB host ports. It supports devices conforming to USB 1.x to 3.0 at bit rates up to 5 Gbps.

18.2.1 Features of USB 3.0 Host

The USB 3.0 Super Speed data interface is a four wire differential (TX and RX pairs) interface that supports simultaneous bi-directional data transmission. The interface supports a bit rate of 5 Gbps with a maximum theoretical data throughput over 3.2 Gbps due to 8b/10b symbol encoding scheme and protocol overhead (link flow control, packet framing and protocol overhead).

Low Frequency Periodic signaling (LFPS) is used to communicate initialization, training and power management information across a link that is in low power link state without using Super Speed signaling. This reduces power consumption.

The USB3.0 port may be paired with any USB2 port at the connector – selection of any USB2 port other than port 0 will require the appropriate mapping.Figure 103 shows the USB3 port paired with USB2 port 0.

USB3.0 Controller Features

- Supported by xHCI software host controller interface
- USB3 port disable
- Supports local dynamic clock gating and trunk clock gating
- Supports USB 3.0 LPM (U0, U1, U2, and U3) and also a SS Disabled low power state

- Support for USB3 Debug Device

Note: Recommended not to disconnect the connection when a debug session is in progress.

18.2.2 Features of USB HSIC

HSIC is a 2-signal (strobe and data) source synchronous serial interface for on board inter-chip USB communication. The interface uses 240 MHz DDR signaling to provide High-Speed 480 Mb/s USB transfers which are 100% host driver compatible with traditional USB cable connected topologies. Full Speed (FS) and Low Speed (LS) USB transfers are not directly supported by the HSIC interface.

For details of HSIC applications supported, Contact local Intel Sales office.

Major feature and performance highlights are as follows:

- Supported by xHCI software host controller interface
- High-Speed 480 Mb/s data rate only
- Source-synchronous serial interface
- Interface Power is only consumed when a transfer is in progress
- No hot plug removal/attach at HSIC pins
- Signals driven at 1.2V standard LVCMOS levels
- Designed for low power applications
- Support for two host ports compliant to High Speed Inter-Chip Supplement (HSIC) to the USB 2.0 Specification. (USB 2.0)

18.3 USB 2.0 Enhanced Host Controller Interface (EHCI)

The EHCI compliant host controller supports up to 4 USB 2.0 ports in legacy mode. USB 2.0 allows data transfers up to 480 Mbps. The controller integrates a Root Matching Hub (RMH) to support USB 1.1 devices.

Note: The EHCI is not used when the xHCI is used. The EHCI is primarily present for legacy usage, in cases when xHCI support is not available.

Note: Intel recommends using the xHCI controller for the USB2.0 ports irrespective of whether USB3.0 ports are implemented. The EHCI controller is provided for legacy OS/driver compatibility which is generally not required for tablet platforms. Using the xHCI controller will deliver significant power and performance benefits.

When following this recommendation on a platform with no USB3.0 support, the Windows logo requirement of USB debug port may not be met. Please consult with Intel regarding the impact of this.

Note: Unlike the xHCI, bandwidth of all four ports on the EHCI is shared across a single HS (480 Mbps) internal link.

18.3.1 Features of EHCI USB 2.0 Controller

The EHCI USB2.0 Controller supports the following features:

- Compliant with the specification for: USB 1.x, 2.0 (1.5 Mbps, 12 Mbps, 480 Mbps).
- 4 Ports shared with xHCI controller
- Enhanced EHCI descriptor caching
- All ports provided through USB Rate Matching Hubs (RMH) to support FS/LS devices
- Supports one Debug port at USB2 transfer rates
- Supports of USB suspend mode including PLL turn off in S0.
- Supports wakeup from suspend states S5 and remote-suspend wakeup
- All USB2 ports provide support for HS/FS/LS devices
- Per port USB disable
- Supports local dynamic clock gating and trunk clock gating
- Supports USB 2.0 LPM (L0, L1 and L2 low power states)

18.4 References

USB 3.0 Specification

USB 2.0 Specification (Includes High-Speed Inter-Chip USB Electrical Specification)

18.4.1 Host Controller Specifications

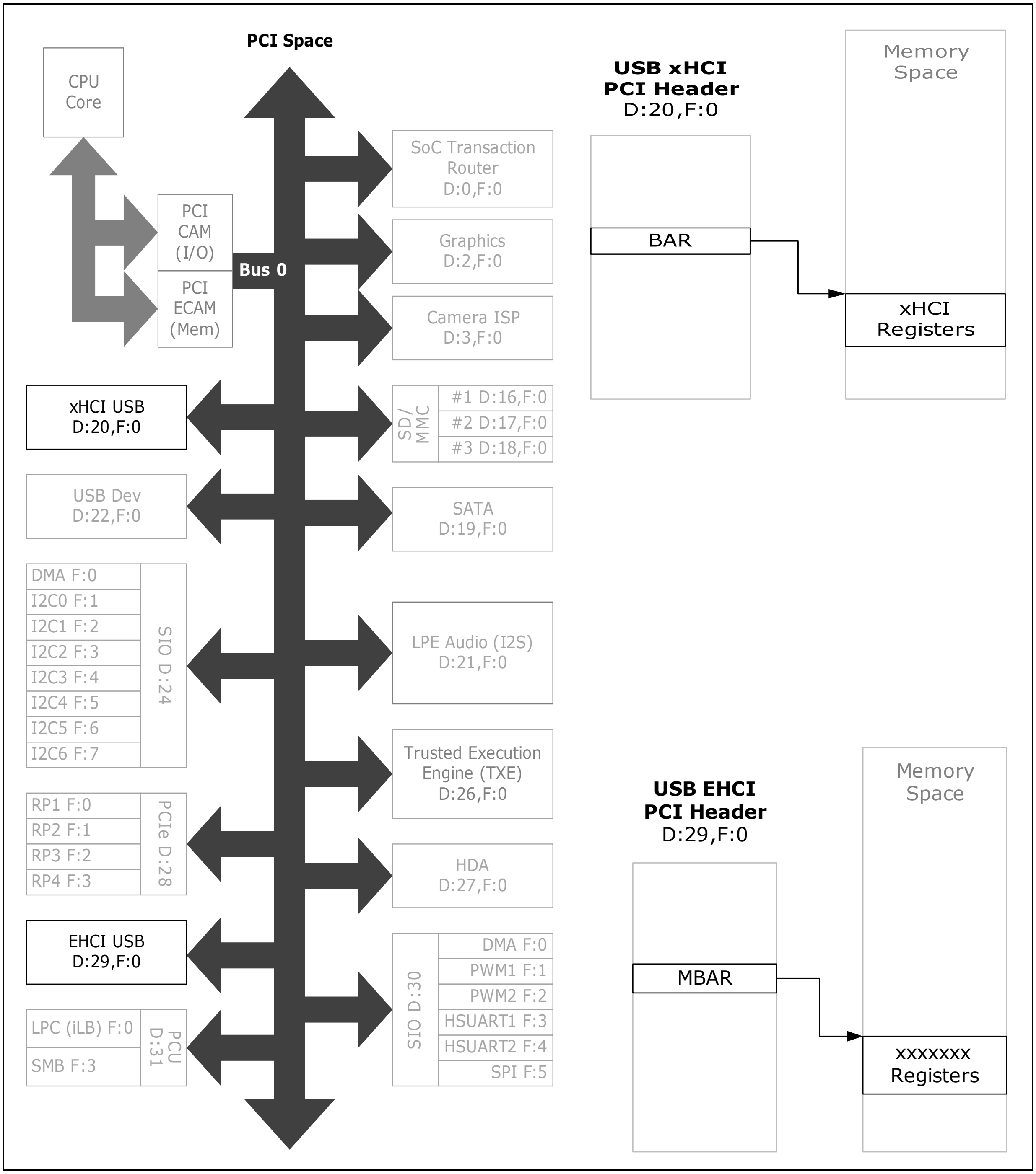
Extensible Host Controller Interface (xHCI) Specification for USB 3.0 version 1.0

Enhanced Host Controller Interface (EHCI) Specification for USB 2.0

18.5 Register Map

Refer to Chapter 3, “Register Access Methods” and Chapter 4, “Mapping Address Spaces” for additional information.

Figure 104. USB Host Controller Register Map



- Section 18.10, "USB EHCI Electrical Message Bus Registers" on page 2436

§

18.6 USB xHCI PCI Configuration Registers

Table 212. Summary of USB xHCI PCI Configuration Registers—0/20/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–1h	2	"Vendor ID (VID)—Offset 0h" on page 2127	8086h
2–3h	2	"Device ID (DID)—Offset 2h" on page 2128	8C31h
4–5h	2	"Command (CMD)—Offset 4h" on page 2128	0000h
6–7h	2	"Device Status (STS)—Offset 6h" on page 2129	0290h
8–8h	1	"Revision ID (RID)—Offset 8h" on page 2131	00h
9–9h	1	"Programming Interface (PI)—Offset 9h" on page 2131	30h
A–Ah	1	"Sub Class Code (SCC)—Offset Ah" on page 2131	03h
B–Bh	1	"Base Class Code (BCC)—Offset Bh" on page 2132	0Ch
D–Dh	1	"Master Latency Timer (MLT)—Offset Dh" on page 2132	00h
E–Eh	1	"Header Type (HT)—Offset Eh" on page 2132	00h
10–17h	8	"Memory Base Address (MBAR)—Offset 10h" on page 2133	0000000000000004h
2C–2Dh	2	"USB Subsystem Vendor ID (SSVID)—Offset 2Ch" on page 2134	0000h
2E–2Fh	2	"USB Subsystem ID (SSID)—Offset 2Eh" on page 2134	0000h
34–34h	1	"Capabilities Pointer (CAP_PTR)—Offset 34h" on page 2135	70h
3C–3Ch	1	"Interrupt Line (ILINE)—Offset 3Ch" on page 2135	00h
3D–3Dh	1	"Interrupt Pin (IPIN)—Offset 3Dh" on page 2135	00h
40–43h	4	"XHC System Bus Configuration 1 (XHCC1)—Offset 40h" on page 2136	000000FDh
44–47h	4	"XHC System Bus Configuration 2 (XHCC2)—Offset 44h" on page 2137	0003C000h
50–53h	4	"Clock Gating (XHCLKGTEN)—Offset 50h" on page 2139	00000120h
58–5Bh	4	"Audio Time Synchronization (AUDSYNC)—Offset 58h" on page 2142	00000000h
60–60h	1	"Serial Bus Release Number (SBRN)—Offset 60h" on page 2143	30h
61–61h	1	"Frame Length Adjustment (FLADJ)—Offset 61h" on page 2143	20h
62–62h	1	"Best Effort Service Latency (BESL)—Offset 62h" on page 2144	00h
70–70h	1	"PCI Power Management Capability ID (PM_CID)—Offset 70h" on page 2144	01h
71–71h	1	"Next Item Pointer #1 (PM_NEXT)—Offset 71h" on page 2145	80h
72–73h	2	"Power Management Capabilities (PM_CAP)—Offset 72h" on page 2145	C1C2h
74–75h	2	"Power Management Control/Status (PM_CS)—Offset 74h" on page 2146	0008h
80–80h	1	"Message Signaled Interrupt CID (MSI_CID)—Offset 80h" on page 2147	05h
81–81h	1	"Next item pointer (MSI_NEXT)—Offset 81h" on page 2148	00h
82–83h	2	"Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h" on page 2148	0086h
84–87h	4	"Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h" on page 2149	00000000h
88–8Bh	4	"Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h" on page 2149	00000000h

Table 212. Summary of USB xHCI PCI Configuration Registers—0/20/0 (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8C–8Dh	2	"Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch" on page 2150	0000h
A0–A3h	4	"High Speed Configuration 1 (HSCFG1)—Offset A0h" on page 2150	00000100h
A4–A7h	4	"High Speed Configuration 2 (HSCFG2)—Offset A4h" on page 2151	00002000h
B0–B3h	4	"Super Speed Configuration 1 (SSCFG1)—Offset B0h" on page 2152	0000008Fh
C0–C3h	4	"XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1)—Offset C0h" on page 2155	00000000h
C4–C7h	4	"XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2)—Offset C4h" on page 2155	00000000h
C8–CBh	4	"XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1)—Offset C8h" on page 2156	00000000h
CC–CFh	4	"XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2)—Offset CCh" on page 2157	00000000h
D0–D3h	4	"USB2 Port Routing (USB2PR)—Offset D0h" on page 2158	00000000h
D4–D7h	4	"USB2 Port Routing Mask (USB2PRM)—Offset D4h" on page 2159	00000000h
D8–DBh	4	"USB3 Port Routing (USB3PR)—Offset D8h" on page 2159	00000000h
DC–DFh	4	"USB3 Port Routing Mask (USB3PRM)—Offset DCh" on page 2160	00000000h
E0–E3h	4	"Fuse and Strap (FUS)—Offset E0h" on page 2160	00000000h
E4–E7h	4	"USB2 Port Disable Override (USB2PDO)—Offset E4h" on page 2162	00000000h
E8–EBh	4	"USB3 Port Disable Override (USB3PDO)—Offset E8h" on page 2162	00000000h
EC–EFh	4	"USB2 FS/LS Port Staggering Control (FSLSPS)—Offset ECh" on page 2163	0000D8D8h
F0–F3h	4	"DFT 1 (DFT1)—Offset F0h" on page 2164	00000000h
F4–F7h	4	"DFT 2 (DFT2)—Offset F4h" on page 2165	00000000h
F8–FBh	4	"Manufacturing Process ID (MANID)—Offset F8h" on page 2166	00000F00h
FC–FFh	4	"DFT 3 (DFT3)—Offset FCh" on page 2167	00000000h

18.6.1 Vendor ID (VID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 16 bits)   **Offset:** [B:0, D:20, F:0] + 0h

Default: 8086h

15			12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
VID															

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Reserved. **Power Well:** Core

18.6.2 Device ID (DID)—Offset 2h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 2h

Default: 8C31h

15			12				8				4				0
1	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1
DID															

Bit Range	Default & Access	Field Name (ID): Description
15:0	8C31h RO/V	**Device ID (DID):** See Global Device ID table in Chap. 6 for value **Power Well:** Core

18.6.3 Command (CMD)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 4h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD					ID	FBE	SERR	WCC	PER	VPS	MWI	SCE	BME	MSE	IOSE

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
10	0b RW	**Interrupt Disable (ID):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable. **Power Well:** Core
9	0b RO	**Fast Back to Back Enable (FBE):** Reserved. **Power Well:** Core
8	0b RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#. See section on error handling. **Power Well:** Core
7	0b RO	**Wait Cycle Control (WCC):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#. **Power Well:** Core
5	0b RO	**VGA Palette Snoop (VPS):** Reserved. **Power Well:** Core
4	0b RO	**Memory Write Invalidate (MWI):** Reserved. **Power Well:** Core
3	0b RO	**Special Cycle Enable (SCE):** Reserved. **Power Well:** Core
2	0b RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus. **Power Well:** Core
1	0b RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set. **Power Well:** Core
0	0b RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only. **Power Well:** Core

18.6.4 Device Status (STS)—Offset 6h

Access Method

Type: PCI Configuration Register (Size: 16 bits) **Offset:** [B:0, D:20, F:0] + 6h

Default: 0290h

15			12				8				4				0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		MDPED	FBBC	UDF	MC	CL	IS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW/1C	**Detected Parity Error (DPE):** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0b RW/1C	**Signaled System Error (SSE):** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. See error handling section for complete list of conditions handled. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
13	0b RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
12	0b RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
11	0b RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort. **Power Well:** Core
10:9	01b RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only. **Power Well:** Core
8	0b RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the Intel PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
7	1b RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only. **Power Well:** Core
6	0b RO	**User Definable Features (UDF):** Reserved as 0. Read-Only. **Power Well:** Core
5	0b RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only. **Power Well:** Core
4	1b RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer. **Power Well:** Core
3	0b RO/V	**Interrupt Status (IS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit. **Power Well:** Core
2:0	000b RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

18.6.5 Revision ID (RID)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 8h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Revision ID (RID):** See Chap 6 for value. **Power Well:** Core

18.6.6 Programming Interface (PI)—Offset 9h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 9h

Default: 30h

7			4				0
0	0	1	1	0	0	0	0
PI							

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification. **Power Well:** Core

18.6.7 Sub Class Code (SCC)—Offset Ah

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + Ah

Default: 03h

7			4				0
0	0	0	0	0	0	1	1
SCC							

Bit Range	Default & Access	Field Name (ID): Description
7:0	03h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller. **Power Well:** Core

18.6.8 Base Class Code (BCC)—Offset Bh

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + Bh

Default: 0Ch

7			4				0
0	0	0	0	1	1	0	0
BCC							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller. **Power Well:** Core

18.6.9 Master Latency Timer (MLT)—Offset Dh

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + Dh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MLT							

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0. **Power Well:** Core

18.6.10 Header Type (HT)—Offset Eh

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + Eh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MFB	CL						

Bit Range	Default & Access	Field Name (ID): Description
7	0b RO	**Multi-Function Bit (MFB):** Read only indicating single function device. **Power Well:** Core
6:0	00h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout. **Power Well:** Core

18.6.11 Memory Base Address (MBAR)—Offset 10h

Value in this register will be different after the enumeration process.

Access Method

Type: PCI Configuration Register (Size: 64 bits)

Offset: [B:0, D:20, F:0] + 10h

Default: 0000000000000004h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	

Fields: BA (63:16), RSVD (15:4), Prefetchable (3), Type (2:1), RTE (0)

Bit Range	Default & Access	Field Name (ID): Description
63:16	000000000000h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries. **Power Well:** Core
15:4	000h RO	**Reserved (RSVD):** Reserved. Read-Only 0, this indicates that this function is requesting an 64KB block of memory. **Power Well:** Core
3	0b RO	**Prefetchable:** This bit is hardwired to 0 indicating that this range should not be prefetched. **Power Well:** Core
2:1	10b RO	**Type:** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0b RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space **Power Well:** Core

18.6.12 USB Subsystem Vendor ID (SSVID)—Offset 2Ch

This register is modified and maintained by BIOS

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 2Ch

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSVID															

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others. NOT for EDS:Writes to this register are controlled by the Access Control bit (ACCTRL). **Power Well:** Core

18.6.13 USB Subsystem ID (SSID)—Offset 2Eh

This register is modified and maintained by BIOS

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 2Eh

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSID															

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). NOT for EDS: Writes to this register are controlled by the Access Control bit (ACCTRL). **Power Well:** Core

18.6.14 Capabilities Pointer (CAP_PTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 8 bits) **Offset:** [B:0, D:20, F:0] + 34h

Default: 70h

7			4				0
0	1	1	1	0	0	0	0
CAP_PTR							

Bit Range	Default & Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges. **Power Well:** Core

18.6.15 Interrupt Line (ILINE)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 8 bits) **Offset:** [B:0, D:20, F:0] + 3Ch

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
ILINE							

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Line (ILINE):** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to. **Power Well:** Core

18.6.16 Interrupt Pin (IPIN)—Offset 3Dh

Access Method

Type: PCI Configuration Register (Size: 8 bits) **Offset:** [B:0, D:20, F:0] + 3Dh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IPIN							

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO/V	**Interrupt pin (IPIN):** Bits 3:0 reflect the value programmed in the interrupt pin registers in chipset configuration space. Bits 7:4 are hardwired to 0000b. See Chap 6 for value. **Power Well:** Core

18.6.17 XHC System Bus Configuration 1 (XHCC1)—Offset 40h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:20, F:0] + 40h

Default: 000000FDh

Bits	Default	Field
31	0	ACCTRL
30:25	000000	ECO1
24	0	RMTASERR
23	0	URD
22	0	URRE
21:19	000	IIL1E
18	0	XHCIL1E
17	0	D3IL1E
16:12	00000	PCPWT
11	0	SWAXHCI
10:8	000	L23HRAWC
7:6	11	UTAGCP
5:4	11	UDAGCNP
3:2	11	UDAGCCP
1:0	01	UDAGC

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/O	**Access Control (ACCTRL):** This bit is used by BIOS to lock/unlock lockable bits. When set to '1' the write access to bits locked by this bit is disabled (locked state). When set to '0', the write access to bit locked by this bit is enabled (unlocked state). Writable once after platform reset. **Power Well:** Core
30:25	00h RW	**ECO1:** ECO bits are used during silicon bringup for FIBing. NOT for EDS **Power Well:** Core
24	0b RW	**Master/Target Abort SERR (RMTASERR):** When set, it allows the out-of-band error reporting from the xHCI Controller to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit. **Power Well:** Core
23	0b RW/C	**Unsupported Request Detected (URD):** Set the HW when xHCI Controller received an unsupported request posted cycle. Cleared by SW when the bit is written with value of '1'. **Power Well:** Core
22	0b RW	**Unsupported Request Report Enable (URRE):** When set this bit allows the URD bit to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit. **Power Well:** Core
21:19	000b RW	**Inactivity Initiated L1 Enable (IIL1E):** If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified. 000: Disabled 001: 32 bb_cclk 010: 64 bb_cclk 011: 128 bb_cclk 100: 256 bb_cclk 101: 512 bb_cclk 110: 1024 bb_cclk 111: 131072 bb_cclk **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**XHC Initiated L1 Enable (XHCIL1E):** If set, allow the XHC initiated L1 power mangement to be enabled. **Power Well:** Core
17	0b RW	**D3 Initiated L1 Enable (D3IL1E):** If set, allow PCI device state D3 initiated L1 power managment to be enables. This bit can only be set if the XHCI L1 Override P2 chicken bit is set. **Power Well:** Core
16:12	00h RW	**Periodic Complete Pre Wake Time (PCPWT):** signal . This allows for platform wake time before the next scheduled periodic transaction. The value programmed in this field represents the # of bytes consumed in the current micro-frame which is required to allow for the periodic complete to de-assert. This allows for a programmable time to cause the periodic complete to de-assert prior to the start of the next micro-frame. Register Format: Bits (16:12) represnets the # of bytes remaining with a 256B granularity. Periodic Complete will de-assert if the bytes consumed in the current micro-frame is less **Power Well:** Core
11	0h RW	**SW Assisted xHC Idle (SWAXHCI):** This bit being set will indicate xHC idleness (through SW means), which must be a '1' to allow L1 entry, and subsequently allow backbone clock to be gated. This bit is to be set by Intel xHCI driver after checking that the xHCI Controller will stay in idle state for a significant period of time, e.g. all ports disconnected. This bit can be cleared under the following conditions (see SWAXHCI Policy bits in xHC System Bus Configuration 2 register): n SW: SW could write 0 to clear this bit. n HW: HW, under policy control, will clear this bit on an MMIO access to the Host Controller. n HW: HW, under policy control, will clear this bit when HW exits Idle state. **Power Well:** Core
10:8	000b RW	**L23 to Host Reset Acknowledge Wait Count (L23HRAWC):** If programmed to non zero, it allows a wait period after the L23 PHY has shutdown before returning host reset acknowledge to PMC. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk **Power Well:** Core
7:6	11b RW	**Upstream Type Arbiter Grant Count Posted (UTAGCP):** Grant count for IOSF upstream L2 request type arbiter for posted type **Power Well:** Core
5:4	11b RW	**Upstream Type Arbiter Grant Count Non Posted (UDAGCNP):** Grant count for IOSF upstream L2 type arbiter for non-posted type **Power Well:** Core
3:2	11b RW	**Upstream Type Arbiter Grant Count Completion (UDAGCCP) (UDAGCCP):** Grant count for IOSF upstream L2 type arbiter for completion type **Power Well:** Core
1:0	01b RW	**Upstream Device Arbiter Grant Count (UDAGC) (UDAGC):** Grant count for IOSF upstream L1 device arbiter **Power Well:** Core

18.6.18 XHC System Bus Configuration 2 (XHCC2)—Offset 44h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + 44h

Default: 0003C000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OCCFGDONE	ECO1					DREQBCC	IDMA_RDREQSZCTRL			XHCUPRDROE	IOSFSRAD	UNPPA						SWAXHCIP		RAWDD	WAWDE	SWACXIHB		SWADMIL1IHB		L1FP2CGWC			RDREQSZCTRL		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/O	**OC Configuration Done (OCCFGDONE):** This bit is used by BIOS to prevent spurious switching during OC configuration. Any write this register bit will cause it to set. It must be set by BIOS after configuration of the OC mapping bits is complete. Once this bit is set, OC mapping shall not be changed by SW. **Power Well:** SUS
30:26	00h RW	**ECO1:** NOT for EDS ECO bits are used during silicon bringup for FIBing. **Power Well:** Core
25	0b RW	**DMA Request Boundary Crossing Control (DREQBCC):** This bit controls the boundary crossing limit of each Read/Write Request. 0: 4KB 1: 64B **Power Well:** Core
24:22	0h RW	**IDMA Read Request Size Control (IDMA_RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 011 - 110: Reserved 111: 64B **Power Well:** Core
21	0b RW	**XHC Upstream Read Relaxed Ordering Enable (XHCUPRDROE):** This policy controls the Relaxed Ordering attribute for upstream reads. 0 - xHC will clear RO for all upstream read requests. 1 - xHC will set RO for all upstream read requests. **Power Well:** Core
20	0b RW	**IOSF Sideband Register Access Disable (IOSFSRAD):** When set, it disables the IOSF sideband interface from accepting any host space register access. **Power Well:** Core
19:14	0Fh RW	**Upstream Non-Posted Pre-Allocation (UNPPA):** This field reserves data sizes, in 64 byte chunks, of the downstream completion resource. This value is zero based. 000000 - 111111: Pre-allocate 64 bytes - 4096 bytes If set greater than the default allows over-allocation If set less than default allows under-allocation Only allowed to be programmed when BME = 0 and no outstanding downstream completion **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
13:12	00b RW	**SW Assisted xHC Idle Policy (SWAXHCIP):** Note: Irrespective of the setting of this field, SW write of 0 to SWAXHCI will clear the bit. 00b (default): xHC HW clears SWAXHCI bit upon: n MMIO access to Host Controller OR n xHC HW exits Idle state 01b: xHC HW does not autonomously clear SWAXHCI bit. The bit could be cleared only by SW. 10b: xHC HW clears SWAXHCI upon MMIO acces to Host Controller. xHC HW exit from Idle state will not clear SWAXHCI. 11b: Reserved **Power Well:** Core
11	0h RW	**MMIO Read After MMIO Write Delay Disable (RAWDD):** This field controls delay on MMIO Read after MMIO Write. 0b (Default): Delay MMIO Read after MMIO Write 1b: Do not delay MMIO Read after MMIO Write Note that this delay applies after the second of the two DW writes in the case where the IOSF Gasket splits a QW write into two single DW writes to the IP. **Power Well:** Core
10	0h RW	**MMIO Write After MMIO Write Delay Enable (WAWDE):** This field controls delay on MMIO Write after previous MMIO Write. 0b (Default): Do not delay MMIO Write after previous MMIO Write 1b: Delay MMIO Write after previous MMIO Write Note that the delay count does not apply on the second of the two DW writes that are generated by IOSF Gasket when it splits a QW write into two. In other words, the second of the two DW writes could happen without any delay with respect to the first DW write. This choice is being made for ease of ECO. The delay count, in this case, will apply after the second of the two DW writes. **Power Well:** Core
9:8	0h RW	**SW Assisted Cx Inhibit (SWACXIHB):** This field controls how the DMI L1 inhibit signal from USB3 to PMC will behave. 00: Never inhibit Cx 01: Inhibit Cx when Isochronous Endpoint is active (PPT Behavior) 10: Inhibit Cx when Periodic Active as defined in 40.4.3.2.1 11: Always inhibit Cx **Power Well:** Core
7:6	0h RW	**SW Assisted DMI L1 Inhibit (SWADMIL1IHB):** This field controls how the DMI L1 inhibit signal from USB3 to DMI will behave. 00: Never inhibit DMI L1. 01: Inhibit DMI L1 when Isochronous Endpoint is active (PPT Behavior). 10: Inhibit DMI L1 when Priodic Active as defined in 40.4.3.2.1. 11: Inhibit DMI L1 if XHCC1.SWAXHCI = 0. **Power Well:** Core
5:3	0h RW	**L1 Force P2 Clock Gating Wait Count (L1FP2CGWC):** If programmed to non zero, it allows L1 force P2 gating off the clock to be delayed after the time-out period specified. If wake up event is detected before the time-out, pclk remains alive and trigger L1 exit as though CPU host is causing the wake, 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk **Power Well:** Core
2:0	000b RW	**Read Request Size Control (RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 010: 512B 011 - 110: Reserved 111: 64B **Power Well:** Core

18.6.19 Clock Gating (XHCLKGTEN)—Offset 50h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + 50h

Default: 00000120h

Bits	31:29	28	27	26	25	24	23:20	19:16	15	14	13	12	11:10	9:8	7:5	4	3	2	1	0
Default	0 0 0	0	0	0	0	0	0 0 0 0	0 0 0 0	0	0	0	0	0 0	0 1	0 0 1	0	0	0	0	0
Field	Rsvd2	NUEFBCGPS	SRAMPGTEN	SSLSE	USB2PLLSE	IOSFSTCGE	HSTCGE	SSTCGE	XHCIGEU3S	XHCFTCLKSE	XHCBBTCGIPISO	XHCHSTCGU2NRWE	XHCUSB2PLLSDLE	HSUXDMIPLLSE	SSPLLSUE	XHCBLCGE	HSLTCGE	SSLTCGE	IOSFBTCGE	IOSFBLCGE

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Rsvd2:** Reserved **Power Well:** Core
28	0b RW	**Nak’ing USB2.0 EPs for Backbone Clock Gating and PLL Shutdown (NUEFBCGPS):** This field controls whether Naking USB2.0 EPs, once in Naking low priority schedule, should be considered as active for the considerations for backbone clock gating and PLL shutdown or not. 0: Naking USB2.0 EPs are not considered to be active for Backbone Clock Gating and PLL Shutdown evaluation. 1: Naking USB2.0 EPs are considered to be active for Backbone clock gating and PLL shutdown evaluation. **Power Well:** Core
27	0b RW	**SRAM Power Gate Enable (SRAMPGTEN):** This register enables the SRAM Power Gating when PLL shutdown conditions for all clock domains have been met 0 - Disallow SRAM Power Gating. 1 - Allow SRAM Power Gating **Power Well:** Core
26	0h RW	**SS Link PLL Shutdown Enable (SSLSE):** This register enables the SS P3 state to be exposed to PXP PLL Shutdown conditions on behalf of all USB SS Ports ontop of trunk clock gating. 0 - P3 state NOT allowed to result in PXP PLL shutdown. 1- P3 state allowed to result in PXP PLL shutdown **Power Well:** Core
25	0h RW	**USB2 PLL Shutdown Enable (USB2PLLSE):** When set, this bit allows USB2 PLL to be shutdown when HS Link trunk clock is gated, and xHC can tolerate PLL spin up time for subsequent clock request. Note: if USB2 PLL Shutdown Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core
24	0h RW	**IOSF Sideband Trunk Clock Gating Enable (IOSFSTCGE):** When set, this bit allows the IOSF sideband clock trunk to be gated when idle conditions are met. **Power Well:** Core
23:20	0h RW	**HS Backbone PXP Trunk Clock Gate Enable (HSTCGE):** This register determines the HS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) NA (no support for U1) (2) ==) U2 (L1) or deeper (3) ==) U3 (L2) or deeper **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**SS Backbone PXP Trunk Clock Gate Enable (SSTCGE):** This register determines the SS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) U1 or deeper (2) ==) U2 or deeper (3) ==) U3 or deeper **Power Well:** Core
15	0h RW	**XHC Ignore_EU3S (XHCIGEU3S):** This register determines if the xHC will use the EU3S as a condition to allow for Frame timer gating. 0 - xHC may allow frame timer to be gated when EU3S is set and all ports are in the required state. 1 - xHC may allow frame timer to be gated regardless of EU3S. **Power Well:** Core
14	0h RW	**XHC Frame Timer Clock Shutdown Enable (XHCFTCLKSE):** This register determines if the xHC will allow the frame timer clock to be gated. 0 - xHC will not allow ICC PLL 96MHz output to be shutdown thus keeping the frame timer running. 1 - xHC will allow ICC PLL 96MHz output to be shutdown under specific conditions. **Power Well:** Core
13	0h RW	**XHC Backbone PXP Trunk Clock Gate In Presence of ISOCH EP (XHCBBTCGIPISO):** This register controls the policy on allowing Backbone PXP trunk clock gate in the presence of IDLE ISOCH EP s with active DB. Allows the periodic active to be used in enabling Backbone PXP trunk clock gating of core clock. 0 Trunk gate of core clock is not allowed when ISOCH EP DB is set and ISOCH EP s are idle. 1 Allow trunk gate of core clock when ISOCH EP DB is set and ISOCH EP s are idle. **Power Well:** Core
12	0h RW	**XHC HS Backbone PXP Trunk Clock Gate U2 non RWE (XHCHSTCGU2NRWE):** This register controls the policy on allowing Backbone PXP trunk gating of core clock when there is atleast 1 non Remote Wake Enabled HS Port in U2. 0 Prevent trunk gate of core clock when a non RWE HS Port is in U2. 1 Allow trunk gate of core clock when a non RWE HS Port is in U2. **Power Well:** Core
11:10	0h RW	**XHC USB2 PLL Shutdown Lx Enable (XHCUSB2PLLSDLE):** This register determines the HS Link state(s) which will be exposed to USB2 PLL Shutdown conditions on behalf of all USB2 HS Ports. Ly is a state allowed to result in USB2 PLL Shutdown when en(x) is asserted. (0) ==) L1 or deeper (1) ==) L2 or deeper **Power Well:** Core
9:8	01b RW	**HS Backbone PXP PLL Shutdown Ux Enable (HSUXDMIPLLSE):** This register determines the Ux state(s) which will be exposed to PXP PLL Shutdown conditions. PLL Shutdown is allowed in: 00b Disabled (Link states shall be disabled for DMI PLL shutdown) 01b U0 or conditions for 10b setting. 10b U2 or conditions for 11b setting. 10b U3, Disconnected, Disabled or Powered-Off. **Power Well:** Core
7:5	001b RW	**SS Backbone PXP PLL Shutdown Ux Enable (SSPLLSUE):** This register determines the Ux state(s) which will be exposed to DMI PLL Shutdown conditions. PLL Shutdown is allowed in: 000b Disabled (Link states shall be ignored for DMI PLL shutdown). 001b U0 or conditions for 010b setting 010b U1 or conditions for 011b setting 011b U2 or conditions for 100b setting 100b U3, Disconnected, Disabled or Powered-Off **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**XHC Backbone Local Clock Gating Enable (XHCBLCGE):** When set, this bit allows XHCI Controller IP backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core
3	0b RW	**HS Link Trunk Clock Gating Enable (HSLTCGE):** When set, this bit allows High Speed Link control's 480 MHz and its 48/60 MHz link clock trunk to be gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled. **Power Well:** Core
2	0b RW	**SS Link Trunk Clock Gating Enable (SSLTCGE):** When set, this bit allows the SuperSpeed Link control's 250 MHz and its divided 125 MHz link clock trunk to ge gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled. **Power Well:** Core
1	0b RW	**IOSF Backbone Trunk Clock Gating Enable (IOSFBTCGE):** When set, this bit allows the IOSF backbone clock trunk to be gated when idle conditions are met. **Power Well:** Core
0	0b RW	**IOSF Gasket Backbone Local Clock Gating Enable (IOSFBLCGE):** When set, this bit allows the IOSF Gasket backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled. **Power Well:** Core

18.6.20 Audio Time Synchronization (AUDSYNC)—Offset 58h

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + 58h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd2		CMFI														Rsvd1			CMFB												

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Rsvd2:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:16	0000h RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX **Power Well:** Core
15:13	0h RO	**Rsvd1:** Reserved. **Power Well:** Core
12:0	0000h RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA. **Power Well:** Core

18.6.21 Serial Bus Release Number (SBRN)—Offset 60h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 60h

Default: 30h

7			4				0
0	0	1	1	0	0	0	0
SBRN							

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0. **Power Well:** SUS

18.6.22 Frame Length Adjustment (FLADJ)—Offset 61h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 61h

Default: 20h

7			4				0
0	0	1	0	0	0	0	0
RSVD		FLTV					

Bit Range	Default & Access	Field Name (ID): Description
7:6	00b RO	**Reserved (RSVD):** . **Power Well:** SUS
5:0	20h RW	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value **Power Well:** SUS

18.6.23 Best Effort Service Latency (BESL)—Offset 62h

Bset Effort Service Latency.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 62h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
DBESLD				DBESL			

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters. **Power Well:** Core
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters. **Power Well:** Core

18.6.24 PCI Power Management Capability ID (PM_CID)—Offset 70h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 70h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1

PM_CID

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field. **Power Well:** Core

18.6.25 Next Item Pointer #1 (PM_NEXT)—Offset 71h

This register is modified and maintained by BIOS

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 71h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0

PM_NEXT

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer #1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed. **Power Well:** Core

18.6.26 Power Management Capabilities (PM_CAP)—Offset 72h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 72h

Default: C1C2h

15			12				8				4				0
1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0
PME_Support					D2_Support	D1_Support	Aux_Current			DSI	RSVD	PMEClock	Version		

Bit Range	Default & Access	Field Name (ID): Description
15:11	11000b RW/L	**PME_Support:** This 5-bit field indicates the power states in which the function may assert PME#. The Intel PCH XHC does not support the D1 or D2 states. For all other states, the Intel PCH XHC is capable of generating PME#. Software should never need to modify this field. NOT for EDS: However, the ability to change this field may prove useful for some systems. **Power Well:** Core
10	0b RW/L	**D2_Support:** The D2 state is not supported. **Power Well:** Core
9	0b RW/L	**D1_Support:** The D1 state is not supported. **Power Well:** Core
8:6	111b RW/L	**Aux_Current:** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known. **Power Well:** Core
5	0b RW/L	**DSI:** The Intel PCH reports 0, indicating that no device-specific initialization is required. **Power Well:** Core
4	0b RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
3	0b RW/L	**PME Clock (PMEClock):** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#. **Power Well:** Core
2:0	010b RW/L	**Version:** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification. **Power Well:** Core

18.6.27 Power Management Control/Status (PM_CS)—Offset 74h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 74h

Default: 0008h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
PME_Status	Data_Scale		Data_Select				PME_En	RSVD				NSR	RSVD2	PowerState	

Bit Range	Default & Access	Field Name (ID): Description
15	0b RW/1C	**PME_Status:** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded. **Power Well:** SUS
14:13	00b RO	**Data_Scale:** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register. **Power Well:** Core
12:9	0h RO	**Data_Select:** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register. **Power Well:** Core
8	0b RW	**PME_En:** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded. **Power Well:** SUS
7:4	0h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
3	1b RO	**No Soft Reset (NSR):**), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Power Well:** Core
2	0b RO	**Reserved (RSVD2):** Reserved. **Power Well:** Core
1:0	00b RW	**PowerState:** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible. **Power Well:** Core

18.6.28 Message Signaled Interrupt CID (MSI_CID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 80h

Default: 05h

7			4				0
0	0	0	0	0	1	0	1
CID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	05h RO	**Capability ID (CID):** Indicates that this is an MSI capability **Power Well:** Core

18.6.29 Next item pointer (MSI_NEXT)—Offset 81h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 81h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
NEXT							

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Next Pointer (NEXT):** Indicates that this is the last item on the capability list **Power Well:** Core

18.6.30 Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 82h

Default: 0086h

15			12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
RSVD							PVM	C64	MME			MMC			MSIE

Bit Range	Default & Access	Field Name (ID): Description
15:9	00h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8	0b RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported **Power Well:** Core
7	1b RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable. **Power Well:** Core
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI. **Power Well:** Core
3:1	011b RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved **Power Well:** Core
0	0b RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used. **Power Well:** Core

18.6.31 Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + 84h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Addr																														RSVD	

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Addr:** Lower DW of system specified message address, always DWORD aligned **Power Well:** Core
1:0	00b RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

18.6.32 Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + 88h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

UpperAddr

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Upper Addr (UpperAddr):** Upper DW of system specified message address. **Power Well:** Core

18.6.33 Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 8Ch

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Data

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Data:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data. **Power Well:** Core

18.6.34 High Speed Configuration 1 (HSCFG1)—Offset A0h

Not for EDS

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + A0h

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	31:16	15:10	9	8	7:2	1	0
Field	ECO1	Rsvd1	HSAAPE	PAPE	ECO2	EN_HSIC_BUS_STATE_TO_BUS_RESET	EN_HSIC_CNCT_DISCNCT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**ECO bits Core (ECO1):** ECO bits are used during silicon bringup for FIBing. **Power Well:** Core
15:10	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
9	0h RW	**xHC HS Async Active Propogation Enable (HSAAPE):** This register controls the hs async active exposusre to PMC via the xHC active indication 0 HS Async Active is not propogated to PMC 1 HS Async Active is propogated to PMC **Power Well:** Core
8	1h RW	**xHC Periodic Active Propogation Enable (PAPE):** This register controls the periodic active exposusre to PMC via the xHC active indication 0 Periodic Active is not propogated to PMC 1 Periodic Active is propogated to PMC **Power Well:** Core
7:2	00h RW	**ECO bits SUS (ECO2):** ECO bits are used during silicon bringup for FIBing. **Power Well:** SUS
1	0h RW	**EN_HSIC_BUS_STATE_TO_BUS_RESET:** Disable VLV2 C0 Fix: Port Power OFF triggering the HSIC BUS State to BUS RESET 0 = VLV2 C0 Fix [DEFAULT] 1 = Revert back to VLV2 B2 functionality **Power Well:** SUS
0	0h RW	**EN_HSIC_CNCT_DISCNCT:** Disable VLV2 C0 Fix: Port Power OFF triggering the HSIC Internal Connect Flag to clear. This will enable Disconnect-Connect capability for HSIC I/F. 0 = VLV2 C0 Fix [DEFAULT] 1 = Revert back to VLV2 B2 functionality **Power Well:** SUS

18.6.35 High Speed Configuration 2 (HSCFG2)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + A4h

Default: 00002000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	

Rsvd1	HSAAIM	HSOAAPEPM	HSIAAPEPM	HSIIPAPC	HSIIPANEPT	HSIIPASIT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ ignore IN EP s. **Power Well:** Core
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling. **Power Well:** Core
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling. **Power Well:** Core
12:11	0h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indicaiton **Power Well:** Core
10:4	00h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation. **Power Well:** Core
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation. **Power Well:** Core

18.6.36 Super Speed Configuration 1 (SSCFG1)—Offset B0h

Refer to the switching flows section of this document. Not for EDS

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**Offset:** [B:0, D:20, F:0] + B0h

Default: 0000008Fh

Bits	31:22	21:18	17	16	15	14	13	12	11:8	7	6	5	4:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	0	0	0	0 0 0 0	1	0	0	0 1	1	1	1
Field	ECO1	LFPSPMU3	LFPSPME	SSPPEN	Rsvd1	MPHYPGEU2	MPHYPGENONU2	SSAAPE	Rsvd2	SSPPENAB	ECO2	RXDETSTGDIS	G2RXPTTV	G2RXPTE	G2RXERXEE	G2RXETXHSDE

Bit Range	Default & Access	Field Name (ID): Description
31:22	000h RW	**ECO1:** ECO bits are used during silicon bringup for FIBing. **Power Well:** Core
21:18	0h RW	**LFPS Power Management in U3 Enable (LFPSPMU3):** This field allows xHC to turn off LFPS Receiver when the port is in U3. This allows the Host Controller to save some extra power (about 50W per port) in idle states if device connected on a port is not Resume capable or Resume enabled. This choice has to be done by BIOS and based on platform knowledge. For example, if an in-box device is not Resume Capable, BIOS could allow xHC to turn-off Rx LFPS when the port is in U3. Each bit represents a port. Bit (16) is for USB3.0 Port 0, Bit (17) is for USB3.0 Port 1 and so on. 0 in a bit position: LFPS Receiver shall be kept enabled when the port is in U3. 1 in a bit position: LFPS Receiver shall be disabled when the port is in U3. **Power Well:** SUS
17	0b RW	**LFPS Power Management Enable (LFPSPME):** This field provides programmability of LFPS Receiver power management capability when USB3.0 ports are Disabled or in Disconnected state. 0: Do not power manage LFPS receiver. LFPS receivers are enabled in all states. 1: Power manage LFPS receiver. LFPS receivers will be turned off if USB3.0 port is Disabled or Disconnected. Note: Default value is being kept at 0 in case EXI architecture/design takes the path of not doing dynamic Rx LFPS enabling for EXI signature detect and disable LFPS Power Management to keep Rx LFPS buffer on for debug. **Power Well:** SUS
16	0b RW	**USB3 SS Port Polling Enable (SSPPEN):** 0: Prevent USB3 Super-speed port to start Polling.LFPS. 1: Allow USB3 Super-speed port to start Polling.LFPS. NOTE: This bit will take effect in allowing/preventing USB3 SS port from starting Polling.LFPS only if SSPPENAB is cleared. **Power Well:** Core
15	0b RO	**Rsvd1:** Reserved. **Power Well:** Core
14	0b RW	**MODPHY Power Gate Enable for U2 (MPHYPGEU2):** This bit controls whether LPT-LPT xHC will allow modPHY power gating or not when a port is in U2 state. Note that this single bit controls all ports of xHC. 0b xHC shall not initiate Power Gate Request If xHC had initiated Power Gate Request before this bit is programmed to 0, xHC shall initiate the handshake to wake modPHY from power gated state. 1b xHC is enabled to initiate Power Gate Request if power gating conditions are met. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
13	0b RW	**MODPHY Power Gate Enable for non-U2 states (MPHYPGENONU2):** This bit controls whether LPT-LPT xHC will allow modPHY power gating or not when a port is in states other than U2. Note that this single bit controls all ports of xHC. 0b xHC shall not initiate Power Gate Request If xHC had initiated Power Gate Request before this bit is programmed to 0, xHC shall initiate the handshake to wake modPHY from power gated state. 1b xHC is enabled to initiate Power Gate Request if power gating conditions are met. **Power Well:** Core
12	0h RW	**xHC SS Async Active Propogation Enable (SSAAPE):** This register controls the ss async active exposusre to PMC via the xHC active indication 0 SS Async Active is not propogated to PMC 1 SS Async Active is propogated to PMC **Power Well:** Core
11:8	0h RO	**Rsvd2:** Reserved **Power Well:** Core
7	1b RW	**USB3 SS Port Polling Enable Active (SSPPENAB):** 0: Allow blocking of USB3 Super-speed port from starting Polling.LFPS. 1: Disallow blocking of USB3 Super-speed port from starting Polling.LFPS (A stepping behavior). NOTE: When this bit is cleared, Polling.LFPS blocking is controlled by SSPPEN bit. **Power Well:** SUS
6	0h RW	**ECO2:** ECO bits are used during silicon bringup for FIBing. **Power Well:** SUS
5	0h RW	**Receiver Detect Staggering Disable (RXDETSTGDIS):** When set, this regiter bit disables receiver detect staggering between all 6 USB3 lanes Note that the bit is ONLY meant for SW to disable the staggering if desired. Once it is set to disabled, SW is not allowed to re-enable the staggering by clearing the bit. **Power Well:** SUS
4:3	1h RW	**Gotorxelecidle Polling Timer Timeout Value (G2RXPTTV):** Timeout value for Gotorxelecidle Polling Timer: 00: 1 to 2 us (Simulation speed up mode only). 01: 19 to 20 us (Default). 10: 23 to 24 us. 11: 199 to 200 us. This register needs to be programmed when G2RXPOLLTMREN = 0. **Power Well:** SUS
2	1b RW	**Gotorxelecidle Polling Timer Enable (G2RXPTE):** If enabled (1), Gasket starts a timer after transmitting high speed data AND not receiving LFPS, and will only de-assert GoToRxElecIdle after timer expires during Polling. If disabled (0), Gasket will assert / de-assert GoToRxElecIdle purely based on Gotorxelecidle assertion upon RxElecIdle de-assertion (LFPS detected) enable bit (G2RXERXEE) and Gotorxelecidle assertion when not transmitting high speed data enable bit (G2RXETXHSDE) **Power Well:** SUS
1	1b RW	**GotoRxElecidle Assertion Upon RxElecIdle Exit Enable (G2RXERXEE):** When enabled (set to '1'), allow Gasket to assert GoToRxElecIdle to UAFE to turn off its receiver upon the de-assertion of GoToRxElecIdle (LFPS detected). This bit needs to be programmed when the USB3 port is not enabled. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	1b RW	**GotoRxElecidle Assertion When Transmitting High Speed Data Enable (G2RXETXHSDE):** When enabled (set to '1'), allow Gaskets to assert GoToRxElecIdle to UAFE to turn off its receiver when not transmitting high speed data: P0 and TxElecIdle = 1. This bit needs to be programmed when the USB3 port is not enabled. **Power Well:** SUS

18.6.37 XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1)—Offset C0h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:20, F:0] + C0h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																				OC2M				Rsvd0				OC1M			

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Rsvd1:** Reserved **Power Well:** SUS
11:8	0h RW/L	**OC2 Mapping (OC2M):** Each bit position maps OC2 to a set of ports as follows: The OC2 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. Bit 15 14 13 12 11 10 9 8 Port 8 7 6 5 4 3 2 1 **Power Well:** SUS
7:4	0h RO	**Rsvd0:** Reserved **Power Well:** SUS
3:0	0h RW/L	**OC1 Mapping (OC1M):** Each bit position maps OC1 to a set of ports as follows: The OC1 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin Bit 7 6 5 4 3 2 1 0 Port 8 7 6 5 4 3 2 1 **Power Well:** SUS

18.6.38 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2)—Offset C4h

Reserved

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:20, F:0] + C4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Rsvd1:** Reserved **Power Well:** Core

18.6.39 XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1)—Offset C8h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + C8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1							OC4M	Rsvd2							OC3M	Rsvd3							OC2M	Rsvd4							OC1M

Bit Range	Default & Access	Field Name (ID): Description
31:25	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
24	0b RW/L	**OC4 Mapping (OC4M):** Each bit position maps OC4 to a set of ports as follows: The OC4 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. Bit 27 26 25 24 Port 4 3 2 1 **Power Well:** SUS
23:17	00h RO	**Rsvd2:** Reserved. **Power Well:** Core
16	0b RW/L	**OC3 Mapping (OC3M):** Each bit position maps OC3 to a set of ports as follows: The OC3 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. Bit 19 18 17 16 Port 4 3 2 1 **Power Well:** SUS
15:9	00h RO	**Rsvd3:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8	0b RW/L	**OC2 Mapping (OC2M):** Each bit position maps OC2 to a set of ports as follows: The OC2 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. Bit 11 10 9 8 Port 4 3 2 1 **Power Well:** SUS
7:1	00h RO	**Rsvd4:** Reserved. **Power Well:** Core
0	0b RW/L	**OC1 Mapping (OC1M):** Each bit position maps OC1 to a set of ports as follows: The OC1 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin Bit 3 2 1 0 Port 4 3 2 1 **Power Well:** SUS

18.6.40 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2)—Offset CCh

The RW/L property of this register is controlled by OCCFDONE bit. Note: U3OCM2 allows the OC pins 8:5 to be mapped to the same 6 SS ports that U3OCM1 allows. This a llows flexibility in pairing SS ports with HS ports at the connector. Care must be taken to make s ure OC pin assignment is consistent across USB3 and USB2 ports (depending upon the pairing).

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + CCh

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1							OC8M	Rsvd2							OC7M	Rsvd3							OC6M	Rsvd4							OC5M

Bit Range	Default & Access	Field Name (ID): Description
31:25	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
24	0b RW/L	**OC8 Mapping (OC8M):** Each bit position maps OC8 to a set of ports as follows: The OC8 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to e nsure that a given port's bit map is set only for one OC pin. Bit 24 Port 1 **Power Well:** SUS
23:17	00h RO	**Rsvd2:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
16	0b RW/L	**OC7 Mapping (OC7M):** Each bit position maps OC7 to a set of ports as follows: The OC7 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to e nsure that a given port's bit map is set only for one OC pin. Bit 16 Port 1 **Power Well:** SUS
15:9	00h RO	**Rsvd3:** Reserved. **Power Well:** Core
8	0b RW/L	**OC6 Mapping (OC6M):** Each bit position maps OC6 to a set of ports as follows: The OC6 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to e nsure that a given port's bit map is set only for one OC pin. Bit 8 Port 1 **Power Well:** SUS
7:1	00h RO	**Rsvd4:** Reserved. **Power Well:** Core
0	0b RW/L	**OC5 Mapping (OC5M):** Each bit position maps OC5 to a set of ports as follows: The OC5 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to e nsure that a given port's bit map is set only for one OC pin Bit 0 Port 1 **Power Well:** SUS

18.6.41 USB2 Port Routing (USB2PR)—Offset D0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + D0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd1 (bits 31:9) | USB2HCSEL (bits 8:0)

Bit Range	Default & Access	Field Name (ID): Description
31:9	000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
8:0	000h RW	**USB2 HC Selector (USB2HCSEL):** This field maps the USB2 port between the XHCI and EHCI controller (it has no effect on USB3). When set to 1, Routes USB2 pins to the XHCI controller. Routes OC pin to XHCI (based on the mapping in the OC register). Masks the USB2 port from the EHCI. Masks OC pin from ECHI. When set to 0, Routes all the USB2 pins to the legacy EHCI. Routes OC pin to EHCI (based on the mapping in the OC register). Masks the USB2 port from the XHCI. Masks OC pin from XHCI. Port to bit mapping is in one-hot encoding, i.e. bit 0 controls port 1 and so on. **Power Well:** SUS

18.6.42 USB2 Port Routing Mask (USB2PRM)—Offset D4h

The RW/L property of this register is controlled by the ACCTRL bit.

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + D4h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Rsvd1						USB2HCSELM	

Bit Range	Default & Access	Field Name (ID): Description
31:9	000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
8:0	000h RW/L	**USB2 HC Selector Mask (USB2HCSELM):** This field allows the BIOS to communicate to the OS which USB 2.0 ports can be switched from the EHCI controller to the xHCI controller. When set to 1, The OS may switch the USB 2.0 port between the EHCI and xHCI host controllers by modifying the corresponding USB2HCSEL bit. When set to 0, The OS shall not modify the corresponding USB2HCSEL bit. BIOS shall set this bit to a '1' if the corresponding USB2HCSEL bit is RW, unless it knows an internal USB 2.0 device attached to that port will not work under xHCI. Port to bit mapping is in one-hot encoding, i.e. bit 0 controls port 1 and so on. **Power Well:** Core

18.6.43 USB3 Port Routing (USB3PR)—Offset D8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + D8h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Rsvd1							USB3SSEN

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**USB3 SS Enable (USB3SSEN):** This field controls whether SuperSpeed capability is enabled for a given USB3 port. When set to 1, Enables SS termination Enables PORTSC to to see the connects on the ports. When set to 0, Disables SS termination Blocks PORTSC from reporting attach/connect. Places port in the lowest power state. **Power Well:** SUS

18.6.44 USB3 Port Routing Mask (USB3PRM)—Offset DCh

The RW/L property of this register is controlled by the ACCTRL bit.

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + DCh

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																												USB3SSENM			

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
3:0	0h RW/L	**USB3 SS Enable Mask (USB3SSENM):** This field allows the BIOS to communicate to the OS which USB 3.0 ports can have the SuperSpeed capabilities enabled. When set to 1, The OS may enable or disable the SuperSpeed capabilities by modifying the corresponding USB3SSEN bit. When set to 0, The OS shall not modify the corresponding USB3SSEN bit. BIOS shall set this bit to a '1' if the corresponding USB3SSEN bit is RW, unless the BIOS has cleared the USB2HCSELM bit for a USB 2.0 port and the BIOS wishes the OS to disable the corresponding SuperSpeed terminations for that physical connector. Port to bit mapping is in one-hot encoding, i.e. bit 0 controls port 1 and so on. **Power Well:** Core

18.6.45 Fuse and Strap (FUS)—Offset E0h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + E0h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Rsvd1	SPARE	USH_DEVID	XDD_EN	SRAMPWRGTDIS	USB2PLLSDIS	USBIOPMDIS	XHCDCGDIS	USBRDIS	SSPRTCNT	HSPRTCNT	XHCFD

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
23:14	000h RO/V	**Spare Fuses (SPARE):** Will be used for VLV2. **Power Well:** SUS
13:11	000b RO/V	**USH DevID (USH_DEVID):** LSB bits of USH PCIe Device ID The 3 LSB bits enable defining up to 8 separate USH SKUs if required **Power Well:** SUS
10	0b RO/V	**Debug Device Enable (XDD_EN):** 0 : Debug Device is Enabled 1: Debug Device is Disabled **Power Well:** SUS
9	0h RO/V	**SRAM Power Gating Disable (SRAMPWRGTDIS):** 0: SRAM Power Gating Enabled 1: SRAM Power Gating Disabled **Power Well:** SUS
8	0h RO/V	**USB2 PLL Shutdown Disable (USB2PLLSDIS):** 0: USB2 PLL shutdown enabled 1: USB2 PLL shutdown disabled **Power Well:** SUS
7	0h RO/V	**USB I/O Power Management Disable (USBIOPMDIS):** 0: USB2 HW LPM and USB3 HW Ux under XHC enabled 1: USB2 HW LPM and USB3 HW Ux under XHC disabled **Power Well:** SUS
6	0h RO/V	**XHC Dynamic Clock Gating Disable (XHCDCGDIS):** 0: USB3 (XHC) dynamic clock gating enabled 1: USB3 (XHC) dynamic clock gating disabled **Power Well:** SUS
5	0h RO/V	**USBr Disable (USBRDIS):** 0: USBr enabled 1: USBr disabled **Power Well:** SUS
4:3	0h RO/V	**SS Port Count (SSPRTCNT):** This field specifies number of SS ports present. Supported combinations are: 00: 6 SS ports 01: 4 SS ports 10: 2 SS ports 11: 0 SS ports **Power Well:** SUS
2:1	0h RO/V	**HS Port Count (HSPRTCNT):** This field specifies number HS ports present. Supported combinations are: 00: 14 HS ports 01: 12 HS ports 10: 10 HS ports 11: N/A (reserved) **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO/V	**XHCI Function Disable (XHCFD):** When asserted, it indicates the XHCI is fused to function disabled. **Power Well:** SUS

18.6.46 USB2 Port Disable Override (USB2PDO)—Offset E4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + E4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																												USB2PDO			

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
3:0	0h RW/O	**USB2 Port Disable Override (USB2PDO):** A '1' in a bit position prevents the corresponding USB2 port from reporting a Device Connection to the XHC. **Power Well:** SUS

18.6.47 USB3 Port Disable Override (USB3PDO)—Offset E8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + E8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																												USB3PDO			

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW/O	**USB3 Port Disable Override (USB3PDO):** A '1' in a bit position prevents the corresponding USB3 port from reporting a Device Connection to the XHC. **Power Well:** SUS

18.6.48 USB2 FS/LS Port Staggering Control (FSLSPS)—Offset ECh

The host controller provides a programmable time offset for each FS/LS port. Based on the value programmed in these registers, the controller will inject a fixed delay on each FS or LS transaction initiated on that port.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + ECh

Default: 0000D8D8h

31–16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
0000 0000 0000 0000	1 1	0 1	1 0	0 0	1 1	0 1	1 0	0 0
RSVD1	FSLSPS8	FSLSPS7	FSLSPS6	FSLSPS5	FSLSPS4	FSLSPS3	FSLSPS2	FSLSPS1

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1 (RSVD1):** Reserved for Future Use **Power Well:** Core
15:14	11b RW	**FS/LS Stagger Offset for USB2 Port 8 (FSLSPS8):** FS/LS Stagger Offset for USB2 Port 8 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** Core
13:12	01b RW	**FS/LS Stagger Offset for USB2 Port 7 (FSLSPS7):** FS/LS Stagger Offset for USB2 Port 7 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** Core
11:10	10b RW	**FS/LS Stagger Offset for USB2 Port 6 (FSLSPS6):** FS/LS Stagger Offset for USB2 Port 6 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** Core
9:8	00b RW	**FS/LS Stagger Offset for USB2 Port 5 (FSLSPS5):** FS/LS Stagger Offset for USB2 Port 5 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** Core
7:6	11b RW	**FS/LS Stagger Offser for USB2 Port 4 (FSLSPS4):** FS/LS Stagger Offset for USB2 Port 4 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:4	01b RW	**FS/LS Stagger Offset for USB2 Port 3 (FSLSPS3):** FS/LS Stagger Offset for USB2 Port 3 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** Core
3:2	10b RW	**FS/LS Stagger Offser for USB2 Port 2 (FSLSPS2):** FS/LS Stagger Offset for USB2 Port 2 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** Core
1:0	00b RW	**FS/LS Stagger Offset for USB2 Port 1 (FSLSPS1):** FS/LS Stagger Offset for USB2 Port 1 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** Core

18.6.49 DFT 1 (DFT1)—Offset F0h

Not for EDS

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + F0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSDFTCRC | Rsvd1 | SSDFTLMSEL | SSDFTCRCSEL | SSDFTCPS

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Super Speed DFT CRC (SSDFTCRC):** These register bits contain the value of Super Speed DFT CRC **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7	0h RW	**Super Speed DFT LFPS Mode Select (SSDFTLMSEL):** This bit selects the Super Speed DFT LFPS mode, and will only take effect when Super Speed HBP mode is enabled. 0b: HBP logic will internally loopback TX LFPS as RX LFPS and AFE RX LFPS path to the controller is disconnected. 1b: RX LFPS path works normally **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
6:3	0h RW	**Super Speed DFT CRC Select (SSDFTCRCSEL):** Super Speed DFT CRC Select (SSDFTCRCSEL): These bits select which Super Speed DFT CRC value is reflected in SSDFTCRC bits. In addition, these bits also select which SuperSpeed DFT CRC MSB value is sent to GPIO monitor pin, i.e. sata3gp_gp37 to aid silicon debug. Live version of selected CRC's MSB will be sent to GPIO monitor pin, i.e. sata3gp_gp37. 0h (default): No SuperSpeed DFT CRC is selected. 1h: Data Payload CRC 2h: Link Management Packet CRC 3h: Transaction Packet CRC 4h: Isochronous Timestamp Packet CRC 5h: Data Packet Header CRC 6h: Link Command Packet CRC Others: Reserved **Power Well:** Core
2:0	0h RW	**Super Speed DFT CRC Port Select (SSDFTCPS):** One CRC per packet type is shared for all the Super Speed ports. These bits select the Super Speed port for which CRC data will be updated. 000b: (default) No SuperSpeed Port is selected 001b: Super Speed Port 0 010b: Super Speed Port 1 011b: Super Speed Port 2 100b: Super Speed Port 3 101b: Super Speed Port 4 110b: Super Speed Port 5 Others: Reserved **Power Well:** Core

18.6.50 DFT 2 (DFT2)—Offset F4h

Not for EDS

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**Offset:** [B:0, D:20, F:0] + F4h

Default: 00000000h

Bits	31:16	15:12	11:8	7:6	5	4:3	2:1	0
Default	0000 0000 0000 0000	0000	0000	00	0	00	00	0
Field	TXCRC	UTMIDFTPS	UTMILPBKLOOPN_3_0	UTMIOPMODE_1_0	UTMITERMSEL	UTMIXCVRSELECT_1_0	UTMILPBKSTS	UTMILPBKEN

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**TX CRC (TXCRC):** These register bits contain the value of TX CRC. This TX CRC is placed right after the 480MHz XCLKQ. **Power Well:** Core
15:12	0h RW	**UTMI+ DFT Port Select (UTMIDFTPS):** One CRC is shared for all the UTMI+ ports. These bits select the UTMI+ port for which CRC data will be updated and loopback status reflected in UTMILPBKSTS. 0h: (default) No UTMI+ Port is selected 1h: UTMI+ Port 0 2h: UTMI+ Port 1 3h: UTMI+ Port 2 4h: UTMI+ Port 3 5h: UTMI+ Port 4 6h: UTMI+ Port 5 7h: UTMI+ Port 6 8h: UTMI+ Port 7 9h: UTMI+ Port 8 Ah: UTMI+ Port 9 Bh: UTMI+ Port 10 Ch: UTMI+ Port 11 Dh: UTMI+ Port 12 Eh: UTMI+ Port 13 Others: Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW	**Loop Number (UTMILPBKLOOPN_3_0):** Number of repeatable fixed pattern within a packet Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) **Power Well:** Core
7:6	0h RW	**Operational Mode (UTMIOPMODE_1_0):** Operational Mode in test mode. These signals select between various operational modes: 00b: Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved **Power Well:** Core
5	0h RW	**Termination Select (UTMITERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled **Power Well:** Core
4:3	0h RW	**Transceiver Select (UTMIXCVRSELECT_1_0):** Transceiver Select in test mode. This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved **Power Well:** Core
2:1	0h RO	**UTMI+ Loopback Status (UTMILPBKSTS):** Loopback Status for port selected by UTMIDFTPS 00b: Reset condition 01b: Comparator has started receiving data and the received data matches with the TX pattern. 10b: Comparator has started receiving data the received data does not match with the TX pattern but there was no assertion of RC error from UTMI. 11b: Comparator has started receiving data and RX ERROR was asserted for at least one clock by UTMI. Note that this does not reflect the status of pattern comparison since RX error from UTMI is unexpected for loopback. **Power Well:** Core
0	0h RW	**Loopback Enable (UTMILPBKEN):** Enable loopback test mode. If asserted, loopback test mode is enabled **Power Well:** Core

18.6.51 Manufacturing Process ID (MANID)—Offset F8h

Not for EDS

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + F8h

Default: 00000F00h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0
Field	Rsvd	DPID	SID		MNFR		PPID	

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (Rsvd):** Reserved. **Power Well:** Core
27:24	0h RO/V	**Dot Portion Process ID (DPID):** See Chap 6 for value **Power Well:** Core
23:16	00h RO/V	**Stepping ID (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate stepping when the Revision ID may not change. See Chap 6 for value **Power Well:** Core
15:8	0Fh RO	**Manufacturer (MNFR):** 0Fh = Intel. **Power Well:** Core
7:0	00h RO/V	**Process Portion Process ID (PPID):** See Chap 6 for value **Power Well:** Core

18.6.52 DFT 3 (DFT3)—Offset FCh

Not for EDS

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + FCh

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Bits 31:16	Bits 15:10	Bits 9:2	Bit 1	Bit 0
UTMILPBKPAT	RSVD	UTMILPBKSEL_7_0	UTMILPBKPATSEL	UTMILPBKTYPE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Loopback Pattern (UTMILPBKPAT):** 2-byte pattern for loopback Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern **Power Well:** Core
15:10	00h RO	**Reserved (RSVD):** Reserved **Power Well:** Core
9:2	00h RW	**Loopback Lane Select (UTMILPBKSEL_7_0):** Port is selected if the corresponding bit is selected Note: MSB is for UTMI+ Port13, LSB is for UTMI+ Port0 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**Loopback Pattern (UTMILPBKPATSEL):** Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet **Power Well:** Core
0	0b RW	**Loopback Type (UTMILPBKTYPE):** Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 0b: Digital Near-End Loopback (DNELB) 1b: Analog Near-End Loopback (ANELB) Note: Analog Far-End Loopback (AFELB) is not supported **Power Well:** Core

18.7 USB xHCI Memory Mapped I/O Registers

Table 213. Summary of USB xHCI Memory Mapped I/O Registers—MBAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–0h	1	"Capability Registers Length (CAPLENGTH)—Offset 0h" on page 2176	80h
2–3h	2	"Host Controller Interface Version Number (HCIVERSION)—Offset 2h" on page 2176	0100h
4–7h	4	"Structural Parameters 1 (HCSPARAMS1)—Offset 4h" on page 2177	07000820h
8–Bh	4	"Structural Parameters 2 (HCSPARAMS2)—Offset 8h" on page 2178	84000054h
C–Fh	4	"Structural Parameters 3 (HCSPARAMS3)—Offset Ch" on page 2179	00040001h
10–13h	4	"Capability Parameters (HCCPARAMS)—Offset 10h" on page 2180	200071E1h
14–17h	4	"Doorbell Offset (DBOFF)—Offset 14h" on page 2182	00003000h
18–1Bh	4	"Runtime Register Space Offset (RTSOFF)—Offset 18h" on page 2182	00002000h
80–83h	4	"USB Command (USBCMD)—Offset 80h" on page 2183	00000000h
84–87h	4	"USB Status (USBSTS)—Offset 84h" on page 2185	00000001h
88–8Bh	4	"Page Size (PAGESIZE)—Offset 88h" on page 2187	00000001h
94–97h	4	"Device Notification Control (DNCTRL)—Offset 94h" on page 2188	00000000h
98–9Bh	4	"Command Ring Low (CRCR_LO)—Offset 98h" on page 2189	00000000h
9C–9Fh	4	"Command Ring High (CRCR_HI)—Offset 9Ch" on page 2190	00000000h
B0–B3h	4	"Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h" on page 2191	00000000h
B4–B7h	4	"Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h" on page 2191	00000000h
B8–BBh	4	"Configure (CONFIG)—Offset B8h" on page 2192	00000000h
480–483h	4	"Port 1 Status and Control USB3 (PORTSC1USB2)—Offset 480h" on page 2193	000002A0h
484–487h	4	"Port 1 Power Management Status and Control USB2 (PORTPMSC1USB2)—Offset 484h" on page 2194	00000000h
48C–48Fh	4	"Port X Hardware LPM Control Register (PORTHLPM1)—Offset 48Ch" on page 2196	00000000h
490–493h	4	"Port 2 Status and Control USB3 (PORTSC2USB2)—Offset 490h" on page 2197	000002A0h
494–497h	4	"Port 2 Power Management Status and Control USB2 (PORTPMSC2USB2)—Offset 494h" on page 2199	00000000h
49C–49Fh	4	"Port X Hardware LPM Control Register (PORTHLPM2)—Offset 49Ch" on page 2200	00000000h
4A0–4A3h	4	"Port 3 Status and Control USB3 (PORTSC3USB2)—Offset 4A0h" on page 2200	000002A0h
4A4–4A7h	4	"Port 3 Power Management Status and Control USB2 (PORTPMSC3USB2)—Offset 4A4h" on page 2202	00000000h
4AC–4AFh	4	"Port X Hardware LPM Control Register (PORTHLPM3)—Offset 4ACh" on page 2203	00000000h
4B0–4B3h	4	"Port 4 Status and Control USB3 (PORTSC4USB2)—Offset 4B0h" on page 2204	000002A0h
4B4–4B7h	4	"Port 4 Power Management Status and Control USB2 (PORTPMSC4USB2)—Offset 4B4h" on page 2206	00000000h

Table 213. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4BC–4BFh	4	"Port X Hardware LPM Control Register (PORTHLPM4)—Offset 4BCh" on page 2207	00000000h
4C0–4C3h	4	"Port 8 Status and Control USB2 (PORTSC5USB2)—Offset 4C0h" on page 2208	000002A0h
4C4–4C7h	4	"Port 5 Power Management Status and Control USB2 (PORTPMSC5USB2)—Offset 4C4h" on page 2210	00000000h
4CC–4CFh	4	"Port X Hardware LPM Control Register (PORTHLPM5)—Offset 4CCh" on page 2211	00000000h
4D0–4D3h	4	"Port 6 Status and Control USB2 (PORTSC6USB2)—Offset 4D0h" on page 2212	000002A0h
4D4–4D7h	4	"Port 6 Power Management Status and Control USB2 (PORTPMSC6USB2)—Offset 4D4h" on page 2214	00000000h
4DC–4DFh	4	"Port X Hardware LPM Control Register (PORTHLPM6)—Offset 4DCh" on page 2215	00000000h
4E0–4E3h	4	"Port 1 Status and Control USB3 (PORTSC1USB3)—Offset 4E0h" on page 2215	000002A0h
4E4–4E7h	4	"Port 1 Power Management Status and Control USB3 (PORTPMSC1USB3)—Offset 4E4h" on page 2217	00000000h
4E8–4EBh	4	"Port 1 Link Info (PORTLI1)—Offset 4E8h" on page 2218	00000000h
2000–2003h	4	"Microframe Index (MFINDEX)—Offset 2000h" on page 2219	00000000h
2020–2023h	4	"Interrupter 1 Management (IMAN1)—Offset 2020h" on page 2219	00000000h
2024–2027h	4	"Interrupter 1 Moderation (IMOD1)—Offset 2024h" on page 2220	00000FA0h
2028–202Bh	4	"Event Ring Segment Table Size 1 (ERSTSZ1)—Offset 2028h" on page 2220	00000000h
2030–2033h	4	"Event Ring Segment Table Base Address Low 1 (ERSTBA_LO1)—Offset 2030h" on page 2221	00000000h
2034–2037h	4	"Event Ring Segment Table Base Address High 1 (ERSTBA_HI1)—Offset 2034h" on page 2222	00000000h
2038–203Bh	4	"Event Ring Dequeue Pointer Low 1 (ERDP_LO1)—Offset 2038h" on page 2222	00000000h
203C–203Fh	4	"Event Ring Dequeue Pointer High 1 (ERDP_HI1)—Offset 203Ch" on page 2223	00000000h
2040–2043h	4	"Interrupter 2 Management (IMAN2)—Offset 2040h" on page 2223	00000000h
2044–2047h	4	"Interrupter 2 Moderation (IMOD2)—Offset 2044h" on page 2224	00000FA0h
2048–204Bh	4	"Event Ring Segment Table Size 2 (ERSTSZ2)—Offset 2048h" on page 2225	00000000h
2050–2053h	4	"Event Ring Segment Table Base Address Low 2 (ERSTBA_LO2)—Offset 2050h" on page 2225	00000000h
2054–2057h	4	"Event Ring Segment Table Base Address High 2 (ERSTBA_HI2)—Offset 2054h" on page 2226	00000000h
2058–205Bh	4	"Event Ring Dequeue Pointer Low 2 (ERDP_LO2)—Offset 2058h" on page 2227	00000000h
205C–205Fh	4	"Event Ring Dequeue Pointer High 2 (ERDP_HI2)—Offset 205Ch" on page 2227	00000000h
2060–2063h	4	"Interrupter 3 Management (IMAN3)—Offset 2060h" on page 2228	00000000h
2064–2067h	4	"Interrupter 3 Moderation (IMOD3)—Offset 2064h" on page 2228	00000FA0h

Table 213. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2068–206Bh	4	“Event Ring Segment Table Size 3 (ERSTSZ3)—Offset 2068h” on page 2229	00000000h
2070–2073h	4	“Event Ring Segment Table Base Address Low 3 (ERSTBA_LO3)—Offset 2070h” on page 2230	00000000h
2074–2077h	4	“Event Ring Segment Table Base Address High 3 (ERSTBA_HI3)—Offset 2074h” on page 2230	00000000h
2078–207Bh	4	“Event Ring Dequeue Pointer Low 3 (ERDP_LO3)—Offset 2078h” on page 2231	00000000h
207C–207Fh	4	“Event Ring Dequeue Pointer High 3 (ERDP_HI3)—Offset 207Ch” on page 2232	00000000h
2080–2083h	4	“Interrupter 4 Management (IMAN4)—Offset 2080h” on page 2232	00000000h
2084–2087h	4	“Interrupter 4 Moderation (IMOD4)—Offset 2084h” on page 2233	00000FA0h
2088–208Bh	4	“Event Ring Segment Table Size 4 (ERSTSZ4)—Offset 2088h” on page 2233	00000000h
2090–2093h	4	“Event Ring Segment Table Base Address Low 4 (ERSTBA_LO4)—Offset 2090h” on page 2234	00000000h
2094–2097h	4	“Event Ring Segment Table Base Address High 4 (ERSTBA_HI4)—Offset 2094h” on page 2235	00000000h
2098–209Bh	4	“Event Ring Dequeue Pointer Low 4 (ERDP_LO4)—Offset 2098h” on page 2235	00000000h
209C–209Fh	4	“Event Ring Dequeue Pointer High 4 (ERDP_HI4)—Offset 209Ch” on page 2236	00000000h
20A0–20A3h	4	“Interrupter 5 Management (IMAN5)—Offset 20A0h” on page 2236	00000000h
20A4–20A7h	4	“Interrupter 5 Moderation (IMOD5)—Offset 20A4h” on page 2237	00000FA0h
20A8–20ABh	4	“Event Ring Segment Table Size 5 (ERSTSZ5)—Offset 20A8h” on page 2238	00000000h
20B0–20B3h	4	“Event Ring Segment Table Base Address Low 5 (ERSTBA_LO5)—Offset 20B0h” on page 2238	00000000h
20B4–20B7h	4	“Event Ring Segment Table Base Address High 5 (ERSTBA_HI5)—Offset 20B4h” on page 2239	00000000h
20B8–20BBh	4	“Event Ring Dequeue Pointer Low 5 (ERDP_LO5)—Offset 20B8h” on page 2240	00000000h
20BC–20BFh	4	“Event Ring Dequeue Pointer High 5 (ERDP_HI5)—Offset 20BCh” on page 2240	00000000h
20C0–20C3h	4	“Interrupter 6 Management (IMAN6)—Offset 20C0h” on page 2241	00000000h
20C4–20C7h	4	“Interrupter 6 Moderation (IMOD6)—Offset 20C4h” on page 2241	00000FA0h
20C8–20CBh	4	“Event Ring Segment Table Size 6 (ERSTSZ6)—Offset 20C8h” on page 2242	00000000h
20D0–20D3h	4	“Event Ring Segment Table Base Address Low 6 (ERSTBA_LO6)—Offset 20D0h” on page 2243	00000000h
20D4–20D7h	4	“Event Ring Segment Table Base Address High 6 (ERSTBA_HI6)—Offset 20D4h” on page 2243	00000000h
20D8–20DBh	4	“Event Ring Dequeue Pointer Low 6 (ERDP_LO6)—Offset 20D8h” on page 2244	00000000h
20DC–20DFh	4	“Event Ring Dequeue Pointer High 6 (ERDP_HI6)—Offset 20DCh” on page 2245	00000000h
20E0–20E3h	4	“Interrupter 7 Management (IMAN7)—Offset 20E0h” on page 2245	00000000h

Table 213. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20E4–20E7h	4	"Interrupter 7 Moderation (IMOD7)—Offset 20E4h" on page 2246	00000FA0h
20E8–20EBh	4	"Event Ring Segment Table Size 7 (ERSTSZ7)—Offset 20E8h" on page 2246	00000000h
20F0–20F3h	4	"Event Ring Segment Table Base Address Low 7 (ERSTBA_LO7)—Offset 20F0h" on page 2247	00000000h
20F4–20F7h	4	"Event Ring Segment Table Base Address High 7 (ERSTBA_HI7)—Offset 20F4h" on page 2248	00000000h
20F8–20FBh	4	"Event Ring Dequeue Pointer Low 7 (ERDP_LO7)—Offset 20F8h" on page 2248	00000000h
20FC–20FFh	4	"Event Ring Dequeue Pointer High 7 (ERDP_HI7)—Offset 20FCh" on page 2249	00000000h
2100–2103h	4	"Interrupter 8 Management (IMAN8)—Offset 2100h" on page 2249	00000000h
2104–2107h	4	"Interrupter 8 Moderation (IMOD8)—Offset 2104h" on page 2250	00000FA0h
2108–210Bh	4	"Event Ring Segment Table Size 8 (ERSTSZ8)—Offset 2108h" on page 2251	00000000h
2110–2113h	4	"Event Ring Segment Table Base Address Low 8 (ERSTBA_LO8)—Offset 2110h" on page 2251	00000000h
2114–2117h	4	"Event Ring Segment Table Base Address High 8 (ERSTBA_HI8)—Offset 2114h" on page 2252	00000000h
2118–211Bh	4	"Event Ring Dequeue Pointer Low 8 (ERDP_LO8)—Offset 2118h" on page 2253	00000000h
211C–211Fh	4	"Event Ring Dequeue Pointer High 8 (ERDP_HI8)—Offset 211Ch" on page 2253	00000000h
3000–3003h	4	"Door Bell 1 (DOORBELL1)—Offset 3000h" on page 2254	00000000h
3004–3007h	4	"Door Bell 2 (DOORBELL2)—Offset 3004h" on page 2255	00000000h
3008–300Bh	4	"Door Bell 3 (DOORBELL3)—Offset 3008h" on page 2256	00000000h
300C–300Fh	4	"Door Bell 4 (DOORBELL4)—Offset 300Ch" on page 2256	00000000h
3010–3013h	4	"Door Bell 5 (DOORBELL5)—Offset 3010h" on page 2257	00000000h
3014–3017h	4	"Door Bell 6 (DOORBELL6)—Offset 3014h" on page 2257	00000000h
3018–301Bh	4	"Door Bell 7 (DOORBELL7)—Offset 3018h" on page 2258	00000000h
301C–301Fh	4	"Door Bell 8 (DOORBELL8)—Offset 301Ch" on page 2258	00000000h
3020–3023h	4	"Door Bell 9 (DOORBELL9)—Offset 3020h" on page 2259	00000000h
3024–3027h	4	"Door Bell 10 (DOORBELL10)—Offset 3024h" on page 2260	00000000h
3028–302Bh	4	"Door Bell 11 (DOORBELL11)—Offset 3028h" on page 2260	00000000h
302C–302Fh	4	"Door Bell 12 (DOORBELL12)—Offset 302Ch" on page 2261	00000000h
3030–3033h	4	"Door Bell 13 (DOORBELL13)—Offset 3030h" on page 2261	00000000h
3034–3037h	4	"Door Bell 14 (DOORBELL14)—Offset 3034h" on page 2262	00000000h
3038–303Bh	4	"Door Bell 15 (DOORBELL15)—Offset 3038h" on page 2262	00000000h
303C–303Fh	4	"Door Bell 16 (DOORBELL16)—Offset 303Ch" on page 2263	00000000h
3040–3043h	4	"Door Bell 17 (DOORBELL17)—Offset 3040h" on page 2264	00000000h
3044–3047h	4	"Door Bell 18 (DOORBELL18)—Offset 3044h" on page 2264	00000000h
3048–304Bh	4	"Door Bell 19 (DOORBELL19)—Offset 3048h" on page 2265	00000000h
304C–304Fh	4	"Door Bell 20 (DOORBELL20)—Offset 304Ch" on page 2265	00000000h

Table 213. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3050–3053h	4	"Door Bell 21 (DOORBELL21)—Offset 3050h" on page 2266	00000000h
3054–3057h	4	"Door Bell 22 (DOORBELL22)—Offset 3054h" on page 2266	00000000h
3058–305Bh	4	"Door Bell 23 (DOORBELL23)—Offset 3058h" on page 2267	00000000h
305C–305Fh	4	"Door Bell 24 (DOORBELL24)—Offset 305Ch" on page 2268	00000000h
3060–3063h	4	"Door Bell 25 (DOORBELL25)—Offset 3060h" on page 2268	00000000h
3064–3067h	4	"Door Bell 26 (DOORBELL26)—Offset 3064h" on page 2269	00000000h
3068–306Bh	4	"Door Bell 27 (DOORBELL27)—Offset 3068h" on page 2269	00000000h
306C–306Fh	4	"Door Bell 28 (DOORBELL28)—Offset 306Ch" on page 2270	00000000h
3070–3073h	4	"Door Bell 29 (DOORBELL29)—Offset 3070h" on page 2270	00000000h
3074–3077h	4	"Door Bell 30 (DOORBELL30)—Offset 3074h" on page 2271	00000000h
3078–307Bh	4	"Door Bell 31 (DOORBELL31)—Offset 3078h" on page 2272	00000000h
307C–307Fh	4	"Door Bell 32 (DOORBELL32)—Offset 307Ch" on page 2272	00000000h
8000–8003h	4	"XECP_SUPP_USB2_0—Offset 8000h" on page 2273	02000802h
8004–8007h	4	"XECP_SUPP_USB2_1—Offset 8004h" on page 2273	20425355h
8008–800Bh	4	"XECP_SUPP_USB2_2—Offset 8008h" on page 2274	30190601h
8010–8013h	4	"XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h" on page 2275	000C0021h
8014–8017h	4	"XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h" on page 2276	05DC0012h
8018–801Bh	4	"XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h" on page 2276	01E00023h
8020–8023h	4	"XECP_SUPP_USB3_0—Offset 8020h" on page 2277	03000802h
8024–8027h	4	"XECP_SUPP_USB3_1—Offset 8024h" on page 2278	20425355h
8028–802Bh	4	"XECP_SUPP_USB3_2—Offset 8028h" on page 2278	10000107h
8030–8033h	4	"XECP_SUPP_USB3_3—Offset 8030h" on page 2279	00050134h
8040–8043h	4	"XECP_CMDM_STS0—Offset 8040h" on page 2280	00000CC1h
8044–8047h	4	"XECP_CMDM_STS1—Offset 8044h" on page 2282	03FC0000h
8048–804Bh	4	"XECP_CMDM_STS2—Offset 8048h" on page 2282	00000000h
804C–804Fh	4	"XECP_CMDM_STS3—Offset 804Ch" on page 2283	00000000h
8050–8053h	4	"XECP_CMDM_STS4—Offset 8050h" on page 2283	00000000h
8054–8057h	4	"XECP_CMDM_STS5—Offset 8054h" on page 2284	00000000h
8070–8073h	4	"Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h" on page 2284	0000FCC0h
8078–807Bh	4	"Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h" on page 2285	00000000h
807C–807Fh	4	"Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch" on page 2286	00000000h
8080–8083h	4	"Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h" on page 2286	00000000h
8094–8097h	4	"Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h" on page 2287	00008100h

Table 213. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80A0–80A3h	4	"Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h" on page 2288	00003C0Fh
80C0–80C3h	4	"AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h" on page 2289	015FC0F0h
80C4–80C7h	4	"Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h" on page 2292	004A4008h
80C8–80CBh	4	"High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h" on page 2293	0001A01Fh
80CC–80CFh	4	"Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh" on page 2294	00014080h
80D0–80D3h	4	"System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h" on page 2294	00032010h
80D4–80D7h	4	"Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h" on page 2295	00000000h
80D8–80DBh	4	"AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 80D8h" on page 2296	00000000h
80E0–80E3h	4	"AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h" on page 2297	808DBCA0h
80E4–80E7h	4	"Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h" on page 2299	00000000h
80E8–80EBh	4	"Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h" on page 2300	00800080h
80EC–80EFh	4	"SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh" on page 2301	18010600h
80F0–80F3h	4	"USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h" on page 2303	310003A0h
80F4–80F7h	4	"USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h" on page 2306	80C40620h
80F8–80FBh	4	"USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h" on page 2307	F865EB6Bh
80FC–80FFh	4	"USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh" on page 2307	00008003h
8100–8103h	4	"Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h" on page 2308	00008008h
8108–810Bh	4	"Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h" on page 2309	00000001h
810C–810Fh	4	"Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch" on page 2309	00008020h
8128–812Fh	8	"USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h" on page 2310	0F42528505647F42h
8130–8133h	4	"USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h" on page 2311	00000000h
8134–813Bh	8	"USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h" on page 2312	000C3C640C05140Ch
813C–813Fh	4	"USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch" on page 2313	8D4258B8h
8140–8143h	4	"Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h" on page 2314	0A019132h
8144–8147h	4	"Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h" on page 2314	0000033Fh

Table 213. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8150–8153h	4	"Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8150h" on page 2316	00000000h
8154–8157h	4	"AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h" on page 2317	01390206h
8164–8167h	4	"USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h" on page 2320	000000FCh
8168–816Bh	4	"USB Power Gating Control (USB_PGC)—Offset 8168h" on page 2321	00000000h
816C–816Fh	4	"xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch" on page 2321	00000400h
8170–8173h	4	"USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h" on page 2324	00090032h
8174–8177h	4	"xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h" on page 2325	0040047Dh
8178–817Bh	4	"xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h" on page 2327	000017FFh
817C–817Fh	4	"xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch" on page 2327	00000000h
8180–8183h	4	"xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h" on page 2328	00000000h
8184–8187h	4	"xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h" on page 2329	00000000h
8344–8347h	4	"USB EP Type Lock Policy (USB_EP_TLP)—Offset 8344h" on page 2330	00000000h
8348–834Bh	4	"USB EP Type Lock Policy - Port Control 1 (USB_EP_TLP1)—Offset 8348h" on page 2333	00000000h
834C–834Fh	4	"USB EP Type Lock Policy - Port Control 2 (USB_EP_TLP2)—Offset 834Ch" on page 2335	00000000h
8460–8463h	4	"USB Legacy Support Capability (USBLEGSUP)—Offset 8460h" on page 2336	00000801h
8464–8467h	4	"USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8464h" on page 2337	00000000h
8480–8483h	4	"Debug Capability ID Register (DCID)—Offset 8480h" on page 2338	0005000Ah
8484–8487h	4	"Debug Capability Doorbell Register (DCDB)—Offset 8484h" on page 2339	00000000h
8488–848Bh	4	"Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8488h" on page 2340	00000000h
8490–8497h	8	"Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8490h" on page 2341	0000000000000000h
8498–849Fh	8	"Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8498h" on page 2341	0000000000000000h
84A0–84A3h	4	"Debug Capability Control Register (DCCTRL)—Offset 84A0h" on page 2342	00000000h
84A4–84A7h	4	"Debug Capability Status Register (DCST)—Offset 84A4h" on page 2343	00000000h
84A8–84ABh	4	"Debug Capability Port Status and Control Register (DCPORTSC)—Offset 84A8h" on page 2344	00000000h
84B0–84B7h	8	"Debug Capability Context Pointer Register (DCCP)—Offset 84B0h" on page 2346	0000000000000000h

Table 213. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
84B8–84BBh	4	"Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 84B8h" on page 2347	00000000h
84BC–84BFh	4	"Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 84BCh" on page 2348	00000000h
8530–8533h	4	"Debug Capability Descriptor Parameters (DCDP)—Offset 8530h" on page 2348	00000000h
8538–853Bh	4	"Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8538h" on page 2349	00000000h

18.7.1 Capability Registers Length (CAPLENGTH)—Offset 0h

This register is used as an offset to add to register base, to find the beginning of the Operational Register Space. This register is modified and maintained by BIOS.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

Offset: [MBAR] + 0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
CAPLENGTH							

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Registers Length (CAPLENGTH):** This field is used as an offset to add to register base, to find the beginning of the Operational Register Space. **Power Well:** Core

18.7.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h

This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision, and the least significant bit is the minor revision, e.g. 0100h corresponds to xHCI version 1.0. This register is modified and maintained by BIOS.

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Offset: [MBAR] + 2h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0100h

15			12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

HCIVERSION

Bit Range	Default & Access	Field Name (ID): Description
15:0	0100h RO	**Host Controller Interface Version Number (HCIVERSION):** This is a two-byte field containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this field represents a major revision, and the least significant bit is the minor revision, e.g. 0100h corresponds to xHCI version 1.0. **Power Well:** Core

18.7.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h

This register defines basic structural parameters supported by this xHC implementation: Number of Device Slots support, Interrupters, Root Hub ports, etc. This register is modified and maintained by BIOS.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 07000820h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

MaxPorts | Rsvd1 | MaxIntrs | MaxSlots

Bit Range	Default & Access	Field Name (ID): Description
31:24	07h RO	**Number of Ports (MaxPorts):** This field specifies the maximum Port Number value, i.e the highest number of Port Register Sets that are addressable in the Operational Register Space (refer to the xHCI for USB specification). Valid values are in the range of 1h to FFh. The value in this field shall reflect the maximum Port Number value assigned by an *xHCI Supported Protocol Capability*, described in the xHCI for USB specification. Software shall refer to these capabilities to identify whether a specific Port Number is valid, and the protocol supported by the associated Port Register Set. **Power Well:** Core
23:19	00h RW/L	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
18:8	008h RW/L	**Number of Interrupters (MaxIntrs):** This field specifies the number of Interrupters implemented on this host controller. Each Interrupter is allocated to a vector of MSI-X, and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space (refer to the xHCI for USB specification). Valid values are in the range of 1h to 400h. A '0' in this field is undefined. **Power Well:** Core
7:0	20h RW/L	**Number of Device Slots (MaxSlots):** This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1h to 400h. A '0' in this field is undefined. **Power Well:** Core

18.7.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h

This register defines additional xHC structural parameters. This register is modified and maintained by BIOS.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 84000054h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0

Bits	Field
31:27	MaxScratchpadBufs
26	SPR
25:8	Rsvd1
7:4	ERSTMax
3:0	IST

Bit Range	Default & Access	Field Name (ID): Description
31:27	10h RW/L	**Max Scratchpad Buffers (MaxScratchpadBufs):** Valid values are 0-31. This field indicates the number of Scratchpad Buffers system software shall reserve for the xHC. Refer to xHCI for USB specification for more information. **Power Well:** Core
26	1b RW/L	**Scratchpad Restore (SPR):** If *Max Scratchpad Buffers* is greater than '0' then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If *Max Scratchpad Buffers* is = '0', then this flag shall be '0'. Refer to the xHCI for USB specification for more information. A value of '1' indicates that the xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events. A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
25:8	00000h RW/L	**Rsvd1:** Reserved. **Power Well:** Core
7:4	5h RW/L	**Event Ring Segment Table Max (ERSTMax):** Valid values are 0-15. This field determines the maximum value supported by the *Event Ring Segment Table Base Size* registers (5.5.2.3.1), where The maximum number of Event Ring Segment Table entries = 2^(ERST Max) e.g. if the ERST Max = 7, then the xHC *Event Ring Segment Table(s)* supports up to 128 entries, if ERST Max = 15, then 32K entries, etc. **Power Well:** Core
3:0	4h RW/L	**Isochronous Scheduling Threshold (IST):** The value in this field indicates to system software the minimum distance (in time) that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/microframes. If bit [3] of IST is cleared to '0', software can add a TRB no later than IST[2.0] microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to '1', software can add a TRB no later than IST[2:0] frames before that TRB is scheduled to be executed. Refer to the xHCI for USB specification for details on how software uses this information for scheduling isochronous transfers. **Power Well:** Core

18.7.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch

This register defines link exit latency related structural parameters. This register is modified and maintained by BIOS.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00040001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
U2DEL																Rsvd1								U1DEL							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0004h RW/L	**U2 Device Exit Latency (U2DEL):** Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: • 0000h = Zero • 0001h = Less than 1 s • 0002h = Less than 2 s • • 07FFh = Less than 2047 s. • 0800-FFFFh = Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW/L	**Rsvd1:** Reserved. **Power Well:** Core
7:0	01h RW/L	**U1 Device Exit Latency (U1DEL):** Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: • 01h = Less than 1 s • 02h = Less than 2 s • ... • 0Ah = Less than 10 s • 0B-FFh = Reserved **Power Well:** Core

18.7.6 Capability Parameters (HCCPARAMS)—Offset 10h

The default values for all fields in this register are implementation dependent. This register defines optional capabilities supported by the xHCI. This register is modified and maintained by BIOS.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 10h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 200071E1h

Bits	31:16	15:12	11:9	8	7	6	5	4	3	2	1	0
Value	0010 0000 0000 0000	0111	000	1	1	1	1	0	0	0	0	1
Field	xECP	MaxPSASize	Rsvd1	PAE	NSS	LTC	LHRC	PIND	PPC	CSZ	BNC	AC64

Bit Range	Default & Access	Field Name (ID): Description
31:16	2000h RW/L	**xHCI Extended Capabilities Pointer (xECP):** This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability. For example, using the offset of Base is 1000h and the xECP value of 0068h, we can calculate the following effective address of the first extended capability: 1000h + (0068h ((2) -) 1000h + 01A0h -) 11A0h a. This is not tightly coupled with the USBBASE address register mapping control. **Power Well:** Core
15:12	7h RW/L	**Maximum Primary Stream Array Size (MaxPSASize):** This field identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = 2^(MaxPSASize+1). Valid MaxPSASize values are 0 to 15, where 0 indicates that Streams are not supported. **Power Well:** Core
11:9	0h RW/L	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8	1b RW/L	**Parse All Event Data (PAE):** This flag indicates whether the host controller implementation parses all Event Data TRBs while advancing to the next TD after a Short Packet, or skips all but the first Event Data TRB. A 1 in this bit indicates that all Event Data TRBs are parsed. A 0 in this bit indicates that only the first Event Data TRB is parsed. Refer to the xHCI for USB specification. **Power Well:** Core
7	1b RW/L	**No Secondary SID Support (NSS):** This flag indicates whether the host controller implementation supports Secondary Stream IDs. A 1 in this bit indicates that Secondary Stream ID decoding is not supported. A 0 in this bit indicates that Secondary Stream ID decoding is supported. Refer to the xHCI for USB specification. **Power Well:** Core
6	1b RW/L	**Latency Tolerance Messaging Capability (LTC):** This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A 1 in this bit indicates that LTM is supported. A 0 in this bit indicates that LTM is not supported. Refer to the xHCI for USB specification. **Power Well:** Core
5	1b RW/L	**Light HC Reset Capability (LHRC):** This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A 1 in this bit indicates that Light Host Controller Reset is supported. A 0 in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the *Light Host Controller Reset* (LHCRST) flag in the USBCMD register. Refer to the xHCI for USB specification. **Power Well:** Core
4	0b RW/L	**Port Indicators (PIND):** This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a 1, the port status and control registers include a read/ writeable field for controlling the state of the port indicator. Refer to the xHCI for USB specification for the definition of the *Port Indicator Control* field. **Power Well:** Core
3	0b RO	**Port Power Control (PPC):** This flag indicates whether the host controller implementation includes port power control. A 1 in this bit indicates the ports have port power switches. A 0 in this bit indicates the port does not have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register. See the xHCI for USB specification. **Power Well:** Core
2	0b RW/L	**Context Size (CSZ):** If this bit is set to 1, then the xHC uses 64 byte Context data structures. If this bit is cleared to 0, then the xHC uses 32 byte Context data structures. Note: This flag does *not* apply to Stream Contexts. **Power Well:** Core
1	0b RW/L	**BW Negotiation Capability (BNC):** This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: • 0 = BW Negotiation not implemented • 1 = BW Negotiation implemented Refer to the xHCI for USB specification for more information on Bandwidth Negotiation. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	1b RW/L	**64-bit Addressing Capability (AC64):** This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this flag have the following interpretation: • 0 = 32-bit address memory pointers implemented • 1 = 64-bit address memory pointers implemented If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers. **Power Well:** Core

18.7.7 Doorbell Offset (DBOFF)—Offset 14h

This register defines the offset of the Doorbell Array base address from the Base.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 14h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00003000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:2	Bits 1:0
DBAO	Rsvd1

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000C00h RO	**Doorbell Array Offset (DBAO):** This field defines the offset in Dwords of the Doorbell Array base address from the Base i.e. the base address of the xHCI Capability register address space. **Power Well:** Core
1:0	0h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.8 Runtime Register Space Offset (RTSOFF)—Offset 18h

This register defines the offset of the HCI Runtime Registers from the Base.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 18h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00002000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:5	RTRSO
4:0	Rsvd1

Bit Range	Default & Access	Field Name (ID): Description
31:5	0000100h RO	**Runtime Register Space Offset (RTRSO):** This field defines the 32-byte offset of the xHCI Runtime Registers from the Base, i.e. Runtime Register Base Address = Base + Runtime Register Set Offset. **Power Well:** Core
4:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.9 USB Command (USBCMD)—Offset 80h

The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:12	Rsvd2
11	EU3S
10	EWE
9	CRS
8	CSS
7	LHCRST
6:4	Rsvd1
3	HSEE
2	INTE
1	HCRST
0	RS

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RO	**Rsvd2:** Reserved. **Power Well:** Core
11	0b RW	**Enable U3 MFINDEX Stop (EU3S):** When set to 1, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0 the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, Training, or Powered-off state. Refer to the xHCI for USB specification for more information. **Power Well:** Core
10	0b RW	**Enable Wrap Event (EWE):** When set to 1, the xHC shall generate an MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to 0 no MFINDEX Wrap Events are generated. Refer to the xHCI for USB specification for more information. When this register is exposed by a Virtual Function (VF), the generation of MFINDEX Wrap Events to VFs shall be emulated by the VMM. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
9	0b RW	**Controller Restore State (CRS):** When set to 1, and HCHalted (HCH) = 1, then the xHC shall perform a Restore State operation and restore its internal state. When set to 1 and *Run/Stop* (R/S) = 1 or *HCHalted* (HCH) = 0, or when cleared to 0, no Restore State operation shall be performed. This flag always returns 0 when read. Refer to the *Restore State Status* (RSS) flag in the USBSTS register for information on Restore State completion. Refer to the xHCI for USB specification, for more information. Note that undefined behavior may occur if a Restore State operation is initiated while *Save State Status* (SSS) = 1. When this register is exposed by a Virtual Function (VF), this bit only controls restoring the state of the xHC instance presented by the selected VF. Refer to the xHCI for USB specification for more information. **Power Well:** Core
8	0b RW	**Controller Save State (CSS):** When written by software with 1 and HCHalted (HCH) = 1, then the xHC shall save any internal state that may be restored by asubsequent Restore State operation. When written by software with 1 and HCHalted (HCH) =0, or written with 0, no Save State operation shall be performed. This flag always returns 0 when read. Refer to the Save State Status (SSS) flag in the USBSTS register for information on Save State completion. Refer to the xHCI for USB specification for more information on xHC Save/Restore operation. Note that undefined behavior may occur if a Save State operation is initiated while Restore State Status (RSS) = 1. When this register is exposed by a Virtual Function (VF), this bit only controls saving the state of the xHC instance presented by the selected VF. Refer to the xHCI for USB specification for more information. **Power Well:** Core
7	0b RW	**Light Host Controller Reset (LHCRST):** Optional normative. If the *Light HC Reset Capability* (LHRC) bit in the HCCPARAMS register is 1, then this flag allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0 indicates the *Light Host Controller Reset* has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a 1 indicates the *Light Host Controller Reset* has not yet completed. If not implemented, a read of this flag shall always return a 0. All registers in the Aux Power well shall maintain the values that had been asserted prior to the Light Host Controller Reset. (Refer to the xHCI for USB specification for more information.) When this register is exposed by a Virtual Function (VF), this bit only generates a Light Reset to the xHC instance presented by the selected VF, e.g. disabling the VF's device slots and setting the associated VF Run bit to Stopped. Refer to the xHCI for USB specification for more information. **Power Well:** Core
6:4	0h RO	**Rsvd1:** Reserved. **Power Well:** Core
3	0b RW	**Host System Error Enable (HSEE):** When this bit is a 1, and the HSE bit in the USBSTS register is a 1, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit. Refer to the xHCI for USB specification for more information. When this register is exposed by a Virtual Function (VF), the effect of the assertion of this bit on the Physical Function (PF0) is determined by the VMM. Refer to the xHCI for USB specification for more information. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**Interrupter Enable (INTE):** This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a 1, then Interrupter host system interrupt generation is allowed, i.e. the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSIX, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism. When this register is exposed by a Virtual Function (VF), this bit only enables the set of Interrupters assigned to the selected VF. **Power Well:** Core
1	0b RW	**Host Controller Reset (HCRST):** This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset. When software writes a 1 to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on the USB is immediately terminated. A USB reset shall not be driven on USB2 downstream ports, however a Hot or Warm Reseta shall be initiated on USB3 Root Hub downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Software shall reinitialize the host controller, as described in the xHCI for USB specification, in order to return the host controller to an operational state. This bit is cleared to 0 by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this bit and shall not write any xHC Operational or Runtime registers until while HCRST is 1. Note, the completion of the xHC reset process is not gated by the Root Hub port reset process. Software shall not set this bit to 1 when the HCHalted (HCH) bit in the USBSTS register is a 0. Attempting to reset an actively running host controller may result in undefined behavior. When this register is exposed by a Virtual Function (VF), this bit only resets the xHC instance presented by the selected VF. Refer to the xHCI for USB specification for more information. **Power Well:** Core
0	0b RW	**Run/Stop (RS):** • 1 = Run • 0 = Stop When set to a 1, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a 1. When this bit is cleared to 0, the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. Refer to section 5.4.1.1 for more information on how R/S shall be managed. The xHC shall halt within 16 ms. after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a 1 to this flag unless the xHC is in the Halted state (i.e. HCH in the USBSTS register is 1). Doing so may yield undefined results. Writing a 0 to this flag when the xHC is in the Running state (i.e. HCH = 0) and any Event Rings are in the Event Ring Full state (refer to section 4.9.4) may yield undefined resultsresult in lost events. When this register is exposed by a Virtual Function (VF), this bit only controls the run state of the xHC instance presented by the selected VF. **Power Well:** Core

18.7.10 USB Status (USBSTS)—Offset 84h

This register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to '0' in this register by writing a '1' to it (RW1C). Refer to specification *eXtensible Host Controller Interface for Universal Serial Bus (xHCI)* for additional information concerning USB interrupt conditions.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 84h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000001h

31–13	12	11	10	9	8	7–5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0 0 0	0	0	0	0	1
Rsvd3	HCE	CNR	SRE	RSS	SSS	Rsvd2	PCD	EINT	HSE	Rsvd1	HCH

Bit Range	Default & Access	Field Name (ID): Description
31:13	00000h RO	**Rsvd3:** Reserved. **Power Well:** Core
12	0b RO	**Host Controller Error (HCE):** This bit is not preset in HC, this is deviation from XHCI 1.0 spec. **Power Well:** Core
11	0b RO	**Controller Not Ready (CNR):** This is deviation from XHCI 1.0 spec. **Power Well:** Core
10	0b RW/C	**Save/Restore Error (SRE):** If an error occurs during a Save or Restore operation, this bit shall be set to 1. This bit shall be cleared to 0 when a Save or Restore operation is initiated or when written with 1. Refer to the xHCI for USB specification for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Save/Restore completion status for the selected VF. Refer to the xHCI for USB specification for more information. **Power Well:** Core
9	0b RO	**Restore State Status (RSS):** When the Controller Restore State (CRS) flag in the USBCMD register is written with 1 this bit shall be set to 1 and remain 1 while the xHC restores its internal state. When the Restore State operation is complete, this bit shall be cleared to 0. Refer to the xHCI for USB specification for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the restoring the state for the selected VF. Refer to the xHCI for USB specification for more information. **Power Well:** Core
8	0b RO	**Save State Status (SSS):** When the *Controller Save State* (CSS) flag in the USBCMD register is written with 1, this bit shall be set to 1 and remain 1 while the xHC saves its internal state. When the Save State operation is complete, this bit shall be cleared to 0. Refer to the xHCI for USB specification for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the saving the state for the selected VF. Refer to the xHCI for USB specification for more information. **Power Well:** Core
7:5	0h RO	**Rsvd2:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW/C	**Port Change Detect (PCD):** The xHC sets this bit to a 1 when any port has a change bit transition from a 0 to a 1. This bit is allowed to be maintained in the Aux Power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits. Refer to the xHCI for USB specification for more information. This bit provides system software an efficient means of determining if there has been Root Hub port activity. Refer to the xHCI for USB specification for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Root Hub Ports associated with the Device Slots assigned to the selected VF. Refer to the xHCI for USB specification for more information. **Power Well:** Core
3	0b RW/C	**Event Interrupt (EINT):** The xHC sets this bit to 1 when the *Interrupt Pending* (IP) bit of any Interrupter transitions from 0 to 1. Refer to the xHCI for USB specification for usage information. Software that uses *EINT* shall clear it prior to clearing any IP flags. A race condition may occur if software clears the *IP* flags, then clears the *EINT* flag, and between the operations another *IP* 0 to '1' transition occurs. In this case, the new IP transition shall be lost. When this register is exposed by a Virtual Function (VF), this bit is the logical 'OR' of the IP bits for the Interrupters assigned to the selected VF. And it shall be cleared to 0 when all associated interrupter IP bits are cleared, i.e. all the VFs Interrupter Event Ring(s) are empty. Refer to the xHCI for USB specification for more information. **Power Well:** Core
2	0b RW/C	**Host System Error (HSE):** The xHC sets this bit to 1 when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. (In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort.) When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USBCMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USBCMD register is a 1, the xHC shall also assert out-of-band error signaling to the host. Refer to the xHCI for USB specification for more information. When this register is exposed by a Virtual Function (VF), the assertion of this bit affects all VFs and reflects the Host System Error state of the Physical Function (PF0). Refer to the xHCI for USB specification for more information. **Power Well:** Core
1	0b RO	**Rsvd1:** Reserved. **Power Well:** Core
0	1b RO	**HCHalted (HCH):** This bit is a 0 whenever the *Run/Stop* (R/S) bit is a 1. The xHC sets this bit to 1 after it has stopped executing as a result of the *Run/Stop* (R/S) bit being cleared to 0, either by software or by the xHC hardware (e.g. internal error). If this bit is '1', then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC, and any received Transaction Packet shall be dropped. When this register is exposed by a Virtual Function (VF), this bit only reflects the Halted state of the xHC instance presented by the selected VF. Refer to the xHCI for USB specification for more information. **Power Well:** Core

18.7.11 Page Size (PAGESIZE)—Offset 88h

The default value for this register is implementation dependent.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 88h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Rsvd1 (bits 31:16), PAGESIZE (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0001h RO	**Page Size (PAGESIZE):** This field defines the page size supported by the xHC implementation. This xHC supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the xHC supports 4k byte page sizes. For a Virtual Function, this register reflects the page size selected in the *System Page Size* field of the SR-IOV Extended Capability structure. For the Physical Function 0, this register reflects the implementation dependent default xHC page size. Various xHC resources reference PAGESIZE to describe their minimum alignment requirements. The maximum possible page size is 128M. **Power Well:** Core

18.7.12 Device Notification Control (DNCTRL)—Offset 94h

This register is used by software to enable or disable the reporting of the reception of specific USB Device Notification Transaction Packets. A *Notification Enable* (Nx, where x = 0 to 15) flag is defined for each of the 16 possible device notification types. If a flag is set for a specific notification type, a Device Notification Event shall be generated when the respective notification packet is received. After reset, all notifications are disabled. Refer to specification *eXtensible Host Controller Interface for Universal Serial Bus (xHCI)*. This register shall be written as a Dword. Byte writes produce undefined results.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 94h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd1 (bits 31:16), N0_N15 (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Notification Enable (N0_N15):** When a Notification Enable bit is set, a Device Notification Event shall be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with a Notification Type field set to '1' (FUNCTIONAL_WAKE), etc. **Power Well:** Core

18.7.13 Command Ring Low (CRCR_LO)—Offset 98h

The Command Ring Control Register provides Command Ring control and status capabilities, and identifies the address and Cycle bit state of the Command Ring Dequeue Pointer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 98h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CRP																										Rsvd1		CRR	CA	CS	RCS

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Command Ring Pointer (CRP):** This field defines low order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when *Command Ring Running* (CCR) = '1'. If the CRCR is written while the Command Ring is stopped (CCR = '0'), the value of this field shall be used to fetch the first Command TRB the next time the *Host Controller Doorbell* register is written with the DB Reason field set to Host Controller Command. If the CRCR is *not* written while the Command Ring is stopped (CRR = '0') then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns '0'. **Power Well:** Core
5:4	0h RO	**Rsvd1:** Reserved. **Power Well:** Core
3	0b RO	**Command Ring Running (CRR):** This flag is set to '1' if the *Run/Stop* (R/S) bit is '1' and the *Host Controller Doorbell* register is written with the *DB Reason* field set to *Host Controller Command*. It is cleared to '0' when the Command Ring is 'stopped' after writing a '1' to the *Command Stop* (CS) or *Command Abort*)CA) flags, or if the *R/S* bit is cleared to '0' **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW/S	**Command Abort (CA):** Writing a '1' to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. Refer to the xHCI for USB specification for more information on aborting a command. The next write to the *Host Controller Doorbell* with *DB Reason* field set to *Host Controller Command* shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if *Command Ring Running* (CCR) = '0'. Reading this bit always returns '0'. **Power Well:** Core
1	0b RW/S	**Command Stop (CS):** Writing a '1' to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a *Command Completion Event* with the *Completion Code* set to *Command Ring Stopped* and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. Refer to the xHCI for USB specification for more information on stopping a command. The next write to the *Host Controller Doorbell* with *DB Reason* field set to *Host Controller Command* shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if *Command Ring Running* (CCR) = '0'. Reading this bit shall always return '0'. **Power Well:** Core
0	0b RW	**Ring Cycle State (RCS):** This bit identifies the value of the xHC *Consumer Cycle State* (CCS) flag for the TRB referenced by the *Command Ring Pointer*. Refer to the xHCI for USB specification for more information. Writes to this flag are ignored if *Command Ring Running* is '1'. If the CRCR is written while the Command Ring is stopped (CCR = '0'), then the value of this flag shall be used to fetch the first Command TRB the next time the *Host Controller Doorbell* register is written with the *DB Reason* field set to *Host Controller Command*. If the CRCR is *not* written while the Command Ring is stopped (CRR = '0'), then the Command Ring shall begin fetching Command TRBs using the current value of the Internal Command Ring CCS flag. Reading this flag always returns '0'. **Power Well:** Core

18.7.14 Command Ring High (CRCR_HI)—Offset 9Ch

The Command Ring Control Register provides Command Ring control and status capabilities, and identifies the address and Cycle bit state of the Command Ring Dequeue Pointer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 9Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRP

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Command Ring Pointer (CRP):** This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when *Command Ring Running* (CCR) = '1'. If the CRCR is written while the Command Ring is stopped (CCR = '0'), the value of this field shall be used to fetch the first Command TRB the next time the *Host Controller Doorbell* register is written with the DB Reason field set to Host Controller Command. If the CRCR is *not* written while the Command Ring is stopped (CRR = '0') then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns '0'. **Power Well:** Core

18.7.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h

The Device Context Base Address Array Pointer Register identifies the base address of the Device Context Base Address Array. The memory structure referenced by this physical memory pointer is assumed to be physically contiguous and 64-byte aligned.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + B0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DCBAAP																										Rsvd1					

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Device Context Base Address Array Pointer (DCBAAP):** This field defines low order bits of the 64-bit base address of the Device Context Pointer Array, which is a table of address pointers that reference Device Context structures for the devices attached to the host. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h

The Device Context Base Address Array Pointer Register identifies the base address of the Device Context Base Address Array. The memory structure referenced by this physical memory pointer is assumed to be physically contiguous and 64-byte aligned.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + B4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DCBAAP

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Device Context Base Address Array Pointer (DCBAAP):** This field defines high order bits of the 64-bit base address of the Device Context Pointer Array, which is a table of address pointers that reference Device Context structures for the devices attached to the host. **Power Well:** Core

18.7.17 Configure (CONFIG)—Offset B8h

This register defines runtime xHC configuration parameters.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + B8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd1 | MaxSlotsEn

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**Max Device Slots Enabled (MaxSlotsEn):** This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously, e.g. a value of 16 specifies that Device Slots 1 to 16 are active. A value of '0' disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references. This field shall not be modified by software if the xHC is running (Run/Stop (R/S) = '1'). **Power Well:** Core

18.7.18 Port 1 Status and Control USB3 (PORTSC1USB2)—Offset 480h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 480h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000002A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
WPR	DR	Rsvd2		WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS	PIC		Port_Speed				PP	PLS				PR	OCA	Rsvd1	PED	CCS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0b RO	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0h RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0b RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky. **Power Well:** SUS
9	1b RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0b RW/S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0b RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

18.7.19 Port 1 Power Management Status and Control USB2 (PORTPMSC1USB2)—Offset 484h

This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a *Host Controller Reset* (HCRST). The USB2 Port Power Management Status and Control register provides the USB2 LPM parameters necessary for the xHC to generate a LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 484h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PTC				Rsvd1											HLE	L1DS								HIRD				RWE	L1S		

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	000h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0b RO	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky. System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of 0 indicates no device is present. The xHC uses this field to lookup information necessary to generate the LPM Token packet. **Power Well:** SUS
7:4	0h RW	**Best Effort Service Latency (HIRD):** Note: This register is sticky. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. For more information about *BESL* value encoding, refer to the xHCI for USB specification. Note that the *BESL* field is used by both software and hardware controlled LPM. Refer to the xHCI for USB specification for more information on *BESL* use and how *DBESL* may be used to establish an initial value for BESL. **Power Well:** SUS
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky. System software sets this flag to enable or disable the device for remote wake from L1. The value of this flag shall temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky. This field is used by software to determine whether an L1- based suspend request (LPM transaction) was successful, specifically: • 0 = Invalid - This field shall be ignored by software. • 1 = Success - Port successfully transitioned to L1 (ACK) • 2 = Not Yet - Device is unable to enter L1 at this time (NYET) • 3 = Not Supported - Device does not support L1 transitions (STALL) • 4 = Timeout/Error - Device failed to respond to the LPM Transaction or an error occurred • 5-7 = Reserved The value of this field is only valid when the port resides in the L0 or L1 state (*PLS* = 0 or 2). Refer to the xHCI for USB specification for more information. **Power Well:** SUS

18.7.20 Port X Hardware LPM Control Register (PORTHLPM1)—Offset 48Ch

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh and 50Ch. This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The field definitions depend on the protocol supported. For USB3, this register is reserved and shall be treated by software as RsvdP. For USB2, the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 48Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:14	Bits 13:10	Bits 9:2	Bits 1:0
RSVD	HIRDD	L1TO	HIRDM

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume upon exit from L1. The HIRDD value is is encoded as follows: • 0h = 50 us (default) • 1h = 125 us • 2h = 200 us • ... • Fh = 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
9:2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. The following are permissible values: • 0 = Initiate L1 using HIRD only time out (default) • 1 = Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD • 2,3 = Reserved Note: This register is sticky. **Power Well:** SUS

18.7.21 Port 2 Status and Control USB3 (PORTSC2USB2)—Offset 490h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 490h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000002A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
WPR	DR	Rsvd2		WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS	PIC		Port_Speed				PP	PLS				PR	OCA	Rsvd1	PED	CCS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0b RO	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0h RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24	0b RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky. **Power Well:** SUS
9	1b RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0b RW/S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0b RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

18.7.22 Port 2 Power Management Status and Control USB2 (PORTPMSC2USB2)—Offset 494h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 494h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

Bits	31:28	27:17	16	15:8	7:4	3	2:0
Default	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0	0 0 0 0	0	0 0 0
Field	PTC	Rsvd1	HLE	L1DS	HIRD	RWE	L1S

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	000h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0b RO	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky. **Power Well:** SUS
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

18.7.23 Port X Hardware LPM Control Register (PORTHLPM2)—Offset 49Ch

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh and 50Ch. This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The field definitions depend on the protocol supported. For USB3, this register is reserved and shall be treated by software as RsvdP. For USB2, the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 49Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																		HIRDD				L1TO								HIRDM	

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume upon exit from L1. The HIRDD value is is encoded as follows: • 0h = 50 us (default) • 1h = 125 us • 2h = 200 us • ... • Fh = 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. The following are permissible values: • 0 = Initiate L1 using HIRD only time out (default) • 1 = Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD • 2,3 = Reserved Note: This register is sticky. **Power Well:** SUS

18.7.24 Port 3 Status and Control USB3 (PORTSC3USB2)—Offset 4A0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4A0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000002A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
WPR	DR	Rsvd2		WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS	PIC		Port_Speed				PP	PLS				PR	OCA	Rsvd1	PED	CCS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0b RO	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0h RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0b RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky. **Power Well:** SUS
9	1b RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0b RW/S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0b RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

18.7.25 Port 3 Power Management Status and Control USB2 (PORTPMSC3USB2)—Offset 4A4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4A4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTC	Rsvd1	HLE	L1DS	HIRD	RWE	L1S

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	000h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0b RO	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky. **Power Well:** SUS
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

18.7.26 Port X Hardware LPM Control Register (PORTHLPM3)—Offset 4ACh

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh and 50Ch. This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The field definitions depend on the protocol supported. For USB3, this register is reserved and shall be treated by software as RsvdP. For USB2, the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4ACh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD	HIRDD	L1TO	HIRDM

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume upon exit from L1. The HIRDD value is is encoded as follows: • 0h = 50 us (default) • 1h = 125 us • 2h = 200 us • ... • Fh = 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. The following are permissible values: • 0 = Initiate L1 using HIRD only time out (default) • 1 = Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD • 2,3 = Reserved Note: This register is sticky. **Power Well:** SUS

18.7.27 Port 4 Status and Control USB3 (PORTSC4USB2)—Offset 4B0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4B0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000002A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
WPR	DR	Rsvd2		WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS	PIC		Port_Speed				PP	PLS				PR	OCA	Rsvd1	PED	CCS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30	0b RO	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0h RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0b RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
9	1b RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0b RW/S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0b RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

18.7.28 Port 4 Power Management Status and Control USB2 (PORTPMSC4USB2)—Offset 4B4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4B4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PTC | Rsvd1 | HLE | L1DS | HIRD | RWE | L1S

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	000h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0b RO	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky. **Power Well:** SUS
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

18.7.29 Port X Hardware LPM Control Register (PORTHLPM4)—Offset 4BCh

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh and 50Ch. This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The field definitions depend on the protocol supported. For USB3, this register is reserved and shall be treated by software as RsvdP. For USB2, the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4BCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																		HIRDD				L1TO								HIRDM	

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume upon exit from L1. The HIRDD value is is encoded as follows: • 0h = 50 us (default) • 1h = 125 us • 2h = 200 us • ... • Fh = 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. The following are permissible values: • 0 = Initiate L1 using HIRD only time out (default) • 1 = Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD • 2,3 = Reserved Note: This register is sticky. **Power Well:** SUS

18.7.30 Port 8 Status and Control USB2 (PORTSC5USB2)—Offset 4C0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4C0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000002A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
WPR	DR	Rsvd2		WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS	PIC		Port_Speed				PP	PLS				PR	OCA	Rsvd1	PED	CCS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0b RO	**Device Removable (DR):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:28	0h RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0b RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky. **Power Well:** SUS
9	1b RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0b RW/S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0b RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

18.7.31 Port 5 Power Management Status and Control USB2 (PORTPMSC5USB2)—Offset 4C4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4C4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31:28	27:17	16	15:8	7:4	3	2:0
0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0	0 0 0 0	0	0 0 0
PTC	Rsvd1	HLE	L1DS	HIRD	RWE	L1S

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	000h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0b RO	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

18.7.32 Port X Hardware LPM Control Register (PORTHLPM5)—Offset 4CCh

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh and 50Ch. This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The field definitions depend on the protocol supported. For USB3, this register is reserved and shall be treated by software as RsvdP. For USB2, the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4CCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																		HIRDD				L1TO								HIRDM	

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume upon exit from L1. The HIRDD value is is encoded as follows: • 0h = 50 us (default) • 1h = 125 us • 2h = 200 us • ... • Fh = 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
9:2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. The following are permissible values: • 0 = Initiate L1 using HIRD only time out (default) • 1 = Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD • 2,3 = Reserved Note: This register is sticky. **Power Well:** SUS

18.7.33 Port 6 Status and Control USB2 (PORTSC6USB2)—Offset 4D0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4D0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000002A0h

Bits	Default	Field
31	0	WPR
30	0	DR
29:28	0 0	Rsvd2
27	0	WOE
26	0	WDE
25	0	WCE
24	0	CAS
23	0	CEC
22	0	PLC
21	0	PRC
20	0	OCC
19	0	WRC
18	0	PEC
17	0	CSC
16	0	LWS
15:14	0 0	PIC
13:10	0 0 0 0	Port_Speed
9	1	PP
8:5	0 1 0 1	PLS
4	0	PR
3	0	OCA
2	0	Rsvd1
1	0	PED
0	0	CCS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0b RO	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0h RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24	0b RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky. **Power Well:** SUS
9	1b RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0b RW/S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0b RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

18.7.34 Port 6 Power Management Status and Control USB2 (PORTPMSC6USB2)—Offset 4D4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4D4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PTC				Rsvd1											HLE	L1DS								HIRD				RWE	L1S		

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	000h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0b RO	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky. **Power Well:** SUS
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

18.7.35 Port X Hardware LPM Control Register (PORTHLPM6)—Offset 4DCh

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh and 50Ch. This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The field definitions depend on the protocol supported. For USB3, this register is reserved and shall be treated by software as RsvdP. For USB2, the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4DCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																		HIRDD				L1TO								HIRDM	

Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume upon exit from L1. The HIRDD value is is encoded as follows: • 0h = 50 us (default) • 1h = 125 us • 2h = 200 us • ... • Fh = 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. The following are permissible values: • 0 = Initiate L1 using HIRD only time out (default) • 1 = Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD • 2,3 = Reserved Note: This register is sticky. **Power Well:** SUS

18.7.36 Port 1 Status and Control USB3 (PORTSC1USB3)—Offset 4E0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4E0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000002A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
WPR	DR	Rsvd2		WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS	PIC		Port_Speed				PP	PLS				PR	OCA	Rsvd1	PED	CCS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0b RO	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0h RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0b RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky. **Power Well:** SUS
9	1b RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0b RW/S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0b RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

18.7.37 Port 1 Power Management Status and Control USB3 (PORTPMSC1USB3)—Offset 4E4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4E4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

PTC	Rsvd1	HLE	L1DS	HIRD	RWE	L1S

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	000h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0b RO	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky. **Power Well:** SUS
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

18.7.38 Port 1 Link Info (PORTLI1)—Offset 4E8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4E8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Rsvd1	LEC

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

18.7.39 Microframe Index (MFINDEX)—Offset 2000h

This register is used by the system software to determine the current periodic frame. The register value is incremented every 125 microseconds (once each microframe). This register is only incremented while *Run/Stop* = '1'. The value of this register affects the SOF value generated by USB2 Bus Instances.

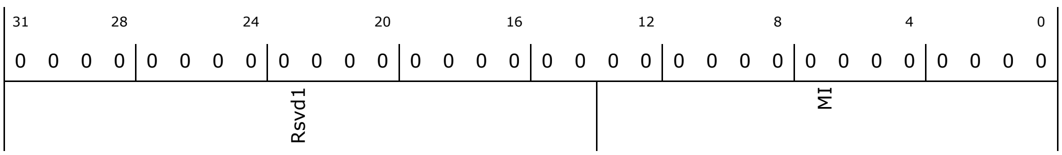
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2000h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	00000h RO	**Rsvd1:** Reserved. **Power Well:** Core
13:0	0000h RO	**Microframe Index (MI):** Reserved. **Power Well:** Core

18.7.40 Interrupter 1 Management (IMAN1)—Offset 2020h

The Interrupter Management registers allow system software to enable, disable, detect and force xHC interrupts. There are 8 IMAN registers. x = 1, 2, ... 8.

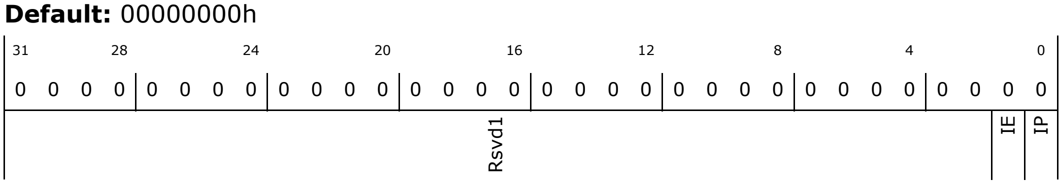
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2020h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0b RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

18.7.41 Interrupter 1 Moderation (IMOD1)—Offset 2024h

The Interrupter Moderation Register controls the 'interrupt moderation' feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC. There are 8 IMOD registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2024h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000FA0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0
IMODC																IMODI															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0' and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags both equal '1', and EHB = '0'. This counter may be written directly by software at any time to alter the interrupt rate. **Power Well:** Core
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Default = '4000' (~1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic, and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. **Power Well:** Core

18.7.42 Event Ring Segment Table Size 1 (ERSTSZ1)—Offset 2028h

The *Event Ring Segment Table Size Register* defines the number of segments supported by the Event Ring Segment Table. There are 8 ERSTSZ registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2028h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Rsvd1 (bits 31:16), ERSTS (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (see specification xHCI for USB). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. **Power Well:** Core

18.7.43 Event Ring Segment Table Base Address Low 1 (ERSTBA_LO1)—Offset 2030h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2030h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: ERSTBA_LO (bits 31:6), Rsvd1 (bits 5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** This field defines the low order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.44 Event Ring Segment Table Base Address High 1 (ERSTBA_HI1)—Offset 2034h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2034h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERSTBA_HI

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core

18.7.45 Event Ring Dequeue Pointer Low 1 (ERDP_LO1)—Offset 2038h

There are 8 ERDP_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2038h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ERDP																												EHB	DESI		

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core
3	0b RW/C	**Event Handler Busy (EHB):** This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to the xHCI for USB specification for more information. **Power Well:** Core
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.46 Event Ring Dequeue Pointer High 1 (ERDP_HI1)—Offset 203Ch

There are 8 ERDP_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 203Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ERDP																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core

18.7.47 Interrupter 2 Management (IMAN2)—Offset 2040h

The Interrupter Management registers allow system software to enable, disable, detect and force xHC interrupts. There are 8 IMAN registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2040h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																														IE	IP

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0b RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

18.7.48 Interrupter 2 Moderation (IMOD2)—Offset 2044h

The Interrupter Moderation Register controls the 'interrupt moderation' feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC. There are 8 IMOD registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2044h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000FA0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0
IMODC																IMODI															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Default undefined. Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0' and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be written directly by software at any time to alter the interrupt rate. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Default = '4000' (~1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic, and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. **Power Well:** Core

18.7.49 Event Ring Segment Table Size 2 (ERSTSZ2)—Offset 2048h

The *Event Ring Segment Table Size Register* defines the number of segments supported by the Event Ring Segment Table. There are 8 ERSTSZ registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2048h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																ERSTS															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (see specification xHCI for USB). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. **Power Well:** Core

18.7.50 Event Ring Segment Table Base Address Low 2 (ERSTBA_LO2)—Offset 2050h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2050h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: ERSTBA_LO (bits 31:6), Rsvd1 (bits 5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** This field defines the low order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.51 Event Ring Segment Table Base Address High 2 (ERSTBA_HI2)—Offset 2054h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2054h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: ERSTBA_HI (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core

18.7.52 Event Ring Dequeue Pointer Low 2 (ERDP_LO2)—Offset 2058h

There are 8 ERDP_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2058h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP | EHB | DESI

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core
3	0b RW/C	**Event Handler Busy (EHB):** This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to the xHCI for USB specification for more information. **Power Well:** Core
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.53 Event Ring Dequeue Pointer High 2 (ERDP_HI2)—Offset 205Ch

There are 8 ERDP_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 205Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core

18.7.54 Interrupter 3 Management (IMAN3)—Offset 2060h

The Interrupter Management registers allow system software to enable, disable, detect and force xHC interrupts. There are 8 IMAN registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2060h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd1 IE IP

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0b RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

18.7.55 Interrupter 3 Moderation (IMOD3)—Offset 2064h

The Interrupter Moderation Register controls the 'interrupt moderation' feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC. There are 8 IMOD registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2064h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000FA0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0

Bits 31:16: IMODC; bits 15:0: IMODI

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0' and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be written directly by software at any time to alter the interrupt rate. **Power Well:** Core
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Default = '4000' (~1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic, and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. **Power Well:** Core

18.7.56 Event Ring Segment Table Size 3 (ERSTSZ3)—Offset 2068h

The *Event Ring Segment Table Size Register* defines the number of segments supported by the Event Ring Segment Table. There are 8 ERSTSZ registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2068h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: Rsvd1; bits 15:0: ERSTS

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (see specification xHCI for USB). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. **Power Well:** Core

18.7.57 Event Ring Segment Table Base Address Low 3 (ERSTBA_LO3)—Offset 2070h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2070h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERSTBA_LO (bits 31:6), Rsvd1 (bits 5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** This field defines the low order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.58 Event Ring Segment Table Base Address High 3 (ERSTBA_HI3)—Offset 2074h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2074h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERSTBA_HI (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core

18.7.59 Event Ring Dequeue Pointer Low 3 (ERDP_LO3)—Offset 2078h

There are 8 ERDP_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2078h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP (bits 31:4), EHB (bit 3), DESI (bits 2:0)

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core
3	0b RW/C	**Event Handler Busy (EHB):** This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to the xHCI for USB specification for more information. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.60 Event Ring Dequeue Pointer High 3 (ERDP_HI3)—Offset 207Ch

There are 8 ERDP_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 207Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core

18.7.61 Interrupter 4 Management (IMAN4)—Offset 2080h

The Interrupter Management registers allow system software to enable, disable, detect and force xHC interrupts. There are 8 IMAN registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2080h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd1 (bits 31:2), IE (bit 1), IP (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0b RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

18.7.62 Interrupter 4 Moderation (IMOD4)—Offset 2084h

The Interrupter Moderation Register controls the 'interrupt moderation' feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC. There are 8 IMOD registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2084h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000FA0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0
IMODC																IMODI															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0' and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be written directly by software at any time to alter the interrupt rate. **Power Well:** Core
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Default = '4000' (~1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic, and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. **Power Well:** Core

18.7.63 Event Ring Segment Table Size 4 (ERSTSZ4)—Offset 2088h

The *Event Ring Segment Table Size Register* defines the number of segments supported by the Event Ring Segment Table. There are 8 ERSTSZ registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2088h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31:16	15:0
0000000000000000	0000000000000000
Rsvd1	ERSTS

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (see specification xHCI for USB). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. **Power Well:** Core

18.7.64 Event Ring Segment Table Base Address Low 4 (ERSTBA_LO4)—Offset 2090h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2090h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31:6	5:0
00000000000000000000000000	000000
ERSTBA_LO	Rsvd1

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** This field defines the low order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.65 Event Ring Segment Table Base Address High 4 (ERSTBA_HI4)—Offset 2094h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2094h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERSTBA_HI

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core

18.7.66 Event Ring Dequeue Pointer Low 4 (ERDP_LO4)—Offset 2098h

There are 8 ERDP_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2098h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

ERDP (31:4), EHB (3), DESI (2:0)

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core
3	0b RW/C	**Event Handler Busy (EHB):** This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to the xHCI for USB specification for more information. **Power Well:** Core
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.67 Event Ring Dequeue Pointer High 4 (ERDP_HI4)—Offset 209Ch

There are 8 ERDP_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 209Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

ERDP (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core

18.7.68 Interrupter 5 Management (IMAN5)—Offset 20A0h

The Interrupter Management registers allow system software to enable, disable, detect and force xHC interrupts. There are 8 IMAN registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20A0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Rsvd1 (31:2), IE (1), IP (0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0b RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

18.7.69 Interrupter 5 Moderation (IMOD5)—Offset 20A4h

The Interrupter Moderation Register controls the 'interrupt moderation' feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC. There are 8 IMOD registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20A4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000FA0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0

Fields: IMODC (31:16), IMODI (15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0' and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be written directly by software at any time to alter the interrupt rate. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Default = '4000' (~1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic, and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. **Power Well:** Core

18.7.70 Event Ring Segment Table Size 5 (ERSTSZ5)—Offset 20A8h

The *Event Ring Segment Table Size Register* defines the number of segments supported by the Event Ring Segment Table. There are 8 ERSTSZ registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20A8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																ERSTS															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (see specification xHCI for USB). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. **Power Well:** Core

18.7.71 Event Ring Segment Table Base Address Low 5 (ERSTBA_LO5)—Offset 20B0h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20B0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ERSTBA_LO (31:6)																										Rsvd1 (5:0)					

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** This field defines the low order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.72 Event Ring Segment Table Base Address High 5 (ERSTBA_HI5)—Offset 20B4h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_HIx registers, with x = 1, 2, … 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20B4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ERSTBA_HI (31:0)																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core

18.7.73 Event Ring Dequeue Pointer Low 5 (ERDP_LO5)—Offset 20B8h

There are 8 ERDP_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20B8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ERDP																												EHB	DESI		

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core
3	0b RW/C	**Event Handler Busy (EHB):** This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to the xHCI for USB specification for more information. **Power Well:** Core
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.74 Event Ring Dequeue Pointer High 5 (ERDP_HI5)—Offset 20BCh

There are 8 ERDP_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20BCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core

18.7.75 Interrupter 6 Management (IMAN6)—Offset 20C0h

The Interrupter Management registers allow system software to enable, disable, detect and force xHC interrupts. There are 8 IMAN registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20C0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd1 | IE | IP

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0b RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

18.7.76 Interrupter 6 Moderation (IMOD6)—Offset 20C4h

The Interrupter Moderation Register controls the 'interrupt moderation' feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC. There are 8 IMOD registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20C4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000FA0h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 0 1 0	0 0 0 0	

Bits 31:16	Bits 15:0
IMODC	IMODI

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0' and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be written directly by software at any time to alter the interrupt rate. **Power Well:** Core
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Default = '4000' (~1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic, and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. **Power Well:** Core

18.7.77 Event Ring Segment Table Size 6 (ERSTSZ6)—Offset 20C8h

The *Event Ring Segment Table Size Register* defines the number of segments supported by the Event Ring Segment Table. There are 8 ERSTSZ registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20C8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:16	Bits 15:0
Rsvd1	ERSTS

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (see xHCI for USB specification). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. **Power Well:** Core

18.7.78 Event Ring Segment Table Base Address Low 6 (ERSTBA_LO6)—Offset 20D0h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20D0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bits 5:0
ERSTBA_LO	Rsvd1

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** This field defines the low order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.79 Event Ring Segment Table Base Address High 6 (ERSTBA_HI6)—Offset 20D4h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20D4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERSTBA_HI

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core

18.7.80 Event Ring Dequeue Pointer Low 6 (ERDP_LO6)—Offset 20D8h

There are 8 ERDP_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20D8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP | EHB | DESI

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core
3	0b RW/C	**Event Handler Busy (EHB):** This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to the xHCI for USB specification for more information. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.81 Event Ring Dequeue Pointer High 6 (ERDP_HI6)—Offset 20DCh

There are 8 ERDP_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20DCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core

18.7.82 Interrupter 7 Management (IMAN7)—Offset 20E0h

The Interrupter Management registers allow system software to enable, disable, detect and force xHC interrupts. There are 8 IMAN registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20E0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd1 | IE | IP

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0b RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

18.7.83 Interrupter 7 Moderation (IMOD7)—Offset 20E4h

The Interrupter Moderation Register controls the 'interrupt moderation' feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC. There are 8 IMOD registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20E4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000FA0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0
IMODC																IMODI															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0' and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be written directly by software at any time to alter the interrupt rate. **Power Well:** Core
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Default = '4000' (~1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic, and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. **Power Well:** Core

18.7.84 Event Ring Segment Table Size 7 (ERSTSZ7)—Offset 20E8h

The *Event Ring Segment Table Size Register* defines the number of segments supported by the Event Ring Segment Table. There are 8 ERSTSZ registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20E8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																ERSTS															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (see xHCI for USB specification). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. **Power Well:** Core

18.7.85 Event Ring Segment Table Base Address Low 7 (ERSTBA_LO7)—Offset 20F0h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20F0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ERSTBA_LO																										Rsvd1					

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** This field defines the low order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.86 Event Ring Segment Table Base Address High 7 (ERSTBA_HI7)—Offset 20F4h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_HIx registers, with x = 1, 2, … 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20F4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERSTBA_HI

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core

18.7.87 Event Ring Dequeue Pointer Low 7 (ERDP_LO7)—Offset 20F8h

There are 8 ERDP_LOx registers, with x = 1, 2, … 8.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20F8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: ERDP (31:4), EHB (3), DESI (2:0)

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core
3	0b RW/C	**Event Handler Busy (EHB):** This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to the xHCI for USB specification for more information. **Power Well:** Core
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.88 Event Ring Dequeue Pointer High 7 (ERDP_HI7)—Offset 20FCh

There are 8 ERDP_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20FCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: ERDP (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core

18.7.89 Interrupter 8 Management (IMAN8)—Offset 2100h

The Interrupter Management registers allow system software to enable, disable, detect and force xHC interrupts. There are 8 IMAN registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2100h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																														IE	IP

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0b RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0b RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

18.7.90 Interrupter 8 Moderation (IMOD8)—Offset 2104h

The Interrupter Moderation Register controls the 'interrupt moderation' feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC. There are 8 IMOD registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2104h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000FA0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0
IMODC																IMODI															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0' and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be written directly by software at any time to alter the interrupt rate. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Default = '4000' (~1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic, and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. **Power Well:** Core

18.7.91 Event Ring Segment Table Size 8 (ERSTSZ8)—Offset 2108h

The *Event Ring Segment Table Size Register* defines the number of segments supported by the Event Ring Segment Table. There are 8 ERSTSZ registers. x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2108h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																ERSTS															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (see specification xHCI for USB). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. **Power Well:** Core

18.7.92 Event Ring Segment Table Base Address Low 8 (ERSTBA_LO8)—Offset 2110h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2110h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: ERSTBA_LO (bits 31:6), Rsvd1 (bits 5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** This field defines the low order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core
5:0	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

18.7.93 Event Ring Segment Table Base Address High 8 (ERSTBA_HI8)—Offset 2114h

The *Event Ring Segment Table Base Address Register* identifies the start address of the Event Ring Segment Table. There are 8 ERSTBA_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2114h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: ERSTBA_HI (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. Refer to the xHCI for USB specification for more information. This field shall not be modified if HCHalted (HCH) = 0. **Power Well:** Core

18.7.94 Event Ring Dequeue Pointer Low 8 (ERDP_LO8)—Offset 2118h

There are 8 ERDP_LOx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 2118h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP (31:4), EHB (3), DESI (2:0)

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core
3	0b RW/C	**Event Handler Busy (EHB):** This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to the xHCI for USB specification for more information. **Power Well:** Core
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.95 Event Ring Dequeue Pointer High 8 (ERDP_HI8)—Offset 211Ch

There are 8 ERDP_HIx registers, with x = 1, 2, ... 8.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 211Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERDP

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. **Power Well:** Core

18.7.96 Door Bell 1 (DOORBELL1)—Offset 3000h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3000h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DBSID (31:16), Rsvd1 (15:8), DBT (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams *(MaxPStreams) 0)*, then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams *(MaxPStreams = 0)* and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to *Device Context Doorbells* and shall be cleared to 0 for *Host Controller Command Doorbells*.[br This field returns 0 when read. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DB Target (DBT):** This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. • **Device Context Doorbells (1-255)** • 0 = Reserved • 1 = Control EP 0 Enqueue Pointer Update • 2 = EP 1 OUT Enqueue Pointer Update • 3 = EP 1 IN Enqueue Pointer Update • 4 = EP 2 OUT Enqueue Pointer Update • 5 = EP 2 IN Enqueue Pointer Update • ... • 30 = EP 15 OUT Enqueue Pointer Update • 31 = EP 15 IN Enqueue Pointer Update • 32:247 = Reserved • 248:255 = Vendor Defined • **Host Controller Doorbell (0)** • 0 = Command Doorbell • 248:255 = Vendor Defined This field returns '0' when read, and should be treated as 'undefined' by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0. **Power Well:** Core

18.7.97 Door Bell 2 (DOORBELL2)—Offset 3004h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3004h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.98 Door Bell 3 (DOORBELL3)—Offset 3008h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3008h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.99 Door Bell 4 (DOORBELL4)—Offset 300Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 300Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.100 Door Bell 5 (DOORBELL5)—Offset 3010h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3010h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.101 Door Bell 6 (DOORBELL6)—Offset 3014h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3014h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.102 Door Bell 7 (DOORBELL7)—Offset 3018h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3018h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.103 Door Bell 8 (DOORBELL8)—Offset 301Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 301Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
DBSID				Rsvd1		DBT	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.104 Door Bell 9 (DOORBELL9)—Offset 3020h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3020h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
DBSID				Rsvd1		DBT	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.105 Door Bell 10 (DOORBELL10)—Offset 3024h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3024h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.106 Door Bell 11 (DOORBELL11)—Offset 3028h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3028h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.107 Door Bell 12 (DOORBELL12)—Offset 302Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 302Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.108 Door Bell 13 (DOORBELL13)—Offset 3030h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3030h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DBSID (31:16)	Rsvd1 (15:8)	DBT (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.109 Door Bell 14 (DOORBELL14)—Offset 3034h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3034h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DBSID (31:16)	Rsvd1 (15:8)	DBT (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.110 Door Bell 15 (DOORBELL15)—Offset 3038h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3038h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.111 Door Bell 16 (DOORBELL16)—Offset 303Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 303Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.112 Door Bell 17 (DOORBELL17)—Offset 3040h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3040h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31:16	15:8	7:0
0000000000000000	00000000	00000000
DBSID	Rsvd1	DBT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.113 Door Bell 18 (DOORBELL18)—Offset 3044h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3044h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31:16	15:8	7:0
0000000000000000	00000000	00000000
DBSID	Rsvd1	DBT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.114 Door Bell 19 (DOORBELL19)—Offset 3048h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3048h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.115 Door Bell 20 (DOORBELL20)—Offset 304Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 304Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.116 Door Bell 21 (DOORBELL21)—Offset 3050h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3050h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.117 Door Bell 22 (DOORBELL22)—Offset 3054h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3054h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.118 Door Bell 23 (DOORBELL23)—Offset 3058h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3058h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.119 Door Bell 24 (DOORBELL24)—Offset 305Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 305Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.120 Door Bell 25 (DOORBELL25)—Offset 3060h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3060h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.121 Door Bell 26 (DOORBELL26)—Offset 3064h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3064h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.122 Door Bell 27 (DOORBELL27)—Offset 3068h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3068h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DBSID (31:16)	Rsvd1 (15:8)	DBT (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.123 Door Bell 28 (DOORBELL28)—Offset 306Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 306Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DBSID (31:16)	Rsvd1 (15:8)	DBT (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.124 Door Bell 29 (DOORBELL29)—Offset 3070h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3070h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.125 Door Bell 30 (DOORBELL30)—Offset 3074h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3074h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.126 Door Bell 31 (DOORBELL31)—Offset 3078h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 3078h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.127 Door Bell 32 (DOORBELL32)—Offset 307Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved. Refer to the xHCI for USB specification for more information.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 307Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DBSID																Rsvd1								DBT							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**DB Stream ID (DBSID):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core
15:8	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	00h RW	**DB Target (DBT):** Refer to field descriptions for the DOORBELL1 register. **Power Well:** Core

18.7.128 XECP_SUPP_USB2_0—Offset 8000h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8000h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 02000802h

31 28 24 20 16 12 8 4 0

0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	0 0 1 0
USB2_MAJ_REV		USB_MIN_REV		NCP		SPID	

Bit Range	Default & Access	Field Name (ID): Description
31:24	02h RO	**USB Major Revision: 2.0 (USB2_MAJ_REV):** Reserved. **Power Well:** Core
23:16	00h RO	**USB Minor Revision (USB_MIN_REV):** Reserved. **Power Well:** Core
15:8	08h RO	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	02h RO	**Supported Protocol ID (SPID):** Reserved. **Power Well:** Core

18.7.129 XECP_SUPP_USB2_1—Offset 8004h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8004h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 20425355h

Bits 31–28	Bits 27–24	Bits 23–20	Bits 19–16	Bits 15–12	Bits 11–8	Bits 7–4	Bits 3–0
0 0 1 0	0 0 0 0	0 1 0 0	0 0 1 0	0 1 0 1	0 0 1 1	0 1 0 1	0 1 0 1

Field (31:0): XECP_SUPP_USB2_1

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1:** Namestring USB **Power Well:** Core

18.7.130 XECP_SUPP_USB2_2—Offset 8008h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8008h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 30190601h

Bits 31–28	Bits 27–24	Bits 23–20	Bits 19–16	Bits 15–12	Bits 11–8	Bits 7–4	Bits 3–0
0 0 1 1	0 0 0 0	0 0 0 1	1 0 0 1	0 0 0 0	0 1 1 0	0 0 0 0	0 0 0 1

Fields: PROT_SPD_ID_CNT (31:28), Rsvd0 (27:21), BLC (20), HLC (19), IHI (18), HSO (17), RSVD (16), CPC (15:8), CPO (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 3 USB 2.0 Speed (High, Full, Low) **Power Well:** Core
27:21	00h RO	**Rsvd0:** Reserved. **Power Well:** Core
20	1b RO	**BESL LPM Capability (BLC):** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. **Power Well:** Core
19	1b RO	**Protocol Defined - Hardware LMP Capability (HLC):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
18	0b RO	**Protocol Defined - Integrated Hub Implementation (IHI):** Reserved. **Power Well:** Core
17	0b RO	**Protocol Defined - High SPeed Only (HSO):** Reserved. **Power Well:** Core
16	1b RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:8	06h RO	**Compatible Port Count (CPC):** Reserved. **Power Well:** Core
7:0	01h RO	**Compatible Port Offset (CPO):** Reserved. **Power Well:** Core

18.7.131 XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8010h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000C0021h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 1

Bits 31:16	Bits 15:9	Bit 8	Bits 7:6	Bits 5:4	Bits 3:0
PSIM	Rsvd0	PFD	PLT	PSIE	PSIV

Bit Range	Default & Access	Field Name (ID): Description
31:16	000Ch RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	00h RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0b RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0h RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	1h RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

18.7.132 XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8014h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 05DC0012h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
PSIM																Rsvd0							PFD	PLT		PSIE		PSIV			

Bit Range	Default & Access	Field Name (ID): Description
31:16	05DCh RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	00h RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0b RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0h RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	1h RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	2h RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

18.7.133 XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8018h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 01E00023h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 1	1 1 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 1 1

Bits	Field
31:16	PSIM
15:9	Rsvd0
8	PFD
7:6	PLT
5:4	PSIE
3:0	PSIV

Bit Range	Default & Access	Field Name (ID): Description
31:16	01E0h RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	00h RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0b RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0h RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	3h RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

18.7.134 XECP_SUPP_USB3_0—Offset 8020h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8020h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 03000802h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	0 0 1 0

Bits	Field
31:24	USB3_MAJ_REV
23:16	USB_MIN_REV
15:8	NCP
7:0	SPID

Bit Range	Default & Access	Field Name (ID): Description
31:24	03h RO	**USB Major Revision: 3.0 (USB3_MAJ_REV):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:16	00h RO	**USB Minor Revision (USB_MIN_REV):** Reserved. **Power Well:** Core
15:8	08h RO	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	02h RO	**Supported Protocol ID (SPID):** Reserved. **Power Well:** Core

18.7.135 XECP_SUPP_USB3_1—Offset 8024h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8024h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 20425355h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1
XECP_SUPP_USB2_1																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1:** Namestring USB **Power Well:** Core

18.7.136 XECP_SUPP_USB3_2—Offset 8028h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8028h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 10000107h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 1 1 1
Field	PROT_SPD_ID_CNT	Rsvd0			CPC		CPO	

Bit Range	Default & Access	Field Name (ID): Description
31:28	1h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed) **Power Well:** Core
27:16	000h RO	**Rsvd0:** Reserved. **Power Well:** Core
15:8	01h RO	**Compatible Port Count (CPC):** Reserved. **Power Well:** Core
7:0	07h RO	**Compatible Port Offset (CPO):** Reserved. **Power Well:** Core

18.7.137 XECP_SUPP_USB3_3—Offset 8030h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8030h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00050134h

Bits	31:28	27:24	23:20	19:16	15:12	11:9	8	7:6	5:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1	0 0 0 0	0 0 0	1	0 0	1 1	0 1 0 0
Field	PSIM				Rsvd0		PFD	PLT	PSIE	PSIV

Bit Range	Default & Access	Field Name (ID): Description
31:16	0005h RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	00h RO	**Rsvd0:** Reserved. **Power Well:** Core
8	1b RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	3h RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	4h RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

18.7.138 XECP_CMDM_STS0—Offset 8040h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8040h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000CC1h

Bit	Default	Field
31	0	IDMA_OWNS_CNTX
30	0	ODMA_OWNS_CNTX
29	0	TRM_OWNS_CNTX
28	0	CMD_RING_REQUESTED_CNTX_LOCK
27	0	CMD_RING_STOP_IN_PROGRESS
26	0	SCH_UPDATE_CLR_EP_IN_PROGRESS
25	0	ADDR_DEV_DONE
24	0	ADDR_DEV_IN_PROGRESS
23	0	EP_STATE_UPDATE_IN_PROGRESS
22	0	EP_STATE_IN_PROGRESS_FROM_STOP_DUE_TO_DB
21	0	EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_EP_ERROR
20	0	EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_STALL
19	0	RSVD
18	0	STOP_IN_PROGRESS
17	0	CMD_RING_DB_PENDING
16	0	CMD_RING_RUNNING
15:8	0 0 0 0 1 1 0 0	CMD_NEXT_CAP_OFFSET
7:0	1 1 0 0 0 0 0 1	VID

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**IDMA_OWNS_CNTX:** Indicates that IDMA module owns the context access currently **Power Well:** Core
30	0h RO	**ODMA_OWNS_CNTX:** Indicates that ODMA module owns the context access currently **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO	**TRM_OWNS_CNTX:** Indicates that TRM modules owns the context access currently **Power Well:** Core
28	0h RO	**CMD_RING_REQUESTED_CNTX_LOCK:** Indicates that Command Manager has requested a context lock **Power Well:** Core
27	0h RO	**CMD_RING_STOP_IN_PROGRESS:** Indicates that Command Ring stop command is in progress **Power Well:** Core
26	0h RO	**SCH_UPDATE_CLR_EP_IN_PROGRESS:** Indicates that clearing an EP out of schedule is in progress **Power Well:** Core
25	0h RO	**ADDR_DEV_DONE:** Indicates that current address device command is done by ODMA **Power Well:** Core
24	0h RO	**ADDR_DEV_IN_PROGRESS:** Indicates that ODMA has an address device command in progress **Power Well:** Core
23	0h RO	**EP_STATE_UPDATE_IN_PROGRESS:** Indicates that updating of EP state is in progress **Power Well:** Core
22	0h RO	**EP_STATE_IN_PROGRESS_FROM_STOP_DUE_TO_DB:** Indicates that doorbell manager is issuing an EP update due to a doorbell ring on an EP that is in stop state **Power Well:** Core
21	0h RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_EP_ERROR:** Indicates that transfer ring manager is issuing an EP update due to an EP error condition detected **Power Well:** Core
20	0h RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_STALL:** Indicates that transfere ring manager is issuing an EP state update due to stall received **Power Well:** Core
19	0h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
18	0h RO	**STOP in progress (STOP_IN_PROGRESS):** Indicates that a STOP on the Command Ring is in progress **Power Well:** Core
17	0h RO	**commend ring has doorbell pending (CMD_RING_DB_PENDING):** Indicates that the commend ring has doorbell pending **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**commend ring running (CMD_RING_RUNNING):** Indicates that the commend ring is running **Power Well:** Core
15:8	0Ch RO	**Command next capability offset (CMD_NEXT_CAP_OFFSET):** Reserved. **Power Well:** Core
7:0	C1h RO	**Vendor defined capability ID (VID):** Reserved. **Power Well:** Core

18.7.139 XECP_CMDM_STS1—Offset 8044h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8044h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 03FC0000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Rsvd0	EMPCS	INT7_TRB_CNT	INT6_TRB_CNT	INT5_TRB_CNT

Bit Range	Default & Access	Field Name (ID): Description
31:26	00h RO	**Rsvd0:** Reserved. **Power Well:** Core
25:18	FFh RO	**Event manager Producer Cycle State (EMPCS):** Reserved. **Power Well:** Core
17:12	00h RO	**Interrupter 7 TRB Count [5:0] (INT7_TRB_CNT):** Reserved. **Power Well:** Core
11:6	00h RO	**Interrupter 6 TRB Count [5:0] (INT6_TRB_CNT):** Reserved. **Power Well:** Core
5:0	00h RO	**Interrupter 5 TRB Count [5:0] (INT5_TRB_CNT):** Reserved. **Power Well:** Core

18.7.140 XECP_CMDM_STS2—Offset 8048h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8048h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Rsvd0 | ERST

Bit Range	Default & Access	Field Name (ID): Description
31:5	0000000h RO	**Rsvd0:** Reserved. **Power Well:** Core
4:0	00h RO	**Event Ring Segment Table (ERST):** count low **Power Well:** Core

18.7.141 XECP_CMDM_STS3—Offset 804Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 804Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Rsvd0 | ERST

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Rsvd0:** Reserved. **Power Well:** Core
15:0	0000h RO	**Event Ring Segment Table (ERST):** count high **Power Well:** Core

18.7.142 XECP_CMDM_STS4—Offset 8050h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8050h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EREPL

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Event Ring Enqueue Pointer Low (EREPL):** Reserved. **Power Well:** Core

18.7.143 XECP_CMDM_STS5—Offset 8054h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8054h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EREPH

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Event Ring Enqueue Pointer High (EREPH):** Reserved. **Power Well:** Core

18.7.144 Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h

This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8070h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0000FCC0h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 0 0	1 1 0 0	0 0 0 0

Bits	Field
31:0	HOST_CTRL_CAP_REG

Bit Range	Default & Access	Field Name (ID): Description
31:0	0000FCC0h RW/L	**Host Controller Capability (HOST_CTRL_CAP_REG):** This is a register that describe the host controller the extended cap location. It includes the XECP_HOST_NEXT_CAP_OFFSET and VEND_DEF_HOST_CAP_ID_192 **Power Well:** Core

18.7.145 Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8078h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Field
31:10	RSVD
9:5	SNDC
4:1	EP_NUM
0	CISM

Bit Range	Default & Access	Field Name (ID): Description
31:10	000000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
9:5	00h RW	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots. **Power Well:** Core
4:1	0h RW	**EP Number (EP_NUM):** 4bits of EP number **Power Well:** Core
0	0b RW	**Clear Internal Scheduler's Mask (CISM):** This is a register that is used to clear the internal scheduler's mask that is used to stop scheduling a particular EP. Bit0 indicates the direction of the EP **Power Well:** Core

18.7.146 Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 807Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HOST_CLR_IN_EP_VALID_REG

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG):** This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP. This field indicates the port number. For a 2port configuration, only bit1:0 are valid. It can scale for the max number of ports that we support. **Power Well:** Core

18.7.147 Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8080h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD | SNDC | EP_NUM | CISPM

Bit Range	Default & Access	Field Name (ID): Description
31:10	000000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
9:5	00h RW	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots **Power Well:** Core
4:1	0h RW	**EP Number (EP_NUM):** 4bits of EP number **Power Well:** Core
0	0b RW	**Clear Internal Scheduler's Poll Mask (CISPM):** This is a register that is used to clear the internal scheduler's poll mask that is used to indicate whether we need to poll this EP. This is used for USB2. Bit0 indicates the direction of the EP **Power Well:** Core

18.7.148 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8094h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00008100h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Field
31:21	SCHED_HOST_CTRL_CONT
20:13	TTE_HOST_CTRL
12:11	CACHE_SZ_CTRL
10:9	MAX_EP_SLOT
8	TO_SCRATCH_PAD_EN
7:0	SCHED_HOST_CTRL

Bit Range	Default & Access	Field Name (ID): Description
31:21	000h RW	**Scheduler Host Control Reg Cont (SCHED_HOST_CTRL_CONT):** method of USB2 port periodic done check (off by default) **Power Well:** Core
20:13	04h RW	**TTE Host Control (TTE_HOST_CTRL):** (0): disable interrupt complete split limit to 3 microframes (1): disable checking of missed microframes (2): disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (3): disable deferred split error request on speculative IN with data payload and no TRB. (7:4): reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:11	0h RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** • 0 = 64 • 1 = 32 • 2,3 = 16 **Power Well:** Core
10:9	0h RW	**Maximum EP Per Slot (MAX_EP_SLOT):** • 0 = 32 • 1 = 16 • 2 = 8 • 3 = 4 **Power Well:** Core
8	1b RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN):** Reserved. **Power Well:** Core
7:0	00h RW	**Scheduler Host Control Reg (SCHED_HOST_CTRL):** • (0): disable poll delay • (1): disable TRM active in EP valid check • (2): enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip) • (3) enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip) • (5:4) scheduler sort pattern • -- 00 (default) search ISO ahead of interrupt within each service interval • -- 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval • -- 10 - search strictly by interval • -- 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3 • (6): disable 1 pack scheduling limit when ISO pending in present microframe • (7): enable check to stop scheduling on port that are not connected **Power Well:** Core

18.7.149 Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80A0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00003C0Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1
RSVD												EN_PP_REG_PDWN	RESERVED		EN_USB_PP2_EN	EN_U3P_CG	EN_P3_OVR_P2_RD	EN_UPP_RST_EP3	RSVD_1												

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
19	0b RW	**Enable PCIe PHY Regulator Power Down (EN_PP_REG_PDWN):** • 0 = Disable PCIe PHY regulator power down mode • 1 = Enable PCIe PHY regulator power down mode **Power Well:** Core
18:17	0h RW	**Reserved (RESERVED):** Reserved **Power Well:** Core
16	0b RW	**Enable USB PHY p2_EN (EN_USB_PP2_EN):** • 0 = Disable USB PHY P2_EN • 1 = Enable USB PHY P2_EN **Power Well:** Core
15	0b RW	**Enable USB3 Port Clock Gate (EN_U3P_CG):** • 0 = Disable USB3 port clock gate • 1 = Enable USB3 port clock gate **Power Well:** Core
14	0b RW	**Enable P3 Override P2 RxDetect (EN_P3_OVR_P2_RD):** • 0 = Disable P3 overriding P2 in RxDetect • 1 = Enable P3 overriding P2 in RxDetect **Power Well:** Core
13	1b RW	**Enable USB PHY Pipe Reset Exit P3 (EN_UPP_RST_EP3):** • 0 = Disable a USB PHY pipe reset when exit P3 • 1 = Enable a USB PHY pipe reset when exit P3 **Power Well:** Core
12:0	1C0Fh RO	**RESERVED (RSVD_1):** Reserved. **Power Well:** Core

18.7.150 AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80C0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 015FC0F0h

Bit	Default	Field
31	0	RST_U3_AM_PDL
30	0	RSVD
29	0	EN_PPIPE_PPHY_RST
28	0	EN_PPWRDN_PERST
27	0	DIS_PERST_MRST
26	0	DIS_PERST_HC
25	0	EN_FAST_RST
24	1	PREV_U3_LDRST
23	0	IGN_MPU_RST
22	1	RSVD_1
21	0	IGN_HC_RST_U2
20	1	IGN_HC_RST_UP_POR
19	1	EN_PLD_RST
18	1	EN_EEP_REL_PU
17	1	IGN_HC_RST_PPP
16	1	IGN_LRST_UPP
15	1	IGN_WR_UPP
14	1	ALL_CPLD_RST
13	0	IGN_HR_U3
12	0	IGN_WR_U3
11	0	IGN_MPU_RST_U3
10	0	IGN_MPU_RST_U2
9	0	IGN_MPU_RST_PC
8	0	IGN_MPU_RST_PP
7	1	IGN_HC_RST_UP
6	1	IGN_WRST_UP
5	1	EN_HC_RST_PPI
4	1	ALL_PO_PDRST
3	0	IGN_PERST_PSD
2	0	IGN_FRST_AUX_PU
1	0	TRIG_FRST
0	0	

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Reset USB3 AUX/Main PD Logic (RST_U3_AM_PDL):** A reset that is designed to reset all USB3 port AUX + Main power domain logic. This is a debug function. It is called cold reset. A write of 1 to this register will issue a cold reset to USB3 ports. **Power Well:** SUS
30	0b RW	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
29	0b RW	**Enable PCIe PIPE Reset As PCIe PHY Reset (EN_PPIPE_PPHY_RST):** This bit set to 1 selects the PCIe PIPE reset as a PCIe PHY power on reset. 0 selects the AUX powerup reset as a PCIe PHY powerup reset. **Power Well:** SUS
28	0b RW	**Ensure PIPE Powerdown On PERST# (EN_PPWRDN_PERST):** This bit ensures any PERST# being asserted will cause PIPE powerdown state transition to P1. **Power Well:** SUS
27	0b RW	**Disable PERST# Main RST (DIS_PERST_MRST):** There is a feature where we only allow PERST# to be treated as a main powerdown reset when it is asserted during the state that is not in D3. This bit disables this feature when it is set to 1. If this bit is set to 1, it means that any PERST# will be treated as a main power domain reset regardless of its Dstate. **Power Well:** SUS
26	0b RW	**Disable PCIe PERST# Host Controller (DIS_PERST_HC):** There is a feature where we can disable PCIe PERST# from reset the host controller until power management control module has done its clock switching. This is for a case where PM entered L23 and immediately PERST# asserted. This bit is designed to enable this feature when set to 1. **Power Well:** SUS
25	0b RW	**Enable Fast Simulation Reset Mode (EN_FAST_RST):** Enable a fast simulation mode for reset function. This is a feature for GLS **Power Well:** SUS
24	1b RW	**Prevent USB3 Link Down Reset (PREV_U3_LDRST):** When set to 1, prevent a reset being generated due to the USB3 port link down condition. **Power Well:** SUS
23	0b RW	**Ignore Main Power Up Reset (IGN_MPU_RST):** When set to 1, ignore the main power up reset for USB3 PIPE PHY reset. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
22	1b RW	**RESERVED (RSVD_1):** Reserved. **Power Well:** SUS
21	0b RW	**Ignore HC Reset USB2 (IGN_HC_RST_U2):** When set to '1', ignore HC reset to reset the USB2 Port logic. **Power Well:** SUS
20	1b RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP_POR):** When set to '1', ignore HC reset to the USB PHY power-on reset. **Power Well:** SUS
19	1b RW	**Enable PCIe Link-Down Reset (EN_PLD_RST):** Enable a reset due to a PCIe link-down condition. The PCIe link down condition will cause a HC reset liked. If this bit is set 1, the PCIe link down condition will only reset the PCIe core. **Power Well:** SUS
18	1b RW	**Enable EEPROM Reload On Power Up (EN_EEP_REL_PU):** When set to '1', enable EEPROM reload on every main power-up. **Power Well:** SUS
17	1b RW	**Ignore HC Reset PCIe PHY PIPE (IGN_HC_RST_PPP):** When set to '1', ignore HC reset to the PCIe PHY PIPE reset. **Power Well:** SUS
16	1b RW	**Ignore LTSSM Reset USB PHY PIPE (IGN_LRST_UPP):** When set to '1', ignore the LTSSM of USB link state transition caused reset to USB PHY PIPE reset. **Power Well:** SUS
15	1b RW	**Ignore Warm Reset USB PHY Power (IGN_WR_UPP):** When set to '1', ignore warm reset the USB PHY power on reset. **Power Well:** SUS
14	1b RW	**Allow Core PCIe Link Down Reset (ALL_CPLD_RST):** When set to '1', allow PCIe link down to cause a reset to the rest of the core. **Power Well:** SUS
13	0b RW	**Ignore Hot Reset USB3 (IGN_HR_U3):** When set to '1', ignore hot reset to the USB3 port logic. **Power Well:** SUS
12	0b RW	**Ignore Warm Reset USB3 (IGN_WR_U3):** When set to '1', ignore warm reset to the USB3 port logic **Power Well:** SUS
11	0b RW	**Ignore Main Power Up Reset USB3 (IGN_MPU_RST_U3):** When set to '1', ignore main power up reset to USB3 port logic. **Power Well:** SUS
10	0b RW	**Ignore Main Power Up Reset USB2 (IGN_MPU_RST_U2):** When set to '1', ignore main power up reset to USB2 port logic. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
9	0b RW	**Ignore Main Power Up Reset PCIe Core (IGN_MPU_RST_PC):** When set to '1', ignore main power up reset to PCIe core. **Power Well:** SUS
8	0b RW	**Ignore Main Power Up Reset PCIe PHY (IGN_MPU_RST_PP):** When set to '1', ignore main power up reset to PCIe PHY. **Power Well:** SUS
7	1b RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP):** When set to '1', ignore HC reset to the USB PHY. **Power Well:** SUS
6	1b RW	**Ignore Warm Reset USB PHY (IGN_WRST_UP):** When set to '1', ignore warm reset to the USB PHY. **Power Well:** SUS
5	1b RW	**Enable HC Reset Per Port Isolation (EN_HC_RST_PPI):** Enables the HC reset or per port reset isolation function. **Power Well:** Core
4	1b RW	**Allow Power Off Power Domain Reset (ALL_PO_PDRST):** When set to '1', allow main power off condition to trigger a main power domain reset. **Power Well:** SUS
3	0b RW	**Ignore Wait For PERST# During Power Shut Down (IGN_PERST_PSD):** When set to '1', ignore waiting for PERST# deassertion during main power shut down. **Power Well:** SUS
2	0b RW	**Ignore Fundamental Reset During AUX Power Up (IGN_FRST_AUX_PU):** If this bit is set and a fundamental reset is asserted during AUX power up, then PERST# shall be ignored and a timeout will be allowed to deassert fundamental reset instead. **Power Well:** SUS
1:0	0h RW	**Trigger Fundamental Reset (TRIG_FRST):** Writing to bit(1:0) to value of 2'b11 will cause a fundamental reset **Power Well:** SUS

18.7.151 Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80C4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 004A4008h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 1 0 0	1 0 1 0	0 1 0 0	0 0 0 0	0 0 0 0	1 0 0 0
RSVD		MAX_TT_BWA			PP_OVRH_SSBW		

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	4A4h RW	**Max. TT BW Allowed (MAX_TT_BWA):** see white paper **Power Well:** Core
11:0	008h RW	**Per Packet Overhead SS BW (PP_OVRH_SSBW):** BW calculation: Overhead per packet for SS BW calculations. see white paper. **Power Well:** Core

18.7.152 High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80C8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0001A01Fh

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 0 1 0	0 0 0 0	0 0 0 1	1 1 1 1
RSVD		PP_OVRH_HSTTBW			PP_OVRH_HSBW		

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	01Ah RW	**Per Packet Overhead HS-TT BW (PP_OVRH_HSTTBW):** BW calculation: Overhead per packet for HS-TT BW calculations. see white paper. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:0	01Fh RW	**Per Packet Overhead HS BW (PP_OVRH_HSBW):** BW calculation: Overhead per packet for HS BW calculations. see white paper. **Power Well:** Core

18.7.153 Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80CCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00014080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
RSVD								PP_OVRH_FSBW												PP_OVRH_LSBW											

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	014h RW	**Per Packet Overhead FS BW (PP_OVRH_FSBW):** BW calculation: Overhead per packet for FS BW calculations. see white paper. **Power Well:** Core
11:0	080h RW	**Per Packet Overhead LS BW (PP_OVRH_LSBW):** BW calculation: Overhead per packet for LS BW calculations. see white paper. **Power Well:** Core

18.7.154 System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80D0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00032010h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 0 1 0	0 0 0 0	0 0 0 1	0 0 0 0	

RSVD	PTTP_OVRH_SBW	PP_OVRH_SBW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	032h RW	**Per TT Packet Overhead System BW (PTTP_OVRH_SBW):** BW calculation: Overhead per TT packet for System BW calculations. see white paper. **Power Well:** Core
11:0	010h RW	**Per Packet Overhead System BW (PP_OVRH_SBW):** BW calculation: Overhead per packet for System BW calculations. see white paper. **Power Well:** Core

18.7.155 Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h

Global defaults for inserting delays between packets in the scheduler for async. types.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80D4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RSVD	HS_BD_EN	HS_BD_DEF	FS_BD_EN	FS_BD_DEF	HS_CD_EN	HS_CD_DEF	FS_CD_EN	FS_CD_DEF	LS_CD_EN	LS_CD_DEF

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
19	0b RW	**High-Speed Bulk Delay Enable (HS_BD_EN):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RW	**High-Speed Bulk Delay Default (HS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
15	0b RW	**Full-Speed Bulk Delay Enable (FS_BD_EN):** Reserved. **Power Well:** Core
14:12	0h RW	**Full-Speed Bulk Delay Default (FS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
11	0b RW	**High-Speed Control Delay Enable (HS_CD_EN):** Reserved. **Power Well:** Core
10:8	0h RW	**High-Speed Control Delay Default (HS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
7	0b RW	**Full-Speed Control Delay Enable (FS_CD_EN):** Reserved. **Power Well:** Core
6:4	0h RW	**Full-Speed Control Default (FS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
3	0b RW	**Low-Speed Control Delay Enable (LS_CD_EN):** Reserved. **Power Well:** Core
2:0	0h RW	**Low-Speed Control Delay Default (LS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core

18.7.156 AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 80D8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80D8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
RSVD	ALL_SW_UP_RST

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
3:0	0h WO	**Allow Software USB PHY RST (ALL_SW_UP_RST):** Allow a USB PHY reset being issued by software. Writing to this register with bit set to 1 will reset the USB PHY that is connected to the port. Bit3:0 indicates the port number of the USB PHY **Power Well:** SUS

18.7.157 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80E0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 808DBCA0h

Bit	Default	Field
31	1	D3_HOT_FXN_EN
30	0	ALL_L1_CORE_CG
29	0	AL_EP_SEXT
28	0	ALL_EP_RCP
27	0	AL_PERST_FRST
26	0	OVR_PCIE_P2_P1
25	0	SET_ISSV_1
24	0	CLR_ISSV_0
23	1	EN_SRE_SW_LD
22	0	RSVD_1
21	0	FORCE_SR1
20	0	CPTR
19	1	CIDS1
18	1	CIDS0
17	0	EN_CFG_UP2
16	1	CCGD
15	1	EN_CFG_RDP3
14	0	EN_CFG_PIPE_RST
13	1	EN_FILT_TX_IDLE
12	1	EN_HE_GEN_PME
11	1	EN_ISOL
10	1	EN_L1_P2_OVR
9	0	EN_CORE_CG
8	0	EN_PHY_STS_TO
7	1	IGN_APE_PC
6	0	EN_P2_OVR_P1
5	1	EN_P2_REM_WAKE
4:1	0 0 0 0	FORCED_PM_STATE
0	0	INIT_FPMS

Bit Range	Default & Access	Field Name (ID): Description
31	1b RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from a pin input set to 1, but we allow software to alter it, if needed. • 1 = D3 hot enabled • 0 = D3 hot not abled. **Power Well:** SUS
30	0b RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state. **Power Well:** SUS
29	0b RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal. **Power Well:** SUS
28	0b RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27	0b RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a foundamental reset **Power Well:** SUS
26	0b RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1. **Power Well:** SUS
25	0b RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1. **Power Well:** SUS
24	0b RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0. **Power Well:** SUS
23	1b RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function. **Power Well:** SUS
22	0b RW	**RESERVED (RSVD_1):** Reserved. **Power Well:** SUS
21	0b RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function. **Power Well:** SUS
20	0b RW	**cfg pcie txreg rd (CPTR):** Reserved. **Power Well:** SUS
19	1b RW	**cfg iob drivestrength[1] (CIDS1):** Reserved. **Power Well:** SUS
18	1b RW	**cfg iob drivestrength[0] (CIDS0):** Reserved. **Power Well:** SUS
17	0b RW	**Enable CFG USB P2 (EN_CFG_UP2):** When set to '1' enable cfg usb p2 **Power Well:** SUS
16	1b RW	**cfg clk gate dis (CCGD):** Reserved. **Power Well:** SUS
15	1b RW	**Enable CFG RXDET P3 (EN_CFG_RDP3):** When set to '1' enable cfg rxdet p3 **Power Well:** SUS
14	0b RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13	1b RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states. **Power Well:** SUS
12	1b RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to enable or not enable the host engine to generate a PME message. **Power Well:** SUS
11	1b RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation **Power Well:** SUS
10	1b RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function. **Power Well:** SUS
9	0b RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' enable core clock gating based on low power state entered **Power Well:** SUS
8	0b RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle. **Power Well:** SUS
7	1b RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support **Power Well:** SUS
6	0b RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state. **Power Well:** SUS
5	1b RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering **Power Well:** SUS
4:1	0h RW	**Forced PM State (FORCED_PM_STATE):** Reserved. **Power Well:** SUS
0	0b RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1 **Power Well:** SUS

18.7.158 Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80E4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30:4	3	2	1	0
0	0000 0000 0000 0000 0000 0000 000	0	0	0	0
EN_DS_BC	RSVD	EN_P3_BC	EN_P2_BC	EN_P1_BC	EN_P0_BC

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Enable DM_SRC Battery Charge (EN_DS_BC):** • 1 - Always enable battery charge DM_SRC if not connected. Don't wait for portable device detect. (spec. ver. 1.2) • 0 - Battery charge spec ver. 1.1. **Power Well:** SUS
30:4	0000000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
3	0b RW	**Enable Port 3 Battery Charging (EN_P3_BC):** • 0 - Battery charging disabled (Physical Port #3) • 1 - Battery charging enabled (Physical Port #3) **Power Well:** SUS
2	0b RW	**Enable Port 2 Battery Charging (EN_P2_BC):** • 0 = Battery charging disabled (Physical Port #2) • 1 = Battery charging enabled (Physical Port #2) **Power Well:** SUS
1	0b RW	**Enable Port 1 Battery Charging (EN_P1_BC):** • 0 = Battery charging disabled (Physical Port #1) • 1 = Battery charging enabled (Physical Port #1) **Power Well:** SUS
0	0b RW	**Enable Port 0 Battery Charging (EN_P0_BC):** • 0 = Battery charging disabled (Physical Port #0) • 1 = Battery charging enabled (Physical Port #0) **Power Well:** SUS

18.7.159 Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80E8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00800080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Fields: RBUF_WM (31:16), XBUF_WM (15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0080h RW	**RBUF water mark (RBUF_WM):** Reserved. **Power Well:** Core
15:0	0080h RW	**XBUF water mark (XBUF_WM):** Reserved. **Power Well:** Core

18.7.160 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80ECh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 18010600h

31			28				24				20				16				12				8				4				0
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Fields: FORCE_LTSSM_ST, DL_LTSSM_ST, DL_U0, FORCED_CMP_PAT, EN_LES_CNT, DEBUG_MD_SEL, PHY_LP_LAT, LR_MIN_TM, LP_MIN_TM, FORCE_LA_PMC, DL_REC_U0, LINK_FTM, DIS_LINK_SCRAM, DL_U3_U0, DL_U2_U0, DL_U1_U0, EN_LINK_LB_MAST, DIS_LINK_CM

Bit Range	Default & Access	Field Name (ID): Description
31:27	03h RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced This value is for test purpose only. **Power Well:** Core
26	0b RW	**Direct Link LTSSM State (DL_LTSSM_ST):** • 0 = Normal operation mode • 1 = Direct link to a specific state specified by bit 31:27 This bit is for test purposes only. It shall be written 0 in normal operation mode. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Direct Link To U0 (DL_U0):** • 0 = Normal operation mode • 1 = Direct link to U0 This bit is for test purposes only. It shall be written 0 in normal operation mode. **Power Well:** Core
24:21	0h RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode This value is for test purpose only. **Power Well:** Core
20	0b RW	**Enable Link Error Slave Count (EN_LES_CNT):** • 0 = Disable link error slave count • 1 = Enable link error slave count **Power Well:** Core
19:17	0h RW	**Debug Mode Select (DEBUG_MD_SEL):** Reserved. **Power Well:** Core
16:15	2h RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode. • 0 = 4 cycles • 1 = 8 cycles • 2 = 16 cycles • 3 = 32 cycles **Power Well:** Core
14:12	0h RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us. **Power Well:** Core
11:9	3h RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us. **Power Well:** Core
8	0b RW	**Force Link Accept PM Command (FORCE_LA_PMC):** • 0 = Normal operation mode • 1 = Force link to accept power management command **Power Well:** Core
7	0b RW	**Direct Link Recovery U0 (DL_REC_U0):** • 0 = Normal operation mode • 1 = Direct link to Recovery from U0 **Power Well:** Core
6	0b RW	**Link Fast Training Mode (LINK_FTM):** • 0 = Normal operation mode • 1 = Link fast training mode This bit should be written 0 in normal operation. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** • 0 = Enable link scrambler • 1 = Disable link scramber **Power Well:** Core
4	0b RW	**Direct Link U3 From U0 (DL_U3_U0):** • 0 = Normal operation mode • 1 = Direct link to U3 from U0 This bit is for test purposes only. It shall be written 0 in normal operation mode. **Power Well:** Core
3	0b RW	**Direct Link U3 From U0 (DL_U2_U0):** • 0 = Normal operation mode • 1 = Direct link to U2 from U0 This bit is for test purposes only. It shall be written 0 in normal operation mode. **Power Well:** Core
2	0b RW	**Direct Link U3 From U0 (DL_U1_U0):** • 0 = Normal operation mode • 1 = Direct link to U1 from U0 This bit is for test purposes only. It shall be written 0 in normal operation mode. **Power Well:** Core
1	0b RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST):** • 0 = Disable link loopback master mode • 1 = Enable link loopback master mode **Power Well:** Core
0	0b RW	**Disable Link Compliance Mode (DIS_LINK_CM):** • 0 = Enable link compliance mode • 1 = Disable link compliance mode **Power Well:** Core

18.7.161 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h

This set of registers is used to control the USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80F0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 310003A0h

Bits	Default	Field
31:24	0 0 1 1 0 0 0 1	FSLS_SE0_DIS_DEL_7_0
23:18	0 0 0 0 0 0	RSVD
17	0	EN_DETECT_NOMINAL_PKT_EOP
16	0	DIS_CHIRP_RESPONSE
15	0	DIS_192B_LIM
14	0	EXT_FSLS_DIS
13:12	0 0	UTMI_RST_SEL
11	0	DIS_HS_DIS_WIN
10	0	DIS_PERR_DET
9	1	DIS_PF_IOUT
8	1	DRV_RESK_FSLS_SER
7	1	EN_U2_DROP_PING
6	0	EN_U2_FORCE_PING
5	1	EN_U2_AUTO_PING
4	0	DIS_PHY_SUSM
3	0	UTMI_INT_CG_DIS
2	0	DIS_PSUSM_DS
1	0	FORCE_PHY_RST
0	0	U2_ACC_SIM_TIM

Bit Range	Default & Access	Field Name (ID): Description
31:24	31h RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred. **Power Well:** SUS
23:18	00h RW	**Reserved (RSVD):** Reserved. **Power Well:** SUS
17	0b RW	**EN_DETECT_NOMINAL_PKT_EOP:** • 0 = Detect minimal packet EOP. • 1 = Detect nominal packet EOP. **Power Well:** SUS
16	0b RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** • 0 = Normal • 1 = Force full speed on host ports (disable chirp response) **Power Well:** SUS
15	0b RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** • 0 = Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. • 1 = Disable 192 byte limit check. **Power Well:** SUS
14	0b RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** • 0 = Internal FS/LS Disconnect from linestate(1:0) • 1 = External provided FS/LS Disconnect from hostdisconnect input **Power Well:** SUS
13:12	0h RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) • 00 = HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) • 01,11 = UTMI reset = ~UTMI suspendm • 10 = UTMI reset = ~UTMI suspendm and synchronization to port clk. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
11	0b RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** • 0 = Enable HS Disconnect Window Function • 1 = Disable HS Disconnect Window Function **Power Well:** SUS
10	0b RW	**Disable Port Error Detection (DIS_PERR_DET):** • 0 = Enable Port Error Detection (default) • 1 = Disable Port Error Detection **Power Well:** SUS
9	1b RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** • 0 = Enable Peek function for ISO-OUT (default) • 1 = Disable Peek function for ISO-OUT **Power Well:** SUS
8	1b RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** • 0 = Drive Resume-K on parallel Interface • 1 = Drive Resume-K directly on FS/LS Serial Interface (default) **Power Well:** SUS
7	1b RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** • 0 = Disable Drop-Ping Function in USB2 Protocol (default) • 1 = Enable Drop-Ping Function in USB2 Protocol **Power Well:** SUS
6	0b RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** • 0 = Disable Force-Ping Function in USB2 Protocol (default) • 1 = Enable Force-Ping Function in USB2 Protocol **Power Well:** SUS
5	1b RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** • 0 = Disable Auto-Ping Function • 1 = Enable Auto-Ping Function in USB2 Protocol (default) **Power Well:** SUS
4	0b RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** • 0 = PHY is suspend=U3,U2,disconnect (default) • 1 = Disable PHY SuspendM in All States **Power Well:** SUS
3	0b RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** • 0 = Normal operation (internal clock gated in U2,U3,disconnect) • 1 = UTMI Internal Clock Gate Disable **Power Well:** SUS
2	0b RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** • 0 = PHY is suspendM=0 in Disconnect State (default) • 1 = Disable PHY SuspendM in Disconnect State **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**Force PHY Reset (FORCE_PHY_RST):** • 0 = Normal Operation (default) • 1 = Force PHY Reset **Power Well:** SUS
0	0b RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** • 0 = Normal Operation (default - FPGA/ASIC) • 1 = USB2 Accelerated Simulation Timing (default - simulation) **Power Well:** SUS

18.7.162 USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h

This set of registers is used to control the USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80F4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 80C40620h

31	30:18	17:5	4:0
1	0 0 0 0 0 0 0 1 1 0 0 0	1 0 0 0 0 0 0 0 1 1 0 0 0	1 0 0 0 0
TOT_RST_DUR_0	CHIRPK_DUR	KJ_DIS_CON_DEL	FSLS_SE0_DIS_DEL_12_8

Bit Range	Default & Access	Field Name (ID): Description
31	1b RW	**Total Reset Duration[0] (TOT_RST_DUR_0):** # of microseconds for total reset duration **Power Well:** SUS
30:18	0031h RW	**Chirp-K Duration (CHIRPK_DUR):** # of microseconds of Chirp-K to register that a device is chirping **Power Well:** SUS
17:5	0031h RW	**K/J Disconnect Connect Delay (KJ_DIS_CON_DEL):** # of microseconds of K/J in disconnected state to register connect has occurred. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
4:0	00h RW	**FS/LS Mode SE0 Disconnect Delay[12:8] (FSLS_SE0_DIS_DEL_12_8):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred. **Power Well:** SUS

18.7.163 USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h

This set of registers is used to control the USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80F8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: F865EB6Bh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	0	0	0	0	1	1	0	0	1	0	1	1	1	1	0	1	0	1	1	0	1	1	0	1	0	1	1
U2_IGN_LS_DUR_3_0				U3_IGN_LS_DUR													TOT_RST_DUR_15_1														

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**U2 Entry Ignore Linestate Changes Duration[3:0] (U2_IGN_LS_DUR_3_0):** # of microseconds after entering U2, linestate changes are ignored as bus settles **Power Well:** SUS
27:15	10CBh RW	**U3 Entry Ignore Linestate Changes Duration (U3_IGN_LS_DUR):** # of microseconds after entering U3, linestate changes are ignored as bus settles **Power Well:** SUS
14:0	6B6Bh RW	**Total Reset Duration[15:1] (TOT_RST_DUR_15_1):** # of microseconds for total reset duration **Power Well:** SUS

18.7.164 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh

This set of registers is used to control the USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80FCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00008003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

RSVD	U2D_RWAKE_DEL	U2_IGN_LS_DUR_12_4

Bit Range	Default & Access	Field Name (ID): Description
31:22	000h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
21:9	0040h RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K **Power Well:** SUS
8:0	003h RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles **Power Well:** SUS

18.7.165 Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8100h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00008008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

RSVD	RSVD_1

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	8008h RW	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

18.7.166 Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8108h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 31:1	Bit 0
Rsvd1	HOSTIF

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RW	**Rsvd1:** Reserved. **Power Well:** Core
0	1b RW	**Host IF (HOSTIF):** Reserved. **Power Well:** Core

18.7.167 Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 810Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00008020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits 31:24	Bits 23:12	Bits 11:0
RSVD	PB_OVRH_SBW	PB_OVRH_SSBW

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	008h RW	**Per Burst Overhead System BW (PB_OVRH_SBW):** BW calculation: Overhead per burst for system BW calculations. see white paper. **Power Well:** Core
11:0	020h RW	**Per Burst Overhead System BW (PB_OVRH_SSBW):** BW calculation: Overhead per burst for SS BW calculations. see white paper. **Power Well:** Core

18.7.168 USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8128h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0F42528505647F42h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4
0000	1111	0100	0010	0101	0010	1000	0101	0000	0101	0110	0100	0111	1111	0100	0010
RSVD	PCIE_MAX_BW			TT_MAX_BW			FSLS_MAX_BW			HS_MAX_BW			SS_MAX_BW		

Bit Range	Default & Access	Field Name (ID): Description
63:60	0h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
59:48	F42h RW	**PCIe Max BW Units (PCIE_MAX_BW):** Max. Number of BW units for PCIe (system interface) (denominator in 90% calculation) **Power Well:** Core
47:36	528h RW	**TT Max BW Units (TT_MAX_BW):** Max. Number of BW units for TTs. (denominator in 90% calculation) **Power Well:** Core
35:24	505h RW	**FS/LS Max BW Units (FSLS_MAX_BW):** Max. Number of BW units for FS/LS ports. (denominator in 90% calculation) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:12	647h RW	**HS Max BW Units (HS_MAX_BW):** Max. Number of BW units for HS ports. (denominator in 80% calculation) **Power Well:** Core
11:0	F42h RW	**SS Max BW Units (SS_MAX_BW):** Max. Number of BW units for SS ports. (denominator in 90% calculation) **Power Well:** Core

18.7.169 USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8130h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31:28	27:26	25:24	23:22	21:20	19:18	17:16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
0 0 0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
RSVD	P14_UTMI_LS	P13_UTMI_LS	P12_UTMI_LS	P11_UTMI_LS	P10_UTMI_LS	P9_UTMI_LS	P8_UTMI_LS	P7_UTMI_LS	P6_UTMI_LS	P5_UTMI_LS	P4_UTMI_LS	P3_UTMI_LS	P2_UTMI_LS	P1_UTMI_LS

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
27:26	0h RO	**Port 14 UTMI Linestate (P14_UTMI_LS):** Reserved. **Power Well:** Core
25:24	0h RO	**Port 13 UTMI Linestate (P13_UTMI_LS):** Reserved. **Power Well:** Core
23:22	0h RO	**Port 12 UTMI Linestate (P12_UTMI_LS):** Reserved. **Power Well:** Core
21:20	0h RO	**Port 11 UTMI Linestate (P11_UTMI_LS):** Reserved. **Power Well:** Core
19:18	0h RO	**Port 10 UTMI Linestate (P10_UTMI_LS):** Reserved. **Power Well:** Core
17:16	0h RO	**Port 9 UTMI Linestate (P9_UTMI_LS):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Port 8 UTMI Linestate (P8_UTMI_LS):** Reserved. **Power Well:** Core
13:12	0h RO	**Port 7 UTMI Linestate (P7_UTMI_LS):** Reserved. **Power Well:** Core
11:10	0h RO	**Port 6 UTMI Linestate (P6_UTMI_LS):** Reserved. **Power Well:** Core
9:8	0h RO	**Port 5 UTMI Linestate (P5_UTMI_LS):** Reserved. **Power Well:** Core
7:6	0h RO	**Port 4 UTMI Linestate (P4_UTMI_LS):** Reserved. **Power Well:** Core
5:4	0h RO	**Port 3 UTMI Linestate (P3_UTMI_LS):** Reserved. **Power Well:** Core
3:2	0h RO	**Port 2 UTMI Linestate (P2_UTMI_LS):** Reserved. **Power Well:** Core
1:0	0h RO	**Port 1 UTMI Linestate (P1_UTMI_LS):** Reserved. **Power Well:** Core

18.7.170 USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8134h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000C3C640C05140Ch

Bits 63–56	Bits 55–48	Bits 47–40	Bits 39–32	Bits 31–24	Bits 23–16	Bits 15–8	Bits 7–0
0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 0	0 0 1 1 1 1 0 0	0 1 1 0 0 1 0 0	0 0 0 0 1 1 0 0	0 0 0 0 0 1 0 1	0 0 0 1 0 1 0 0	0 0 0 0 1 1 0 0
RSVD	LSTX_GAP_TIME	LSRX_GAP_TIME	LS_GAP_TIME	FS_GAP_TIME	HSRX_GAP_TIME	HSTXSOF_GAP_TIME	HSTX_GAP_TIME

Bit Range	Default & Access	Field Name (ID): Description
63:56	00h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
55:48	0ch RW	**GAP time after LS TX thru FS hub (LSTX_GAP_TIME):** Reserved. **Power Well:** Core
47:40	3ch RW	**GAP time after LS RX thru FS hub (LSRX_GAP_TIME):** Reserved. **Power Well:** Core
39:32	64h RW	**GAP timer after LS (LS_GAP_TIME):** Reserved. **Power Well:** Core
31:24	0ch RW	**GAP time after FS (FS_GAP_TIME):** Reserved. **Power Well:** Core
23:16	05h RW	**GAP time after HS RX (HSRX_GAP_TIME):** Reserved. **Power Well:** Core
15:8	14h RW	**GAP time after HS TX SOF (HSTXSOF_GAP_TIME):** Reserved. **Power Well:** Core
7:0	0ch RW	**GAP time HS TX Packet (HSTX_GAP_TIME):** Reserved. **Power Well:** Core

18.7.171 USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 813Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 8D4258B8h

31 28 24 20 16 12 8 4 0

1 0 0 0 | 1 1 0 1 | 0 1 0 0 | 0 0 1 0 | 0 1 0 1 | 1 0 0 0 | 1 0 1 1 | 1 0 0 0

LS_BUS_TO | FS_BUS_TO | HS_BUS_TO

Bit Range	Default & Access	Field Name (ID): Description
31:21	46ah RW	**Bus timeout count for LS (LS_BUS_TO):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
20:10	096h RW	**Bus timeout count for FS (FS_BUS_TO):** Reserved. **Power Well:** Core
9:0	0b8h RW	**Bus timeout count for HS (HS_BUS_TO):** Reserved. **Power Well:** Core

18.7.172 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8140h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0A019132h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	1	1	0	0	1	0
EIH								BPSAW												BPSMID											

Bit Range	Default & Access	Field Name (ID): Description
31:24	0ah RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1. **Power Well:** Core
23:12	019h RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. • Register Format: • Bits [11:7] # of 125us uframes • Bits [6:0] # of microseconds (0-124) **Power Well:** Core
11:0	132h RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdown. Register Format: • Bits [11:7] # of 125us uframes • Bits [6:0] # of microseconds (0-124) **Power Well:** Core

18.7.173 Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h

These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8144h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0000033Fh

31:10	9	8	7	6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	1	0	0	1	1	1	1	1	1
RSVD	HS_INT_OUT_ALRM	HS_INT_IN_ALRM	SS_INT_OUT_FC_ALRM	SS_INT_IN_FC_ALRM	SS_INT_OUT_ALRM	SS_INT_IN_ALRM	HS_ISO_OUT_ALRM	HS_ISO_IN_ALRM	SS_ISO_OUT_ALRM	SS_ISO_IN_ALRM

Bit Range	Default & Access	Field Name (ID): Description
31:10	000000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
9	1b RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM):** Reserved. **Power Well:** Core
8	1b RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM):** Reserved. **Power Well:** Core
7	0b RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM):** Reserved. **Power Well:** Core
6	0b RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM):** Reserved. **Power Well:** Core
5	1b RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM):** Reserved. **Power Well:** Core
4	1b RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM):** Reserved. **Power Well:** Core
3	1b RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM):** Reserved. **Power Well:** Core
2	1b RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM):** Reserved. **Power Well:** Core
1	1b RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	1b RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM):** Reserved. **Power Well:** Core

18.7.174 Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8150h

The Latency Tolerance Control Register is used by SW to control which BELT is returned when this register is read. SW shall write to this register to program a Slot-ID, Port-ID and BELT Select to determine which BELT is selected. When this register is read the selected BELT is returned.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8150h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

Bits	31:30	29:17	16	15:12	11:5	4:0
Default	00	0000000000000	0	0000	0000000	00000
Field	BELT_SEL	Rsvd1	PORT_SEL	Rsvd	BELTV	SLOT_SEL

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h WO	**BELT Select (BELT_SEL):** This field determines what value will be selected to read back from SW when reading this register. • 0 = Returns the SW programmed Latency Tolerance Value • 1 = Returns the Lowest BELT in the Host • 2 = Returns the BELT for the requested Slot-ID (Slot Select) • 3 = Returns the BELT for the requested Port-ID (Port Select) **Power Well:** Core
29:17	0h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0h WO	**Port Select (PORT_SEL):** Used to select the BELT for a given Port # when the BELT Select is programmed to select the Port-ID (this field is 0 based) **Power Well:** Core
15:12	0h RO	**Rsvd:** Reserved. **Power Well:** Core
11:5	0h RO	**BELT Value (BELTV):** Value of selected BELT is return in this field **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4:0	00h RW	**Slot Select (SLOT_SEL):** Reads will return: BELT Value (BELTV) [4:0]: Value of selected BELT is return in this field Writes will control : Slot Select (): Used to select the BELT for a given Slot # when the BELT Select is programmed to select the Slot-ID (this field is zero based) **Power Well:** Core

18.7.175 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8154h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 01390206h

Bits	Default	Field
31:28	0 0 0 0	RSVD0
27:25	0 0 0	RSVD
24	1	EN_L1_EXIT_NOTIF_PCIE
23	0	DIS_PLC_ON_DISCONNECT
22	0	TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2
21	1	DIS_P2_OVERWRITE_DUE2_D3HOT
20	1	ENABLE_AUTO_U3_ENTRY_FROM_U2_U3
19	1	DIS_LINKDOWN_RST_DURING_LOW_POWER
18	0	EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0
17	0	U2_EXIT_LFPS_TIMER_VALUE
16	1	EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP
15:14	0 0	P3_ENTRY_TIMEOUT
13	0	EN_U2_P3
12:11	0 0	FINE_DM_SEL
10	0	EN_LP_CORE_CG
9	1	DIS_U3_PORT_SCE
8:4	0 0 0 0 0	DEB_MODE_SEL
3	0	EN_AWAK_NIDLE
2	1	EN_PMC_P1_EXIT_P2
1	1	EN_PP_CLK_ISOL
0	0	EN_P2OVRP1_ADET

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**RESERVED0 (RSVD0):** Reserved. **Power Well:** SUS
27:25	0h RW	**RESERVED (RSVD):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24	1b RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCie core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. • 1 = enables this feature • 0 = disables this feature. **Power Well:** SUS
23	0b RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** • 1 = do not assert PLC for disconnection • 0 = assert PLC for disconnection **Power Well:** SUS
22	0b RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2:** This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. • 1 = treat Logic IDLE as TS2 received when in some PCIe LTSSM state. • 0 = disable this feature. **Power Well:** SUS
21	1b RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. • 1 = disables p2 overwrite due to the D3HOT where PCIe core enters the L1. • 0 = enables P2 overwrite even if we are in D3Hot. **Power Well:** SUS
20	1b RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** • 1 = enables the port to enter U3 automatically when in U1/U2 • 0 = disables the port to enter U3 automatically when in U1/U2 **Power Well:** SUS
19	1b RW	**No linkdown reset is issued during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issued during low power state. **Power Well:** SUS
18	0b RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0:** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. • 1 = enable this feature • 0 = disable this feature **Power Well:** SUS
17	0b RW	**U2_EXIT_LFPS_TIMER_VALUE:** This bit selects U2 exit LFPS timer value. • 0 = 320ns 400ns in 25MHz domain • 1 = 240ns 320ns in 25MHz domain **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP:** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. • 1 = enables this function • 0 = disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed. **Power Well:** SUS
15:14	0h RW	**P3_ENTRY_TIMEOUT:** This field defines the timeout value to enter P3 mode in U2. • 00 = 7us 8us • 01 = 511us 512us • 10 = disables the timer (0us) • 11 = disables the timer (0us) **Power Well:** SUS
13	0b RW	**Enable U2 P3 Mode (EN_U2_P3):** • 0 = Disable U2 P3 mode • 1 = Enable U2 P3 mode **Power Well:** SUS
12:11	0h RW	**Fine Debug Mode Select (FINE_DM_SEL):** Reserved. **Power Well:** SUS
10	0b RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1', enable core clock gating based on low power state entered **Power Well:** SUS
9	1b RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** • 0 = Enable USB3 port status change event generation if any change bit is not cleared • 1 = Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0 **Power Well:** SUS
8:4	00h RW	**Debug Mode Select Register (DEB_MODE_SEL):** Reserved. **Power Well:** SUS
3	0b RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1, enables the auto wakeup function when engine has identified non IDLE condition. **Power Well:** SUS
2	1b RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set to 1, enables the PM control module to transition to P1 instead of P0 upon exit from P2. **Power Well:** SUS
1	1b RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1, enables the PCIe PIPE CLK to be isolated when main power is removed. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1, enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending. **Power Well:** SUS

18.7.176 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8164h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000000FCh

Bits	31:8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	1	1	1	1	1	0	0
Field	RSVD	EN_CMDM_TXRXB	EN_TTE_TXRXB	EN_IDMA_TXRXB	EN_ODMA_TXRXB	EN_TRM_TXRXB	EN_SCH_TXRXB	EN_RXB_CD	EN_TXB_CD

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
7	1b RW	**EN_CMDM_TXRXB:** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
6	1b RW	**EN_TTE_TXRXB:** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
5	1b RW	**EN_IDMA_TXRXB:** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
4	1b RW	**EN_ODMA_TXRXB:** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
3	1b RW	**EN_TRM_TXRXB:** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	1b RW	**EN_SCH_TXRXB:** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
1	0b RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits) **Power Well:** Core
0	0b RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits) **Power Well:** Core

18.7.177 USB Power Gating Control (USB_PGC)—Offset 8168h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8168h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD
USB_SRAM_PGE

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
0	0b RW	**USB SRAM power gating enable (USB_SRAM_PGE):** When set enables power gating on USB ports. Usage of this bit is further qualified with xHCI SRAM Dynamic Power Gating Disable fuse. If the fuse disables dynamic power gating, setting this bit to 1 shall not enable power gating feature. This bit always returns the value that was written to it irrespective of the setting of xHCI SRAM Dynamic Power Gating Disable fuse. **Power Well:** Core

18.7.178 xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 816Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000400h

Bits	31:20	19	18	17	16	15	14	13:12	11:8	7	6	5	4	3	2	1	0
Default	0000 0000 0000	0	0	0	0	0	0	0 0	0 1 0 0	0	0	0	0	0	0	0	0
Field	RSVD	PARUSB3_ENG_GEN	PARUSB3_LINK_GEN	PARUSB2_CLK_GEN	USHIP_PCGEN	RSVD1	USB3_AC_CGE	RX_DT_ACG	U2R_BM_CG	FTCGPU2E	USB2_PC_TE	XHCI_AC_GE	XHCI_APMB_CGE	USB3_AC_TGE	USB3_AP_CGE	MPP_AC_GEU2	MPP_AC_GE_DDU3

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**Reserved (RSVD):** Reserved.
19	0b RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition. **Power Well:** SUS
18	0b RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition. **Power Well:** SUS
17	0b RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition. **Power Well:** SUS
16	0b RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition. **Power Well:** SUS
15	0b RO	**Reserved1 (RSVD1):** Reserved
14	0b RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it, irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. • 0x0 = 100ms • 0x1 = 12ms • Others = Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively. **Power Well:** SUS
11:8	4h RW	**U2 Residency Before ModPHY Clock Gating (U2R_BM_CG):** Before gating ModPHY Aux clock, Host Controller shall wait for this time in U2. This time is meant to ensure that the attached device has entered U2 as well. • 0x0 = 1us • 0x1 = 128us • 0x2 = 256us • 0x3 = 512us • 0x4 = 640us • 0x5 = 768us • 0x6 = 896us • 0x7 = 1024us • Others = Reserved Note: This counter shall start counting once pipe has entered PS3 state in response to link in U2. **Power Well:** SUS
7	0h RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2. **Power Well:** SUS
6	0b RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow. **Power Well:** SUS
5	0b RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
4	0b RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
3	0b RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**USB3 Port Aux/Port clock gating enable (USB3_AP_CGE):** When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
1	0b RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
0	0b RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS

18.7.179 USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8170h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00090032h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

RSVD	MIN_U3E_LFPS_D	MIN_U2_ELFPS_D	XHCI_MAX_PING_LFPS	RSVD_1	XHCI_BESL_HIRD_DT

Bit Range	Default & Access	Field Name (ID): Description
31:22	000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
21:19	001b RW	**Min U3 Exit LFPS Duration (MIN_U3E_LFPS_D):** This field defines the minimum duration of LFPS driven by Host Controller upon U3 exit LFPS handshake. Note that there is an uncertainty of +-16us in actual duration driven by the Host Controller. • • 0b000 = 96us • 0b001 = 160us • 0b010 = 224us • 0b011 = 288us • 0b100 = 352us • 0b101 = 416us • 0b110 = 480us • 0b111 = 544us **Power Well:** SUS
18:16	001b RW	**Min U2 Exit LFPS Duration (MIN_U2_ELFPS_D):** This field defines the minimum duration of LFPS driven by Host Controller upon U2 exit LFPS handshake. Note that there is an uncertainty of +-16us in actual duration driven by the Host Controller. • 0b000 = 96us • 0b001 = 160us • 0b010 = 224us • 0b011 = 288us • 0b100 = 352us • 0b101 = 416us • 0b110 = 480us • 0b111 = 544us **Power Well:** SUS
15	0b RW	**Max PING LFPS Rx Detection (XHCI_MAX_PING_LFPS):** This field defines the maximum timing for PING LFPS. If an incoming LFPS will be considered a PING if it has a timing such that it is less than or equal to the selected value. Otherwise it will be considered for the other types of LFPS. • 0b Max PING LFPS timing set to 256 ns • (32 link clocks) • 1b Max PING LFPS timing set to 320 ns (40 link clocks) **Power Well:** SUSe
14:10	00h RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
9:0	032h RW	**xHCI BESL to HIRD Distance (XHCI_BESL_HIRD_DT):** This field defines the gap between BESL and duration of Resume signalling from Host upon Host Initiated Resume from USB2.0 LPM. The default value of this register corresponds to xHCI spec defined 50us value. • Value BESL to HIRD Distance • 000h = 0us • 001h = 1us • 002h = 2us • 3FFh = 1023us **Power Well:** SUS

18.7.180 xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8174h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0040047Dh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	0	1
DIS_SDT_IDL_NR	RSVD					XLTRTP	XLTRE	PA_LTV												USB2_PL0_LTV											

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** • 0 = (default) allow scheduler direct transition from IDLE to NO requirement • 1 = Disable scheduler direct transition from IDLE to NO requirement **Power Well:** Core
30:26	00h RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
25	0b RW	**XHCI LTR Transition Policy (XLTRTP):** When '0', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timout and stays in Active until the next service boundary. When '1', the LTR messaging state machine transitions through High ? Med ? Low ? Active states assuming enough latency is available for each transition. **Power Well:** Core
24	0b RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC. **Power Well:** Core
23:12	400h RW	**Periodic Active LTV (PA_LTV):** • **23:22 Latency Scale** • 00b = Reserved • 01b = Latency Value to be multiplied by 1024 • 10b = Latency Value to be multiplied by 32,768 • 11b = Latency Value to be multiplied by 1,048,576 • • **21:12 Latency Value (ns) Defaults to 0 microseconds** **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:0	47Dh RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** • **11:10 Latency Scale** • 00b = Reserved • 01b = Latency Value to be multiplied by 1024 • 10b = Latency Value to be multiplied by 32,768 • 11b = Latency Value to be multiplied by 1,048,576 • • **9:0 Latency Value Defaults to 128 Microseconds(ns)** **Power Well:** Core

18.7.181 xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8178h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 000017FFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
RSVD																			LTV_LMT												

Bit Range	Default & Access	Field Name (ID): Description
31:13	00000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
12:0	17FFh RW	**LTV Limit (LTV_LMT):** This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a workaround or mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible - 101b • 12:10: Latency Multiplier Field • 000b - Value times 1 ns • 001b - Value times 32 ns • 010b - Value times 1,024 ns • 011b - Value times 32,768 ns • 100b - Value times 1,048,576 ns • 101b - Value times 33,554,432 ns • 110b-111b - Not Permitted • 9:0: Latency Value Default = 3FFh **Power Well:** Core

18.7.182 xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 817Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			MHIT													RSVD_1			HIWL												

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
28:16	0000h RW	**Minimum High Idle Time (MHIT):** LTR value can be indicated. This value must be larger than HIWL. • 12:7 - Time value in # of 125 Microsecond Bus Intervals (0 - 8ms) • 6:0 - Fractional BI Time value in Microseconds (0 - 124 Microseconds) **Power Well:** Core
15:13	0h RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
12:0	0000h RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state This value must be larger than MIWL and LIWL. • 12:7 - Time value in # of 125 Microseconds Bus Intervals (0 - 8ms) • 6:0 - Fractional BI Time value in Microseconds (0 - 124 Microseconds) **Power Well:** Core

18.7.183 xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8180h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			MMIT													RSVD_1			MIWL												

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
28:16	0000h RW	**Minimum Medium Idle Time (MMIT):** LTR value can be indicated. This value must be larger than MIWL. • 12:7 - Time value in # of 125 Microseconds Bus Intervals (0 - 8ms) • 6:0 - Fractional BI Time value in Microseconds (0 - 124 Microseconds) **Power Well:** Core
15:13	0h RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
12:0	0000h RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL. • 12:7 - Time value in # of 125 Microseconds Bus Intervals (0 - 8ms) • 6:0 - Fractional BI Time value in Microseconds (0 - 124 Microseconds) **Power Well:** Core

18.7.184 xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8184h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			MLIT													RSVD_1			LIWL												

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
28:16	0000h RW	**Minimum Low Idle Time (MLIT):** LTR value can be indicated. This value must be larger than LIWL • 12:7 - Time value in # of 125 Microseconds Bus Intervals (0 - 8ms) • 6:0 - Fractional BI Time value in Microseconds (0 - 124 Microseconds) **Power Well:** Core
15:13	0h RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:0	0000h RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. • 12:7 - Time value in # of 125 Microsecond Bus Intervals (0 - 8ms) • 6:0 - Fractional BI Time value in Microseconds (0 - 124 Microseconds) **Power Well:** Core

18.7.185 USB EP Type Lock Policy (USB_EP_TLP)—Offset 8344h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8344h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

Bit(s)	Default	Field
31:24	0 0 0 0 0 0 0 0	RSVD
23	0	POL3_INT_IN
22	0	POL3_BULK_IN
21	0	POL3_ISOCH_IN
20	0	POL3_CTRL
19	0	POL3_INT_OUT
18	0	POL3_BULK_OUT
17	0	POL3_ISOCH_OUT
16	0	RSVD_1
15	0	POL2_INT_IN
14	0	POL2_BULK_IN
13	0	POL2_ISOCH_IN
12	0	POL2_CTRL
11	0	POL2_INT_OUT
10	0	POL2_BULK_OUT
9	0	POL2_ISOCH_OUT
8	0	RSVD_2
7	0	POL1_INT_IN
6	0	POL1_BULK_IN
5	0	POL1_ISOCH_IN
4	0	POL1_CTRL
3	0	POL1_INT_OUT
2	0	POL1_BULK_OUT
1	0	POL1_ISOCH_OUT
0	0	USB_EP_TLPM_EN

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
23	0b RW/L	**Policy 3 Interrupt IN EP Type (POL3_INT_IN):** • 1 - EP Type = 7 is allowed by Policy 3 • 0 - EP Type = 7 is not allowed by Policy 3 **Power Well:** Core
22	0b RW/L	**Policy 3 Bulk IN EP Type (POL3_BULK_IN):** • 1 - EP Type = 6 is allowed by Policy 3 • 0 - EP Type = 6 is not allowed by Policy 3 **Power Well:** Core
21	0b RW/L	**Policy 3 Isochronous IN EP Type (POL3_ISOCH_IN):** • 1 - EP Type = 5 is allowed by Policy 3 • 0 - EP Type = 5 is not allowed by Policy 3 **Power Well:** Core
20	0b RW/L	**Policy 3 Control EP Type (POL3_CTRL):** • 1 - EP Type = 4 is allowed by Policy 3 • 0 - EP Type = 4 is not allowed by Policy 3 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
19	0b RW/L	**Policy 3 Interrupt OUT EP Type (POL3_INT_OUT):** • 1 - EP Type = 3 is allowed by Policy 3 • 0 - EP Type = 3 is not allowed by Policy 3 **Power Well:** Core
18	0b RW/L	**Policy 3 Bulk OUT EP Type (POL3_BULK_OUT):** • 1 - EP Type = 2 is allowed by Policy 3 • 0 - EP Type = 2 is not allowed by Policy 3 **Power Well:** Core
17	0b RW/L	**Policy 3 Isochronous OUT EP Type (POL3_ISOCH_OUT):** • 1 - EP Type = 1 is allowed by Policy 3 • 0 - EP Type = 1 is not allowed by Policy 3 **Power Well:** Core
16	0b RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
15	0b RW/L	**Policy 2 Interrupt IN EP Type (POL2_INT_IN):** • 1 - EP Type = 7 is allowed by policy 2 • 0 - EP Type = 7 is not allowed by policy 2 **Power Well:** Core
14	0b RW/L	**Policy 2 Bulk IN EP Type (POL2_BULK_IN):** • 1 - EP Type = 6 is allowed by policy 2 • 0 - EP Type = 6 is not allowed by policy 2 **Power Well:** Core
13	0b RW/L	**Policy 2 Isochronous IN EP Type (POL2_ISOCH_IN):** • 1 - EP Type = 5 is allowed by policy 2 • 0 - EP Type = 5 is not allowed by policy 2 **Power Well:** Core
12	0b RW/L	**Policy 2 Control EP Type (POL2_CTRL):** • 1 - EP Type = 4 is allowed by policy 2 • 0 - EP Type = 4 is not allowed by policy 2 **Power Well:** Core
11	0b RW/L	**Policy 2 Interrupt OUT EP Type (POL2_INT_OUT):** • 1 - EP Type = 3 is allowed by policy 2 • 0 - EP Type = 3 is not allowed by policy 2 **Power Well:** Core
10	0b RW/L	**Policy 2 Bulk OUT EP Type (POL2_BULK_OUT):** • 1 - EP Type = 2 is allowed by policy 2 • 0 - EP Type = 2 is not allowed by policy 2 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
9	0b RW/L	**Policy 2 Isochronous OUT EP Type (POL2_ISOCH_OUT):** • 1 - EP Type = 1 is allowed by policy 2 • 0 - EP Type = 1 is not allowed by policy 2 **Power Well:** Core
8	0b RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
7	0b RW/L	**Policy 1 Interrupt IN EP Type (POL1_INT_IN):** • 1 - EP Type = 7 is allowed by policy 1 • 0 - EP Type = 7 is not allowed by policy 1 **Power Well:** Core
6	0b RW/L	**Policy 1 Bulk IN EP Type (POL1_BULK_IN):** • 1 - EP Type = 6 is allowed by policy 1 • 0 - EP Type = 6 is not allowed by policy 1 **Power Well:** Core
5	0b RW/L	**Policy 1 Isochronous IN EP Type (POL1_ISOCH_IN):** • 1 - EP Type = 5 is allowed by policy 1 • 0 - EP Type = 5 is not allowed by policy 1 **Power Well:** Core
4	0b RW/L	**Policy 1 Control EP Type (POL1_CTRL):** • 1 - EP Type = 4 is allowed by policy 1 • 0 - EP Type = 4 is not allowed by policy 1 **Power Well:** Core
3	0b RW/L	**Policy 1 Interrupt OUT EP Type (POL1_INT_OUT):** • 1 - EP Type = 3 is allowed by policy 1 • 0 - EP Type = 3 is not allowed by policy 1 **Power Well:** Core
2	0b RW/L	**Policy 1 Bulk OUT EP Type (POL1_BULK_OUT):** • 1 - EP Type = 2 is allowed by policy 1 • 0 - EP Type = 2 is not allowed by policy 1 **Power Well:** Core
1	0b RW/L	**Policy 1 Isochronous OUT EP Type (POL1_ISOCH_OUT):** • 1 - EP Type = 1 is allowed by policy 1 • 0 - EP Type = 1 is not allowed by policy 1 **Power Well:** Core
0	0b RW/L	**USB EP Type Lock Policy match enable (USB_EP_TLPM_EN):** Globally enable policy matching **Power Well:** Core

18.7.186 USB EP Type Lock Policy - Port Control 1 (USB_EP_TLP1)—Offset 8348h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8348h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31:30	29:28	27:26	25:24	23:22	21:20	19:18	17:16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
EN_USB_LPM_RP16	EN_USB_LPM_RP15	EN_USB_LPM_RP14	EN_USB_LPM_RP13	EN_USB_LPM_RP12	EN_USB_LPM_RP11	EN_USB_LPM_RP10	EN_USB_LPM_RP9	EN_USB_LPM_RP8	EN_USB_LPM_RP7	EN_USB_LPM_RP6	EN_USB_LPM_RP5	EN_USB_LPM_RP4	EN_USB_LPM_RP3	EN_USB_LPM_RP2	EN_USB_LPM_RP1

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW/L	**Enable USB Lock Policy match on root port number 16 (EN_USB_LPM_RP16):** • 00 = policy is not enabled for root port number 16 • 01 = policy 1 is enabled for root port number 16 • 10 = policy 2 is enabled for root port number 16 • 11 = policy 3 is enabled for root port number 16 **Power Well:** Core
29:28	0h RW/L	**Enable USB Lock Policy match on root port number 15 (EN_USB_LPM_RP15):** • 00 = policy is not enabled for root port number 15 • 01 = policy 1 is enabled for root port number 15 • 10 = policy 2 is enabled for root port number 15 • 11 = policy 3 is enabled for root port number 15 **Power Well:** Core
27:26	0h RW/L	**Enable USB Lock Policy match on root port number 14 (EN_USB_LPM_RP14):** • 00 = policy is not enabled for root port number 14 • 01 = policy 1 is enabled for root port number 14 • 10 = policy 2 is enabled for root port number 14 • 11 = policy 3 is enabled for root port number 14 **Power Well:** Core
25:24	0h RW/L	**Enable USB Lock Policy match on root port number 13 (EN_USB_LPM_RP13):** • 00 = policy is not enabled for root port number 13 • 01 = policy 1 is enabled for root port number 13 • 10 = policy 2 is enabled for root port number 13 • 11 = policy 3 is enabled for root port number 13 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RW/L	**Enable USB Lock Policy match on root port number 12 (EN_USB_LPM_RP12):** • 00 = policy is not enabled for root port number 12 • 01 = policy 1 is enabled for root port number 12 • 10 = policy 2 is enabled for root port number 12 • 11 = policy 3 is enabled for root port number 12 **Power Well:** Core
21:20	0h RW/L	**Enable USB Lock Policy match on root port number 11 (EN_USB_LPM_RP11):** • 00 = policy is not enabled for root port number 11 • 01 = policy 1 is enabled for root port number 11 • 10 = policy 2 is enabled for root port number 11 • 11 = policy 3 is enabled for root port number 11 **Power Well:** Core
19:18	0h RW/L	**Enable USB Lock Policy match on root port number 10 (EN_USB_LPM_RP10):** • 00 = policy is not enabled for root port number 10 • 01 = policy 1 is enabled for root port number 10 • 10 = policy 2 is enabled for root port number 10 • 11 = policy 3 is enabled for root port number 10 **Power Well:** Core
17:16	0h RW/L	**Enable USB Lock Policy match on root port number 9 (EN_USB_LPM_RP9):** • 00 = policy is not enabled for root port number 9 • 01 = policy 1 is enabled for root port number 9 • 10 = policy 2 is enabled for root port number 9 • 11 = policy 3 is enabled for root port number 9 **Power Well:** Core
15:14	0h RW/L	**Enable USB Lock Policy match on root port number 8 (EN_USB_LPM_RP8):** • 00 = policy is not enabled for root port number 8 • 01 = policy 1 is enabled for root port number 8 • 10 = policy 2 is enabled for root port number 8 • 11 = policy 3 is enabled for root port number 8 **Power Well:** Core
13:12	0h RW/L	**Enable USB Lock Policy match on root port number 7 (EN_USB_LPM_RP7):** • 00 = policy is not enabled for root port number 7 • 01 = policy 1 is enabled for root port number 7 • 10 = policy 2 is enabled for root port number 7 • 11 = policy 3 is enabled for root port number 7 **Power Well:** Core
11:10	0h RW/L	**Enable USB Lock Policy match on root port number 6 (EN_USB_LPM_RP6):** • 00 = policy is not enabled for root port number 6 • 01 = policy 1 is enabled for root port number 6 • 10 = policy 2 is enabled for root port number 6 • 11 = policy 3 is enabled for root port number 6 **Power Well:** Core
9:8	0h RW/L	**Enable USB Lock Policy match on root port number 5 (EN_USB_LPM_RP5):** • 00 = policy is not enabled for root port number 5 • 01 = policy 1 is enabled for root port number 5 • 10 = policy 2 is enabled for root port number 5 • 11 = policy 3 is enabled for root port number 5 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW/L	**Enable USB Lock Policy match on root port number 4 (EN_USB_LPM_RP4):** • 00 = policy is not enabled for root port number 4 • 01 = policy 1 is enabled for root port number 4 • 10 = policy 2 is enabled for root port number 4 • 11 = policy 3 is enabled for root port number 4 **Power Well:** Core
5:4	0h RW/L	**Enable USB Lock Policy match on root port number 3 (EN_USB_LPM_RP3):** • 00 = policy is not enabled for root port number 3 • = policy 1 is enabled for root port number 3 • 10 = policy 2 is enabled for root port number 3 • 11 = policy 3 is enabled for root port number 3 **Power Well:** Core
3:2	0h RW/L	**Enable USB Lock Policy match on root port number 2 (EN_USB_LPM_RP2):** • 00 = policy is not enabled for root port number 2 • 01 = policy 1 is enabled for root port number 2 • 10 = policy 2 is enabled for root port number 2 • 11 = policy 3 is enabled for root port number 2 **Power Well:** Core
1:0	0h RW/L	**Enable USB Lock Policy match on root port number 1 (EN_USB_LPM_RP1):** • 00 = policy is not enabled for root port number 1 • 01 = policy 1 is enabled for root port number 1 • 10 = policy 2 is enabled for root port number 1 • 11 = policy 3 is enabled for root port number 1 **Power Well:** Core

18.7.187 USB EP Type Lock Policy - Port Control 2 (USB_EP_TLP2)—Offset 834Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 834Ch

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

Bits	31:8	7:6	5:4	3:2	1:0
Default	0000 0000 0000 0000 0000 0000	00	00	00	00
Field	RSVD	EN_USB_LPM_RP20	EN_USB_LPM_RP19	EN_USB_LPM_RP18	EN_USB_LPM_RP17

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
7:6	0h RW/L	**Enable USB Lock Policy match on root port number 20 (EN_USB_LPM_RP20):** • 00 = policy is not enabled for root port number 20 • 01 = policy 1 is enabled for root port number 20 • 10 = policy 2 is enabled for root port number 20 • 11 = policy 3 is enabled for root port number 20 **Power Well:** Core
5:4	0h RW/L	**Enable USB Lock Policy match on root port number 19 (EN_USB_LPM_RP19):** • 00 = policy is not enabled for root port number 19 • 01 = policy 1 is enabled for root port number 19 • 10 = policy 2 is enabled for root port number 19 • 11 = policy 3 is enabled for root port number 19 **Power Well:** Core
3:2	0h RW/L	**Enable USB Lock Policy match on root port number 18 (EN_USB_LPM_RP18):** • 00 = policy is not enabled for root port number 18 • 01 = policy 1 is enabled for root port number 18 • 10 = policy 2 is enabled for root port number 18 • 11 = policy 3 is enabled for root port number 18 **Power Well:** Core
1:0	0h RW/L	**Enable USB Lock Policy match on root port number 17 (EN_USB_LPM_RP17):** • 00 = policy is not enabled for root port number 17 • 01 = policy 1 is enabled for root port number 17 • 10 = policy 2 is enabled for root port number 17 • 11 = policy 3 is enabled for root port number 17 **Power Well:** Core

18.7.188 USB Legacy Support Capability (USBLEGSUP)—Offset 8460h

This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8460h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000801h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 1

Field	Rsvd2	HCOSOS	Rsvd1	HCBIOSOS	NextCP	CID
Bits	31:25	24	23:17	16	15:8	7:0

Bit Range	Default & Access	Field Name (ID): Description
31:25	00h RO	**Rsvd2:** Reserved. **Power Well:** Core
24	0b RW	**HC OS Owned Semaphore (HCOSOS):** Reserved. **Power Well:** SUS
23:17	00h RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0b RW	**HC BIOS Owned Semaphore (HCBIOSOS):** Reserved. **Power Well:** SUS
15:8	08h RW/S	**Next Capability Pointer (NextCP):** Reserved. **Power Well:** SUS
7:0	01h RW/L	**Capability ID (CID):** Reserved. **Power Well:** SUS

18.7.189 USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8464h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8464h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28:21	20	19:17	16	15	14	13	12:5	4	3:1	0
0	0	0	0 0 0 0 0 0 0 0	0	0 0 0	0	0	0	0	0 0 0 0 0 0 0 0	0	0 0 0	0
SMIBAR	SMIPCIC	SMIOSOC	Rsvd4	SMIHSE	Rsvd3	SMIEI	SMIBARE	SMIPCICE	SMIOSOE	Rsvd2	SMIHSEE	Rsvd1	USBSMIE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW/C	**SMI on BAR (SMIBAR):** Reserved. **Power Well:** SUS
30	0b RW/C	**SMI on PCI Command (SMIPCIC):** Reserved. **Power Well:** SUS
29	0b RW/C	**SMI on OS Ownership Change (SMIOSOC):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
28:21	00h RO	**Rsvd4:** Reserved. **Power Well:** Core
20	0b RO	**SMI on Host System Error (SMIHSE):** Reserved. **Power Well:** SUS
19:17	0h RO	**Rsvd3:** Reserved. **Power Well:** Core
16	0b RO	**SMI on Event Interrupt (SMIEI):** Reserved. **Power Well:** SUS
15	0b RW	**SMI on BAR Enable (SMIBARE):** Reserved. **Power Well:** SUS
14	0b RW	**SMI on PCI Command Enable (SMIPCICE):** Reserved. **Power Well:** SUS
13	0b RW	**SMI on OS Ownership Enable (SMIOSOE):** Reserved. **Power Well:** SUS
12:5	00h RO	**Rsvd2:** Reserved. **Power Well:** Core
4	0b RW	**SMI on Host System Error Enable (SMIHSEE):** Reserved. **Power Well:** SUS
3:1	0h RO	**Rsvd1:** Reserved. **Power Well:** Core
0	0b RW	**USB SMI Enable (USBSMIE):** Reserved. **Power Well:** SUS

18.7.190 Debug Capability ID Register (DCID)—Offset 8480h

The Debug Capability *ID Register* links the USB Debug Capability into the xHCI list of Extended Capabilities and defines its basic capabilities. This register is modified and maintained by BIOS.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8480h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0005000Ah

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

RSVD (31:21) | DCERSTM (20:16) | NCP (15:8) | CID (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:21	000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
20:16	05h RW	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Valid values are 0 15. This field determines the maximum value supported by the Debug Capability Event Ring Segment Table Base Size registers (see xHCI USB specification), where: The maximum number of Event Ring Segment Table entries = 2^(DCERST Max) e.g. if DCERST Max = 7, then the *Debug Capability Event Ring Segment Table(s)* supports up to 128 entries, 15 then 32K entries, etc. Note: This register is sticky. **Power Well:** Core
15:8	00h RW	**Next Capability Pointer (NCP):** This field indicates the location of the next capability with respect to the effective address of this capability. Refer to the xHCI USB specification for more information on this field. Note: This register is sticky. **Power Well:** Core
7:0	0Ah RW	**Capability ID (CID):** Refer to the xHCI USB specification for descriptions of the capabilities listed below. Note: This register is sticky. • 0 = Reserved • 1 = USB Legacy Support • 2 = Supported Protocol • 3 = Extended Power Management • 4 = I/O Virtualization • 5 = Message Interrupt • 6 = Local Memory • 7-9 = Reserved **Power Well:** Core

18.7.191 Debug Capability Doorbell Register (DCDB)—Offset 8484h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8484h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (31:16) | DBTGT (15:8) | RSVD_1 (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	00h RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:8	00h RW	**Doorbell Target (DBTGT):** This field defines the target of the doorbell reference. The table below defines the Debug Capability notification that is generated by ringing the doorbell. • 0 = Data EP 1 OUT Enqueue Pointer Update • 1 = Data EP 1 IN Enqueue Pointer Update • 2:255 = Reserved This field returns '0' when read and the value should be treated as undefined by software. **Power Well:** Core
7:0	00h RW	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

18.7.192 Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8488h

The Debug Capability *Event Ring Segment Table Size Register* defines the number of segments supported by the Debug Capability Event Ring Segment Table.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 8488h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																ERSTS															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the *Debug Capability Event Ring Segment Table Base Address* register. The maximum value supported by an xHC implementation for this register is defined by the *DCERST Max* field in the DCID register. See the xHCI USB specification for more information. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'. **Power Well:** Core

18.7.193 Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8490h

The *Debug Capability Event Ring Segment Table Base Address Register* identifies the start address of the Debug Capability Event Ring Segment Table.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8490h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0

Bits 63:4	Bits 3:0
ERSTBAR	RSVD

Bit Range	Default & Access	Field Name (ID): Description
63:4	000000000000000h RW	**Event Ring Segment Table Base Address Register (ERSTBAR):** This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the *Debug Capability Enable* field in the DCCTRL register to 1. **Power Well:** Core
3:0	0h RW	**Reserved (RSVD):** Reserved. **Power Well:** Core

18.7.194 Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8498h

The *Debug Capability Event Ring Dequeue Pointer Register* is written by software to define the Debug Capability Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it has finished the evaluation of an Event(s) on the Debug Capability Event Ring.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8498h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0

Bits 63:4	Bit 3	Bits 2:0
DQP	RSVD	DESI

Bit Range	Default & Access	Field Name (ID): Description
63:4	000000000000000h RW	**Dequeue Pointer (DQP):** This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the *Debug Capability Enable* field in the DCCTRL register to '1'. **Power Well:** Core
3	0b RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

18.7.195 Debug Capability Control Register (DCCTRL)—Offset 84A0h

The *Debug Capability Control Register* is used to manage the Debug Capability.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 84A0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30:24	23:16	15:5	4	3	2	1	0
0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0
DCE	DADDR	DMBS	RSVD	DRC	HIT	HOT	LSE	DCR

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Debug Capability Enable (DCE):** Setting this bit to a 1 enables xHCI USB Debug Capability operation. This bit is a 0 if the USB Debug Capability is disabled. Clearing this bit releases the Root Hub port assigned to the Debug Capability, and terminates any Debug Capability Transfer or Event Ring activity. **Power Well:** Core
30:24	00h RO	**Device Address (DADDR):** This field reports the USB device address assigned to the Debug Device during the enumeration process. This field is valid when the *DbC Run* bit is 1. **Power Well:** Core
23:16	00h RO	**Debug Max Burst Size (DMBS):** This field identifies the maximum burst size supported by the bulk endpoints of this DbC implementation. LPT-LP USB Debug Device does not support bursting. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:5	000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
4	0b RW/C	**DbC Run Change (DRC):** This bit shall be set to '1' when DCR bit is cleared to '0', i.e. by any DbC Port State transition that exits the DbC-Configured state. While this bit is 1 the *Debug Capability Doorbell Register* (DCDB) is disabled. Software shall clear this bit to re-enable the DCDB. **Power Well:** Core
3	0b RW/S	**Halt IN TR (HIT):** While this bit is 1 the Debug Capability shall generate STALL TPs for all OUT DPs received for the IN TR. The Debug Capability shall clear this bit when a ClearFeature(ENDPOINT_HALT) request is received for the endpoint. This field is valid only when the Debug Capability is in Run Mode (DCR = 1). When not in Run Mode, this field shall return 0 when read, and writes will have no effect. Refer to the xHCI USB specification for more information. **Power Well:** Core
2	0b RW/S	**Halt OUT TR (HOT):** While this bit is 1 the Debug Capability shall generate STALL TPs for all IN TPs received for the OUT TR. The Debug Capability shall clear this bit when a ClearFeature(ENDPOINT_HALT) request is received for the endpoint. This field is valid only when the Debug Capability is in Run Mode (DCR = 1). When not in Run Mode, this field shall return 0 when read, and writes will have no effect. Refer to the xHCI USB specification for more information. **Power Well:** Core
1	0b RW	**Link Status Event Enable (LSE):** Setting this bit to a 1 enables the Debug Capability to generate Port Status Change Events due to the *Port Link Status Change* bit transitioning from a 0 to a 1. Refer to the xHCI USB specification for more information. **Power Well:** Core
0	0b RO	**DbC Run (DCR):** When 0, Debug Device is not in the Configured state. When 1, Debug Device is in the Configured state and bulk Data pipe transactions are accepted by Debug Capability and routed to the IN and OUT Transfer Rings. A 0 to 1 transition of the *Port Reset* (DCPORTSC:PR) bit will clear this bit to 0. **Power Well:** Core

18.7.196 Debug Capability Status Register (DCST)—Offset 84A4h

The *Debug Capability Status Register* reports capability related status information to software.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 84A4h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPNUM (31:24)	RSVD (23:1)	ERNE (0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Debug Port Number (DPNUM):** This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port. **Power Well:** Core
23:1	000000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
0	0b RO	**Event Ring Not Empty (ERNE):** When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the *Debug Capability Event Ring Dequeue Pointer* register. **Power Well:** Core

18.7.197 Debug Capability Port Status and Control Register (DCPORTSC)—Offset 84A8h

The fields of the *Debug Capability PORTSC Register* are defined below and provide information about the state of the Root Hub port that is assigned to the Debug Capability. Note that the fields in this register function differently than those in a normal *Port Status and Control Register* (described in section 5.4.8) because the Root Hub port assigned to the Debug Capability is acting as an Upstream Facing Port, not a Downstream Facing Port.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 84A8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								CEC	PLC	PRC	RSVD_1			CSC	RSVD_2				PSPD				RSVD_3	PLS				PR	RSVD_4		PED	CCS

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
23	0b RW/C	**Port Config Error Change (CEC):** This flag indicates that the port failed to configure its link partner. • 0 = No change • 1 = Port Config Error detected Software shall clear this bit by writing a '1' to it. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22	0b RW/C	**Port Link Status Change (PLC):** This flag is set to '1' due to the following PLS transitions: • U0 -) U3 = Suspend signaling detected from Debug Host • U3 -) U0 = Resume complete • Polling -) Disabled = Training Error • Ux or Recovery -) Inactive = Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'. **Power Well:** Core
21	0b RW/C	**Port Reset Change (PRC):** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). • '0' = No change • '1' = Reset complete Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'. **Power Well:** Core
20:18	0h RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
17	0b RW/C	**Connect Status Change (CSC):** an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'. **Power Well:** Core
16:14	0h RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
13:10	0h RO	**Port Speed (PSPD):** This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases, this field shall indicate Undefined Speed. • 0 Undefined Speed • 1-15 Protocol Speed ID (PSI) Refer to the xHCI for USB specification for the definition of PSIs. Note: The Debug Capability does not support LS, FS, or HS operation. **Power Well:** Core
9	0b RO	**Reserved (RSVD_3):** Reserved. **Power Well:** Core
8:5	0h RO	**Port Link State (PLS):** This field reflects its current link state. This field is only relevant when a Debug Host is attached (Debug Port Number) '0'). • 0 = Link is in the U0 State • 1 = Link is in the U1 State • 2 = Link is in the U2 State • 3 = Link is in the U3 State (Device Suspended) • 4 = Link is in the Disabled State • 5 = Link is in the RxDetect State • 6 = Link is in the Inactive State • 7 = Link is in the Polling State • 8 = Link is in the Recovery State • 9 = Link is in the Hot Reset State • 15:10 = Reserved Note: Transitions between different states are not reflected until the transition is complete. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Port Reset (PR):** • '1' = Port is in Reset • '0' = Port is not in Reset This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'. **Power Well:** Core
3:2	0h RO	**Reserved (RSVD_4):** Reserved. **Power Well:** Core
1	0b RW	**Port Enabled/Disabled (PED):** • '1' = Enabled. • '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PED transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion of DCPORTSC PR, or by software. • 0 = Debug Capability Root Hub port is disabled. • 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = '0') the port's link shall enter the SS.Disabled state and remain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note: This bit is not affected by PORTSC PR bit transitions. This field is '0' if DCE or CCS are '0'. **Power Well:** Core
0	0b RO	**Current Connect Status (CCS):** • '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. • '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the *Connect Status Change* (CSC) field in the *Port Status Change Event* that was generated by a '0' to '1' transition of this bit. This flag is '0' if Debug Capability Enable (DCE) is '0'. **Power Well:** Core

18.7.198 Debug Capability Context Pointer Register (DCCP)—Offset 84B0h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 84B0h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

DCCPR | RSVD

Bit Range	Default & Access	Field Name (ID): Description
63:4	000000000 000000h RW	**Debug Capability Context Pointer Register (DCCPR):** This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'. **Power Well:** Core
3:0	0h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

18.7.199 Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 84B8h

The *Debug Capability Device Descriptor Register 1* identifies the Device Protocol and Vendor ID values that shall be reported by DbC in its Device Descriptor when it is enumerated by a Debug Host. Refer to section 9.6.1, Table 9-8 in the USB3 spec. This register shall be initialized before enabling the DbC (DCE = '1').

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 84B8h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

VID | RSVD | DBCPR

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Vendor ID (VID):** This field is presented by the Debug Device in the USB Device Descriptor *idVendor* field. **Power Well:** Core
15:8	00h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**DbC Protocol (DBCPR):** This field is presented by the Debug Device in the USB Interface Descriptor *bInterfaceProtocol* field. • 0 = Debug Target vendor defined • 1 = GNU Remote Debug Command Set supported • 2-255 = Reserved **Power Well:** Core

18.7.200 Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 84BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 84BCh

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DREV																PID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**Device Revision (DREV):** This field is presented by the Debug Device in the USB Device Descriptor bcdDevice field. **Power Well:** Core
15:0	0000h RW	**Product ID (PID):** This field is presented by the Debug Device in the USB Device Descriptor idProduct field. **Power Well:** Core

18.7.201 Debug Capability Descriptor Parameters (DCDP)—Offset 8530h

The *Debug Capability Device Descriptor Register 2* identifies the Device Revision and Product ID values that shall be reported by DbC in its Device Descriptor when it is enumerated by a Debug Host. Refer to section 9.6.1, Table 9-8 in the Universal Serial Bus 3.0 Specification.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8530h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (31:8), MPF (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
7:0	00h RW	**Max Power Field (MPF):** This field will be used by USB Debug Device to report maximum power consumption when the device is fully operational. This value is returned by bMaxPower field in response to Configuration Descriptor read from the debug device. Note: bU1DevExitLat and bU2DevExitLat fields returned in BOS Descriptor read will be taken from the corresponding fields from the Host Controller space. **Power Well:** Core

18.7.202 Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8538h

This register contains a number of fields that provide a specific level of configurability for the OUT DMA that is part of Debug Device logic. This configurability is above and beyond that defined in the xHCI specification.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8538h

MBAR Type: PCI Configuration Register (Size: 64 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (31:19), EN_ACK_FCA (18), RSVD_1 (17:14), EN_ACK_FIFO_ICA (13), RSVD_2 (12:9), CL_OWN_CS (8), RET_OD_ACK_CR (7), RSVD_3 (6), RET_ODCF_SM_IS (5), RET_ODRF_SM_IS (4), RET_ODRDF_SM_IS (3), RSVD_4 (2:0)

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
18	0b RW	**Enable ACK FIFO credit accounting (EN_ACK_FCA):** Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
17:14	0h RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
13	0b RW	**Enable ACK FIFO ICA mechanisms (EN_ACK_FIFO_ICA):** Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP **Power Well:** Core
12:9	0h RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
8	0b RW	**Clear ownership of context semaphore (CL_OWN_CS):** Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines **Power Well:** Core
7	0b RW	**Return OD ACK credits (RET_OD_ACK_CR):** Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports **Power Well:** Core
6	0b RO	**Reserved (RSVD_3):** Reserved. **Power Well:** Core
5	0b RW	**Return ODCF SM to idle state (RET_ODCF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state **Power Well:** Core
4	0b RW	**Return ODRF SM to idle state (RET_ODRF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state **Power Well:** Core
3	0b RW	**Return ODRDF SM to idle state (RET_ODRDF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state **Power Well:** Core
2:0	0h RO	**Reserved (RSVD_4):** Reserved. **Power Well:** Core

18.8 USB EHCI PCI Configuration Registers

Table 214. Summary of USB EHCI PCI Configuration Registers—0/29/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–0h	1	"Vendor ID and Device ID (VID_DID)—Offset 0h" on page 2352	00008086h
4–4h	1	"Command and Device Status (CMD_STS)—Offset 4h" on page 2352	02900000h
8–Bh	4	"Revision ID and Programming Interface and Sub/Base Class Code (RID_PI_CC)—Offset 8h" on page 2355	0C032000h
C–Fh	4	"Reserved and Master Latency Timer and Header Type (RSVD_MLT_HT)—Offset Ch" on page 2356	00000000h
10–13h	4	"Memory Base Address (MBAR)—Offset 10h" on page 2357	00000000h
2C–2Fh	4	"USB2 Subsystem Vendor ID and USB2 Subsystem ID (SSVID_SSID)—Offset 2Ch" on page 2358	00000000h
34–37h	4	"Capabilities Pointer and Reserved (CAP_PTR_RSVD)—Offset 34h" on page 2358	00000050h
3C–3Fh	4	"Interrupt Line and Interrupt Pin and Reserved (ILINE_IPIN_RSVD)—Offset 3Ch" on page 2359	00000000h
50–53h	4	"PCI Power Management Capability ID and Next Item Pointer #1 and PM Capabilities (PM_CID_NEXT_CAP)—Offset 50h" on page 2359	C9C35801h
54–57h	4	"Power Management Control/Status (PM_CS)—Offset 54h" on page 2361	00000008h
58–5Bh	4	"Debug Port Capability ID and Next Item Pointer #2 and Debug Port Base Offset (DP_CID_NEXT_BASE)—Offset 58h" on page 2362	20A0980Ah
60–63h	4	"Serial Bus Release Number and Frame Length Adjustment and Port Wake Capability (SBRN_FLA_PWC)—Offset 60h" on page 2363	07FF2020h
64–67h	4	"Port Disable Override and RMH Device Removable (PDO_RMHDR)—Offset 64h" on page 2364	00000000h
68–6Bh	4	"USB2 Legacy Support Extended Capability (ULSEC)—Offset 68h" on page 2365	00000001h
6C–6Fh	4	"USB2 Legacy Support Control/Status (ULSCS)—Offset 6Ch" on page 2366	00000000h
70–73h	4	"Intel-Specific USB2 SMI (ISU2SMI)—Offset 70h" on page 2369	00000000h
74–77h	4	"OverCurrent Mapping (OCMAP)—Offset 74h" on page 2371	C0300C03h
7C–7Fh	4	"EHC Suspend Well Configuration and RMH Wake Control (EHCSUSCFGRMHWC)—Offset 7Ch" on page 2371	0000408Ch
F8–FBh	4	"Manufacturer's ID (MANID)—Offset F8h" on page 2374	00000F86h

18.8.1 Vendor ID and Device ID (VID_DID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:29, F:0] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

Bits 31:16	Bits 15:0
RSVD	VID_0

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15:0	8086h RO	**Vendor ID (VID_0):** 16-bit field which indicates company vendor as Intel. **Power Well:** Core

18.8.2 Command and Device Status (CMD_STS)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:29, F:0] + 4h

Default: 02900000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31	30	29	28	27	26:25	24	23	22	21	20	19	18:11	10	9	8	7	6	5	4	3	2	1	0
DPE_0	SSE_0	RMA_0	RTA_0	STA_0	DEVT_0	MDPED_0	FBCAP_0	UDF_0	CLKCAP_0	CAPLIST_0	INTRSTS_0	RSVD	INTRDIS_0	FBE_0	SERREN_0	WCC_0	PER_0	VGAPS_0	PMWE_0	SCE_0	BME_0	MSE_0	IOSE_0

Bit Range	Default & Access	Field Name (ID): Description
31	0b RWC	**Detected Parity Error (DPE_0):** This bit is set whenever a parity error is seen on the internal interface to the USB2 host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a '1' to this bit location. **Power Well:** Core
30	0b RWC	**Signaled System Error (SSE_0):** This bit is set whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. The following conditions can cause the generation of SERR#: a parity error is seen on address, command, or data (if the data was targeting the EHC) on the internal interface to the USB2 host controller due to a parity error on the system interface and bit 6 of the Command register is set to 1. An EHC-initiated memory read results in a completion packet with a status other than successful on the system interface (if SERR on Aborts Enable is also set) Software clears this bit by writing a '1' to this bit location. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29	0b RWC	**Received Master-Abort Status (RMA_0):** This bit is set when USB2, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit and the SERR on Aborts Enable (bit 3, offset 84h). Software clears this bit by writing a '1' to this bit location. **Power Well:** Core
28	0b RWC	**Received Target Abort Status (RTA_0):** This bit is set when USB2, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit and the SERR on Aborts Enable (bit 3, offset 84h). Software clears this bit by writing a '1' to this bit location. **Power Well:** Core
27	0b RO	**Signaled Target-Abort Status (STA_0):** This bit is used to indicate when the USB2 function responds to a cycle with a target abort. There is no reason for this to happen, so this bit will be hard-wired to '0'. Read-Only **Power Well:** Core
26:25	01b RO	**DEVSEL# Timing Status (DEVT_0):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only. **Power Well:** Core
24	0b RWC	**Master Data Parity Error Detected (MDPED_0):** This bit is set whenever a data parity error is detected on a USB2 read completion packet on the internal interface to the USB2 host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a '1' to this bit location. **Power Well:** Core
23	1b RO	**Fast Back-to-Back Capable (FBCAP_0):** Reserved as '1'. **Power Well:** Core
22	0b RO	**User Definable Features (UDF_0):** Reserved as '0' **Power Well:** Core
21	0b RO	**66 Mhz Capable (CLKCAP_0):** Reserved as '0' **Power Well:** Core
20	1b RO	**Capabilities List (CAPLIST_0):** Hardwired to '1' indicating that offset 34h contains a valid capabilities pointer. **Power Well:** Core
19	0b RO	**Interrupt Status (INTRSTS_0):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit. **Power Well:** Core
18:11	00000000b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0b RW	**Interrupt Disable (INTRDIS_0):** When cleared to '0', the function is capable of generating interrupts. When '1', the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable. This bit defaults to '0'. This bit is added as part of the PCI 2.3 Specification. **Power Well:** Core
9	0b RO	**Fast Back to Back Enable (FBE_0):** Reserved as '0'. **Power Well:** Core
8	0b RW	**SERR# Enable (SERREN_0):** on a memory read completion (if SERR on Aborts Enable is also set) Detection of an address or command parity error and the Parity Error Response bit is setDetection of a data parity error (when the data is going to the EHC) and the Parity Error Response bit is set **Power Well:** Core
7	0b RO	**Wait Cycle Control (WCC_0):** Reserved as '0'. **Power Well:** Core
6	0b RW	**Parity Error Response (PER_0):** When set to 1, the USB2 Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the EHCI specification. If it detects bad parity on the address or command phases when this bit is set to 1, the host controller does not take the cycle, halts the host controller (if currently not halted) and sets the host system error bit in the USBSTS register. Note that this applies to both requests and completions from the system interface. See section 9.19.2.4 for information regarding parity errors detected by the Prefetch DMA Engine. This bit must be set in order for the parity errors to generate SERR#. **Power Well:** Core
5	0b RO	**VGA Palette Snoop (VGAPS_0):** Reserved as '0' **Power Well:** Core
4	0b RO	**Postable Memory Write Enable (PMWE_0):** Reserved as '0' **Power Well:** Core
3	0b RO	**Special Cycle Enable (SCE_0):** Reserved as '0' **Power Well:** Core
2	0b RW	**Bus Master Enable (BME_0):** When set, bus mastering from EHCI is allowed, and will generate memory reads and writes for USB transfers. Notes on the EHC implementation: - Writes to change this bit occur immediately. Specifically, a write followed by a read will return the updated value. - When the BME bit is changed from 1 to 0, the EHC will cease accessing main memory within 2 microframes (250 usec). During this time, any number of reads and/or writes to memory may occur. - Clearing the BME bit shuts down the EHC DMA engines in the same manner that clearing the Run/Stop does. However, the schedule status bits and the HCHalted bit do not change based on the BME value. **Power Well:** Core
1	0b RW	**Memory Space Enable (MSE_0):** This bit controls access to the USB2 Memory Space registers. If this bit is set, accesses to the USB2 registers are enabled. The Base Address register for USB2 should be programmed before this bit is set. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0b RO	**I/O Space Enable (IOSE_0):** Reserved as '0'. **Power Well:** Core

18.8.3 Revision ID and Programming Interface and Sub/Base Class Code (RID_PI_CC)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 8h

Default: 0C032000h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
BCC_0								SCC_0								PI_0								RID_0							

Bit Range	Default & Access	Field Name (ID): Description
31:24	0Ch RO	**Base Class Code (BCC_0):** A value of 0Ch indicates that this is a Serial Bus controller. **Power Well:** Core
23:16	03h RO	**Sub Class Code (SCC_0):** A value of 03h indicates that this is a Universal Serial Bus Host Controller. **Power Well:** Core
15:8	20h RO	**Programming Interface (PI_0):** A value of 20h indicates that this USB2 Host Controller conforms to the EHCI specification. **Power Well:** Core
7:0	00h RO	**Revision ID (RID_0):** The value reported in this register indicates stepping of the host controller hardware. **Power Well:** Core

18.8.4 Reserved and Master Latency Timer and Header Type (RSVD_MLT_HT)—Offset Ch

Reserved, for padding Master Latency Timer Header Type Reserved

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:29, F:0] + Ch

Default: 00000000h

Bits	31:24	23	22:16	15:8	7:0
Value	0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	RSVD	MFB_0	CFG_LYT_0	MLT_0	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Multi Function Bit (MFB_0):** When set to 1 this indicates that this is a multifunction device. Default to 0 since EHCI is at function 0, no other function beyond. **Power Well:** Core
22:16	0000000b RO	**Configuration Layout (CFG_LYT_0):** Hardwired to 0 to indicate a standard PCI configuration layout. **Power Well:** Core
15:8	00h RO	**Master Latency Timer (MLT_0):** Because the USB2 controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0 **Power Well:** Core
7:0	00h RO	**Reserved (RSVD):** Reserved.

18.8.5 Memory Base Address (MBAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BA_0 (31:10)	RSVD (9:4)	PFETCH_0 (3)	TYPE_0 (2:1)	RTE_0 (0)

Bit Range	Default & Access	Field Name (ID): Description
31:10	000000h RW	**Base Address (BA_0):** Bits (31:10) correspond to memory address signals (31:10), respectively. This gives 1 KB of relocatable memory space aligned to 1 KB boundaries. **Power Well:** Core
9:4	000000b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Prefetchable (PFETCH_0):** Read Only. This bit is hardwired to 0 indicating that this range should not be prefetched. **Power Well:** Core
2:1	00b RO	**Type (TYPE_0):** indicating that this range can be mapped anywhere within 32-bit address space. **Power Well:** Core
0	0b RO	**Resource Type Indicator (RTE_0):** Read Only. This bit is hardwired to 0 indicating that the base address field in this register maps to memory space **Power Well:** Core

18.8.6 USB2 Subsystem Vendor ID and USB2 Subsystem ID (SSVID_SSID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 2Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits 31:16	Bits 15:0
USB2SSID_0	USB2SVID_0

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/L	**USB2 Subsystem ID (USB2SSID_0):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). Writes to this register are enabled when the WRT_RDONLY bit (offset 80h, bit 0) is set to 1. Writes should be done as a single 16-bit cycle. Reset: none **Power Well:** Core
15:0	0000h RW/L	**USB2 Subsystem Vendor ID (USB2SVID_0):** This register, in combination with the USB2 Subsystem ID register, enables the operating system to distinguish each subsystem from the others. Writes to this register are enabled when the WRT_RDONLY bit (offset 80h, bit 0) is set to 1. Reset: none **Power Well:** Core

18.8.7 Capabilities Pointer and Reserved (CAP_PTR_RSVD)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 34h

Default: 00000050h

31	28	24	20	16	12	8	4	0
	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1	0 0 0 0

Bits 31:8	Bits 7:0
RSVD	CAP_PTR_0

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	50h RO	**Capabilities Pointer (CAP_PTR_0):** This register points to the starting offset of the USB2 capabilities ranges. **Power Well:** Core

18.8.8 Interrupt Line and Interrupt Pin and Reserved (ILINE_IPIN_RSVD)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 3Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																IPIN_0								ILINE_0							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15:8	00h RO	**Interrupt Pin (IPIN_0):** Bits 3:0 reflect the value programmed in the interrupt pin registers in chipset configuration space. Bits 7:4 are hardwired to 0000b. NOTE: As a single function device, only INTA# may be used while the other three interrupt lines have no meaning. (refer to PCI 3.0 spec section 2.2.6 Interrupt Pins) **Power Well:** Core
7:0	00h RW	**Interrupt line (ILINE_0):** This data is not used by the SOC. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to. Reset: core well and D3-to-D0. **Power Well:** Core

18.8.9 PCI Power Management Capability ID and Next Item Pointer #1 and PM Capabilities (PM_CID_NEXT_CAP)—Offset 50h

PCI Power Management Capabilities ID Next Item Pointer #1 Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 50h

Default: C9C35801h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	1	1	1	0	0	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1
RSVD					D2SUP_0	D1SUP_0	AUXCUR_0			DSI_0	RSVD	PMECLK_0	VERS_0			PM_NEXT_0								PM_CID_0							

Bit Range	Default & Access	Field Name (ID): Description
31:27	11001b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**D2_Support (D2SUP_0):** The D2 state is not supported. Reset: core well, but not D3-to-D0. **Power Well:** Core
25	0b RO	**D1_Support (D1SUP_0):** The D1 state is not supported. Reset: core well, but not D3-to-D0. **Power Well:** Core
24:22	111b RW/L	**Aux_Current (AUXCUR_0):** The USB2 SIP EHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known. **Power Well:** Core
21	0b RO	**DSI (DSI_0):** The Intel EHC reports 0, indicating that no device-specific initialization is required. Reset: core well, but not D3-to-D0. **Power Well:** Core
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**PME Clock (PMECLK_0):** The Intel EHC reports 0, indicating that no PCI clock is required to generate PME#. Reset: core well, but not D3-to-D0. **Power Well:** Core
18:16	011b RW/L	**Version (VERS_0):** Version: The Intel EHC reports 011, indicating that it complies with Revision 1.21 of the PCI Power Management Specification. Note: As contigency plan, the bit can be reverted by BIOS to 010b to support PCI PM Revision 1.1, by manipulating the offset80h Access Control register's WRT_RDONLY bit. **Power Well:** Core
15:8	58h RW/L	**Next Item Pointer #1 (PM_NEXT_0):** This register defaults to 58h, which indicates that the next capability registers begin at configuration offset 58h. This register is writable when the WRT_RDONLY bit is set. This allows BIOS to effectively hide the Debug Port capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of 58h implies Debug Port and FLR capabilities visible 98h implies Debug Port invisible, next capability is FLR 00h implies that both Debug port and FLR capability are hidden Note that this value is never expected to be programmed. Reset: core well, but not D3-to-D0 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	01h RO	**PCI Power Management Capability ID (PM_CID_0):** A value of 01h indicates that this is a PCI Power Management capabilities field. **Power Well:** Core

18.8.10 Power Management Control/Status (PM_CS)—Offset 54h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 54h

Default: 00000008h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
RSVD																PMESTS_0	DTScl_0		DTSel_0				PMEEN_0	RSVD				NO_SOFT_RESET	RSVD	PWRST_0	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15	0b RWC	**PME_Status (PMESTS_0):** This bit is set when the EHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded. **Power Well:** Resume
14:13	00b RO	**Data_Scale (DTScl_0):** because it does not support the associated Data register. **Power Well:** Resume
12:9	0h RO	**Data_Select (DTSel_0):** because it does not support the associated Data register. **Power Well:** Resume
8	0b RW	**PME_En (PMEEN_0):** A '1' enables the EHC to generate an internal PME signal when PME_Status is '1'. This bit must be explicitly cleared by the operating system each time it is initially loaded. **Power Well:** Resume
7:4	0000b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	1b RO	**No Soft Reset (NO_SOFT_RESET):** A '0' indicates device does perform an internal reset upon D3hot to D0 transition via software control of the PowerState bits. Configuration Context is lost. Full re-initialization sequence is needed to return the device to D0 Initialized.(Default to '1') Note: As contigency plan, the bit can be reverted by BIOS to 0, by manipulating the offset80h Access Control register?s WRT_RDONLY bit. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.
1:0	00b RW	**PowerState (PWRST_0):** This 2-bit field is used both to determine the current power state of EHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3hot state, the accesses to the EHC memory range must not be accepted; but the configuration space must still be accessible. When not in the D0 state, the generation of the interrupt output is blocked. Specifically, the PIRQ[H] is not asserted when not in the D0 state. When software changes this value from the D3hot state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function. **Power Well:** Resume

18.8.11 Debug Port Capability ID and Next Item Pointer #2 and Debug Port Base Offset (DP_CID_NEXT_BASE)—Offset 58h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 58h

Default: 20A0980Ah

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0	1	0
BARNUM_0			DPOFFSET_0													RSVD								DP_CID_0							

Bit Range	Default & Access	Field Name (ID): Description
31:29	001b RO	**BAR Number (BARNUM_0):** Read-Only. This field is hardwired to 001b to indicate the memory BAR at offset 10h in the EHCI configuration space. Reset: Not applicable. **Power Well:** Core
28:16	00A0h RO	**Debug Port Offset (DPOFFSET_0):** This field is hardwired to 0A0h to indicate that the debug port registers begin at offset A0h in the EHCI memory range. Reset: Not applicable. **Power Well:** Core
15:8	98h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0Ah RO	**Debug Port Capability ID (DP_CID_0):** This register is hardwired to 0Ah which indicates that this is the start of a Debug Port Capability structure. Reset: Not applicable. **Power Well:** Core

18.8.12 Serial Bus Release Number and Frame Length Adjustment and Port Wake Capability (SBRN_FLA_PWC)—Offset 60h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 60h

Default: 07FF2020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits 31:27	Bits 26:17	Bit 16	Bits 15:14	Bits 13:8	Bits 7:0
RSVD	PortWKCapMask_0	PortWKImp_0	RSVD	FLTV_0	SBRN_0

Bit Range	Default & Access	Field Name (ID): Description
31:27	00000b RO	**Reserved (RSVD):** Reserved.
26:17	3FFh RW	**Port Wake Up Capability Mask (PortWKCapMask_0):** Bit positions 1 through 8 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, position 2 port 2, etc. Are only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
16	1b RW	**Port Wake Implemented (PortWKImp_0):** A '1' in bit 0 indicates that this register is implemented to software. Are only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
15:14	00b RO	**Reserved (RSVD):** Reserved.
13:8	100000b RW	**Frame Length Timing Value (FLTV_0):** Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Are only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
7:0	20h RO	**Serial Bus Release Number (SBRN_0):** value of 20h indicates that this controller follows USB release 2.0 **Power Well:** Resume

18.8.13 Port Disable Override and RMH Device Removable (PDO_RMHDR)—Offset 64h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 64h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD							DRBM_0								RSVD									RSVD							

Bit Range	Default & Access	Field Name (ID): Description
31:25	0000000b RO	**Reserved (RSVD):** Reserved.
24:17	00h RW	**Device Removable Bit Map (DRBM_0):** A 1 in a given bit position in this field indicates that the corresponding downstream port of the RMH is connected to a non-removable device. A 0 indicates that the port is exposed to the user. Bits 8:1 are mapped to Ports 8:1. This bits control the value returned by the RMH in the Deviceremovable field of the Hub Descriptor. A 1 in a given bit position in this register will result in the corresponding bit in the DeviceRemovable field of the hub descriptor being set to 1 as well (indicating that the port is connected to a non-removable device). System BIOS is expected to set these values upon Boot and resume from Sx states. **Power Well:** Core
16:8	000000000 b RO	**Reserved (RSVD):** Reserved.
7:0	00h RO	**Reserved (RSVD):** Reserved.

18.8.14 USB2 Legacy Support Extended Capability (ULSEC)—Offset 68h

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**Offset:** [B:0, D:29, F:0] + 68h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
RSVD							HCOSOS_0	RSVD							HCBIOS_0	NxtEHCICapP_0								CapID_0							

Bit Range	Default & Access	Field Name (ID): Description
31:25	0000000b RO	**Reserved (RSVD):** Reserved.
24	0b RW	**HC OS Owned Semaphore (HCOSOS_0):** System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as clear. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
23:17	0000000b RO	**Reserved (RSVD):** Reserved.
16	0b RW	**HC BIOS Owned Semaphore (HCBIOS_0):** The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will clear this bit in response to a request for ownership of the EHCI controller by system software. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
15:8	00h RO	**Next EHCI Capability Pointer (NxtEHCICapP_0):** A value of 00h indicates that there are no EHCI Extended Capability structures in this device. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
7:0	01h RO	**Capability ID (CapID_0):** A value of 01h indicates that this EHCI Extended Capability is the Legacy Support Capability. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume

18.8.15 USB2 Legacy Support Control/Status (ULSCS)—Offset 6Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:29, F:0] + 6Ch

Default: 00000000h

Bit	31	30	29	28:22	21	20	19	18	17	16	15	14	13	12:6	5	4	3	2	1	0
Default	0	0	0	0000000	0	0	0	0	0	0	0	0	0	0000000	0	0	0	0	0	0
Field	SMIonBAR_0	SMIonPCICom_0	SMIonOSSC_0	RSVD	SMIonAA_0	SMIonHSE_0	SMIonFLR_0	SMIonPCD_0	SMIonUE_0	SMIoUSBC_0	SMIonBARE_0	SMIonPCICE_0	SMIonOSSOE_0	RSVD	SMIonAAE_0	SMIonHSEE_0	SMIonFLRE_0	SMIonPCE_0	SMIonUSBEE_0	SMIonUSBCE_0

Bit Range	Default & Access	Field Name (ID): Description
31	0b RWC	**SMI on BAR (SMIonBAR_0):** This bit is set to '1' whenever the Base Address Register (BAR) is written. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
30	0b RWC	**SMI on PCI Command (SMIonPCICom_0):** This bit is set to '1' whenever the PCI Command Register is written. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
29	0b RWC	**SMI on OS Ownership Change (SMIonOSSC_0):** This bit is set to '1' whenever the HC OS Owned Semaphore bit in the USB2 Legacy Support Extended Capability register transitions from 1 to a 0 or 0 to a 1. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
28:22	00h RO	**Reserved (RSVD):** Reserved.
21	0b RO	**SMI on Async Advance (SMIonAA_0):** Shadow bit of the Interrupt on Async Advance bit in the USB2STS register. To clear this bit system software must write a one to the Interrupt on Async Advance bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
20	0b RO	**SMI on Host System Error (SMIonHSE_0):** Shadow bit of Host System Error bit in the USB2STS. To clear this bit system software must write a one to the Host System Error bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
19	0b RO	**SMI on Frame List Rollover (SMIonFLR_0):** Shadow bit of Frame List Rollover bit in the USB2STS register. To clear this bit system software must write a one to the Frame List Rollover bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
18	0b RO	**SMI on Port Change Detect (SMIonPCD_0):** Shadow bit of Port Change Detect bit in the USB2STS register. To clear this bit system software must write a one to the Port Change Detect bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
17	0b RO	**SMI on USB Error (SMIonUE_0):** Shadow bit of USB Error Interrupt (USBERRINT) bit in the USB2STS register. To clear this bit system software must write a one to the USB Error Interrupt bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
16	0b RO	**SMI on USB Complete (SMIoUSBC_0):** Shadow bit of USB Interrupt (USBINT) bit in the USB2STS register. To clear this bit system software must write a one to the USB Interrupt bit in the USB2STS register. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
15	0b RW	**SMI on BAR Enable (SMIonBARE_0):** When this bit is '1' and SMIonBAR_0 is '1', then the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
14	0b RW	**SMI on PCI Command Enable (SMIonPCICE_0):** When this bit is '1' and SMI on PCI Command is '1', then the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
13	0b RW	**SMI on OS Ownership Enable (SMIonOSSOE_0):** When this bit is a one AND the OS Ownership Change bit is one, the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
12:6	00h RO	**Reserved (RSVD):** Reserved.
5	0b RW	**SMI on Async Advance Enable (SMIonAAE_0):** When this bit is a one, and the SMI on Async Advance bit is a one, the host controller will issue an SMI immediately. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
4	0b RW	**SMI on Host System Error Enable (SMIonHSEE_0):** When this bit is a one, and the SMI on Host System Error is a one, the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
3	0b RW	**SMI on Frame List Rollover Enable (SMIonFLRE_0):** When this bit is a one, and the SMI on Frame List Rollover bit is a one, the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
2	0b RW	**SMI on Port Change Enable (SMIonPCE_0):** When this bit is a one, and the SMI on Port Change Detect bit is a one, the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
1	0b RW	**SMI on USB Error Enable (SMIonUSBEE_0):** When this bit is a one, and the SMI on USB Error bit is a one, the host controller will issue an SMI immediately. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume
0	0b RW	**SMI on USB Complete Enable (SMIonUSBCE_0):** When this bit is a one, and the SMI on USB Complete bit is a one, the host controller will issue an SMI immediately. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition. **Power Well:** Resume

18.8.16 Intel-Specific USB2 SMI (ISU2SMI)—Offset 70h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + 70h

Default: 00000000h

Bits 31:22	21	20	19	18	17	16	15:6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0
SMIonPO1_0	SMIonPMCSR_0	SMIonAsync_0	SMIonPeriodic_0	SMIonCF_0	SMIonHCHalted_0	SMIonHCRst_0	SMIonPOEn_0	SMIonPMSCREn_0	SMIonAsyncEn_0	SMIonPeriodicEn_0	SMIonCFEn_0	SMIonHCHaltedEn_0	SMIonHCRstEn_0

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RWC	**SMI on PortOwner (SMIonPO1_0):** Bits 29:22 correspond to the Port Owner bits for ports 1 (22) through 8 (29). These bits are set to '1' whenever the associated Port Owner bits transition from 0-)1 or 1-)0. Software clears these bits by writing a one. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
21	0b RWC	**SMI on PMCSR (SMIonPMCSR_0):** This bit is set to '1' whenever software modifies the Power State bits in the Power Management Control/Status register. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
20	0b RWC	**SMI on Async (SMIonAsync_0):** This bit is set to '1' whenever the Async Schedule Enable bit transitions from 1-)0 or 0-)1. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
19	0b RWC	**SMI on Periodic (SMIonPeriodic_0):** This bit is set to '1' whenever the Periodic Schedule Enable bit transitions from 1-)0 or 0-)1. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
18	0b RWC	**SMI on CF (SMIonCF_0):** This bit is set to '1' whenever the Configure Flag transitions from 1-)0 or 0-)1. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
17	0b RWC	**SMI on HCHalted (SMIonHCHalted_0):** This bit is set to '1' whenever HCHalted transitions to '1' as a result of the Run/Stop bit being cleared. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
16	0b RWC	**SMI on HCReset (SMIonHCRst_0):** This bit is set to '1' whenever HCRESET transitions to '1'. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
15:6	000h RW	**SMI on PortOwner Enable (SMIonPOEn_0):** When any of these bits are '1' and the corresponding SMI on PortOwner bits are '1', then the host controller will issue an SMI. Unused ports should have their corresponding bits cleared. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
5	0b RW	**SMI on PMSCR Enable (SMIonPMSCREn_0):** When this bit is '1' and SMI on PMSCR is '1', then the host controller will issue an SMI. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
4	0b RW	**SMI on Async Enable (SMIonAsyncEn_0):** When this bit is '1 and SMI on Async is '1' , then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
3	0b RW	**SMI on Periodic Enable (SMIonPeriodicEn_0):** When this bit is '1 and SMI on Periodic is '1', then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
2	0b RW	**SMI on CF Enable (SMIonCFEn_0):** When this bit is '1' and SMI on CF is '1', then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
1	0b RW	**SMI on HCHalted Enable (SMIonHCHaltedEn_0):** When this bit is a '1' and SMI on HCHalted is '1', then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume
0	0b RW	**SMI on HCReset Enable (SMIonHCRstEn_0):** When this bit is a '1' and SMI on HCHalted is '1', then the host controller will issue an SMI. This register is implemented in the Suspend Well. This register is only reset by the resume power well going low. It is not reset by the core power well going low or by a D3-to-D0 state transition **Power Well:** Resume

18.8.17 OverCurrent Mapping (OCMAP)—Offset 74h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:29, F:0] + 74h

Default: C0300C03h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1
OCMAPD_0								OCMAPC_0								OCMAPB_0								OCMAPA_0							

Bit Range	Default & Access	Field Name (ID): Description
31:24	C0h RW	**OC Mapping D (OCMAPD_0):** Each bit position maps OC4, for EHCI1 to a set of ports as follows: The OC4 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. **Power Well:** Resume
23:16	30h RW	**OC Mapping C (OCMAPC_0):** OC Mapping C. Each bit position maps OC3, for EHCI1 to a set of ports as follows: The OC3 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. **Power Well:** Resume
15:8	0Ch RW	**OC Mapping B (OCMAPB_0):** OC Mapping B. Each bit position maps OC2, for EHCI1 to a set of ports as follows: The OC2 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. **Power Well:** Resume
7:0	03h RW	**OC Mapping A (OCMAPA_0):** OC Mapping A: Each bit position maps OC1, for EHCI1 to a set of ports as follows: The OC1 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. **Power Well:** Core

18.8.18 EHC Suspend Well Configuration and RMH Wake Control (EHCSUSCFGRMHWC)—Offset 7Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:29, F:0] + 7Ch

Default: 0000408Ch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	1	0	0
RSVD							RMHIEWCS_0	RSVD				RMHUWDR_0	RMHUWOCD_0	RMHUWDD_0	RMHUWCE_0	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:25	0000000b RO	**Reserved (RSVD):** Reserved.
24	0b RW	**RMH Inherit EHCI Wake Control Settings (RMHIEWCS_0):** When this bit is set, the RMH behaves as if bits 2:0 of this register reflect the appropriate bits of EHCI PORTSC0 bits 22:20. **Power Well:** Resume
23:20	0000b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**RMH Upstream Wake on Device Resume (RMHUWDR_0):** This bit governs the hub behavior when globally suspended. When this bit is 0 it enables the port to be sensitive to device initiated resume events as system wake-up events. i.e, the hub will initiate a resume on its upstream port and cause a wake when a device resume occurs on an enabled DS port When this bit is set to 1 and a device resume event is seen on a downstream port, the hub does not initiate a wake upstream and does not cause a wake. **Power Well:** Resume
18	0b RW	**RMH Upstream Wake on OC Disable (RMHUWOCD_0):** This bit governs the hub behavior when globally suspended. When this bit is 0 it enables the port to be sensitive to overcurrent conditions as system wake-up events. i.e,, the hub will initiate a resume on its upstream port and cause a wake when an OC condition occurs on an enabled DS port When this bit is set to 1 and an over current event is seen, the hub does not initiate a wake upstream and does not cause a wake. **Power Well:** Resume
17	0b RW	**RMH Upstream Wake on Disconnect Disable (RMHUWDD_0):** This bit governs the hub behavior when globally suspended. When this bit is set to 0, the globally suspended hub treats disconnect events on downstream port as resume events to be propagated upstream. In this case, it is allowed to initiate a wake on its upstream por and cause a system wake in response to a disconnect event on a downstream port When this bit is set to 1, and the hub is globally suspended, the hub does not initiate a resume on its upstream port or cause a resume when a disconnect event occurs on a downstream port. **Power Well:** Resume
16	0b RW	**RMH Upstream Wake on Connect Enable (RMHUWCE_0):** This bit governs the hub behavior when globally suspended. When this bit is set to 0, and the hub is globally suspended, the hub treats connect events on a downstream port as resume events to be propagated upstream. As well as waking up the system. When this bit is set to 1,and the hub is globally suspended, the hub does not wake the system nor does it initiate a resume on its upstream port when a connect event occurs on a downstream port. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Reserved (RSVD):** Reserved.
14	1b RO	**Reserved (RSVD):** Reserved.
13	0b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11:10	00b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	1b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	1b RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

18.8.19 Manufacturer's ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:29, F:0] + F8h

Default: 00000F86h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1	0
RSVD				DPID_0				MSID_0								MAN_0								PPID_0							

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD):** Reserved.
27:24	0h RO	**Dot portion of Process ID (DPID_0):** Dot portion of Process ID: Indicates the dot Note: Process is reflected in bits [7:0] This is SIP customer implementation specific and SIP customer need to tie off the field accordingly. **Power Well:** Core
23:16	00h RO	**Manufacturing Stepping Identifier (MSID_0):** Stepping ID: This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. This is SIP customer implementation specific and SIP customer need to tie off the field accordingly. Implementation Note: A single Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step. **Power Well:** Core
15:8	0Fh RO	**Manufacturer (MAN_0):** 0Fh = Intel **Power Well:** Core
7:0	86h RO	**Process portion of process ID (PPID_0):** Process portion of process ID: Indicates the process. Note: Dot is reflected in bits [27:24] This is SIP customer implementation specific and SIP customer need to tie off the field accordingly. Implementation Note: It is recommended that the Manufacturing ID is implemented in one place and readable from all functions. This minimizes the changes required for a process shrink. **Power Well:** Core

18.9 USB EHCI Memory Mapped IO Registers

Table 215. Summary of USB EHCI Memory Mapped I/O Registers—MBAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–0h	1	"Capability Registers Length and HC Interface Version Number (CAP_HCIV)—Offset 0h" on page 2376	01000020h
4–4h	1	"Host Controller Structural Parameters (HCSPARAMS)—Offset 4h" on page 2377	00200008h
8–Bh	4	"Host Controller Capability Parameters (HCCPARAMS)—Offset 8h" on page 2379	00036881h
20–23h	4	"USB2 Command Register (USB2CMD)—Offset 20h" on page 2380	00080000h
24–27h	4	"USB2 Status (USB2STS)—Offset 24h" on page 2383	00001000h
28–2Bh	4	"USB2 Interrupt Enable (USB2INTR)—Offset 28h" on page 2385	00000000h
2C–2Fh	4	"Frame Index (FRINDEX)—Offset 2Ch" on page 2387	00000000h
30–33h	4	"Control Data Structure Segment Register (CTRLDSSEGMENT)—Offset 30h" on page 2387	00000000h
34–37h	4	"Periodic Frame List Base Address (PERIODICLISTBASE)—Offset 34h" on page 2388	00000000h
38–3Bh	4	"Current Asynchronous List Address (ASYNCLISTADDR)—Offset 38h" on page 2388	00000000h
60–63h	4	"Configure Flag Register (CONFIGFLAG)—Offset 60h" on page 2389	00000000h
64–67h	4	"Port Status and Control (PORTSC1)—Offset 64h" on page 2391	00003000h
68–6Bh	4	"Port Status and Control (PORTSC2)—Offset 68h" on page 2395	00003000h
6C–6Fh	4	"Port Status and Control (PORTSC3)—Offset 6Ch" on page 2400	00003000h
70–73h	4	"Port Status and Control (PORTSC4)—Offset 70h" on page 2404	00003000h
74–77h	4	"Port Status and Control (PORTSC5)—Offset 74h" on page 2409	00003000h
78–7Bh	4	"Port Status and Control (PORTSC6)—Offset 78h" on page 2413	00003000h
7C–7Fh	4	"Port Status and Control (PORTSC7)—Offset 7Ch" on page 2418	00003000h
80–83h	4	"Port Status and Control (PORTSC8)—Offset 80h" on page 2422	00003000h
A0–A0h	1	"Debug Port Control/Status Register (DP_CTRLSTS)—Offset A0h" on page 2427	00000000h
A4–A4h	1	"USB PIDs Register (DP_USB_PIDs)—Offset A4h" on page 2429	00000000h

Table 215. Summary of USB EHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A4-A4H	1	"USB PIDs Register (DP_USB_PIDs)—Offset A4h" on page 2429	00000000h
A8–AFh	8	"Debug Port Data Buffer Bytes 7:0 (DP_DATA_BUF_B)—Offset A8h" on page 2431	0000000000000000h
B0–B3h	4	"Debug Port Config Register (DP_CFG)—Offset B0h" on page 2432	00007F01h
4113- 4413h	4	"USB Test Per Port Register 1 (USB2_TEST_PERPORT_REG1_LANE0/1/2/3) - Offset 4113h/4213h/4313h/4413h" on page 2432	00000000h
4213- 4423h	4	"Per Port RCOMP High Speed Pull down Register (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_LANE0/1/2/3) - Offset 4123h/4223h/4323h/4423h" on page 2433	00000011h
4126- 4426h	4	"USB Per Port (USB2_PER_PORT_2_LANE0/1/2/3) - Offset 4126h/4226h/4326h/4426h" on page 2433	00001249h

18.9.1 Capability Registers Length and HC Interface Version Number (CAP_HCIV)—Offset 0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 01000020h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 0 | 0 0 0 0

Bits 31:16	Bits 15:8	Bits 7:0
HCIVERSION_B0_0	RSVD	CAPLENGTH_0

Bit Range	Default & Access	Field Name (ID): Description
31:16	0100h RO	**Host Controller Interface Version Number (HCIVERSION_B0_0):** This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms. **Power Well:** Core
15:8	00h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	20h RO	**Capability Registers Length (CAPLENGTH_0):** This register is used as an offset to add to the Memory Base Register to find the beginning of the Operational Register Space. This is fixed at 20h, indicating that the Operation Registers begin at offset 20h. **Power Well:** Resume

18.9.2 Host Controller Structural Parameters (HCSPARAMS)—Offset 4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00200008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
RSVD								DP_N_0				RSVD			RSVD	N_CC_0				N_PCC_0				PRR_0	RSVD		RSVD	NPORTS_0			

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved (RSVD):** Reserved.
23:20	2h RO	**Debug Port Number (DP_N_0):** Hardwired to 2h, indicating that the Debug Port is on the 2nd port on the EHC. This register is only reset by the resume power well going low. It is not reset by a D3-to-D0 state transition or HCRESET (Host Controller Reset) **Power Well:** Resume
19:17	000b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Number of Companion Controllers (N_CC_0):** This field indicates the number of companion controllers associated with this USB 2.0 host controller. A zero in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value larger than one in this field indicates there are companion USB 1.1 host controller(s). Port-ownership hand-offs are supported. High, Full- and Low-speed devices are supported on the host controller root ports. There are no companion controllers. This field is set to '0' as Read-Only bit. **Power Well:** Core
11:8	0h RO	**Number of Ports per Companion Controller (N_PCC_0):** This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software. Read-Only. This register is only reset by the resume power well going low. It is not reset by a D3-to-D0 state transition or HCRESET (Host Controller Reset) **Power Well:** Core
7	0b RO	**Port Routing Rules (PRR_0):** This field indicates the method used by this implementation for how all ports are mapped to companion controllers. This is hardwired to 0, indicating that the first N_PCC (=2) ports are routed to the lowest numbered function companion host controller, the next N_PCC ports are routed to the next lowest function companion controller, and so on **Power Well:** Resume
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3:0	8h RW	**N_PORTS (NPORTS_0):** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1H to FH. The default value for the EHCI controller indicates 8 ports. BIOS may overwrite the default value to properly describe the board or chip SKU . (please refer to RMH Configuration Details in section 1.23.2). A zero in this field is undefined. Integrated RMH - If USBr is disabled, this should be updated by BIOS to 2 such that the EHC reports 2ports to be default, port 0 assigned to the RMH and port 1 assigned to the debug device. If USB-R is enabled, the number reported should be updated to 3 by BIOS (port 2 will be assigned to USB-R in this case) Legacy Mode - The default value for the EHCI controller indicates 8 ports. If USB-R support is enabled, BIOS should account for the additional ports in calculating the value to write to this field. **Power Well:** Resume

18.9.3 Host Controller Capability Parameters (HCCPARAMS)—Offset 8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00036881h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	1
RSVD														ASPFC_0	PSPFC_0	EECP_0								IST_0				RSVD	ASPC_0	PFLF_0	AC64_0

Bit Range	Default & Access	Field Name (ID): Description
31:18	00000000000000b RO	**Reserved (RSVD):** Reserved.
17	1b RW	**Asynchronous Schedule Prefetch Capability (ASPFC_0):** This bit indicates that tthe hardware support the Asynch schedule prefetch enable bit in the USB command register. **Power Well:** Resume
16	1b RW	**Periodic Schedule Prefetch Capability (PSPFC_0):** This bit indicates that the EHC hardware supports the Periodic Schedule prefetch bit in the USB2 Command Register. **Power Well:** Core
15:8	68h RO	**EHCI Extended Capabilities Pointer (EECP_0):** This field is hardwired to 68h, indicating that the EHCI capabilities list exists and begins at offset 68h in the PCI configuration space. **Power Well:** Resume
7:4	8h RO	**Isochronous Scheduling Threshold (IST_0):** This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit [7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame. Refer to the EHCI specification for details on how software uses this information for scheduling isochronous transfers. The Intel USB2 hardwires this field to 8h. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Asynchronous Schedule Park Capability (ASPC_0):** This bit is hardwired to 0 indicating that the Host Controller does not support this optional feature. **Power Well:** Resume
1	0b RO	**Programmable Frame List Flag (PFLF_0):** If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and must be set to zero. If set to a one, then system software can specify and use a smaller frame list and configure the host controller via the USBCMD register Frame List Size field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous. The Intel EHC does not support different frame list lengths. This bit is read-only '0'. **Power Well:** Core
0	1b RO	**64-bit Addressing Capability (AC64_0):** This field documents the addressing range capability of this implementation. The value of this field determines whether software should use the 32-bit or 64-bit data structures. Values for this field have the following interpretation:0b data structures using 32-bit address memory pointers; 1b data structures using 64-bit address memory pointers The USB2 SIP supports 64-bit addressing only. This bit is read-only '1'. **Power Well:** Resume

18.9.4 USB2 Command Register (USB2CMD)—Offset 20h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 20h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00080000h

Bits	31:24	23:16	15:14	13	12	11:8	7	6	5	4	3:2	1	0
Default	0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0	0 0	0	0	0 0 0 0	0	0	0	0	0 0	0	0
Field	RSVD	ITC_0	RSVD	RSVD	RSVD	UAPMB_0	LHCR_0	IAAD_0	ASE_0	PSE_0	FLS_0	HCRESET_0	RS_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved (RSVD):** Reserved.
23:16	08h RW	**Interrupt Threshold Control (ITC_0):** This field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. Value Maximum Interrupt Interval 00h Reserved 01h 1 micro-frame 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames (default, equates to 1 ms) 10h 16 micro-frames (2 ms) 20h 32 micro-frames (4 ms) 40h 64 micro-frames (8 ms) Refer to Section 4 in the EHCI specification for interrupts affected by this field. **Power Well:** Core
15:14	00b RO	**Reserved (RSVD):** Reserved.
13	0b RO	**Reserved (RSVD):** Reserved.
12	0h RO	**Reserved (RSVD):** Reserved.
11:8	0h RO	**Unimplemented Asynchronous Park Mode Bits (UAPMB_0):** This field is hardwired to 000b because the host controller does not support this optional feature. **Power Well:** Core
7	0b RO	**Light Host Controller Reset (LHCR_0):** Read Only 0b. The Intel EHC does not implement this optional reset and hardwires this bit to 0. **Power Well:** Core
6	0b RW	**Interrupt on Async Advance Doorbell (IAAD_0):** This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state , it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold. See the EHCI specification for operational details. The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one. Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0b RW	**Asynchronous Schedule Enable (ASE_0):** This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean: 0b Do not process the Asynchronous Schedule 1b Use the ASYNCLISTADDR register to access the Asynchronous Schedule. **Power Well:** Core
4	0b RW	**Periodic Schedule Enable (PSE_0):** This bit controls whether the host controller skips processing the Periodic Schedule. Values mean: 0b Do not process the Periodic Schedule 1b Use the PERIODICLISTBASE register to access the Periodic Schedule. **Power Well:** Core
3:2	00b RO	**Frame List Size (FLS_0):** This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. . This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean:00b 1024 elements (4096 bytes) Default value; 01b 512 elements (2048 bytes); 10b 256 elements (1024 bytes) - for resource-constrained environments **Power Well:** Core
1	0b RW	**Host Controller Reset (HCRESET_0):** This control bit used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. Note: PCI Configuration registers and Host Controller Capability Registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership will be disowned by the host controller(s), with the side effects described in the EHCI spec. Software must reinitialize the host controller in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HCHalted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior. This reset must be used to leave EHCI port test modes. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Run/Stop (RS_0):** 1=Run. 0=Stop. When set to a 1, the Host Controller proceeds with execution of the schedule. The Host Controller continues execution as long as this bit is set to a 1. When this bit is set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 microframes after software clears the Run bit. The HC Halted bit in the status register indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software should not write a 1 to this field unless the host controller is in the Halted state (i.e. HCHalted in the USBSTS register is a one). The following table explains how the different combinations of Run and Halted must be interpreted: Run/Stop Halted Interpretation 0 0 Valid- in the process of halting 0 1 Valid- halted 1 0 Valid- running 1 1 Invalid- the HCHalted bit clears immediately Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being cleared (and also affect the Host Error bit). **Power Well:** Core

18.9.5 USB2 Status (USB2STS)—Offset 24h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 24h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00001000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																ASS_0	PSS_0	RECL_0	HCHALT_0	RSVD						IAA_0	HSE_0	FLR_0	PCD_0	USBERRINT_0	USBINT_0

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0b RO	**Asynchronous Schedule Status (ASS_0):** This bit reports the current real status of the Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0). **Power Well:** Core
14	0b RO	**Periodic Schedule Status (PSS_0):** This bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0). The Prefetch-Based Pause feature prevents this bit from transitioning to 0 if it currently has a request pending, in addition to the regular Periodic DMA engine. **Power Well:** Core
13	0b RO	**Reclamation (RECL_0):** This is a read-only status bit, which is used to detect an empty asynchronous schedule. The operational model and valid transitions for this bit are described in Section 4 of the EHCI Specification. **Power Well:** Core
12	1b RO	**HCHalted (HCHALT_0):** This bit is a zero whenever the Run/Stop bit is a one. The Host Controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware (e.g. internal error). The Prefetch-Based Pause feature prevents this bit from transitioning to 0 if it is currently has a request pending, in addition to the regular DMA engines. **Power Well:** Core
11:6	000000b RO	**Reserved (RSVD):** Reserved.
5	0b RWC	**Interrupt on Async Advance (IAA_0):** System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0b RWC	**Host System Error (HSE_0):** The Host Controller sets this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being set. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system (if enabled in the Interrupt Enable Register). **Power Well:** Core
3	0b RWC	**Frame List Rollover (FLR_0):** The Host Controller sets this bit to a one when the Frame List Index (see Section 9.3.2.4) rolls over from its maximum value to zero. Since the USB2 SIP only supports the 1024-entry Frame List Size, the Frame List Index rolls over every time FRNUM[13] toggles. **Power Well:** Core
2	0b RWC	**Port Change Detect (PCD_0):** The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to a one after system software has relinquished ownership of a connected port by writing a zero to a port's Port Owner bit. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, over-current change, enable/disable change and connect status change). Regardless of the implementation, whenever this bit is readable (i.e., in the D0 state), it must provide a valid view of the Port Status registers. **Power Well:** Core
1	0b RWC	**USB Error Interrupt (USBERRINT_0):** The Host Controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set. See the EHCI specification for a list of the USB errors that will result in this interrupt being asserted. **Power Well:** Core
0	0b RWC	**USB Interrupt (USBINT_0):** The Host Controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes). **Power Well:** Core

18.9.6 USB2 Interrupt Enable (USB2INTR)—Offset 28h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 28h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																										IAAE_0	HSEE_0	FLRE_0	PCIE_0	USBEIE_0	USBIE_0

Bit Range	Default & Access	Field Name (ID): Description
31:6	0000000h RO	**Reserved (RSVD):** Reserved.
5	0b RW	**Interrupt on Async Advance Enable (IAAE_0):** When this bit is a one, and the Interrupt on Async Advance bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit. **Power Well:** Core
4	0b RW	**Host System Error Enable (HSEE_0):** When this bit is a one, and the Host System Error Status bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit. **Power Well:** Core
3	0b RW	**Frame List Rollover Enable (FLRE_0):** When this bit is a one, and the Frame List Rollover bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit. **Power Well:** Core
2	0b RW	**Port Change Interrupt Enable (PCIE_0):** When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit. **Power Well:** Core
1	0b RW	**USB Error Interrupt Enable (USBEIE_0):** When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBERRINT bit. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**USB Interrupt Enable (USBIE_0):** When this bit is a one, and the USBINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBINT bit. **Power Well:** Core

18.9.7 Frame Index (FRINDEX)—Offset 2Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																		FLCIFN_0													

Bit Range	Default & Access	Field Name (ID): Description
31:14	000000000000000000b RO	**Reserved (RSVD):** Reserved.
13:0	00000000000000b RW	**Frame List Current Index/Frame Number (FLCIFN_0):** The value in this register increments at the end of each time frame (e.g. micro-frame). Bits (12:3) are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index **Power Well:** Core

18.9.8 Control Data Structure Segment Register (CTRLDSSEGMENT)—Offset 30h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 30h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

UPPADDR_0

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Upper Address[63 (UPPADDR_0):** 32]: This 32-bit field corresponds to address bits 63:32 when forming a control data structure address. **Power Well:** Core

18.9.9 Periodic Frame List Base Address (PERIODICLISTBASE)—Offset 34h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 34h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BALow_0 (31:12) | RSVD (11:0)

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BALow_0):** These bits correspond to memory address signals (31:12), respectively. **Power Well:** Core
11:0	000000000000b RO	**Reserved (RSVD):** Reserved.

18.9.10 Current Asynchronous List Address (ASYNCLISTADDR)—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 38h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LPL_0																											RSVD				

Bit Range	Default & Access	Field Name (ID): Description
31:5	0000000h RW	**Link Pointer Low (LPL_0):** These bits correspond to memory address signals (31:5), respectively. This field may only reference a Queue Head (QH). **Power Well:** Core
4:0	0000b RO	**Reserved (RSVD):** Reserved.

18.9.11 Configure Flag Register (CONFIGFLAG)—Offset 60h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 60h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																															CF_0

Bit Range	Default & Access	Field Name (ID): Description
31:1	00000000h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Configure Flag (CF_0):** Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. See section 4 of the EHCI spec for operation details. 0b Port routing control logic default-routes each port to the classic host controllers. 1b Port routing control logic default-routes all ports to this host controller. This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset. **Power Well:** Resume

18.9.12 Port Status and Control (PORTSC1)—Offset 64h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 64h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00003000h

Bits	31:23	22	21	20	19:16	15:14	13	12	11:10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0	0	0	0	0 0 0 0	0 0	1	1	0 0	0	0	0	0	0	0	0	0	0	0
Field	RSVD	WKOCE_P0_0	WKDSCNNTE_P0_0	WKCNNTE_P0_0	PTC_P0_0	PIC_P0_0	PO_P0_0	PP_P0_0	LS_P0_0	RSVD	PORTRST_P0_0	SUSP_P0_0	FPR_P0_0	OCC_P0_0	OCACT_P0_0	PEDC_P0_0	RSVD	CSC_P0_0	CCS_P0_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set. **Power Well:** Resume
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC setsthe PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0). **Power Well:** Resume
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1). **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one. **Power Well:** Resume
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior. **Power Well:** Resume
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details. **Power Well:** Resume
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power. **Power Well:** Resume
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared. **Power Well:** Resume
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. **Power Well:** Resume
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner. **Power Well:** Resume
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'. **Power Well:** Resume
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. **Power Well:** Resume
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. **Power Well:** Resume

18.9.13 Port Status and Control (PORTSC2)—Offset 68h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 68h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00003000h

Bits	Default	Field
31:23	0 0 0 0 0 0 0 0 0	RSVD
22	0	WKOCE_P0_0
21	0	WKDSCNNTE_P0_0
20	0	WKCNNTE_P0_0
19:16	0 0 0 0	PTC_P0_0
15:14	0 0	PIC_P0_0
13	1	PO_P0_0
12	1	PP_P0_0
11:10	0 0	LS_P0_0
9	0	RSVD
8	0	PORTRST_P0_0
7	0	SUSP_P0_0
6	0	FPR_P0_0
5	0	OCC_P0_0
4	0	OCACT_P0_0
3	0	PEDC_P0_0
2	0	RSVD
1	0	CSC_P0_0
0	0	CCS_P0_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC setsthe PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0). **Power Well:** Resume
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1). **Power Well:** Resume
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one. **Power Well:** Resume
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior. **Power Well:** Resume
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power. **Power Well:** Resume
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset **Power Well:** Resume
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. **Power Well:** Resume
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. **Power Well:** Resume
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'. **Power Well:** Resume
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. **Power Well:** Resume
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. **Power Well:** Resume

18.9.14 Port Status and Control (PORTSC3)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 6Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00003000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
RSVD									WKOCE_P0_0	WKDSCNNTE_P0_0	WKCNNTE_P0_0	PTC_P0_0				PIC_P0_0		PO_P0_0	PP_P0_0	LS_P0_0		RSVD	PORTRST_P0_0	SUSP_P0_0	FPR_P0_0	OCC_P0_0	OCACT_P0_0	PEDC_P0_0	RSVD	CSC_P0_0	CCS_P0_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set. **Power Well:** Resume
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC setsthe PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0). **Power Well:** Resume
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1). **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one. **Power Well:** Resume
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior. **Power Well:** Resume
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details. **Power Well:** Resume
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power. **Power Well:** Resume
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared. **Power Well:** Resume
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. **Power Well:** Resume
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner. **Power Well:** Resume
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'. **Power Well:** Resume
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. **Power Well:** Resume
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. **Power Well:** Resume

18.9.15 Port Status and Control (PORTSC4)—Offset 70h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 70h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00003000h

Bits	Default	Field
31:23	0 0 0 0 0 0 0 0 0	RSVD
22	0	WKOCE_P0_0
21	0	WKDSCNNTE_P0_0
20	0	WKCNNTE_P0_0
19:16	0 0 0 0	PTC_P0_0
15:14	0 0	PIC_P0_0
13	1	PO_P0_0
12	1	PP_P0_0
11:10	0 0	LS_P0_0
9	0	RSVD
8	0	PORTRST_P0_0
7	0	SUSP_P0_0
6	0	FPR_P0_0
5	0	OCC_P0_0
4	0	OCACT_P0_0
3	0	PEDC_P0_0
2	0	RSVD
1	0	CSC_P0_0
0	0	CCS_P0_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC setsthe PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0). **Power Well:** Resume
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1). **Power Well:** Resume
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one. **Power Well:** Resume
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior. **Power Well:** Resume
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power. **Power Well:** Resume
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset **Power Well:** Resume
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. **Power Well:** Resume
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. **Power Well:** Resume
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'. **Power Well:** Resume
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. **Power Well:** Resume
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. **Power Well:** Resume

18.9.16 Port Status and Control (PORTSC5)—Offset 74h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 74h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00003000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:23	RSVD
22	WKOCE_P0_0
21	WKDSCNNTE_P0_0
20	WKCNNTE_P0_0
19:16	PTC_P0_0
15:14	PIC_P0_0
13	PO_P0_0
12	PP_P0_0
11:10	LS_P0_0
9	RSVD
8	PORTRST_P0_0
7	SUSP_P0_0
6	FPR_P0_0
5	OCC_P0_0
4	OCACT_P0_0
3	PEDC_P0_0
2	RSVD
1	CSC_P0_0
0	CCS_P0_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set. **Power Well:** Resume
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC setsthe PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0). **Power Well:** Resume
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1). **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one. **Power Well:** Resume
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior. **Power Well:** Resume
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details. **Power Well:** Resume
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power. **Power Well:** Resume
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared. **Power Well:** Resume
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. **Power Well:** Resume
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner. **Power Well:** Resume
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'. **Power Well:** Resume
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. **Power Well:** Resume
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. **Power Well:** Resume

18.9.17 Port Status and Control (PORTSC6)—Offset 78h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 78h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00003000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
RSVD									WKOCE_P0_0	WKDSCNNTE_P0_0	WKCNNTE_P0_0	PTC_P0_0				PIC_P0_0		PO_P0_0	PP_P0_0	LS_P0_0		RSVD	PORTRST_P0_0	SUSP_P0_0	FPR_P0_0	OCC_P0_0	OCACT_P0_0	PEDC_P0_0	RSVD	CSC_P0_0	CCS_P0_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC setsthe PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0). **Power Well:** Resume
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1). **Power Well:** Resume
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one. **Power Well:** Resume
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior. **Power Well:** Resume
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power. **Power Well:** Resume
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset **Power Well:** Resume
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. **Power Well:** Resume
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. **Power Well:** Resume
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'. **Power Well:** Resume
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. **Power Well:** Resume
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. **Power Well:** Resume

18.9.18 Port Status and Control (PORTSC7)—Offset 7Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 7Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00003000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
RSVD									WKOCE_P0_0	WKDSCNNTE_P0_0	WKCNNTE_P0_0	PTC_P0_0				PIC_P0_0		PO_P0_0	PP_P0_0	LS_P0_0		RSVD	PORTRST_P0_0	SUSP_P0_0	FPR_P0_0	OCC_P0_0	OCACT_P0_0	PEDC_P0_0	RSVD	CSC_P0_0	CCS_P0_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set. **Power Well:** Resume
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC setsthe PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0). **Power Well:** Resume
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1). **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one. **Power Well:** Resume
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior. **Power Well:** Resume
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details. **Power Well:** Resume
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power. **Power Well:** Resume
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared. **Power Well:** Resume
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. **Power Well:** Resume
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner. **Power Well:** Resume
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'. **Power Well:** Resume
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. **Power Well:** Resume
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. **Power Well:** Resume

18.9.19 Port Status and Control (PORTSC8)—Offset 80h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + 80h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00003000h

Bits	Default	Field
31:23	0 0 0 0 0 0 0 0 0	RSVD
22	0	WKOCE_P0_0
21	0	WKDSCNNTE_P0_0
20	0	WKCNNTE_P0_0
19:16	0 0 0 0	PTC_P0_0
15:14	0 0	PIC_P0_0
13	1	PO_P0_0
12	1	PP_P0_0
11:10	0 0	LS_P0_0
9	0	RSVD
8	0	PORTRST_P0_0
7	0	SUSP_P0_0
6	0	FPR_P0_0
5	0	OCC_P0_0
4	0	OCACT_P0_0
3	0	PEDC_P0_0
2	0	RSVD
1	0	CSC_P0_0
0	0	CCS_P0_0

Bit Range	Default & Access	Field Name (ID): Description
31:23	000h RO	**Reserved (RSVD):** Reserved.
22	0b RW	**Wake on Over-current Enable (WKOCE_P0_0):** Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Over-current Active bit (bit 4 of this register) is set. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
21	0b RW	**Wake on Disconnect Enable (WKDSCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. When enabled to do so, the EHC setsthe PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (i.e., bit 0 of this register changes from 1 to 0). **Power Well:** Resume
20	0b RW	**Wake on Connect Enable (WKCNNTE_P0_0):** Writing this bit to a one enables the port to be sensitive to device connects as wake-up events. When enabled to do so, the EHC sets the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (i.e., bit 0 of this register changes from 0 to 1). **Power Well:** Resume
19:16	0h RW	**Port Test Control (PTC_P0_0):** When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b - 1111b are reserved): Bits Test Mode 0000b Test mode not enabled 0001b Test J_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0010b Test K_STATE- During this test mode the hardware forces pre-emphasis disabled to the AFE if bit 29 of the USB2 Safe Mode Register is set (config offset FCh.bit 29) 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE Refer to USB Specification Revision 2.0, Chapter 7 and the EHCI specification, Chapter 4 for details on each test mode. The EHC does not support the option to run the port tests while the Run/Stop bit is a one. **Power Well:** Resume
15:14	00b RW	**Port Indicator Control (PIC_P0_0):** Writing to these bits directly controls the corresponding LED output pins. Bit 15 is inverted to generate USBLEDG#(n) where n is the port number. Bit 14 is inverted to generate USBLEDA#(n). Software is responsible for controlling these as specified in the USB Specification Revision 2.0. Bit Value Meaning 00b Port indicators are off 01b Amber 10b Green 11b Undefined The Intel EHC only supports bit value of 00b. Other values will result in unspecified behavior. **Power Well:** Resume
13	1b RW	**Port Owner (PO_P0_0):** This bit unconditionally goes to a 0b when the Configure Flag makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configure Flag bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
12	1b RO	**Port Power (PP_P0_0):** Hard-wired with a value of '1' on the Intel EHC. This indicates that the port does have power. **Power Well:** Resume
11:10	00b RO	**Line Status (LS_P0_0):** These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: Bits(11:10) USB State Interpretation 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset **Power Well:** Resume
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RW	**Port Reset (PORTRST_P0_0):** 1=Port is in Reset. 0=Port is not in Reset. Default = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to guarantee the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detets that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero. The HCHalted bit in the USB2STS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HCHALTED bit is a one. The Run/Stop bit in the Command Register must be set in order for the Port Reset bit to be cleared. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
7	0b RW	**Suspend (SUSP_P0_0):** 1=Port in suspend state. 0=Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to a 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:Software sets the Force Port Resume bit to a zero (from a one). Software sets the Port Reset bit to a one (from a zero). If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero) the results are undefined. **Power Well:** Resume
6	0b RW	**Force Port Resume (FPR_P0_0):** 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. **Power Well:** Resume
5	0b RWC	**Over-current Change (OCC_P0_0):** This bit gets set to a one when there is a change to the Over-current Active bit. Software clears this bit by writing a one to this bit position. The functionality of this bit is not dependent upon the port owner. **Power Well:** Resume

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Over-current Active (OCACT_P0_0):** 1=This port currently has an over-current condition. 0=This port does not have an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The functionality of this bit is not dependent upon the port owner. The Intel EHC automatically disables the port when the over-current active bit is '1'. **Power Well:** Resume
3	0b RWC	**Port Enable/Disable Change (PEDC_P0_0):** 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. **Power Well:** Resume
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RWC	**Connect Status Change (CSC_P0_0):** 1=Change in Current Connect Status. 0=No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. **Power Well:** Resume
0	0b RO	**Current Connect Status (CCS_P0_0):** 1=Device is present on port. 0=No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. **Power Well:** Resume

18.9.20 Debug Port Control/Status Register (DP_CTRLSTS)—Offset A0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + A0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	OWNERCNT_0	RSVD	ENABLEDCNT_0	RSVD											DONESTS_0	LINKIDSTS_0				RSVD	INUSECNT_0	EXCP_STS_0			ERRGOODSTS_0	GOCNT_0	WRRDCNT_0	DATALENCNT_0			

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RW	**OWNER_CNT (OWNERCNT_0):** When software writes a 1 to this bit, the ownership of the debug port is forced to the EHCI controller (i.e. immediately taken away from the companion Classic USB Host Controller) If the port was already owned by the EHCI controller, then setting this bit has no effect. This bit overrides all of the ownership-related bits in the standard EHCI registers. Note that the value in this bit does not affect the value reported in the PORTSC Port Owner bit. **Power Well:** Core
29	0b RO	**Reserved (RSVD):** Reserved.
28	0b RW	**ENABLED_CNT (ENABLEDCNT_0):** This bit = 1 if the debug port is enabled for operation. Software can clear this by writing a zero to it. The hardware clears the bit for the same conditions where hardware clears the Port Enable/Disable bit (in the PORTSC register). (Note this bit is not cleared when software clears the Port Enabled/Disabled bit in the PORTSC.) Software can directly set this bit if the port is already enabled in the associated Port Status and Control register (this is enforced by the hardware). Reset default = 0. **Power Well:** Core
27:17	00000000000b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
16	0b RWC	**DONE_STS (DONESTS_0):** Read/Write-Clear. This bit is set by hardware to indicate that the request is complete. Writing a 1 to this bit will clear it if it is set. Writing a 0 to this bit has no effect. Reset default = 0 **Power Well:** Core
15:12	0000b RO	**LINK_ID_STS (LINKIDSTS_0):** Read-Only. This field identifies the link interface. It is hardwired to 0h to indicate that it is a USB Debug Port. **Power Well:** Core
11	0b RO	**Reserved (RSVD):** Reserved.
10	0b RO	**IN_USE_CNT (INUSECNT_0):** Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software. This bit is cleared after reset. (This bit has no affect on hardware.) **Power Well:** Core
9:7	000b RO	**EXCEPTION_STS (EXCP_STS_0):** Read-Only. This field indicates the exception when the ERROR_GOOD#_STS bit is set. This field should be ignored if the ERROR_GOOD#_STS bit is 0. 000 No Error. Note: this should not be seen, since this field should only be checked if there is an erro. 001 Transaction error: indicates the USB2 transaction had an error (CRC, bad PID, timeout, etc.) 010 HW error. Request was attempted (or in progress) when port was suspended or reset. All Others are reserved Reset default = 000b **Power Well:** Core
6	0b RO	**ERROR_GOOD_STS (ERRGOODSTS_0):** Read-Only. The hardware clears this bit to 0 upon the proper completion of a read or write. The hardware sets this bit to indicate that an error has occurred. Details on the nature of the error are provided in the Exception field. Reset default = 0. **Power Well:** Core
5	0b RW	**GO_CNT (GOCNT_0):** Software sets this bit to cause the hardware to perform a read or write request. Writing a 0 to this bit has no effect. Writing a 1 to this bit when it is already set may result in undefined behavior. When set, the hardware clears this bit when the hardware sets the DONE_STS bit. Reset default = 0. **Power Well:** Core
4	0b RW	**WRITE_READ_CNT (WRRDCNT_0):** Software sets this bit to indicate that the current request is a write. Software clears this bit to indicate that the current request is a read. Reset default = 0. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0000b RW	**DATA_LEN_CNT (DATALENCNT_0):** This field is used to indicate the size of the data to be transferred. Reset default = 0h. For write operations, this field is set by software to indicate to the hardware how many bytes of data in Data Buffer are to be transferred to the console. A value of 0h indicates that a zero-length packet should be sent. A value of 1-8 indicates 1-8 bytes are to be transferred. Values 9-Fh are illegal and how hardware behaves if used is undefined. For read operations, this field is set by hardware to indicate to software how many bytes in Data Buffer are valid in response to a read operation. A value of 0h indicates that a zero length packet was returned and the state of Data Buffer is not defined. A value of 1-8 indicates 1-8 bytes were received. Hardware is not allowed to return values 9-Fh. The transferring of data always starts with byte 0 in the data area and moves toward byte 7 until the transfer size is reached. **Power Well:** Core

18.9.21 USB PIDs Register (DP_USB_PIDs)—Offset A4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + A4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Field	RSVD		RECEIVED_PID_STS_0		SEND_PID_CNT_0		TOKEN_PID_CNT_0	

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	00h RO	**RECEIVED_PID_STS (RECEIVED_PID_STS_0):** The hardware updates this field with the received PID for transactions in either direction. When the controller is writing data, this field is updated with the handshake PID that is received from the device. When the host controller is reading data, this field is updated with the data packet PID (if the device sent data), or the handshake PID (if the device NAKs the request). This field is valid when the hardware clears the GO_DONE#_CNT bit. Reset Default = 0. **Power Well:** Core
15:8	00h RW	**SEND_PID_CNT (SEND_PID_CNT_0):** The hardware sends this PID to begin the data packet when sending data to USB (ie. WRITE_READ#_CNT is asserted). Software will typically set this field to either DATA0 or DATA1 PID values. Reset Default = 0 **Power Well:** Core
7:0	00h RW	**TOKEN_PID_CNT (TOKEN_PID_CNT_0):** The hardware sends this PID as the Token PID for each USB transaction. Software will typically set this field to either IN, OUT or SETUP PID values. Reset Default = 0. **Power Well:** Core

18.9.22 Debug Port Data Buffer Bytes 7:0 (DP_DATA_BUF_B)—Offset A8h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + A8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

DATABUFFER_0

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RW	**DATABUFFER (DATABUFFER_0):** These are the 8 bytes of the data buffer. Bits 7:0 correspond to least significant byte (byte 0). Bits 63:56 correspond to the most significant byte (byte 7). The bytes in the Data Buffer must be written with data before software initiates a write request. For a read request, the Data Buffer contains valid data when DONE_STS is set by the hardware, ERROR_GOOD#_STS is cleared by the hardware, and the DATA_LENGTH_CNT field indicates the number of bytes that are valid. Reset Default = 0. **Power Well:** Core

18.9.23 Debug Port Config Register (DP_CFG)—Offset B0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [MBAR] + B0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:29, F:0] + 10h

Default: 00007F01h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1

Fields: RSVD (31:15), USB_ADDR_CNF_0 (14:8), RSVD (7:4), USB_ENDPT_CNF_0 (3:0)

Bit Range	Default & Access	Field Name (ID): Description
31:15	000000000 00000000b RO	**Reserved (RSVD):** Reserved.
14:8	7fh RW	**USB_ADDRESS_CNF (USB_ADDR_CNF_0):** 7-bit field that identifies the USB device address used by the controller for all Token PID generation. This is a R/W field that is set to 7Fh after reset **Power Well:** Core
7:4	0000b RO	**Reserved (RSVD):** Reserved.
3:0	01h RW	**USB_ENDPOINT_CNF (USB_ENDPT_CNF_0):** This 4-bit field identifies the endpoint used by the controller for all Token PID generation. This is a R/W field that is set to 01h after reset. **Power Well:** Core

18.9.24 USB Test Per Port Register 1 (USB2_TEST_PERPORT_REG1_LANE0/1/2/3) - Offset 4113h/4213h/4313h/4413h

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x43] + 4113h/4213h/4313h/4413h

Op Codes: 6h - Read, 7h – Write

Default: 00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	Reserved.
8	0x0 RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
7:4	0x0 RW	Reserved.
3	0x0 RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
2:0	RW	Reserved.

18.9.25 Per Port RCOMP High Speed Pull down Register (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_LANE0/1/2/3) - Offset 4123h/4223h/4323h/4423h

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x43] + 4123h/4223h/4323h/4423h

Op Codes: 6h - Read, 7h – Write

Default: 00000011h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	Reserved.
29:24	0x0 RW	Reserved.
23:15	0x0 R0	Reserved.
14:8	0x0 RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
7:5	0x0 RW	Reserved.
23:15	0x1 RW	Reserved.
14:8	0x0 RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
2:0	0x1 RW	Restricted

18.9.26 USB Per Port (USB2_PER_PORT_2_LANE0/1/2/3) - Offset 4126h/4226h/4326h/4426h

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x43] + 4126h/4226h/4326h/4426h

Op Codes: 6h - Read, 7h – Write

Default: 00001249h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	Reserved.
12:11	0x2 RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
10:9	0x1 RO	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
8	0x0 RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
7:5	0x0 RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
4:2	0x0 RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.
1:0	RW	This register field is used in the workaround in the erratum VL184. It is Reserved for all other purposes.

18.10 USB EHCI Electrical Message Bus Registers

Table 216. Summary of USB EHCI Message Bus Registers—0x43

Offset	Register Name (Register Symbol)	Default Value
4100–4103h	"USB2 PER PORT (USB2_PER_PORT_LANE0)—Offset 4100h" on page 2436	0004F201h
4200–4203h	"USB2 PER PORT (USB2_PER_PORT_LANE1)—Offset 4200h" on page 2438	0004F201h
4300–4303h	"USB2 PER PORT (USB2_PER_PORT_LANE2)—Offset 4300h" on page 2440	0004F201h
4400–4403h	"USB2 PER PORT (USB2_PER_PORT_LANE3)—Offset 4400h" on page 2442	0004F201h
4500–4503h	"USB2 PER PORT (USB2_PER_PORT_LANE4)—Offset 4500h" on page 2443	0004F201h
4600–4603h	"USB2 PER PORT (USB2_PER_PORT_LANE5)—Offset 4600h" on page 2445	0004F201h
4700–4703h	"USB2 PER PORT (USB2_PER_PORT_LANE6)—Offset 4700h" on page 2447	0004F201h
4800–4803h	"USB2 PER PORT (USB2_PER_PORT_LANE7)—Offset 4800h" on page 2449	0004F201h

18.10.1 USB2 PER PORT (USB2_PER_PORT_LANE0)—Offset 4100h

Access Method

Type: Message Bus Register (Size: 32 bits) **Offset:** [Port: 0x43] + 4100h

Op Codes:
h - Read, h - Write

Default: 0004F201h

Bits	Default	Field
31:26	0 0 0 0 0 0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22	0	RSVD
21	0	RSVD
20	0	RSVD
19:17	0 1 0	RSVD
16	0	RSVD
15	1	PERPORTTXPREEMPEN_0
14	1	PERPORTTXPEHALF_0
13:11	1 1 0	PERPORTPETXISET_0
10:8	0 1 0	RSVD
7	0	RSVD
6:4	0 0 0	RSVD
3	0	PORTRESERVED
2	0	RSVD
1	0	RSVD
0	1	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22	0b RO	**Reserved (RSVD):** Reserved.
21	0b RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19:17	010b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.
15	1b RW	**PerPort HS Transmitter Pre-emphasis (PERPORTTXPREEMPEN_0):** Config bit (per port) Enables HS transmitter pre-emphasis for the respective ports 1 enabled pre-emphasis or when PORTRESERVED[0]=1 0 disabled pre-emphasis This has to be 1 if either to enable pre-emphasis or de-emphasis, 0 to completely turn OFF. **Power Well:** SUS
14	1b RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF_0):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis or when PORTRESERVED[0]=1 in de-emphasis mode, this has to be 0 **Power Well:** SUS
13:11	110b RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET_0):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Voh 000 0mV 001 11.250mV 010 16.875mV 011 28.125mV 100 28.125mV 101 39.375mV 110 45.000mV (default) 111 56.250mV **Power Well:** SUS
10:8	010b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6:4	000b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RW	**DE-EMPHASIS ON/OFF FOR DEBUG (PORTRESERVED):** Config bit to select De-emphasis mode ON/OFF for TX-HS debug purpose. 0 De-emphasis OFF (default) 1 De-emphasis ON In order to enable De-emphasis ON, ensure RERPORTTXPREEMPEN(0h15)=1 and PERPORTTXPEHALF(0h14)=0 **Power Well:** SUS
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	1b RO	**Reserved (RSVD):** Reserved.

18.10.2 USB2 PER PORT (USB2_PER_PORT_LANE1)—Offset 4200h

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x43] + 4200h

Op Codes:
h - Read, h - Write

Default: 0004F201h

Bits	Default	Field
31:26	000000	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22	0	RSVD
21	0	RSVD
20	0	RSVD
19:17	010	RSVD
16	0	RSVD
15	1	PERPORTTXPREEMPEN_0
14	1	PERPORTTXPEHALF_0
13:11	110	PERPORTPETXISET_0
10:8	010	RSVD
7	0	RSVD
6:4	000	RSVD
3	0	PORTRESERVED
2	0	RSVD
1	0	RSVD
0	1	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22	0b RO	**Reserved (RSVD):** Reserved.
21	0b RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19:17	010b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.
15	1b RW	**PerPort HS Transmitter Pre-emphasis (PERPORTTXPREEMPEN_0):** Config bit (per port) Enables HS transmitter pre-emphasis for the respective ports 1 enabled pre-emphasis or when PORTRESERVED[0]=1 0 disabled pre-emphasis This has to be 1 if either to enable pre-emphasis or de-emphasis, 0 to completely turn OFF. **Power Well:** SUS
14	1b RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF_0):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis or when PORTRESERVED[0]=1 in de-emphasis mode, this has to be 0 **Power Well:** SUS
13:11	110b RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET_0):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Voh 000 0mV 001 11.250mV 010 16.875mV 011 28.125mV 100 28.125mV 101 39.375mV 110 45.000mV (default) 111 56.250mV **Power Well:** SUS
10:8	010b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6:4	000b RO	**Reserved (RSVD):** Reserved.
3	0b RW	**DE-EMPHASIS ON/OFF FOR DEBUG (PORTRESERVED):** Config bit to select De-emphasis mode ON/OFF for TX-HS debug purpose. 0 De-emphasis OFF (default) 1 De-emphasis ON In order to enable De-emphasis ON, ensure RERPORTTXPREEMPEN(0h15)=1 and PERPORTTXPEHALF(0h14)=0 **Power Well:** SUS
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Reserved (RSVD):** Reserved.
0	1b RO	**Reserved (RSVD):** Reserved.

18.10.3 USB2 PER PORT (USB2_PER_PORT_LANE2)—Offset 4300h

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x43] + 4300h

Op Codes:
h - Read, h - Write

Default: 0004F201h

Bits	Default	Field
31:26	0 0 0 0 0 0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22	0	RSVD
21	0	RSVD
20	0	RSVD
19:17	1 0 0	RSVD
16	0	RSVD
15	1	PERPORTTXPREEMPEN_0
14	1	PERPORTTXPEHALF_0
13:11	1 1 0	PERPORTPETXISET_0
10:8	0 1 0	RSVD
7	0	RSVD
6:4	0 0 0	RSVD
3	0	PORTRESERVED
2	0	RSVD
1	0	RSVD
0	1	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22	0b RO	**Reserved (RSVD):** Reserved.
21	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19:17	010b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.
15	1b RW	**PerPort HS Transmitter Pre-emphasis (PERPORTTXPREEMPEN_0):** Config bit (per port) Enables HS transmitter pre-emphasis for the respective ports 1 enabled pre-emphasis or when PORTRESERVED[0]=1 0 disabled pre-emphasis This has to be 1 if either to enable pre-emphasis or de-emphasis, 0 to completely turn OFF. **Power Well:** SUS
14	1b RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF_0):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis or when PORTRESERVED[0]=1 in de-emphasis mode, this has to be 0 **Power Well:** SUS
13:11	110b RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET_0):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Voh 000 0mV 001 11.250mV 010 16.875mV 011 28.125mV 100 28.125mV 101 39.375mV 110 45.000mV (default) 111 56.250mV **Power Well:** SUS
10:8	010b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6:4	000b RO	**Reserved (RSVD):** Reserved.
3	0b RW	**DE-EMPHASIS ON/OFF FOR DEBUG (PORTRESERVED):** Config bit to select De-emphasis mode ON/OFF for TX-HS debug purpose. 0 De-emphasis OFF (default) 1 De-emphasis ON In order to enable De-emphasis ON, ensure RERPORTTXPREEMPEN(0h15)=1 and PERPORTTXPEHALF(0h14)=0 **Power Well:** SUS
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	1b RO	**Reserved (RSVD):** Reserved.

18.10.4 USB2 PER PORT (USB2_PER_PORT_LANE3)—Offset 4400h

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x43] + 4400h

Op Codes:
h - Read, h - Write

Default: 0004F201h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	1
RSVD						RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD			RSVD	PERPORTTXPREEMPEN_0	PERPORTTXPEHALF_0	PERPORTPETXISET_0			RSVD			RSVD	RSVD			PORTRESERVED	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22	0b RO	**Reserved (RSVD):** Reserved.
21	0b RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19:17	010b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	1b RW	**PerPort HS Transmitter Pre-emphasis (PERPORTTXPREEMPEN_0):** Config bit (per port) Enables HS transmitter pre-emphasis for the respective ports 1 enabled pre-emphasis or when PORTRESERVED[0]=1 0 disabled pre-emphasis This has to be 1 if either to enable pre-emphasis or de-emphasis, 0 to completely turn OFF. **Power Well:** SUS
14	1b RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF_0):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis or when PORTRESERVED[0]=1 in de-emphasis mode, this has to be 0 **Power Well:** SUS
13:11	110b RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET_0):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Voh 000 0mV 001 11.250mV 010 16.875mV 011 28.125mV 100 28.125mV 101 39.375mV 110 45.000mV (default) 111 56.250mV **Power Well:** SUS
10:8	010b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6:4	000b RO	**Reserved (RSVD):** Reserved.
3	0b RW	**DE-EMPHASIS ON/OFF FOR DEBUG (PORTRESERVED):** Config bit to select De-emphasis mode ON/OFF for TX-HS debug purpose. 0 De-emphasis OFF (default) 1 De-emphasis ON In order to enable De-emphasis ON, ensure RERPORTTXPREEMPEN(0h15)=1 and PERPORTTXPEHALF(0h14)=0 **Power Well:** SUS
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	1b RO	**Reserved (RSVD):** Reserved.

18.10.5 USB2 PER PORT (USB2_PER_PORT_LANE4)—Offset 4500h

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x43] + 4500h

Op Codes:
h - Read, h - Write

Default: 0004F201h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	1

RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | PERPORTTXPREEMPEN_0 | PERPORTTXPEHALF_0 | PERPORTPETXISET_0 | RSVD | RSVD | RSVD | PORTRESERVED | RSVD | RSVD | RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22	0b RO	**Reserved (RSVD):** Reserved.
21	0b RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19:17	010b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.
15	1b RW	**PerPort HS Transmitter Pre-emphasis (PERPORTTXPREEMPEN_0):** Config bit (per port) Enables HS transmitter pre-emphasis for the respective ports 1 enabled pre-emphasis or when PORTRESERVED[0]=1 0 disabled pre-emphasis This has to be 1 if either to enable pre-emphasis or de-emphasis, 0 to completely turn OFF. **Power Well:** SUS
14	1b RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF_0):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis or when PORTRESERVED[0]=1 in de-emphasis mode, this has to be 0 **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:11	110b RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET_0):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Voh 000 0mV 001 11.250mV 010 16.875mV 011 28.125mV 100 28.125mV 101 39.375mV 110 45.000mV (default) 111 56.250mV **Power Well:** SUS
10:8	010b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6:4	000b RO	**Reserved (RSVD):** Reserved.
3	0b RW	**DE-EMPHASIS ON/OFF FOR DEBUG (PORTRESERVED):** Config bit to select De-emphasis mode ON/OFF for TX-HS debug purpose. 0 De-emphasis OFF (default) 1 De-emphasis ON In order to enable De-emphasis ON, ensure RERPORTTXPREEMPEN(0h15)=1 and PERPORTTXPEHALF(0h14)=0 **Power Well:** SUS
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	1b RO	**Reserved (RSVD):** Reserved.

18.10.6 USB2 PER PORT (USB2_PER_PORT_LANE5)—Offset 4600h

Access Method

Type: Message Bus Register
(Size: 32 bits)

Offset: [Port: 0x43] + 4600h

Op Codes:
h - Read, h - Write

Default: 0004F201h

Bits	Default	Field
31:26	0 0 0 0 0 0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22	0	RSVD
21	0	RSVD
20	0	RSVD
19:17	0 1 0	RSVD
16	0	RSVD
15	1	PERPORTTXPREEMPEN_0
14	1	PERPORTTXPEHALF_0
13:11	1 1 0	PERPORTPETXISET_0
10:8	0 1 0	RSVD
7	0	RSVD
6:4	0 0 0	RSVD
3	0	PORTRESERVED
2	0	RSVD
1	0	RSVD
0	1	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22	0b RO	**Reserved (RSVD):** Reserved.
21	0b RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19:17	010b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.
15	1b RW	**PerPort HS Transmitter Pre-emphasis (PERPORTTXPREEMPEN_0):** Config bit (per port) Enables HS transmitter pre-emphasis for the respective ports 1 enabled pre-emphasis or when PORTRESERVED[0]=1 0 disabled pre-emphasis This has to be 1 if either to enable pre-emphasis or de-emphasis, 0 to completely turn OFF. **Power Well:** SUS
14	1b RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF_0):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis or when PORTRESERVED[0]=1 in de-emphasis mode, this has to be 0 **Power Well:** SUS
13:11	110b RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET_0):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Voh 000 0mV 001 11.250mV 010 16.875mV 011 28.125mV 100 28.125mV 101 39.375mV 110 45.000mV (default) 111 56.250mV **Power Well:** SUS
10:8	010b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:4	000b RO	**Reserved (RSVD):** Reserved.
3	0b RW	**DE-EMPHASIS ON/OFF FOR DEBUG (PORTRESERVED):** Config bit to select De-emphasis mode ON/OFF for TX-HS debug purpose. 0 De-emphasis OFF (default) 1 De-emphasis ON In order to enable De-emphasis ON, ensure RERPORTTXPREEMPEN(0h15)=1 and PERPORTTXPEHALF(0h14)=0 **Power Well:** SUS
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	1b RO	**Reserved (RSVD):** Reserved.

18.10.7 USB2 PER PORT (USB2_PER_PORT_LANE6)—Offset 4700h

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x43] + 4700h

Op Codes:
h - Read, h - Write

Default: 0004F201h

Bits	Default	Field
31:26	0 0 0 0 0 0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22	0	RSVD
21	0	RSVD
20	0	RSVD
19:17	0 1 0	RSVD
16	0	RSVD
15	1	PERPORTTXPREEMPEN_0
14	1	PERPORTTXPEHALF_0
13:11	1 1 0	PERPORTPETXISET_0
10:8	0 1 0	RSVD
7	0	RSVD
6:4	0 0 0	RSVD
3	0	PORTRESERVED
2	0	RSVD
1	0	RSVD
0	1	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23	0b RO	**Reserved (RSVD):** Reserved.
22	0b RO	**Reserved (RSVD):** Reserved.
21	0b RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19:17	010b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.
15	1b RW	**PerPort HS Transmitter Pre-emphasis (PERPORTTXPREEMPEN_0):** Config bit (per port) Enables HS transmitter pre-emphasis for the respective ports 1 enabled pre-emphasis or when PORTRESERVED[0]=1 0 disabled pre-emphasis This has to be 1 if either to enable pre-emphasis or de-emphasis, 0 to completely turn OFF. **Power Well:** SUS
14	1b RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF_0):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis or when PORTRESERVED[0]=1 in de-emphasis mode, this has to be 0 **Power Well:** SUS
13:11	110b RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET_0):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Voh 000 0mV 001 11.250mV 010 16.875mV 011 28.125mV 100 28.125mV 101 39.375mV 110 45.000mV (default) 111 56.250mV **Power Well:** SUS
10:8	010b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6:4	000b RO	**Reserved (RSVD):** Reserved.
3	0b RW	**DE-EMPHASIS ON/OFF FOR DEBUG (PORTRESERVED):** Config bit to select De-emphasis mode ON/OFF for TX-HS debug purpose. 0 De-emphasis OFF (default) 1 De-emphasis ON In order to enable De-emphasis ON, ensure RERPORTTXPREEMPEN(0h15)=1 and PERPORTTXPEHALF(0h14)=0 **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	1b RO	**Reserved (RSVD):** Reserved.

18.10.8 USB2 PER PORT (USB2_PER_PORT_LANE7)—Offset 4800h

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x43] + 4800h

Op Codes:
h - Read, h - Write

Default: 0004F201h

Bits	Default	Field
31:26	0 0 0 0 0 0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22	0	RSVD
21	0	RSVD
20	0	RSVD
19:17	0 1 0	RSVD
16	0	RSVD
15	1	PERPORTTXPREEMPEN_0
14	1	PERPORTTXPEHALF_0
13:11	1 1 0	PERPORTPETXISET_0
10:8	0 1 0	RSVD
7	0	RSVD
6:4	0 0 0	RSVD
3	0	PORTRESERVED
2	0	RSVD
1	0	RSVD
0	1	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0b RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19:17	010b RO	**Reserved (RSVD):** Reserved.
16	0b RO	**Reserved (RSVD):** Reserved.
15	1b RW	**PerPort HS Transmitter Pre-emphasis (PERPORTTXPREEMPEN_0):** Config bit (per port) Enables HS transmitter pre-emphasis for the respective ports 1 enabled pre-emphasis or when PORTRESERVED[0]=1 0 disabled pre-emphasis This has to be 1 if either to enable pre-emphasis or de-emphasis, 0 to completely turn OFF. **Power Well:** SUS
14	1b RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF_0):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis or when PORTRESERVED[0]=1 in de-emphasis mode, this has to be 0 **Power Well:** SUS
13:11	110b RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET_0):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Voh 000 0mV 001 11.250mV 010 16.875mV 011 28.125mV 100 28.125mV 101 39.375mV 110 45.000mV (default) 111 56.250mV **Power Well:** SUS
10:8	010b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6:4	000b RO	**Reserved (RSVD):** Reserved.
3	0b RW	**DE-EMPHASIS ON/OFF FOR DEBUG (PORTRESERVED):** Config bit to select De-emphasis mode ON/OFF for TX-HS debug purpose. 0 De-emphasis OFF (default) 1 De-emphasis ON In order to enable De-emphasis ON, ensure RERPORTTXPREEMPEN(0h15)=1 and PERPORTTXPEHALF(0h14)=0 **Power Well:** SUS
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.

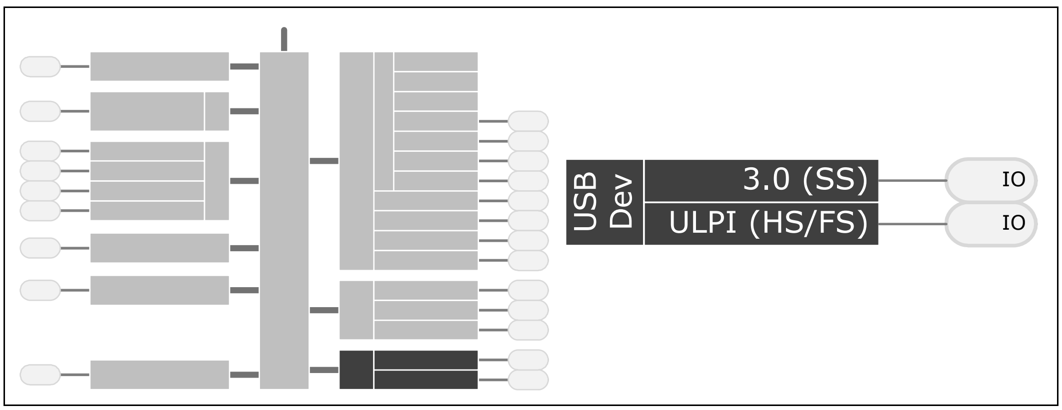
Bit Range	Default & Access	Field Name (ID): Description
0	1b RO	**Reserved (RSVD):** Reserved.

19 USB Device Controller Interfaces (3.0, ULPI)

The SoC implements a single USB 3.0 device controller, where the platform acts as a peripheral to another device or another PC.

The USB Device controller supports connections at Super Speed (3.0) on the USB3DEV interface, and High and Full speeds (2.0/1.x) on the ULPI interface. To support High and Full Speed devices on ULPI, an external PHY is required.

Note: The ULPI interface must be implemented even if only SuperSpeed support is required. The USB3DEV interface will not operate if the ULPI interface is disabled.



19.0.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 217. USB 3.0 Device Signals

Signal Name	Direction Plat. Power	Description
USB3DEV_RXP/N[0]	I V1P0S	**Data In:** High speed serialized data inputs
USB3DEV_TXP/N[0]	O V1P0S	**Data Out:** High speed serialized data outputs.
USB3DEV_REXT[0]		**Resistor Compensation:** An external resistor must be connected between this pin and package ground. Contact your Intel representative for details.

Table 218. USB ULPI Device Signals

Signal Name	Direction Plat. Power	Description
USB_ULPI_CLK	I V1P8A	**Interface Clock** By default, control and data signals are synchronous to clock.
USB_ULPI_DATA[7:0]	I/O V1P8A	**Bi-directional data bus** Driven low by the Link during idle. The Link starts a transfer by sending a non-zero pattern. The PHY must assert USB_ULPI_DIR before using the data bus. A turnaround cycle is required every time that USB_ULPI_DIR toggles.
USB_ULPI_DIR	I V1P8A	**Direction of the data bus** By default, USB_ULPI_DIR is low and the PHY listens for non-zero data from the Link. The PHY asserts USB_ULPI_DIR to get control of the data bus.
USB_ULPI_NXT	I V1P8A	**Next Data** The PHY drives USB_ULPI_NXT high to throttle the data bus
USB_ULPI_STP	O V1P8A	**Stop data** The Link drives USB_ULPI_STP high to signal the end of its data stream. The Link can also drive USB_ULPI_STP high to request data bus access from the PHY
USB_ULPI_REFCLK	O V1P8A	**Reference clock** ULPI reference clock for external PHY
USB_ULPI_RST#	O V1P8A	**Reset** Used to reset the external PHY. Not part of ULPI specification. Optionally used by driver.

19.1 USB Device Controller

The USB device controller can control one USB 3.0 Device port. Either a combo SS + ULPI Device port, or UPLI only port. It supports hosts conforming to USB 3.0 at bit rates up to 5 Gbps on USB3DEV interface as well as USB 2.0 hosts at up to 480 Mbps via a PHY on ULPI.

19.1.1 Features

Features supported by the Device Controller include:

- Enumerable by both ACPI and PCI. The USB3 device subsystem is designed to appear to the OS as a true PCI device. It will also support ACPI-enumerated methods.
- Device controller registers and data structures are implemented as extensions to the EHCI programmers interface.
- Support for LPM (Link Power Management)

Some of the key features of the ULPI device controller are:

- Supports up to 8 endpoints when acting as device
- 8-bit data interface transmitted at 60 MHz ULPI clock

Note: Recommended not to disconnect the connection when a debug session is in progress.

19.1.2 Power Management Features

The USB 3.0 device subsystem supports the following device power states:

- D0: Functional and highest power state.
- RTD3 (D3): Software managed deepest low power state in which state is saved/ restored if needed prior to entry/exit

19.1.2.1 D0

This is the Functional and highest power state. The USB 3.0 device subsystem is in this state when the USB link is in U0 (U0 is the normal operational state where packets can be transmitted and received).

19.1.2.2 D3

D3 is a low power state that is used when the link is suspended; for example, U3 (U3 is a link state where a device is put into a suspend state. Significant link and device powers are saved).

This is a software directed state in which the controller is either power gated or the power is disabled.

19.1.3 Interrupts

A Functional Interrupt is generated by the logic in the USB device controller core to indicate the occurrence of an event needing application intervention. The design of the USB device core is such that events such as "link change" that would traditionally trigger an interrupt through an interrupt status register, are instead delivered to an 'Event buffer' in host memory, together with an interrupt indicating this.

19.2 References

Universal Serial Bus (USB) 3.0 Revision Specification

Universal Serial Bus (USB) 2.0 Revision Specification

ULPI Working Group: http://www.ulpi.org/

19.3 Register Map

See Chapters Section 3, "Register Access Methods" on page 69 and Section 4, "Mapping Address Spaces" on page 75 for additional information. Also note that the device controller also contains both device and host registers. The host functionality of this controller is not fully functional and should not be used. See the USB Host chapter for host controllers.

§

19.4 USB 3.0 Device PCI Configuration Registers

Table 219. Summary of USB 3.0 Device PCI Configuration Registers—0/22/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 2456	00000000h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 2456	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 2458	00000000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 2458	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 2459	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 2459	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 2460	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2461	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 2461	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 2462	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 2462	48030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 2463	00000008h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 2463	00000000h

19.4.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:22, F:0] + 0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DEVICEID (31:16)	VENDORID (15:0)

Bit Range	Default & Access	Description
31:16	0000h RO	**DEVICEID:** Reserved.
15:0	0000h RO	**VENDORID:** Reserved.

19.4.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

STATUSCOMMAND: [B:0, D:22, F:0] + 4h

Default: 00100000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0		RMA	RCA	Reserved1							CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**RMA:** Reserved.
28	0h RW/1C	**RCA:** Reserved.
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**CAPLIST:** Reserved.
19	0h RO	**INTR_STATUS:** Reserved.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**INTR_DISABLE:** Reserved.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR_ENABLE:** Reserved.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**BME:** Reserved.
1	0h RW	**MSE:** Reserved.
0	0h RO	**Reserved6:** Reserved.

19.4.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:22, F:0] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: CLASS_CODES (bits 31:8), RID (bits 7:0)

Bit Range	Default & Access	Description
31:8	000000h RO	**CLASS_CODES:** Reserved.
7:0	00h RO	**RID:** Reserved.

19.4.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:22, F:0] + Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved0 (bits 31:24), MULFNDEV (bit 23), HEADERTYPE (bits 22:16), LATTIMER (bits 15:8), CACHELINE_SIZE (bits 7:0)

Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**MULFNDEV:** Reserved.
22:16	00h RO	**HEADERTYPE:** Reserved.

Bit Range	Default & Access	Description
15:8	00h RO	**LATTIMER:** Reserved.
7:0	00h RW	**CACHELINE_SIZE:** Reserved.

19.4.5 reg_BAR_type (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits) **BAR:** [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Reserved.
11:4	00h RO	**SIZEINDICATOR:** Reserved.
3	0h RO	**PREFETCHABLE:** Reserved.
2:1	0h RO	**TYPE:** Reserved.
0	0h RO	**MESSAGE_SPACE:** Reserved.

19.4.6 reg_BAR1_type (BAR1)—Offset 14h

BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits) **BAR1:** [B:0, D:22, F:0] + 14h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BASEADDR1 | SIZEINDICATOR1 | PREFETCHABLE1 | TYPE1 | MESSAGE_SPACE1

Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** Reserved.
11:4	00h RO	**SIZEINDICATOR1:** Reserved.
3	0h RO	**PREFETCHABLE1:** Reserved.
2:1	0h RO	**TYPE1:** Reserved.
0	0h RO	**MESSAGE_SPACE1:** Reserved.

19.4.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SUBSYSTEMID: [B:0, D:22, F:0] + 2Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

SUBSYSTEMID | SUBSYSTEMVENDORID

Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Reserved.
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Reserved.

19.4.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**EXPANSION_ROM_BASEADDR:** [B:0, D:22, F:0] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

19.4.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**CAPABILITYPTR:** [B:0, D:22, F:0] + 34h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Reserved0 (bits 31:8) | CAPPTR_POWER (bits 7:0)

Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**CAPPTR_POWER:** Reserved.

19.4.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTERRUPTREG: [B:0, D:22, F:0] + 3Ch

Default: 00000100h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0
MAX_LAT		MIN_GNT		Reserved0	INTPIN	INTLINE	

Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Reserved.
23:16	00h RO	**MIN_GNT:** Reserved.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**INTPIN:** Reserved.
7:0	00h RW	**INTLINE:** Reserved.

19.4.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

POWERCAPID: [B:0, D:22, F:0] + 80h

Default: 48030001h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 1 0 0	1 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Field	Bits
PMESUPPORT	31:27
Reserved0	26:19
VERSION	18:16
NXTCAP	15:8
POWER_CAP	7:0

Bit Range	Default & Access	Description
31:27	09h RO	**PMESUPPORT:** Reserved.
26:19	00h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Description
18:16	3h RO	**VERSION:** Reserved.
15:8	00h RO	**NXTCAP:** Reserved.
7:0	01h RO	**POWER_CAP:** Reserved.

19.4.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:22, F:0] + 84h

Default: 00000008h

31:16	15	14:9	8	7:4	3	2	1:0
0000 0000 0000 0000	0	000 000	0	0000	1	0	00
Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PMESTATUS:** Reserved.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PMEENABLE:** Reserved.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**NO_SOFT_RESET:** Reserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**POWERSTATE:** Reserved.

19.4.13 reg_MANID_type (MANID)—Offset F8h

Manufacturers ID

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

MANID: [B:0, D:22, F:0] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MANID																															

Bit Range	Default & Access	Description
31:0	00000000h RO	**MANID:** Reserved.

19.5 USB 3.0 Device PCI Configuration Registers

Table 220. Summary of USB 3.0 Device PCI Configuration Registers—0/22/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 2465	00000000h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 2465	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 2467	00000000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 2467	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 2468	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 2468	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 2469	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2470	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 2470	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 2471	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 2471	48030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 2472	00000008h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 2472	00000000h

19.5.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVVENDID: [B:0, D:22, F:0] + 0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Description
31:16	0000h RO	**DEVICEID:** Reserved.
15:0	0000h RO	**VENDORID:** Reserved.

19.5.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

STATUSCOMMAND: [B:0, D:22, F:0] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0	RMA	RCA	Reserved1	CAPLIST	INTR_STATUS	Reserved2	Reserved3	INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5	BME	MSE	Reserved6

Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** Reserved.
29	0h RW/1C	**RMA:** Reserved.
28	0h RW/1C	**RCA:** Reserved.
27:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**CAPLIST:** Reserved.
19	0h RO	**INTR_STATUS:** Reserved.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**INTR_DISABLE:** Reserved.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR_ENABLE:** Reserved.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**BME:** Reserved.
1	0h RW	**MSE:** Reserved.
0	0h RO	**Reserved6:** Reserved.

19.5.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

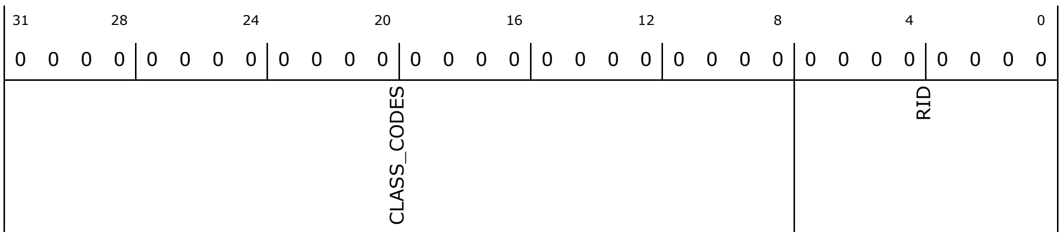
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REVCLASSCODE: [B:0, D:22, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	000000h RO	**CLASS_CODES:** Reserved.
7:0	00h RO	**RID:** Reserved.

19.5.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

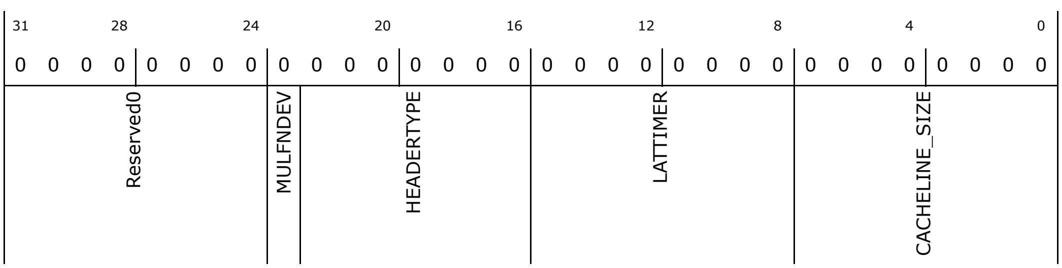
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLLATHEADERBIST: [B:0, D:22, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved.
23	0h RO	**MULFNDEV:** Reserved.
22:16	00h RO	**HEADERTYPE:** Reserved.

Bit Range	Default & Access	Description
15:8	00h RO	**LATTIMER:** Reserved.
7:0	00h RW	**CACHELINE_SIZE:** Reserved.

19.5.5 reg_BAR_type (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Reserved.
11:4	00h RO	**SIZEINDICATOR:** Reserved.
3	0h RO	**PREFETCHABLE:** Reserved.
2:1	0h RO	**TYPE:** Reserved.
0	0h RO	**MESSAGE_SPACE:** Reserved.

19.5.6 reg_BAR1_type (BAR1)—Offset 14h

BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BAR1: [B:0, D:22, F:0] + 14h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR1																				SIZEINDICATOR1								PREFETCHABLE1	TYPE1		MESSAGE_SPACE1

Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** Reserved.
11:4	00h RO	**SIZEINDICATOR1:** Reserved.
3	0h RO	**PREFETCHABLE1:** Reserved.
2:1	0h RO	**TYPE1:** Reserved.
0	0h RO	**MESSAGE_SPACE1:** Reserved.

19.5.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**SUBSYSTEMID:** [B:0, D:22, F:0] + 2Ch

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Reserved.
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Reserved.

19.5.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [B:0, D:22, F:0] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

19.5.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPABILITYPTR: [B:0, D:22, F:0] + 34h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Reserved0

CAPPTR_POWER

Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	80h RO	**CAPPTR_POWER:** Reserved.

19.5.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**INTERRUPTREG:** [B:0, D:22, F:0] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

MAX_LAT (31:24) | MIN_GNT (23:16) | Reserved0 (15:12) | INTPIN (11:8) | INTLINE (7:0)

Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Reserved.
23:16	00h RO	**MIN_GNT:** Reserved.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**INTPIN:** Reserved.
7:0	00h RW	**INTLINE:** Reserved.

19.5.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**POWERCAPID:** [B:0, D:22, F:0] + 80h

Default: 48030001h

31			28				24				20				16				12				8				4				0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

PMESUPPORT (31:27) | Reserved0 (26:19) | VERSION (18:16) | NXTCAP (15:8) | POWER_CAP (7:0)

Bit Range	Default & Access	Description
31:27	09h RO	**PMESUPPORT:** Reserved.
26:19	00h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Description
18:16	3h RO	**VERSION:** Reserved.
15:8	00h RO	**NXTCAP:** Reserved.
7:0	01h RO	**POWER_CAP:** Reserved.

19.5.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMECTRLSTATUS: [B:0, D:22, F:0] + 84h

Default: 00000008h

Bits	31:16	15	14:9	8	7:4	3	2	1:0
Value	0000 0000 0000 0000	0	000 000	0	0000	1	0	00
Field	Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PMESTATUS:** Reserved.
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PMEENABLE:** Reserved.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**NO_SOFT_RESET:** Reserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**POWERSTATE:** Reserved.

19.5.13 reg_MANID_type (MANID)—Offset F8h

Manufacturers ID

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

MANID: [B:0, D:22, F:0] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Description
31:0	00000000h RO	**MANID:** Reserved.

19.6 USB 3.0 Device Memory Mapped I/O Registers

Table 221. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"CAPLENGTH—Offset 0h" on page 2480	00960020h
4h	4	"HCSPARAMS1—Offset 4h" on page 2481	0200017Fh
8h	4	"HCSPARAMS2—Offset 8h" on page 2482	140000F1h
Ch	4	"HCSPARAMS3—Offset Ch" on page 2482	07FF000Ah
10h	4	"HCCPARAMS—Offset 10h" on page 2483	0220F04Ch
14h	4	"DBOFF—Offset 14h" on page 2484	00000480h
18h	4	"RTSOFF—Offset 18h" on page 2485	00000440h
1Ch	4	"Rsvd_HC—Offset 1Ch" on page 2486	00000000h
20h	4	"USBCMD—Offset 20h" on page 2486	00000000h
24h	4	"USBSTS—Offset 24h" on page 2488	00000001h
28h	4	"PAGESIZE—Offset 28h" on page 2489	00000001h
34h	4	"DNCTRL—Offset 34h" on page 2489	00000000h
38h	4	"CRCR_LO—Offset 38h" on page 2490	00000000h
3Ch	4	"CRCR_HI—Offset 3Ch" on page 2491	00000000h
50h	4	"DCBAAP_LO—Offset 50h" on page 2492	00000000h
54h	4	"DCBAAP_HI—Offset 54h" on page 2492	00000000h
58h	4	"CONFIG—Offset 58h" on page 2493	00000000h
420h	4	"PORTSC1—Offset 420h" on page 2493	000002A0h
424h	4	"PORTPMSC1—Offset 424h" on page 2496	00000000h
428h	4	"PORTLI—Offset 428h" on page 2497	00000000h
42Ch	4	"PORTHLPMC—Offset 42Ch" on page 2497	00000000h
430h	4	"PORTSC2—Offset 430h" on page 2498	000002A0h
434h	4	"PORTPMSC2—Offset 434h" on page 2501	00000000h
440h	4	"MFINDEX—Offset 440h" on page 2502	00000000h
444h	4	"RsvdZ—Offset 444h" on page 2502	00000000h
460h	4	"IMAN—Offset 460h" on page 2502	00000000h
464h	4	"IMOD—Offset 464h" on page 2503	00000FA0h
468h	4	"ERSTSZ—Offset 468h" on page 2504	00000000h
46Ch	4	"RsvdP—Offset 46Ch" on page 2504	00000000h
470h	4	"ERSTBA_LO—Offset 470h" on page 2505	00000000h
474h	4	"ERSTBA_HI—Offset 474h" on page 2505	00000000h
478h	4	"ERDP_LO—Offset 478h" on page 2506	00000000h
47Ch	4	"ERDP_HI—Offset 47Ch" on page 2506	00000000h
480h	4	"DB_0—Offset 480h" on page 2507	00000000h
484h	4	"DB_1—Offset 484h" on page 2508	00000000h
488h	4	"DB_2—Offset 488h" on page 2509	00000000h

Table 221. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
48Ch	4	"DB_3—Offset 48Ch" on page 2510	00000000h
490h	4	"DB_4—Offset 490h" on page 2511	00000000h
494h	4	"DB_5—Offset 494h" on page 2512	00000000h
498h	4	"DB_6—Offset 498h" on page 2513	00000000h
49Ch	4	"DB_7—Offset 49Ch" on page 2514	00000000h
4A0h	4	"DB_8—Offset 4A0h" on page 2515	00000000h
4A4h	4	"DB_9—Offset 4A4h" on page 2516	00000000h
4A8h	4	"DB_10—Offset 4A8h" on page 2517	00000000h
4ACh	4	"DB_11—Offset 4ACh" on page 2518	00000000h
4B0h	4	"DB_12—Offset 4B0h" on page 2519	00000000h
4B4h	4	"DB_13—Offset 4B4h" on page 2520	00000000h
4B8h	4	"DB_14—Offset 4B8h" on page 2521	00000000h
4BCh	4	"DB_15—Offset 4BCh" on page 2522	00000000h
4C0h	4	"DB_16—Offset 4C0h" on page 2523	00000000h
880h	4	"USBLEGSUP—Offset 880h" on page 2524	00000401h
884h	4	"USBLEGCTLSTS—Offset 884h" on page 2525	00000000h
890h	4	"SUPTPRT2_DW0—Offset 890h" on page 2526	02000002h
894h	4	"SUPTPRT2_DW1—Offset 894h" on page 2526	02000110h
898h	4	"SUPTPRT2_DW2—Offset 898h" on page 2527	00080001h
8A0h	4	"SUPTPRT3_DW0—Offset 8A0h" on page 2528	03000002h
8A4h	4	"SUPTPRT3_DW1—Offset 8A4h" on page 2529	00000000h
8A8h	4	"SUPTPRT3_DW2—Offset 8A8h" on page 2529	00000000h
C100h	4	"GSBUSCFG0—Offset C100h" on page 2530	00000006h
C104h	4	"GSBUSCFG1—Offset C104h" on page 2531	00000F00h
C108h	4	"GTXTHRCFG—Offset C108h" on page 2532	230A0000h
C10Ch	4	"GRXTHRCFG—Offset C10Ch" on page 2532	22800000h
C110h	4	"GCTL—Offset C110h" on page 2533	45803000h
C118h	4	"GSTS—Offset C118h" on page 2535	3E800002h
C120h	4	"GSNPSID—Offset C120h" on page 2536	5533192Ah
C124h	4	"GGPIO—Offset C124h" on page 2536	00000000h
C128h	4	"GUID—Offset C128h" on page 2537	12345678h
C12Ch	4	"GUCTL—Offset C12Ch" on page 2537	7FC0C600h
C130h	4	"GBUSERRADDRLO—Offset C130h" on page 2538	00000000h
C134h	4	"GBUSERRADDRHI—Offset C134h" on page 2539	00000000h
C138h	4	"GPRTBIMAPLO—Offset C138h" on page 2539	00000000h
C13Ch	4	"GPRTBIMAPHI—Offset C13Ch" on page 2540	00000000h
C140h	4	"GHWPARAMS0—Offset C140h" on page 2541	2020400Ah
C144h	4	"GHWPARAMS1—Offset C144h" on page 2542	0260C93Bh
C148h	4	"GHWPARAMS2—Offset C148h" on page 2543	008086A0h

Table 221. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C14Ch	4	"GHWPARAMS3—Offset C14Ch" on page 2543	10420089h
C150h	4	"GHWPARAMS4—Offset C150h" on page 2545	48822004h
C154h	4	"GHWPARAMS5—Offset C154h" on page 2545	04202088h
C158h	4	"GHWPARAMS6—Offset C158h" on page 2546	0C00AC20h
C15Ch	4	"GHWPARAMS7—Offset C15Ch" on page 2547	038807E6h
C160h	4	"GDBGFIFOSPACE—Offset C160h" on page 2548	00420000h
C164h	4	"GDBGLTSSM—Offset C164h" on page 2549	01010440h
C180h	4	"GPRTBIMAP_HSLO—Offset C180h" on page 2550	00000000h
C184h	4	"GPRTBIMAP_HSHI—Offset C184h" on page 2551	00000000h
C188h	4	"GPRTBIMAP_FSLO—Offset C188h" on page 2552	00000000h
C18Ch	4	"GPRTBIMAP_FSHI—Offset C18Ch" on page 2552	00000000h
C200h	4	"GUSB2PHYCFG—Offset C200h" on page 2553	0000A410h
C240h	4	"GUSB2I2CCTL—Offset C240h" on page 2554	00000000h
C280h	4	"GUSB2PHYACC—Offset C280h" on page 2555	00000000h
C2C0h	4	"GUSB3PIPECTL—Offset C2C0h" on page 2556	02044002h
C300h	4	"GTXFIFOSIZ0—Offset C300h" on page 2558	00000042h
C304h	4	"GTXFIFOSIZ1—Offset C304h" on page 2559	00420184h
C308h	4	"GTXFIFOSIZ2—Offset C308h" on page 2559	01C60184h
C30Ch	4	"GTXFIFOSIZ3—Offset C30Ch" on page 2560	034A0184h
C310h	4	"GTXFIFOSIZ4—Offset C310h" on page 2560	04CE0082h
C314h	4	"GTXFIFOSIZ5—Offset C314h" on page 2561	05500082h
C318h	4	"GTXFIFOSIZ6—Offset C318h" on page 2561	05D20082h
C31Ch	4	"GTXFIFOSIZ7—Offset C31Ch" on page 2562	06540082h
C320h	4	"GTXFIFOSIZ8—Offset C320h" on page 2562	06D60022h
C324h	4	"GTXFIFOSIZ9—Offset C324h" on page 2563	06F80022h
C328h	4	"GTXFIFOSIZ10—Offset C328h" on page 2563	071A0022h
C32Ch	4	"GTXFIFOSIZ11—Offset C32Ch" on page 2564	073C0022h
C330h	4	"GTXFIFOSIZ12—Offset C330h" on page 2564	075E0022h
C334h	4	"GTXFIFOSIZ13—Offset C334h" on page 2565	07800022h
C338h	4	"GTXFIFOSIZ14—Offset C338h" on page 2565	07A20022h
C33Ch	4	"GTXFIFOSIZ15—Offset C33Ch" on page 2566	07C40022h
C380h	4	"GRXFIFOSIZ0—Offset C380h" on page 2566	00000385h
C384h	4	"GRXFIFOSIZ1—Offset C384h" on page 2567	03850000h
C388h	4	"GRXFIFOSIZ2—Offset C388h" on page 2567	03850000h
C400h	4	"GEVNTADRLO—Offset C400h" on page 2568	00000000h
C404h	4	"GEVNTADRHI—Offset C404h" on page 2568	00000000h
C408h	4	"GEVNTSIZ—Offset C408h" on page 2568	00000000h
C40Ch	4	"GEVNTCOUNT—Offset C40Ch" on page 2569	00000000h
C600h	4	"GHWPARAMS8—Offset C600h" on page 2569	00002000h

Table 221. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C700h	4	"DCFG—Offset C700h" on page 2570	00080800h
C704h	4	"DCTL—Offset C704h" on page 2571	00000000h
C708h	4	"DEVTEN—Offset C708h" on page 2572	00000000h
C70Ch	4	"DSTS—Offset C70Ch" on page 2573	00120004h
C710h	4	"DGCMDPAR—Offset C710h" on page 2574	00000000h
C714h	4	"DGCMDPAR—Offset C710h" on page 2574	00000000h
C720h	4	"DALEPENA—Offset C720h" on page 2575	00000000h
C800h	4	"DEPCMDPAR2_0—Offset C800h" on page 2576	00000000h
C804h	4	"DEPCMDPAR1_0—Offset C804h" on page 2576	00000000h
C808h	4	"DEPCMDPAR0_0—Offset C808h" on page 2577	00000000h
C80Ch	4	"DEPCMD_0—Offset C80Ch" on page 2577	00000000h
C810h	4	"DEPCMDPAR2_1—Offset C810h" on page 2578	00000000h
C814h	4	"DEPCMDPAR1_1—Offset C814h" on page 2578	00000000h
C818h	4	"DEPCMDPAR0_1—Offset C818h" on page 2579	00000000h
C81Ch	4	"DEPCMD_1—Offset C81Ch" on page 2579	00000000h
C820h	4	"DEPCMDPAR2_2—Offset C820h" on page 2580	00000000h
C824h	4	"DEPCMDPAR1_2—Offset C824h" on page 2580	00000000h
C828h	4	"DEPCMDPAR0_2—Offset C828h" on page 2581	00000000h
C82Ch	4	"DEPCMD_2—Offset C82Ch" on page 2581	00000000h
C830h	4	"DEPCMDPAR2_3—Offset C830h" on page 2582	00000000h
C834h	4	"DEPCMDPAR1_3—Offset C834h" on page 2582	00000000h
C838h	4	"DEPCMDPAR0_3—Offset C838h" on page 2583	00000000h
C83Ch	4	"DEPCMD_3—Offset C83Ch" on page 2583	00000000h
C840h	4	"DEPCMDPAR2_4—Offset C840h" on page 2584	00000000h
C844h	4	"DEPCMDPAR1_4—Offset C844h" on page 2584	00000000h
C848h	4	"DEPCMDPAR0_4—Offset C848h" on page 2585	00000000h
C84Ch	4	"DEPCMD_4—Offset C84Ch" on page 2585	00000000h
C850h	4	"DEPCMDPAR2_5—Offset C850h" on page 2586	00000000h
C854h	4	"DEPCMDPAR1_5—Offset C854h" on page 2586	00000000h
C858h	4	"DEPCMDPAR0_5—Offset C858h" on page 2587	00000000h
C85Ch	4	"DEPCMD_5—Offset C85Ch" on page 2587	00000000h
C860h	4	"DEPCMDPAR2_6—Offset C860h" on page 2588	00000000h
C864h	4	"DEPCMDPAR1_6—Offset C864h" on page 2588	00000000h
C868h	4	"DEPCMDPAR0_6—Offset C868h" on page 2589	00000000h
C86Ch	4	"DEPCMD_6—Offset C86Ch" on page 2589	00000000h
C870h	4	"DEPCMDPAR2_7—Offset C870h" on page 2590	00000000h
C874h	4	"DEPCMDPAR1_7—Offset C874h" on page 2590	00000000h
C878h	4	"DEPCMDPAR0_7—Offset C878h" on page 2591	00000000h
C87Ch	4	"DEPCMD_7—Offset C87Ch" on page 2591	00000000h

Table 221. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C880h	4	"DEPCMDPAR2_8—Offset C880h" on page 2592	00000000h
C884h	4	"DEPCMDPAR1_8—Offset C884h" on page 2593	00000000h
C888h	4	"DEPCMDPAR0_8—Offset C888h" on page 2593	00000000h
C88Ch	4	"DEPCMD_8—Offset C88Ch" on page 2593	00000000h
C890h	4	"DEPCMDPAR2_9—Offset C890h" on page 2594	00000000h
C894h	4	"DEPCMDPAR1_9—Offset C894h" on page 2595	00000000h
C898h	4	"DEPCMDPAR0_9—Offset C898h" on page 2595	00000000h
C89Ch	4	"DEPCMD_9—Offset C89Ch" on page 2596	00000000h
C8A0h	4	"DEPCMDPAR2_10—Offset C8A0h" on page 2596	00000000h
C8A4h	4	"DEPCMDPAR1_10—Offset C8A4h" on page 2597	00000000h
C8A8h	4	"DEPCMDPAR0_10—Offset C8A8h" on page 2597	00000000h
C8ACh	4	"DEPCMD_10—Offset C8ACh" on page 2598	00000000h
C8B0h	4	"DEPCMDPAR2_11—Offset C8B0h" on page 2599	00000000h
C8B4h	4	"DEPCMDPAR1_11—Offset C8B4h" on page 2599	00000000h
C8B8h	4	"DEPCMDPAR0_11—Offset C8B8h" on page 2599	00000000h
C8BCh	4	"DEPCMD_11—Offset C8BCh" on page 2600	00000000h
C8C0h	4	"DEPCMDPAR2_12—Offset C8C0h" on page 2601	00000000h
C8C4h	4	"DEPCMDPAR1_12—Offset C8C4h" on page 2601	00000000h
C8C8h	4	"DEPCMDPAR0_12—Offset C8C8h" on page 2602	00000000h
C8CCh	4	"DEPCMD_12—Offset C8CCh" on page 2602	00000000h
C8D0h	4	"DEPCMDPAR2_13—Offset C8D0h" on page 2603	00000000h
C8D4h	4	"DEPCMDPAR1_13—Offset C8D4h" on page 2603	00000000h
C8D8h	4	"DEPCMDPAR0_13—Offset C8D8h" on page 2604	00000000h
C8DCh	4	"DEPCMD_13—Offset C8DCh" on page 2604	00000000h
C8E0h	4	"DEPCMDPAR2_14—Offset C8E0h" on page 2605	00000000h
C8E4h	4	"DEPCMDPAR1_14—Offset C8E4h" on page 2606	00000000h
C8E8h	4	"DEPCMDPAR0_14—Offset C8E8h" on page 2606	00000000h
C8ECh	4	"DEPCMD_14—Offset C8ECh" on page 2606	00000000h
C8F0h	4	"DEPCMDPAR2_15—Offset C8F0h" on page 2607	00000000h
C8F4h	4	"DEPCMDPAR1_15—Offset C8F4h" on page 2608	00000000h
C8F8h	4	"DEPCMDPAR0_15—Offset C8F8h" on page 2608	00000000h
C8FCh	4	"DEPCMD_15—Offset C8FCh" on page 2609	00000000h
C900h	4	"DEPCMDPAR2_16—Offset C900h" on page 2609	00000000h
C904h	4	"DEPCMDPAR1_16—Offset C904h" on page 2610	00000000h
C908h	4	"DEPCMDPAR0_16—Offset C908h" on page 2610	00000000h
C90Ch	4	"DEPCMD_16—Offset C90Ch" on page 2611	00000000h
C910h	4	"DEPCMDPAR2_17—Offset C910h" on page 2612	00000000h
C914h	4	"DEPCMDPAR1_17—Offset C914h" on page 2612	00000000h
C918h	4	"DEPCMDPAR0_17—Offset C918h" on page 2612	00000000h

Table 221. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C91Ch	4	"DEPCMD_17—Offset C91Ch" on page 2613	00000000h
C920h	4	"DEPCMDPAR2_18—Offset C920h" on page 2614	00000000h
C924h	4	"DEPCMDPAR1_18—Offset C924h" on page 2614	00000000h
C928h	4	"DEPCMDPAR0_18—Offset C928h" on page 2615	00000000h
C92Ch	4	"DEPCMD_18—Offset C92Ch" on page 2615	00000000h
C930h	4	"DEPCMDPAR2_19—Offset C930h" on page 2616	00000000h
C934h	4	"DEPCMDPAR1_19—Offset C934h" on page 2616	00000000h
C938h	4	"DEPCMDPAR0_19—Offset C938h" on page 2617	00000000h
C93Ch	4	"DEPCMD_19—Offset C93Ch" on page 2617	00000000h
C940h	4	"DEPCMDPAR2_20—Offset C940h" on page 2618	00000000h
C944h	4	"DEPCMDPAR1_20—Offset C944h" on page 2619	00000000h
C948h	4	"DEPCMDPAR0_20—Offset C948h" on page 2619	00000000h
C94Ch	4	"DEPCMD_20—Offset C94Ch" on page 2619	00000000h
C950h	4	"DEPCMDPAR2_21—Offset C950h" on page 2620	00000000h
C954h	4	"DEPCMDPAR1_21—Offset C954h" on page 2621	00000000h
C958h	4	"DEPCMDPAR0_21—Offset C958h" on page 2621	00000000h
C95Ch	4	"DEPCMD_21—Offset C95Ch" on page 2622	00000000h
C960h	4	"DEPCMDPAR2_22—Offset C960h" on page 2622	00000000h
C964h	4	"DEPCMDPAR1_22—Offset C964h" on page 2623	00000000h
C968h	4	"DEPCMDPAR0_22—Offset C968h" on page 2623	00000000h
C96Ch	4	"DEPCMD_22—Offset C96Ch" on page 2624	00000000h
C970h	4	"DEPCMDPAR2_23—Offset C970h" on page 2625	00000000h
C974h	4	"DEPCMDPAR1_23—Offset C974h" on page 2625	00000000h
C978h	4	"DEPCMDPAR0_23—Offset C978h" on page 2625	00000000h
C97Ch	4	"DEPCMD_23—Offset C97Ch" on page 2626	00000000h
C980h	4	"DEPCMDPAR2_24—Offset C980h" on page 2627	00000000h
C984h	4	"DEPCMDPAR1_24—Offset C984h" on page 2627	00000000h
C988h	4	"DEPCMDPAR0_24—Offset C988h" on page 2628	00000000h
C98Ch	4	"DEPCMD_24—Offset C98Ch" on page 2628	00000000h
C990h	4	"DEPCMDPAR2_25—Offset C990h" on page 2629	00000000h
C994h	4	"DEPCMDPAR1_25—Offset C994h" on page 2629	00000000h
C998h	4	"DEPCMDPAR0_25—Offset C998h" on page 2630	00000000h
C99Ch	4	"DEPCMD_25—Offset C99Ch" on page 2630	00000000h
C9A0h	4	"DEPCMDPAR2_26—Offset C9A0h" on page 2631	00000000h
C9A4h	4	"DEPCMDPAR1_26—Offset C9A4h" on page 2632	00000000h
C9A8h	4	"DEPCMDPAR0_26—Offset C9A8h" on page 2632	00000000h
C9ACh	4	"DEPCMD_26—Offset C9ACh" on page 2632	00000000h
C9B0h	4	"DEPCMDPAR2_27—Offset C9B0h" on page 2633	00000000h
C9B4h	4	"DEPCMDPAR1_27—Offset C9B4h" on page 2634	00000000h

Table 221. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR (Continued)

Offset	Size	Register ID—Description	Default Value
C9B8h	4	"DEPCMDPAR0_27—Offset C9B8h" on page 2634	00000000h
C9BCh	4	"DEPCMD_27—Offset C9BCh" on page 2635	00000000h
C9C0h	4	"DEPCMDPAR2_28—Offset C9C0h" on page 2635	00000000h
C9C4h	4	"DEPCMDPAR1_28—Offset C9C4h" on page 2636	00000000h
C9C8h	4	"DEPCMDPAR0_28—Offset C9C8h" on page 2636	00000000h
C9CCh	4	"DEPCMD_28—Offset C9CCh" on page 2637	00000000h
C9D0h	4	"DEPCMDPAR2_29—Offset C9D0h" on page 2638	00000000h
C9D4h	4	"DEPCMDPAR1_29—Offset C9D4h" on page 2638	00000000h
C9D8h	4	"DEPCMDPAR0_29—Offset C9D8h" on page 2638	00000000h
C9DCh	4	"DEPCMD_29—Offset C9DCh" on page 2639	00000000h
C9E0h	4	"DEPCMDPAR2_30—Offset C9E0h" on page 2640	00000000h
C9E4h	4	"DEPCMDPAR1_30—Offset C9E4h" on page 2640	00000000h
C9E8h	4	"DEPCMDPAR0_30—Offset C9E8h" on page 2641	00000000h
C9ECh	4	"DEPCMD_30—Offset C9ECh" on page 2641	00000000h
C9F0h	4	"DEPCMDPAR2_31—Offset C9F0h" on page 2642	00000000h
C9F4h	4	"DEPCMDPAR1_31—Offset C9F4h" on page 2642	00000000h
C9F8h	4	"DEPCMDPAR0_31—Offset C9F8h" on page 2643	00000000h
C9FCh	4	"DEPCMD_31—Offset C9FCh" on page 2643	00000000h
CC00h	4	"OCFG—Offset CC00h" on page 2644	00000000h
CC04h	4	"OCTL—Offset CC04h" on page 2645	00000040h
CC08h	4	"OEVT—Offset CC08h" on page 2646	80000000h
CC0Ch	4	"OEVTEN—Offset CC0Ch" on page 2648	00000000h
CC10h	4	"OSTS—Offset CC10h" on page 2649	00000019h
CC20h	4	"ADPCFG—Offset CC20h" on page 2650	00000000h
CC24h	4	"ADPCTL—Offset CC24h" on page 2650	00000000h
CC28h	4	"ADPEVT—Offset CC28h" on page 2651	00000000h
CC2Ch	4	"ADPEVTEN—Offset CC2Ch" on page 2652	00000000h
CC30h	4	"BCFG—Offset CC30h" on page 2653	00000000h
CC38h	4	"BCEVT—Offset CC38h" on page 2653	00000000h
CC3Ch	4	"BCEVTEN—Offset CC3Ch" on page 2654	00000000h

19.6.1 CAPLENGTH—Offset 0h

This register is used as an offset to add to register base to find the beginning of the Operational Register Space.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CAPLENGTH: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00960020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

HCIVERSION | RSVD0 | CAPLENGTH

Bit Range	Default & Access	Description
31:16	096h RO	**HCIVERSION:** This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0.xs
15:8	0h RO	**RSVD0:** Reserved.
7:0	20h RO	**CAPLENGTH:** This register is used as an offset to add to register base to find the beginning of the Operational Register Space.

19.6.2 HCSPARAMS1—Offset 4h

number of ports implemented is 2 because there is 1 DWC_USB2_HOST_NUM_U2_ROOT_PORTS and 1 DWC_USB3_HOST_NUM_U3_ROOT_PORT

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HCSPARAMS1: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0200017Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1

MAXPORTS | HCSPARAMS1_RSVD1 | MAXINTRS | MAXSLOTS

Bit Range	Default & Access	Description
31:24	02h RO	**MAXPORTS:** Number of Ports (MaxPorts). This field specifies the maximum Port Number value, i.e. the highest numbered Port Register Set that are addressable in the Operational Register Space (refer to Table 29). Valid values are in the range of 1h to FFh. The value in this field shall reflect the maximum Port Number value assigned by an xHCI Supported Protocol Capability, described in section 7.2. Software shall refer to these capabilities to identify whether a specific Port Number is valid, and the protocol supported by the associated Port Register Set.
23:19	0h RO	**HCSPARAMS1_RSVD1:** reserved

Bit Range	Default & Access	Description
18:8	1h RO	**MAXINTRS:** Number of Interrupters (MaxIntrs). This field specifies the number of Interrupters implemented on this host controller. Each Interrupter may be allocated to a MSI or MSI-X vector and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space (refer to section 5.5). Valid values are in the range of 1h to 400h. A 0 in this field is undefined.
7:0	7fh RO	**MAXSLOTS:** Number of Device Slots (MaxSlots). This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of 0 is reserved.

19.6.3 HCSPARAMS2—Offset 8h

Host Controller Structural Parameters 2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

HCSPARAMS2: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 140000F1h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 1	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	0 0 0 1

Field	Bits
MAXSCRATCHPADBUFS	31:27
SPR	26
HCSPARAMS2_RSVD1	25:13
IOCINTERVAL	12:8
ERSTMAX	7:4
IST	3:0

Bit Range	Default & Access	Description
31:27	02h RO	**MAXSCRATCHPADBUFS:** For xHCI 0.96,this field is Max Scratchpad Bufs / For xHCI 1.0, this field is Max Scratchpad Bufs Lo
26	1h RO	**SPR:** Scratchpad Restore (SPR)
25:13	0h RO	**HCSPARAMS2_RSVD1:** reserved
12:8	0h RO	**IOCINTERVAL:** This field is valid only for xHCI 0.96. For xHCI 1.0, this field is Reserved.
7:4	fh RO	**ERSTMAX:** Event Ring Segment Table Max (ERST Max)
3:0	1h RO	**IST:** Isochronous Scheduling Threshold (IST)

19.6.4 HCSPARAMS3—Offset Ch

Structural Parameters 3 Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

HCSPARAMS3: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07FF000Ah

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

U2_DEVICE_EXIT_LAT | HCSPARAMS3_RSVD | U1_DEVICE_EXIT_LAT

Bit Range	Default & Access	Description
31:16	07ffh RO	**U2_DEVICE_EXIT_LAT:** Reserved.
15:8	0h RO	**HCSPARAMS3_RSVD:** Reserved.
7:0	0ah RO	**U1_DEVICE_EXIT_LAT:** Reserved.

19.6.5 HCCPARAMS—Offset 10h

Capability Parameters Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

HCCPARAMS: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0220F04Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	1	1	0	0

XECP | MAXPSASIZE | HCCPARAMS_RSVD | SBD | FSE | NSS | LTC | LHRC | PIND | PPC | CSZ | BNC | AC64

Bit Range	Default & Access	Description
31:16	220h RO	**XECP:** Based on configuration, core automatically updates it

Bit Range	Default & Access	Description
15:12	fh RO	**MAXPSASIZE:** Maximum Primary Stream Array Size
11:10	0h RO	**HCCPARAMS_RSVD:** Reserved
9	0h RO	**SBD:** Secondary Bandwidth Domain Reporting (SBD)
8	0h RO	**FSE:** For xHCI 0.96, this field is Force Stopped Event (FSE) / For xHCI 1.0, this field is Parse All Event Data (PAE)
7	0h RO	**NSS:** No Secondary SID Support (NSS). This flag indicates whether the host controller implementation supports Secondary Stream IDs. A 1 in this bit indicates that Secondary Stream ID decoding is not supported. A 0 in this bit indicates that Secondary Stream ID decoding is supported. (refer to Sections 4.12.2 and 6.2.3).
6	1h RO	**LTC:** Latency Tolerance Messaging Capability (LTC). This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A 1 in this bit indicates that LTM is supported. A 0 in this bit indicates that LTM is not supported. Refer to section 4.13.1 for more information on LTM.
5	0h RO	**LHRC:** Light HC Reset Capability (LHRC). This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A 1 in this bit indicates that Light Host Controller Reset is supported. A 0 in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the Light Host Controller Reset (LHCRST) flag in the USBCMD register (refer to Section 5.4.1).
4	0h RO	**PIND:** Port Indicators (PIND). This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a 1, the port status and control registers include a read/writeable field for controlling the state of the port indicator. Refer to Section 5.4.8 for definition of the Port Indicator Control field.
3	1h RO	**PPC:** Port Power Control (PPC). This flag indicates whether the host controller implementation includes port power control. A 1 in this bit indicates the ports have port power switches. A 0 in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register (refer to Section 5.4.8).
2	1h RO	**CSZ:** Context Size (CSZ). If this bit is set to 1, then the xHC uses 64 byte Context data structures. If this bit is cleared to 0, then the xHC uses 32 byte Context data structures. Note: This flag does not apply to Stream Contexts.
1	0h RO	**BNC:** BW Negotiation Capability (BNC). This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: for Value 0 Description BW Negotiation not implemented. for Value 1 DescriptionBW Negotiation implemented. Refer to section 4.16 of XHCI specification for more information on Bandwidth Negotiation.
0	0h RO	**AC64:** 64-bit Addressing Capability (AC64). This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this flag have the following interpretation: for Value 0 Description 32-bit address memory pointers implemented. for Value 1 description 64-bit address memory pointers implemented. If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.

19.6.6 DBOFF—Offset 14h

Doorbell Offset Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DBOFF: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000480h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0

DOORBELL_ARRAY_OFFSET | RSVD4

Bit Range	Default & Access	Description
31:2	120h RO	**DOORBELL_ARRAY_OFFSET:** Based on configuration, core automatically updates it
1:0	0h RO	**RSVD4:** Reserved

19.6.7 RTSOFF—Offset 18h

Runtime Register Space Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RTSOFF: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000440h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0

RUNTIME_REG_SPACE_OFFSET | RSVD5

Bit Range	Default & Access	Description
31:5	22h RO	**RUNTIME_REG_SPACE_OFFSET:** Based on configuration, core automatically updates it
4:0	0h RO	**RSVD5:** Reserved

19.6.8 Rsvd_HC—Offset 1Ch

reserved

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Rsvd_HC: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:0
Default	0000 0000 0000 0000 0000 0000 0000 0000
Field	RSVD6

Bit Range	Default & Access	Description
31:0	0h RO	**RSVD6:** Reserved.

19.6.9 USBCMD—Offset 20h

USB Command Register Bit Definitions

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

USBCMD: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6:4	3	2	1	0
Default	0000 0000 0000 0000 0000	0	0	0	0	0	000	0	0	0	0
Field	RSVD8	EU3S	EWE	CRS	CSS	LHCRST	RSVD7	HSEE	INTE	HCRST	R_S

Bit Range	Default & Access	Description
31:12	0h RO	**RSVD8:** reserved
11	0h RW	**EU3S:** Enable U3 MFINDEX Stop (EU3S) - RW. Default = 0. When set to 1, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0 the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, Training, or Powered-off state. Refer to section 4.14.2 for more information.
10	0h RW	**EWE:** Enable Wrap Event (EWE) - RW. Default = 0. When set to 1, the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to 0 no MFINDEX Wrap Events are generated. Refer to section 4.14.2 for more information. When this register is exposed by a Virtual Function (VF), the generation of MFINDEX Wrap Events to VFs shall be emulated by the VMM.

Bit Range	Default & Access	Description
9	0h RW	**CRS:** Controller Restore State: This command is similar to the USBCMD. CRS bit in host mode and initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'.
8	0h RW	**CSS:** Controller Save State: This command is similar to the USBCMD. CSS bit in host mode and initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'.
7	0h RW	**LHCRST:** Light Host Controller Reset (LHCRST) RO or RW. Optional normative. Default = 0. If the Light HC Reset Capability (LHRC) bit in the HCCPARAMS register is 1, then this flag allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0 indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a 1 indicates the Light Host Controller Reset has not yet completed. If not implemented, a read of this flag shall always return a 0. All registers in the Aux Power well shall maintain the values that had been asserted prior to the Light Host Controller Reset. Refer to section 4.23.1 for more information. When this register is exposed by a Virtual Function (VF), this bit only generates a Light Reset to the xHC instance presented by the selected VF, e.g. Disable the VFs device slots and set the associated VF Run bit to Stopped. Refer to section 8 for more information.
6:4	0h RO	**RSVD7:** Reserved
3	0h RW	**HSEE:** Host System Error Enable (HSEE) RW. Default = 0. When this bit is a 1, and the HSE bit in the USBSTS register is a 1, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit. Refer to section 4.10.2.6 for more information. When this register is exposed by a Virtual Function (VF), the effect of the assertion of this bit on the Physical Function (PF0) is determined by the VMM. Refer to section 8 for more information.
2	0h RW	**INTE:** Interrupter Enable (INTE) RW. Default = 0. This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a 1, then Interrupter host system interrupt generation is allowed, e.g. the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSI-X, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism. When this register is exposed by a Virtual Function (VF), this bit only enables the set of Interrupters assigned to the selected VF. Refer to section 7.7.2 for more information.
1	0h RW	**HCRST:** Host Controller Reset (HCRST) RW. Default = 0. This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset. When software writes a 1 to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on the USB is immediately terminated. A USB reset shall not be driven on USB2 downstream ports, however a Hot or Warm Reset shall be initiated on USB3 Root Hub downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Software shall reinitialize the host controller as described in Section 4.1 in order to return the host controller to an operational state. This bit is cleared to 0 by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this bit and shall not write any xHC Operational or Runtime registers until while HCRST is 1. Note, the completion of the xHC reset process is not gated by the Root Hub port reset process. Software shall not set this bit to 1 when the HCHalted (HCH) bit in the USBSTS register is a 0. Attempting to reset an actively running host controller may result in undefined behavior. When this register is exposed by a Virtual Function (VF), this bit only resets the xHC instance presented by the selected VF. Refer to section 8 for more information.

Bit Range	Default & Access	Description
0	0h RW	**R_S:** Run/Stop (R/S) RW. Default = 0. 1 = Run. 0 = Stop. When set to a 1, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a 1. When this bit is cleared to 0, the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. Refer to section 5.4.1.1 for more information on how R/S shall be managed. The xHC shall halt within 16 ms. after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a 1 to this flag unless the xHC is in the Halted state (i.e. HCH in the USBSTS register is 1). Doing so may yield undefined results. Writing a 0 to this flag when the xHC is in the Running state (i.e. HCH = 0) and any Event Rings are in the Event Ring Full state (refer to section 4.9.4) may result in lost events. When this register is exposed by a Virtual Function (VF), this bit only controls the run state of the xHC instance presented by the selected VF. Refer to section 8 for more information.

19.6.10 USBSTS—Offset 24h

USB Command Register Bit Definitions

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

USBSTS: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
RSVD11																			HCE	CNR	SRE	RSS	SSS	RSVD10			PCD	EINT	HSE	RSVD9	HCH

Bit Range	Default & Access	Description
31:13	0h RO	**RSVD11:** reserved
12	0h RO	**HCE:** Host Controller Error (HCE) - RO. Default = 0. 0' = No internal xHC error conditions exist '1' = Internal xHC error condition. This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC. Refer to section 4.24.1 of xhci specification for more information.
11	0h RO	**CNR:** Controller Not Ready (CNR) - RO. Default = '1'. '0' = Ready '1' = Not Ready. Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared ('0') until the next Chip Hardware Reset.
10	0h RO	**SRE:** Save/Restore Error (SRE) -RW1C. Default = '0'. If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'. Refer to section 4.23.2 of xhci specification for more information.
9	0h RO	**RSS:** Restore State Status: This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.RSS to '0'.
8	0h RO	**SSS:** Save State Status: This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'

Bit Range	Default & Access	Description
7:5	0h RO	**RSVD10:** reserved
4	0h RW	**PCD:** Reserved.
3	0h RO	**EINT:** Reserved.
2	0h RO	**HSE:** Reg field HSE
1	0h RO	**RSVD9:** reserved
0	1h RO	**HCH:** Reg field HCH

19.6.11 PAGESIZE—Offset 28h

Page Size Register Bit Definitions. This register is used by software to enable or disable the reporting of the reception of specific USB Device Notification Transaction Packets. A Notification Enable (Nx, where x = 0 to 15) flag is defined for each of the 16 possible device notification types. If a flag is set for a specific notification type, a Device Notification Event shall be generated when the respective notification packet is received. After reset all notifications are disabled. Refer to section 6.4.2.7. This register shall be written as a Dword. Byte writes produce undefined results.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PAGESIZE: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 31:16	Bits 15:0
RSVD12	PAGE_SIZE

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD12:** reserved
15:0	1h RO	**PAGE_SIZE:** Reg field PAGE_SIZE

19.6.12 DNCTRL—Offset 34h

Device Notification Register Bit Definitions.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DNCTRL: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD13 (31:16), N0_N15 (15:0)

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD13:** reserved
15:0	0h RW	**N0_N15:** Reg field N0_N15

19.6.13 CRCR_LO—Offset 38h

Register CRCR_LO

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CRCR_LO: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: CMD_RING_PNTR (31:6), RSVD14 (5:4), CRR (3), CA (2), CS (1), RCS (0)

Bit Range	Default & Access	Description
31:6	0h RW	**CMD_RING_PNTR:** Command Ring Pointer - RW. Default = 0. This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running (CRR) = 1. If the CRCR is written while the Command Ring is stopped (CCR = 0), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CCR = 0) then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns 0.
5:4	0h RO	**RSVD14:** reserved

Bit Range	Default & Access	Description
3	0h RW	**CRR:** Command Ring Running (CRR) - RO. Default = 0. This flag is set to 1 if the Run/Stop (R/S) bit is 1 and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to 0 when the Command Ring is stopped after writing a 1 to the Command Stop (CS) or Command Abort (CA) flags, or if the R/S bit is cleared to 0.
2	0h RW	**CA:** Command Abort (CA) - RW1S. Default = 0. Writing a 1 to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. Refer to section 4.6.1.2 for more information on aborting a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0. Reading this bit always returns 0.
1	0h RW	**CS:** Command Stop (CS) - RW1S. Default = 0. Writing a 1 to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. Refer to section 4.6.1.1 for more information on stopping a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0. Reading this bit shall always return 0.
0	0h RW	**RCS:** Ring Cycle State (RCS) - RW. This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Refer to section 4.9.3 for more information. Writes to this flag are ignored if Command Ring Running (CRR) is 1. If the CRCR is written while the Command Ring is stopped (CRR = 0), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CRR = 0), then the Command Ring shall begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns 0.

19.6.14 CRCR_HI—Offset 3Ch

Register CRCR_HI

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CRCR_HI: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CMD_RING_PNTR

Bit Range	Default & Access	Description
31:0	0h RW	**CMD_RING_PNTR:** Reg field CMD_RING_PNTR

19.6.15 DCBAAP_LO—Offset 50h

Register DCBAAP_LO

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DCBAAP_LO: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DEVICE_CONTEXT_BAAP | RSVD16

Bit Range	Default & Access	Description
31:6	0h RW	**DEVICE_CONTEXT_BAAP:** Reg field DEVICE_CONTEXT_BAAP
5:0	0h RO	**RSVD16:** reserved

19.6.16 DCBAAP_HI—Offset 54h

Register DCBAAP_HI

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DCBAAP_HI: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DEVICE_CONTEXT_BAAP

Bit Range	Default & Access	Description
31:0	0h RW	**DEVICE_CONTEXT_BAAP:** Reg field DEVICE_CONTEXT_BAAP

19.6.17 CONFIG—Offset 58h

Configure Register Bit Definitions. This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST). The initial conditions of a port are described in section 4.19 of xhci specification .

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CONFIG: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:8	RSVD17
7:0	MAXSLOTSEN

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD17:** reserved
7:0	0h RW	**MAXSLOTSEN:** Reg field MAXSLOTSEN

19.6.18 PORTSC1—Offset 420h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PORTSC1: [BAR] + 420h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 000002A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0

Bits	Field
31	WPR
30	DR
29:28	RSVD20
27	WOE
26	WDE
25	WCE
24	RSVD19
23	CEC
22	PLC
21	PRC
20	OCC
19	WRC
18	PEC
17	CSC
16	LWS
15:14	PIC
13:10	PORTSPEED
9	PP
8:5	PLS
4	PR
3	OCA
2	RSVD18
1	PED
0	CCS

Bit Range	Default & Access	Description
31	0h RW	**WPR:** Warm Port Reset (WPR) RW1S/RsvdZ. Default = 0. When software writes a 1 to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to 1. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return 0 when read. Refer to section 4.19.5.1. of XHCI specification. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
30	0h RW	**DR:** Device Removable (DR) - RO. This flag indicates if this port has a removable device attached. 1 = Device is non-removable. 0 = Device is removable.
29:28	0h RO	**RSVD20:** reserved
27	0h RW	**WOE:** Wake on Over-current Enable (WOE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to over-current conditions as system wake-up eventsn. Refer to section 4.15 for operational model.
26	0h RW	**WDE:** Wake on Disconnect Enable (WDE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to device disconnects as system wake-up eventsn. Refer to section 4.15 for operational model.
25	0h RW	**WCE:** Wake on Connect Enable (WCE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to device connects as system wake-up events . Refer to section 4.15 for operational model.
24	0h RO	**RSVD19:** reserved
23	0h RW	**CEC:** Port Config Error Change (CEC) RW1CS/RsvdZ. Default = 0. This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 for more information on change bit usage. Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be RsvdZ.
22	0h RW	**PLC:** Port Link State Change (PLC) RW1CS. Default = 0. This flag is set to 1 due to the following PLS transitions mentioned in the XHCI specification
21	0h RW	**PRC:** Port Reset Change (PRC) RW1CS. Default = 0. This flag is set to 1 due to a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to 1 if the reset processing was forced to terminate due to software clearing PP or PED to '0'. 0 = No change. 1 = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5. Refer to section 4.19.2 for more information on change bit usage.
20	0h RW	**OCC:** Over-current Change (OCC) RW1CS. Default = 0. This bit shall be set to a 1 when there is a 0 to 1 or 1 to 0 transition of Over-current Active (OCA). Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage.
19	0h RW	**WRC:** Warm Port Reset Change (WRC) RW1CS/RsvdZ. Default = 0. This bit is set when Warm Reset processing on this port completes. 0 = No change. 1 = Warm Reset complete. Note that this flag shall not be set to 1 if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.1. Refer to section 4.19.2 for more information on change bit usage. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
18	0h RW	**PEC:** Port Enabled/Disabled Change (PEC) RW1CS. Default = 0. 1 = change in PED. 0 = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to 0. Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage. For a USB2 protocol port, this bit shall be set to 1 only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to 1.

Bit Range	Default & Access	Description
17	0h RW	**CSC:** Connect Status Change (CSC) RW1CS. Default = 0. 1 = Change in CCS. 0 = No change. This flag indicates a change has occurred in the ports Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to 0, or the CAS transition was due to software setting WPR to 1. The xHC sets this bit to 1 for all changes to the port device connect status , even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be setting an already-set bit (i.e., the bit will remain 1). Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage.
16	0h RW	**LWS:** Port Link State Write Strobe (LWS) RW. Default = 0. When this bit is set to 1 on a write reference to this register, this flag enables writes to the PLS field. When 0, write data in PLS field is ignored. Reads to this bit return 0.
15:14	0h RW	**PIC:** Port Indicator Control (PIC) RWS. Default = 0. Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a 0.
13:10	0h RW	**PORTSPEED:** Port Speed (Port Speed) ROS. Default = 0. This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected (CCS = 1) in all other cases this field shall indicate Undefined Speed. (more information in the XHCI specification)
9	1h RW	**PP:** Port Power (PP) RWS. Default = 1. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = 0 if PPC = 0. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again , undefined behavior may occur if this procedure is not followed. 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' = on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a 1 to 0 (removing power from the port). Note: If this is an SSIC Port, then the DSP Disconnect process is initiated by '1' to '0' transition of PP. Refer to section 5.1.2 in the SSIC Spec for more information. Refer to section 4.19.4 for more information.
8:5	5h RW	**PLS:** Port Link State (PLS) RWS. Default = RxDetect (5). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port.
4	0h RW	**PR:** Port Reset (PR) RW1S. Default = 0. 1 = Port Reset signaling is asserted. 0 = Port is not in Reset. When software writes a 1 to this bit generating a 0 to 1 transition, the bus reset sequence is initiated ; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a 1 to this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1. This flag is 0 if PP is 0.
3	0h RW	**OCA:** Over-current Active (OCA) RO. Default = 0. 1 = This port currently has an over-current condition. 0 = This port does not have an over-current condition. This bit shall automatically transition from a 1 to a 0 when the over-current condition is removed.
2	0h RO	**RSVD18:** reserved

Bit Range	Default & Access	Description
1	0h RW	**PED:** Port Enabled/Disabled (PED) RW1CS. Default = 0. 1 = Enabled. 0 = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a 1 to this flag. A port may be disabled by software writing a 1 to this flag. This flag shall automatically be cleared to 0 by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = 0) downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = 1) to transition PED to 1 and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to 1 upon the completion of successful link training. When the port is in the Disabled state, software shall write a 5 (RxDetect) to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2. PED shall automatically be cleared to 0 when PR is set to 1, and set to 1 when PR transitions from 1 to 0 after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a 1, it shall also write a 0 to the PR bit . This flag is 0 if PP is 0.
0	0h RW	**CCS:** Current Connect Status (CCS) ROS. Default = 0. 1 = A device is connected to the port. 0 = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to 1. Refer to sections 4.19.3 and 4.19.4 for more details on the Connect Status Change (CSC) assertion conditions. This flag is 0 if PP is 0.

19.6.19 PORTPMSC1—Offset 424h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PORTPMSC1: [BAR] + 424h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0

31:28	27:16	15:8	7:4	3	2:0
PORT_TEST_CONTROL	RSVD21	L1DS	HIRD	RWE	L1S

Bit Range	Default & Access	Description
31:28	0h RW	**PORT_TEST_CONTROL:** reserved
27:16	0h RO	**RSVD21:** reserved
15:8	0h RW	**L1DS:** Reg field L1DSLOT

Bit Range	Default & Access	Description
7:4	0h RW	**HIRD:** Host Initiated Resume Duration (HIRD) - RW. Default = '0'. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. The HIRD value is encoded as follows: Value Description 0h 50 s. (default) 1h 125 s. 2h 200 s. Fh 1.175 ms. The value of 0000b is interpreted as 50 s. Each incrementing value up adds 75 s. to the previous value. For example, 0001b is 125 s, 0010b is 200s and so on. Based on this rule, the maximum value resume drive time is at encoding value 1111b which represents 1.2ms. Note that the HIRD field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 of xhci specification for more information on HIRD use. Refer to Section 4.1 of the USB2 LPM spec for more information on the use of the HIRD field.
3	0h RW	**RWE:** Port Test Control
2:0	0h RO	**L1S:** L1 Status (L1S) - RO. Default = 0. This field is used by software to determine whether an L1based suspend request (LMP transaction) was successful, specifically: Value Meaning 0 Invalid - This field shall be ignored by software. 1 Success - Port successfully transitioned to L1 (ACK) 2 Not Yet - Device is unable to enter L1 at this time (NYET) 3 Not Supported -Device does not support L1 transitions (STALL) 4 Timeout/ Error -Device failed to respond to the LPM Transaction or an error occurred 5-7 Reserved The value of this field is only valid when the port resides in the L0 or L1 state (PLS = '0' or '2'). Refer to section 4.23.5.1.1 for more information.

19.6.20 PORTLI—Offset 428h

Port Link Info Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PORTLI: [BAR] + 428h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD22																LINK_ERROR_COUNT															

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD22:** reserved
15:0	0h RO	**LINK_ERROR_COUNT:** Reg field LINK_ERROR_COUNT

19.6.21 PORTHLPMC—Offset 42Ch

The definition of the fields in the PORTHLPMC register depend on the USB protocol supported by the port. This register is in the Aux Power well. It is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST).

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PORTHLPMC: [BAR] + 42Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD | HIRDD | L1TIMEOUT | HIRDM

Bit Range	Default & Access	Description
31:14	0h RO	**RSVD:** reserved
13:10	0h RW	**HIRDD:** Best Effort Service Latency Deep (BESLD) - RWS. Default = 0. System software sets this field to indicate to the recipient device how long the xHC will drive resume on an exit from U2. Refer to section 4.23.5.1.1.1 for more information on BESLD use. The BESLD value encoding is defined in Table 13. Refer to section 5.2.6 for information on how DBESLD may be used to establish an initial value for BESLD
9:2	0h RW	**L1TIMEOUT:** L1 Timeout RWS. Default = 00h. Timeout value for the L1 inactivity timer (LPM Timer). This field shall be set to 00h by the assertion of PR to 1. Refer to section 4.23.5.1.1.1 for more information on L1 Timeout operation. The following are permissible values: for 00h 128 s. (default). for 01h 256 s. for 02h 512 s. for 03h 768 s. . . . for FFh 65,280 s.
1:0	0h RW	**HIRDM:** Host Initiated Resume Duration Mode (HIRDM) - RWS. Default = 0h. Indicates which HIRD value should be used. The following are permissible values: for 0 Initiate L1 using BESL only on timeout. (default). for 1 Initiate L1 using BESLD on timeout. If rejected by device, initiate L1 using BESL. for 3-2 Reserved.

19.6.22 PORTSC2—Offset 430h

A host controller shall implement one or more port registers. The number of port registers implemented by a particular instantiation of a host controller is documented in the HCSPARAMS1 register (Section 5.3.3). Software uses this information as an input parameter to determine how many ports need to be serviced

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PORTSC2: [BAR] + 430h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 000002A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0

WPR | DR | RSVD25 | WOE | WDE | WCE | RSVD24 | CEC | PLC | PRC | OCC | WRC | PEC | CSC | LWS | PIC | PORTSPEED | PP | PLS | PR | OCA | RSVD23 | PED | CCS

Bit Range	Default & Access	Description
31	0h RW	**WPR:** Warm Port Reset (WPR) RW1S/RsvdZ. Default = 0. When software writes a 1 to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to 1. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return 0 when read. Refer to section 4.19.5.1. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
30	0h RW	**DR:** Device Removable (DR) - RO. This flag indicates if this port has a removable device attached. 1 = Device is non-removable. 0 = Device is removable.
29:28	0h RO	**RSVD25:** reserved
27	0h RW	**WOE:** Wake on Over-current Enable (WOE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to over-current conditions as system wake-up eventsn. Refer to section 4.15 for operational model.
26	0h RW	**WDE:** Wake on Disconnect Enable (WDE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to device disconnects as system wake-up eventsn. Refer to section 4.15 for operational model.
25	0h RW	**WCE:** Wake on Connect Enable (WCE) RWS. Default = 0. Writing this bit to a 1 enables the port to be sensitive to device connects as system wake-up events . Refer to section 4.15 for operational model.
24	0h RO	**RSVD24:** reserved
23	0h RW	**CEC:** Port Config Error Change (CEC) RW1CS/RsvdZ. Default = 0. This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.2 of XHCI specification for more information on change bit usage. Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be RsvdZ.
22	0h RW	**PLC:** Port Link State Change (PLC) RW1CS. Default = 0. This flag is set to 1 due to the PLS transitions in the XHCI specification
21	0h RW	**PRC:** Port Reset Change (PRC) RW1CS. Default = 0. This flag is set to 1 due to a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to 1 if the reset processing was forced to terminate due to software clearing PP or PED to '0'. 0 = No change. 1 = Reset complete. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.of XHCI specification. Refer to section 4.19.2 of XHCI specification. for more information on change bit usage.
20	0h RW	**OCC:** Over-current Change (OCC) RW1CS. Default = 0. This bit shall be set to a 1 when there is a 0 to 1 or 1 to 0 transition of Over-current Active (OCA). Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage.
19	0h RW	**WRC:** Warm Port Reset Change (WRC) RW1CS/RsvdZ. Default = 0. This bit is set when Warm Reset processing on this port completes. 0 = No change. 1 = Warm Reset complete. Note that this flag shall not be set to 1 if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. Refer to section 4.19.5.1. Refer to section 4.19.2 for more information on change bit usage. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be RsvdZ.
18	0h RW	**PEC:** Port Enabled/Disabled Change (PEC) RW1CS. Default = 0. 1 = change in PED. 0 = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to 0. Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage. For a USB2 protocol port, this bit shall be set to 1 only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to 1.

Bit Range	Default & Access	Description
17	0h RW	**CSC:** Connect Status Change (CSC) RW1CS. Default = 0. 1 = Change in CCS. 0 = No change. This flag indicates a change has occurred in the ports Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to 0, or the CAS transition was due to software setting WPR to 1. The xHC sets this bit to 1 for all changes to the port device connect status , even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be setting an already-set bit (i.e., the bit will remain 1). Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 for more information on change bit usage.
16	0h RW	**LWS:** Port Link State Write Strobe (LWS) RW. Default = 0. When this bit is set to 1 on a write reference to this register, this flag enables writes to the PLS field. When 0, write data in PLS field is ignored. Reads to this bit return 0.
15:14	0h RW	**PIC:** Port Indicator Control (PIC) RWS. Default = 0. Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a 0
13:10	0h RW	**PORTSPEED:** Port Speed (Port Speed) ROS. Default = 0. This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected (CCS = 1) in all other cases this field shall indicate Undefined Speed.
9	1h RW	**PP:** Port Power (PP) RWS. Default = 1. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = 0 if PPC = 0. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again , undefined behavior may occur if this procedure is not followed. 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' = on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a 1 to 0 (removing power from the port). Note: If this is an SSIC Port, then the DSP Disconnect process is initiated by '1' to '0' transition of PP. Refer to section 5.1.2 in the SSIC Spec for more information. Refer to section 4.19.4 for more information.
8:5	5h RW	**PLS:** Port Link State (PLS) RWS. Default = RxDetect (5). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port.
4	0h RW	**PR:** Port Reset (PR) RW1S. Default = 0. 1 = Port Reset signaling is asserted. 0 = Port is not in Reset. When software writes a 1 to this bit generating a 0 to 1 transition, the bus reset sequence is initiated ; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a 1 to this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1. of XHCI specification. This flag is 0 if PP is 0.
3	0h RW	**OCA:** Over-current Active (OCA) RO. Default = 0. 1 = This port currently has an over-current condition. 0 = This port does not have an over-current condition. This bit shall automatically transition from a 1 to a 0 when the over-current condition is removed.
2	0h RO	**RSVD23:** reserved

Bit Range	Default & Access	Description
1	0h RW	**PED:** Port Enabled/Disabled (PED) RW1CS. Default = 0. 1 = Enabled. 0 = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a 1 to this flag. A port may be disabled by software writing a 1 to this flag. This flag shall automatically be cleared to 0 by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = 0) downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = 1) to transition PED to 1 and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to 1 upon the completion of successful link training. When the port is in the Disabled state, software shall write a 5 (RxDetect) to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2. of xhci specification. PED shall automatically be cleared to 0 when PR is set to 1, and set to 1 when PR transitions from 1 to 0 after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a 1, it shall also write a 0 to the PR bit. This flag is 0 if PP is 0.
0	0h RW	**CCS:** Current Connect Status (CCS) ROS. Default = 0. 1 = A device is connected to the port. 0 = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to 1. Refer to sections 4.19.3 and 4.19.4 for more details on the Connect Status Change (CSC) assertion conditions. This flag is 0 if PP is 0.

19.6.23 PORTPMSC2—Offset 434h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PORTPMSC2: [BAR] + 434h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD26															FLA	U2_TIMEOUT								U1_TIMEOUT							

Bit Range	Default & Access	Description
31:17	0h RO	**RSVD26:** reserved
16	0h RW	**FLA:** Reg field FLA
15:8	0h RW	**U2_TIMEOUT:** Reg field U2_TIMEOUT
7:0	0h RW	**U1_TIMEOUT:** Reg field U1_TIMEOUT

19.6.24 MFINDEX—Offset 440h

Microframe Index Register Bit Definitions.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MFINDEX: [BAR] + 440h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD27 (bits 31:14) | MICROFRAME_INDEX (bits 13:0)

Bit Range	Default & Access	Description
31:14	0h RO	**RSVD27:** reserved
13:0	0h RO	**MICROFRAME_INDEX:** Reg field MICROFRAME_INDEX

19.6.25 RsvdZ—Offset 444h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RsvdZ: [BAR] + 444h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD28 (bits 31:0)

Bit Range	Default & Access	Description
31:0	0h RO	**RSVD28:** reserved

19.6.26 IMAN—Offset 460h

Interrupter Management Register Bit Definitions.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

IMAN: [BAR] + 460h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD29																														IE	IP

Bit Range	Default & Access	Description
31:2	0h RO	**RSVD29:** reserved
1	0h RW	**IE:** Interrupt Enable (IE) RW. Default = 0. This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set (1), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is 0, then the Interrupter is prohibited from generating interrupts.
0	0h RW	**IP:** Interrupt Pending (IP) - RW1C. Default = 0. This flag represents the current state of the Interrupter. If IP = 1, an interrupt is pending for this Interrupter. A 0 value indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.5 of XHCI specification for the conditions that modify the state of this flag.

19.6.27 IMOD—Offset 464h

Interrupter Moderation Register. Software may use this register to pace (or even out) the delivery of interrupts to the host CPU. This register provides a guaranteed inter-interrupt delay between interrupts asserted by the xHC, regardless of USB traffic conditions. To independently validate configuration settings, software may use the following algorithm to convert the inter-interrupt Interval value to the common 'interrupts/sec' performance metric:

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

IMOD: [BAR] + 464h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000FA0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0
IMODC																IMODI															

Bit Range	Default & Access	Description
31:16	0h RW	**IMODC:** Interrupt Moderation Counter (IMODC) - RW. Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate.

Bit Range	Default & Access	Description
15:0	fa0h RW	**IMODI:** Interrupt Moderation Interval (IMODI) - RW. Default = '4000' (~1ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty.

19.6.28 ERSTSZ—Offset 468h

Event Ring Segment Table Size Register Bit Definitions.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ERSTSZ: [BAR] + 468h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD30																ERS_TABLE_SIZE															

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD30:** reserved
15:0	0h RW	**ERS_TABLE_SIZE:** Event Ring Segment Table Size RW. Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register (5.3.4). For Secondary Interrupters: Writing a value of 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled.

19.6.29 RsvdP—Offset 46Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RsvdP: [BAR] + 46Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD31

Bit Range	Default & Access	Description
31:0	0h RO	**RSVD31:** reserved

19.6.30 ERSTBA_LO—Offset 470h

Register ERSTBA_LO

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO: [BAR] + 470h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

ERS_TABLE_BAR | RSVD32

Bit Range	Default & Access	Description
31:4	0h RW	**ERS_TABLE_BAR:** Reg field ERS_TABLE_BAR
3:0	0h RO	**RSVD32:** reserved

19.6.31 ERSTBA_HI—Offset 474h

Register ERSTBA_HI

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI: [BAR] + 474h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERS_TABLE_BAR

Bit Range	Default & Access	Description
31:0	0h RW	**ERS_TABLE_BAR:** Reg field ERS_TABLE_BAR

19.6.32 ERDP_LO—Offset 478h

Register ERDP_LO

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ERDP_LO: [BAR] + 478h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERD_PNTR | EHB | DESI

Bit Range	Default & Access	Description
31:4	0h RW	**ERD_PNTR:** Reg field ERD_PNTR
3	0h RW	**EHB:** HC OS Owned Semaphore HC BIOS Owned Semaphore USB SMI Enable SMI on Host System Error Enable SMI on OS Ownership Enable SMI on PCI Command Enable SMI on BAR Enable SMI on Event Interrupt SMI on Host System Error SMI on OS Ownership Change SMI on PCI Command SMI on BAR Compatible Port Count HC OS Owned Semaphore HC BIOS Owned Semaphore USB SMI Enable SMI on Host System Error Enable SMI on OS Ownership Enable SMI on PCI Command Enable SMI on BAR Enable SMI on Event Interrupt SMI on Host System Error SMI on OS Ownership Change SMI on PCI Command SMI on BAR Compatible Port Count
2:0	0h RW	**DESI:** Dequeue ERST Segment Index (DESI) RW. Default = 0. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

19.6.33 ERDP_HI—Offset 47Ch

Register ERDP_HI

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ERDP_HI: [BAR] + 47Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ERD_PNTR

Bit Range	Default & Access	Description
31:0	0h RW	**ERD_PNTR:** Reg field ERD_PNTR

19.6.34 DB_0—Offset 480h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_0: [BAR] + 480h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DB_STREAM_ID | RSVD33 | DB_TARGET

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.35 DB_1—Offset 484h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_1: [BAR] + 484h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:16	15:8	7:0
Default	0000 0000 0000 0000	0000 0000	0000 0000
Field	DB_STREAM_ID	RSVD33	DB_TARGET

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.36 DB_2—Offset 488h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_2: [BAR] + 488h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DB_STREAM_ID																RSVD33								DB_TARGET							

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.37 DB_3—Offset 48Ch

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_3: [BAR] + 48Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DB_STREAM_ID (31:16) | RSVD33 (15:8) | DB_TARGET (7:0)

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.38 DB_4—Offset 490h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_4: [BAR] + 490h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:8	Bits 7:0
DB_STREAM_ID	RSVD33	DB_TARGET

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.39 DB_5—Offset 494h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_5: [BAR] + 494h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:8	7:0
DB_STREAM_ID	RSVD33	DB_TARGET

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.40 DB_6—Offset 498h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_6: [BAR] + 498h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:16	15:8	7:0
Default	0000 0000 0000 0000	0000 0000	0000 0000
Field	DB_STREAM_ID	RSVD33	DB_TARGET

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.41 DB_7—Offset 49Ch

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_7: [BAR] + 49Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DB_STREAM_ID																RSVD33								DB_TARGET							

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.42 DB_8—Offset 4A0h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_8: [BAR] + 4A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DB_STREAM_ID (31:16)	RSVD33 (15:8)	DB_TARGET (7:0)

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.43 DB_9—Offset 4A4h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_9: [BAR] + 4A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DB_STREAM_ID																RSVD33								DB_TARGET							

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.44 DB_10—Offset 4A8h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_10: [BAR] + 4A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

31:16	15:8	7:0
DB_STREAM_ID	RSVD33	DB_TARGET

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.45 DB_11—Offset 4ACh

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_11: [BAR] + 4ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Field	DB_STREAM_ID				RSVD33		DB_TARGET	

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.46 DB_12—Offset 4B0h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_12: [BAR] + 4B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:16	Bits 15:8	Bits 7:0
DB_STREAM_ID	RSVD33	DB_TARGET

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.47 DB_13—Offset 4B4h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_13: [BAR] + 4B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DB_STREAM_ID																RSVD33								DB_TARGET							

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.48 DB_14—Offset 4B8h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_14: [BAR] + 4B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DB_STREAM_ID																RSVD33								DB_TARGET							

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.49 DB_15—Offset 4BCh

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DB_15: [BAR] + 4BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							DB_STREAM_ID												RSVD33								DB_TARGET				

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.50 DB_16—Offset 4C0h

The Doorbell Array is organized as an array of up to 256 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DB_16: [BAR] + 4C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DB_STREAM_ID																RSVD33								DB_TARGET							

Bit Range	Default & Access	Description
31:16	0h RW	**DB_STREAM_ID:** DB Stream ID - RW. Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams) 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
15:8	0h RO	**RSVD33:** reserved

Bit Range	Default & Access	Description
7:0	0h RW	**DB_TARGET:** DB Target RW. Doorbell Target. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) for Value 0 the Definition is Reserved for Value 1 the Definition is Control EP 0 Enqueue Pointer Update for Value 2 the Definition is EP 1 OUT Enqueue Pointer Update for Value 3 the Definition is EP 1 IN Enqueue Pointer Update for Value 4 the Definition is EP 2 OUT Enqueue Pointer Update for Value 5 the Definition is EP 2 IN Enqueue Pointer Update . . . for Value 30 the Definition is EP 15 OUT Enqueue Pointer Update for Value 31 the Definition is EP 15 IN Enqueue Pointer Update for Value 32:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined Host Controller Doorbell (0) for Value 0 the Definition is Command Doorbell for Value 1:247 the Definition is Reserved for Value 248:255 the Definition is Vendor Defined This field returns 0 when read and should be treated as undefined by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.

19.6.51 USBLEGSUP—Offset 880h

The USBLEGSUP capability requires support for Byte accesses for Semaphore address, refer to section 7.1.of xhci specification. usb legacy support capability DW

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

USBLEGSUP: [BAR] + 880h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000401h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

Bits	Field
31:25	RSVD35
24	HC_OS_OWNED
23:17	RSVD34
16	HC_BIOS_OWNED
15:8	NEXT_CAPABILITY_POINTER
7:0	CAPABILITY_ID

Bit Range	Default & Access	Description
31:25	0h RO	**RSVD35:** reserved
24	0h RW	**HC_OS_OWNED:** Reg field HC_OS_OWNED SEMAPHORE
23:17	0h RO	**RSVD34:** reserved
16	0h RW	**HC_BIOS_OWNED:** Reg field HC_BIOS_OWNED SEMAPHORE
15:8	04h RO	**NEXT_CAPABILITY_POINTER:** Reg field NEXT_CAPABILITY_POINTER

Bit Range	Default & Access	Description
7:0	01h RO	**CAPABILITY_ID:** Reg field CAPABILITY_ID

19.6.52 USBLEGCTLSTS—Offset 884h

usb legacy support capability DW

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

USBLEGCTLSTS: [BAR] + 884h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SMI_ON_BAR	SMI_ON_PCI	SMI_ON_OS	RSVD39								SMI_ON_HOST	RSVD38			SMI_ON_EVENT	SMI_ON_BAR_E	SMI_ON_PCI_E	SMI_ON_OS_E	RSVD37								SMI_ON_HOST_E	RSVD36			USB_SMI_ENABLE

Bit Range	Default & Access	Description
31	0h RO	**SMI_ON_BAR:** Reg field SMI_ON_BAR
30	0h RO	**SMI_ON_PCI:** Reg field SMI_ON_PCI COMMAND
29	0h RO	**SMI_ON_OS:** Reg field SMI_ON_OS OWNERSHIP CHANGE
28:21	0h RO	**RSVD39:** reserved
20	0h RO	**SMI_ON_HOST:** Reg field SMI_ON_HOST SYSTEM ERROR
19:17	0h RO	**RSVD38:** reserved
16	0h RO	**SMI_ON_EVENT:** Reg field SMI_ON_EVENT INTERRUPT
15	0h RW	**SMI_ON_BAR_E:** Reg field SMI_ON_BAR ENABLE
14	0h RW	**SMI_ON_PCI_E:** Reg field SMI_ON_PCI COMMAND ENABLE
13	0h RW	**SMI_ON_OS_E:** Reg field SMI_ON_OS OWNERSHIP ENABLE
12:5	0h RO	**RSVD37:** Reserved

Bit Range	Default & Access	Description
4	0h RW	**SMI_ON_HOST_E:** Reg field SMI_ON_HOST SYSTEM ERROR ENABLE
3:1	0h RO	**RSVD36:** Reserved
0	0h RW	**USB_SMI_ENABLE:** Reg field USB_SMI_ENABLE

19.6.53 SUPTPRT2_DW0—Offset 890h

usb legacy support capability DW

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUPTPRT2_DW0: [BAR] + 890h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 02000002h

31 … 24	23 … 16	15 … 8	7 … 0
0 0 0 0 0 0 1 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 0
MAJOR_REVISION	MINOR_REVISION	NEXT_CAPABILITY_POINTER	CAPABILITY_ID

Bit Range	Default & Access	Description
31:24	02h RW	**MAJOR_REVISION:** Reg field MAJOR_REVISION
23:16	0h RW	**MINOR_REVISION:** Reg field MINOR_REVISION
15:8	0h RW	**NEXT_CAPABILITY_POINTER:** Reg field NEXT_CAPABILITY_POINTER
7:0	02h RW	**CAPABILITY_ID:** reg field CAPABILITY_ID

19.6.54 SUPTPRT2_DW1—Offset 894h

Register SUPTPRT2_DW1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SUPTPRT2_DW1: [BAR] + 894h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 02000110h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

NAME_STRING

Bit Range	Default & Access	Description
31:0	02000110h RW	**NAME_STRING:** Reg field NAME_STRING

19.6.55 SUPTPRT2_DW2—Offset 898h

flag Value After Reset: 0x0 Register SUPTPRT2_DW2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SUPTPRT2_DW2: [BAR] + 898h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00080001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

RSVD40 | HLC | IHI | HSO | L1C | COMPATIBLE_PORT_COUNT | COMPATIBLE_PORT_OFFSET

Bit Range	Default & Access	Description
31:20	0000h RO	**RSVD40:** reserved
19	1h RO	**HLC:** Hardware LMP capability (HLC) RO.when XHCI 100 - Default = 1'b1. when XHCI 096 - Default = 1'b0 . If this bit is set to 1, the ports described by this xHCI supported Protocol Capability support hardware controlled USB2 Link Power Management. Refer to section 4.23.5.1.1.1.

Bit Range	Default & Access	Description
18	0h RO	**IHI:** Integrated Hub Implementation (IHI) RO. Default = 1'b0. If this bit is cleared to 0, the Root Hub to External xHC port mapping adheres to the default mapping described in section 4.24.2.1. if this bit is set to 1, the Root Hub to External xHc port mapping does not adhere to the default mapping described in section 4.24.2.1, and an ACPI or other mechanism is required to define the mapping
17	0h RO	**HSO:** High-speed Only (HSO) RO. Default = 1'b0. If this bit is cleared to 0 the USB2 ports described by this capability are Low-, Full-, and high speed capable. If this bit is set to 1, the USB2 ports described by this capability are High-speed only, e.g. the ports dont support Low- or Full-Speed operation. High-speed only implementations may introduce a Teir mismatch, refer to section 4.24.2 for more information.
16	0h RW	**L1C:** Reserved
15:8	0h RW	**COMPATIBLE_PORT_COUNT:** Reg field COMPATIBLE_PORT_COUNT
7:0	01h RW	**COMPATIBLE_PORT_OFFSET:** Reg field COMPATIBLE_PORT_OFFSET

19.6.56 SUPTPRT3_DW0—Offset 8A0h

flag Value After Reset: 0x0 Register SUPTPRT3_DW0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SUPTPRT3_DW0: [BAR] + 8A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 03000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
MAJOR_REVISION								MINOR_REVISION								NEXT_CAPABILITY_POINTER								CAPABILITY_ID							

Bit Range	Default & Access	Description
31:24	0x03 RW	**MAJOR_REVISION:** 0x0 Reg field MAJOR_REVISION
23:16	00h RW	**MINOR_REVISION:** flag Value After Reset: 0x0 Reg field MINOR_REVISION
15:8	0h RW	**NEXT_CAPABILITY_POINTER:** Reg field NEXT_CAPABILITY_POINTER
7:0	02h RW	**CAPABILITY_ID:** Reg field CAPABILITY_ID

19.6.57 SUPTPRT3_DW1—Offset 8A4h

Register SUPTPRT3_DW1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SUPTPRT3_DW1: [BAR] + 8A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAME_STRING																															

Bit Range	Default & Access	Description
31:0	0h RW	**NAME_STRING:** field NAME_STRING

19.6.58 SUPTPRT3_DW2—Offset 8A8h

0x0 Register SUPTPRT3_DW2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SUPTPRT3_DW2: [BAR] + 8A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD41															L1C	COMPATIBLE_PORT_COUNT								COMPATIBLE_PORT_OFFSET							

Bit Range	Default & Access	Description
31:17	0h RO	**RSVD41:** reserved

Bit Range	Default & Access	Description
16	0h RW	**L1C:** reserved
15:8	0h RW	**COMPATIBLE_PORT_COUNT:** Reg field COMPATIBLE_PORT_COUNT
7:0	0h RW	**COMPATIBLE_PORT_OFFSET:** 0x0 Reg field COMPATIBLE_PORT_OFFSET

19.6.59 GSBUSCFG0—Offset C100h

Global SoC Bus Configuration Register 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GSBUSCFG0: [BAR] + C100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000006h

Bits	31:12	11	10:8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0	0	0	0	0	0	1	1	0
Field	GSBUSCFG0_RSVD1	DATBIGEND	GSBUSCFG0_RSVD0	INCR256BRSTENA	INCR128BRSTENA	INCR64BRSTENA	INCR32BRSTENA	INCR16BRSTENA	INCR8BRST	INCR4BRSTENA	INCRBRSTENA

Bit Range	Default & Access	Description
31:12	0h RO	**GSBUSCFG0_RSVD1:** Reserved
11	0h RW	**DATBIGEND:** Data Access is Big-Endian (DatBigEnd). This bit controls the endian mode for data accesses. 0: Little-endian (default) 1: Big-endian In big-endian mode, DMA access (both read and write) for packet data will utilize a Byte Invariant Big-Endian mode (see Section Little-Endian and Big-Endian in the DWC SuperSpeed USB 3.0 Controller User Guide). Note: Since AXI requires byteinvariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate.See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI master (DWC_USB3_MBUS_TYPE=1), this bit must be set to zero.
10:8	0h RO	**GSBUSCFG0_RSVD0:** Reserved
7	0h RW	**INCR256BRSTENA:** INCR256 Burst Type Enable
6	0h RW	**INCR128BRSTENA:** INCR128 Burst Type Enable
5	0h RW	**INCR64BRSTENA:** INCR64 Burst Type Enable

Bit Range	Default & Access	Description
4	0h RW	**INCR32BRSTENA:** INCR32 Burst Type Enable
3	0h RW	**INCR16BRSTENA:** INCR16 Burst Type Enable
2	1h RW	**INCR8BRST:** INCR8 Burst Type Enable
1	1h RW	**INCR4BRSTENA:** INCR4 Burst Type Enable
0	0h RW	**INCRBRSTENA:** Undefined Length INCR Burst Type Enable (INCRBrstEna). Input to BUS-GM When enabled, this has higher priority than other burst types. For the AHB configuration. if this bit is set to 1, AHB master tries to do only one INCR burst for each transfer unless it has to break it at a 1Kbyte boundary. If this bit is set to 0, the AHB master may still use INCR burst type at the beginning and end bursts of transfers to align the address. The middle bursts are INCR4/8/16, depending when the type is enabled.

19.6.60 GSBUSCFG1—Offset C104h

Global SoC Bus Configuration Register 1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GSBUSCFG1: [BAR] + C104h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000F00h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Field
31:13	RSVD0
12	EN1KPAGE
11:8	BREQLIMIT
7:4	DATADRSPC
3:0	DESADRSPC

Bit Range	Default & Access	Description
31:13	0h RO	**RSVD0:** reserved
12	0h RW	**EN1KPAGE:** 1k Page Boundary Enable: By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	fh RW	**BREQLIMIT:** AXI Pipelined Transfers Burst Request Limit (PipeTransLimit) The field controls the number of outstanding pipelined transfers requests the AXI master will push to the AXI slave. Once the AXI master reaches this limit, it will not make more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete.This field is encoded as follows: h0: 1 request h1: 2 requests h2: 3 requests h3: 4 requests hF: 16 requests
7:4	0h RW	**DATADRSPC:** Reserved
3:0	0h RW	**DESADRSPC:** Reserved

19.6.61 GTXTHRCFG—Offset C108h

Global Tx Threshold Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXTHRCFG: [BAR] + C108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 230A0000h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTXTHRCFG_RSVD4 | USBXMITPKTCNTEN | GTXTHRCFG_RSVD3 | USBXMITPKTCNT | USBMAXTXBURSTSIZE | GTXTHRCFG_RSVD2 | GTXTHRCFG_RSVD1

Bit Range	Default & Access	Description
31:30	0h RW	**GTXTHRCFG_RSVD4:** Reserved
29	1h RW	**USBXMITPKTCNTEN:** USB Transmit Packet Count Enable (USBTxPktCntSel). This field enables/disables the USB transmission multi-packet thresholding: 0: USB transmission multi-packet thresholding is disabled, the core can only start transmission on the USB after the entire packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The core can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO This mode is only valid in the host mode. It is only used for SuperSpeed.
28	0h RO	**GTXTHRCFG_RSVD3:** Reserved
27:24	3h RO	**USBXMITPKTCNT:** USB Transmit Packet Count (USBTxPktCnt) This field specifies the number of packets that must be in the TXFIFO before the core can start transmission for the corresponding USB transaction (burst). This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15.
23:16	0Ah RW	**USBMAXTXBURSTSIZE:** USB Maximum TX Burst Size: When USBTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the core should do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. User can program a smaller value to this field to limit the TX burst size that the core can do. It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints in the host mode. Valid values are from 1 to 16.
15:11	0h RO	**GTXTHRCFG_RSVD2:** Reserved
10:0	0h RW	**GTXTHRCFG_RSVD1:** Reserved

19.6.62 GRXTHRCFG—Offset C10Ch

Global Rx Threshold Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GRXTHRCFG: [BAR] + C10Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 22800000h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GRXTHRCFG_RSVD3	USBRXPKTCNTSEL	GRXTHRCFG_RSVD2	USBRXPKTCNT	USBMAXRXBURSTSIZE	GRXTHRCFG_RSVD1

Bit Range	Default & Access	Description
31:30	0h RO	**GRXTHRCFG_RSVD3:** Reserved
29	1h RW	**USBRXPKTCNTSEL:** USB ReceivePacket Count Enable: This field enables/disables the USB reception multi-packet thresholding: n 0: The core can only start reception on the USB when the RX FIFO has space for at least one packet. n 1: The core can only start reception on the USB when the RX FIFO has space for at least USBRxPktCnt amount of packets. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	0h RO	**GRXTHRCFG_RSVD2:** Reserved
27:24	2h RW	**USBRXPKTCNT:** USB Receive Packet Count: This field specifies space (in number of packets) that must be available in the RX FIFO before the core can start the corresponding USB RX transaction (burst). This field is only valid when the USB Receive Packet Count Enable field is set to one. The valid values are from 1 to 15.
23:19	10h RW	**USBMAXRXBURSTSIZE:** USB Maximum Receive Burst Size: This field is only valid when USBRxPktCntSel is one. This field specifies the Maximum Bulk IN burst the core should do. When the system bus is slower than the USB, RX FIFO can overrun during a long burst. User can program a smaller value to this field to limit the RX burst size that the core can do. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints in the host mode. Valid values are from 1 to 16.
18:0	0h RO	**GRXTHRCFG_RSVD1:** Reserved

19.6.63 GCTL—Offset C110h

Global Common Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GCTL: [BAR] + C110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 45803000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:19	PWRDNSCALE
18	MASTERFILTBYPASS
17	BYPSSETADDRINDEVMODE
16	U2RSTECN
15:14	FRMSCLDWN
13:12	PRTCAPDIR
11	CORESOFTRST
10	SOFITPSYNC
9	GCTL_RSVD2
8	DEBUGATTACH
7:6	RAMCLKSEL
5:4	SCALEDOWN
3	DISSCRAMBLE
2	GCTL_RSVD1
1	GBLHIBERNATIONEN
0	DSBLCLKGTNG

Bit Range	Default & Access	Description
31:19	08b0h RW	**PWRDNSCALE:** Reg field PWRDNSCALE
18	0h RW	**MASTERFILTBYPASS:** Master Filter Bypass: When this bit is set to 1'b1, irrespective of the parameter DWC_USB3_EN_BUS_FILTERS chosen, all the filters in the DWC_usb3_filter module will be bypassed. The double synchronizers to mac_clk preceding the filters will also be bypassed. For enabling the filters, this bit should be 1'b0.
17	0h RW	**BYPSSETADDRINDEVMODE:**
16	0h RW	**U2RSTECN:** If the super speed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode.
15:14	0h RW	**FRMSCLDWN:** This field scales down device view of a SOF/USOF/ITP duration. For SS/HS mode: Value of 2'h3 implements interval to be 15. 625 us Value of 2'h2 implements interval to be 31.25 us Value of 2'h1 implements interval to be 62.5 us Value of 2'h0 implements interval to be125us For FS mode, the scale-down value is multiplied by 8.
13:12	3h RW	**PRTCAPDIR:** Reg field PRTCAPDIR
11	0h RW	**CORESOFTRST:** Core Soft Reset (CoreSoftReset) 1b0 - No soft reset 1b1 - Soft reset to core When you reset PHYs (using GUBS3PHYCFG or GUSB3PIPECTL registers), you must keep the core in reset state until PHY clocks are stable. This controls the bus, ram, and mac domain resets.
10	0h RW	**SOFITPSYNC:** Sync ITP to reference clock
9	0h RO	**GCTL_RSVD2:** Disable U1/U2 timer Scaledown (U1U2TimerScale) If set to '1' along with GCTL[5:4] (ScaleDown) = 2'bX1 disables the scale down of U1/U2 inactive timer values. This is for simulation mode only.
8	0h RW	**DEBUGATTACH:** Debug Attach
7:6	0h RW	**RAMCLKSEL:** Reg field RAMCLKSEL
5:4	0h RW	**SCALEDOWN:** reg field SCALEDOWN
3	0h RW	**DISSCRAMBLE:** Disable Scrambling
2	0h RO	**GCTL_RSVD1:** Reserved

Bit Range	Default & Access	Description
1	0h RW	**GBLHIBERNATIONEN:** This bit enables hibernation at the global level. If hibernation is not enabled via this bit, the PMU immediately accepts the D0-)D3 and D3-)D0 power state change requests, but does not save or restore any core state. In addition, the PMUs will never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	0h RW	**DSBLCLKGTNG:** Disable Clock Gating

19.6.64 GSTS—Offset C118h

Global Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GSTS: [BAR] + C118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 3E800002h

Bits	Default bits	Field
31:20	0011 1110 1000	CBELT
19:11	0000 0000 0	RSVD7
10	0	OTG_IP
9	0	BC_IP
8	0	ADP_IP
7	0	Host_IP
6	0	Device_IP
5	0	CSRTimeout
4	0	BUSERRADDRVLD
3:2	00	R6
1:0	10	CURMOD

Bit Range	Default & Access	Description
31:20	3e8h RO	**CBELT:** Current BELT Value: In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
19:11	0h RO	**RSVD7:** reserved
10	0h RO	**OTG_IP:** OTG Interrupt Pending: This field indicates that there is a pending interrupt pertaining to OTG in OEVT register.
9	0h RO	**BC_IP:** Battery Charger Interrupt Pending: This field indicates that there is a pending interrupt pertaining to BC in BCEVT register.
8	0h RO	**ADP_IP:** ADP Interrupt Pending: This field indicates that there is a pending interrupt pertaining to ADP in ADPEVT register.
7	0h RO	**Host_IP:** Host Interrupt Pending: This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.
6	0h RO	**Device_IP:** Device Interrupt Pending: This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.
5	0h RO	**CSRTimeout:** CSR Timeout: When this bit is 1'b1, it indicates that software performed a write or read to a core register that could not be completed within DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles (default: 65535).
4	0h RO	**BUSERRADDRVLD:** Bus Error Address Valid

Bit Range	Default & Access	Description
3:2	0h RO	**R6:** Reg field R6
1:0	2h RO	**CURMOD:** Reg field CURMOD

19.6.65 GSNPSID—Offset C120h

flag Value After Reset: 0x5533210a Global Synopsys ID Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GSNPSID: [BAR] + C120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 5533192Ah

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	0	0	1	0	1	0	1	0

SYNOPSYSID

Bit Range	Default & Access	Description
31:0	5533192ah RO	**SYNOPSYSID:** flag Value After Reset: 0x5533210a Reg field SYNOPSYSID

19.6.66 GGPIO—Offset C124h

Global General Purpose Input/Output Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GGPIO: [BAR] + C124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPO (bits 31:16), GPI (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**GPO:** General Purpose Output: This field's value is driven out on the gp_o[15:0] core output port.

Bit Range	Default & Access	Description
15:0	0h RO	**GPI:** General Purpose Input: This field's read value reflects the gp_i[15:0] core input value.

19.6.67 GUID—Offset C128h

flag Value After Reset: 0x8086a0 Global User ID Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GUID: [BAR] + C128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 12345678h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0

USERID (bits 31:0)

Bit Range	Default & Access	Description
31:0	12345678h RW	**USERID:** flag Value After Reset: 0x8086a0 Reg field USERID

19.6.68 GUCTL—Offset C12Ch

flag Value After Reset: 0x200ce00 Global User Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GUCTL: [BAR] + C12Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 7FC0C600h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Fields: MAC3FLADJ (31:22), NOEXTRDL (21), PSQEXTRRESSP (20:18), SPRSCTRLTRANSEN (17), RESBWHSEPS (16), CMDEVADDR (15), USBHSTINAUTORETRYEN (14), GUCTL_RSVD1 (13:11), DTCT (10:9), DTFT (8:0)

Bit Range	Default & Access	Description
31:22	1ffh RW	**MAC3FLADJ:**
21	0h RW	**NOEXTRDL:**
20:18	0h RW	**PSQEXTRRESSP:**
17	0h RW	**SPRSCTRLTRANSEN:** Sparse Control Transaction Enable: Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/ frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames.
16	0h RW	**RESBWHSEPS:** Reserving 85% Bandwidth for HS Periodic EPs
15	1h RW	**CMDEVADDR:** Compliance Mode for Device Address: When this bit is 1'b1, Slot ID may have different value than Device Address if max_slot_enabled (128. n 1'b1: Increment Device Address on each Address Device command. n 1'b0: Device Address is equal to Slot ID. The xHCI compliance requires this bit to be set to 1'. The 0' mode is for debug purpose only. This all ows you to easily identify a device connected to a port in the Lecroy or Eliisys trace during hardware debug. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
14	1h RW	**USBHSTINAUTORETRYEN:** Host IN Auto Retry: When set, this field enables the Auto Retry feature. For IN transfers (non-isochronous) that encounter data packets with CRC errors or internal overrun scenarios, the auto retry feature causes the Host core to reply to the device with a non-terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP != 0). If the Auto Retry feature is disabled (default), the core will respond with a terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP = 0). n 1'b0: Auto Retry Disabled n 1'b1: Auto Retry Enabled In device mode this bit should be 0
13:11	0h RO	**GUCTL_RSVD1:**
10:9	3h RW	**DTCT:** Device Timeout Coarse Tuning: This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The core first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: n 2'b00: 0 usec -) use DTFT value instead n 2'b01: 500 usec n 2'b10: 1.5 msec n 2'b11: 6.5 msec
8:0	0h RW	**DTFT:** Device Timeout Fine Tuning: This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. For the 125 MHz clk (8 ns period), this is calculated as follows: (DTFT value) * 256 * (8 ns) Quick Reference: n if DTFT = 0x2, 2*256*8 = 4usec timeout n if DTFT = 0x5, 5*256*8 = 10usec timeout n if DTFT = 0xA, 10*256*8 = 20usec timeout n if DTFT = 0x10, 16*256*8 = 32usec timeout n if DTFT = 0x19, 25*256*8 = 51usec timeout n if DTFT = 0x31, 49*256*8 = 100usec timeout n if DTFT = 0x62, 98*256*8 = 200usec timeout

19.6.69 GBUSERRADDRLO—Offset C130h

Register GBUSERRADDRLO

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GBUSERRADDRLO: [BAR] + C130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUSERRADDR

Bit Range	Default & Access	Description
31:0	0h RO	**BUSERRADDR:** Reg field BUSERRADDR

19.6.70 GBUSERRADDRHI—Offset C134h

Register GBUSERRADDRHI

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GBUSERRADDRHI: [BAR] + C134h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUSERRADDR

Bit Range	Default & Access	Description
31:0	0h RO	**BUSERRADDR:** Reg field BUSERRADDR

19.6.71 GPRTBIMAPLO—Offset C138h

0x0 Register R

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GPRTBIMAPLO: [BAR] + C138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
BINUM8	BINUM7	BINUM6	BINUM5	BINUM4	BINUM3	BINUM2	BINUM1

Bit Range	Default & Access	Description
31:28	0h RO	**BINUM8:** Reg field BINUM8
27:24	0h RO	**BINUM7:** Reg field BINUM7
23:20	0h RO	**BINUM6:** Reg field BINUM6
19:16	0h RO	**BINUM5:** Reg field BINUM5
15:12	0h RO	**BINUM4:** Reg field BINUM4
11:8	0h RO	**BINUM3:** Reg field BINUM3
7:4	0h RO	**BINUM2:** Reg field BINUM2
3:0	0h RW	**BINUM1:** flag Value After Reset: 0x1 Reg field BINUM1

19.6.72 GPRTBIMAPHI—Offset C13Ch

Register R

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GPRTBIMAPHI: [BAR] + C13Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Rsvd16	BINUM15	BINUM14	BINUM13	BINUM12	BINUM11	BINUM10	BINUM9

Bit Range	Default & Access	Description
31:28	0h RO	**Rsvd16:** reserved
27:24	0h RO	**BINUM15:** Reg field BINUM15

Bit Range	Default & Access	Description
23:20	0h RO	**BINUM14:** Reg field BINUM14
19:16	0h RO	**BINUM13:** Reg field BINUM13
15:12	0h RO	**BINUM12:** Reg field BINUM12
11:8	0h RO	**BINUM11:** Reg field BINUM11
7:4	0h RO	**BINUM10:** Reg field BINUM10
3:0	0h RO	**BINUM9:** Reg field BINUM9

19.6.73 GHWPARAMS0—Offset C140h

Global Hardware Parameters Register 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHWPARAMS0: [BAR] + C140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 2020400Ah

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
DWC_USB3_AWIDTH								DWC_USB3_SDWIDTH								DWC_USB3_MDWIDTH								DWC_USB3_SBUS_TYPE		DWC_USB3_MBUS_TYPE			DWC_USB3_MODE		

Bit Range	Default & Access	Description
31:24	20h RO	**DWC_USB3_AWIDTH:**
23:16	20h RO	**DWC_USB3_SDWIDTH:**
15:8	40h RO	**DWC_USB3_MDWIDTH:**
7:6	0h RO	**DWC_USB3_SBUS_TYPE:**
5:3	1h RO	**DWC_USB3_MBUS_TYPE:**

Bit Range	Default & Access	Description
2:0	2h RO	**DWC_USB3_MODE:**

19.6.74 GHWPARAMS1—Offset C144h

Global Hardware Parameters Register 1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHWPARAMS1: [BAR] + C144h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0260C93Bh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	1	1	1	0	1	1

GHWPARAMS1_RSVD2 | DWC_USB3_RM_OPT_FEATURES | GHWPARAMS1_RSVD1 | DWC_USB3_RAM_BUS_CLKS_SYNC | DWC_USB3_MAC_RAM_CLKS_SYNC | DWC_USB3_MAC_PHY_CLKS_SYNC | DWC_USB3_EN_PWROPT | DWC_USB3_SPRAM_TYP | DWC_USB3_NUM_RAMS | DWC_USB3_DEVICE_NUM_INT | DWC_USB3_ASPACEWIDTH | DWC_USB3_REQINFOWIDTH | DWC_USB3_DATAINFOWIDTH | DWC_USB3_BURSTWIDTH | DWC_USB3_IDWIDTH

Bit Range	Default & Access	Description
31	0h RO	**GHWPARAMS1_RSVD2:**
30	0h RO	**DWC_USB3_RM_OPT_FEATURES:**
29	0h RO	**GHWPARAMS1_RSVD1:**
28	0h RO	**DWC_USB3_RAM_BUS_CLKS_SYNC:** Reserved.
27	0h RO	**DWC_USB3_MAC_RAM_CLKS_SYNC:** Reserved.
26	0h RO	**DWC_USB3_MAC_PHY_CLKS_SYNC:**
25:24	2h RO	**DWC_USB3_EN_PWROPT:**
23	0h RO	**DWC_USB3_SPRAM_TYP:**

Bit Range	Default & Access	Description
22:21	3h RO	**DWC_USB3_NUM_RAMS:**
20:15	01h RO	**DWC_USB3_DEVICE_NUM_INT:**
14:12	4h RO	**DWC_USB3_ASPACEWIDTH:** Reserved.
11:9	4h RO	**DWC_USB3_REQINFOWIDTH:**
8:6	4h RO	**DWC_USB3_DATAINFOWIDTH:**
5:3	7h RO	**DWC_USB3_BURSTWIDTH:**
2:0	3h RO	**DWC_USB3_IDWIDTH:**

19.6.75 GHWPARAMS2—Offset C148h

Global Hardware Parameters Register 2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHWPARAMS2: [BAR] + C148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 008086A0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0

DWC_USB3_USERID

Bit Range	Default & Access	Description
31:0	008086a0h RO	**DWC_USB3_USERID:**

19.6.76 GHWPARAMS3—Offset C14Ch

Global Hardware Parameters Register 3

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHWPARAMS3: [BAR] + C14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 10420089h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1

Bits	Field
31	GHWPARAMS3_RSVD2
30:23	DWC_USB3_CACHE_TOTAL_XFER_RESOURCES
22:18	DWC_USB3_NUM_IN_EPS
17:12	DWC_USB3_NUM_EPS
11	DWC_USB3_ULPI_CARKIT
10	DWC_USB3_VENDOR_CTL_INTERFACE
9:8	GHWPARAMS3_RSVD1
7:6	DWC_USB3_HSPHY_DWIDTH
5:4	DWC_USB3_FSPHY_INTERFACE
3:2	DWC_USB3_HSPHY_INTERFACE
1:0	DWC_USB3_SSPHY_INTERFACE

Bit Range	Default & Access	Description
31	0h RO	**GHWPARAMS3_RSVD2:**
30:23	20h RO	**DWC_USB3_CACHE_TOTAL_XFER_RESOURCES:**
22:18	10h RO	**DWC_USB3_NUM_IN_EPS:**
17:12	20h RO	**DWC_USB3_NUM_EPS:**
11	0h RO	**DWC_USB3_ULPI_CARKIT:**
10	0h RO	**DWC_USB3_VENDOR_CTL_INTERFACE:**
9:8	0h RO	**GHWPARAMS3_RSVD1:**
7:6	2h RO	**DWC_USB3_HSPHY_DWIDTH:**
5:4	0h RO	**DWC_USB3_FSPHY_INTERFACE:**
3:2	2h RO	**DWC_USB3_HSPHY_INTERFACE:**
1:0	1h RO	**DWC_USB3_SSPHY_INTERFACE:**

19.6.77 GHWPARAMS4—Offset C150h

falg Value After Reset: 0x48a22004 Global Hardware Parameters Register 4

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHWPARAMS4: [BAR] + C150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 48822004h

31			28				24				20				16				12				8				4				0
0	1	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0

DWC_USB3_BMU_LSP_DEPTH	DWC_USB3_BMU_PTL_DEPTH	DWC_USB3_EN_ISOC_SUPT	GHWPARAMS4_RSVD2	DWC_USB3_NUM_SS_USB_INSTANCES	DWC_USB3_HIBER_SCRATCHBUFS	GHWPARAMS4_RSVD1	DWC_USB3_CACHE_TRBS_PER_TRANSFER

Bit Range	Default & Access	Description
31:28	4h RO	**DWC_USB3_BMU_LSP_DEPTH:**
27:24	8h RO	**DWC_USB3_BMU_PTL_DEPTH:**
23	1h RO	**DWC_USB3_EN_ISOC_SUPT:**
22:21	0h RO	**GHWPARAMS4_RSVD2:**
20:17	1h RO	**DWC_USB3_NUM_SS_USB_INSTANCES:**
16:13	1h RO	**DWC_USB3_HIBER_SCRATCHBUFS:**
12:6	0h RO	**GHWPARAMS4_RSVD1:**
5:0	04h RO	**DWC_USB3_CACHE_TRBS_PER_TRANSFER:**

19.6.78 GHWPARAMS5—Offset C154h

Global Hardware Parameters Register 5

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHWPARAMS5: [BAR] + C154h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 04202088h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 1 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	1 0 0 0	1 0 0 0

Bits	Field
31:28	GHWPARAMS5_RSVD
27:22	DWC_USB3_DFQ_FIFO_DEPTH
21:16	DWC_USB3_DWQ_FIFO_DEPTH
15:10	DWC_USB3_TXQ_FIFO_DEPTH
9:4	DWC_USB3_RXQ_FIFO_DEPTH
3:0	DWC_USB3_BMU_BUSGM_DEPTH

Bit Range	Default & Access	Description
31:28	0h RO	**GHWPARAMS5_RSVD:**
27:22	10h RO	**DWC_USB3_DFQ_FIFO_DEPTH:**
21:16	20h RO	**DWC_USB3_DWQ_FIFO_DEPTH:**
15:10	08h RO	**DWC_USB3_TXQ_FIFO_DEPTH:**
9:4	08h RO	**DWC_USB3_RXQ_FIFO_DEPTH:**
3:0	8h RO	**DWC_USB3_BMU_BUSGM_DEPTH:**

19.6.79 GHWPARAMS6—Offset C158h

Global Hardware Parameters Register 6

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHWPARAMS6: [BAR] + C158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0C00AC20h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0

Bits	Field
31:16	DWC_USB3_RAM0_DEPTH
15	DWC_USB3_EN_BUS_FILTERS
14	DWC_USB3_EN_BC
13	OTG_SS_Support
12	ADPSupport
11	HNPSupport
10	SRPSupport
9:8	ghwparams6_9_8
7	DWC_USB3_EN_FPGA
6	GHWPARAMS6_RSVD
5:0	DWC_USB3_PSQ_FIFO_DEPTH

Bit Range	Default & Access	Description
31:16	0c00h RO	**DWC_USB3_RAM0_DEPTH:**
15	1h RO	**DWC_USB3_EN_BUS_FILTERS:**
14	0h RO	**DWC_USB3_EN_BC:**
13	1h RO	**OTG_SS_Support:** Reg field CORECONSULTANT
12	0h RO	**ADPSupport:** DWC_USB3_EN_ADP:
11	1h RO	**HNPSupport:** RSP/HNP Support Enabled: The application uses this bit to determine the DWC_usb3 core's RSP/HNP support. If DWC_USB3_EN_OTG=2, n 1'b0: RSP and HNP support is not enabled. The only exception for this rule is for SSPC-OTG devices where RSP support is not enabled, but HNP support is enabled. (Refer OCFG.SSPC-OTG bit) n 1'b1: RSP and HNP support is enabled If DWC_USB3_EN_OTG=1, n 1'b0: HNP support is not enabled n 1'b1: HNP support is enabled This bit is enabled only if HNP mode was specified for HNP Mode of Operation in coreConsultant (parameter DWC_USB3_EN_OTG is not 0, and DWC_USB3_MODE is DRD). Other wise, it reads 0.
10	1h RO	**SRPSupport:** SRP Support Enabled: The application uses this bit to determine the DWC_usb3 core's SRP support. n1'b0: SRP support is not enabled n 1'b1: SRP support is enabled This bit is 1'b1 when the parameter DWC_USB3_EN_OTG is not 0.
9:8	0h RO	**ghwparams6_9_8:** Reg field CORECONSULTANT
7	0h RO	**DWC_USB3_EN_FPGA:**
6	0h RO	**GHWPARAMS6_RSVD:**
5:0	20h RO	**DWC_USB3_PSQ_FIFO_DEPTH:**

19.6.80 GHWPARAMS7—Offset C15Ch

Global Hardware Parameters Register 7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHWPARAMS7: [BAR] + C15Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 038807E6h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1	0

Fields: DWC_USB3_RAM2_DEPTH (31:16), DWC_USB3_RAM1_DEPTH (15:0)

Bit Range	Default & Access	Description
31:16	0388h RO	**DWC_USB3_RAM2_DEPTH:**
15:0	07e6h RO	**DWC_USB3_RAM1_DEPTH:**

19.6.81 GDBGFIFOSPACE—Offset C160h

flag Value After Reset: 0x820000 Global Debug Queue/FIFO Space Available Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GDBGFIFOSPACE: [BAR] + C160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00420000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: SPACE_AVAILABLE (31:16), RSVD8 (15:8), FIFO_QUEUE_SELECT (7:0)

Bit Range	Default & Access	Description
31:16	42h RO	**SPACE_AVAILABLE:** Reg field SPACE_AVAILABLE

Bit Range	Default & Access	Description
15:8	0h RO	**RSVD8:** reserved
7:0	0h RW	**FIFO_QUEUE_SELECT:** Reg field FIFO_QUEUE_SELECT

19.6.82 GDBGLTSSM—Offset C164h

Global Debug LTSSM Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GDBGLTSSM: [BAR] + C164h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 01010440h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0

RSVD14, LTDBTIMEOUT, LTDBLINKSTATE, LTDBSUBSTATE, ELASTICBUFFERMODE, TXELECLDLE, RXPOLARITY, TxDetRxLoopback, LTDBPhyCmdState, POWERDOWN, RXEQTRAIN, TXDEEMPHASIS, LTDBClkState, TXSWING, RXTERMINATION, TXONESZEROS

Bit Range	Default & Access	Description
31:27	0h RO	**RSVD14:** reserved
26	0h RO	**LTDBTIMEOUT:** LTDB Timeout
25:22	4h RO	**LTDBLINKSTATE:** flag Value After Reset: 0x0 LTDB Link State
21:18	0h RO	**LTDBSUBSTATE:** LTDB Sub-State
17	0h RO	**ELASTICBUFFERMODE:** Elastic Buffer Mode
16	1h RO	**TXELECLDLE:** Tx Elec Idle
15	0h RO	**RXPOLARITY:** Rx Polarity
14	0h RO	**TxDetRxLoopback:** Tx Detect Rx/Loopback:

Bit Range	Default & Access	Description
13:11	0h RO	**LTDBPhyCmdState:** LTSSM PHY command State: n 000: PHY_IDLE (PHY command state is in IDLE. No PHY request pending) n 001: PHY_DET (Request to start Receiver detection) n 010: PHY_DET_3 (Wait for Phy_Status (Receiver detection)) n 011: PHY_PWR_DLY (Delay Pipe3_PowerDown P0 -) P1/P2/P3 request) n 100: PHY_PWR_A (Delay for internal logic) n 101: PHY_PWR_B (Wait for Phy_Status(Power state change request))
10:9	2h RO	**POWERDOWN:** flag Value After Reset: 0x0 Reg field POWERDOWN
8	0h RO	**RXEQTRAIN:** RxEq Train
7:6	1h RO	**TXDEEMPHASIS:** flag Value After Reset: 0x0 Reg field TXDEEMPHASIS
5:3	0h RO	**LTDBClkState:** LTSSM Clock State: n 000: CLK_NORM (PHY is in non-P3 state and PCLK is running) n 001: CLK_TO_P3 (P3 entry request to PHY) n 010: CLK_WAIT1 (Wait for Phy_Status (P3 request)) n 011: CLK_P3 (PHY is in P3 and PCLK is not running) n 100: CLK_TO_P0 (P3 exit request to PHY) n 101: CLK_WAIT2 (Wait for Phy_Status (P3 exit request))
2	0h RO	**TXSWING:** Tx Swing
1	0h RO	**RXTERMINATION:** Rx Termination
0	0h RO	**TXONESZEROS:** Tx Ones/Zeros

19.6.83 GPRTBIMAP_HSLO—Offset C180h

High Speed port to bus instance mapping

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAP_HSLO: [BAR] + C180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
BINUM8	BINUM7	BINUM6	BINUM5	BINUM4	BINUM3	BINUM2	BINUM1

Bit Range	Default & Access	Description
31:28	0h RO	**BINUM8:** Reg field BINUM8
27:24	0h RO	**BINUM7:** Reg field BINUM7
23:20	0h RO	**BINUM6:** Reg field BINUM6

Bit Range	Default & Access	Description
19:16	0h RO	**BINUM5:** Reg field BINUM5
15:12	0h RO	**BINUM4:** Reg field BINUM4
11:8	0h RO	**BINUM3:** Reg field BINUM3
7:4	0h RO	**BINUM2:** Reg field BINUM2
3:0	0h RW	**BINUM1:** flag Value After Reset: 0x1 Reg field BINUM1

19.6.84 GPRTBIMAP_HSHI—Offset C184h

High Speed port to bus instance mapping

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GPRTBIMAP_HSHI: [BAR] + C184h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd16				BINUM15				BINUM14				BINUM13				BINUM12				BINUM11				BINUM10				BINUM9			

Bit Range	Default & Access	Description
31:28	0h RO	**Rsvd16:** reserved
27:24	0h RO	**BINUM15:** Reg field BINUM15
23:20	0h RO	**BINUM14:** Reg field BINUM14
19:16	0h RO	**BINUM13:** Reg field BINUM13
15:12	0h RO	**BINUM12:** Reg field BINUM12
11:8	0h RO	**BINUM11:** Reg field BINUM11
7:4	0h RO	**BINUM10:** Reg field BINUM10
3:0	0h RO	**BINUM9:** Reg field BINUM9

19.6.85 GPRTBIMAP_FSLO—Offset C188h

Register Full Speed port to bus instance mapping

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAP_FSLO: [BAR] + C188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
BINUM8	BINUM7	BINUM6	BINUM5	BINUM4	BINUM3	BINUM2	BINUM1	

Bit Range	Default & Access	Description
31:28	0h RO	**BINUM8:** Reg field BINUM8
27:24	0h RO	**BINUM7:** Reg field BINUM7
23:20	0h RO	**BINUM6:** Reg field BINUM6
19:16	0h RO	**BINUM5:** Reg field BINUM5
15:12	0h RO	**BINUM4:** Reg field BINUM4
11:8	0h RO	**BINUM3:** Reg field BINUM3
7:4	0h RO	**BINUM2:** Reg field BINUM2
3:0	0h RW	**BINUM1:** flag Value After Reset: 0x1 Reg field BINUM1

19.6.86 GPRTBIMAP_FSHI—Offset C18Ch

Register Full Speed port to bus instance mapping

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPRTBIMAP_FSHI: [BAR] + C18Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Field	Rsvd16	BINUM15	BINUM14	BINUM13	BINUM12	BINUM11	BINUM10	BINUM9

Bit Range	Default & Access	Description
31:28	0h RO	**Rsvd16:** reserved
27:24	0h RO	**BINUM15:** Reg field BINUM15
23:20	0h RO	**BINUM14:** Reg field BINUM14
19:16	0h RO	**BINUM13:** Reg field BINUM13
15:12	0h RO	**BINUM12:** Reg field BINUM12
11:8	0h RO	**BINUM11:** Reg field BINUM11
7:4	0h RO	**BINUM10:** Reg field BINUM10
3:0	0h RO	**BINUM9:** Reg field BINUM9

19.6.87 GUSB2PHYCFG—Offset C200h

Register Rs

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GUSB2PHYCFG: [BAR] + C200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000A410h

Bits	31	30:19	18	17	16	15	14	13:10	9	8	7	6	5	4	3	2:0
Default	0	0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	1	0	1 0 0 1	0	0	0	0	0	1	0	0 0 0
Field	PHYSOFTRST	GUSB2PHYCFG_RSVD3	ULPIEXTVBUSINDIACTOR	ULPIEXTVBUSDRV	ULPICLKSUSM	ULPIAUTORES	GUSB2PHYCFG_RSVD2	USBTRDTIM	GUSB2PHYCFG_RSVD1	ENBLSLPM	PHYSEL	SUSPENDUSB20	FSINTF	ULPI_UTMI_Sel	PHYIF	TOUTCALIB

Bit Range	Default & Access	Description
31	0h RW	**PHYSOFTRST:** Reg field PHYSOFTRST *Note:* A register value of 0 will asserts the reset otherwise a register value of 1 will de-assert
30:19	0h RO	**GUSB2PHYCFG_RSVD3:**
18	0h RW	**ULPIEXTVBUSINDIACTOR:** Reg field ULPIEXTVBUSINDIACTOR
17	0h RW	**ULPIEXTVBUSDRV:** Reg field ULPIEXTVBUSDRV
16	0h RW	**ULPICLKSUSM:** Reg field ULPICLKSUSM
15	1h RW	**ULPIAUTORES:** flag Value After Reset: 0x0 Reg field ULPIAUTORES
14	0h RO	**GUSB2PHYCFG_RSVD2:**
13:10	9h RW	**USBTRDTIM:** Reg field USBTRDTIM
9	0h RO	**GUSB2PHYCFG_RSVD1:**
8	0h RW	**ENBLSLPM:** Reg field ENBLSLPM
7	0h WO	**PHYSEL:** Reg field PHYSEL
6	0h RW	**SUSPENDUSB20:** SUSPENDUSB20
5	0h RO	**FSINTF:** Reg field FSINTF
4	1h RO	**ULPI_UTMI_Sel:** flag Value After Reset: 0x0 ULPI or UTMI+ Select: The application uses this bit to select a UTMI+ or ULPI Interface. n 1'b0: UTMI+ Interface n 1'b1: ULPI Interface This bit is writable only if UTMI+ and ULPI is specified for High-Speed PHY Interface(s) in coreConsultant configuration (DWC_USB3_HSPHY_INTERFACE = 3). Otherwise, this bit is Read Only and the value depends on the interface selected through DWC_USB3_HSPHY_INTERFACE.
3	0h RW	**PHYIF:** Reg field PHYIF
2:0	0h RW	**TOUTCALIB:**

19.6.88 GUSB2I2CCTL—Offset C240h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GUSB2I2CCTL: [BAR] + C240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26:25	24	23	22:16	15:8	7:0
0	0	0	0	0	0 0	0	0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
RSVD	BSYDNE	ACK	RW	I2CDATSE0	I2CDEVADR	I2CSUSPCTL	I2CEN	ADDR	REGADDR	RWDATA

Bit Range	Default & Access	Description
31	0h RW	**RSVD:**
30	0h RW	**BSYDNE:** Reg field BSYDNE
29	0h RO	**ACK:**
28	0h RW	**RW:**
27	0h RW	**I2CDATSE0:** Reg field I2CDATSE0
26:25	0h RW	**I2CDEVADR:** Reg field I2CDEVADR
24	0h RW	**I2CSUSPCTL:** Reg field I2CSUSPCTL
23	0h RW	**I2CEN:** Reg field I2CEN
22:16	0h RW	**ADDR:** Reg field ADDR
15:8	0h RW	**REGADDR:** Reg field REGADDR
7:0	0h RW	**RWDATA:** Reg field RWDATA

19.6.89 GUSB2PHYACC—Offset C280h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GUSB2PHYACC: [BAR] + C280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD42					DISUIPIDRVR	NEWREGREQ	VSTSDONE	VSTSBSY	REGWR	REGADDR						VCTRL_EXTREGADDR								REGDATA							

Bit Range	Default & Access	Description
31:27	0h RO	**RSVD42:** reserved
26	0h RO	**DISUIPIDRVR:** Reg field DISUIPIDRVR
25	0h RO	**NEWREGREQ:** Reg field NEWREGREQ
24	0h RO	**VSTSDONE:** Reg field VSTSDONE
23	0h RO	**VSTSBSY:** Reg field VSTSBSY
22	0h RO	**REGWR:** Reg field REGWR
21:16	0h RO	**REGADDR:** Reg field REGADDR
15:8	0h RO	**VCTRL_EXTREGADDR:** TDB
7:0	0h RO	**REGDATA:** Reg field REGDATA

19.6.90 GUSB3PIPECTL—Offset C2C0h

flag Value After Reset: 0x2020002

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GUSB3PIPECTL: [BAR] + C2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 02044002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0

PHYSOFTRST, GUSB3PIPECTL_RSVD2, UX_EXIT_IN_PX, PING_ENHANCEMENT_EN, U1U2EXITFAIL_TO_RECOV, RequestP1P2P3, StartRxdetU3RxDet, DisRxDetU3RxDet, DELAYP1P2P3, DELAYP0TOP1P2P3TRANS, SUSPENDENABLE, DATWIDTH, ABORTRXDETU2EXIT, SKIPRXDET, LFPSP0ALGN, P3P2TRANOK, P3EXSIGP2, LFPSFILTER, GUSB3PIPECTL_RSVD1, TX_SWING, TX_MARGIN, TX_DE_EPHASIS, ELASTIC_BUFFER_MODE

Bit Range	Default & Access	Description
31	0h RW	**PHYSOFTRST:** Reg field PHYSOFTRST
30:28	0h RO	**GUSB3PIPECTL_RSVD2:**
27	0h RW	**UX_EXIT_IN_PX:** Ux Exit in Px: n 0: The core does U1/U2/U3 exit in PHY power state P0 (default behavior) n 1: The core does U1/U2/U3 exitin PHY power state P1/P2/P3 respectively This bit is added for SS PHY workaround where SS PHY injects a glitch on pipe3_RxElecIdle while receiving Ux exit LFPS, and pipe3_PowerDown change is in progress. Note: This bit is used by third-party SS PHY. It should be set to '0' for Synopsys PHY.
26	0h RW	**PING_ENHANCEMENT_EN:** Ping Enhancement Enable: When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for Downstream port only. Note: This bit is used by third-party SS PHY. It should be set to '0' for Synopsys PHY.
25	1h RW	**U1U2EXITFAIL_TO_RECOV:** Reg field u1u2exitfail_to_recov
24	0h RW	**REQUESTp1p2p3 (RequestP1P2P3):**
23	0h RW	**STARTRXDETU3RXDET (StartRxdetU3RxDet):** Reg field StartRxDetU3RxDet
22	0h RW	**DISRXDETU3RXDET (DisRxDetU3RxDet):** Disable Receiver Detection in U3/Rx.Det: When set, the core does not do receiver detection in U3 or Rx.Detect state. DWC_USB3_GUSB3PIPECTL_INIT[23] should be used to start receiver detection manually. This bit is valid for Downstream ports only. Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality. Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. n 1'b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0 n 1'b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIlde and pipe3_RxValid. Note: This bit should be set to '1' for Synopsys PHY. It is also used by third-party SS PHY.
21:19	0h RW	**DELAYP1P2P3:** Reg field DelayP1P2P3
18	1h RW	**DELAYP0TOP1P2P3TRANS:**
17	0h RW	**SUSPENDENABLE:** Reg field SUSPENDENABLE
16:15	0h RO	**DATWIDTH:** Reg field DATWIDTH

Bit Range	Default & Access	Description
14	1h RW	**ABORTRXDETU2EXIT:**
13	0h RW	**SKIPRXDET:** Skip Rx Detect: When set, the core skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.
12	0h RW	**LFPSP0ALGN:** LFPS P0 Align: When set, n The core deasserts LFPS transmission on the clock edge that it requests Phy power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. n The core requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state. Currently, this bit is only used in USB 3.0 HUB with Synopsys PHY. For other USB 3.0 Host, Device, and DRD cores, this is not required.
11	0h RW	**P3P2TRANOK:** Reg field P3P2TranOK
10	0h RW	**P3EXSIGP2:** Reg field P3ExSigP2
9	0h RW	**LFPSFILTER:** Reg field LFPSFILTER
8:7	0h RO	**GUSB3PIPECTL_RSVD1:**
6	0h RW	**TX_SWING:** Reg field TX_SWING
5:3	0h RW	**TX_MARGIN:** Reg field TX_MARGIN
2:1	1h RW	**TX_DE_EMPHASIS:**
0	0h RW	**ELASTIC_BUFFER_MODE:** Reg field ELASTIC_BUFFER_MODE

19.6.91 GTXFIFOSIZ0—Offset C300h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ0: [BAR] + C300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000042h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

TXFSTADDR_0 (bits 31:16) | TXFDEP_0 (bits 15:0)

Bit Range	Default & Access	Description
31:16	0h RW	**TXFSTADDR_0:** Reserved.

Bit Range	Default & Access	Description
15:0	0042h RW	**TXFDEP_0:**

19.6.92 GTXFIFOSIZ1—Offset C304h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ1: [BAR] + C304h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00420184h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0

TXFSTADDR_1 (bits 31:16) | TXFDEP_1 (bits 15:0)

Bit Range	Default & Access	Description
31:16	0042h RW	**TXFSTADDR_1:**
15:0	0184h RW	**TXFDEP_1:**

19.6.93 GTXFIFOSIZ2—Offset C308h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ2: [BAR] + C308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 01C60184h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0

TXFSTADDR_2 (bits 31:16) | TXFDEP_2 (bits 15:0)

Bit Range	Default & Access	Description
31:16	01c6h RW	**TXFSTADDR_2:**

Bit Range	Default & Access	Description
15:0	0184h RW	**TXFDEP_2:** Reserved.

19.6.94 GTXFIFOSIZ3—Offset C30Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ3: [BAR] + C30Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 034A0184h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0

Bits 31:16: TXFSTADDR_3; Bits 15:0: TXFDEP_3

Bit Range	Default & Access	Description
31:16	034ah RW	**TXFSTADDR_3:**
15:0	0184h RW	**TXFDEP_3:**

19.6.95 GTXFIFOSIZ4—Offset C310h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ4: [BAR] + C310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 04CE0082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits 31:16: TXFSTADDR_4; Bits 15:0: TXFDEP_4

Bit Range	Default & Access	Description
31:16	04ceh RW	**TXFSTADDR_4:**

Bit Range	Default & Access	Description
15:0	0082h RW	**TXFDEP_4:**

19.6.96 GTXFIFOSIZ5—Offset C314h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ5: [BAR] + C314h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 05500082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Fields: TXFSTADDR_5 (bits 31:16), TXFDEP_5 (bits 15:0)

Bit Range	Default & Access	Description
31:16	0550h RW	**TXFSTADDR_5:**
15:0	0082h RW	**TXFDEP_5:**

19.6.97 GTXFIFOSIZ6—Offset C318h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ6: [BAR] + C318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 05D20082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Fields: TXFSTADDR_6 (bits 31:16), TXFDEP_6 (bits 15:0)

Bit Range	Default & Access	Description
31:16	05d2h RW	**TXFSTADDR_6:**

Bit Range	Default & Access	Description
15:0	0082h RW	**TXFDEP_6:**

19.6.98 GTXFIFOSIZ7—Offset C31Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ7: [BAR] + C31Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 06540082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Fields: TXFSTADDR_7 (bits 31:16), TXFDEP_7 (bits 15:0)

Bit Range	Default & Access	Description
31:16	0654h RW	**TXFSTADDR_7:**
15:0	0082h RW	**TXFDEP_7:**

19.6.99 GTXFIFOSIZ8—Offset C320h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ8: [BAR] + C320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 06D60022h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Fields: TXFSTADDR_8 (bits 31:16), TXFDEP_8 (bits 15:0)

Bit Range	Default & Access	Description
31:16	06d6h RW	**TXFSTADDR_8:**

Bit Range	Default & Access	Description
15:0	0022h RW	**TXFDEP_8:**

19.6.100 GTXFIFOSIZ9—Offset C324h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ9: [BAR] + C324h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 06F80022h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
TXFSTADDR_9																TXFDEP_9															

Bit Range	Default & Access	Description
31:16	06f8h RW	**TXFSTADDR_9:**
15:0	0022h RW	**TXFDEP_9:**

19.6.101 GTXFIFOSIZ10—Offset C328h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ10: [BAR] + C328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 071A0022h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
TXFSTADDR_10																TXFDEP_10															

Bit Range	Default & Access	Description
31:16	071ah RW	**TXFSTADDR_10:**

Bit Range	Default & Access	Description
15:0	0022h RW	**TXFDEP_10:**

19.6.102 GTXFIFOSIZ11—Offset C32Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ11: [BAR] + C32Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 073C0022h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits 31:16: TXFSTADDR_11; Bits 15:0: TXFDEP_11

Bit Range	Default & Access	Description
31:16	073ch RW	**TXFSTADDR_11:**
15:0	0022h RW	**TXFDEP_11:**

19.6.103 GTXFIFOSIZ12—Offset C330h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ12: [BAR] + C330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 075E0022h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits 31:16: TXFSTADDR_12; Bits 15:0: TXFDEP_12

Bit Range	Default & Access	Description
31:16	075eh RW	**TXFSTADDR_12:**

Bit Range	Default & Access	Description
15:0	0022h RW	**TXFDEP_12:**

19.6.104 GTXFIFOSIZ13—Offset C334h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ13: [BAR] + C334h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07800022h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
TXFSTADDR_13																TXFDEP_13															

Bit Range	Default & Access	Description
31:16	0780h RW	**TXFSTADDR_13:**
15:0	0022h RW	**TXFDEP_13:**

19.6.105 GTXFIFOSIZ14—Offset C338h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ14: [BAR] + C338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07A20022h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
TXFSTADDR_14																TXFDEP_14															

Bit Range	Default & Access	Description
31:16	07a2h RW	**TXFSTADDR_14:**

Bit Range	Default & Access	Description
15:0	0022h RW	**TXFDEP_14:**

19.6.106 GTXFIFOSIZ15—Offset C33Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GTXFIFOSIZ15: [BAR] + C33Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 07C40022h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits 31:16: TXFSTADDR_15; Bits 15:0: TXFDEP_15

Bit Range	Default & Access	Description
31:16	07c4h RW	**TXFSTADDR_15:**
15:0	0022h RW	**TXFDEP_15:**

19.6.107 GRXFIFOSIZ0—Offset C380h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GRXFIFOSIZ0: [BAR] + C380h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000385h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	1

Bits 31:16: RXFSTADDR_0; Bits 15:0: RXFDEP_0

Bit Range	Default & Access	Description
31:16	0h RW	**RXFSTADDR_0:**

Bit Range	Default & Access	Description
15:0	0385h RW	**RXFDEP_0:**

19.6.108 GRXFIFOSIZ1—Offset C384h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GRXFIFOSIZ1: [BAR] + C384h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 03850000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
RXFSTADDR_1	RXFDEP_1

Bit Range	Default & Access	Description
31:16	0385h RW	**RXFSTADDR_1:**
15:0	0000h RW	**RXFDEP_1:**

19.6.109 GRXFIFOSIZ2—Offset C388h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GRXFIFOSIZ2: [BAR] + C388h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 03850000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
RXFSTADDR_2	RXFDEP_2

Bit Range	Default & Access	Description
31:16	0385h RW	**RXFSTADDR_2:**

Bit Range	Default & Access	Description
15:0	0h RW	**RXFDEP_2:**

19.6.110 GEVNTADRLO—Offset C400h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GEVNTADRLO: [BAR] + C400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EVNTADRLO

Bit Range	Default & Access	Description
31:0	0h RW	**EVNTADRLO:** field EVNTADRLO

19.6.111 GEVNTADRHI—Offset C404h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GEVNTADRHI: [BAR] + C404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EVNTADRHI

Bit Range	Default & Access	Description
31:0	0h RW	**EVNTADRHI:** Reg field EVNTADRHI

19.6.112 GEVNTSIZ—Offset C408h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GEVNTSIZ: [BAR] + C408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30:16	15:0
0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
EVNTINTRPTMASK	RSVD74	EVENTSIZ

Bit Range	Default & Access	Description
31	0h RW	**EVNTINTRPTMASK:** Reg field EVNTINTRPTMASK
30:16	0h RO	**RSVD74:** reserved
15:0	0h RW	**EVENTSIZ:** Reg field EVENTSIZ

19.6.113 GEVNTCOUNT—Offset C40Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GEVNTCOUNT: [BAR] + C40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:16	15:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
RSVD75	EVNTCOUNT

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD75:** reserved
15:0	0h RO	**EVNTCOUNT:** Reg field EVNTCOUNT

19.6.114 GHWPARAMS8—Offset C600h

flag Value After Reset: 0xc00 Global Hardware Parameters Register 8

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GHWPARAMS8: [BAR] + C600h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00002000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

DWC_USB3_DCACHE_DEPTH_INFO

Bit Range	Default & Access	Description
31:0	2000h RO	**DWC_USB3_DCACHE_DEPTH_INFO:**

19.6.115 DCFG—Offset C700h

flag Value After Reset: 0x80804 Device Configuration Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DCFG: [BAR] + C700h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00080800h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

DCFG_RSVD | IGNSTRMPP | LPMCAP | NUMP | INTRNUM | PERFRINT | DEVADDR | DEVSPD

Bit Range	Default & Access	Description
31:24	0h RO	**DCFG_RSVD:**
23	0h RW	**IGNSTRMPP:** Reserved

Bit Range	Default & Access	Description
22	0h RW	**LPMCAP:** LPM Capable
21:17	04h RW	**NUMP:** Reg field NUMP
16:12	0h RW	**INTRNUM:** Reg field INTRNUM
11:10	2h RW	**PERFRINT:** Reg field PERFRINT
9:3	0h RW	**DEVADDR:** Reg field DEVADDR
2:0	0h RW	**DEVSPD:** flag Value After Reset: 0x4 Reg field DEVSPD

19.6.116 DCTL—Offset C704h

Device Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DCTL: [BAR] + C704h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RUN_STOP	CSFTRST	LSFTRST	HIRDTHRES	APPL1RES	RSVD40	TRGTULST	RSVD41	INITU2ENA	REJECTU2DIS	INITU1ENA	REJECTU1DIS	ULSTCHNGREQ	TSTCTL	RSVD0

Bit Range	Default & Access	Description
31	0h RW	**RUN_STOP:** Run/Stop
30	0h RW	**CSFTRST:** Core Soft Reset
29	0h RW	**LSFTRST:** Light Soft Reset
28:24	0h RW	**HIRDTHRES:** Reg field HIRDTHRES
23	0h RW	**APPL1RES:** LPM Response Programmed by Application
22:21	0h RO	**RSVD40:** reserved

Bit Range	Default & Access	Description
20:17	0h RW	**TRGTULST:**
16:13	0h RO	**RSVD41:** reserved
12	0h RW	**INITU2ENA:** Initiate U2 Enable
11	0h RW	**REJECTU2DIS:**
10	0h RW	**INITU1ENA:** Compliance
9	0h RW	**REJECTU1DIS:**
8:5	0h RW	**ULSTCHNGREQ:** Reg field ULSTCHNGREQ
4:1	0h RW	**TSTCTL:** Reg field TSTCTL
0	0h RO	**RSVD0:** reserved

19.6.117 DEVTEN—Offset C708h

Device Event Enable Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEVTEN: [BAR] + C708h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
								RSVD2										U2INACTTIMOUTRCVDEN	VENDEVTSTRCVDEN	EVNTOVERFLOWEN	CMDCMPLTEN	ERRTICERREVTEN	RSVD39	SOFTEVTEN	EOPFEVTEN	RSVD3	WKUPEVTEN	ULSTCNGEN	CONNECTDONEEVTEN	USBRSTEVTEN	DISSCONNEVTEN

Bit Range	Default & Access	Description
31:14	0h RO	**RSVD2:** reserved
13	0h RW	**U2INACTTIMOUTRCVDEN:** U2 Inactivity Timeout LMP Received Event Enable

Bit Range	Default & Access	Description
12	0h RW	**VENDEVTSTRCVDEN:** Vendor Device Test LMP Received Event
11	0h RW	**EVNTOVERFLOWEN:** Event Buffer Overflow Event Enable
10	0h RW	**CMDCMPLTEN:** Generic Command Complete Event Enable
9	0h RW	**ERRTICERREVTEN:** Erratic Error Event Enable
8	0h RW	**RSVD39:** reserved
7	0h RW	**SOFTEVTEN:** Start of
6	0h RW	**EOPFEVTEN:** End of Periodic Frame Event Enable
5	0h RW	**RSVD3:** reserved
4	0h RW	**WKUPEVTEN:** Resume/Remote Wakeup Detected Event Enable
3	0h RW	**ULSTCNGEN:** USB/Link State Change Event Enable
2	0h RW	**CONNECTDONEEVTEN:** Connection Done Enable
1	0h RW	**USBRSTEVTEN:** USB Reset Enable
0	0h RW	**DISSCONNEVTEN:** Disconnect Detected Event Enable

19.6.118 DSTS—Offset C70Ch

flag Value After Reset: 0x20820004 Device Status Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTS: [BAR] + C70Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00120004h

Bits	Value	Field
31:30	0 0	DSTS_RSVD2
29	0	DCNRD
28	0	SRE
27:26	0 0	DSTS_RSVD1
25	0	RSS
24	0	SSS
23	0	COREIDLE
22	0	DEVCTRLHLT
21:18	0 1 0 0	USBLNKST
17	1	RXFIFOEMPTY
16:3	0 0 0 0 0 0 0 0 0 0 0 0 0 0	SOFFN
2:0	1 0 0	CONNECTSPD

Bit Range	Default & Access	Description
31:30	0h RO	**DSTS_RSVD2:**
29	0h RO	**DCNRD:** Value After Reset: 0x1 Device Controller Not Ready: The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. Software must wait for this bit to be de-asserted to zero before processing DS TS.USBLnk
28	0h RW	**SRE:** Save/Restore Error (SRE) -RW1C. Default = '0'. If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'. Refer to section 4.23.2 for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Save/Restore completion status for the selected VF. Refer to section 8 for more information.x
27:26	0h RO	**DSTS_RSVD1:**
25	0h RO	**RSS:** Restore State Status: This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.RSS to '0'
24	0h RO	**SSS:** Save State Status: This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'.
23	0h RO	**COREIDLE:** flag Value After Reset: 0x1 Core Idle
22	0h RO	**DEVCTRLHLT:** Device Controller Halted
21:18	4h RO	**USBLNKST:** flag Value After Reset: 0x0 Reg field USBLNKST
17	1h RO	**RXFIFOEMPTY:** RxFIFO Empty
16:3	0h RO	**SOFFN:** Frame/Microframe Number of the Received SOF: When the core is operating at high-speed, this field contains a microframe number. When the core is operating at full- or low-speed, this field contains a frame number.
2:0	4h RO	**CONNECTSPD:** Reg field CONNECTSPD

19.6.119 DGCMDPAR—Offset C710h

Device Generic Command Parameter Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DGCMDPAR: [BAR] + C710h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reserved.

19.6.120 DGCMD—Offset C714h

Device Generic Command Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DGCMD: [BAR] + C714h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

RSVD6 CMDSTATUS Rsvd5 CMDACT Rsvd4 CMDIOC CMDTYP

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD6:** reserved
15:12	0h RO	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RO	**Rsvd5:** reserved
10	0h WO	**CMDACT:** Command Active
9	0h RO	**Rsvd4:** reserved
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.121 DALEPENA—Offset C720h

Device Active USB Endpoint Enable Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DALEPENA: [BAR] + C720h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

USBACTEP

Bit Range	Default & Access	Description
31:0	0h RW	**USBACTEP:** Reg field USBACTEP

19.6.122 DEPCMDPAR2_0—Offset C800h

Reg field PARAMETER

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_0: [BAR] + C800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.123 DEPCMDPAR1_0—Offset C804h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_0: [BAR] + C804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.124 DEPCMDPAR0_0—Offset C808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_0: [BAR] + C808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.125 DEPCMD_0—Offset C80Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_0: [BAR] + C80Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.126 DEPCMDPAR2_1—Offset C810h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_1: [BAR] + C810h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.127 DEPCMDPAR1_1—Offset C814h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_1: [BAR] + C814h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.128 DEPCMDPAR0_1—Offset C818h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR0_1: [BAR] + C818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.129 DEPCMD_1—Offset C81Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_1: [BAR] + C81Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.130 DEPCMDPAR2_2—Offset C820h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_2: [BAR] + C820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.131 DEPCMDPAR1_2—Offset C824h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_2: [BAR] + C824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.132 DEPCMDPAR0_2—Offset C828h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_2: [BAR] + C828h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.133 DEPCMD_2—Offset C82Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_2: [BAR] + C82Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.134 DEPCMDPAR2_3—Offset C830h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_3: [BAR] + C830h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.135 DEPCMDPAR1_3—Offset C834h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_3: [BAR] + C834h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.136 DEPCMDPAR0_3—Offset C838h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_3: [BAR] + C838h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.137 DEPCMD_3—Offset C83Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_3: [BAR] + C83Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.138 DEPCMDPAR2_4—Offset C840h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_4: [BAR] + C840h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.139 DEPCMDPAR1_4—Offset C844h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_4: [BAR] + C844h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
PARAMETER							

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.140 DEPCMDPAR0_4—Offset C848h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_4: [BAR] + C848h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
PARAMETER							

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.141 DEPCMD_4—Offset C84Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_4: [BAR] + C84Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
STREAMNUM				CMDSTATUS	HIPRI_FORCERM, CMDACT, R39, CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.142 DEPCMDPAR2_5—Offset C850h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_5: [BAR] + C850h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reserved.

19.6.143 DEPCMDPAR1_5—Offset C854h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_5: [BAR] + C854h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PARAMETER																															

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reserved.

19.6.144 DEPCMDPAR0_5—Offset C858h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_5: [BAR] + C858h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PARAMETER																															

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.145 DEPCMD_5—Offset C85Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_5: [BAR] + C85Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
STREAMNUM																CMDSTATUS				HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90				CMDTYP			

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.146 DEPCMDPAR2_6—Offset C860h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_6: [BAR] + C860h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.147 DEPCMDPAR1_6—Offset C864h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_6: [BAR] + C864h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:0
Default	0000 0000 0000 0000 0000 0000 0000 0000
Field	PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.148 DEPCMDPAR0_6—Offset C868h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_6: [BAR] + C868h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:0
Default	0000 0000 0000 0000 0000 0000 0000 0000
Field	PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.149 DEPCMD_6—Offset C86Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_6: [BAR] + C86Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:16	15:12	11	10	9	8	7:4	3:0
Default	0000 0000 0000 0000	0000	0	0	0	0	0000	0000
Field	STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.150 DEPCMDPAR2_7—Offset C870h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_7: [BAR] + C870h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.151 DEPCMDPAR1_7—Offset C874h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_7: [BAR] + C874h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.152 DEPCMDPAR0_7—Offset C878h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_7: [BAR] + C878h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.153 DEPCMD_7—Offset C87Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_7: [BAR] + C87Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:16	15:12	11	10	9	8	7:4	3:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0
STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.154 DEPCMDPAR2_8—Offset C880h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_8: [BAR] + C880h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.155 DEPCMDPAR1_8—Offset C884h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_8: [BAR] + C884h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.156 DEPCMDPAR0_8—Offset C888h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_8: [BAR] + C888h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.157 DEPCMD_8—Offset C88Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_8: [BAR] + C88Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.158 DEPCMDPAR2_9—Offset C890h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_9: [BAR] + C890h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.159 DEPCMDPAR1_9—Offset C894h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_9: [BAR] + C894h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.160 DEPCMDPAR0_9—Offset C898h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_9: [BAR] + C898h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.161 DEPCMD_9—Offset C89Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_9: [BAR] + C89Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP
31:16	15:12	11	10	9	8	7:4	3:0

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.162 DEPCMDPAR2_10—Offset C8A0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_10: [BAR] + C8A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PARAMETER																															

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.163 DEPCMDPAR1_10—Offset C8A4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_10: [BAR] + C8A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PARAMETER																															

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.164 DEPCMDPAR0_10—Offset C8A8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_10: [BAR] + C8A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.165 DEPCMD_10—Offset C8ACh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_10: [BAR] + C8ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.166 DEPCMDPAR2_11—Offset C8B0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_11: [BAR] + C8B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.167 DEPCMDPAR1_11—Offset C8B4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_11: [BAR] + C8B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.168 DEPCMDPAR0_11—Offset C8B8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_11: [BAR] + C8B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.169 DEPCMD_11—Offset C8BCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_11: [BAR] + C8BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39

Bit Range	Default & Access	Description
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.170 DEPCMDPAR2_12—Offset C8C0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_12: [BAR] + C8C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.171 DEPCMDPAR1_12—Offset C8C4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_12: [BAR] + C8C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.172 DEPCMDPAR0_12—Offset C8C8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_12: [BAR] + C8C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.173 DEPCMD_12—Offset C8CCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_12: [BAR] + C8CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Command Active
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.174 DEPCMDPAR2_13—Offset C8D0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_13: [BAR] + C8D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.175 DEPCMDPAR1_13—Offset C8D4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_13: [BAR] + C8D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.176 DEPCMDPAR0_13—Offset C8D8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_13: [BAR] + C8D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.177 DEPCMD_13—Offset C8DCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_13: [BAR] + C8DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
STREAMNUM																CMDSTATUS				HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90				CMDTYP			

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Command Interrupt on Complete
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.178 DEPCMDPAR2_14—Offset C8E0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_14: [BAR] + C8E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PARAMETER																															

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.179 DEPCMDPAR1_14—Offset C8E4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_14: [BAR] + C8E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.180 DEPCMDPAR0_14—Offset C8E8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_14: [BAR] + C8E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.181 DEPCMD_14—Offset C8ECh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_14: [BAR] + C8ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:16	15:12	11	10	9	8	7:4	3:0
0000 0000 0000 0000	0000	0	0	0	0	0000	0000
STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.182 DEPCMDPAR2_15—Offset C8F0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_15: [BAR] + C8F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:0
0000 0000 0000 0000 0000 0000 0000 0000
PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.183 DEPCMDPAR1_15—Offset C8F4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_15: [BAR] + C8F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.184 DEPCMDPAR0_15—Offset C8F8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_15: [BAR] + C8F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.185 DEPCMD_15—Offset C8FCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_15: [BAR] + C8FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.186 DEPCMDPAR2_16—Offset C900h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_16: [BAR] + C900h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.187 DEPCMDPAR1_16—Offset C904h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_16: [BAR] + C904h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.188 DEPCMDPAR0_16—Offset C908h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_16: [BAR] + C908h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.189 DEPCMD_16—Offset C90Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_16: [BAR] + C90Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDACT
11	0h RW	**HIPRI_FORCERM:** Reg field CMDACT
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.190 DEPCMDPAR2_17—Offset C910h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_17: [BAR] + C910h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.191 DEPCMDPAR1_17—Offset C914h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_17: [BAR] + C914h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.192 DEPCMDPAR0_17—Offset C918h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_17: [BAR] + C918h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.193 DEPCMD_17—Offset C91Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_17: [BAR] + C91Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM, CMDSTATUS, HIPRI_FORCERM, CMDACT, R39, CMDIOC, RSVD90, CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39

Bit Range	Default & Access	Description
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.194 DEPCMDPAR2_18—Offset C920h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_18: [BAR] + C920h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.195 DEPCMDPAR1_18—Offset C924h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_18: [BAR] + C924h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.196 DEPCMDPAR0_18—Offset C928h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_18: [BAR] + C928h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: PARAMETER (31:0)

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.197 DEPCMD_18—Offset C92Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_18: [BAR] + C92Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM (31:16)	CMDSTATUS (15:12)	HIPRI_FORCERM (11)	CMDACT (10)	R39 (9)	CMDIOC (8)	RSVD90 (7:4)	CMDTYP (3:0)

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.198 DEPCMDPAR2_19—Offset C930h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_19: [BAR] + C930h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.199 DEPCMDPAR1_19—Offset C934h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_19: [BAR] + C934h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.200 DEPCMDPAR0_19—Offset C938h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_19: [BAR] + C938h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.201 DEPCMD_19—Offset C93Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_19: [BAR] + C93Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.202 DEPCMDPAR2_20—Offset C940h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_20: [BAR] + C940h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reserved.

19.6.203 DEPCMDPAR1_20—Offset C944h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_20: [BAR] + C944h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.204 DEPCMDPAR0_20—Offset C948h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_20: [BAR] + C948h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.205 DEPCMD_20—Offset C94Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_20: [BAR] + C94Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31–16	15–12	11	10	9	8	7–4	3–0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0
STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reserved.
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.206 DEPCMDPAR2_21—Offset C950h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_21: [BAR] + C950h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31–0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.207 DEPCMDPAR1_21—Offset C954h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_21: [BAR] + C954h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.208 DEPCMDPAR0_21—Offset C958h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_21: [BAR] + C958h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.209 DEPCMD_21—Offset C95Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMD_21: [BAR] + C95Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP
31:16	15:12	11	10	9	8	7:4	3:0

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.210 DEPCMDPAR2_22—Offset C960h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_22: [BAR] + C960h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.211 DEPCMDPAR1_22—Offset C964h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_22: [BAR] + C964h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.212 DEPCMDPAR0_22—Offset C968h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_22: [BAR] + C968h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.213 DEPCMD_22—Offset C96Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_22: [BAR] + C96Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.214 DEPCMDPAR2_23—Offset C970h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_23: [BAR] + C970h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.215 DEPCMDPAR1_23—Offset C974h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_23: [BAR] + C974h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.216 DEPCMDPAR0_23—Offset C978h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_23: [BAR] + C978h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.217 DEPCMD_23—Offset C97Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_23: [BAR] + C97Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39

Bit Range	Default & Access	Description
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.218 DEPCMDPAR2_24—Offset C980h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR2_24: [BAR] + C980h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.219 DEPCMDPAR1_24—Offset C984h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DEPCMDPAR1_24: [BAR] + C984h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.220 DEPCMDPAR0_24—Offset C988h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_24: [BAR] + C988h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: PARAMETER (31:0)

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.221 DEPCMD_24—Offset C98Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_24: [BAR] + C98Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: STREAMNUM (31:16), CMDSTATUS (15:12), HIPRI_FORCERM (11), CMDACT (10), R39 (9), CMDIOC (8), RSVD90 (7:4), CMDTYP (3:0)

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.222 DEPCMDPAR2_25—Offset C990h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_25: [BAR] + C990h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.223 DEPCMDPAR1_25—Offset C994h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_25: [BAR] + C994h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.224 DEPCMDPAR0_25—Offset C998h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_25: [BAR] + C998h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.225 DEPCMD_25—Offset C99Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_25: [BAR] + C99Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
STREAMNUM																CMDSTATUS				HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90				CMDTYP			

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.226 DEPCMDPAR2_26—Offset C9A0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_26: [BAR] + C9A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PARAMETER																															

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.227 DEPCMDPAR1_26—Offset C9A4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_26: [BAR] + C9A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.228 DEPCMDPAR0_26—Offset C9A8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_26: [BAR] + C9A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.229 DEPCMD_26—Offset C9ACh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_26: [BAR] + C9ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:16	15:12	11	10	9	8	7:4	3:0
Default	0000 0000 0000 0000	0000	0	0	0	0	0000	0000
Field	STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.230 DEPCMDPAR2_27—Offset C9B0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_27: [BAR] + C9B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:0
Default	0000 0000 0000 0000 0000 0000 0000 0000
Field	PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.231 DEPCMDPAR1_27—Offset C9B4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_27: [BAR] + C9B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.232 DEPCMDPAR0_27—Offset C9B8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_27: [BAR] + C9B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.233 DEPCMD_27—Offset C9BCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_27: [BAR] + C9BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.234 DEPCMDPAR2_28—Offset C9C0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_28: [BAR] + C9C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.235 DEPCMDPAR1_28—Offset C9C4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_28: [BAR] + C9C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.236 DEPCMDPAR0_28—Offset C9C8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_28: [BAR] + C9C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.237 DEPCMD_28—Offset C9CCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_28: [BAR] + C9CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STREAMNUM | CMDSTATUS | HIPRI_FORCERM | CMDACT | R39 | CMDIOC | RSVD90 | CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reserved.
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.238 DEPCMDPAR2_29—Offset C9D0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_29: [BAR] + C9D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.239 DEPCMDPAR1_29—Offset C9D4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_29: [BAR] + C9D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.240 DEPCMDPAR0_29—Offset C9D8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	DEPCMDPAR0_29: [BAR] + C9D8h

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_29: [BAR] + C9D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: PARAMETER (31:0)

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.241 DEPCMD_29—Offset C9DCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_29: [BAR] + C9DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: STREAMNUM (31:16), CMDSTATUS (15:12), HIPRI_FORCERM (11), CMDACT (10), R39 (9), CMDIOC (8), RSVD90 (7:4), CMDTYP (3:0)

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39

Bit Range	Default & Access	Description
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.242 DEPCMDPAR2_30—Offset C9E0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_30: [BAR] + C9E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.243 DEPCMDPAR1_30—Offset C9E4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_30: [BAR] + C9E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.244 DEPCMDPAR0_30—Offset C9E8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_30: [BAR] + C9E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Field	PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.245 DEPCMD_30—Offset C9ECh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_30: [BAR] + C9ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:16	15:12	11	10	9	8	7:4	3:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0
Field	STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.246 DEPCMDPAR2_31—Offset C9F0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR2_31: [BAR] + C9F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.247 DEPCMDPAR1_31—Offset C9F4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR1_31: [BAR] + C9F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.248 DEPCMDPAR0_31—Offset C9F8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMDPAR0_31: [BAR] + C9F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PARAMETER

Bit Range	Default & Access	Description
31:0	0h RW	**PARAMETER:** Reg field PARAMETER

19.6.249 DEPCMD_31—Offset C9FCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEPCMD_31: [BAR] + C9FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:16	15:12	11	10	9	8	7:4	3:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	0	0 0 0 0	0 0 0 0
STREAMNUM	CMDSTATUS	HIPRI_FORCERM	CMDACT	R39	CMDIOC	RSVD90	CMDTYP

Bit Range	Default & Access	Description
31:16	0h RW	**STREAMNUM:**
15:12	0h RW	**CMDSTATUS:** Reg field CMDSTATUS
11	0h RW	**HIPRI_FORCERM:** Reg field HIPRI_FORCERM
10	0h RW	**CMDACT:** Reg field CMDACT
9	0h RW	**R39:** Reg field R39
8	0h RW	**CMDIOC:** Reg field CMDIOC
7:4	0h RW	**RSVD90:** reserved
3:0	0h RW	**CMDTYP:** Reg field CMDTYP

19.6.250 OCFG—Offset CC00h

OTG Configuration Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OCFG: [BAR] + CC00h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31:3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0
RSVD0	OTG_Version	HNPCap	SRPCap

Bit Range	Default & Access	Description
31:3	0h RO	**RSVD0:** reserved

Bit Range	Default & Access	Description
2	0h RW	**OTG_Version:**
1	0h RW	**HNPCap:** RSP/HNP Capability: The terminology RSP is used when the core is operating in SS mode, and HNP is used when the core is operating in non-SS mode. The application uses this bit to control the DWC_usb3 core's RSP/HNP capabilities. n 1'b0: RSP/HNP capability is not enabled. n 1'b1: RSP/HNP capability is enabled. Note: This bit is writable only if RSP/HNP mode is specified for Mode of Operation in coreConsultant, that is when DWC_USB3_EN_OTG != 0 and DWC_USB3_MODE = DRD. If RSP/HNP mode is not specified, this bit is Read Only, and is set to 1'b0.
0	0h RW	**SRPCap:** SRP Capability: The application uses this bit to control the DWC_usb3 core's SRP capabilities. n 1'b0: SRP capability is not enabled. n 1'b1: SRP capability is enabled. If this bit is not set for B-device, it cannot request the connected A-device (host) to activate Vbus and start a session. If this bit is not set for A-device, it cannot detect the SRP from B-device (device) to activate Vbus and start a session. Note: This bit is writable only if OTG is enabled in coreConsultant (DWC_USB3_EN_OTG !=0). If OTG is not enabled, then this bit is Read Only and is set to 1'b0.

19.6.251 OCTL—Offset CC04h

OTG Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OCTL: [BAR] + CC04h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000040h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
RSVD0																									PeriMode	PrtPwrCtl	HNPReq	SesReq	TermSelDLPulse	DevSetHNPEn	HstSetHNPEn

Bit Range	Default & Access	Description
31:7	0h RO	**RSVD0:** reserved
6	1h RW	**PeriMode:** Peripheral Mode: Application uses this bit to program the core to work as a peripheral or as a host. n 1'b0: The OTG device acts as a host n 1'b1: The OTG device acts as a peripheral
5	0h RW	**PrtPwrCtl:** Port Power Control: Application sets this bit to initiate Vbus drive when it is an A-device. The application should clearthis bit only if it wants to switch off the Vbus to B-device. The core clears this bit in the following conditions: n Transition from any state to A-IDLE state defined in OTG2.0 state machine. n When AIDL_BDIS_TOUT occurs in A_SUSPEND n When A_WAIT_BCON_TOUT occurs in A_WAIT_BCON n Transition to any B- state defined in OTG2.0 state machine
4	0h RW	**HNPReq:** HNP Request: n 1'b0: No HNP request n 1'b1: HNP request The application sets this bit to initiate a HNP request to the connected USB host. The application clears this bit by writing a 1'b0 when either of the following is detected: n OEVT.OTGBDevBHostEndEvnt n OEVT.OTGBDevVBusChngEvnt

Bit Range	Default & Access	Description
3	0h RW	**SesReq:** Session Request: n 1'b0: No session request n 1'b1: Session request The application sets this bit to initiate a session request on the USB. Writing 1'b1 to this field will trigger the core to send SRP (data line pulsing) on PHY interface. In the absence of OEVT.OTGBDevSessVldDetEvnt after a session request, the application must wait for atleast TB_SRP_FAIL time (6 secs) before initiating another session request. This field returns 1'b0 when read.
2	0h RW	**TermSelDLPulse:** TermSel DLine Pulsing Selection: This bit selects utmi_termselect to drive data line pulse during SRP. n 1'b0: Data line pulsing using utmi_txvalid (default). n 1'b1: Data line pulsing using utmi_termsel.
1	0h RW	**DevSetHNPEn:** Device Set RSP/HNP Enable: n 1'b0: RSP/HNP is not enabled in the application n 1'b1: RSP/HNP is enabled in the application The application sets this bit in the following scenario: n In HS/FS mode, when it successfully receives a SetFeature.SetHNPEnable command from the connected USB host. n In SS mode, when it has sent a b3_ntf_hst_rel to the A-device, or the A-device has sent an a3_ntf_host_req. Note: The terminology RSP is used when the core is operating in SS mode, and HNP is used when the core is operating in non-SS mode.
0	0h RW	**HstSetHNPEn:** Host Set RSP/HNP Enable: n 1'b0: Host Set RSP/HNP is not enabled n 1'b1: Host Set RSP/HNP is enabled The application sets this bit in the following scenario: n In HS/FS mode, when it has successfully enabled HNP (using the SetFeature.SetHNPEnable command) from the connected device. n In SS mode, when it has successfully enabled b3_rsp_enable feature in RSP-capable Device using SetFeature command while operating as an A-Host, or when it has received a b3_ntf_hst_rel through SetFeature command while operating as A-peripheral. Note: The terminology RSP is used when the core is operating in SS mode, and HNP is used when the core is operating in non-SS mode.

19.6.252 OEVT—Offset CC08h

Value After Reset: 0x0 OTG Events Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OEVT: [BAR] + CC08h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 80000000h

Bits	Default	Field
31	1	DeviceMode
30:25	0 0 0 0 0 0	RSVD0
24	0	OTGConIDStsChngEvnt
23:21	0 0 0	RSVD1
20	0	OTGADevBHostEndEvnt
19	0	OTGADevHostEvnt
18	0	OTGADevHNPChngEvnt
17	0	OTGADevSRPDetEvnt
16	0	OTGADevSessEndDetEvnt
15:12	0 0 0 0	RSVD2
11	0	OTGBDevBHostEndEvnt
10	0	OTGBDevHNPChngEvnt
9	0	OTGBDevSessVldDetEvnt
8	0	OTGBDevVBUSChngEvnt
7:4	0 0 0 0	RSVD3
3	0	BSesVld
2	0	HstNegSts
1	0	SesReqSts
0	0	OEVTError

Bit Range	Default & Access	Description
31	1h RO	**DeviceMode:** Device Mode: Indicates whether the device is in A-device or B-device mode based on utmiotg_iddig n 1'b0: A-Device mode n1'b1: B-Device mode The rest of the OTG Event Information bits (OTGxxxxEvtInfo) in OEVT register will be based on the contents of this field.

Bit Range	Default & Access	Description
30:25	0h RO	**RSVD0:** reserved
24	0h RO	**OTGConIDStsChngEvnt:** Write Behavior: oneToClear Connector ID Status Change Event: Set in both A-Dev/B-Dev Mode. This event is generated when there is a change in connector ID status.
23:21	0h RO	**RSVD1:** reserved
20	0h RO	**OTGADevBHostEndEvnt:** Write Behavior: oneToClear A-device B-Host End Event: Set in A-device Mode Only. The event is generated when B-device hascompleted its host role. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
19	0h RO	**OTGADevHostEvnt:** Write Behavior: oneToClear A-device host event: Set in A-device Mode Only. This event is generated when A-device enters host role. In HS/FS mode, it occurs after the initial connect to a B-device as A-host as well as when there is a role change from A-peripheral to A-host. Note: This bit is applicable only for OTG 2.0 mode of operation.
18	0h RO	**OTGADevHNPChngEvnt:** Write Behavior: oneToClear A-Dev HNP Change Event: Set in A-device Mode Only. The event is generated when there is an HNP attempt. Note: This bit is applicable only for OTG 2.0 mode of operation.
17	0h RO	**OTGADevSRPDetEvnt:** Write Behavior: oneToClear SRP Detect Event: Set in A-device Mode Only. This event is asserted when a session request from the B-device is detected via SRP. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
16	0h RO	**OTGADevSessEndDetEvnt:** Write Behavior: oneToClear Session End Detected Event: Set in A-device Mode Only. This event is asserted when the utmisrp_avalid signal goes low indicating the end of a session. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation
15:12	0h RO	**RSVD2:** Reserved
11	0h RO	**OTGBDevBHostEndEvnt:** Write Behavior: oneToClear B-Device B-Host End Event: Set in B-device Mode Only. This event is generated when B-device has completed its host role. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
10	0h RO	**OTGBDevHNPChngEvnt:** Write Behavior: oneToClear B-Dev HNP Change Event: Set in B-Device Mode only. This event is generated when there is a Success or Failure of an HNP attempt. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
9	0h RO	**OTGBDevSessVldDetEvnt:** Write Behavior: oneToClear Session Valid Detected Event: Set in B-device Mode Only. This event is asserted when there is a valid Vbus from A-device and B-device succeeds in starting a session. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
8	0h RO	**OTGBDevVBUSChngEvnt:** Write Behavior: oneToClear Vbus Change Event: Set in B-device Mode Only. This event is asserted when the utmisrp_bvalid signal goes low (indicating the end of a session), or goes high. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
7:4	0h RO	**RSVD3:** reserved
3	0h RO	**BSesVld:** Indicates the Device mode transceiver status. Indicates the Device mode transceiver status. The core updates this bit when OEVTEN.OTGBDevVBUSChngEvnt is set. 1b0: B-session is not valid 1b1: B-session is valid Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
2	0h RO	**HstNegSts:** Host Negotiation Status: The core updates this bit when any of the following bits is set: n OEVTEN.OTGADevHNPChngEvnt n OEVTEN.OTGBDevHNPChngEvnt This bit indicates Host Negotiation Success or Failure. n 1'b0: Host negotiation failure. In A-device, for HS/FS, this indicates an imminent end of session indication from the core. In B-device, for HS/LS, it indicates that the timer used to wait for an A-device to signal a connection (b_ase0_brst_tmout in OTG 2.0) timed out resulting in B-device staying as B-peripheral. n 1'b1: Host negotiation success. This indicates that the host negotiation was successful. Note: This bit is a pplicable only for OTG 2.0 mode of operation.

Bit Range	Default & Access	Description
1	0h RO	**SesReqSts:** Session Request Status: The core updates this bit when OEVTEN.OTGBDevSessVldDetEvnt is set. o 1'b0: Session request due to Vbus. This indicates that the session started due to Vbus without SRP detection by A-host. o 1'b1: Session request due to SRP. This indicates that the session started as a result of successful SRP detection by A-host. Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
0	0h RO	**OEVTError:** Write Behavior: oneToClear OTG Event Error: There are no errors currently defined.

19.6.253 OEVTEN—Offset CC0Ch

OTG Events Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OEVTEN: [BAR] + CC0Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	Value	Field
31:25	0 0 0 0 0 0 0	RSVD0
24	0	OTGConIDStsChngEvntEn
23:21	0 0 0	RSVD1
20	0	OTGADevBHostEndEvntEn
19	0	OTGADevHostEvntEn
18	0	OTGADevHNPChngEvntEn
17	0	OTGADevSRPDetEvntEn
16	0	OTGADevSessEndDetEvntEn
15:12	0 0 0 0	RSVD2
11	0	OTGBDevBHostEndEvntEn
10	0	OTGBDevHNPChngEvntEn
9	0	OTGBDevSessVldDetEvntEn
8	0	OTGBDevVBUSChngEvntEn
7:0	0 0 0 0 0 0 0 0	RSVD3

Bit Range	Default & Access	Description
31:25	0h RO	**RSVD0:** reserved
24	0h RW	**OTGConIDStsChngEvntEn:** Connector ID Status Change Event (OTGConIDStsChngEvnt) Set in both A-Dev/B-Dev Mode: This Event is generated when there is a change in connector ID status
23:21	0h RO	**RSVD1:** reserved
20	0h RW	**OTGADevBHostEndEvntEn:** A-device B-Host End Event Enable (OTGADevBHostEndEvntEn) When this bit is set, OEVT.OTGADevBHostEndEvnt is enabled. Else the event is disabled.
19	0h RW	**OTGADevHostEvntEn:** A-device host event: When this bit is set, OEVT.OTGADevHostEvnt is enabled. If not, the event is disabled
18	0h RW	**OTGADevHNPChngEvntEn:** A-Dev HNP Change EventEn: When this bit is set, OEVT.OTGADevHNPChngEvnt is enabled. If not, the event is disabled
17	0h RW	**OTGADevSRPDetEvntEn:** SRP Detect Event Enable: When this bit is set, OEVT.OTGADevSRPDetEvnt is enabled. If not, the event is disabled

Bit Range	Default & Access	Description
16	0h RW	**OTGADevSessEndDetEvntEn:** Session End Detected Event Enable (OTGADevSessEndDetEvntEn) When this bit is set, OEVT.OTGADevSessEndEvnt is enabled. Else the event is disabled
15:12	0h RO	**RSVD2:** reserved
11	0h RW	**OTGBDevBHostEndEvntEn:** B-device B-Host End Event Enable: When this bit is set, OEVT.OTGBDevHostEndEvnt is enabled. If not, the event is disabled
10	0h RW	**OTGBDevHNPChngEvntEn:** B-Dev HNP Change Event Enable: When this bit is set, OEVT.OTGBDevHNPChngEvnt is enabled. If not, the event is disabled
9	0h RW	**OTGBDevSessVldDetEvntEn:** Session Valid Detected Event Enable (OTGBDevSessVldDetEvntEn) Set in B-device Mode Only: This Event is asserted when there is a valid VBUS from A-device and B-device succeeds in starting a session.
8	0h RW	**OTGBDevVBUSChngEvntEn:** Vbus Change Event Enable: When this bit is set, OEVT.OTGBDevVBUSChngEvnt is enabled. If not, the event is disabled
7:0	0h RO	**RSVD3:** reserved

19.6.254 OSTS—Offset CC10h

flag Value After Reset: 0x819 OTG Status Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSTS: [BAR] + CC10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000019h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3	2	1	0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1	0	0	1
Field	RSVD0					OTGstate	RSVD1	xHCIPrtPower	BSesVld	ASesVld	ConIDSts

Bit Range	Default & Access	Description
31:12	0h RO	**RSVD0:** reserved
11:8	0h RO	**OTGstate:** This is a debug field indicating the current state of the OTG state machine. Value Encoding 4'b0000 A_IDLE 4'b0001 A_WAIT_VRISE 4'b0010 A_WAIT_BCON 4'b0011 A_WAIT_VFALL 4'b0100 A_VBUS_ERR 4'b0101 A_HOST 4'b0110 A_SUSPEND 4'b1111 A_PERIPHERAL 4'b0111 A_WAIT_PPWR 4'b1000 B_IDLE 4'b1001 B_SRP_INIT 4'b1010 B_PERIPHERAL 4'b1011 B_WAIT_ACON 4'b1100 B_HOST 4'b1101 A_WAIT_SWITCH 4'b1110 B_WAIT _SWITCH
7:4	1h RO	**RSVD1:** reserved
3	1h RO	**xHCIPrtPower:** This bit reflects the PORTSC.PP bit in the xHCI register.

Bit Range	Default & Access	Description
2	0h RO	**BSesVld:** Indicates the Device mode transceiver status. Indicates the Device mode transceiver status. The core updates this bit when OEVTEN.OTGBDevVBUSChngEvnt is set. 1b0: B-session is not valid 1b1: B-session is valid Note: This bit is applicable for OTG 2.0 and OTG 3.0 modes of operation.
1	0h RO	**ASesVld:** Indicates the Host mode transceiver status. 1b0: A-session is not valid 1b1: A-session is valid
0	1h RO	**ConIDSts:** Connector ID Status: Indicates the connector ID status n 1'b0: The DWC_usb3 core is in A-device mode n 1'b1: The DWC_usb3 core isin B-device mode Note: The reset value of this field depends on the power-on value of the IDDIG signal from the PHY.

19.6.255 ADPCFG—Offset CC20h

ADP Configuration Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ADPCFG: [BAR] + CC20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PrbPer	PrbDelta	PrbDschg	RSVD0

Bit Range	Default & Access	Description
31:30	0h RW	**PrbPer:** Probe Period: These bits set the T_ADP_PRB as follows: n 2'b00: 0.775 sec n 2'b01: 1.55 sec n 2'b10: 2.275 sec n 2'b11: Reserved The scaledown values for PrbPer are: n 2'b00: 12.5ms n 2'b01: 18.75ms n 2'b10: 25 ms n 2'b11: 31.25 ms
29:28	0h RW	**PrbDelta:** Probe Delta: These bits set the resolution for RTIM value. They are defined in units of 32 kHz clock cycles as follows: n2'b00: 1 cycles n 2'b01: 2 cycles n 2'b10: 3 cycles n 2'b11: 4 cycles For example, if this value is chosen to be 2'b01, it means that RTIM increments for every two 32 kHz clock cycles.
27:26	0h RW	**PrbDschg:** Probe Discharge: These bits set the time for TADP_DSCHG. They are defined as follows: n 2'b00: 4 msec n 2'b01: 8 msec n 2'b10: 16 msec n 2'b11: 32 msec The scaledown values for the PrbDschg are as follows: n 2'b00: 62.5 us n 2'b01: 125 us n 2'b10: 250 us n 2'b11: 500 us
25:0	0h RO	**RSVD0:** reserved

19.6.256 ADPCTL—Offset CC24h

ADP Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ADPCTL: [BAR] + CC24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0	EnaPrb	EnaSns	ADPEn	ADPRes	WB	RSVD1

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD0:** reserved
28	0h RW	**EnaPrb:** Enable Probe: When set to 1'b1 along with ADPEn, the core performs a probe operation.
27	0h RW	**EnaSns:** ADP Enable: When set to 1'b1, the core performs either ADP probing or sensing based on EnaPrb and EnaSns. ADPEn = 1'b0 gates the suspend clock for major portion of ADP related logic.
26	0h RW	**ADPEn:** ADP Enable: When set to 1'b1, the core performs either ADP probing or sensing based on EnaPrb and EnaSns. ADPEn = 1'b0 gates the suspend clock for major portion of ADP related logic.
25	0h RW	**ADPRes:** ADP Reset: When set to 1'b1, the ADP controller is reset. This bit is auto-cleared after the reset procedure is complete in the ADP controller.
24	0b RO	**WB:** Write Busy: n 1'b0: Write Completed n 1'b1: Write in Progress The application can read or write ADPCFG and ADPCTL registers only if this field is cleared. Hardware sets this bit when the write is in progress in the Suspend clock domain.
23:0	0h RO	**RSVD1:** reserved

19.6.257 ADPEVT—Offset CC28h

ADP Event Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ADPEVT: [BAR] + CC28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0	AdpPrbEvnt	AdpSnsEvnt	AdpTmoutEvnt	ADPRstCmpltEvnt	RSVD1	RTIM

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD0:** Reserved
28	0h RO	**AdpPrbEvnt:** Write Behavior: oneToClear ADP Probe Event: When this event is set, it means that the Vbus voltage is greater than VadpPrb or VadpPrb is reached.
27	0h RO	**AdpSnsEvnt:** Write Behavior: oneToClear ADP Sense Event: When this event is set, it means that the Vbus voltage is greater than VadpSns or VadpSns is reached.
26	0h RO	**AdpTmoutEvnt:** Write Behavior: oneToClear ADP Timeout Event: This event is relevant when ADP probe command is executed. When this event is set, it means that the ramp time is completed (GADPCTL.RTIM has reached its terminal value of 0x7FF). This is a debug feature that allows software to read the ramp time after each cycle.
25	0h RO	**ADPRstCmpltEvnt:** Write Behavior: oneToClear This event, when set, indicates that the ADP Reset command is successful
24:11	0h RO	**RSVD1:** reserved
10:0	0h RO	**RTIM:** RAMP TIME: These bits capture the latest time it took for Vbus to ramp from VADP_SINK to VADP_PRB. The bits are defined in units of 32 kHz clock cycles as follows: n 0x000: 1 cycles n 0x001: 2 cycles n 0x002: 3 cycles and so on till, n 0x7FF: 2048 cycles A time of 1024 cycles at 32 kHz corresponds to a time of 32 msec. Note for scaledown ramp_timeout, n PrbDelta = 2'b00 =) 6250 us n PrbDelta = 2'b01 =) 3125 us n PrbDelta = 2'b10 =) 1562.5 us n PrbDelta = 2'b11 =) 781.25 us

19.6.258 ADPEVTEN—Offset CC2Ch

ADP Event Enable Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ADPEVTEN: [BAR] + CC2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

Bits	31:29	28	27	26	25	24:0
Default	0 0 0	0	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Field	RSVD0	AdpPrbEvntEn	AdpSnsEvntEn	AdpTmoutEvntEn	ADPRstCmpltEvntEn	RSVD1

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD0:** Reserved
28	0h RW	**AdpPrbEvntEn:** ADP Probe Event Enable: When this bit is set, ADPPrbEvnt in ADPEVT register is enabled.
27	0h RW	**AdpSnsEvntEn:** ADP Sense Event Enable: When this bit is set, AdpSnsEvntEn in ADPEVT register is enabled.

Bit Range	Default & Access	Description
26	0h RW	**AdpTmoutEvntEn:** ADP Timeout Event Enable: When this bit is set, AdpTmoutEvntEn in ADPEVT register is enabled.
25	0h RW	**ADPRstCmpltEvntEn:** ADP Reset complete Event Enable: When this bit is set, ADPRstCmpltEvnt in ADPEVT register is enabled.
24:0	0h RO	**RSVD1:** Reserved

19.6.259 BCFG—Offset CC30h

BC Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCFG: [BAR] + CC30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD | IDDIG_SEL | CHIRP_EN

Bit Range	Default & Access	Description
31:2	0h RO	**RSVD:**
1	0h RW	**IDDIG_SEL:**
0	0h RW	**CHIRP_EN:**

19.6.260 BCEVT—Offset CC38h

BC Event Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCEVT: [BAR] + CC38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0							MV_ChngEvnt	RSVD1																			MultValIdBc				

Bit Range	Default & Access	Description
31:25	0h RO	**RSVD0:** reserved
24	0h RO	**MV_ChngEvnt:**
23:5	0h RO	**RSVD1:**
4:0	0h RO	**MultValIdBc:**

19.6.261 BCEVTEN—Offset CC3Ch

BC Event Enable Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

BCEVTEN: [BAR] + CC3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0							MV_ChngEvntEna	RSVD1																							

Bit Range	Default & Access	Description
31:25	0h RO	**RSVD0:** reserved
24	0h RW	**MV_ChngEvntEna:**
23:0	0h RO	**RSVD1:** reserved

19.7 USB 3.0 Device Memory Mapped I/O Registers

Table 222. Summary of USB 3.0 Device Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
8h	2	"APBFC_ILDOA0—Offset 8h" on page 2655	0000h
Ch	2	"APBFC_ILDOACLK0—Offset Ch" on page 2656	0000h
10h	2	"APBFC_ILDOS0—Offset 10h" on page 2657	0000h
14h	2	"APBFC_IPMA0—Offset 14h" on page 2658	0000h
18h	2	"APBFC_IPMA1—Offset 18h" on page 2660	0000h
1Ch	2	"APBFC_OPMA0—Offset 1Ch" on page 2661	0000h
20h	2	"APBFC_IPIPE0—Offset 20h" on page 2661	0000h
24h	2	"APBFC_IPIPE1A—Offset 24h" on page 2662	0000h
28h	2	"APBFC_IPIPE1B—Offset 28h" on page 2663	0000h
2Ch	2	"APBFC_IPIPE1C—Offset 2Ch" on page 2664	0000h
30h	2	"APBFC_IPIPE2—Offset 30h" on page 2664	0000h
34h	2	"APBFC_IPIPE3—Offset 34h" on page 2665	0000h
38h	2	"APBFC_OPIPE0—Offset 38h" on page 2666	0000h
3Ch	2	"APBFC_OPIPE1A—Offset 3Ch" on page 2667	0000h
40h	2	"APBFC_OPIPE1B—Offset 40h" on page 2668	0000h
44h	2	"APBFC_OPIPE1C—Offset 44h" on page 2669	0000h
48h	2	"APBFC_OPIPE2—Offset 48h" on page 2669	0000h
4Ch	2	"APBFC_OTG3_MISC0—Offset 4Ch" on page 2670	000Bh
50h	2	"APBFC_OTG3_MISC1—Offset 50h" on page 2671	0000h
54h	2	"APBFC_OTG3_MISC2—Offset 54h" on page 2671	1100h
58h	2	"APBFC_OTG3_MISC3—Offset 58h" on page 2672	7008h
5Ch	2	"APBFC_U3PMU_CFG0_REG—Offset 5Ch" on page 2673	0000h
60h	2	"APBFC_U3PMU_CFG1_REG—Offset 60h" on page 2674	0000h

19.7.1 APBFC_ILDOA0—Offset 8h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_ILDOA0: [BAR + 10F800h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	APBFC_ILDOA0_RSVD						ildoa_trimoverride_reg					ildoa_trimoverride_reg_sel	ildoa_trimoverridesel_reg	ildoa_trimoverridesel_reg_sel	ildoa_en_reg	lildoa_en_reg_sel

Bit Range	Default & Access	Description
15:10	0h RW	**APBFC_ILDOA0_RSVD:** Reserved.
9:5	0h RW	**ildoa_trimoverride_reg:** Reserved.
4	0b RW	**ildoa_trimoverride_reg_sel:** Reserved.
3	0b RW	**ildoa_en_reg (ildoa_trimoverridesel_reg):** Reserved.
2	0b RW	**ildoa_trimoverridesel_reg_sel:** Reserved.
1	0b RW	**ildoa_en_reg:** Reserved.
0	0b RW	**lildoa_en_reg_sel:** Reserved.

19.7.2 APBFC_ILDOACLK0—Offset Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_ILDOACLK0: [BAR + 10F800h] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APBFC_ILDOACLK0_RSVD						ildoaclk_trimoverride_reg					ildoaclk_trimoverride_reg_sel	ildoaclk_trimoverridesel_reg	ildoaclk_trimoverridesel_reg_sel	ildoaclk_en_reg	ildoaclk_en_reg_sel

Bit Range	Default & Access	Description
15:10	0h RW	**APBFC_ILDOACLK0_RSVD:** Reserved.
9:5	0h RW	**ildoaclk_trimoverride_reg:** Reserved.
4	0b RW	**ildoaclk_trimoverride_reg_sel:** Reserved.
3	0b RW	**ildoaclk_trimoverridesel_reg:** Reserved.
2	0b RW	**ildoaclk_trimoverridesel_reg_sel:** Reserved.
1	0b RW	**ildoaclk_en_reg:** Reserved.
0	0b RW	**ildoaclk_en_reg_sel:** Reserved.

19.7.3 APBFC_ILDOS0—Offset 10h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_ILDOS0: [BAR + 10F800h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

Bits	15:10	9:5	4	3	2	1	0
Default	0 0 0 0 0 0	0 0 0 0 0	0	0	0	0	0
Field	APBFC_ILDOS0_RSVD	ildos_trimoverride_reg	ildos_trimoverride_reg_sel	ildos_trimoverridesel_reg	ildos_trimoverridesel_reg_sel	ildos_en_reg	ildos_en_reg_sel

Bit Range	Default & Access	Description
15:10	0h RW	**APBFC_ILDOS0_RSVD:** Reserved.
9:5	0h RW	**ildos_trimoverride_reg:** Reserved.
4	0b RW	**ildos_trimoverride_reg_sel:** Reserved.
3	0b RW	**ildos_trimoverridesel_reg:** Reserved.
2	0b RW	**ildos_trimoverridesel_reg_sel:** Reserved.
1	0b RW	**ildos_en_reg:** Reserved.
0	0b RW	**ildos_en_reg_sel:** Reserved.

19.7.4 APBFC_IPMA0—Offset 14h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_IPMA0: [BAR + 10F800h] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IPMA_CMN_REFCLK_RCV_EN_REG	IPMA_CMN_REFCLK_RCV_EN_REG_SEL	IPMA_CMN_REFCLK_INT_SEL_REG	IPMA_CMN_REFCLK_INT_SEL_REG_SEL	IPMA_CMN_REFCLK_INT_B_REG	IPMA_CMN_REFCLK_INT_B_REG_SEL	IPMA_CMN_REFCLK_INT_REG	IPMA_CMN_REFCLK_INT_REG_SEL	IPMA_CMN_REFCLK_DISABLE_REG	IPMA_CMN_REFCLK_DISABLE_REG_SEL	IPMA_CMN_REFCLK_ALL_SEL_REG	IPMA_CMN_REFCLK_ALL_SEL_REG_SEL	IPMA_CMN_MACRO_EN_REG	IPMA_CMN_MACRO_EN_REG_SEL	IPMA_CMN_ANA_DISABLE_REG	IPMA_CMN_ANA_DISABLE_REG_SEL

Bit Range	Default & Access	Description
15	0b RW	**IPMA_CMN_REFCLK_RCV_EN_REG:** Reserved.
14	0b RW	**IPMA_CMN_REFCLK_RCV_EN_REG_SEL:** Reserved.
13	0b RW	**IPMA_CMN_REFCLK_INT_SEL_REG:** Reserved.
12	0b RW	**IPMA_CMN_REFCLK_INT_SEL_REG_SEL:** Reserved.
11	0b RW	**IPMA_CMN_REFCLK_INT_B_REG:** Reserved.
10	0b RW	**IPMA_CMN_REFCLK_INT_B_REG_SEL:** Reserved.
9	0b RW	**IPMA_CMN_REFCLK_INT_REG:** Reserved.
8	0b RW	**IPMA_CMN_REFCLK_INT_REG_SEL:** Reserved.
7	0b RW	**IPMA_CMN_REFCLK_DISABLE_REG:** Reserved.
6	0b RW	**IPMA_CMN_REFCLK_DISABLE_REG_SEL:** Reserved.
5	0b RW	**IPMA_CMN_REFCLK_ALL_SEL_REG:** Reserved.
4	0b RW	**IPMA_CMN_REFCLK_ALL_SEL_REG_SEL:** Reserved.
3	0b RW	**IPMA_CMN_MACRO_EN_REG:** Reserved.
2	0b RW	**IPMA_CMN_MACRO_EN_REG_SEL:** Reserved.
1	0b RW	**IPMA_CMN_ANA_DISABLE_REG:** Reserved.

Bit Range	Default & Access	Description
0	0b RW	**IPMA_CMN_ANA_DISABLE_REG_SEL:** Reserved.

19.7.5 APBFC_IPMA1—Offset 18h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_IPMA1: [BAR + 10F800h] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APBFC_IPMA1_RSVD			ipma_cmn_refclk_freqsel_reg						ipma_cmn_refclk_freqsel_reg_sel	ipma_tx_ls_diag_data_reg	ipma_tx_ls_diag_data_reg_sel	ipma_rx_epath_disable_reg	ipma_rx_epath_disable_reg_sel	ipma_ls_diag_sel_reg	ipma_ls_diag_sel_reg_sel

Bit Range	Default & Access	Description
15:13	0h RO	**APBFC_IPMA1_RSVD:** Reserved.
12:7	0h RW	**ipma_cmn_refclk_freqsel_reg:** Reserved.
6	0b RW	**ipma_cmn_refclk_freqsel_reg_sel:** Reserved.
5	0b RW	**ipma_tx_ls_diag_data_reg:** Reserved.
4	0b RW	**ipma_tx_ls_diag_data_reg_sel:** Reserved.
3	0b RW	**ipma_rx_epath_disable_reg:** Reserved.
2	0b RW	**ipma_rx_epath_disable_reg_sel:** Reserved.
1	0b RW	**ipma_ls_diag_sel_reg:** Reserved.
0	0b RW	**ipma_ls_diag_sel_reg_sel:** Reserved.

19.7.6 APBFC_OPMA0—Offset 1Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OPMA0: [BAR + 10F800h] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APBFC_OPMA_RSVD										OPMA_RX_LS_DIAG_DATA_P_REG	OPMA_RX_LS_DIAG_DATA_P_REG_SEL	OPMA_RX_LS_DIAG_DATA_M_REG	OPMA_RX_LS_DIAG_DATA_M_REG_SEL	OPMA_CMN_REFCLK_ACTIVE_REG	OPMA_CMN_REFCLK_ACTIVE_REG_SEL

Bit Range	Default & Access	Description
15:6	0h RW	**APBFC_OPMA_RSVD:** Reserved.
5	0b RW	**OPMA_RX_LS_DIAG_DATA_P_REG:** Reserved.
4	0b RW	**OPMA_RX_LS_DIAG_DATA_P_REG_SEL:** Reserved.
3	0b RW	**OPMA_RX_LS_DIAG_DATA_M_REG:** Reserved.
2	0b RW	**OPMA_RX_LS_DIAG_DATA_M_REG_SEL:** Reserved.
1	0b RW	**OPMA_CMN_REFCLK_ACTIVE_REG:** Reserved.
0	0b RW	**OPMA_CMN_REFCLK_ACTIVE_REG_SEL:** Reserved.

19.7.7 APBFC_IPIPE0—Offset 20h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_IPIPE0: [BAR + 10F800h] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IPIPE_RX_TERM_REG	IPIPE_RX_TERM_REG_SEL	IPIPE_RX_POLARITY_REG	IPIPE_RX_POLARITY_REG_SEL	IPIPE_RX_EQ_TRAINING_REG	IPIPE_RX_EQ_TRAINING_REG_SEL	IPIPE_RESET_B_REG	IPIPE_RESET_B_REG_SEL	IPIPE_POWERDOWN_REG		IPIPE_POWERDOWN_REG_SEL	IPIPE_PHY_MODE_REG		IPIPE_PHY_MODE_REG_SEL	IPIPE_ELASTIC_BUF_MODE_REG	IPIPE_ELASTIC_BUF_MODE_REG_SEL

Bit Range	Default & Access	Description
15	0b RW	**IPIPE_RX_TERM_REG:** Reserved.
14	0b RW	**IPIPE_RX_TERM_REG_SEL:** Reserved.
13	0b RW	**IPIPE_RX_POLARITY_REG:** Reserved.
12	0b RW	**IPIPE_RX_POLARITY_REG_SEL:** Reserved.
11	0b RW	**IPIPE_RX_EQ_TRAINING_REG:** Reserved.
10	0b RW	**IPIPE_RX_EQ_TRAINING_REG_SEL:** Reserved.
9	0b RW	**IPIPE_RESET_B_REG:** Reserved.
8	0b RW	**IPIPE_RESET_B_REG_SEL:** Reserved.
7:6	0h RW	**IPIPE_POWERDOWN_REG:** Reserved.
5	0b RW	**IPIPE_POWERDOWN_REG_SEL:** Reserved.
4:3	0h RW	**IPIPE_PHY_MODE_REG:** Reserved.
2	0b RW	**IPIPE_PHY_MODE_REG_SEL:** Reserved.
1	0b RW	**IPIPE_ELASTIC_BUF_MODE_REG:** Reserved.
0	0b RW	**IPIPE_ELASTIC_BUF_MODE_REG_SEL:** Reserved.

19.7.8 APBFC_IPIPE1A—Offset 24h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_IPIPE1A: [BAR + 10F800h] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APBFC_IPIPE1A_RSVD				IPIPE_TX_DATA_REG_A											IPIPE_TX_DATA_REG_SEL_A

Bit Range	Default & Access	Description
15:12	0h RO	**APBFC_IPIPE1A_RSVD:** Reserved.
11:1	0h RW	**IPIPE_TX_DATA_REG_A:** Reserved.
0	0b RW	**IPIPE_TX_DATA_REG_SEL_A:** Reserved.

19.7.9 APBFC_IPIPE1B—Offset 28h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_IPIPE1B: [BAR + 10F800h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APBFC_IPIPE1B_RSVD				IPIPE_TX_DATA_REG_B											IPIPE_TX_DATA_REG_SEL_B

Bit Range	Default & Access	Description
15:12	0h RO	**APBFC_IPIPE1B_RSVD:** Reserved.
11:1	0h RW	**IPIPE_TX_DATA_REG_B:** Reserved.
0	0b RW	**IPIPE_TX_DATA_REG_SEL_B:** Reserved.

19.7.10 APBFC_IPIPE1C—Offset 2Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_IPIPE1C: [BAR + 10F800h] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:11	Bits 10:1	Bit 0
APBFC_IPIPE1C_RSVD	IPIPE_TX_DATA_REG_C	IPIPE_TX_DATA_REG_SEL_C

Bit Range	Default & Access	Description
15:11	0h RO	**APBFC_IPIPE1C_RSVD:** Reserved.
10:1	0h RW	**IPIPE_TX_DATA_REG_C:** Reserved.
0	0b RW	**IPIPE_TX_DATA_REG_SEL_C:** Reserved.

19.7.11 APBFC_IPIPE2—Offset 30h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_IPIPE2: [BAR + 10F800h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IPIPE_TX_MARGIN_REG					IPIPE_TX_MARGIN_REG_SEL	IPIPE_TX_ELEC_IDLE_REG	IPIPE_TX_ELEC_IDLE_REG_SEL	IPIPE_TX_DEEMPH_REG		IPIPE_TX_DEEMPH_REG_SEL	IPIPE_TX_DATA_K_REG				IPIPE_TX_DATA_K_REG_SEL

Bit Range	Default & Access	Description
15:11	0h RW	**IPIPE_TX_MARGIN_REG:** Reserved.
10	0b RW	**IPIPE_TX_MARGIN_REG_SEL:** Reserved.
9	0b RW	**IPIPE_TX_ELEC_IDLE_REG:** Reserved.
8	0b RW	**IPIPE_TX_ELEC_IDLE_REG_SEL:** Reserved.
7:6	0h RW	**IPIPE_TX_DEEMPH_REG:** Reserved.
5	0b RW	**IPIPE_TX_DEEMPH_REG_SEL:** Reserved.
4:1	0h RW	**IPIPE_TX_DATA_K_REG:** Reserved.
0	0b RW	**IPIPE_TX_DATA_K_REG_SEL:** Reserved.

19.7.12 APBFC_IPIPE3—Offset 34h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_IPIPE3: [BAR + 10F800h] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APBFC_IPIPE3_RSVD										IPIPE_TX_SWING_REG	IPIPE_TX_SWING_REG_SEL	IPIPE_TX_ONES_ZEROS_REG	IPIPE_TX_ONES_ZEROS_REG_SEL	IPIPE_TX_DET_RX_LPBK_REG	IPIPE_TX_DET_RX_LPBK_REG_SEL

Bit Range	Default & Access	Description
15:6	0h RO	**APBFC_IPIPE3_RSVD:** Reserved.
5	0b RW	**IPIPE_TX_SWING_REG:** Reserved.
4	0b RW	**IPIPE_TX_SWING_REG_SEL:** Reserved.
3	0b RW	**IPIPE_TX_ONES_ZEROS_REG:** Reserved.
2	0b RW	**IPIPE_TX_ONES_ZEROS_REG_SEL:** Reserved.
1	0b RW	**IPIPE_TX_DET_RX_LPBK_REG:** Reserved.
0	0b RW	**IPIPE_TX_DET_RX_LPBK_REG_SEL:** Reserved.

19.7.13 APBFC_OPIPE0—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OPIPE0: [BAR + 10F800h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPIPE_RX_DATA_K_REG				OPIPE_RX_DATA_K_REG_SEL	OPIPE_RX_ELEC_IDLE_REG	OPIPE_RX_ELEC_IDLE_REG_SEL	OPIPE_POWER_PRESENT_REG	OPIPE_POWER_PRESENT_REG_SEL	OPIPE_PHY_STATUS_REG	OPIPE_PHY_STATUS_REG_SEL	OPIPE_DATA_BUS_WIDTH_REG		OPIPE_DATA_BUS_WIDTH_REG_SEL	OPIPE_CLK_REG	OPIPE_CLK_REG_SEL

Bit Range	Default & Access	Description
15:12	0h RW	**OPIPE_RX_DATA_K_REG:** Reserved.
11	0b RW	**OPIPE_RX_DATA_K_REG_SEL:** Reserved.
10	0b RW	**OPIPE_RX_ELEC_IDLE_REG:** Reserved.
9	0b RW	**OPIPE_RX_ELEC_IDLE_REG_SEL:** Reserved.
8	0b RW	**OPIPE_POWER_PRESENT_REG:** Reserved.
7	0b RW	**OPIPE_POWER_PRESENT_REG_SEL:** Reserved.
6	0b RW	**OPIPE_PHY_STATUS_REG:** Reserved.
5	0b RW	**OPIPE_PHY_STATUS_REG_SEL:** Reserved.
4:3	0h RW	**OPIPE_DATA_BUS_WIDTH_REG:** Reserved.
2	0b RW	**OPIPE_DATA_BUS_WIDTH_REG_SEL:** Reserved.
1	0b RW	**OPIPE_CLK_REG:** Reserved.
0	0b RW	**OPIPE_CLK_REG_SEL:** Reserved.

19.7.14 APBFC_OPIPE1A—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OPIPE1A: [BAR + 10F800h] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15:12	11:1	0
APBFC_OPIPE1A_REG_	OPIPE_RX_DATA_REG_A	OPIPE_RX_DATA_REG_A_SEL

Bit Range	Default & Access	Description
15:12	0h RW	**APBFC_OPIPE1A_REG_:** Reserved.
11:1	0h RW	**OPIPE_RX_DATA_REG_A:** Reserved.
0	0b RW	**OPIPE_RX_DATA_REG_A_SEL:** Reserved.

19.7.15 APBFC_OPIPE1B—Offset 40h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OPIPE1B: [BAR + 10F800h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15:12	11:1	0
APBFC_OPIPE1B_RSVD	OPIPE_RX_DATA_REG_B	OPIPE_RX_DATA_REG_B_SEL

Bit Range	Default & Access	Description
15:12	0h RO	**APBFC_OPIPE1B_RSVD:** Reserved.
11:1	0h RW	**OPIPE_RX_DATA_REG_B:** Reserved.

Bit Range	Default & Access	Description
0	0b RW	**OPIPE_RX_DATA_REG_B_SEL:** Reserved.

19.7.16 APBFC_OPIPE1C—Offset 44h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OPIPE1C: [BAR + 10F800h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APBFC_OPIPE1C_RSVD					OPIPE_RX_DATA_REG_C										OPIPE_RX_DATA_REG_C_SEL

Bit Range	Default & Access	Description
15:11	0h RO	**APBFC_OPIPE1C_RSVD:** Reserved.
10:1	0h RW	**OPIPE_RX_DATA_REG_C:** Reserved.
0	0b RW	**OPIPE_RX_DATA_REG_C_SEL:** Reserved.

19.7.17 APBFC_OPIPE2—Offset 48h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OPIPE2: [BAR + 10F800h] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
APBFC_OPIPE2_RSVD										OPIPE_RX_VALID_REG	OPIPE_RX_VALID_REG_SEL	OPIPE_RX_STATUS_REG			OPIPE_RX_STATUS_REG_SEL

Bit Range	Default & Access	Description
15:6	0h RO	**APBFC_OPIPE2_RSVD:** Reserved.
5	0b RW	**OPIPE_RX_VALID_REG:** Reserved.
4	0b RW	**OPIPE_RX_VALID_REG_SEL:** Reserved.
3:1	0h RW	**OPIPE_RX_STATUS_REG:** Reserved.
0	0b RW	**OPIPE_RX_STATUS_REG_SEL:** Reserved.

19.7.18 APBFC_OTG3_MISC0—Offset 4Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OTG3_MISC0: [BAR + 10F800h] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 000Bh

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
xm_rid_flis				xm_bmisc_info_flis				xm_bid_flis				pme_en_flis	bigendian_gs_flis	bus_clken_gm_flis	bus_clken_gs_flis

Bit Range	Default & Access	Description
15:12	0b RW	**xm_rid_flis:** Reserved.
11:8	0b RW	**xm_bmisc_info_flis:** Reserved.

Bit Range	Default & Access	Description
7:4	0b RW	**xm_bid_flis:** Reserved.
3	1b RW	**pme_en_flis:** Reserved.
2	0b RW	**bigendian_gs_flis:** Reserved.
1	1b RW	**bus_clken_gm_flis:** Reserved.
0	1b RW	**bus_clken_gs_flis:** Reserved.

19.7.19 APBFC_OTG3_MISC1—Offset 50h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OTG3_MISC1: [BAR + 10F800h] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

gp_in_flis

Bit Range	Default & Access	Description
15:0	0b RW	**gp_in_flis:** Reserved.

19.7.20 APBFC_OTG3_MISC2—Offset 54h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OTG3_MISC2: [BAR + 10F800h] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 1100h

Bits	15:12	11:8	7:6	5:4	3:0
Default	0 0 0 1	0 0 0 1	0 0	0 0	0 0 0 0
Field	host_num_u3_port_flis	host_num_u2_port_flis	hub_port_perm_attach_flis	APBFC_OTG3_MISC2_RSVD	xm_rmisc_info_flis

Bit Range	Default & Access	Description
15:12	0001b RW	**host_num_u3_port_flis:** Reserved.
11:8	0001b RW	**host_num_u2_port_flis:** Reserved.
7:6	0b RW	**hub_port_perm_attach_flis:** Reserved.
5:4	00b RO	**APBFC_OTG3_MISC2_RSVD:** Reserved.
3:0	0b RW	**xm_rmisc_info_flis:** Reserved.

19.7.21 APBFC_OTG3_MISC3—Offset 58h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_OTG3_MISC3: [BAR + 10F800h] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 7008h

Bits	15	14	13	12:7	6	5	4	3	2	1	0
Default	0	1	1	1 0 0 0 0 0	0	0	0	1	0	0	0
Field	APBFC_OTG3_MISC3_RSVD	xhc_bme_flis	xhci_revision_flis	fladj_30mhz_reg_flis	host_legacy_smi_bar_wr_flis	host_legacy_smi_pci_cmd_reg_wr_flis	host_msi_enable_flis	host_port_power_control_present_flis	host_u3_port_disable_flis	host_u2_port_disable_flis	xm_csysreq_flis

Bit Range	Default & Access	Description
15	0b RO	**APBFC_OTG3_MISC3_RSVD:** Reserved.
14	1b RW	**xhc_bme_flis:** Reserved.
13	1b RW	**xhci_revision_flis:** Reserved.
12:7	100000b RW	**fladj_30mhz_reg_flis:** Reserved.
6	0b RW	**host_legacy_smi_bar_wr_flis:** Reserved.
5	0b RW	**host_legacy_smi_pci_cmd_reg_wr_flis:** Reserved.
4	0b RW	**host_msi_enable_flis:** Reserved.
3	1b RW	**host_port_power_control_present_flis:** Reserved.
2	0b RW	**host_u3_port_disable_flis:** Reserved.
1	0b RW	**host_u2_port_disable_flis:** Reserved.
0	0b RW	**xm_csysreq_flis:** Reserved.

19.7.22 APBFC_U3PMU_CFG0_REG—Offset 5Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_U3PMU_CFG0_REG: [BAR + 10F800h] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

p3p_u3pmu_cfg0_flis

Bit Range	Default & Access	Description
15:0	0h RW	**p3p_u3pmu_cfg0_flis:** Reserved.

19.7.23 APBFC_U3PMU_CFG1_REG—Offset 60h

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

APBFC_U3PMU_CFG1_REG: [BAR + 10F800h] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:22, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
p3p_u3pmu_cfg1_flis															

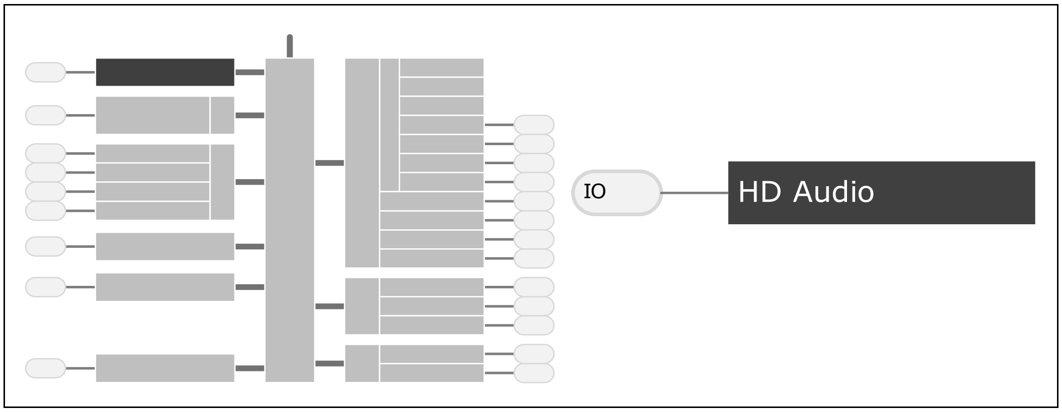
Bit Range	Default & Access	Description
15:0	0h RW	**p3p_u3pmu_cfg1_flis:** Reserved.

20 Intel® High Definition Audio

The Intel® High Definition Audio (Intel® HD Audio) is an architecture and infrastructure to support high-quality audio implementations for PCs.

Note: The High Definition Audio interface is multiplexed on the same balls as LPE_I2S[1:0].

Note: When High Definition Audio is active, the LPE Audio functionality is disabled.



The Intel® High Definition Audio (Intel® HD Audio) controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and internal/external CODECs. The controller communicates with the internal/external CODECs over the Intel® HD Audio serial link.The output DMA engines move digital data from system memory to a D-A converter in a CODEC. The SoC implements a single Serial Data Output (SDO) signal that is connected to the external CODECs. The input DMA engines move digital data from the A-D converter in the CODEC to system memory. The platform supports up to two external CODECs by implementing two Serial Data Input (SDI) signals, each being dedicated to a single CODEC.

Audio software renders outbound, and processes inbound data to/from buffers in memory. The location of the individual buffers is described by a Buffer Descriptor List that is fetched and processed by the audio controller. The data in the buffers is arranged in a pre-defined format. The output DMA engines fetch the digital data from memory and reformat it based on the programmed sample rate, bits/sample and number of channels. The data from the output DMA engines is then combined and serially sent to the CODEC(s) over the Intel® HD Audio link. The input DMA engines receive data from the CODEC(s) over the Intel® HD Audio link and format the data based on the programmable attributes for that stream. The data is then written to memory in the predefined format for software to process. Each DMA engine moves one "stream" of data. A single CODEC can accept or generate multiple "streams" of data, one for each A-D or D-A converter in the CODEC. Multiple CODECs can accept the same output "stream" processed by a single DMA engine.

Codec commands and responses are also transported to and from the CODEC via DMA engines. The DMA engine dedicated to transporting commands from the Command Output Ring Buffer (CORB) in memory to the CODEC(s) is called the CORB engine. The DMA engine dedicated to transporting responses from the CODEC(s) to the Response Input Ring Buffer in memory is called the RIRB engine. Every command sent to a CODEC yields a response from that CODEC. Some commands are "broadcast" type commands in which case a response will be generated from each CODEC. A CODEC may also be programmed to generate unsolicited responses, which the RIRB engine also processes. The platform also supports Programmed IO-based Immediate Command/Response transport mechanism that can be used by BIOS prior to memory initialization.

20.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 223. Signals

Signal Name	Direction Plat. Power	Description
HDA_RST#	O VAUD	**Intel HD Audio Reset:** Master H/W reset to external Codecs
HDA_SYNC	O VAUD	**Intel HD Audio Sync:** 48 kHz fixed rate
HDA_CLK	O VAUD	**Intel HD Audio Bit Clock (Output):** 24 MHz serial data clock generated by the Intel HD Audio controller
HDA_SDO	O VAUD	**Intel HD Audio Data Out:** Serial TDM data output to the Codec(s). The serial output is double-pumped for a bit rate of 48 Mb/s
HDA_SDI[1:0]	I/O VAUD	**Intel HD Audio Serial Data In[1:0]:** Serial TDM data input from the CODEC(s). The serial input is single-pumped for a bit rate of 24 Mb/s.
HDA_LPE_RCOMP	O	Impedance/ current Compensation Output.

The signals in the table above are all muxed and maybe used by other functions.

20.2 Features

The Intel® HD Audio Controller supports the following features:

- Supports MSI and legacy interrupt delivery
- Support for ACPI D3 and D0 Device States
- Supports up to:
  - 6 streams (three input, three output)
  - 16 channels per stream
  - 32 bits/sample
  - 192 kHz sample rate
- 24 MHz HDA_CLK supports
  - SDO double pumped at 48 Mb/s
  - SDI single pumped at 24 Mb/s
- Supports 1.5V mode only
- Supports optional Immediate Command/Response mechanism

20.3 References

High Definition Audio Specification, Revision 1.0a

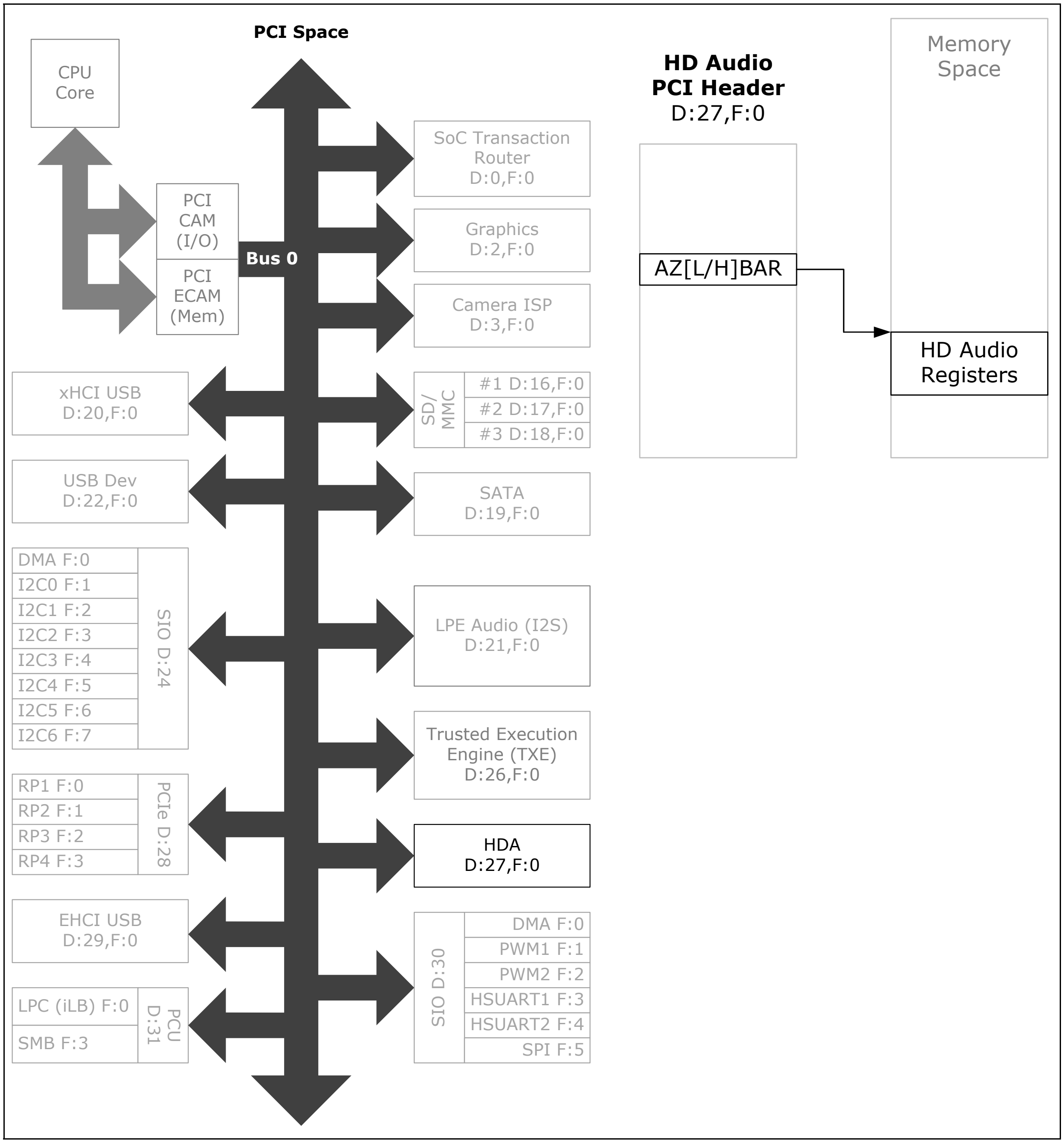
- http://www.intel.com/content/www/us/en/standards/high-definition-audio-specification.html

20.4 Register Map

See Chapters 3 and 4 for additional information.

Note: PCI mode is supported, but not PCIe mode. Must set TM1.HAPD bit to 1b for PCI mode.

Figure 105. Intel® HD Audio Register Map



20.5 HD Audio PCI Configuration Registers

Table 224. Summary of HD Audio PCI Configuration Registers—0/27/0

Offset	Size	Register ID—Description	Default Value
0h	2	"VID—Offset 0h" on page 2680	8086h
2h	2	"DID—Offset 2h" on page 2680	0F04h
4h	2	"CMD—Offset 4h" on page 2681	0000h
6h	2	"STS—Offset 6h" on page 2682	0010h
8h	1	"RID—Offset 8h" on page 2683	00h
9h	1	"PI—Offset 9h" on page 2683	00h
Ah	1	"SCC—Offset Ah" on page 2683	03h
Bh	1	"BCC—Offset Bh" on page 2684	04h
Ch	1	"CLS—Offset Ch" on page 2684	00h
Dh	1	"LT—Offset Dh" on page 2685	00h
Eh	1	"HTYPE—Offset Eh" on page 2685	00h
Fh	1	"BIST—Offset Fh" on page 2685	00h
10h	4	"AZLBAR—Offset 10h" on page 2686	00000004h
14h	4	"AZUBAR—Offset 14h" on page 2686	00000000h
2Ch	2	"SVID—Offset 2Ch" on page 2687	0000h
2Eh	2	"SID—Offset 2Eh" on page 2687	0000h
34h	1	"CAPPTR—Offset 34h" on page 2687	50h
3Ch	1	"INTLN—Offset 3Ch" on page 2688	00h
3Dh	1	"INTPN—Offset 3Dh" on page 2688	01h
40h	1	"AZCTL—Offset 40h" on page 2689	01h
42h	1	"IOBC—Offset 42h" on page 2689	00h
43h	1	"TM1—Offset 43h" on page 2690	57h
4Ch	1	"DCKCTL—Offset 4Ch" on page 2690	00h
4Dh	1	"DCKSTS—Offset 4Dh" on page 2691	80h
50h	2	"PID—Offset 50h" on page 2691	6001h
52h	2	"PC—Offset 52h" on page 2692	C842h
54h	4	"PCS—Offset 54h" on page 2693	00000000h
60h	2	"MID—Offset 60h" on page 2693	7005h
62h	2	"MMC—Offset 62h" on page 2694	0080h
64h	4	"MMLA—Offset 64h" on page 2694	00000000h
68h	4	"MMUA—Offset 68h" on page 2695	00000000h
6Ch	2	"MMD—Offset 6Ch" on page 2695	0000h
70h	2	"PXID—Offset 70h" on page 2696	0010h
72h	2	"PXC—Offset 72h" on page 2696	0091h
74h	4	"DEVCAP—Offset 74h" on page 2697	10000000h
78h	2	"DEVCAP—Offset 74h" on page 2697	0800h

Table 224. Summary of HD Audio PCI Configuration Registers—0/27/0 (Continued)

Offset	Size	Register ID—Description	Default Value
7Ah	2	"DEVS—Offset 7Ah" on page 2698	0010h
F8h	4	"MANID—Offset F8h" on page 2699	00000F00h
100h	4	"VCCAP—Offset 100h" on page 2700	13010002h
104h	4	"PVCCAP1—Offset 104h" on page 2700	00000001h
108h	4	"PVCCAP2—Offset 108h" on page 2701	00000000h
10Ch	2	"PVCCTL—Offset 10Ch" on page 2701	0000h
10Eh	2	"PVCSTS—Offset 10Eh" on page 2702	0000h
110h	4	"VC0CAP—Offset 110h" on page 2702	00000000h
114h	4	"VC0CTL—Offset 114h" on page 2703	800000FFh
11Ah	2	"VC0STS—Offset 11Ah" on page 2704	0000h
11Ch	4	"VCICAP—Offset 11Ch" on page 2704	00000000h
120h	4	"VCICTL—Offset 120h" on page 2705	00000000h
126h	2	"VCISTS—Offset 126h" on page 2706	0000h
130h	4	"RCCAP—Offset 130h" on page 2706	00010005h
134h	4	"ESD—Offset 134h" on page 2707	0F000100h
140h	4	"L1DESC—Offset 140h" on page 2708	00000001h
148h	4	"L1LADD—Offset 148h" on page 2708	00000000h
14Ch	4	"L1UADD—Offset 14Ch" on page 2709	00000000h

20.5.1 VID—Offset 0h

Vendor ID

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

VID: [B:0, D:27, F:0] + 0h

Default: 8086h

15			12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
VID															

Bit Range	Default & Access	Description
15:0	8086h RO	**VID:** Vendor ID

20.5.2 DID—Offset 2h

Device ID

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

DID: [B:0, D:27, F:0] + 2h

Default: 0F04h

15			12				8				4				0
0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0
DID															

Bit Range	Default & Access	Description
15:0	0f04h RO	**DID:** Device ID: This field identifies the particular device. DID[15:7] indicates SoC, DID[6:1]=6'b000010 indicates HDAudio device, DID[0] comes from fuse indicates HDAudio SKU

20.5.3 CMD—Offset 4h

Command

Access Method

Type: PCI Configuration Register (Size: 16 bits)

CMD: [B:0, D:27, F:0] + 4h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved					ID	FBE	SEN	WCC	PER	VGS	MWI	SCE	BME	MSE	IOS

Bit Range	Default & Access	Description
15:11	0000h RO	**Reserved:** Reserved
10	0h RW	**ID:** Interrupt Disable
9	0h RO	**FBE:** Fast back to back enable. Not implemented.
8	0h RW	**SEN:** SERR enable
7	0h RO	**WCC:** Wait Cycle Control. Not implemented.
6	0h RW	**PER:** Parity error response. Not implemented.
5	0h RO	**VGS:** VGA Pallete Snoop. Not implemented.
4	0h RO	**MWI:** Memory write and invalidate enable. Not implemented.
3	0h RO	**SCE:** Special cycle enable. Not implemented.
2	0h RW	**BME:** Bus master enable

Bit Range	Default & Access	Description
1	0h RW	**MSE:** Memory space enable
0	0h RO	**IOS:** I/O space enabled. Not implemented.

20.5.4 STS—Offset 6h

Status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

STS: [B:0, D:27, F:0] + 6h

Default: 0010h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
DPE	SERRS	RMA	RTA	STA	DEVT		MDPE	FBC	Reserved	C66	CLIST	IS	Reserved_1		

Bit Range	Default & Access	Description
15	0h RO	**DPE:** Detected parity error. Not implemented.
14	0h RO	**SERRS:** SERR Status
13	0h WOC	**RMA:** Recieved master abort
12	0h RO	**RTA:** Recieved target abort. Not implemented.
11	0h RO	**STA:** Signaled target abort. Not implemented.
10:9	0h RO	**DEVT:** DEVSEL timing status. Not implemented.
8	0h RO	**MDPE:** Master data parity error. Not implemented.
7	0h RO	**FBC:** Fast back to back capable. Not implemented.
6	0h RO	**Reserved:** Reserved
5	0h RO	**C66:** 66MHz capable. Not implemented.
4	1h RO	**CLIST:** Capabilities list exist
3	0h RO	**IS:** Interrupt Status. Shows legacy interrupt signal status. Doesn't apply to MSI.

Bit Range	Default & Access	Description
2:0	0h RO	**Reserved_1:** reserved

20.5.5 RID—Offset 8h

Revision ID

Access Method

Type: PCI Configuration Register (Size: 8 bits)

RID: [B:0, D:27, F:0] + 8h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Description
7:0	0h RO	**RID:** Revision ID

20.5.6 PI—Offset 9h

Programming Interface

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PI: [B:0, D:27, F:0] + 9h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PI							

Bit Range	Default & Access	Description
7:0	0h RO	**PI:** Programming Interface

20.5.7 SCC—Offset Ah

Sub Class Code

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SCC: [B:0, D:27, F:0] + Ah

Default: 03h

7			4				0
0	0	0	0	0	0	1	1
SCC							

Bit Range	Default & Access	Description
7:0	03h RO	**SCC:** Sub Class Code

20.5.8 BCC—Offset Bh

Base Class Code

Access Method

Type: PCI Configuration Register (Size: 8 bits) **BCC:** [B:0, D:27, F:0] + Bh

Default: 04h

7			4				0
0	0	0	0	0	1	0	0
BCC							

Bit Range	Default & Access	Description
7:0	04h RO	**BCC:** Base Class Code

20.5.9 CLS—Offset Ch

Cache line size

Access Method

Type: PCI Configuration Register (Size: 8 bits) **CLS:** [B:0, D:27, F:0] + Ch

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CLS							

Bit Range	Default & Access	Description
7:0	0h RW	**CLS:** Cache line size

20.5.10 LT—Offset Dh

Latency timer

Access Method

Type: PCI Configuration Register (Size: 8 bits)

LT: [B:0, D:27, F:0] + Dh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
LT							

Bit Range	Default & Access	Description
7:0	0h RO	**LT:** Latency timer

20.5.11 HTYPE—Offset Eh

Header type

Access Method

Type: PCI Configuration Register (Size: 8 bits)

HTYPE: [B:0, D:27, F:0] + Eh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HTYPE							

Bit Range	Default & Access	Description
7:0	0h RO	**HTYPE:** Header type

20.5.12 BIST—Offset Fh

Built in self test. Not implemented.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

BIST: [B:0, D:27, F:0] + Fh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
BIST							

Bit Range	Default & Access	Description
7:0	0h RO	**BIST:** Built in self test. Not implemented.

20.5.13 AZLBAR—Offset 10h

Lower Base Address (BAR)

Access Method

Type: PCI Configuration Register (Size: 32 bits)

AZLBAR: [B:0, D:27, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
LBA (31:14)																		Reserved (13:4)										PREF	ADDRNG		SPTYP

Bit Range	Default & Access	Description
31:14	0h RW	**LBA:** Lower Base Address
13:4	0h RO	**Reserved:** Reserved
3	0h RO	**PREF:** Prefetchable
2:1	2h RO	**ADDRNG:** Address Range
0	0h RO	**SPTYP:** Space Type (Memory)

20.5.14 AZUBAR—Offset 14h

Upper Base Address (BAR)

Access Method

Type: PCI Configuration Register (Size: 32 bits)

AZUBAR: [B:0, D:27, F:0] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
UBA (31:0)																															

Bit Range	Default & Access	Description
31:0	0h RW	**UBA:** Upper Base Address

20.5.15 SVID—Offset 2Ch

subsystem vendor ID

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

SVID: [B:0, D:27, F:0] + 2Ch

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SVID															

Bit Range	Default & Access	Description
15:0	0h RWO	**SVID:** subsystem vendor ID. This field is written by BIOS. No hardware action is taken according to this register

20.5.16 SID—Offset 2Eh

subsystem ID

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

SID: [B:0, D:27, F:0] + 2Eh

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SID															

Bit Range	Default & Access	Description
15:0	0h RWO	**SID:** subsystem ID. This field is written by BIOS. No hardware action is taken according to this register

20.5.17 CAPPTR—Offset 34h

Capabilities pointer

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

CAPPTR: [B:0, D:27, F:0] + 34h

Default: 50h

7			4				0
0	1	0	1	0	0	0	0
CAPPTR							

Bit Range	Default & Access	Description
7:0	50h RO	**CAPPTR:** Capabilities pointer

20.5.18 INTLN—Offset 3Ch

Interrupt Line

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

INTLN: [B:0, D:27, F:0] + 3Ch

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
INTLN							

Bit Range	Default & Access	Description
7:0	0h RW	**INTLN:** Interrupt Line

20.5.19 INTPN—Offset 3Dh

Interrupt Pin

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

INTPN: [B:0, D:27, F:0] + 3Dh

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
Reserved				INTPN			

Bit Range	Default & Access	Description
7:4	0h RO	**Reserved:** Reserved
3:0	1h RO	**IP (INTPN):** Interrupt Pin

20.5.20 AZCTL—Offset 40h

Azalia controller

Access Method

Type: PCI Configuration Register (Size: 8 bits)

AZCTL: [B:0, D:27, F:0] + 40h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
Reserved							AZ_AC97

Bit Range	Default & Access	Description
7:1	0h RO	**Reserved:** Reserved
0	1h RO	**AZ_AC97# (AZ_AC97):** This register is always 1'b1 indicating Azalia

20.5.21 IOBC—Offset 42h

IO Buffer control

Access Method

Type: PCI Configuration Register (Size: 8 bits)

IOBC: [B:0, D:27, F:0] + 42h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved_0		ASRC		Reserved_1	AVDDIS	MVSEL	VMODE

Bit Range	Default & Access	Description
7:6	0h RO	**Reserved_0:** Reserved
5:4	0h RO	**ASRC:** Audio buffer slew rate control
3	0h RO	**Reserved_1:** Reserved
2	0h RO	**AVDDIS:** Automatic voltage detector disable
1	0h RO	**MVSEL:** Manual voltage select

Bit Range	Default & Access	Description
0	0h RO	**VMODE:** voltage mode

20.5.22 TM1—Offset 43h

Test mode 1

Access Method

Type: PCI Configuration Register (Size: 8 bits)

TM1: [B:0, D:27, F:0] + 43h

Default: 57h

7			4				0
0	1	0	1	0	1	1	1
RSVD	RSVD	RSVD	RSVD	HAPD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Description
7	0h RO	**Reserved (RSVD):** Reserved.
6	1h RO	**Reserved (RSVD):** Reserved.
5	0h RO	**Reserved (RSVD):** Reserved.
4	1h RO	**Reserved (RSVD):** Reserved.
3	0h RWO	**HAPD:** HD Audio PCI/PCIe# device
2	1h RO	**Reserved (RSVD):** Reserved.
1	1h RO	**Reserved (RSVD):** Reserved.
0	1h RO	**Reserved (RSVD):** Reserved.

20.5.23 DCKCTL—Offset 4Ch

Docking control

Access Method

Type: PCI Configuration Register (Size: 8 bits)

DCKCTL: [B:0, D:27, F:0] + 4Ch

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							DA

Bit Range	Default & Access	Description
7:1	0h RO	**Reserved:** reserved
0	0h RW	**DA:** Dock attach

20.5.24 DCKSTS—Offset 4Dh

Docking status

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

DCKSTS: [B:0, D:27, F:0] + 4Dh

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
DS	Reserved						DM

Bit Range	Default & Access	Description
7	1h RWO	**DS:** Docking support
6:1	0h RO	**Reserved:** reserved
0	0h RO	**DM:** Dock Mated

20.5.25 PID—Offset 50h

Power Management Capability ID

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

PID: [B:0, D:27, F:0] + 50h

Default: 6001h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
NEXTCAP								CAPID							

Bit Range	Default & Access	Description
15:8	60h RO	**NEXTCAP:** Next Capability.
7:0	01h RO	**CAPID:** Capability ID.

20.5.26 PC—Offset 52h

Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PC: [B:0, D:27, F:0] + 52h

Default: C842h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0
PMES					D2S	D1S	AC			DSI	Reserved	PMEC	VS		

Bit Range	Default & Access	Description
15:11	19h RO	**PMES:** PME_Support (PMES): Indicates PME# can be generated from D3 and D0 states.
10	0h RO	**D2S:** D2 state. Not supported.
9	0h RO	**D1S:** D1 state. Not supported.
8:6	1h RO	**AC:** Aux Current
5	0h RO	**DSI:** Device specific initialization
4	0h RO	**Reserved:** Reserved
3	0h RO	**PMEC:** PME Clock. Does not apply.
2:0	2h RO	**VS:** Version (VS): Indicates support for Revision 1.1 of the PCI Power Management Specification.

20.5.27 PCS—Offset 54h

Power Management control and status

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCS: [B:0, D:27, F:0] + 54h

Default: 00000000h

Bits	31:24	23	22	21:16	15	14:9	8	7:2	1:0
Default	0 0 0 0 0 0 0 0	0	0	0 0 0 0 0 0	0	0 0 0 0 0 0	0	0 0 0 0 0 0	0 0
Field	DT	BPCCE	B23	Reserved_0	PMES	Reserved_1	PMEE	Reserved_2	PS

Bit Range	Default & Access	Description
31:24	0h RO	**DT:** Data. Does not apply.
23	0h RO	**BPCCE:** Bus power control enable. Does not apply.
22	0h RO	**B23:** Does not apply.
21:16	0h RO	**Reserved_0:** Reserved
15	0h RW1C	**PMES:** PME Status (PMES): This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME_En bit. This bit resides in the Suspend well. This bit is in the Suspend well and cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	0h RO	**Reserved_1:** Reserved
8	0h RW	**PMEE:** PME enable
7:2	0h RO	**Reserved_2:** reserved
1:0	0h RW	**PS:** Power State (PS): This field is used both to determine the current power state of the Intel HD Audio controller and to set a new power state. The values are: 00 D0 state 11 D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio controllers configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

20.5.28 MID—Offset 60h

MSI Capability ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MID: [B:0, D:27, F:0] + 60h

Default: 7005h

15			12				8				4				0
0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1
NEXTCAP								CAPID							

Bit Range	Default & Access	Description
15:8	70h RO	**NEXTCAP:** Next Capability. The value of this field depends on the TM1.HAPD bit. When TM1.HAPD is 0, this field has a value of 70h where it points to the PCI Express capability structure. When TM1.HAPD bit is 1, this field has a value of 00h to indicate that this is the last capability structure in the list.
7:0	05h RO	**CAPID:** Capability ID.

20.5.29 MMC—Offset 62h

MSI Message Control

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MMC: [B:0, D:27, F:0] + 62h

Default: 0080h

15			12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Reserved								ADD64	MME			MMC			ME

Bit Range	Default & Access	Description
15:8	0h RO	**Reserved:** Reserved
7	1h RO	**ADD64:** 64-bit Address support
6:4	0h RO	**MME:** Multiple Message Enable
3:1	0h RO	**MMC:** Multiple Message Capable
0	0h RW	**ME:** MSI Enable (ME): If set to 1 an MSI will be generated instead of an INTx# signal. If set to 0, an MSI may not be generated.

20.5.30 MMLA—Offset 64h

MSI Lower Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MMLA: [B:0, D:27, F:0] + 64h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MLA																														Reserved	

Bit Range	Default & Access	Description
31:2	0h RW	**MLA:** MSI Lower Address
1:0	0h RO	**Reserved:** Reserved

20.5.31 MMUA—Offset 68h

MSI Upper Address

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

MMUA: [B:0, D:27, F:0] + 68h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MUA																															

Bit Range	Default & Access	Description
31:0	0h RW	**MUA:** MSI Upper Address

20.5.32 MMD—Offset 6Ch

MSI Data

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

MMD: [B:0, D:27, F:0] + 6Ch

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MD															

Bit Range	Default & Access	Description
15:0	0h RW	**MD:** MSI Data

20.5.33 PXID—Offset 70h

PCIe Capability ID

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

PXID: [B:0, D:27, F:0] + 70h

Default: 0010h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
NEXTCAP								CAPID							

Bit Range	Default & Access	Description
15:8	00h RO	**NEXTCAP:** Next Capability.
7:0	10h RO	**CAPID:** Capability ID.

20.5.34 PXC—Offset 72h

PCI express capabilities

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

PXC: [B:0, D:27, F:0] + 72h

Default: 0091h

15			12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1
Reserved		IMN					SI	DPT				CV			

Bit Range	Default & Access	Description
15:14	0h RO	**Reserved:** reserved
13:9	0h RO	**IMN:** Interrupt message number
8	0h RO	**SI:** Slot implemented
7:4	9h RO	**DPT:** Device/port type
3:0	1h RO	**CV:** Capability version

20.5.35 DEVCAP—Offset 74h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVCAP: [B:0, D:27, F:0] + 74h

Default: 10000000h

31			28				24				20				16				12				8				4				0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED	RSVD	SPLS	SPLV	RESERVED1	PIP	AIP	ABP	L1CAP	L0SCAP	ETCAP	PFCAP	MPCAP

Bit Range	Default & Access	Description
31:29	0h RO	**RESERVED:** reserved
28	1h RO	**Reserved (RSVD):** Reserved.
27:26	0h RO	**SPLS:** Captured Slot Power Limit Scale
25:18	0h RO	**SPLV:** Captured Slot Power Limit Value
17:15	0h RO	**RESERVED1:** reserved
14	0h RO	**PIP:** Power Indicator Present
13	0h RO	**AIP:** Attention Indicator Present
12	0h RO	**ABP:** Attention Button Present
11:9	0h RWO	**L1CAP:** Endpoint L1 Acceptable Latency
8:6	0h RWO	**L0SCAP:** Endpoint L0s Acceptable Latency
5	0h RO	**ETCAP:** Extended Tag Field Support
4:3	0h RO	**PFCAP:** Phantom Functions Supported
2:0	0h RO	**MPCAP:** Max Payload Size Supported

20.5.36 DEVC—Offset 78h

Device control

Access Method

Type: PCI Configuration Register (Size: 16 bits)

DEVC: [B:0, D:27, F:0] + 78h

Default: 0800h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	MRRS			NSNPEN	AUXPEN	PEEN	ETEN	MAXPAY			ROEN	URREN	FEREN	NFEREN	CEREN

Bit Range	Default & Access	Description
15	0h RO	**Reserved (RSVD):** Reserved.
14:12	0h RO	**MRRS:** Max read request size
11	1h RW	**NSNPEN:** Enable No Snoop
10	0h RO	**AUXPEN:** Auxiliary Power PM Enable
9	0h RO	**PEEN:** Phantom Functions Enable
8	0h RO	**ETEN:** Extended Tag Field Enable
7:5	0h RO	**MAXPAY:** Max Payload Size
4	0h RO	**ROEN:** Enable Relaxed Ordering
3	0h RW	**URREN:** Unsupported Request Reporting Enable
2	0h RW	**FEREN:** Fatal Error Reporting Enable
1	0h RW	**NFEREN:** Non-Fatal Error Reporting Enable
0	0h RW	**CEREN:** Correctable Error Reporting Enable

20.5.37 DEVS—Offset 7Ah

Device status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

DEVS: [B:0, D:27, F:0] + 7Ah

Default: 0010h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
RESERVED										TXP	AUXDET	URDET	FEDET	NFEDET	CEDET

Bit Range	Default & Access	Description
15:6	0h RO	**RESERVED:** RESERVED
5	0h RO	**TXP:** Transactions Pending
4	1h RO	**AUXDET:** AUX Power Detected
3	0h RO	**URDET:** Unsupported Request Detected
2	0h RO	**FEDET:** Fatal Error Detected
1	0h RO	**NFEDET:** Non-Fatal Error Detected
0	0h RO	**CEDET:** Correctable Error Detected

20.5.38 MANID—Offset F8h

Manufacturer ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:27, F:0] + F8h

Default: 00000F00h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
RESERVED				DPID				SID								MNFR								PPID							

Bit Range	Default & Access	Description
31:28	0h RO	**RESERVED:** RESERVED
27:24	0h RO	**DPID:** Dot Portion Process ID
23:16	0h RO	**SID:** Stepping ID
15:8	0Fh RO	**MNFR:** Manufacturer
7:0	0h RO	**PPID:** Process Portion Process ID

20.5.39 VCCAP—Offset 100h

Virtual Channel Cap Header

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VCCAP: [B:0, D:27, F:0] + 100h

Default: 13010002h

31:20	19:16	15:0
0001 0011 0000	0001	0000 0000 0000 0010
NXTCAP	CV	PCIEECID

Bit Range	Default & Access	Description
31:20	130h RWO	**NXTCAP:** Next Capability Offset (NXTCAP): Points to the next capability header, which is the Root Complex Link Declaration Enhanced Capability Header. This register is RWO to support removing the Root Complex Topology Capability from the PCI Express Extended Capability List. For systems which support the Root Complex Topology Capability Structure, boot BIOS should write a 130h to this register, otherwise boot BIOS should write a 000h to this register.
19:16	1h RWO	**CV:** Capability Version (CV): This register is RWO to support removing the PCI Express Extended Capabilities from Azalia. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 1h to this register, otherwise boot BIOS should write a 0h to this register.
15:0	2h RWO	**PCIEECID:** PCI Express Extended Capability ID (PCIEECID): This register is RWO to support removing the PCI Express Extended Capabilities from Azalia. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 0002h to this register, otherwise boot BIOS should write a 0000h to this register.

20.5.40 PVCCAP1—Offset 104h

Port VC Capability

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PVCCAP1: [B:0, D:27, F:0] + 104h

Default: 00000001h

31:12	11:10	9:8	7	6:4	3	2:0
0000 0000 0000 0000 0000	00	00	0	000	0	001
RESERVED	PARBTBLES	RC	RESERVED1	LPVCCNT	RESERVED2	VCCNT

Bit Range	Default & Access	Description
31:12	0h RO	**RESERVED:** RESERVED

Bit Range	Default & Access	Description
11:10	0h RO	**PARBTBLES:** Port Arbitration Table Entry Size
9:8	0h RO	**RC:** Reference Clock
7	0h RO	**RESERVED1:** RESERVED
6:4	0h RO	**LPVCCNT:** Low Priority Extended VC Count
3	0h RO	**RESERVED2:** RESERVED
2:0	1h RO	**VCCNT:** Extended VC Count

20.5.41 PVCCAP2—Offset 108h

Port VC Capability 2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PVCCAP2: [B:0, D:27, F:0] + 108h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VCARBTBL								RESERVED																VCARBCAP							

Bit Range	Default & Access	Description
31:24	0h RO	**VCARBTBL:** VC Arbitration Table Offset
23:8	0h RO	**RESERVED:** RESERVED
7:0	0h RO	**VCARBCAP:** VC Arbitration Capability

20.5.42 PVCCTL—Offset 10Ch

Port VC Control

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PVCCTL: [B:0, D:27, F:0] + 10Ch

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED												VCARBSEL			LVCARBTBL

Bit Range	Default & Access	Description
15:4	0h RO	**RESERVED:** RESERVED
3:1	0h RO	**VCARBSEL:** VC Arbitration Select
0	0h RO	**LVCARBTBL:** Load VC Arbitration Table

20.5.43 PVCSTS—Offset 10Eh

Port VC Status

Access Method

Type: PCI Configuration Register (Size: 16 bits) **PVCSTS:** [B:0, D:27, F:0] + 10Eh

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED															VCARBTBLSTS

Bit Range	Default & Access	Description
15:1	0h RO	**RESERVED:** RESERVED
0	0h RO	**VCARBTBLSTS:** VC Arbitration Table Status

20.5.44 VC0CAP—Offset 110h

VC0 Resource Capability

Access Method

Type: PCI Configuration Register (Size: 32 bits) **VC0CAP:** [B:0, D:27, F:0] + 110h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PARBTBL								RESERVED	MTS							RST	APS	RESERVED1						PARBCAP							

Bit Range	Default & Access	Description
31:24	0h RO	**PARBTBL:** Port Arbitration Table Offset
23	0h RO	**RESERVED:** RESERVED
22:16	0h RO	**MTS:** Maximum Time Slots
15	0h RO	**RST:** Reject Snoop Transactions
14	0h RO	**APS:** Advanced Packet Switching
13:8	0h RO	**RESERVED1:** RESERVED
7:0	0h RO	**PARBCAP:** Port Arbitration Capability

20.5.45 VC0CTL—Offset 114h

VC0 Resource Control

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

VC0CTL: [B:0, D:27, F:0] + 114h

Default: 800000FFh

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
VC0EN	RESERVED				VC0ID			RESERVED1				PARBSEL			LPARBTBL	RESERVED2								VC0MAP							VC0MAP0

Bit Range	Default & Access	Description
31	1h RO	**VC0EN:** VC0 Enable
30:27	0h RO	**RESERVED:** RESERVED
26:24	0h RO	**VC0ID:** VC0 ID

Bit Range	Default & Access	Description
23:20	0h RO	**RESERVED1:** RESERVED
19:17	0h RO	**PARBSEL:** Port Arbitration Select
16	0h RO	**LPARBTBL:** Load Port Arbitration Table
15:8	0h RO	**RESERVED2:** RESERVED
7:1	7Fh RW	**VC0MAP:** TC/VC0 Map
0	1h RO	**VC0MAP0:** TC/VC0 Map

20.5.46 VC0STS—Offset 11Ah

VC0 Resource Status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

VC0STS: [B:0, D:27, F:0] + 11Ah

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED														VCNP	PARBTBLSTS

Bit Range	Default & Access	Description
15:2	0h RO	**RESERVED:** RESERVED
1	0h RO	**VCNP:** VC0 Negotiation Pending
0	0h RO	**PARBTBLSTS:** Port Arbitration Table Status

20.5.47 VCICAP—Offset 11Ch

VCi Resource Capabilities

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VCICAP: [B:0, D:27, F:0] + 11Ch

Default: 00000000h

31	28			24				20				16				12				8				4				0
0 0 0 0				0 0 0 0				0 0 0 0				0 0 0 0				0 0 0 0				0 0 0 0				0 0 0 0	0 0 0 0

Fields: PARBTBL (31:24), RESERVED (23), MTS (22:16), RST (15), APS (14), RESERVED1 (13:8), PARBCAP (7:0)

Bit Range	Default & Access	Description
31:24	0h RO	**PARBTBL:** Port Arbitration Table Offset
23	0h RO	**RESERVED:** RESERVED
22:16	0h RO	**MTS:** Maximum Time Slots
15	0h RO	**RST:** Reject Snoop Transactions
14	0h RO	**APS:** Advanced Packet Switching
13:8	0h RO	**RESERVED1:** RESERVED
7:0	0h RO	**PARBCAP:** Port Arbitration Capability

20.5.48 VCICTL—Offset 120h

VCi control register

Access Method

Type: PCI Configuration Register (Size: 32 bits) **VCICTL:** [B:0, D:27, F:0] + 120h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: VCIEN (31), Reserved_0 (30:27), VCIID (26:24), Reserved_1 (23:20), PARBSEL (19:17), LPARBTBL (16), Reserved_2 (15:8), VCIM (7:1), VCIM0 (0)

Bit Range	Default & Access	Description
31	0h RW	**VCIEN:** VCi Enable
30:27	0h RO	**Reserved_0:** Reserved
26:24	0h RW	**VCIID:** VCi ID
23:20	0h RO	**Reserved_1:** Reserved

Bit Range	Default & Access	Description
19:17	0h RO	**PARBSEL:** Port arbitration select. Doesn't apply.
16	0h RO	**LPARBTBL:** Load port arbitration table. Dosn't apply.
15:8	0h RO	**Reserved_2:** reserved
7:1	0h RW	**VCIM:** TC/VCi map
0	0h RO	**VCIM0:** TC/VCi map bit 0. Not used.

20.5.49 VCISTS—Offset 126h

VCi Resource Status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

VCISTS: [B:0, D:27, F:0] + 126h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED														VCNP	PARBTBLSTS

Bit Range	Default & Access	Description
15:2	0h RO	**RESERVED:** RESERVED
1	0h RO	**VCNP:** VCi Negotiation Pending
0	0h RO	**PARBTBLSTS:** Port Arbitration Table Status

20.5.50 RCCAP—Offset 130h

Root Complex Link Declaration Capability Header

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RCCAP: [B:0, D:27, F:0] + 130h

Default: 00010005h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1
NXTCAP			CV	PCIEECID			

Bit Range	Default & Access	Description
31:20	0h RO	**NXTCAP:** Next Capability Offset
19:16	1h RO	**CV:** Capability Version
15:0	5h RO	**PCIEECID:** PCI Express Extended Capability ID

20.5.51 ESD—Offset 134h

Element Self Description

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ESD: [B:0, D:27, F:0] + 134h

Default: 0F000100h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0
PORT		COMPID		LNKENT		RESERVED	ELTYP

Bit Range	Default & Access	Description
31:24	0Fh RO	**PORT:** Port Number
23:16	00h RO	**COMPID:** Component ID
15:8	01h RO	**LNKENT:** Number of Link Entries
7:4	0h RO	**RESERVED:** RESERVED
3:0	0h RO	**ELTYP:** Element Type

20.5.52 L1DESC—Offset 140h

Link 1 Description

Access Method

Type: PCI Configuration Register (Size: 32 bits)

L1DESC: [B:0, D:27, F:0] + 140h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
TPORT								TCOMPID								RESERVED														LNKTYP	LNKVLD

Bit Range	Default & Access	Description
31:24	0h RO	**TPORT:** Target Port Number
23:16	0h RO	**TCOMPID:** Target Component ID
15:2	0h RO	**RESERVED:** RESERVED
1	0h RO	**LNKTYP:** Link Type
0	1h RO	**LNKVLD:** Link Valid

20.5.53 L1LADD—Offset 148h

Link 1 Lower Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

L1LADD: [B:0, D:27, F:0] + 148h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
L1LADD																		RESERVED													

Bit Range	Default & Access	Description
31:14	0h RO	**L1LADD:** Link 1 Lower Address
13:0	0h RO	**RESERVED:** RESERVED

20.5.54 L1UADD—Offset 14Ch

Link 1 Upper Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**L1UADD:** [B:0, D:27, F:0] + 14Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

L1UADD

Bit Range	Default & Access	Description
31:0	0h RO	**L1UADD:** Link 1 Upper Address

20.6 HD Audio Memory Mapped I/O Registers

Table 225. Summary of HD Audio Memory Mapped I/O Registers—AZLBAR

Offset	Size	Register ID—Description	Default Value
0h	2	"GCAP—Offset 0h" on page 2713	4401h
2h	1	"VMIN—Offset 2h" on page 2714	00h
3h	1	"VMAJ—Offset 3h" on page 2714	01h
4h	2	"OUTPAY—Offset 4h" on page 2715	003Ch
6h	2	"INPAY—Offset 6h" on page 2715	001Dh
8h	4	"GCTL—Offset 8h" on page 2716	00000000h
Ch	1	"WAKEEN—Offset Ch" on page 2718	00h
Eh	1	"WAKESTS—Offset Eh" on page 2719	00h
10h	2	"GSTS—Offset 10h" on page 2719	0000h
18h	2	"OUTSTRMPAY—Offset 18h" on page 2720	0030h
1Ah	2	"INSTRMPAY—Offset 1Ah" on page 2721	0018h
20h	4	"INTCTL—Offset 20h" on page 2722	00000000h
24h	4	"INTSTS—Offset 24h" on page 2723	00000000h
30h	4	"WALCLK—Offset 30h" on page 2724	00000000h
38h	4	"SSYNC—Offset 38h" on page 2725	00000000h
40h	4	"CORBLBASE—Offset 40h" on page 2726	00000000h
44h	4	"CORBUBASE—Offset 44h" on page 2726	00000000h
48h	2	"CORBWP—Offset 48h" on page 2727	0000h
4Ah	2	"CORBRP—Offset 4Ah" on page 2728	0000h
4Ch	1	"CORBCTL—Offset 4Ch" on page 2728	00h
4Dh	1	"CORBSTS—Offset 4Dh" on page 2729	00h
4Eh	1	"CORBSIZE—Offset 4Eh" on page 2730	42h
50h	4	"RIRBLBASE—Offset 50h" on page 2731	00000000h
54h	4	"RIRBUBASE—Offset 54h" on page 2732	00000000h
58h	2	"RIRBWP—Offset 58h" on page 2733	0000h
5Ah	2	"RINTCNT—Offset 5Ah" on page 2734	0000h
5Ch	1	"RIRBCTL—Offset 5Ch" on page 2735	00h
5Dh	1	"RIRBSTS—Offset 5Dh" on page 2736	00h
5Eh	1	"RIRBSIZE—Offset 5Eh" on page 2737	42h
60h	4	"IC—Offset 60h" on page 2737	00000000h
64h	4	"IR—Offset 64h" on page 2738	00000000h
68h	2	"ICS—Offset 68h" on page 2739	0000h
70h	4	"DPLBASE—Offset 70h" on page 2739	00000000h
74h	4	"DPUBASE—Offset 74h" on page 2741	00000000h
80h	4	"ISD0CTL_STS—Offset 80h" on page 2742	00040000h
84h	4	"ISD0LPIB—Offset 84h" on page 2743	00000000h

Table 225. Summary of HD Audio Memory Mapped I/O Registers—AZLBAR (Continued)

Offset	Size	Register ID—Description	Default Value
88h	4	"ISD0CBL—Offset 88h" on page 2744	00000000h
8Ch	2	"ISD0LVI—Offset 8Ch" on page 2745	0000h
8Eh	2	"ISD0FIFOW—Offset 8Eh" on page 2746	0004h
90h	2	"ISD0FIFOS—Offset 90h" on page 2746	0000h
92h	2	"ISD0FMT—Offset 92h" on page 2747	0000h
98h	4	"ISD0BDLPLBA—Offset 98h" on page 2748	00000000h
9Ch	4	"ISD0BDLPUBA—Offset 9Ch" on page 2749	00000000h
A0h	4	"ISD1CTL_STS—Offset A0h" on page 2750	00040000h
A4h	4	"ISD1LPIB—Offset A4h" on page 2751	00000000h
A8h	4	"ISD1CBL—Offset A8h" on page 2752	00000000h
ACh	2	"ISD1LVI—Offset ACh" on page 2753	0000h
AEh	2	"ISD1FIFOW—Offset AEh" on page 2753	0004h
B0h	2	"ISD1FIFOS—Offset B0h" on page 2754	0000h
B2h	2	"ISD1FMT—Offset B2h" on page 2754	0000h
B8h	4	"ISD1BDLPLBA—Offset B8h" on page 2755	00000000h
BCh	4	"ISD1BDLPUBA—Offset BCh" on page 2756	00000000h
C0h	4	"ISD2CTL_STS—Offset C0h" on page 2757	00040000h
C4h	4	"ISD2LPIB—Offset C4h" on page 2759	00000000h
C8h	4	"ISD2CBL—Offset C8h" on page 2760	00000000h
CCh	2	"ISD2LVI—Offset CCh" on page 2760	0000h
CEh	2	"ISD2FIFOW—Offset CEh" on page 2761	0004h
D0h	2	"ISD2FIFOS—Offset D0h" on page 2761	0000h
D2h	2	"ISD2FMT—Offset D2h" on page 2762	0000h
D8h	4	"ISD2BDLPLBA—Offset D8h" on page 2763	00000000h
DCh	4	"ISD2BDLPUBA—Offset DCh" on page 2764	00000000h
E0h	4	"ISD3CTL_STS—Offset E0h" on page 2765	00040000h
E4h	4	"ISD3LPIB—Offset E4h" on page 2766	00000000h
E8h	4	"ISD3CBL—Offset E8h" on page 2767	00000000h
ECh	2	"ISD3LVI—Offset ECh" on page 2768	0000h
EEh	2	"ISD3FIFOW—Offset EEh" on page 2768	0004h
F0h	2	"ISD3FIFOS—Offset F0h" on page 2769	0000h
F2h	2	"ISD3FMT—Offset F2h" on page 2769	0000h
F8h	4	"ISD3BDLPLBA—Offset F8h" on page 2770	00000000h
FCh	4	"ISD3BDLPUBA—Offset FCh" on page 2771	00000000h
100h	4	"OSD0CTL_STS—Offset 100h" on page 2772	00040000h
104h	4	"OSD0LPIB—Offset 104h" on page 2774	00000000h
108h	4	"OSD0CBL—Offset 108h" on page 2775	00000000h
10Ch	2	"OSD0LVI—Offset 10Ch" on page 2775	0000h
10Eh	2	"OSD0FIFOW—Offset 10Eh" on page 2776	0004h

Table 225. Summary of HD Audio Memory Mapped I/O Registers—AZLBAR (Continued)

Offset	Size	Register ID—Description	Default Value
110h	2	"OSD0FIFOS—Offset 110h" on page 2776	0000h
112h	2	"OSD0FMT—Offset 112h" on page 2777	0000h
118h	4	"OSD0BDLPLBA—Offset 118h" on page 2778	00000000h
11Ch	4	"OSD0BDLPUBA—Offset 11Ch" on page 2779	00000000h
120h	4	"OSD1CTL_STS—Offset 120h" on page 2780	00040000h
124h	4	"OSD1LPIB—Offset 124h" on page 2781	00000000h
128h	4	"OSD1CBL—Offset 128h" on page 2782	00000000h
12Ch	2	"OSD1LVI—Offset 12Ch" on page 2783	0000h
12Eh	2	"OSD1FIFOW—Offset 12Eh" on page 2783	0004h
130h	2	"OSD1FIFOS—Offset 130h" on page 2784	0000h
132h	2	"OSD1FMT—Offset 132h" on page 2784	0000h
138h	4	"OSD1BDLPLBA—Offset 138h" on page 2785	00000000h
13Ch	4	"OSD1BDLPUBA—Offset 13Ch" on page 2786	00000000h
140h	4	"OSD2CTL_STS—Offset 140h" on page 2787	00040000h
144h	4	"OSD2LPIB—Offset 144h" on page 2789	00000000h
148h	4	"OSD2CBL—Offset 148h" on page 2790	00000000h
14Ch	2	"OSD2LVI—Offset 14Ch" on page 2790	0000h
14Eh	2	"OSD2FIFOW—Offset 14Eh" on page 2791	0004h
150h	2	"OSD2FIFOS—Offset 150h" on page 2792	0000h
152h	2	"OSD2FMT—Offset 152h" on page 2792	0000h
158h	4	"OSD2BDLPLBA—Offset 158h" on page 2793	00000000h
15Ch	4	"OSD2BDLPUBA—Offset 15Ch" on page 2794	00000000h
160h	4	"OSD3CTL_STS—Offset 160h" on page 2795	00040000h
164h	4	"OSD3LPIB—Offset 164h" on page 2797	00000000h
168h	4	"OSD3CBL—Offset 168h" on page 2798	00000000h
16Ch	2	"OSD3LVI—Offset 16Ch" on page 2799	0000h
16Eh	2	"OSD3FIFOW—Offset 16Eh" on page 2799	0004h
170h	2	"OSD3FIFOS—Offset 170h" on page 2800	0000h
172h	2	"OSD3FMT—Offset 172h" on page 2801	0000h
178h	4	"OSD3BDLPLBA—Offset 178h" on page 2802	00000000h
17Ch	4	"OSD3BDLPUBA—Offset 17Ch" on page 2803	00000000h
2030h	4	"WLCLKA—Offset 2030h" on page 2803	00000000h
2084h	4	"ISD0LPIBA—Offset 2084h" on page 2804	00000000h
20A4h	4	"ISD1LPIBA—Offset 20A4h" on page 2805	00000000h
20C4h	4	"ISD2LPIBA—Offset 20C4h" on page 2805	00000000h
20E4h	4	"ISD3LPIBA—Offset 20E4h" on page 2806	00000000h
2104h	4	"OSD0LPIBA—Offset 2104h" on page 2807	00000000h

Table 225. Summary of HD Audio Memory Mapped I/O Registers—AZLBAR (Continued)

Offset	Size	Register ID—Description	Default Value
2124h	4	"OSD1LPIBA—Offset 2124h" on page 2807	00000000h
2144h	4	"OSD2LPIBA—Offset 2144h" on page 2808	00000000h
2164h	4	"OSD3LPIBA—Offset 2164h" on page 2809	00000000h

20.6.1 GCAP—Offset 0h

Global Capabilities

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

GCAP: [AZLBAR] + 0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 4401h

15			12				8				4				0
0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1

Bits 15:12	Bits 11:8	Bits 7:3	Bits 2:1	Bit 0
NUMBER_OF_OUTPUT_STREAMS_SUPPORTED	NUMBER_OF_INPUT_STREAMS_SUPPORTED	NUMBER_OF_BIDIRECTIONAL_STREAMS_SUPPORTED	NUMBER_OF_SERIAL_DATA_OUT_SIGNALS	BIT_ADDRESS_SUPPORTED

Bit Range	Default & Access	Description
15:12	4h RW	**NUMBER_OF_OUTPUT_STREAMS_SUPPORTED:** 0011b indicates that in this SoC, Intel HD Audio controller supports three output streams.
11:8	4h RW	**NUMBER_OF_INPUT_STREAMS_SUPPORTED:** 0011b indicates that in this SoC, Intel HD Audio controller supports three output streams.
7:3	00h RO	**NUMBER_OF_BIDIRECTIONAL_STREAMS_SUPPORTED:** 00000b indicates that the Intel HD Audio controller supports 0 bidirectional streams.
2:1	0h RO	**NUMBER_OF_SERIAL_DATA_OUT_SIGNALS:** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal.

Bit Range	Default & Access	Description
0	01h RW	**BIT_ADDRESS_SUPPORTED:** A 1 indicates that the Intel HD Audio controller supports 64 bit addressing for BDL addresses data buffer addresses and command buffer addresses.

20.6.2 VMIN—Offset 2h

Minor Version

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

VMIN: [AZLBAR] + 2h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0

MINOR_VERSION

Bit Range	Default & Access	Description
7:0	00h RO	**MINOR_VERSION:** Indicates SoC supports minor revision number 00h of the Intel HD Audio specification.

20.6.3 VMAJ—Offset 3h

Major Version

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

VMAJ: [AZLBAR] + 3h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1

MAJOR_VERSION

Bit Range	Default & Access	Description
7:0	01h RO	**MAJOR_VERSION:** Indicates SoC supports major revision number 1 of the Intel HD Audio specification.

20.6.4 OUTPAY—Offset 4h

Output Payload Capability

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OUTPAY: [AZLBAR] + 4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 003Ch

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

OUTPUT_PAYLOAD_CAPABILITY

Bit Range	Default & Access	Description
15:0	003Ch RO	**OUTPUT_PAYLOAD_CAPABILITY:** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16 bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz the data is double pumped provides 1000 bits per frame or 62.5 words in total. 40 bits are used for command and control leaving 60 words available for data payload. 00h 0 words 01h 1 word payload FFh 255h word payload

20.6.5 INPAY—Offset 6h

Input Payload Capability

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

INPAY: [AZLBAR] + 6h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 001Dh

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

INPUT_PAYLOAD_CAPABILITY

Bit Range	Default & Access	Description
15:0	001Dh RO	**INPUT_PAYLOAD_CAPABILITY:** Indicates the total input payload available on the link. This does not include bandwidth used for response. This measurement is in 16 bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame or 31.25 words in total. 36 bits are used for response leaving 29 words for data payload. 00h 0 words 01h 1 word payload FFh 255h word payload

20.6.6 GCTL—Offset 8h

Global Control

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GCTL: [AZLBAR] + 8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

Bits	31:9	8	7:2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0	0	0
Field	RESERVED0	ACCEPT_UNSOLICITED_RESPONSE_ENABLE	RESERVED1	FLUSH_CONTROL	CONTROLLER_RESET

Bit Range	Default & Access	Description
31:9	0h RO	**RESERVED0:** reserved
8	0h RW	**ACCEPT_UNSOLICITED_RESPONSE_ENABLE:** If UNSOL is a 1 Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If UNSOL is a 0 unsolicited responses are not accepted and dropped on the floor.
7:2	00h RO	**RESERVED1:** reserved
1	0h RW	**FLUSH_CONTROL:** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated the DMA Position Buffer must be programmed with a valid memory address by software but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also all streams must be stopped the associated RUN bit must be 0 . When the flush is initiated the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	0h RW	**CONTROLLER_RESET:** Writing a 0 to this bit causes the Intel HD Audio controller to be reset. All state machines FIFO s and non Suspend well memory mapped configuration registers except ECAP and PCI Configuration Registers in the controller will be reset. The Intel HD Audio link RESET signal will be asserted and all other link signals will be driven to their reset values. After the hardware has completed sequencing into the reset state it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and de assert the Intel HD Audio link RESET signal. Software is responsible forsetting clearing this bit such that the minimum Intel HD Audio link RESET signal assertion pulse width specification is met. When the controller hardware is ready to begin operation it will report a1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST bit defaults to a 0 after hardware reset therefore software needs to write a 1 to this bit to begin operation. Note thatthe CORB RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST is written to 0 asserted in order to assure a clean re start. When setting or clearing CRST software must ensure that minimum link timing requirements minimum RESET assertion time etc. are met. When CRST is 0 indicating that the controller is in reset writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST bit itself. The Global Control register is write able as a DWord Word or Byte even when CRST is 0 if the byte enable for the byte containing the CRST bit Byte Enable 0 is active. If Byte Enable 0 is not active writes to the Global Control register will be ignored when CRST is 0. When CRST is 0 reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST or on a D3hot gt D0 transition.

20.6.7 WAKEEN—Offset Ch

Wake Enable

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

WAKEEN: [AZLBAR] + Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED0				SDIN_WAKE_ENABLE_FLAGS			

Bit Range	Default & Access	Description
7:4	0h RO	**RESERVED0:** reserved
3:0	0h RW	**SDIN_WAKE_ENABLE_FLAGS:** Bits which control which SDI signal s may generate a wake event. A 1 bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake.

20.6.8 WAKESTS—Offset Eh

Wake Status

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

WAKESTS: [AZLBAR] + Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED0				SDIN_STATE			

Bit Range	Default & Access	Description
7:4	0h RO	**RESERVED0:** reserved
3:0	0h RO	**SDIN_STATE:** Flag bits that indicate which SDI signal s received a State Change event. The bits are cleared by writing 1 s to them.

20.6.9 GSTS—Offset 10h

Global Status

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

GSTS: [AZLBAR] + 10h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0														FLUSH_STATUS	RESERVED1

Bit Range	Default & Access	Description
15:2	0000h RO	**RESERVED0:** reserved
1	0h RW	**FLUSH_STATUS:** This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1to clear this bit before the next time FCNTRL is set.

Bit Range	Default & Access	Description
0	0h RO	**RESERVED1:** reserved

20.6.10 OUTSTRMPAY—Offset 18h

Output Stream Payload Capability

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OUTSTRMPAY: [AZLBAR] + 18h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0030h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

OUTPUT_STREAM_PAYLOAD_CAPABILITY

Bit Range	Default & Access	Description
15:0	0030h RO	**OUTPUT_STREAM_PAYLOAD_CAPABILITY:** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words 96B is the maximum supported therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h 0 words 01h 1 word payload FFh 255h word payload

20.6.11 INSTRMPAY—Offset 1Ah

Input Stream Payload Capability

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

INSTRMPAY: [AZLBAR] + 1Ah

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0018h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

INPUT_STREAM_PAYLOAD_CAPABILITY

Bit Range	Default & Access	Description
15:0	0018h RO	**INPUT_STREAM_PAYLOAD_CAPABILITY:** Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words 48B is the maximum supported therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h 0 words 01h 1 word payload FFh 255h word payload

20.6.12 INTCTL—Offset 20h

Interrupt Control

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

INTCTL: [AZLBAR] + 20h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GLOBAL_INTERRUPT_ENABLE	CONTROLLER_INTERRUPT_ENABLE	RESERVED0	STREAM_INTERRUPT_ENABLE

Bit Range	Default & Access	Description
31	0h RW	**GLOBAL_INTERRUPT_ENABLE:** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space such as the Interrupt Enable bit in the PCI Configuration Space. This bit is not affected by controller reset.
30	0h RW	**CONTROLLER_INTERRUPT_ENABLE:** Enables the general interrupt for controller functions. When set to 1 and GIE is enabled the controller generates an interrupt when the CIS bit gets set. This bit is not affected by controller reset.
29:8	0h RO	**RESERVED0:** reserved
7:0	00h RW	**STREAM_INTERRUPT_ENABLE:** When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC 1 in the BDL entry being completed or as a result of a FIFO error underrun or overrun occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially based on their order in the register set. Bit 0 Input Stream 1 Bit 1 Input Stream 2 Bit 2 Input Stream 3 Bit 3 Input Stream 4 Bit 4 Output Stream 1 Bit 5 Output Stream 2 Bit 6 Output Stream 3 Bit 7 Output Stream 4

20.6.13 INTSTS—Offset 24h

Interrupt Status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

INTSTS: [AZLBAR] + 24h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31	30	29:8	7:0
0	0	0000 0000 0000 0000 0000 00	0000 0000
GLOBAL_INTERRUPT_STATUS	RESERVED0	RESERVED1	STREAM_INTERRUPT_STATUS

Bit Range	Default & Access	Description
31	0h RO	**GLOBAL_INTERRUPT_STATUS:** This bit is an OR of all of the interrupt status bits in this register.
30	0h RO	**RESERVED0:** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt a Response Buffer Overrun Interrupt CORB Memory Error Interrupt Error Present Interrupt Intel Reserved or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.
29:8	0h RO	**RESERVED1:** reserved
7:0	00h RW	**STREAM_INTERRUPT_STATUS:** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream s interrupt status bits. The streams are numbered and the SIS bits assigned sequentially based on their order in the register set. Bit 0 Input Stream 1 Bit 1 Input Stream 2 Bit 2 Input Stream 3 Bit 3 Input Stream 4 Bit 4 Output Stream 1 Bit 5 Output Stream 2 Bit 6 Output Stream 3 Bit 7 Output Stream 4

20.6.14 WALCLK—Offset 30h

Wall Clock Counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

WALCLK: [AZLBAR] + 30h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WALL_CLOCK_COUNTER

Bit Range	Default & Access	Description
31:0	0h RO	**WALL_CLOCK_COUNTER:** 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

20.6.15 SSYNC—Offset 38h

Stream Synchronization

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSYNC: [AZLBAR] + 38h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED0 (bits 31:8) | STREAM_SYNCHRONIZATION_BITS (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RESERVED0:** reserved
7:0	00h RW	**STREAM_SYNCHRONIZATION_BITS:** The Stream Synchronization bits when set to 1 block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor bit 0 corresponds to the first Stream Descriptor etc. To synchronously start a set of DMA engines the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. When all streams are ready FIFORDY 1 the associated SSYNC bits can all be set to 0 at the same time and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams first the bits are set in the SSYNC register and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially based on their order in the register set. Bit 0 Input Stream 1 Bit 1 Input Stream 2 Bit 2 Input Stream 3 Bit 3 Input Stream 4 Bit 4 Output Stream 1 Bit 5 Output Stream 2 Bit 6 Output Stream 3 Bit 7 Output Stream 4 Each bit can be reset by their respective stream reset.

20.6.16 CORBLBASE—Offset 40h

CORB Lower Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CORBLBASE: [AZLBAR] + 40h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CORB_LOWER_BASE_ADDRESS (bits 31:7)
CORB_LOWER_BASE_UNIMPLEMENTED_BITS (bits 6:0)

Bit Range	Default & Access	Description
31:7	0h RW	**CORB_LOWER_BASE_ADDRESS:** Lower address of the Command Output Ring Buffer allowing the CORB Base Address to be assigned on any 64 B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	00h RO	**CORB_LOWER_BASE_UNIMPLEMENTED_BITS:** Hardwired to 0. This requires the CORB to be allocated with 128 byte granularity to allow for cache line fetch optimizations.

20.6.17 CORBUBASE—Offset 44h

CORB Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CORBUBASE: [AZLBAR] + 44h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
CORB_UPPER_BASE_ADDRESS							

Bit Range	Default & Access	Description
31:0	0h RW	**CORB_UPPER_BASE_ADDRESS:** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

20.6.18 CORBWP—Offset 48h

CORB Write Pointer

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

CORBWP: [AZLBAR] + 48h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED0		CORB_WRITE_POINTER	

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**CORB_WRITE_POINTER:** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries 256 x 4B 1KB . This field may be written while the DMA engine is running.

20.6.19 CORBRP—Offset 4Ah

CORB Read Pointer

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

CORBRP: [AZLBAR] + 4Ah

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CORB_READ_POINTER_RESET	RESERVED0							CORB_READ_POINTER							

Bit Range	Default & Access	Description
15	0h RW	**CORB_READ_POINTER_RESET:** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	00h RO	**RESERVED0:** reserved
7:0	00h RO	**CORB_READ_POINTER:** Software reads this field to determine how many commands it can write to the CORB without over running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over written by software. Supports 256 CORB entries 256 x 4B 1KB . This field may be read while the DMA engine is running.

20.6.20 CORBCTL—Offset 4Ch

CORB Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

CORBCTL: [AZLBAR] + 4Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED0						ENABLE_CORB_DMA_ENGINE	CORB_MEMORY_ERROR_INTERRUPT_ENABLE

Bit Range	Default & Access	Description
7:2	00h RO	**RESERVED0:** reserved
1	0h RW	**ENABLE_CORB_DMA_ENGINE:** 0 DMA Stop 1 DMA Run After SW writes a 0 to this bit the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**CORB_MEMORY_ERROR_INTERRUPT_ENABLE:** If this bit is set and GIE and CIE are enabled the controller will generate an interrupt if the MEI status bit is set.

20.6.21 CORBSTS—Offset 4Dh

CORB Status

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

CORBSTS: [AZLBAR] + 4Dh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED0							CORB_MEMORY_ERROR_INDICATION

Bit Range	Default & Access	Description
7:1	00h RO	**RESERVED0:** reserved
0	0h RW	**CORB_MEMORY_ERROR_INDICATION:** If this status bit is set the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However this type of error leaves the audio subsystem in an unviable state and typically requires CRST .

20.6.22 CORBSIZE—Offset 4Eh

CORB Size

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

CORBSIZE: [AZLBAR] + 4Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 42h

7			4				0
0	1	0	0	0	0	1	0
CORB_SIZE_CAPABILITY				RESERVED0		CORB_SIZE	

Bit Range	Default & Access	Description
7:4	4h RO	**CORB_SIZE_CAPABILITY:** 0100b indicates that the HD Audio controller only supports a CORB size of 256 CORB entries 1024B .

Bit Range	Default & Access	Description
3:2	0h RO	**RESERVED0:** reserved
1:0	02h RO	**CORB_SIZE:** Hardwired to 10b which sets the CORB size to 256 entries 1024B .

20.6.23 RIRBLBASE—Offset 50h

RIRB Lower Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RIRBLBASE: [AZLBAR] + 50h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIRB_LOWER_BASE_ADDRESS

RIRB_LOWER_BASE_UNIMPLEMENTED_BITS

Bit Range	Default & Access	Description
31:7	0h RW	**RIRB_LOWER_BASE_ADDRESS:** Lower address of the Response Input Ring Buffer allowing the RIRB Base Address to be assigned on any 64 B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	00h RO	**RIRB_LOWER_BASE_UNIMPLEMENTED_BITS:** Hardwired to 0 to force 128 byte buffer alignment for cache line fetch optimizations.

20.6.24 RIRBUBASE—Offset 54h

RIRB Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RIRBUBASE: [AZLBAR] + 54h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIRB_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**RIRB_UPPER_BASE_ADDRESS:** Upper 32 bits of address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

20.6.25 RIRBWP—Offset 58h

RIRB Write Pointer

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

RIRBWP: [AZLBAR] + 58h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RIRB_WRITE_POINTER_RESET	RESERVED0							RIRB_WRITE_POINTER							

Bit Range	Default & Access	Description
15	0h WO	**RIRB_WRITE_POINTER_RESET:** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0 s. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.
14:8	00h RO	**RESERVED0:** reserved
7:0	00h RO	**RIRB_WRITE_POINTER:** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units since each RIRB entry is 2 Dwords long . Supports up to 256 RIRB entries 256 x 8B 2KB . This field may be read while the DMA engine is running.

20.6.26 RINTCNT—Offset 5Ah

Response Interrupt Count

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

RINTCNT: [AZLBAR] + 5Ah

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0								N_RESPONSE_INTERRUPT_COUNT							

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**N_RESPONSE_INTERRUPT_COUNT:** 0000_0001b 1 Response sent to RIRB 1111_1111b 255 Responses sent to RIRB 0000_0000b 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned as opposed to the number of frames in which there were responses. If more than one codec responds in one frame then the count is increased by the number of responses received in the frame.

20.6.27 RIRBCTL—Offset 5Ch

RIRB Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

RIRBCTL: [AZLBAR] + 5Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED0					RESPONSE_OVERRUN_INTERRUPT_CONTROL	RIRB_DMA_ENABLE	RESPONSE_INTERRUPT_CONTROL

Bit Range	Default & Access	Description
7:3	00h RO	**RESERVED0:** reserved
2	0h RW	**RESPONSE_OVERRUN_INTERRUPT_CONTROL:** If this bit is set and GIE and CIE are enabled the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.
1	0h RW	**RIRB_DMA_ENABLE:** 0 DMA Stop 1 DMA Run After SW writes a 0 to this bit the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**RESPONSE_INTERRUPT_CONTROL:** 0 Disable Interrupt 1 Generate an interrupt if GIE and CIE are enabled after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs whichever occurs first . The N counter is reset when the interrupt is generated.

20.6.28 RIRBSTS—Offset 5Dh

RIRB Status

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

RIRBSTS: [AZLBAR] + 5Dh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED0					RESPONSE_OVERRUN_INTERRUPT_STATUS	RESERVED1	RESPONSE_INTERRUPT

Bit Range	Default & Access	Description
7:3	00h RO	**RESERVED0:** reserved
2	0h RW	**RESPONSE_OVERRUN_INTERRUPT_STATUS:** Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.
1	0h RO	**RESERVED1:** reserved
0	0h RW	**RESPONSE_INTERRUPT:** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI x inputs whichever occurs first . Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

20.6.29 RIRBSIZE—Offset 5Eh

RIRB Size

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

RIRBSIZE: [AZLBAR] + 5Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 42h

7			4				0
0	1	0	0	0	0	1	0
RIRB_SIZE_CAPABILITY				RESERVED0		RIRB_SIZE	

Bit Range	Default & Access	Description
7:4	4h RO	**RIRB_SIZE_CAPABILITY:** 0100b indicates that the HD Audio controller only supports a RIRB size of 256 RIRB entries 2048B .
3:2	0h RO	**RESERVED0:** reserved
1:0	02h RO	**RIRB_SIZE:** Hardwired to 10b which sets the RIRB size to 256 entries 2048B .

20.6.30 IC—Offset 60h

Immediate Command

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC: [AZLBAR] + 60h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IMMEDIATE_COMMAND_WRITE

Bit Range	Default & Access	Description
31:0	0h RW	**IMMEDIATE_COMMAND_WRITE:** The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.

20.6.31 IR—Offset 64h

Immediate Response

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IR: [AZLBAR] + 64h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IMMEDIATE_RESPONSE_READ

Bit Range	Default & Access	Description
31:0	0h RO	**IMMEDIATE_RESPONSE_READ:** This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame there is no guarantee as to which response will be latched. Therefore broadcast type commands must not be issued via the Immediate Command mechanism.

20.6.32 ICS—Offset 68h

Immediate Command Status

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ICS: [AZLBAR] + 68h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0														IMMEDIATE_RESULT_VALID	IMMEDIATE_COMMAND_BUSY

Bit Range	Default & Access	Description
15:2	0000h RO	**RESERVED0:** reserved
1	0h RW	**IMMEDIATE_RESULT_VALID:** This bit is set to a 1 by hardware when a new response is latched into the IRR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit by writing a one to it before issuing a new command so that the software may determine when a new response has arrived.
0	0h RW	**IMMEDIATE_COMMAND_BUSY:** When this bit as read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 via software writing a 1 the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register the controller hardware sets the IRV flag and clears the ICB bit back to 0. SW may write this bit to a 0 if the bit fails to return to 0 after a reasonable timeout period. Note that an Immediate Command must not be issued while the CORB RIRB mechanism is operating otherwise the responses conflict. This must be enforced by software.

20.6.33 DPLBASE—Offset 70h

DMA Position Lower Base Address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPLBASE: [AZLBAR] + 70h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:7	Bits 6:1	Bit 0
DMA_POSITION_LOWER_BASE_ADDRESS	DMA_POSITION_LOWER_BASE_UNIMPLEMENTED_BITS	DMA_POSITION_BUFFER_ENABLE

Bit Range	Default & Access	Description
31:7	0h RW	**DMA_POSITION_LOWER_BASE_ADDRESS:** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	00h RO	**DMA_POSITION_LOWER_BASE_UNIMPLEMENTED_BITS:** Hardwired to 0 to force 128 byte buffer alignment for cache line write optimizations.
0	0h RW	**DMA_POSITION_BUFFER_ENABLE:** When this bit is set to a 1 the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically typically once frame . Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream s DMA buffer. This has particular relevance in systems which support isochronous transfer the stream positions in the software visible memory buffer must represent stream data which has reached the Global Observation point.

20.6.34 DPUBASE—Offset 74h

DMA position Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DPUBASE: [AZLBAR] + 74h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_POSITION_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**DMA_POSITION_UPPER_BASE_ADDRESS:** Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

20.6.35 ISD0CTL_STS—Offset 80h

Input Stream Descriptor 0 Control and status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD0CTL_STS: [AZLBAR] + 80h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 1 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED1 | FIFO_READY | DESCRIPTOR_ERROR | FIFO_ERROR | BUFFER_COMPLETION_INTERRUPT_STATUS | RESERVED2 | STREAM_NUMBER | BIDIRECTIONAL_DIRECTION_CONTROL | TRAFFIC_PRIORITY | STRIPE_CONTROL | RESERVED0 | DESCRIPTOR_ERROR_INTERRUPT_ENABLE | FIFO_ERROR_INTERRUPT_ENABLE | INTERRUPT_ON_COMPLETION_ENABLE | STREAM_RUN | STREAM_RESET

Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For input streams the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an input stream this indicates a FIFO overrun occurring while the RUN bit is set. When this happens the FIFO pointers don t increment and the incoming data is not written into the FIFO thereby being lost.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved

Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When an input stream is detected on any of the SDIx signals that match this value the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number two different SDIx inputs may not be configured with the same stream number. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** This field is meaningless for input streams.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error overrun for input will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

20.6.36 ISD0LPIB—Offset 84h

Input Stream Descriptor 0 Link Position in Buffer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD0LPIB: [AZLBAR] + 84h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.37 ISD0CBL—Offset 88h

Input Stream Descriptor 0 Cyclic Buffer Length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD0CBL: [AZLBAR] + 88h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CYCLIC_BUFFER_LENGTH

Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

20.6.38 ISD0LVI—Offset 8Ch

Input Stream Descriptor 0 Last Valid Index

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD0LVI: [AZLBAR] + 8Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:8	Bits 7:0
RESERVED0	LAST_VALID_INDEX

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1 i.e. there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

20.6.39 ISD0FIFOW—Offset 8Eh

Input Stream Descriptor 0 FIFO Eviction Watermark

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD0FIFOW: [AZLBAR] + 8Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RESERVED0													FIFO_WATERMARK		

Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes accumulated in the FIFO before the controller will start an eviction of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For input streams the FIFOW value is determined by the EM3.ISRWS SEM3.ISRWS field.

20.6.40 ISD0FIFOS—Offset 90h

Input Stream Descriptor 0 FIFO Size

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD0FIFOS: [AZLBAR] + 90h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FIFO_SIZE															

Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be revicted by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA d into memory and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in ISD0FMT register. As the default value is zero, SW must write to the respective ISD0FMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

20.6.41 ISD0FMT—Offset 92h

Input Stream Descriptor 0 Format

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD0FMT: [AZLBAR] + 92h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULTIPLE			SAMPLE_BASE_RATE_DIVISOR			RESERVED1	BITS_PER_SAMPLE			NUMBER_OF_CHANNELS			

Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved

Bit Range	Default & Access	Description
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

20.6.42 ISD0BDLPLBA—Offset 98h

Input Stream Descriptor 0 Buffer Descriptor List Pointer Lower Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD0BDLPLBA: [AZLBAR] + 98h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS (31:7) | RESERVED0 (6:1) | PROTECT (0)

Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved

Bit Range	Default & Access	Description
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

20.6.43 ISD0BDLPUBA—Offset 9Ch

Input Stream Descriptor 0 Buffer Descriptor List Pointer Upper Base Address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD0BDLPUBA: [AZLBAR] + 9Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

20.6.44 ISD1CTL_STS—Offset A0h

Input Stream Descriptor 1 Control and status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD1CTL_STS: [AZLBAR] + A0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:30	RESERVED1
29	FIFO_READY
28	DESCRIPTOR_ERROR
27	FIFO_ERROR
26	BUFFER_COMPLETION_INTERRUPT_STATUS
25:24	RESERVED2
23:20	STREAM_NUMBER
19	BIDIRECTIONAL_DIRECTION_CONTROL
18	TRAFFIC_PRIORITY
17:16	STRIPE_CONTROL
15:5	RESERVED0
4	DESCRIPTOR_ERROR_INTERRUPT_ENABLE
3	FIFO_ERROR_INTERRUPT_ENABLE
2	INTERRUPT_ON_COMPLETION_ENABLE
1	STREAM_RUN
0	STREAM_RESET

Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For input streams the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an input stream this indicates a FIFO overrun occurring while the RUN bit is set. When this happens the FIFO pointers don t increment and the incoming data is not written into the FIFO thereby being lost.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved

Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When an input stream is detected on any of the SDIx signals that match this value the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number two different SDIx inputs may not be configured with the same stream number. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** This field is meaningless for input streams.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error overrun for input will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

20.6.45 ISD1LPIB—Offset A4h

Input Stream Descriptor 1 Link Position in Buffer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD1LPIB: [AZLBAR] + A4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LINK_POSITION_IN_BUFFER																															

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.46 ISD1CBL—Offset A8h

Input Stream Descriptor 1 Cyclic Buffer Length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD1CBL: [AZLBAR] + A8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CYCLIC_BUFFER_LENGTH																															

Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

20.6.47 ISD1LVI—Offset ACh

Input Stream Descriptor 1 Last Valid Index

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD1LVI: [AZLBAR] + ACh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0								LAST_VALID_INDEX							

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1 i.e. there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

20.6.48 ISD1FIFOW—Offset AEh

Input Stream Descriptor 1 FIFO Eviction Watermark

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD1FIFOW: [AZLBAR] + AEh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RESERVED0													FIFO_WATERMARK		

Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes accumulated in the FIFO before the controller will start an eviction of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For input streams the FIFOW value is determined by the EM3.ISRWS SEM3.ISRWS field.

20.6.49 ISD1FIFOS—Offset B0h

Input Stream Descriptor 1 FIFO Size

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD1FIFOS: [AZLBAR] + B0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FIFO_SIZE															

Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be revicted by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA d into memory and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in ISD1FMT register. As the default value is zero, SW must write to the respective ISD1FMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

20.6.50 ISD1FMT—Offset B2h

Input Stream Descriptor 1 Format

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD1FMT: [AZLBAR] + B2h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULTIPLE			SAMPLE_BASE_RATE_DIVISOR			RESERVED1	BITS_PER_SAMPLE			NUMBER_OF_CHANNELS			

Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

20.6.51 ISD1BDLPLBA—Offset B8h

Input Stream Descriptor 1 Buffer Descriptor List Pointer Lower Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD1BDLPLBA: [AZLBAR] + B8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS	RESERVED0	PROTECT

Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

20.6.52 ISD1BDLPUBA—Offset BCh

Input Stream Descriptor 1 Buffer Descriptor List Pointer Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD1BDLPUBA: [AZLBAR] + BCh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

20.6.53 ISD2CTL_STS—Offset C0h

Input Stream Descriptor 2 Control and status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD2CTL_STS: [AZLBAR] + C0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED1 | FIFO_READY | DESCRIPTOR_ERROR | FIFO_ERROR | BUFFER_COMPLETION_INTERRUPT_STATUS | RESERVED2 | STREAM_NUMBER | BIDIRECTIONAL_DIRECTION_CONTROL | TRAFFIC_PRIORITY | STRIPE_CONTROL | RESERVED0 | DESCRIPTOR_ERROR_INTERRUPT_ENABLE | FIFO_ERROR_INTERRUPT_ENABLE | INTERRUPT_ON_COMPLETION_ENABLE | STREAM_RUN | STREAM_RESET

Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For input streams the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an input stream this indicates a FIFO overrun occurring while the RUN bit is set. When this happens the FIFO pointers don t increment and the incoming data is not written into the FIFO thereby being lost.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When an input stream is detected on any of the SDIx signals that match this value the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number two different SDIx inputs may not be configured with the same stream number. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** This field is meaningless for input streams.

Bit Range	Default & Access	Description
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error overrun for input will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

20.6.54 ISD2LPIB—Offset C4h

Input Stream Descriptor 2 Link Position in Buffer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD2LPIB: [AZLBAR] + C4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.55 ISD2CBL—Offset C8h

Input Stream Descriptor 2 Cyclic Buffer Length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD2CBL: [AZLBAR] + C8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CYCLIC_BUFFER_LENGTH

Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

20.6.56 ISD2LVI—Offset CCh

Input Stream Descriptor 2 Last Valid Index

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD2LVI: [AZLBAR] + CCh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0								LAST_VALID_INDEX							

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1 i.e. there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

20.6.57 ISD2FIFOW—Offset CEh

Input Stream Descriptor 2 FIFO Eviction Watermark

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD2FIFOW: [AZLBAR] + CEh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RESERVED0													FIFO_WATERMARK		

Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes accumulated in the FIFO before the controller will start an eviction of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For input streams the FIFOW value is determined by the EM3.ISRWS SEM3.ISRWS field.

20.6.58 ISD2FIFOS—Offset D0h

Input Stream Descriptor 2 FIFO Size

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD2FIFOS: [AZLBAR] + D0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FIFO_SIZE															

Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be revicted by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA d into memory and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in ISD2FMT register. As the default value is zero, SW must write to the respective ISD2FMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

20.6.59 ISD2FMT—Offset D2h

Input Stream Descriptor 2 Format

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD2FMT: [AZLBAR] + D2h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULTIPLE			SAMPLE_BASE_RATE_DIVISOR			RESERVED1	BITS_PER_SAMPLE			NUMBER_OF_CHANNELS			

Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved

Bit Range	Default & Access	Description
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

20.6.60 ISD2BDLPLBA—Offset D8h

Input Stream Descriptor 2 Buffer Descriptor List Pointer Lower Base Address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD2BDLPLBA: [AZLBAR] + D8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:7	Bits 6:1	Bit 0
BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS	RESERVED0	PROTECT

Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

20.6.61 ISD2BDLPUBA—Offset DCh

Input Stream Descriptor 2 Buffer Descriptor List Pointer Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD2BDLPUBA: [AZLBAR] + DCh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

20.6.62 ISD3CTL_STS—Offset E0h

Input Stream Descriptor 3 Control and status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD3CTL_STS: [AZLBAR] + E0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:30	RESERVED1
29	FIFO_READY
28	DESCRIPTOR_ERROR
27	FIFO_ERROR
26	BUFFER_COMPLETION_INTERRUPT_STATUS
25:24	RESERVED2
23:20	STREAM_NUMBER
19	BIDIRECTIONAL_DIRECTION_CONTROL
18	TRAFFIC_PRIORITY
17:16	STRIPE_CONTROL
15:5	RESERVED0
4	DESCRIPTOR_ERROR_INTERRUPT_ENABLE
3	FIFO_ERROR_INTERRUPT_ENABLE
2	INTERRUPT_ON_COMPLETION_ENABLE
1	STREAM_RUN
0	STREAM_RESET

Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For input streams the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an input stream this indicates a FIFO overrun occurring while the RUN bit is set. When this happens the FIFO pointers don t increment and the incoming data is not written into the FIFO thereby being lost.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved

Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When an input stream is detected on any of the SDIx signals that match this value the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number two different SDIx inputs may not be configured with the same stream number. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** This field is meaningless for input streams.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error overrun for input will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

20.6.63 ISD3LPIB—Offset E4h

Input Stream Descriptor 3 Link Position in Buffer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD3LPIB: [AZLBAR] + E4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.64 ISD3CBL—Offset E8h

Input Stream Descriptor 3 Cyclic Buffer Length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD3CBL: [AZLBAR] + E8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CYCLIC_BUFFER_LENGTH

Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

20.6.65 ISD3LVI—Offset ECh

Input Stream Descriptor 3 Last Valid Index

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD3LVI: [AZLBAR] + ECh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0								LAST_VALID_INDEX							

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1 i.e. there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

20.6.66 ISD3FIFOW—Offset EEh

Input Stream Descriptor 3 FIFO Eviction Watermark

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD3FIFOW: [AZLBAR] + EEh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RESERVED0													FIFO_WATERMARK		

Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes accumulated in the FIFO before the controller will start an eviction of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For input streams the FIFOW value is determined by the EM3.ISRWS SEM3.ISRWS field.

20.6.67 ISD3FIFOS—Offset F0h

Input Stream Descriptor 3 FIFO Size

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD3FIFOS: [AZLBAR] + F0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIFO_SIZE (bits 15:0)

Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be revicted by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA d into memory and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in ISD3FMT register. As the default value is zero, SW must write to the respective ISD3FMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

20.6.68 ISD3FMT—Offset F2h

Input Stream Descriptor 3 Format

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

ISD3FMT: [AZLBAR] + F2h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULTIPLE			SAMPLE_BASE_RATE_DIVISOR			RESERVED1	BITS_PER_SAMPLE			NUMBER_OF_CHANNELS			

Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** 0 48 kHz 1 44.1 kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

20.6.69 ISD3BDLPLBA—Offset F8h

Input Stream Descriptor 3 Buffer Descriptor List Pointer Lower Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD3BDLPLBA: [AZLBAR] + F8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS

RESERVED0

PROTECT

Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

20.6.70 ISD3BDLPUBA—Offset FCh

Input Stream Descriptor 3 Buffer Descriptor List Pointer Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD3BDLPUBA: [AZLBAR] + FCh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

20.6.71 OSD0CTL_STS—Offset 100h

Output Stream Descriptor 0 Control and status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD0CTL_STS: [AZLBAR] + 100h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED1		FIFO_READY	DESCRIPTOR_ERROR	FIFO_ERROR	BUFFER_COMPLETION_INTERRUPT_STATUS	RESERVED2		STREAM_NUMBER				BIDIRECTIONAL_DIRECTION_CONTROL	TRAFFIC_PRIORITY	STRIPE_CONTROL					RESERVED0								DESCRIPTOR_ERROR_INTERRUPT_ENABLE	FIFO_ERROR_INTERRUPT_ENABLE	INTERRUPT_ON_COMPLETION_ENABLE	STREAM_RUN	STREAM_RESET

Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For output streams the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link it will have this stream number encoded on the SYNC signal. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in the HD Audio controller. Therefore it is hardwired to 0 s.
15:5	000h RO	**RESERVED0:** reserved

Bit Range	Default & Access	Description
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error under run for output will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

20.6.72 OSD0LPIB—Offset 104h

Output Stream Descriptor 0 Link Position in Buffer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD0LPIB: [AZLBAR] + 104h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.73 OSD0CBL—Offset 108h

Output Stream Descriptor 0 Cyclic Buffer Length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD0CBL: [AZLBAR] + 108h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CYCLIC_BUFFER_LENGTH																															

Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

20.6.74 OSD0LVI—Offset 10Ch

Output Stream Descriptor 0 Last Valid Index

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD0LVI: [AZLBAR] + 10Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0								LAST_VALID_INDEX							

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1 i.e. there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

20.6.75 OSD0FIFOW—Offset 10Eh

Output Stream Descriptor 0 FIFO Fetch Watermark

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD0FIFOW: [AZLBAR] + 10Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RESERVED0													FIFO_WATERMARK		

Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes free in the FIFO before the controller will start a fetch of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For output streams the FIFOW value is determined by the EM4.OSRWS SEM4.OSRWS field.

20.6.76 OSD0FIFOS—Offset 110h

Output Stream Descriptor 0 FIFO Size

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD0FIFOS: [AZLBAR] + 110h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIFO_SIZE

Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA d into memory but not yet transmitted on the link and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in OSD0FMT register. As the default value is zero, SW must write to the OSD0FMT register to kick of the FIFO size calculation and read back to find out the HW allocated FIFO size.

20.6.77 OSD0FMT—Offset 112h

Output Stream Descriptor 0 Format

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD0FMT: [AZLBAR] + 112h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED0 | SAMPLE_BASE_RATE | SAMPLE_BASE_RATE_MULTIPLE | SAMPLE_BASE_RATE_DIVISOR | RESERVED1 | BITS_PER_SAMPLE | NUMBER_OF_CHANNELS

Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved

Bit Range	Default & Access	Description
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

20.6.78 OSD0BDLPLBA—Offset 118h

Output Stream Descriptor 0 Buffer Descriptor List Pointer Lower Base Address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD0BDLPLBA: [AZLBAR] + 118h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS (bits 31:7), RESERVED0 (bits 6:1), PROTECT (bit 0)

Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

20.6.79 OSD0BDLPUBA—Offset 11Ch

Output Stream Descriptor 0 Buffer Descriptor List Pointer Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD0BDLPUBA: [AZLBAR] + 11Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

20.6.80 OSD1CTL_STS—Offset 120h

Output Stream Descriptor 1 Control and status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD1CTL_STS: [AZLBAR] + 120h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:30	RESERVED1
29	FIFO_READY
28	DESCRIPTOR_ERROR
27	FIFO_ERROR
26	BUFFER_COMPLETION_INTERRUPT_STATUS
25:24	RESERVED2
23:20	STREAM_NUMBER
19	BIDIRECTIONAL_DIRECTION_CONTROL
18	TRAFFIC_PRIORITY
17:16	STRIPE_CONTROL
15:5	RESERVED0
4	DESCRIPTOR_ERROR_INTERRUPT_ENABLE
3	FIFO_ERROR_INTERRUPT_ENABLE
2	INTERRUPT_ON_COMPLETION_ENABLE
1	STREAM_RUN
0	STREAM_RESET

Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For output streams the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved

Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link it will have this stream number encoded on the SYNC signal. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in the HD Audio controller. Therefore it is hardwired to 0 s.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error under run for output will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

20.6.81 OSD1LPIB—Offset 124h

Output Stream Descriptor 1 Link Position in Buffer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD1LPIB: [AZLBAR] + 124h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.82 OSD1CBL—Offset 128h

Output Stream Descriptor 1 Cyclic Buffer Length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD1CBL: [AZLBAR] + 128h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CYCLIC_BUFFER_LENGTH

Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

20.6.83 OSD1LVI—Offset 12Ch

Output Stream Descriptor 1 Last Valid Index

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD1LVI: [AZLBAR] + 12Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0								LAST_VALID_INDEX							

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1 i.e. there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

20.6.84 OSD1FIFOW—Offset 12Eh

Output Stream Descriptor 1 FIFO Fetch Watermark

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD1FIFOW: [AZLBAR] + 12Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RESERVED0													FIFO_WATERMARK		

Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes free in the FIFO before the controller will start a fetch of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For output streams the FIFOW value is determined by the EM4.OSRWS SEM4.OSRWS field.

20.6.85 OSD1FIFOS—Offset 130h

Output Stream Descriptor 1 FIFO Size

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD1FIFOS: [AZLBAR] + 130h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FIFO_SIZE															

Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA d into memory but not yet transmitted on the link and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in OSD1FMT register. As the default value is zero, SW must write to the OSD1FMT register to kick of the FIFO size calculation and read back to find out the HW allocated FIFO size.

20.6.86 OSD1FMT—Offset 132h

Output Stream Descriptor 1 Format

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD1FMT: [AZLBAR] + 132h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULTIPLE			SAMPLE_BASE_RATE_DIVISOR			RESERVED1	BITS_PER_SAMPLE			NUMBER_OF_CHANNELS			

Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

20.6.87 OSD1BDLPLBA—Offset 138h

Output Stream Descriptor 1 Buffer Descriptor List Pointer Lower Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD1BDLPLBA: [AZLBAR] + 138h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:7	Bits 6:1	Bit 0
BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS	RESERVED0	PROTECT

Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

20.6.88 OSD1BDLPUBA—Offset 13Ch

Output Stream Descriptor 1 Buffer Descriptor List Pointer Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD1BDLPUBA: [AZLBAR] + 13Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

20.6.89 OSD2CTL_STS—Offset 140h

Output Stream Descriptor 2 Control and status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD2CTL_STS: [AZLBAR] + 140h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	RESERVED1		FIFO_READY	DESCRIPTOR_ERROR	FIFO_ERROR	BUFFER_COMPLETION_INTERRUPT_STATUS	RESERVED2		STREAM_NUMBER				BIDIRECTIONAL_DIRECTION_CONTROL	TRAFFIC_PRIORITY	STRIPE_CONTROL		RESERVED0											DESCRIPTOR_ERROR_INTERRUPT_ENABLE	FIFO_ERROR_INTERRUPT_ENABLE	INTERRUPT_ON_COMPLETION_ENABLE	STREAM_RUN	STREAM_RESET

Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For output streams the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link it will have this stream number encoded on the SYNC signal. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in the HD Audio controller. Therefore it is hardwired to 0 s.
15:5	000h RO	**RESERVED0:** reserved

Bit Range	Default & Access	Description
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error under run for output will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

20.6.90 OSD2LPIB—Offset 144h

Output Stream Descriptor 2 Link Position in Buffer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD2LPIB: [AZLBAR] + 144h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.91 OSD2CBL—Offset 148h

Output Stream Descriptor 2 Cyclic Buffer Length

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD2CBL: [AZLBAR] + 148h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CYCLIC_BUFFER_LENGTH

Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

20.6.92 OSD2LVI—Offset 14Ch

Output Stream Descriptor 2 Last Valid Index

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD2LVI: [AZLBAR] + 14Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0								LAST_VALID_INDEX							

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1 i.e. there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

20.6.93 OSD2FIFOW—Offset 14Eh

Output Stream Descriptor 2 FIFO Fetch Watermark

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD2FIFOW: [AZLBAR] + 14Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RESERVED0													FIFO_WATERMARK		

Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved

Bit Range	Default & Access	Description
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes free in the FIFO before the controller will start a fetch of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For output streams the FIFOW value is determined by the EM4.OSRWS SEM4.OSRWS field.

20.6.94 OSD2FIFOS—Offset 150h

Output Stream Descriptor 2 FIFO Size

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD2FIFOS: [AZLBAR] + 150h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FIFO_SIZE															

Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA d into memory but not yet transmitted on the link and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in OSD2FMT register. As the default value is zero, SW must write to the OSD2FMT register to kick of the FIFO size calculation and read back to find out the HW allocated FIFO size.

20.6.95 OSD2FMT—Offset 152h

Output Stream Descriptor 2 Format

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD2FMT: [AZLBAR] + 152h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULTIPLE			SAMPLE_BASE_RATE_DIVISOR			RESERVED1	BITS_PER_SAMPLE			NUMBER_OF_CHANNELS			

Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

20.6.96 OSD2BDLPLBA—Offset 158h

Output Stream Descriptor 2 Buffer Descriptor List Pointer Lower Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD2BDLPLBA: [AZLBAR] + 158h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS

RESERVED0

PROTECT

Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

20.6.97 OSD2BDLPUBA—Offset 15Ch

Output Stream Descriptor 2 Buffer Descriptor List Pointer Upper Base Address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD2BDLPUBA: [AZLBAR] + 15Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

20.6.98 OSD3CTL_STS—Offset 160h

Output Stream Descriptor 3 Control and status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD3CTL_STS: [AZLBAR] + 160h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RESERVED1	FIFO_READY	DESCRIPTOR_ERROR	FIFO_ERROR	BUFFER_COMPLETION_INTERRUPT_STATUS	RESERVED2	STREAM_NUMBER	BIDIRECTIONAL_DIRECTION_CONTROL	TRAFFIC_PRIORITY	STRIPE_CONTROL	RESERVED0	DESCRIPTOR_ERROR_INTERRUPT_ENABLE	FIFO_ERROR_INTERRUPT_ENABLE	INTERRUPT_ON_COMPLETION_ENABLE	STREAM_RUN	STREAM_RESET

Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For output streams the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link it will have this stream number encoded on the SYNC signal. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in the HD Audio controller. Therefore it is hardwired to 0 s.
15:5	000h RO	**RESERVED0:** reserved

Bit Range	Default & Access	Description
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error under run for output will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

20.6.99 OSD3LPIB—Offset 164h

Output Stream Descriptor 3 Link Position in Buffer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD3LPIB: [AZLBAR] + 164h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.100 OSD3CBL—Offset 168h

Output Stream Descriptor 3 Cyclic Buffer Length

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD3CBL: [AZLBAR] + 168h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CYCLIC_BUFFER_LENGTH

Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

20.6.101 OSD3LVI—Offset 16Ch

Output Stream Descriptor 3 Last Valid Index

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD3LVI: [AZLBAR] + 16Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0								LAST_VALID_INDEX							

Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1 i.e. there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

20.6.102 OSD3FIFOW—Offset 16Eh

Output Stream Descriptor 3 FIFO Fetch Watermark

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD3FIFOW: [AZLBAR] + 16Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RESERVED0													FIFO_WATERMARK		

Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes free in the FIFO before the controller will start a fetch of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For output streams the FIFOW value is determined by the EM4.OSRWS SEM4.OSRWS field.

20.6.103 OSD3FIFOS—Offset 170h

Output Stream Descriptor 3 FIFO Size

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD3FIFOS: [AZLBAR] + 170h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIFO_SIZE

Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA d into memory but not yet transmitted on the link and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in OSD3FMT register. As the default value is zero, SW must write to the OSD3FMT register to kick of the FIFO size calculation and read back to find out the HW allocated FIFO size.

20.6.104 OSD3FMT—Offset 172h

Output Stream Descriptor 3 Format

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

OSD3FMT: [AZLBAR] + 172h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED0	SAMPLE_BASE_RATE	SAMPLE_BASE_RATE_MULTIPLE			SAMPLE_BASE_RATE_DIVISOR			RESERVED1	BITS_PER_SAMPLE			NUMBER_OF_CHANNELS			

Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

20.6.105 OSD3BDLPLBA—Offset 178h

Output Stream Descriptor 3 Buffer Descriptor List Pointer Lower Base Address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD3BDLPLBA: [AZLBAR] + 178h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

Bits	31:7	6:1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0
Field	BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS	RESERVED0	PROTECT

Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

20.6.106 OSD3BDLPUBA—Offset 17Ch

Output Stream Descriptor 3 Buffer Descriptor List Pointer Upper Base Address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD3BDLPUBA: [AZLBAR] + 17Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS

Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

20.6.107 WLCLKA—Offset 2030h

Wall Clock Alias

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

WLCLKA: [AZLBAR] + 2030h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WALL_CLOCK_COUNTER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**WALL_CLOCK_COUNTER_ALIAS:** This is an alias of the WALCK register. 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

20.6.108 ISD0LPIBA—Offset 2084h

Input Stream Descriptor 0 Link Position in Buffer Alias

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD0LPIBA: [AZLBAR] + 2084h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.109 ISD1LPIBA—Offset 20A4h

Input Stream Descriptor 1 Link Position in Buffer Alias

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD1LPIBA: [AZLBAR] + 20A4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.110 ISD2LPIBA—Offset 20C4h

Input Stream Descriptor 2 Link Position in Buffer Alias

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD2LPIBA: [AZLBAR] + 20C4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.111 ISD3LPIBA—Offset 20E4h

Input Stream Descriptor 3 Link Position in Buffer Alias

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ISD3LPIBA: [AZLBAR] + 20E4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.112 OSD0LPIBA—Offset 2104h

Output Stream Descriptor 0 Link Position in Buffer Alias

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD0LPIBA: [AZLBAR] + 2104h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.113 OSD1LPIBA—Offset 2124h

Output Stream Descriptor 1 Link Position in Buffer Alias

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD1LPIBA: [AZLBAR] + 2124h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.114 OSD2LPIBA—Offset 2144h

Output Stream Descriptor 2 Link Position in Buffer Alias

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD2LPIBA: [AZLBAR] + 2144h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

20.6.115 OSD3LPIBA—Offset 2164h

Output Stream Descriptor 3 Link Position in Buffer Alias

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OSD3LPIBA: [AZLBAR] + 2164h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LINK_POSITION_IN_BUFFER_ALIAS

Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

21 Low Power Engine (LPE) for Audio (I^2S)

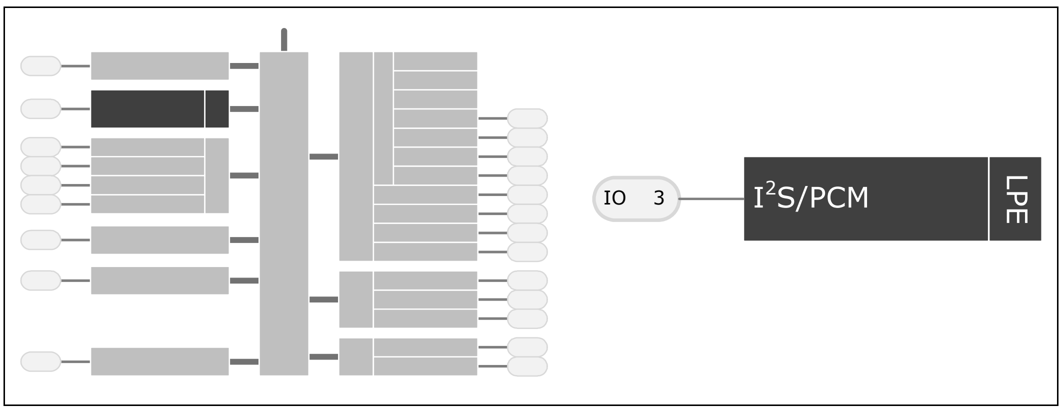
The Low Power Engine for Audio provides acceleration for common audio and voice functions. The voice and audio engine provides a mechanism for rendering audio and voice streams and tones from the operating system, applications to an audio or voice codec, and ultimately to the speaker, headphones, or Bluetooth headsets.

Audio streams in the SoC can be encoded and decoded by the Low Power Engine (LPE) in the Audio subsystem.

LPE Audio provides three external I^2S audio interfaces.

Note: LPE_I2S[1:0] are multiplexed on the same balls as High Definition Audio.

Note: When LPE is active, the High Definition Audio functionality is disabled.



21.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 226. LPE Signals

Signal Name	Direction Plat. Power	Description
LPE_I2S2[0:2]_CLK	I/O V1P8S	Clock signal for I^{2}S
LPE_I2S2[0:2]_FRM	I/O V1P8S	Frame select signal for I^{2}S
LPE_I2S2[0:2]_DATAIN	I V1P8S	RX data for I^{2}S
LPE_I2S2[0:2]_DATAOUT	O V1P8S	TX data for I^{2}S

† All LPE signals are muxed and may be used by other functions.

21.2 Features

The LPE Audio Subsystem consists of the following:

- Integrated, power-efficient 32-bit architecture core with 24-bit audio processing instructions
- Core processing speeds up to 343 MHz
- Closely Coupled Memories (CCMs)
  - 80KB Instruction RAM
  - 160KB Data RAM
  - 48KB Instruction Cache
  - 96KB Data Cache
- Very low-power consumption coupled with high-fidelity 24-bit audio
- Dual-issue, static, super-scalar VLIW processing engine
- Mode-less switching between 16-, 24-, and 64-bit dual-issue instructions
- Dual MACs which can operate with 32 x 16-bit and/or 24 x 24-bit operands
- Inter-Process Communication (IPC) mechanism to communicate with the SoC Processor Core including 4KB mailbox memory
- Flexible audio interfaces include three SSPs with I^{2}S port functionality for I-directional audio transfers
  - I^{2}S mode supports PCM payloads
  - Frame counters for all I^{2}S ports
- High Performance DMA
  - DMA IP to support multiple outstanding transactions
  - Interleaved scatter-gather support for Audio DMA transfers
- Clock switching logic including new frequency increments

- External timer function with an always running clock.

The LPE core runs at a peak clock frequency of 343 MHz and has dedicated on-chip program and data memories and caches. The LPE core can access shared SRAM blocks, and external DRAM through OCP fabric. It communicates with audio peripherals using the audio sub-fabric, and employs Inter-Processor Communication (IPC) mechanism to communicate with the SoC Processor Core.

The Audio subsystem includes two OCP-based DMA engines. These DMA engines support single and multi-block transfers. They can be configured to transfer data between DRAM and audio CCMs or transfer data between CCMs and the audio peripheral interfaces

All these interfaces are peripherals in the Audio subsystem. LPE, LPE DMA, or the SoC processor core may access the peripherals during normal operation. The PMC may access all peripherals during specific tasks such as at boot time or during power state changes.A complete audio solution based on an internal audio processing engine which includes several I^2S-based output ports.

The audio core used is a dedicated audio DSP core designed specifically for audio processing (decoding, post-processing, mixing, etc.)

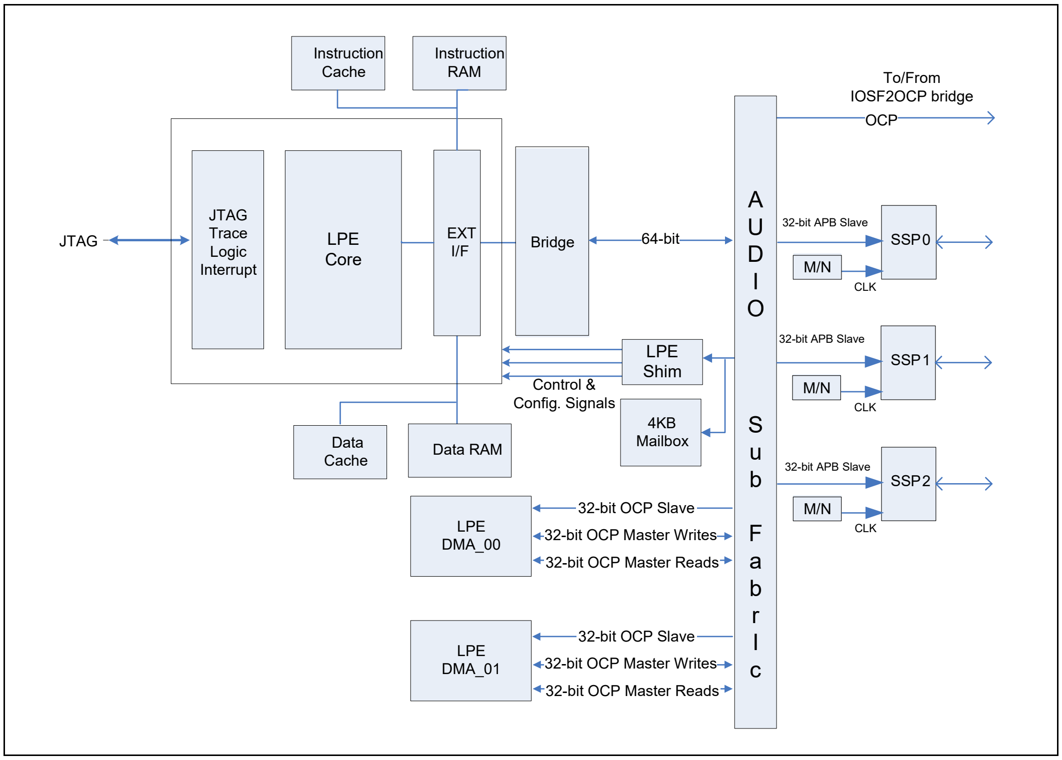
Note: LPE requires systems with more than 512MB memory. This is required since the LPE firmware must reside at a stolen memory location on 512MB boundaries below 3 GiB. The LPE firmware itself is ~1MB, and is reserved by BIOS for LPE use.

21.3 Detailed Block Level Description

21.3.1 LPE Core

The LPE core in the SoC runs at maximum frequency of 343 MHz and interfaces with the rest of the SoC system through the OCP bus. It is one of the masters on the Audio Sub-Fabric The SoC Processor Core and LPE DMA engines are the other masters on the fabric. The following figure shows the LPE core and its interfaces.

Figure 106.Audio Cluster Block Diagram

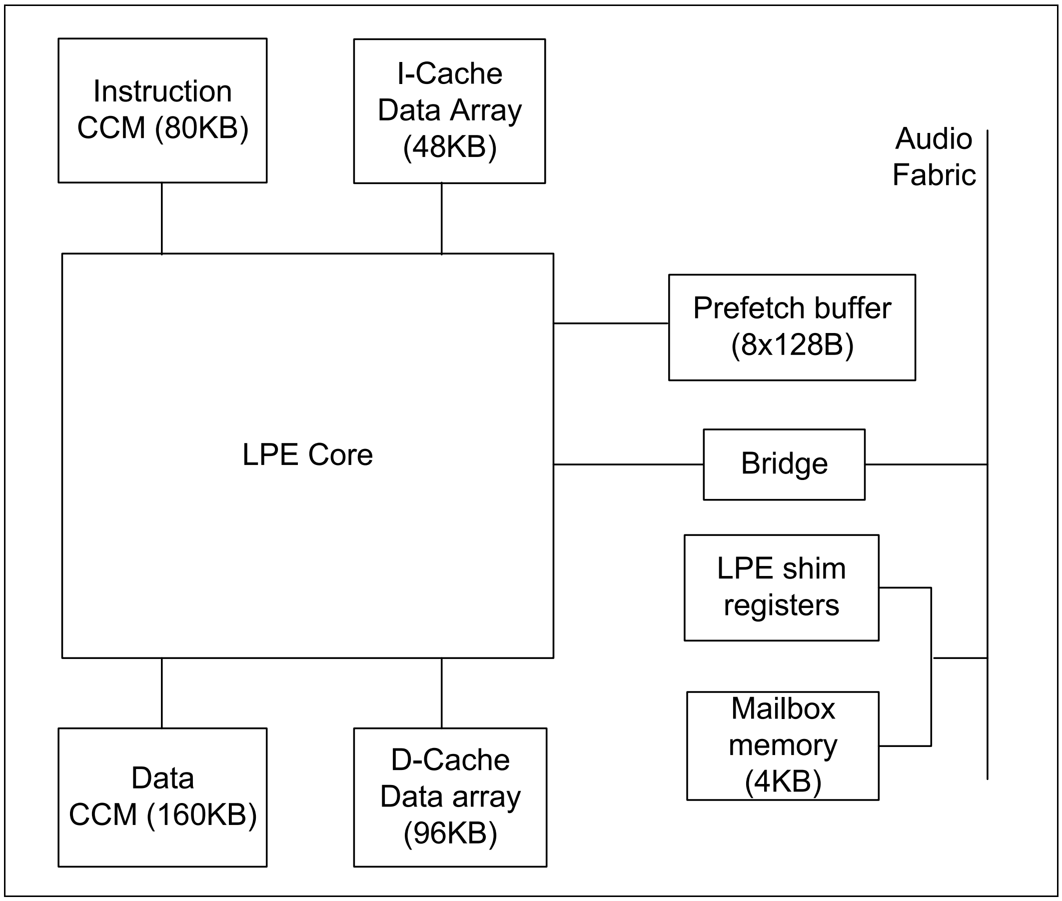


The main DSP hardware is a two-multiplier, multiply/accumulate unit, a register file LPE_PR to hold pairs of 24-bit data items, a register file LPE-OR to hold 56-bit accumulator values, an arithmetic/logic unit to operate on the LPE_PR and LPE_OR values, and a shift unit to operate on the LPE_PR and LPE_OR values. The multiply/ accumulate unit also supports multiplication of 32-bit values from LPE_OR registers by 16-bit values from LPE_PR registers, with the 48-bit result written or accumulated in the LPE_OR register. The instructions for the DSP subsystems are built from operations that are divided into two sets: the slot 0 set and the slot 1 set. In each execution cycle, zero or one operations from each set can be executed independently according to the static bundling expressed in the machine code.

21.3.2 Memory Architecture

The LPE core is configured to use local memory and local caches. It has 80KB of Instruction Closely Coupled Memory (CCM), 160KB of Data CCM, 48KB of Instruction Cache and 96KB of Data Cache. The LPE core also has access to 4KB of mailbox memory and external DRAM.

Figure 107. Memory Connections for LPE



21.3.3 Instruction Closely Coupled Memory (CCM)

Instruction CCM for the core is used for loading commonly used routines as well as time-critical processing. Examples of time critical processing are acoustic echo cancellation and noise cancellation during voice calls.

Instruction CCM is initialized after reset by an external DMA controller. Runtime update of instruction CCM can be done either using explicit instructions or using an external DMA controller with inbound access.

21.3.4 Data Closely Coupled Memory (CCM)

Data CCM can be initialized after reset by an external DMA controller using inbound access. Runtime update of data CCM can be done either using stores to Data CCM or using an external DMA controller with inbound access.

21.3.5 Mailbox Memory and Data Exchange

The mailbox memory is a shared memory region in LPE address space that is accessible by the SOC Processor Core, PMC, and LPE. It is used when Doorbell registers cannot hold all the information that one processor wishes to communicate to the other. A typical example of such data blocks are audio stream related parameters when starting a new stream. The structures of data communicated through the mailbox are not defined in hardware so that software may partition the mailbox memory in any desired way and create any meaningful structures required.

21.4 Software Implementation Considerations

21.4.1 SoC Processor Core Cache Coherence

Traffic generated by the LPE core is considered non-cacheable and non-coherent with respect to the SoC Processor Core cache. DMA traffic is considered cacheable and checked for coherency with the SoC Processor Core cache.

Implications of this implementation are as follows:

- All code and tables for the LPE core need to be explicitly flushed from the SoC Processor Core cache if they are ever accessed.
- If the LPE core directly accesses data buffers in system DDR, the driver must explicitly flush the buffer from the SoC Processor Core cache
- If DMA accesses data buffers from system DRAM, the driver need not flush the data buffer from the SoC Processor Core cache.

21.4.2 Interrupts

21.4.2.1 LPE Peripheral Interrupts

Each of the LPE peripherals generates its own interrupts. SSP0, SSP1, and SSP2 have one interrupt each. Each of the DMA channels have individual interrupt lines. These interrupts are connected to the LPE core through the PISR register. The same interrupts are routed to IOAPIC through the ISRX register. The LPE core and SoC Processor Core have individual masks to enable these interrupts.

21.4.2.2 Interrupts Between SoC Processor Core and the LPE

The interrupts between the SoC Processor Core and the LPE are handled through the inter-processor communication registers. Whenever the SoC Processor Core writes to the IPCX communication register an interrupt is generated to the LPE. The LPE firmware sees there is a message waiting from the SoC Processor Core, and reads the IPCX register for the data. This data is a pre-configured message, where the message structure has been decided beforehand between the SoC Processor Core and the LPE. Similarly we have the IPCD register for the communication between the LPE and SoC Processor Core. Once the LPE writes to the IPCD register, an interrupt should be generated for the SoC Processor Core and the SoC Processor Core should read the message from the IPCD register and act accordingly. From a software viewpoint, the mechanism remains the same as before. From a hardware view point, the interrupt to IA-32 gets routed by means of the IOAPIC block. The IPC from Audio to SoC Processor Core gets a dedicated interrupt line to the IOAPIC.

21.4.2.3 Interrupts between PMC and LPE

The interrupts between PMC and LPE are also handled using Inter Process Communication registers.

21.4.3 Power Management Options for the LPE Core

- WAITI
  - Allows the LPE core to suspend operation until an interrupt occurs by executing the optional WAITI instruction.
- External Run/Stall Control Signal
  - This processor input allows external logic to stall large portions of the LPE pipeline by shutting off the clock to much of the processor's logic to reduce operating power when the LPE computational capabilities are not immediately needed by the system.

Note: Using the WAITI instruction to power down the processor will save more power than use of the external run/stall signal because the WAITI instruction disables more of the LPE’s internal clocks.

21.4.4 External Timer

This timer always runs from SSP clock (before M/N divider) at 19.2/25MHz. The timer starts running once the run bit (refer to the External timer register definition for details) is set and the clear bit is cleared.

The timer generates an Interrupt pulse when the counter value matches the "match" value. The interrupt does not get generated if the match value is set to "0". The timer runs in free running mode and rolls over after all 32 bits have become all 1's.

The timer continues to run as long as the run bit is set. Once the run bit is cleared the timer holds the current value. The clear bit needs to be set to restart the timer from "0".

21.5 Clocks

21.5.1 Clock Frequencies

Table 227 shows the clock frequency options for the Audio functional blocks.

Table 227. Clock Frequencies

Clock	Frequency	Notes
Audio core	25/50/100/200/267/343 MHz	Audio input clock trunk. CCU drives one of several frequencies as noted.
DMA 0	25/50 MHz	DMA clock
DMA1	25/50 MHz	DMA clock
Audio fabric clock	25/50 MHz	Fabric clock derived from audio core clock
SSP0 Clock	Fabric side: 25/50 MHz Link side: Up to 19.2/25 MHz	SSP0 clock domains
SSP1 Clock	Fabric side: 25/50 MHz Link side: Up to 19.2/25 MHz	SSP1 clock domains
SSP2 Clock	Fabric side: 25/50 MHz Link side: Up to 19.2/25 MHz	SSP2 clock domains

21.5.2 50 MHz Clock for LPE

50 MHz, the 2X OSC clock, is added to increase MIPS for low power MP3 mode. This frequency will be supplied by the clock doubler internal to the SoC's Clock Control Unit.

21.5.3 Cache and CCM Clocking

Data CCM, Data cache, Instruction CCM, and Instruction Cache run off of the LPE clock. These memories are in a single clock domain.

Note: All Data CCM and Instruction CCM run in the same clock domain.

21.5.4 SSP Clocking

SSP could be used as either clock masters or clock slaves. Consequently, theses IP have dual clock domains.

The first clock domain is clocked from an internal clock (e.g., fabric clock) and is used for generic logic like interrupt generation and register access.

The second clock domain drives the serial shift register (either driven internally or externally). When driven internally, this clock can be sourced from XTAL clock 25 MHz or PLL 19.2 MHz. These clocks are then divided down within the serial interface IP to generate the final bit clock for the interface.

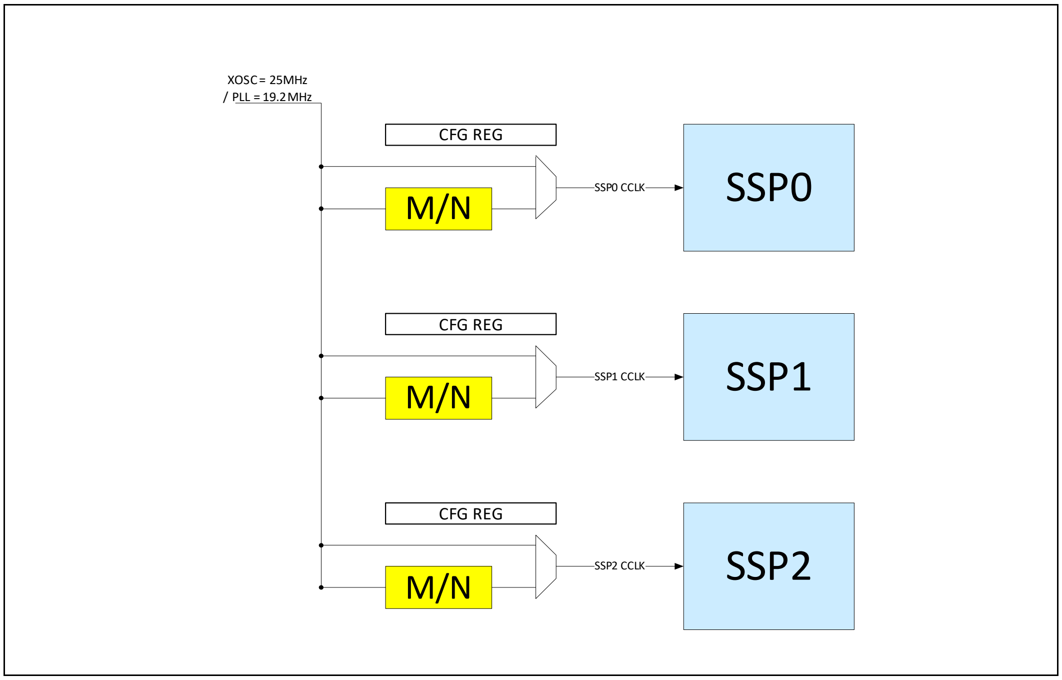
After power on, if the SSP input IO clock is in high state, first transition of the clock from high to low may be missing due to the Soc clock gating logic.

Note: "Frame Master" mode cannot be used when operating as clock slave and "Frame Slave" mode cannot be used when operating as clock master.

21.5.5 M/N Divider

LPE SSP in master mode uses the SSP CCLK to drive the serial clock. It has very limited option to divide CCLK. An M/N divider is added between the 19.2/25 MHz clock (XOSC) from CCU to each SSP CCLK input as shown in following diagram:

Figure 108.SSP CCLK Structure



Note: The maximum SSP CCLK frequency is listed in Table 132.

The LPE M/N divider is designed to produce a clock signal for the SSP block used in master mode. The divider is based on a generic NOM/DENOM divider. The supplied Master clock is 25 MHz (XTAL) or 19.2 MHz (LPPLL), but usually be used by the 25 MHz clock.

This mechanism is good for a wide spectrum of generated clocks. Two registers must be configured to get the target SSP clock. The values for the Nominator and Denominator registers are the smallest divider of:

$$\frac{Nominator}{Denominator} = \frac{Source\_clock}{Target\_clock}$$

21.5.5.1 Example

If we want to generate 17.64 MHz (=400x44.1 KHz) output clock out of 25 MHz clock, we need to program "NOM = 441" and "DENOM = 625":

17.64 MHz = (441/625) x 25 MHz

In general the M over N can generate fractional devisor that could be used for generating the required clocks for Audio codec. Table 228 describes some configuration options of this generic divider:

Table 228. M/N Values, Examples

Source Clock Frequency	Requested Clock	M/N Value
25 MHz	48 KHz	6/3125
	48K x 24 = 1.152 MHz	1152/25000
	48K x32 = 1.536 MHz	1536/25000
	48K x 64 = 3.072 MHz	3072/25000
	44.1 KHz	441/250000
	48K x 400 = 19.2 MHz	96/125
	44.1K x 400 = 17.64 MHz	441/625

21.5.5.2 Accuracy and Jitter

The output of the M/N is equal to the desired clock in average with Jitter of 20nTXE for 25 MHz input clock.

21.5.5.3 Configuration

Following configurable fields per M/N divider/SSP are in LPE shim registers:

Table 229. M/N Configurable Fields

Field	Width	Description
Bypass	1 bit	When set M/N divider is bypass. Clock from CCU is connected directly to SSP CCLK
EN	1 bit	Enable the divider
Update	1 bit	Update divider parameters
M Value	20 bits	Nominator value
N Value	20 bits	Denominator value

21.6 SSP (I^2S)

The SoC audio subsystem consists of the LPE Audio Engine and three Synchronous Serial Protocol (SSP) ports. These ports are used in PCM mode and enable simultaneous support of voice and audio streams over I^2S. The SoC audio subsystem also includes two DMA controllers dedicated to the LPE. The LPE DMA controllers are used for transferring data between external memory and CCMs, between CCMs and the SSP ports, and between CCMs. All peripheral ports can operate simultaneously.

21.6.1 Introduction

The Enhanced SSP Serial Ports are full-duplex synchronous serial interfaces. They can connect to a variety of external analog-to-digital (A/D) converters, audio, and telecommunication codecs, and many other devices which use serial protocols for transferring data. Formats supported include National* Microwire, Texas Instruments* Synchronous Serial Protocol (SSP), Motorola* Serial Peripheral Interface (SPI) protocol and a flexible Programmable Serial Port protocol (PSP).

The Enhanced SSPs operate in master mode (the attached peripheral functions as a slave) or slave mode (the attached peripheral functions as a master), and support serial bit rates from 0 to 25 Mbps, dependent on the input clock. Serial data formats range from 4 to 32-bits in length. Two on-chip register blocks function as independent FIFOs for transmit and receive data.

FIFOs may be loaded or emptied by the system processor using single transfers or DMA burst transfers of up to the FIFO depth. Each 32-bit word from the bus fills one entry in a FIFO using the lower significant bits of a 32-bit word.

21.6.2 SSP Features

The SSP port features are:

- Inter-IC Sound (I^2S) protocols, are supported by programming the Programmable Serial Protocol (PSP).
- One FIFO for transmit data (TXFIFO) and a second, independent, FIFO for receive data (RXFIFO), where each FIFO is 16 samples deep x 32 bits wide
- Data sample sizes from 8, 16, 18 and 24bits

- 12.5 Mbps maximum serial bit-rate in both modes: master and slave.
- Clock master or slave mode operations
- Receive-without-transmit operation
- Network mode with up to eight time slots for PSP formats, and independent transmit/receive in any/all/none of the time slots.
- After updating SSP configuration, for example active slot count, the SSP will need to be disabled and enabled again. In other words, a SSP will not function correctly if a user changes the configuration setting on the fly.

21.6.3 Operation

Serial data is transferred between the LPE core or the SoC Processor Core and an external peripheral through FIFOs in one of the SSP ports. Data transfers between an SSP port and memory are initiated by either the LPE core or the SoC Processor Core using programmed I/O, or by DMA bursts. Although it is possible to initiate transfers directly from the SoC Processor Core, current driver design uses LPE for all PCM operations. Separate transmit and receive FIFOs and serial data paths permit simultaneous transfers in both directions to and from the external peripheral, depending on the protocols chosen.

Programmed I/O can transfer data between:

- The LPE core and the FIFO Data register for the TXFIFO
- The SoC Processor Core and the FIFO Data register for the TXFIFO
- The LPE core and the FIFO Data register for the RXFIFO
- The SoC Processor Core and the FIFO Data register for the RXFIFO
- The SoC Processor Core and the control or status registers
- The LPE core and the control or status registers

DMA bursts can transfer data between:

- Universal memory and the FIFO Data register for the TXFIFO
- Universal memory and the FIFO Data register for the RXFIFO
- Universal memory and the sequentially addressed control or status registers

21.6.4 LPE and DMA FIFO Access

The LPE or DMA access data through the Enhanced SSP Port's Transmit and Receive FIFOs. An LPE access takes the form of programmed I/O, transferring one FIFO entry per access. LPE accesses would normally be triggered off of an SSSR Interrupt and must always be 32 bits wide. LPE Writes to the FIFOs are 32 bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (EDSS/DSS value). LPE Reads to the FIFOs are also 32 bits wide, but the Receive data written into the RX FIFO (from the RXD line) is stored with zeroes in the MSBs down to the programmed data size. The FIFOs can also be accessed by DMA bursts, which must be in multiples of 1, 2 or 4 bytes, depending upon the EDSS value, and must also transfer one FIFO entry per access. When the SSCR0.EDSS bit is set, DMA bursts must be in multiples of 4 bytes (the DMA must have the Enhanced SSP configured as a 32-bit peripheral).The DMA's width register must be at least the SSP data size programmed into the SSP control registers EDSS and DSS. The FIFO is seen as one 32-bit location by the processor. For Writes, the Enhanced SSP port takes the data from the Transmit FIFO, serializes it, and sends it over the serial wire (I2S[2:0]_DATAOUT) to the external peripheral. Receive data from the external peripheral (on I2S[2:0]_DATAIN) is converted to parallel words and stored in the Receive FIFO.

A programmable FIFO trigger threshold, when exceeded, generates an Interrupt or DMA service request that, if enabled, signals the CPU or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO.

The Transmit and Receive FIFOs are differentiated by whether the access is a Read or a Write transfer. Reads automatically target the Receive FIFO, while Writes will write data to the Transmit FIFO. From a memory-map perspective, they are at the same address. FIFOs are 16 samples deep by 32 bits wide. Each read or write is to 1 SSP sample.

21.6.5 Supported Formats

The SSP consists of four pins that are used to transfer data between the SoC and external Audio codecs, modems, or other peripherals. Although four serial-data formats exist, each has the same basic structure, and in all cases the following pins are used in the following manner:

- I2Sx_CLK—Defines the bit rate at which serial data is driven onto and sampled from the port
- I2Sx_FRM—Defines the boundaries of a basic data "unit," comprised of multiple serial bits
- I2Sx_DATAIN—The serial data path for transmitted data, from system to peripheral
- I2Sx_DATAOUT—The serial data path for received data, from peripheral to system

A data frame can contain from 4 to 32 bits, depending on the selected format. Serial data is transmitted most significant bit first. The Programmable Serial Protocol (PSP) format is used to implement I^{2}S.

Master and Slave modes are supported. When driven by the Enhanced SSP, the I2Sx_CLK only toggles during active transfers (not continuously) unless ECRA/ECRB functions are used. When the I2Sx_CLK is driven by another device, it is allowed to be either continuous or only driven during transfers, but certain restrictions on PSP parameters apply.

Normally, the serial clock (I2Sx_CLK), if driven by the Enhanced SSP Port, only toggles while an active data transfer is underway. There are several conditions, however, that may cause the clock to run continuously. If the Receive With Out Transmit mode is enabled by setting the SSCR1.RWOT bit to 1, the I2Sx_CLK will toggle regardless of whether Transmit data exists within the Transmit FIFO. The I2Sx_CLK will also toggle continuously if the Enhanced SSP is in Network mode, or if ECRA, or ECRB is enabled. At other times, I2Sx_CLK will be held in an inactiveI2Sx_FRM or idle state, as defined by the specified protocol under which it operates.

21.6.5.1 Programmable Serial Protocol (PSP)

There are many variations of the frame behavior for different codecs and protocol formats. To allow flexibility the PSP format allows I2Sx_FRM to be programmable in direction, delay, polarity, and width. Master and Slave modes are supported. PSP can be programmed to be either full or half duplex.

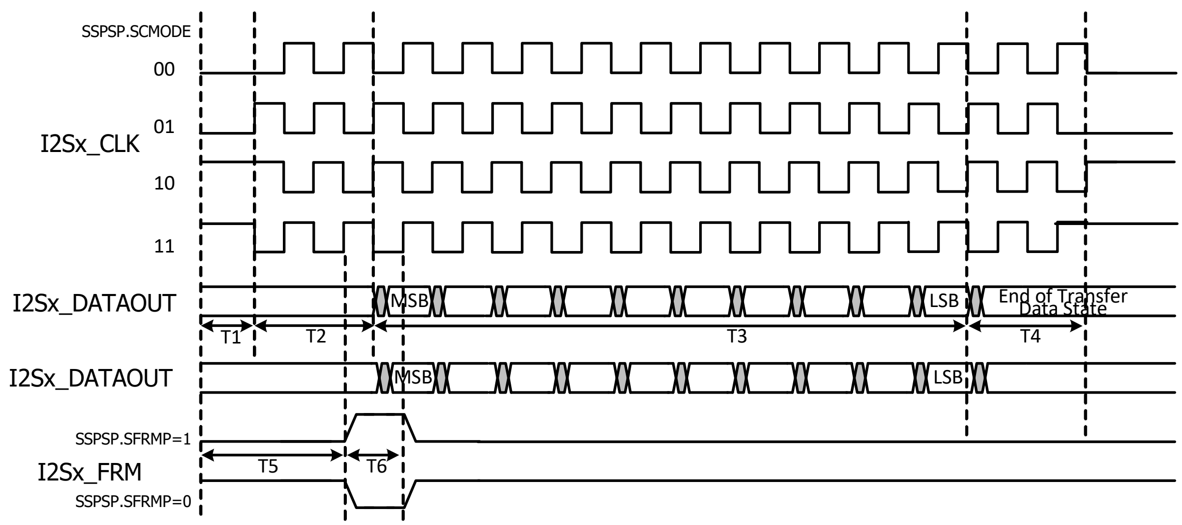
The I2Sx_CLK function behavior varies between each format. PSP lets programmers choose which edge of I2Sx_CLK to use for switching Transmit data, and for sampling Receive data. In addition, programmers can control the idle state for I2Sx_CLK and the number of active clocks that precede and follow the data transmission.

The PSP format provides programmability for several parameters that determine the transfer timings between data samples. There are four possible serial clock sub-modes, depending on the I2Sx_CLK edges selected for driving data and sampling received data, and the selection of idle state of the clock.

For the PSP format, the Idle and Disable modes of the I2Sx_DATAOUT, I2Sx_CLK, and I2Sx_FRM are programmable by means of the SSPSP.ETDS, SSPSP.SCMODE and SSPSP.SFRMP bits. When Transmit data is ready, the I2Sx_CLK will remain in its Idle state for the number of serial clock (I2Sx_CLK) clock periods programmed within the Start Delay (SSPSP.STRTDLY) field. I2Sx_CLK will then start toggling, I2Sx_DATAOUT will remain in the idle state for the number of cycles programmed within the Dummy Start (SSPSP.DMYSTRT) field. The I2Sx_FRM signal will be asserted after the number of half-clocks programmed in the SSPSP.SFRDLY field. The I2Sx_FRM signal will remain asserted for the number of clocks programmed within the SSPSP.SFRMWDTH then de-assert. Four to 32 bits can be transferred per frame. Once the last bit (LSB) is transferred, the I2Sx_CLK will continue toggling based off the Dummy Stop (SSPSP.DMYSTOP) field. I2Sx_DATAOUT either retains the last value transmitted or is forced to zero, depending on the value programmed within the End of Transfer Data State (SSPSP.ETDS) field, when the controller goes into Idle mode, unless the Enhanced SSP port is disabled or reset (which forces I2Sx_DATAOUT to zero).

With the assertion of I2Sx_FRM, Receive data is simultaneously driven from the peripheral on I2Sx_DATAIN, most significant bit first. Data transitions on I2Sx_CLK based on the Serial Clock Mode selected and is sampled by the controller on the opposite edge. When the Enhanced SSP is a master to the frame synch (I2Sx_FRM) and a slave to the clock (I2Sx_CLK), then at least three extra clocks (I2Sx_CLKs) will be needed at the beginning and end of each block of transfers to synchronize control signals from the APB clock domain into the SSP clock domain (a block of transfers is a group of back-to-back continuous transfers).

Figure 109. Programmable Serial Protocol Format



NOTE: When in PSP format, if the SSP is the master of the clock (I2Sx_CLK is an output) and the SSPSP.ETDS bit is cleared, the End of Transfer Data State for the I2Sx_DATAOUT line is 0. If the SSP is the master of the clock, and the SSPSP.ETDS bit is set, the I2Sx_DATAOUT line remains at the last bit transmitted (LSB). If the SSP is a slave to the clock (I2Sx_CLK is an input), and modes 1 or 3 are used, the ETDS can only change from the LSB if more clocks (I2Sx_CLK) are sent to the SSP (i.e., dummy stop clocks or slave clock is free running.

Figure 110. Programmable Serial Protocol Format (Consecutive Transfers)

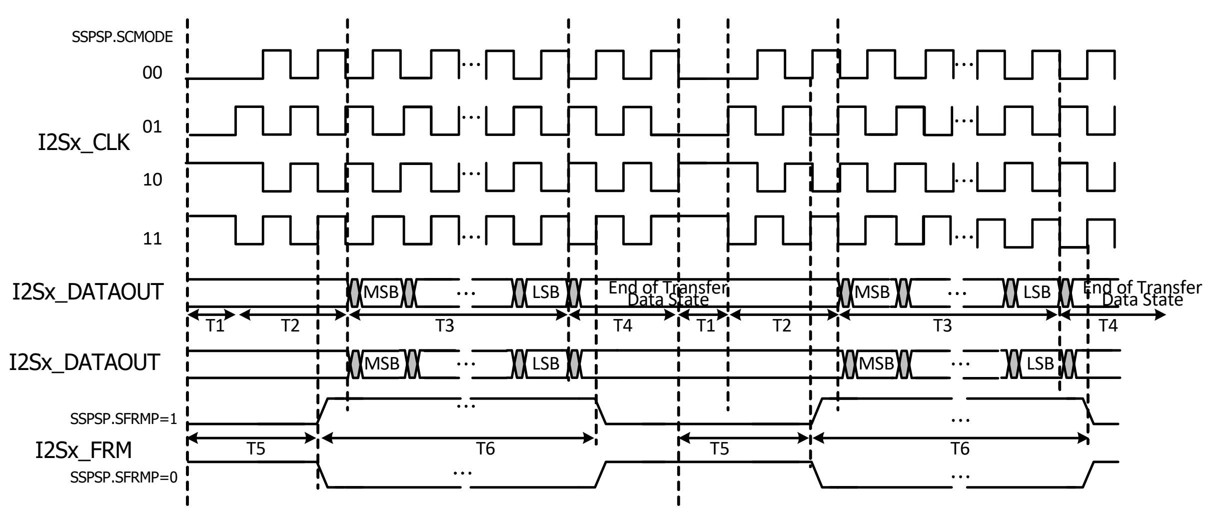


Table 230. Programmable Protocol Parameters

Symbol	Definition (Register.Bit Field)	Range	Units
	Serial Clock Mode (SSPSP.SCMODE)	(Drive, Sample, I2Sx_CLK Idle) 0 = Fall, Rise, Low 1 = Rise, Fall, Low 2 = Rise, Fall, High 3 = Fall, Rise, High	
	Serial Frame Polarity (SSPSP.SFRMP)	High or Low	
T1	Start Delay (SSPSP.STRTDLY)	0–7	Clock Period
T2	Dummy Start (SSPSP.DMYSTRT)	0–3	Clock Period
T3	Data Size (SSCRO.EDSS AND SSCRO.DSS)	4–32	Clock Period
T4	Dummy Stop (SSPSP.DMYSTOP)	0–3	Clock Period
T5	I2Sx_FRM Delay (SPSP.SFRMDLY)	0–88	Half Clock Period
T6	I2Sx_FRM Width (SSPSP.SFRMWDTH)	1–44	Clock Period
	End of Transfer Data State (SSPSP.ETDS)	Low or [bit 0]	

Note: The I2Sx_FRM Delay must not extend beyond the end of T4. I2Sx_FRM Width must be asserted for at least 1 I2Sx_CLK, and should be de-asserted before the end of the T4 cycle (for example, in terms of time, not bit values, (T5 + T6) <= (T1 + T2 + T3 + T4), 1<= T6 < (T2 + T3 + T4), and (T5 + T6) >= (T1 + 1) to ensure that I2Sx_FRM is asserted for at least 2 edges of the I2Sx_CLK). The T1 Start Delay value should be programmed to 0 when the I2Sx_CLK is enabled by either of the SSCR1.ECRA or SSCR1.ECRB bits. While the PSP can be programmed to generate the assertion of I2Sx_FRM during the middle of the data transfer (after the MSB was sent), the Enhanced SSP will not be able to receive data in Frame slave mode (SSCR1SFRMDIR = 1) if the assertion of Frame is not before the MSB is sent (i.e. T5 <= T2 if SSCR1.SFRMDIR =1). Transmit Data will transition from the "End of Transfer Data State" to the next MSB value upon the assertion of Frame. The Start Delay field should be programmed to 0 whenever I2Sx_CLK or I2Sx_FRM is configured as an input. Clock state is not defined between two active frame periods. Clock can be active or inactive between two active frame periods.

21.7 Programming Model

The CPU or DMA access data through the Enhanced SSP Port's Transmit and Receive FIFOs. A CPU access takes the form of programmed I/O, transferring one FIFO entry per access. CPU accesses would normally be triggered off of an SSSR Interrupt and must always be 32 bits wide. The CPU Writes to the FIFOs are 32 bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (EDSS/DSS value). CPU Reads to the FIFOs are also 32 bits wide, but the Receive data written into the RX FIFO (from the RXD line) is stored with zeroes in the MSBs down to the programmed data size. The FIFOs can also be accessed by DMA bursts, which must be in multiples of 1, 2, or 4 bytes, depending upon the EDSS value, and must also transfer one FIFO entry per access. When the SSCR0.EDSS bit is set, DMA bursts must be in multiples of 4 bytes (the DMA must have the Enhanced SSP configured as a 32-bit peripheral). The DMA DCMD.width register must be at least the SSP data size programmed into the SSP control registers EDSS and DSS. The FIFO is seen as one 32-bit location by the processor. For Writes, the Enhanced SSP port takes the data from the Transmit FIFO, serializes it, and sends it over the serial wire (I2Sx_DATAOUT) to the external peripheral. Receive data from the external peripheral (on I2Sx_DATAIN) is converted to parallel words and stored in the Receive FIFO.

A programmable FIFO trigger threshold, when exceeded, generates an Interrupt or DMA service request that, if enabled, signals the IA-32 CPU or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO. The Transmit and Receive FIFOs are differentiated by whether the access is a Read or a Write transfer. Reads automatically target the Receive FIFO, while Writes will write data to the Transmit FIFO. From a memory-map perspective, they are at the same address. Each read or write is 1 SSP sample.

21.7.1 PIO and DMA Programming Considerations

All CPU and DMA accesses transfer one FIFO entry per access. Data in the FIFOs is always stored with one 32-bit value per data sample, regardless of the format data word length. Within each 32-bit field, the stored data sample is right-justified, with the least significant bit of the word in bit 0. In the Receive FIFO, unused bits are packed as zeroes above the most significant bit. In the Transmit FIFO, unused don't-care bits are above the most significant bit (i.e., DMA and CPU access do not have to write to the unused bit locations). Logic in the Enhanced SSP automatically formats data in the Transmit FIFO so that the sample is properly transmitted on I2Sx_DATAOUT in the selected frame format.

Two separate and independent FIFOs are present for Transmit (to peripheral) and Receive (from peripheral) serial data. FIFOs are filled or emptied by programmed I/O or DMA bursts.

21.7.1.1 Programmed IO Considerations

FIFO filling and emptying can be performed by the processor in response to an Interrupt from the FIFO logic. Each FIFO has a programmable FIFO trigger threshold at which an Interrupt is triggered. When the number of entries in the Receive FIFO exceeds the SSCR1.RFT value, an interrupt is generated (if enabled), which signals the CPU to empty the Receive FIFO. When the number of entries in the Transmit FIFO is less than or equal to the SSCR1.TFT value plus 1, an Interrupt is generated (if enabled), which signals the CPU to refill the Transmit FIFO.

Users can also poll the Enhanced SSP Status register to determine how many samples are in a FIFO, and whether the FIFO is full or empty. Software is responsible for ensuring that the proper RFT and TFT values are chosen to prevent ROR and TUR error conditions.

Note: If the software attempts to read from an empty Receive FIFO, it will receive a duplicate of the previously read value.

21.7.1.2 DMA Considerations

The DMA controller can also be programmed to transfer data to and from the Enhanced SSP FIFOs. To prevent over-runs of the Transmit FIFO or under-runs of the Receive FIFO when using the DMA, be careful when setting the Transmit and Receive FIFO trigger threshold levels.

There are restrictions on how the DMA can be programmed when used with the SSP Controller.

- The DMA Transfer Width must be greater than or equal to the SSP data size. For example if the SSP Data Size is 16b then the DMA Transfer Width should be 16b.
- The DMA may not support the DMA Transfer Width of the SSP Data Size and therefore the DMA Transfer Width must be larger than the SSP Data Size. If this is the case then software must manage any extra data bits.
- The DMA Burst Transaction Length for RX must be less than or equal to the RX Threshold.
- The DMA Burst Transaction Length for TX must be less than or equal to the number of empty locations in the TX FIFO. A safe value is the Total TX FIFO Size - TX Threshold.
- DMA must be in Fixed Address mode to read or write the SSP Data Register.

In full-duplex formats where the Enhanced SSP always receives the same number of data samples as it transmits, the DMA should be set up to transmit and receive the same number of bytes.

Note: A TFT value of 0 means that there is one sample left in the TX FIFO.

Because the Enhanced SSP is not flow controlled, software must program the TX FIFO Threshold (TFT), RX FIFO Threshold (RFT), and the DMA burst size to ensure that a TX FIFO overflow or RX FIFO underflow does not occur. Software must also ensure that the Enhanced SSP DMA requests are properly prioritized in the system to prevent fatal overruns and under-runs.

The programming model for using the DMA is as follows:

- Program the total number of Transmit/Receive byte lengths, DMA burst, and DMA Width in the DMA.
- Set the preferred values in the Enhanced SSP Control registers.
- Enable the Enhanced SSP by setting SSCR0.SSE.
- Set the run bit in DMA Command Register.

- The DMA will wait for either the Transmit or Receive Service requests.
- If the Transmit/Receive byte length is not an even multiple of the transfer burst size, a trailing byte condition may occur.

21.7.2 Trailing Bytes in the Receive FIFO

When the number of samples in the Receive FIFO is less than its FIFO trigger threshold level, and no additional data is received, the remaining bytes are called trailing bytes. Trailing bytes can be handled by either the DMA or the processor, as indicated by the SSCR1.TRAIL bit. Trailing bytes are identified by means of a timeout mechanism and the existence of data within the Receive FIFO.

21.7.2.1 Timeout

A timeout condition exists when the Receive FIFO has been idle for a period of time (in APB clocks) defined by the value programmed within the Timeout register (SSTO). When a timeout occurs, the receiver timeout interrupt SSSR.TINT bit will be set to a 1, and if the Timeout Interrupt is enabled SSCR1.TINTE=1, a Timeout Interrupt will occur to signal the processor that a timeout condition has occurred. The timeout timer is reset after a new sample is received. Once the SSSR.TINT bit is set it must be cleared by software by writing a 1 to it. Clearing this bit also causes the Timeout Interrupt, if enabled, to be de-asserted.

21.7.2.2 Peripheral Trailing Byte Interrupt

It is possible for the DMA to reach the end of its Descriptor chain while removing Receive FIFO data. When this happens, the processor is forced to take over because the DMA can no longer service the Enhanced SSP request until a new chain is linked. When the DMA has reached the end of its Descriptor chain, and there is data in the receive FIFO, the Enhanced SSP will do the following:

- Sets the peripheral trailing byte interrupt SSSR.PINT bit to 1
- Asserts the Enhanced SSP Interrupt to signal to the processor that a Peripheral Trailing Byte Interrupt condition has occurred (if SSCR1.PINTE=1 to enable the interrupt).
- Sets the SSSR.EOC status bit which must be cleared by software. If more data is received after the EOC bit was set (and EOC bit is still set), then the SSSR.PINT bit will be set to a 1.

Once the SSSR.PINT bit is set, it must be cleared by software by writing a 1 to it. Clearing the SSSR.PINT bit also de-asserts the Peripheral Interrupt if it has been enabled (SSCR1.PINTE=1).

The remaining bytes must then be removed by means of a processor I/O as described in the processor-based method below, or by reprogramming a new Descriptor chain and restarting the DMA. Programmers need to be aware of this possibility. Refer to the DMA chapter for details on Descriptor programming and “end of chain” events.

21.7.2.3 Removing Trailing Bytes (Processor Based SSCR1.TRAIL=0)

This is the default method indicated by a zero in the SSCR1.TRAIL bit. In this case, no Receive DMA service request is generated. To read out the trailing bytes, software should wait for the timeout Interrupt and then read all remaining entries as indicated by the SSSR.RFL and SSSR.RNE bits within the Enhanced SSP Status register (SSSR).

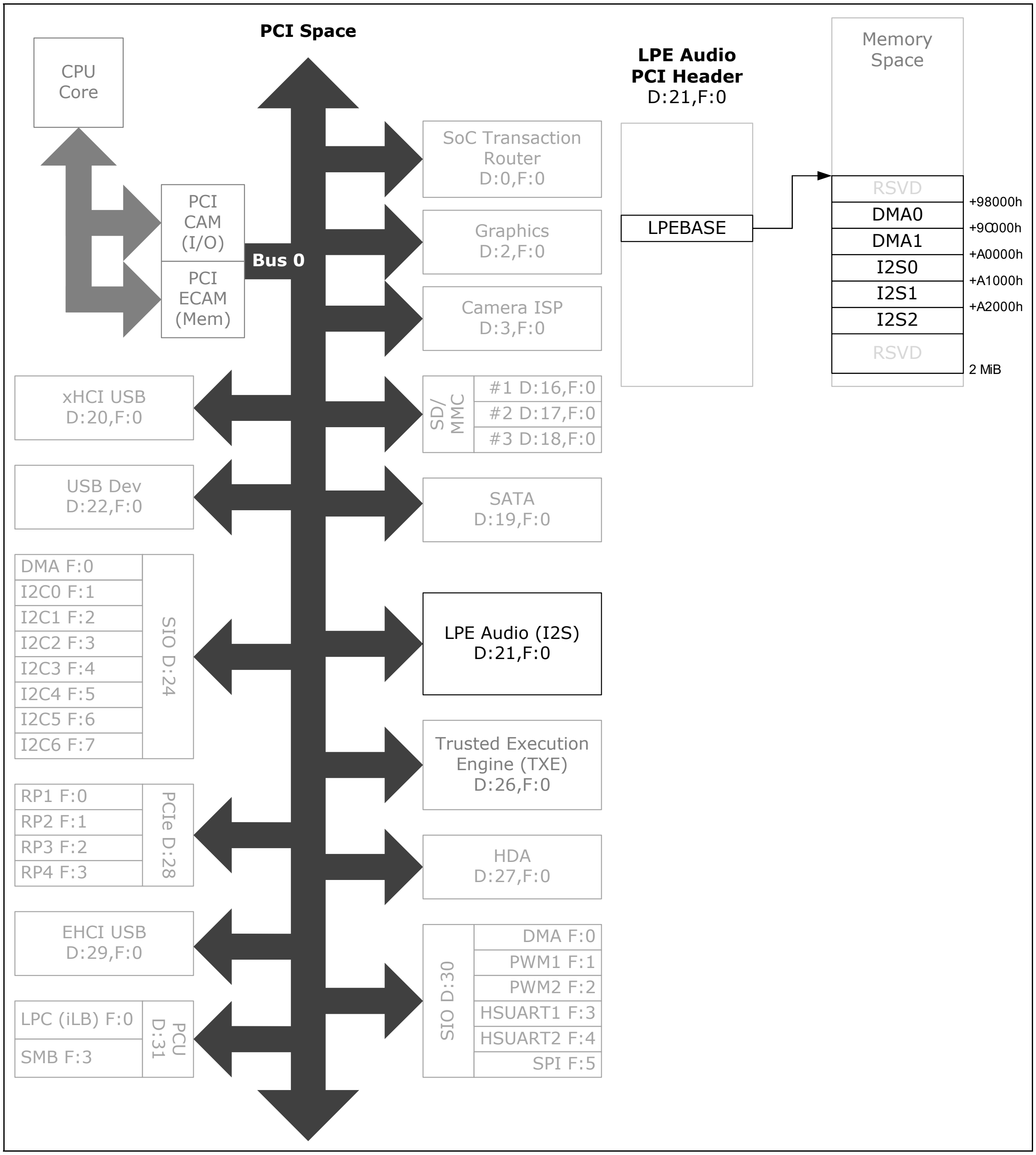
Note: To use the Trailing bytes feature through the CPU, the Timeout Interrupt must be enabled by setting SSCR1.TINTE=1 (to enable the interrupt).

21.7.2.4 Removing Trailing Bytes (DMA Based SSCR1.TRAIL=1)

When the DMA is to handle trailing bytes (SSCR1.TRAIL = 1) a DMA service request is automatically issued for the remaining number of samples left in the Receive buffer. The DMA will then empty the contents of the Receive buffer unless the DMA reaches the end of its Descriptor chain. If a timeout occurs, the processor is only interrupted by means of a Timeout Interrupt if it has been enabled by setting SSCR1.TINTE=1. When handling trailing bytes by means of the DMA, if a timeout occurs and the receive FIFO is empty, an End-of-Receive (EOR) will be sent to the DMA Controller. If an EOC occurs at the time that the last sample is read out of the FIFO (the DMA descriptor chain was just exactly long enough), and the timeout counter is still running (that is, a time out has not occurred and the SSTO register is non-zero), then, when the time out does occur, the Enhanced SSP will generate a DMA request which will create an RAS interrupt from the DMA. When this occurs, software must re-program the DMA registers and re-enable the channel for the Enhanced SSP to send its EOR to the DMA controller.

21.8 Register Map

Figure 111. Low Power Engine for Audio Register Map



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21.9 Low Power Audio PCI Configuration Registers

Table 231. Summary of Low Power Audio PCI Configuration Registers—0/21/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 2831	0F288086h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 2831	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 2833	04010000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 2833	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 2834	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 2834	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 2835	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2836	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 2836	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 2837	00000100h
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 2837	00030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 2838	00000008h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 2839	01000F00h

21.9.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEVVENDID: [0/21/0] + 0h

Default: 0F288086h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Description
31:16	0F28h RO	**DEVICEID:** Device ID
15:0	8086h RO	**VENDORID:** Vendor ID

21.9.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

STATUSCOMMAND: [0/21/0] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0		RMA	RCA	Reserved1							CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** reserved
29	0h RW/1C	**RMA:** Received Master Abort: Not Implemented
28	0h RW/1C	**RCA:** Received Target Abort: Not Implemented
27:21	00h RO	**Reserved1:** reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** reserved
15:11	00h RO	**Reserved3:** reserved
10	0h RW	**INTR_DISABLE:** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does not send Interrupt Assert message through the IOSF Sideband Channel. Reset value of this bit is 0. This bit has no connection with the interrupt status bit
9	0h RO	**Reserved4:** reserved
8	0h RW	**SERR_ENABLE:** not implemented
7:3	00h RO	**Reserved5:** reserved
2	0h RW	**BME:** If this bit is 0,the Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**MSE:** Memory Space Enable: This bit controls Bridge response to downstream memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0h RO	**Reserved6:** reserved

21.9.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

REVCLASSCODE: [0/21/0] + 8h

Default: 04010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: CLASS_CODES (31:8), RID (7:0)

Bit Range	Default & Access	Description
31:8	040100h RO	**CLASS_CODES:** Class Code
7:0	00h RO	**RID:** Revision ID

21.9.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CLLATHEADERBIST: [0/21/0] + Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved0 (31:24), MULFNDEV (23), HEADERTYPE (22:16), LATTIMER (15:8), CACHELINE_SIZE (7:0)

Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved
23	0h RO	**MULFNDEV:** MULFNDEV
22:16	00h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.

Bit Range	Default & Access	Description
15:8	00h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0. Similar to other Intel IPs.
7:0	00h RW	**CACHELINE_SIZE:** Cacheline Size: This register is implemented as R/W with default as 0. Similar to other Intel IPs.

21.9.5 reg_BAR_type (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

BAR: [0/21/0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR																				SIZEINDICATOR								PREFETCHABLE	TYPE		MESSAGE_SPACE

Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Base Address register
11:4	00h RO	**SIZEINDICATOR:** Size indicator
3	0h RO	**PREFETCHABLE:** Indicates that this BAR is not prefetchable.
2:1	0h RO	**TYPE:** 00 indicates BAR lies in 32bit address range
0	0h RO	**MESSAGE_SPACE:** message space

21.9.6 reg_BAR1_type (BAR1)—Offset 14h

BAR1 -Base Address Register1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

BAR1: [0/21/0] + 14h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** This field is present if BAR1 is enabled through private configuration space. Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1 region is always 4K.
11:4	00h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE1:** 00 indicates BAR lies in 32bit address range
0	0h RO	**MESSAGE_SPACE1:** message space

21.9.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SUBSYSTEMID: [0/21/0] + 2Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

SUBSYSTEMID	SUBSYSTEMVENDORID

Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Subsystem ID
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor

21.9.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

EXPANSION_ROM_BASEADDR: [0/21/0] + 30h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
EXPANSION_ROM_BASE							

Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Value of all zeros indicates no support for Expansion ROM

21.9.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CAPABILITYPTR: [0/21/0] + 34h

Default: 00000080h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
Reserved0						CAPPTR_POWER	

Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** reserved
7:0	80h RO	**CAPPTR_POWER:** Indicates what the next capability is. This capability points to the PM Capability, 0x80, structure.

21.9.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

INTERRUPTREG: [0/21/0] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

MAX_LAT	MIN_GNT	Reserved0	INTPIN	INTLINE

Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** reserved
11:8	1h RO	**INTPIN:** Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA
7:0	00h RW	**INTLINE:** Bridge does not use this field directly. It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

21.9.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

POWERCAPID: [0/21/0] + 80h

Default: 00030001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP

Bit Range	Default & Access	Description
31:27	00h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal at the same time in that power state. bit 11 X XXX1b: PME# can be asserted from D0 bit 12 X XX1Xb: PME# can be asserted from D1. Bridge does not support this state. bit 13 X X1XXb: PME# can be asserted from D2. Bridge does not support this state. bit 14 X 1XXXb:PME# can be asserted from D3hot bit 15 1 XXXXb:PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	00h RO	**Reserved0:** reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**NXTCAP:** Points to the next capability structure. This points to NULL
7:0	01h RO	**POWER_CAP:** Indicates this is power management capability.

21.9.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

reserved

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PMECTRLSTATUS: [0/21/0] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Reserved0																PMESTATUS	Reserved1						PMEENABLE	Reserved2				NO_SOFT_RESET	Reserved3	POWERSTATE	

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** reserved
15	0h RW/1C	**PMESTATUS:** 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit
14:9	00h RO	**Reserved1:** reserved
8	0h RW	**PMEENABLE:** pme enable
7:4	0h RO	**Reserved2:** reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset.Configuration Context is preserved.

Bit Range	Default & Access	Description
2	0h RO	**Reserved3:** reserved
1:0	0h RW	**POWERSTATE:** This field is used both to determine the current power state and to set a new power state.[BR]The values are: 00 D0 state 11 D3HOT state Others Reserved Note: If the software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally. The data is discarded and no state change occurs. Note: When in the D3HOT states, interrupts are blocked. D3Hot cannot be used for downstream decode on fabric ports.

21.9.13 reg_MANID_type (MANID)—Offset F8h

Manufacturers ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MANID: [0/21/0] + F8h

Default: 01000F00h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Description
31:0	01000f00h RO	**MANID:** Manufacturing ID

21.10 pci_mem Address Map

Table 232. Summary of Memory Mapped I/O Registers—0/21/0

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 2840	0F288086h
4h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 2840	00100000h
8h	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 2841	04010000h
Ch	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 2842	00000000h
10h	4	"reg_BAR_type (BAR)—Offset 10h" on page 2842	00000000h
14h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 2843	00000000h
2Ch	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 2844	00000000h
30h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2844	00000000h
34h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 2845	00000080h
3Ch	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 2845	00000100h

Table 232. Summary of Memory Mapped I/O Registers—0/21/0 (Continued)

Offset	Size	Register ID—Description	Default Value
80h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 2846	00030001h
84h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 2847	00000008h
F8h	4	"reg_MANID_type (MANID)—Offset F8h" on page 2848	01000F00h

21.10.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DEVVENDID: [0/21/0] + 0h

Default: 0F288086h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Description
31:16	0F28h RO	**DEVICEID:** Device ID
15:0	8086h RO	**VENDORID:** Vendor ID

21.10.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

STATUSCOMMAND: [0/21/0] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0		RMA	RCA	Reserved1							CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Description
31:30	0h RO	**Reserved0:** reserved

Bit Range	Default & Access	Description
29	0h RW/1C	**RMA:** Received Master Abort: Not Implemented
28	0h RW/1C	**RCA:** Received Target Abort: Not Implemented
27:21	00h RO	**Reserved1:** reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** reserved
15:11	00h RO	**Reserved3:** reserved
10	0h RW	**INTR_DISABLE:** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does not send Interrupt Assert message through the IOSF Sideband Channel. Reset value of this bit is 0. This bit has no connection with the interrupt status bit
9	0h RO	**Reserved4:** reserved
8	0h RW	**SERR_ENABLE:** not implemented
7:3	00h RO	**Reserved5:** reserved
2	0h RW	**BME:** If this bit is 0,the Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**MSE:** Memory Space Enable: This bit controls Bridge response to downstream memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0h RO	**Reserved6:** reserved

21.10.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

REVCLASSCODE: [0/21/0] + 8h

Default: 04010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
CLASS_CODES	RID

Bit Range	Default & Access	Description
31:8	040100h RO	**CLASS_CODES:** Class Code
7:0	00h RO	**RID:** Revision ID

21.10.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CLLATHEADERBIST: [0/21/0] + Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Description
31:24	00h RO	**Reserved0:** Reserved
23	0h RO	**MULFNDEV:** MULFNDEV
22:16	00h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	00h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0. Similar to other Intel IPs.
7:0	00h RW	**CACHELINE_SIZE:** Cacheline Size: This register is implemented as R/W with default as 0. Similar to other Intel IPs.

21.10.5 reg_BAR_type (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

BAR: [0/21/0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:12	Bits 11:4	Bit 3	Bits 2:1	Bit 0
BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR:** Base Address register
11:4	00h RO	**SIZEINDICATOR:** Size indicator
3	0h RO	**PREFETCHABLE:** Indicates that this BAR is not prefetchable.
2:1	0h RO	**TYPE:** 00 indicates BAR lies in 32bit address range
0	0h RO	**MESSAGE_SPACE:** message space

21.10.6 reg_BAR1_type (BAR1)—Offset 14h

BAR1 -Base Address Register1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

BAR1: [0/21/0] + 14h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:12	Bits 11:4	Bit 3	Bits 2:1	Bit 0
BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Description
31:12	00000h RW	**BASEADDR1:** This field is present if BAR1 is enabled through private configuration space. Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1 region is always 4K.
11:4	00h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Indicates that this BAR is not prefetchable

Bit Range	Default & Access	Description
2:1	0h RO	**TYPE1:** 00 indicates BAR lies in 32bit address range
0	0h RO	**MESSAGE_SPACE1:** message space

21.10.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SUBSYSTEMID: [0/21/0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Description
31:16	0000h RW/O	**SUBSYSTEMID:** Subsystem ID
15:0	0000h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor

21.10.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

EXPANSION_ROM_BASEADDR: [0/21/0] + 30h

Default: 00000000h

31	28		24		20		16		12		8		4		0
0 0 0 0		0 0 0 0		0 0 0 0		0 0 0 0		0 0 0 0		0 0 0 0		0 0 0 0		0 0 0 0
EXPANSION_ROM_BASE															

Bit Range	Default & Access	Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Value of all zeros indicates no support for Expansion ROM

21.10.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CAPABILITYPTR: [0/21/0] + 34h

Default: 00000080h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	
Reserved0 (31:8)						CAPPTR_POWER (7:0)		

Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved0:** reserved
7:0	80h RO	**CAPPTR_POWER:** Indicates what the next capability is. This capability points to the PM Capability, 0x80, structure.

21.10.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

INTERRUPTREG: [0/21/0] + 3Ch

Default: 00000100h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 0 0 0

MAX_LAT | MIN_GNT | Reserved0 | INTPIN | INTLINE

Bit Range	Default & Access	Description
31:24	00h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** reserved
11:8	1h RO	**INTPIN:** Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA
7:0	00h RW	**INTLINE:** Bridge does not use this field directly. It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

21.10.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

POWERCAPID: [0/21/0] + 80h

Default: 00030001h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1

PMESUPPORT | Reserved0 | VERSION | NXTCAP | POWER_CAP

Bit Range	Default & Access	Description
31:27	00h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal at the same time in that power state. bit 11 X XXX1b: PME# can be asserted from D0 bit 12 X XX1Xb: PME# can be asserted from D1. Bridge does not support this state. bit 13 X X1XXb: PME# can be asserted from D2. Bridge does not support this state. bit 14 X 1XXXb:PME# can be asserted from D3hot bit 15 1 XXXXb:PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	00h RO	**Reserved0:** reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification.

Bit Range	Default & Access	Description
15:8	00h RO	**NXTCAP:** Points to the next capability structure. This points to NULL
7:0	01h RO	**POWER_CAP:** Indicates this is power management capability.

21.10.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

reserved

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PMECTRLSTATUS: [0/21/0] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

31:16	15	14:9	8	7:4	3	2	1:0
Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved0:** reserved
15	0h RW/1C	**PMESTATUS:** 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit
14:9	00h RO	**Reserved1:** reserved
8	0h RW	**PMEENABLE:** pme enable
7:4	0h RO	**Reserved2:** reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset.Configuration Context is preserved.
2	0h RO	**Reserved3:** reserved
1:0	0h RW	**POWERSTATE:** This field is used both to determine the current power state and to set a new power state.[BR]The values are: 00 D0 state 11 D3HOT state Others Reserved Note: If the software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally. The data is discarded and no state change occurs. Note: When in the D3HOT states, interrupts are blocked. D3Hot cannot be used for downstream decode on fabric ports.

21.10.13 reg_MANID_type (MANID)—Offset F8h

Manufacturers ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **MANID:** [0/21/0] + F8h

Default: 01000F00h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
MANID																															

Bit Range	Default & Access	Description
31:0	01000f00h RO	**MANID:** Manufacturing ID

§ §

21.11 Memory Mapped Shim Registers

Table 233. Summary of LPE Shim Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	8	"reg_CSR_type (CSR)—Offset 0h" on page 2850	0000000001E40001h
8h	8	"reg_XT_PISR_type (PISR)—Offset 8h" on page 2851	0000000000000000h
10h	8	"reg_XT_PIMR_type (PIMR)—Offset 10h" on page 2852	0000000000000000h
18h	8	"reg_IA_PISR_type (ISRX)—Offset 18h" on page 2853	0000000000000000h
20h	8	"reg_ISRD_type (ISRD)—Offset 20h" on page 2854	0000000000000000h
28h	8	"reg_IA_PIMR_type (IMRX)—Offset 28h" on page 2855	0000000000000000h
30h	8	"reg_IMRD_type (IMRD)—Offset 30h" on page 2856	0000000000000000h
38h	8	"reg_IPCX_type (IPCX)—Offset 38h" on page 2857	0000000000000000h
40h	8	"reg_IPCD_type (IPCD)—Offset 40h" on page 2858	0000000000000000h
48h	8	"reg_ISRSC_type (ISRSC)—Offset 48h" on page 2858	0000000000000000h
50h	8	"reg_ISRLPESC_type (ISRLPESC)—Offset 50h" on page 2859	0000000000000000h
58h	8	"reg_IMRSC_type (IMRSC)—Offset 58h" on page 2860	0000000000000000h
60h	8	"reg_IMRLPESC_type (IMRLPESC)—Offset 60h" on page 2861	0000000000000000h
68h	8	"reg_IPCSC_type (IPCSC)—Offset 68h" on page 2861	0000000000000000h
70h	8	"reg_IPCLPESC_type (IPCLPESC)—Offset 70h" on page 2862	0000000000000000h
78h	8	"reg_CLKCTL_type (CLKCTL)—Offset 78h" on page 2863	0000000000070013h
80h	8	"reg_FR_LAT_REQ_type (FR_LAT_REQ)—Offset 80h" on page 2863	0000000000000000h
88h	8	"reg_CHICKEN_BITS_type (CHICKEN_BITS)—Offset 88h" on page 2864	0000000000000000h
90h	8	"reg_ISRPSH_type (ISRPSH)—Offset 90h" on page 2865	0000000000000000h
98h	8	"reg_ISRLPEPSH_type (ISRLPEPSH)—Offset 98h" on page 2866	0000000000000000h
A0h	8	"reg_IMRPSH_type (IMRPSH)—Offset A0h" on page 2866	0000000000000000h
A8h	8	"reg_IMRLPEPSH_type (IMRLPEPSH)—Offset A8h" on page 2867	0000000000000000h
B0h	8	"reg_IPCPSH_type (IPCPSH)—Offset B0h" on page 2868	0000000000000000h
B8h	8	"reg_IPCLPEPSH_type (IPCLPEPSH)—Offset B8h" on page 2868	0000000000000000h
C0h	8	"reg_EXT_TIMER_CNTL_type (EXT_TIMER_CNTL)—Offset C0h" on page 2869	0000000000000000h
C8h	8	"reg_EXT_TIMER_STAT_type (EXT_TIMER_STAT)—Offset C8h" on page 2870	0000000000000000h
D0h	8	"reg_S0ix_TIMER_CNTL_type (S0ix_TIMER_CNTL)—Offset D0h" on page 2870	0000000000000000h
D8h	8	"reg_S0ix_TIMER_STAT_type (S0ix_TIMER_STAT)—Offset D8h" on page 2871	0000000000000000h
E0h	8	"reg_RAW_PISR_type (XT_RAW_PISR)—Offset E0h" on page 2872	0000000000000000h
E8h	8	"reg_SSP0_DIV_CTRL_type (SSP0_DIV_CTRL)—Offset E8h" on page 2873	8000000100000001h
F0h	8	"reg_SSP1_DIV_CTRL_type (SSP1_DIV_CTRL)—Offset F0h" on page 2873	8000000100000001h
F8h	8	"reg_SSP2_DIV_CTRL_type (SSP2_DIV_CTRL)—Offset F8h" on page 2874	8000000100000001h

21.11.1 reg_CSR_type (CSR)—Offset 0h

This register controls clock and reset of the block, various configurations of the block and reflects general status of the block.

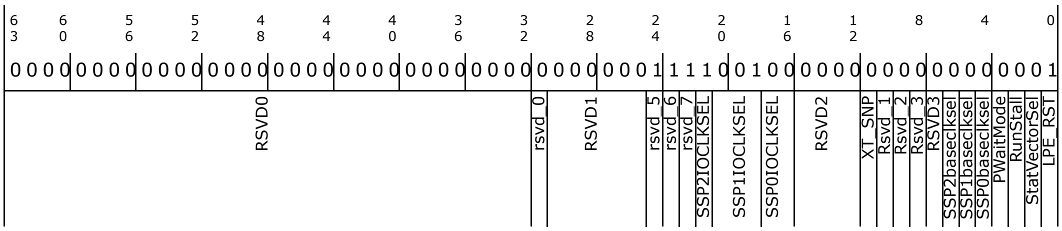
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

CSR: [BAR + 140000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000001E40001h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31	0b RW	**rsvd_0:** Reserved
30:25	0b RO	**RSVD1:** Reserved
24	1b RW	**rsvd_5:** Reserved
23	1b RW	**rsvd_6:** Reserved
22	1b RW	**rsvd_7:** Reserved
21:20	10b RW	**SSP2IOCLKSEL:** SSP 2 IO clock select 0: select SSP 0 IO clock for SSP 2 IO clock input 1: select SSP 1 IO clock for SSP 2 IO clock input 2: select SSP 2 IO clock for SSP 2 IO clock input
19:18	01b RW	**SSP1IOCLKSEL:** SSP 1 IO clock select 0: select SSP 0 IO clock for SSP 1 IO clock input 1: select SSP 1 IO clock for SSP 1 IO clock input 2: select SSP 2 IO clock for SSP 1 IO clock input
17:16	00b RW	**SSP0IOCLKSEL:** SSP 0 IO clock select 0: select SSP 0 IO clock for SSP 0 IO clock input 1: select SSP 1 IO clock for SSP 0 IO clock input 2: select SSP 2 IO clock for SSP 0 IO clock input
15:12	0b RO	**RSVD2:** Reserved
11	0b RW	**XT_SNP:** This bit controls whether the Tensilica initiated traffic is Snooped or Non-snooped. 0 =) Non-Snooped 1 =) Snooped
10	0b RW	**Rsvd_1:** Reserved
9	0b RW	**Rsvd_2:** Reserved

Bit Range	Default & Access	Description
8	0b RW	**Rsvd_3:** Reserved
7	0b RO	**RSVD3:** Reserved
6	0b RW	**SSP2baseclksel:** 1 =) Select 25 Mhz clock for the SSP2 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock
5	0b RW	**SSP1baseclksel:** 1 =) Select 25 Mhz clock for the SSP1 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock
4	0b RW	**SSP0baseclksel:** 1 =) Select 25 Mhz clock for the SSP0 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock
3	0b RO	**PWaitMode:** Satus bit when set to '1 indicates that LPE core is stalled.
2	0b RW	**RunStall:** When set to '1, LPE core is stalled.
1	0b RW	**StatVectorSel:** When set to '1, LPE core boots from the Alternate reset vector. This is set to ff2c_0000 - first address of Audio IRAM. Default reset vector is set to 0x100000. This needs to be set to 1'b1 for TNG.
0	1b RW	**LPE_RST:** LPE Reset. LPE held in reset state until this bit is set to 1. Minimum number of cycles is defined LPE manual. The bit should be cleared to bring the LPE out of reset.

21.11.2 reg_XT_PISR_type (PISR)—Offset 8h

PISR

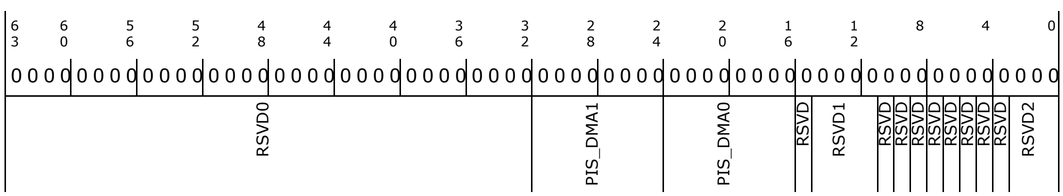
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

PISR: [BAR + 140000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	00000000b RW/1C	**PIS_DMA1:** DMA 1 interrupts
23:16	00000000b RW/1C	**PIS_DMA0:** DMA 0 interrupts
15	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
14:11	0b RO	**RSVD1:** Reserved
10	0b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	0b RO	**RSVD2:** Reserved

21.11.3 reg_XT_PIMR_type (PIMR)—Offset 10h

PIMR

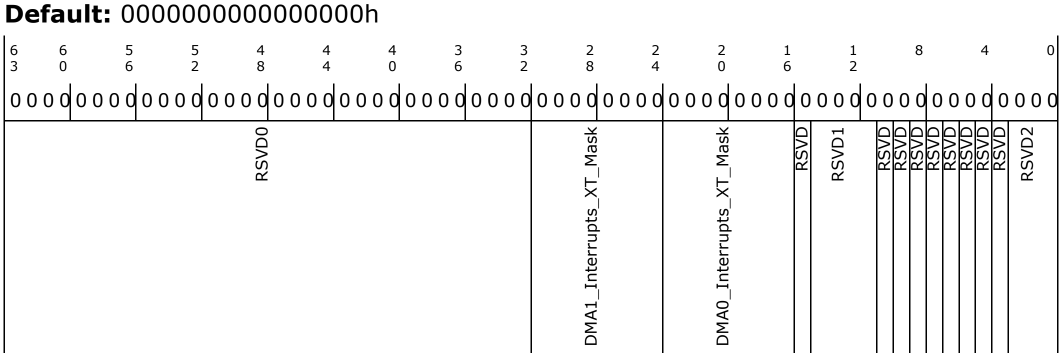
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

PIMR: [BAR + 140000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
31:24	00000000b RW	**DMA1_Interrupts_XT_Mask:** DMA 1 interrupts
23:16	00000000b RW	**DMA0_Interrupts_XT_Mask:** DMA 0 interrupts
15	0b RO	**Reserved (RSVD):** Reserved.
14:11	0b RO	**RSVD1:** Reserved
10	0b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	0b RO	**RSVD2:** Reserved

21.11.4 reg_IA_PISR_type (ISRX)—Offset 18h

PISR

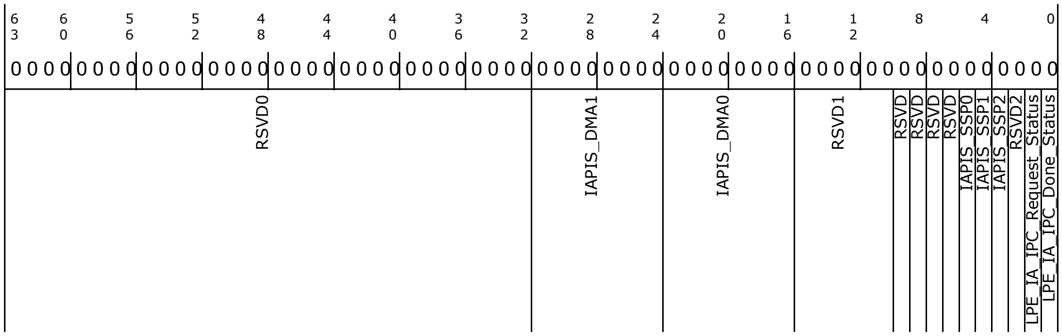
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRX: [BAR + 140000h] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	00000000b RW/1C	**IAPIS_DMA1:** DMA 1 interrupts
23:16	00000000b RW/1C	**IAPIS_DMA0:** DMA 0 interrupts
15:10	0b RO	**RSVD1:** Reserved
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RW/1C	**IAPIS_SSP0:** SSP0 Interrupt Request for SC 1: interrupt when SSP0 interrupt is asserted. 0: Deasserted
4	0b RW/1C	**IAPIS_SSP1:** SSP1 Interrupt Request for SC 1: interrupt when SSP1 interrupt is asserted. 0: Deasserted
3	0b RW/1C	**IAPIS_SSP2:** SSP2 Interrupt Request for SC 1: interrupt when SSP2 interrupt is asserted. 0: Deasserted
2	0b RO	**RSVD2:** Reserved
1	0b RO	**LPE_IA_IPC_Request_Status:** IPCD Interrupt Request 1: interrupt when LPE writes a message into IPCD register with bit 63 set 0: Deasserted
0	0b RO	**LPE_IA_IPC_Done_Status:** IPCX Interrupt Request 1: interrupt when LPE writes a message into IPCX register with bit 62 set is asserted 0: Deasserted.

21.11.5 reg_ISRD_type (ISRD)—Offset 20h

ISRD

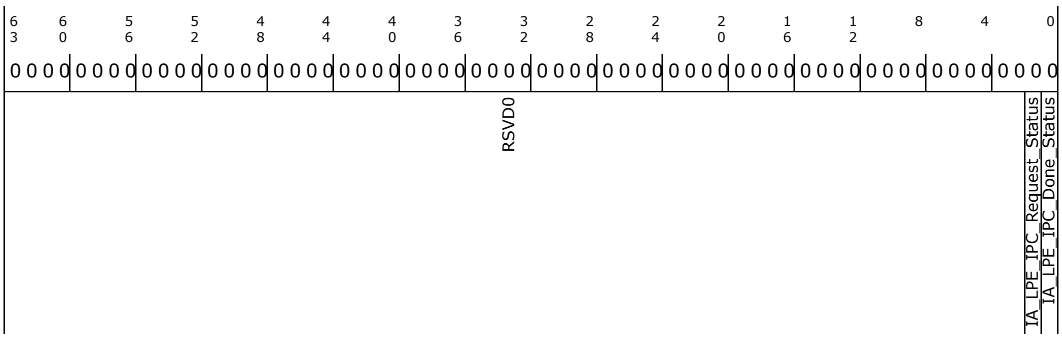
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

ISRD: [BAR + 140000h] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RO	**IA_LPE_IPC_Request_Status:** IPCIA Interrupt Request to LPE 1: interrupt when IA-32 CPU writes a message into IPCIA register with bit 63 set. 0: Deasserted
0	0b RO	**IA_LPE_IPC_Done_Status:** IPCLPEIA Interrupt Request to LPE 1: interrupt when IA-32 CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

21.11.6 reg_IA_PIMR_type (IMRX)—Offset 28h

PIMR

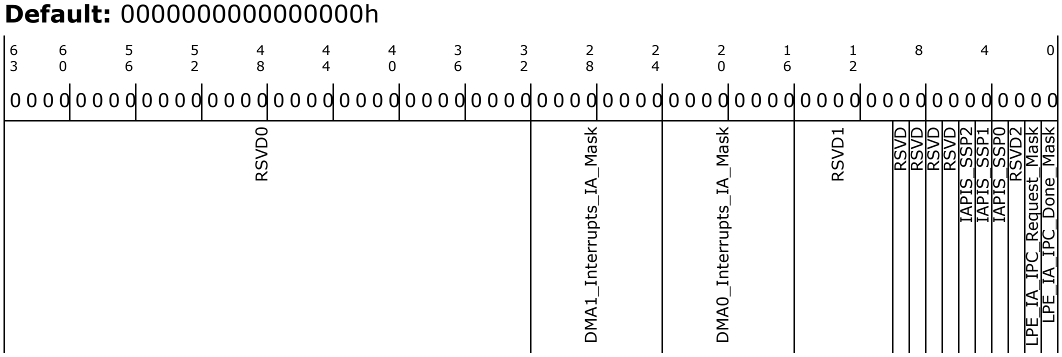
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IMRX: [BAR + 140000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	0b RW	**DMA1_Interrupts_IA_Mask:** DMA 1 interrupts mask
23:16	0b RW	**DMA0_Interrupts_IA_Mask:** DMA 0 interrupts mask
15:10	0b RO	**RSVD1:** Reserved
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RW	**IAPIS_SSP2:** SSP2 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
4	0b RW	**IAPIS_SSP1:** SSP1 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
3	0b RW	**IAPIS_SSP0:** SSP0 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
2	0b RO	**RSVD2:** Reserved
1	0b RW	**LPE_IA_IPC_Request_Mask:** LPE to IA IPC Request Mask 1: Interrupt is masked 0: Interrupt is unmasked
0	0b RW	**LPE_IA_IPC_Done_Mask:** LPE to IA IPC Done Mask 1: Interrupt is masked 0: Interrupt is unmasked

21.11.7 reg_IMRD_type (IMRD)—Offset 30h

IMRD

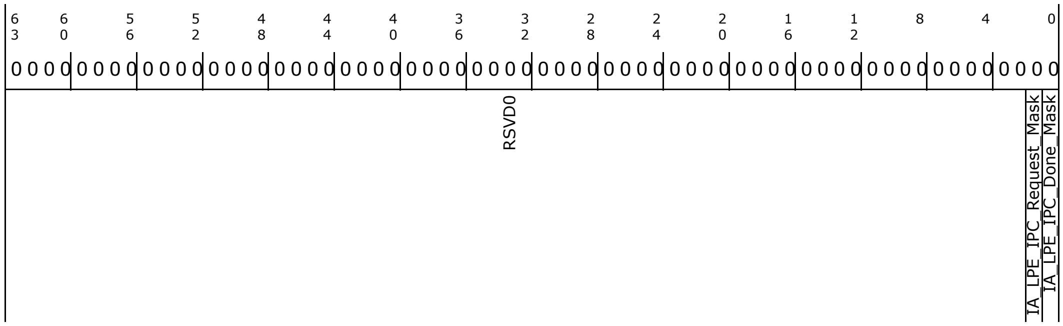
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IMRD: [BAR + 140000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RW	**IA_LPE_IPC_Request_Mask:** IPCIA interrupt Enable to LPE
0	0b RW	**IA_LPE_IPC_Done_Mask:** IPCLPEIA interrupt Enable to LPE

21.11.8 reg_IPCX_type (IPCX)—Offset 38h

The Inter-process Status and Message register for IA-32 contains a message sent from the IA-32 CPU to LPE. The format of the CPU message bits (61:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCIA is not empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPEIA. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The IA-32 CPU must not attempt to write into IPCIA if bit 63 is set.

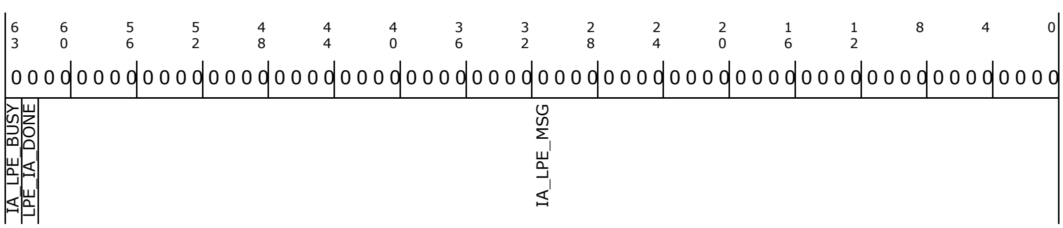
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IPCX: [BAR + 140000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**IA_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message

Bit Range	Default & Access	Description
62	0b RW	**LPE_IA_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	0000000000000000h RW	**IA_LPE_MSG:** IA-32 to LPE Message

21.11.9 reg_IPCD_type (IPCD)—Offset 40h

Inter-process Status and Message register for LPE contains a message sent from LPE to IA-32 CPU. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When IA-32 CPU reads the message code from the register, and writes back with the bit 63 cleared. When the IA-32 CPU processes the message sent by LPE, it may set bit 63 in IPCD to assert interrupt request to LPE. The LPE must not attempt to write into IPCLPEIA if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IPCD: [BAR + 140000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	62	61:0
0	0	000000000000000000000000000000000000000000000000000000000000000
LPE_IA_BUSY	IA_LPE_DONE	LPE_IA_MSG

Bit Range	Default & Access	Description
63	0b RW	**LPE_IA_BUSY:** Busy. When this bit is cleared, the IA CPU is Ready to accept a new message
62	0b RW	**IA_LPE_DONE:** Done. When the bit is set, the IA CPU completed operation and requests attention from LPE
61:0	0000000000000000h RW	**LPE_IA_MSG:** LPE to IA CPU Message

21.11.10 reg_ISRSC_type (ISRSC)—Offset 48h

ISRSC

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

ISRSC: [BAR + 140000h] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

RSVD0 | Wake_SCU_Status | GoS0ixInt_SCU_Status | RSVD1 | LPE_SC_IPC_Request_Status | LPE_SC_IPC_Done_Status

Bit Range	Default & Access	Description
63:34	0b RO	**RSVD0:** Reserved
33	0b RW/1C	**Wake_SCU_Status:** This bit is set by hardware when a blocked transaction is detected. It generates a wake to the SCU
32	0b RW/1C	**GoS0ixInt_SCU_Status:** This bit is set by expiry of the Re-entry timer. The bit gets set only if GoS0ixInt_En bit is set and this interrupt is unmasked.
31:2	0b RO	**RSVD1:** Reserved
1	0b RO	**LPE_SC_IPC_Request_Status:** IPCLPESC Interrupt Request 1: interrupt when LPE writes a message into IPCLPESC register with bit 63 set 0: Deasserted
0	0b RW/1C	**LPE_SC_IPC_Done_Status:** IPCSC Interrupt Request 1: interrupt when LPE writes a message into IPCSC register with bit 62 set is asserted 0: Deasserted.

21.11.11 reg_ISRLPESC_type (ISRLPESC)—Offset 50h

ISRLPESC

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRLPESC: [BAR + 140000h] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

RSVD0 | SC_LPE_IPC_Request_Status | SC_LPE_IPC_Done_Status

Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RO	**SC_LPE_IPC_Request_Status:** IPCSC Interrupt Request to LPE 1: interrupt when SC writes a message into IPCSC register with bit 63 set. 0: Deasserted
0	0b RO	**SC_LPE_IPC_Done_Status:** IPCLPESC Interrupt Request to LPE 1: interrupt when SC CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

21.11.12 reg_IMRSC_type (IMRSC)—Offset 58h

IMRSC

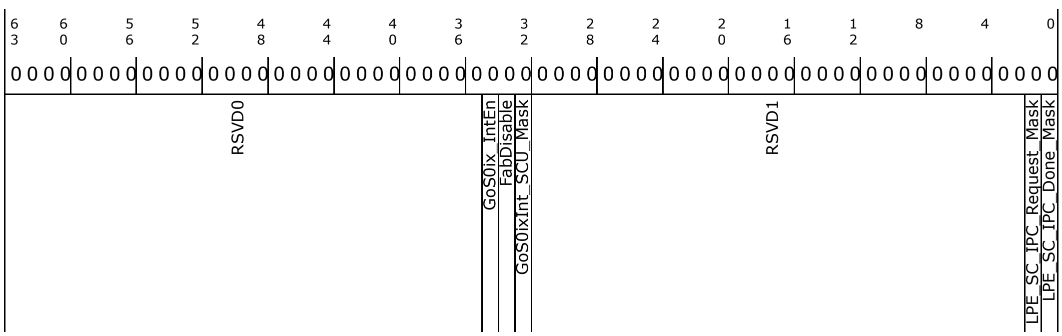
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IMRSC: [BAR + 140000h] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:35	0b RO	**RSVD0:** Reserved
34	0b RW/1C	**GoS0ix_IntEn:** This bit indicates that Reentry to S0iX interrupts to SCU are enabled. The bit is set by hardware when a transaction is blocked at the Audio to Secondary interface due to the secondary fabric being gated and the fabdisable bit being set. Software is expected to clear this bit along with the Secondary Fabric Reject bit. This disables the interrupts.
33	0b RW	**FabDisable:** This bit is used to generate the wake interrupt to SCU. When set the interrupt generation is enabled. When cleared the interrupt generation is disabled
32	0b RW	**GoS0ixInt_SCU_Mask:** Mask bit for S0ix Reentry interrupt to SCU
31:2	0b RO	**RSVD1:** Reserved
1	0b RW	**LPE_SC_IPC_Request_Mask:** IPCLPESC Interrupt Enable to SC CPU
0	0b RW	**LPE_SC_IPC_Done_Mask:** IPCSC Interrupt Enable to SC CPU

21.11.13 reg_IMRLPESC_type (IMRLPESC)—Offset 60h

IMRLPRESC

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IMRLPESC: [BAR + 140000h] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0

RSVD0 | SC_LPE_IPC_Request_Mask | SC_LPE_IPC_Done_Mask

Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RW	**SC_LPE_IPC_Request_Mask:** IPCSC interrupt Enable to LPE
0	0b RW	**SC_LPE_IPC_Done_Mask:** IPCLPESC interrupt Enable to LPE

21.11.14 reg_IPCSC_type (IPCSC)—Offset 68h

The Inter-process Status and Message register for SC contains a message sent from the SC CPU to LPE. The format of the CPU message bits (29:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCSC is not empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPESC. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The SC CPU must not attempt to write into IPCIA if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IPCSC: [BAR + 140000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

SC_LPE_BUSY | LPE_SC_DONE | SC_LPE_MSG

Bit Range	Default & Access	Description
63	0b RW	**SC_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message
62	0b RW	**LPE_SC_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	0000000000000000h RW	**SC_LPE_MSG:** SC to LPE Message

21.11.15 reg_IPCLPESC_type (IPCLPESC)—Offset 70h

Inter-process Status and Message register for LPE contains a message sent from LPE to SC. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When SC reads the message code from the register, and writes back with the bit 63 cleared. When the SC CPU processes the message sent by LPE, it may set bit 62 in IPCLPESC to assert interrupt request to LPE. The LPE must not attempt to write into IPCD if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IPCLPESC: [BAR + 140000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

LPE_SC_BUSY | SC_LPE_DONE | LPE_SC_MSG

Bit Range	Default & Access	Description
63	0b RW	**LPE_SC_BUSY:** Busy. When this bit is cleared, the SC CPU is Ready to accept a new message
62	0b RW	**SC_LPE_DONE:** Done. When the bit is set, the SC CPU completed operation and requests attention from LPE
61:0	0h RW	**LPE_SC_MSG:** LPE to SC CPU Message

21.11.16 reg_CLKCTL_type (CLKCTL)—Offset 78h

LPE Clock Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

CLKCTL: [BAR + 140000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000070013h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 1	0 0 0 0	0 0 0 0	0 0 0 1	0 0 1 1	

RSVD0 | RSVD | RSVD1 | EN_SSP2_CLK | EN_SSP1_CLK | EN_SSP0_CLK | RSVD2 | OSC_MODE | FRCHNGGO | FRCHNGACK | RSVD3 | CLK_DIV

Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:25	0000000b RO	**RSVD:** Reserved
24:19	0b RO	**RSVD1:** Reserved
18	1b RW	**EN_SSP2_CLK:** clock output enable
17	1b RW	**EN_SSP1_CLK:** clock output enable
16	1b RW	**EN_SSP0_CLK:** clock output enable
15:7	0b RO	**RSVD2:** Reserved
6	0b RO	**OSC_MODE:** 1 indicates that PLL is turned off
5	0b RW/1S	**FRCHNGGO:** Go bit indicating that the value in 2:0 can be applied to core. This bit will get cleared on the rising edge of the ack from Clock Control Unit.
4	1b RO	**FRCHNGACK:** Sets on the falling edge of ack. A 1'b1 indicates that the frequency change is done. The bit auto clears on the rising edge of frequency change request.
3	0b RO	**RSVD3:** Reserved
2:0	011b RW	**CLK_DIV:** 000: 25 MHz(XTAL) 001: 25 Mhz(XTAL) 010: 50 Mhz(2xXTAL) 011: 50 Mhz(default) 100: 100 Mhz 101: 200 Mhz 110: 267 Mhz 111: 343 Mhz

21.11.17 reg_FR_LAT_REQ_type (FR_LAT_REQ)—Offset 80h

LPE

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

FR_LAT_REQ: [BAR + 140000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

RSVD0, Latency_tol, RSVD1, Required_freq

Bit Range	Default & Access	Description
63:7	0b RO	**RSVD0:** Reserved
6:4	0b RW	**Latency_tol:** Latency tolerance for Cache Misses is listed here. SCU firmware is required to read this register and make a decision on whether it can enter a lower power state and still meet the latency tolerance.
3	0b RO	**RSVD1:** Reserved
2:0	0b RW	**Required_freq:** The following encoding specifies the frequency that the Audio Cluster requires for current operations. 000: 25 MHz(XTAL) 001: 25 Mhz(XTAL) 010: 50 Mhz(2xXTAL) 011: 50 Mhz(default) 100: 100 Mhz 101: 200 Mhz 110: 267 Mhz 111: 343 Mhz Please note, that this does not guarantee that this frequency will be generated from the CCU. The SCU firmware is required to read this register before making a decision on entering lower power states.

21.11.18 reg_CHICKEN_BITS_type (CHICKEN_BITS)—Offset 88h

LPE

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

CHICKEN_BITS: [BAR + 140000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

RSVD0, DMA_Debug_Select, XT_posted_only_traffic, IPC_wakes_SCU, bug_2431329_fix_disable, disable_ssp2_dma_finish, disable_ssp1_dma_finish, disable_ssp0_dma_finish, waiti_fix_enable

Bit Range	Default & Access	Description
63:8	0b RO	**RSVD0:** Reserved
7	0b RW	**DMA_Debug_Select:** Setting this bit will select DMA 1 debug signals to be routed to the VISA Mux.
6	0b RW	**XT_posted_only_traffic:** Setting this bit will select make all the traffic from Tensilica to be posted.
5	0b RW	**IPC_wakes_SCU:** Setting this to 1 will cause the IPC to be fed into the wake cone for SCU.
4	0b RW	**bug_2431329_fix_disable:** Setting this to 1 will disable the synopsys compatible hardware handshake mechanism. Keep this set to 0 for regular hardware handshake operation.
3	0b RW	**disable_ssp2_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
2	0b RW	**disable_ssp1_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
1	0b RW	**disable_ssp0_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
0	0b RW	**waiti_fix_enable:** Setting this bit to 1 makes the frequency change request to be valid only if the core is in WAITI.

21.11.19 reg_ISRPSH_type (ISRPSH)—Offset 90h

ISRPSH

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

ISRPSH: [BAR + 140000h] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0

Fields: RSVD0 (63:2), LPE_PSH_IPC_Request_Status (1), LPE_PSH_IPC_Done_Status (0)

Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
1	0b RO	**LPE_PSH_IPC_Request_Status:** IPCLPEPSH Interrupt Request 1: interrupt when LPE writes a message into IPCLPEPSH register with bit 63 set 0: Deasserted
0	0b RW/1C	**LPE_PSH_IPC_Done_Status:** IPCPSH Interrupt Request 1: interrupt when LPE writes a message into IPCPSH register with bit 62 set is asserted 0: Deasserted.

21.11.20 reg_ISRLPEPSH_type (ISRLPEPSH)—Offset 98h

ISRLPEPSH

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

ISRLPEPSH: [BAR + 140000h] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

RSVD0 | PSH_LPE_IPC_Request_Status | PSH_LPE_IPC_Done_Status

Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RO	**PSH_LPE_IPC_Request_Status:** IPCPSH Interrupt Request to LPE 1: interrupt when PSH writes a message into IPCPSH register with bit 63 set. 0: Deasserted
0	0b RO	**PSH_LPE_IPC_Done_Status:** IPCLPEPSH Interrupt Request to LPE 1: interrupt when PSH CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

21.11.21 reg_IMRPSH_type (IMRPSH)—Offset A0h

IMRPSH

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IMRPSH: [BAR + 140000h] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

RSVD0 | LPE_PSH_IPC_Request_Mask | LPE_PSH_IPC_Done_Mask

Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RW	**LPE_PSH_IPC_Request_Mask:** IPCLPEPSH Interrupt Enable to PSH CPU
0	0b RW	**LPE_PSH_IPC_Done_Mask:** IPCPSH Interrupt Enable to PSH CPU

21.11.22 reg_IMRLPEPSH_type (IMRLPEPSH)—Offset A8h

IMRLPEPSH

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

IMRLPEPSH: [BAR + 140000h] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

RSVD0 | PSH_LPE_IPC_Request_Mask | PSH_LPE_IPC_Done_Mask

Bit Range	Default & Access	Description
63:2	0b RO	**RSVD0:** Reserved
1	0b RW	**PSH_LPE_IPC_Request_Mask:** IPCPSH interrupt Enable to LPE

Bit Range	Default & Access	Description
0	0b RW	**PSH_LPE_IPC_Done_Mask:** IPCLPEPSH interrupt Enable to LPE

21.11.23 reg_IPCPSH_type (IPCPSH)—Offset B0h

The Inter-process Status and Message register for PSH contains a message sent from the PSH CPU to LPE. The format of the CPU message bits (29:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCPSH is not empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPEPSH. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The PSH CPU must not attempt to write into IPCIA if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IPCPSH: [BAR + 140000h] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63 60 56 52 48 44 40 36 32 28 24 20 16 12 8 4 0

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

PSH_LPE_BUSY
LPE_PSH_DONE
PSH_LPE_MSG

Bit Range	Default & Access	Description
63	0b RW	**PSH_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message
62	0b RW	**LPE_PSH_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	000000000 0000000h RW	**PSH_LPE_MSG:** PSH to LPE Message

21.11.24 reg_IPCLPEPSH_type (IPCLPEPSH)—Offset B8h

Inter-process Status and Message register for LPE contains a message sent from LPE to PSH. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When PSH reads the message code from the register, and writes back with the bit 63 cleared. When the PSH CPU processes the message sent by LPE, it may set bit 62 in IPCLPEPSH to assert interrupt request to LPE. The LPE must not attempt to write into IPCD if bit 63 is set.

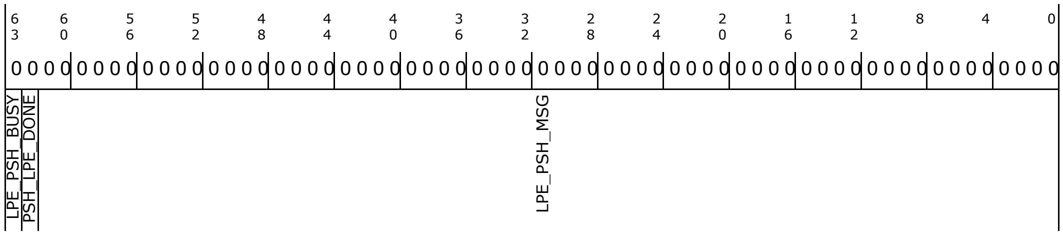
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

IPCLPEPSH: [BAR + 140000h] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**LPE_PSH_BUSY:** Busy. When this bit is cleared, the PSH CPU is Ready to accept a new message
62	0b RW	**PSH_LPE_DONE:** Done. When the bit is set, the PSH CPU completed operation and requests attention from LPE
61:0	0h RW	**LPE_PSH_MSG:** LPE to PSH CPU Message

21.11.25 reg_EXT_TIMER_CNTL_type (EXT_TIMER_CNTL)—Offset C0h

External Timer Control Register

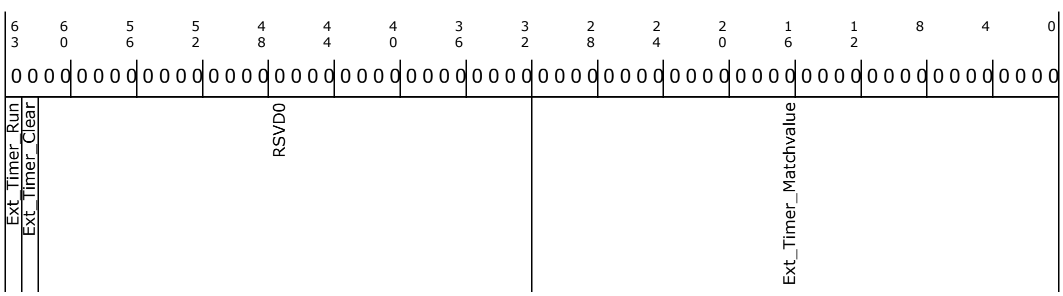
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

EXT_TIMER_CNTL: [BAR + 140000h] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**Ext_Timer_Run:** Timer Run bit. The timer runs only when this bit is set. It resumes running from the current value in the readvalue bits. Clearing the bit pauses the timer.
62	0b RW/S	**Ext_Timer_Clear:** Timer Clear bit. Clears the timer and sets the value back to zero. This should also be reflected in the readvalue bits

Bit Range	Default & Access	Description
61:32	0b RO	**RSVD0:** Reserved
31:0	0b RW	**Ext_Timer_Matchvalue:** The timer will generate a pulse when the Readvalue reaches Matchvalue. The pulse causes a level interrupt to get set in the PISR register. The PISR interrupt needs to be cleared before the next pulse is generated. The timer keeps counting beyond the Readvalue. Setting the Matchvalue to zero makes this a free running timer and no interrupt will be generated in this case. For correct operation, the ISR should either set a new Matchvalue or set it to zero. If nothing is done, the timer will roll over and trigger an interrupt again when it reaches the Matchvalue.

21.11.26 reg_EXT_TIMER_STAT_type (EXT_TIMER_STAT)—Offset C8h

External Timer Control Register

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

EXT_TIMER_STAT: [BAR + 140000h] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	
RSVD0								Ext_Timer_Readvalue								

Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:0	0b RO	**Ext_Timer_Readvalue:** Shows the current count value of the timer

21.11.27 reg_S0ix_TIMER_CNTL_type (S0ix_TIMER_CNTL)—Offset D0h

External Timer Control Register

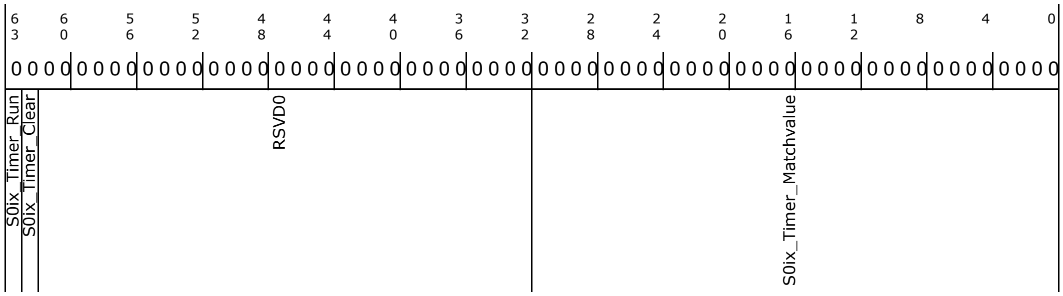
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

S0ix_TIMER_CNTL: [BAR + 140000h] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63	0b RW	**S0ix_Timer_Run:** Timer Run bit. The timer runs only when this bit is set. It resumes running from the current value in the readvalue bits. Clearing the bit pauses the timer.
62	0b RW/S	**S0ix_Timer_Clear:** Timer Clear bit. Clears the timer and sets the value back to zero. This should also be reflected in the readvalue bits
61:32	0b RO	**RSVD0:** Reserved
31:0	0b RW	**S0ix_Timer_Matchvalue:** The timer will generate a pulse when the Readvalue reaches Matchvalue. The pulse causes a level interrupt to get set in the PISR register. The PISR interrupt needs to be cleared before the next pulse is generated. The timer keeps counting beyond the Readvalue. Setting the Matchvalue to zero makes this a free running timer and no interrupt will be generated in this case. For correct operation, the ISR should either set a new Matchvalue or set it to zero. If nothing is done, the timer will roll over and trigger an interrupt again when it reaches the Matchvalue.

21.11.28 reg_S0ix_TIMER_STAT_type (S0ix_TIMER_STAT)—Offset D8h

External Timer Control Register

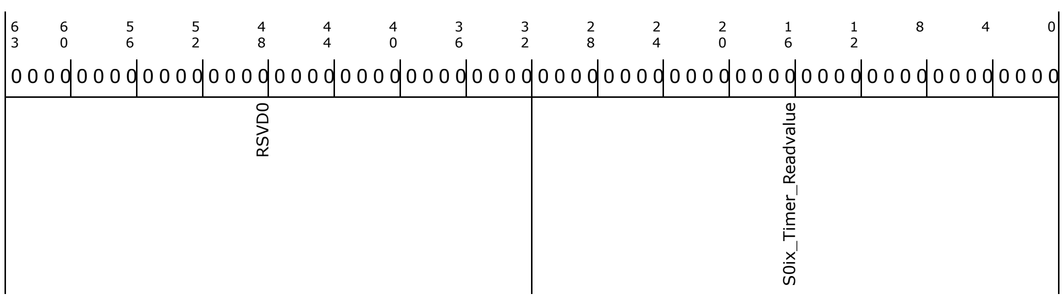
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

S0ix_TIMER_STAT: [BAR + 140000h] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
31:0	0b RO	**S0ix_Timer_Readvalue:** Shows the current count value of the timer

21.11.29 reg_RAW_PISR_type (XT_RAW_PISR)—Offset E0h

RAW PISR

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

XT_RAW_PISR: [BAR + 140000h] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

RSVD0	RAW_PIS_DMA1	RAW_PIS_DMA0	RSVD1	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD2

Bit Range	Default & Access	Description
63:32	0b RO	**RSVD0:** Reserved
31:24	00000000b RO	**RAW_PIS_DMA1:** DMA 1 interrupts
23:16	00000000b RO	**RAW_PIS_DMA0:** DMA 0 interrupts
15:10	0b RO	**RSVD1:** Reserved
9	0b RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Reserved (RSVD):** Reserved.
7	0b RO	**Reserved (RSVD):** Reserved.
6	0b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
2:0	0b RO	**RSVD2:** Reserved

21.11.30 reg_SSP0_DIV_CTRL_type (SSP0_DIV_CTRL)—Offset E8h

SSP0 M/N Clock Divider control - Add for VLV

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

SSP0_DIV_CTRL: [BAR + 140000h] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 8000000100000001h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Divider_Bypass | Divider_En | Divider_Update | RSVD0 | Divider_M | RSVD1 | Divider_N

Bit Range	Default & Access	Description
63	1b RW	**Divider_Bypass:** SSP0 Bypass divider
62	0b RW	**Divider_En:** SSP0 Enable divider
61	0b RW	**Divider_Update:** SSP0 Update divider
60:52	0b RO	**RSVD0:** Reserved
51:32	1b RW	**Divider_M:** SSP0 Nominator value
31:20	0b RO	**RSVD1:** Reserved
19:0	1b RW	**Divider_N:** SSP0 Denominator value

21.11.31 reg_SSP1_DIV_CTRL_type (SSP1_DIV_CTRL)—Offset F0h

SSP1 M/N Clock Divider control - Add for VLV

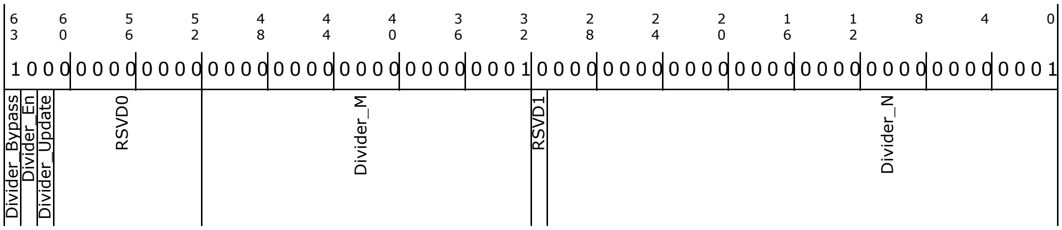
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

SSP1_DIV_CTRL: [BAR + 140000h] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 8000000100000001h



Bit Range	Default & Access	Description
63	1b RW	**Divider_Bypass:** SSP1 Bypass divider
62	0b RW	**Divider_En:** SSP1 Enable divider
61	0b RW	**Divider_Update:** SSP1 Update divider
60:52	0b RO	**RSVD0:** Reserved
51:32	1b RW	**Divider_M:** SSP1 Nominator value
31:20	0b RO	**RSVD1:** Reserved
19:0	1b RW	**Divider_N:** SSP1 Denominator value

21.11.32 reg_SSP2_DIV_CTRL_type (SSP2_DIV_CTRL)—Offset F8h

SSP2 M/N Clock Divider control - Add for VLV

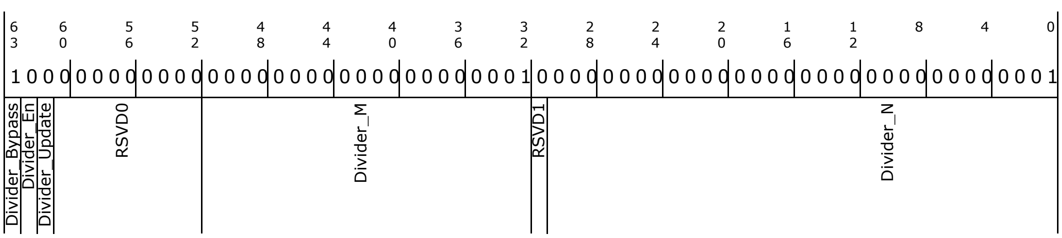
Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

SSP2_DIV_CTRL: [BAR + 140000h] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 8000000100000001h



Bit Range	Default & Access	Description
63	1b RW	**Divider_Bypass:** SSP2 Bypass divider

Bit Range	Default & Access	Description
62	0b RW	**Divider_En:** SSP2 Enable divider
61	0b RW	**Divider_Update:** SSP2 Update divider
60:52	0b RO	**RSVD0:** Reserved
51:32	1b RW	**Divider_M:** SSP2 Nominator value
31:20	0b RO	**RSVD1:** Reserved
19:0	1b RW	**Divider_N:** SSP2 Denominator value

21.12 Low Power Audio I^{2}S0 Address Map

Table 234. Summary of Low Power Audio I^{2}S0 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	“SSP Control 0 Register (SSCR0)—Offset 0h” on page 2876	00000000h
4h	4	“SSP Control 1 Register (SSCR1)—Offset 4h” on page 2877	43000000h
8h	4	“SSP Status Register (SSSR)—Offset 8h” on page 2879	0000F004h
Ch	4	“SSP Interupt Test Register (SSITR)—Offset Ch” on page 2881	00000000h
10h	4	“SSP Data Register (SSDR)—Offset 10h” on page 2881	00000000h
28h	4	“SSP Time-Out Regsiter (SSTO)—Offset 28h” on page 2882	00000000h
2Ch	4	“SSP Programmable Protocol Register (SSPSP)—Offset 2Ch” on page 2883	00000000h
30h	4	“SSM TX Time Slot Active Register (SSTSA)—Offset 30h” on page 2884	00000000h
34h	4	“SSP RX Time Slot Active Register (SSRSA)—Offset 34h” on page 2884	00000000h
38h	4	“SSP Time Slot Status Register (SSTSS)—Offset 38h” on page 2885	00000000h
3Ch	4	“SSP Audio Clock Divider (SSACD)—Offset 3Ch” on page 2885	00000000h
40h	4	“SSP Control 2 Register (SSCR2)—Offset 40h” on page 2886	000000C0h
44h	4	“SSP Frame Select Register (SSFS)—Offset 44h” on page 2887	00000001h
48h + [0-7]*4h	4	“SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h” on page 2888	00000000h
68h	4	“SSP FIFO Level Register (SFIFOL)—Offset 68h” on page 2889	FFFF0000h
6Ch	4	“SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch” on page 2889	00000000h
70h	4	“SSP Control 3 Register (SSCR3)—Offset 70h” on page 2890	0002C604h
74h	4	“SSP Control 4 Register (SSCR4)—Offset 74h” on page 2891	00000000h
78h	4	“SSP Control 5 Register (SSCR5)—Offset 78h” on page 2892	00000000h
7Ch	4	“ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch” on page 2893	00000000h
80h	4	“Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h” on page 2893	00000000h
84h	4	“ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h” on page 2894	00000000h
88h	4	“ASRC Frame Count (ASRC_FRMCNT)—Offset 88h” on page 2894	00000000h

21.12.1 SSP Control 0 Register (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR0: [BAR + 0A0000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MOD	ACS	RSVD	RSVD	RSVD	FRDC	TIM	RIM	NCS	EDSS	SCR	SSE	ECS	FRF	DSS

Bit Range	Default & Access	Description
31	0b RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0b RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0b RO	**Reserved (RSVD):** Reserved.
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26:24	000b RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0b RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0b RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0b RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0b RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0b RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	00b RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0000b RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

21.12.2 SSP Control 1 Register (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSCR1: [BAR + 0A0000h] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 43000000h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TTELP	TTE	EBCEI	SCFR	ECRA	ECRB	SCLKDIR	SFRMDIR	RWOT	TRAIL	TSRE	RSRE	TINTE	PINTE	RSVD	IFS	STRF	EFWR	RFT				TFT				MWDS	SPH	SPO	LBM	TIE	RIE

Bit Range	Default & Access	Description
31	0b RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	1b RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0b RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
28	0b RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0b RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0b RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	1b RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	1b RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0b RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0b RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0b RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0b RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0b RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0b RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0b RW	**RSVD:** Reserved
16	0b RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)

Bit Range	Default & Access	Description
15	0b RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0b RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled
13:10	0000b RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0000b RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0b RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0b RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0b RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0b RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0b RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0b RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

21.12.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSSR: [BAR + 0A0000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000F004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0

Fields: RSVD1, ASRC_Interrupt, BCE, CSS, TUR, EOC, TINT, PINT, RSVD2, RFL, TFL, ROR, RFS, TFS, BSY, RNE, TNF, RSVD3

Bit Range	Default & Access	Description
31:25	00h RO	**RSVD1:** Reserved
24	0b RW/1C	**ASRC Interrupt (ASRC_Interrupt):** The interrupt bit is set to 1 when the frame count matches the frame threshold. This is Write 1 to clear register bit.
23	0b RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0b RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0b RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0b RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0b RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0b RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	00b RO	**RSVD2:** Reserved
15:12	1111b RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0000b RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0b RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0b RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0b RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0b RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0b RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1b RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full

Bit Range	Default & Access	Description
1:0	00b RO	**RSVD3:** Reserved

21.12.4 SSP Interupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSITR: [BAR + 0A0000h] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD1																								TROR	TRFS	TTFS	RSVD2				

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD1:** Reserved
7	0b RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0b RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0b RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	00000b RO	**RSVD2:** Reserved

21.12.5 SSP Data Register (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the

register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**SSDR:** [BAR + 0A0000h] + 10h
	BAR Type: PCI Configuration Register (Size: 32 bits) **BAR Reference:** [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA																															

Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

21.12.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes and reads are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**SSTO:** [BAR + 0A0000h] + 28h
	BAR Type: PCI Configuration Register (Size: 32 bits) **BAR Reference:** [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								TIMEOUT																							

Bit Range	Default & Access	Description
31:24	00h RO	**RSVD:** Reserved
23:0	000000h RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

21.12.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSPSP: [BAR + 0A0000h] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits 31, 28, 24, 20, 16, 12, 8, 4, 0 — all 32 bits: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

RSVD1	FSRT	DMYSTOP	RSVD2	SFRMWDTH	SFRMDLY	DMYSTRT	STRTDLY	ETDS	SFRMP	SCMODE

Bit Range	Default & Access	Description
31:26	000000b RO	**RSVD1:** Reserved
25	0b RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	00b RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0b RW	**RSVD2:** Reserved
21:16	000000b RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0000000b RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	00b RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	000b RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0b RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)

Bit Range	Default & Access	Description
2	0b RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	00b RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

21.12.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSA: [BAR + 0A0000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								TTSA							

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

21.12.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSRSA: [BAR + 0A0000h] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:8	7:0
Default	000000000000000000000000	00000000
Field	RSVD	RTSA

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

21.12.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTSS: [BAR + 0A0000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31	30:3	2:0
Default	0	0000000000000000000000000000	000
Field	NMBSY	RSVD	TSS

Bit Range	Default & Access	Description
31	0b RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0000000h RO	**RSVD:** Reserved
2:0	000b RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

21.12.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the

SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSACD: [BAR + 0A0000h] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																									ACPS			SCDB	ACDS		

Bit Range	Default & Access	Description
31:7	0000000h RO	**RSVD:** Reserved
6:4	000b RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0b RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	000b RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

21.12.12 SSP Control 2 Register (SSCR2)—Offset 40h

The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR2: [BAR + 0A0000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 000000C0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
RSVD0																				ASRC_INTR_MASK	ASRC_FRM_CNTR_EN	ASRC_CNTR_CLR	ASRC_CNTR_EN	FIFO_EMPTY_FIX_EN	UNDRN_FIX_EN	Reserved		CLK_DEL_EN	SLV_EXT_CLK_RUN_EN	Underrun_fix_1	Underrun_fix_0

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold. Software should override this bit, since it have no reset value
10	0b RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.
9	0b RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0b RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	1b RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	1b RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5:4	00b RW	**Reserved:** This is a RW bit with no effect on IP behavior
3	0b RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0b RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0b RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0b RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

21.12.13 SSP Frame Select Register (SSFS)—Offset 44h

The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSFS: [BAR + 0A0000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
RSVD0																												FRAME_SEL			

Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3:0	0001b RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

21.12.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FRAME_CNT[0-7]: [BAR + 0A0000h] + 48h + [0-7]*4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FCNT_EN	RSVD0						FCNT_RST	FCNT																							

Bit Range	Default & Access	Description
31	0b RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0b RO	**RSVD0:** Reserved
24	0b WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	000000h RO	**Slot Frame Count (FCNT):** SSP frame count.

21.12.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOL: [BAR + 0A0000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: FFFF0000h

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							RFL																TFL								

Bit Range	Default & Access	Description
31:16	FFFFh RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0000h RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

21.12.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOTT: [BAR + 0A0000h] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							RFT																TFT								

Bit Range	Default & Access	Description
31:16	0000h RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0000h RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

21.12.17 SSP Control 3 Register (SSCR3)—Offset 70h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSCR3: [BAR + 0A0000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0002C604h

Bits	Default	Field
31:18	0000 0000 0000 00	RSVD0
17	1	SYN_FIX_EN
16	0	MST_CLK_EN
15	1	STRETCH_RX
14	1	STRETCH_TX
13	0	RSVD
12	0	RSVD
11	0	I2S_VISA_EN
10	1	I2S_RX_EN
9	1	I2S_TX_EN
8	0	RSVD
7:6	0 0	RSVD
5	0	RSVD
4	0	I2S_RX_SS_FIX_EN
3	0	I2S_TX_SS_FIX_EN
2	1	RSVD
1	0	I2S_MODE_EN
0	0	FRM_MST_EN

Bit Range	Default & Access	Description
31:18	0b RO	**RSVD0:** Reserved
17	1b RW	**Sync Fix Enable (SYN_FIX_EN):** This is a chicken bit for enabling the synchronizer fix for clr_underrun_ssp signal. SW should preserve this bit at its default value.
16	0b RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	1b RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	1b RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.

Bit Range	Default & Access	Description
13	0b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	0b RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	1b RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	1b RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0b RO	**Reserved (RSVD):** Reserved.
7:6	00b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0b RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0b RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

21.12.18 SSP Control 4 Register (SSCR4)—Offset 74h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR4: [BAR + 0A0000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:16	15:7	6:0
Value	0000 0000 0000 0000	0000 0000 0	000 0000
Field	RSVD0	TOT_FRM_PRD	RSVD

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	00h RO	**Reserved (RSVD):** Reserved.

21.12.19 SSP Control 5 Register (SSCR5)—Offset 78h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR5: [BAR + 0A0000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:26	25:1	0
Value	0000 00	00 0000 0000 0000 0000 0000 000	0
Field	RSVD0	FRM_ASRT_WIDTH	RSVD

Bit Range	Default & Access	Description
31:26	0b RO	**RSVD0:** Reserved
25:1	0000000h RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.

Bit Range	Default & Access	Description
0	0b RO	**Reserved (RSVD):** Reserved.

21.12.20 ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch

This is a 32 bit free running counter that can be enabled, paused or cleared using bits in the SSCR2_XR register. The value reflected here will be noted down in the timer snapshot register when the frame count matches the frame threshold

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FRT: [BAR + 0A0000h] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FREE_RUN_TIMER

Bit Range	Default & Access	Description
31:0	00000000h RO/V	**ASRC free running timer (FREE_RUN_TIMER):** This field reflects the value of the free running timer.

21.12.21 Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h

The frame threshold value at which the timer snapshot will be taken is written here.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FTC: [BAR + 0A0000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:16) | ASRC_FTC (bits 15:0)

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RW	**ASRC Frame Threshold (ASRC_FTC):** The 16 bit frame threshold value needs to be written here. Every time the frame count matches the frame threshold a snapshot of the free running timer will be taken and stored in the snapshot register. An interrupt will be generated as well. If the frame threshold is changed on the fly during operation then the following behavior is expected. Previous value = A, New value value = B If B) A : The frame counter keeps counting up to the new value. Nothing happens when the frame counter reaches the old value of A. If B (A : The frame counter resets to zero on the next frame. No interrupt or snapshot is generated in this case.

21.12.22 ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h

Frame Snapshot Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ASRC_SNPSHT: [BAR + 0A0000h] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ASRC_TIMER_SNAPSHOT

Bit Range	Default & Access	Description
31:0	00000000h RO	**ASRC Frame Snapshot (ASRC_TIMER_SNAPSHOT):** This field holds the 32 bit snapshot value. The value is noted on the clock cycle when the frame threshold matches the frame count.

21.12.23 ASRC Frame Count (ASRC_FRMCNT)—Offset 88h

Frame Count Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ASRC_FRMCNT: [BAR + 0A0000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																ASRC_FRM_COUNT															

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RO	**ASRC Frame Count (ASRC_FRM_COUNT):** This is the current frame count. This is a debug register and the value is noted in this register only when the LSB of the frame counter flips. If the counter is cleared when it was at an even value, the cleared value is not reflected here.

21.13 Low Power Audio I^2S0 Address Map

Table 235. Summary of Low Power Audio I^2S0 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 2896	00000000h
4h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 2897	43000000h
8h	4	"SSP Status Register (SSSR)—Offset 8h" on page 2899	0000F004h
Ch	4	"SSP Interupt Test Register (SSITR)—Offset Ch" on page 2901	00000000h
10h	4	"SSP Data Register (SSDR)—Offset 10h" on page 2901	00000000h
28h	4	"SSP Time-Out Regsiter (SSTO)—Offset 28h" on page 2902	00000000h
2Ch	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 2903	00000000h
30h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 2904	00000000h
34h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 2904	00000000h
38h	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 2905	00000000h
3Ch	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 2905	00000000h
40h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 2906	000000C0h
44h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 2907	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 2908	00000000h
68h	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 2909	FFFF0000h
6Ch	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 2909	00000000h
70h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 2910	0002C604h
74h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 2911	00000000h
78h	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 2912	00000000h
7Ch	4	"ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch" on page 2913	00000000h
80h	4	"Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h" on page 2913	00000000h
84h	4	"ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h" on page 2914	00000000h
88h	4	"ASRC Frame Count (ASRC_FRMCNT)—Offset 88h" on page 2914	00000000h

21.13.1 SSP Control 0 Register (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR0: [BAR + 0A1000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

MOD	ACS	RSVD	RSVD	RSVD	FRDC	TIM	RIM	NCS	EDSS	SCR	SSE	ECS	FRF	DSS
0	0	0	0	0	0 0 0	0	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0	0	0	0 0	0 0 0 0

Bit Range	Default & Access	Description
31	0b RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0b RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0b RO	**Reserved (RSVD):** Reserved.
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26:24	000b RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0b RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0b RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0b RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0b RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0b RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	00b RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0000b RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

21.13.2 SSP Control 1 Register (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSCR1: [BAR + 0A1000h] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 43000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TTELP	TTE	EBCEI	SCFR	ECRA	ECRB	SCLKDIR	SFRMDIR	RWOT	TRAIL	TSRE	RSRE	TINTE	PINTE	RSVD	IFS	STRF	EFWR	RFT				TFT				MWDS	SPH	SPO	LBM	TIE	RIE

Bit Range	Default & Access	Description
31	0b RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	1b RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0b RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
28	0b RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0b RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0b RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	1b RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	1b RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0b RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0b RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0b RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0b RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0b RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0b RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0b RW	**RSVD:** Reserved
16	0b RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)

Bit Range	Default & Access	Description
15	0b RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0b RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled
13:10	0000b RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0000b RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0b RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0b RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0b RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0b RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0b RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0b RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

21.13.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSSR: [BAR + 0A1000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000F004h

31	28	24	20	16	12	8	4	0
	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	0 1 0 0

RSVD1	ASRC_Interrupt	BCE	CSS	TUR	EOC	TINT	PINT	RSVD2	RFL	TFL	ROR	RFS	TFS	BSY	RNE	TNF	RSVD3

Bit Range	Default & Access	Description
31:25	00h RO	**RSVD1:** Reserved
24	0b RW/1C	**ASRC Interrupt (ASRC_Interrupt):** The interrupt bit is set to 1 when the frame count matches the frame threshold. This is Write 1 to clear register bit.
23	0b RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0b RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0b RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0b RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0b RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0b RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	00b RO	**RSVD2:** Reserved
15:12	1111b RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0000b RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0b RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0b RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0b RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0b RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0b RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1b RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full

Bit Range	Default & Access	Description
1:0	00b RO	**RSVD3:** Reserved

21.13.4 SSP Interupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSITR: [BAR + 0A1000h] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD1																								TROR	TRFS	TTFS	RSVD2				

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD1:** Reserved
7	0b RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0b RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0b RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	00000b RO	**RSVD2:** Reserved

21.13.5 SSP Data Register (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the

register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSDR: [BAR + 0A1000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA																															

Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

21.13.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes and reads are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTO: [BAR + 0A1000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								TIMEOUT																							

Bit Range	Default & Access	Description
31:24	00h RO	**RSVD:** Reserved
23:0	000000h RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

21.13.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSPSP: [BAR + 0A1000h] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD1	FSRT	DMYSTOP	RSVD2	SFRMWDTH	SFRMDLY	DMYSTRT	STRTDLY	ETDS	SFRMP	SCMODE

Bit Range	Default & Access	Description
31:26	000000b RO	**RSVD1:** Reserved
25	0b RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	00b RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0b RW	**RSVD2:** Reserved
21:16	000000b RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0000000b RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	00b RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	000b RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0b RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)

Bit Range	Default & Access	Description
2	0b RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	00b RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

21.13.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTSA: [BAR + 0A1000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								TTSA							

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

21.13.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSRSA: [BAR + 0A1000h] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD | RTSA

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

21.13.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTSS: [BAR + 0A1000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

NMBSY | RSVD | TSS

Bit Range	Default & Access	Description
31	0b RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0000000h RO	**RSVD:** Reserved
2:0	000b RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

21.13.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the

SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSACD: [BAR + 0A1000h] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:7	6:4	3	2:0
Default	0000000 0000 0000 0000 0000 0000 0	000	0	000
Field	RSVD	ACPS	SCDB	ACDS

Bit Range	Default & Access	Description
31:7	0000000h RO	**RSVD:** Reserved
6:4	000b RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0b RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	000b RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

21.13.12 SSP Control 2 Register (SSCR2)—Offset 40h

The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR2: [BAR + 0A1000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 000000C0h

Bits	31:12	11	10	9	8	7	6	5:4	3	2	1	0
Default	0000 0000 0000 0000 0000	0	0	0	0	1	1	00	0	0	0	0
Field	RSVD0	ASRC_INTR_MASK	ASRC_FRM_CNTR_EN	ASRC_CNTR_CLR	ASRC_CNTR_EN	FIFO_EMPTY_FIX_EN	UNDRN_FIX_EN	Reserved	CLK_DEL_EN	SLV_EXT_CLK_RUN_EN	Underrun_fix_1	Underrun_fix_0

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold. Software should override this bit, since it have no reset value
10	0b RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.
9	0b RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0b RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	1b RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	1b RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5:4	00b RW	**Reserved:** This is a RW bit with no effect on IP behavior
3	0b RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0b RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0b RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0b RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

21.13.13 SSP Frame Select Register (SSFS)—Offset 44h

The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSFS: [BAR + 0A1000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000001h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	

RSVD0 (31:4)	FRAME_SEL (3:0)

Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3:0	0001b RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

21.13.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

FRAME_CNT[0-7]: [BAR + 0A1000h] + 48h + [0-7]*4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

FCNT_EN (31)	RSVD0 (30:25)	FCNT_RST (24)	FCNT (23:0)

Bit Range	Default & Access	Description
31	0b RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0b RO	**RSVD0:** Reserved
24	0b WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	000000h RO	**Slot Frame Count (FCNT):** SSP frame count.

21.13.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOL: [BAR + 0A1000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: FFFF0000h

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RFL																TFL															

Bit Range	Default & Access	Description
31:16	FFFFh RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0000h RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

21.13.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOTT: [BAR + 0A1000h] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RFT																TFT															

Bit Range	Default & Access	Description
31:16	0000h RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0000h RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

21.13.17 SSP Control 3 Register (SSCR3)—Offset 70h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSCR3: [BAR + 0A1000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0002C604h

Bit(s)	Default	Field
31:18	0 0 0 0 0 0 0 0 0 0 0 0 0 0	RSVD0
17	1	SYN_FIX_EN
16	0	MST_CLK_EN
15	1	STRETCH_RX
14	1	STRETCH_TX
13	0	RSVD
12	0	RSVD
11	0	I2S_VISA_EN
10	1	I2S_RX_EN
9	1	I2S_TX_EN
8	0	RSVD
7:6	0 0	RSVD
5	0	RSVD
4	0	I2S_RX_SS_FIX_EN
3	0	I2S_TX_SS_FIX_EN
2	1	RSVD
1	0	I2S_MODE_EN
0	0	FRM_MST_EN

Bit Range	Default & Access	Description
31:18	0b RO	**RSVD0:** Reserved
17	1b RW	**Sync Fix Enable (SYN_FIX_EN):** This is a chicken bit for enabling the synchronizer fix for clr_underrun_ssp signal. SW should preserve this bit at its default value.
16	0b RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	1b RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	1b RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.

Bit Range	Default & Access	Description
13	0b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	0b RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	1b RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	1b RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0b RO	**Reserved (RSVD):** Reserved.
7:6	00b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0b RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0b RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

21.13.18 SSP Control 4 Register (SSCR4)—Offset 74h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSCR4: [BAR + 0A1000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:7	Bits 6:0
RSVD0	TOT_FRM_PRD	RSVD

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	00h RO	**Reserved (RSVD):** Reserved.

21.13.19 SSP Control 5 Register (SSCR5)—Offset 78h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSCR5: [BAR + 0A1000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:26	Bits 25:1	Bit 0
RSVD0	FRM_ASRT_WIDTH	RSVD

Bit Range	Default & Access	Description
31:26	0b RO	**RSVD0:** Reserved
25:1	0000000h RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.

Bit Range	Default & Access	Description
0	0b RO	**Reserved (RSVD):** Reserved.

21.13.20 ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch

This is a 32 bit free running counter that can be enabled, paused or cleared using bits in the SSCR2_XR register. The value reflected here will be noted down in the timer snapshot register when the frame count matches the frame threshold

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ASRC_FRT: [BAR + 0A1000h] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FREE_RUN_TIMER

Bit Range	Default & Access	Description
31:0	00000000h RO/V	**ASRC free running timer (FREE_RUN_TIMER):** This field reflects the value of the free running timer.

21.13.21 Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h

The frame threshold value at which the timer snapshot will be taken is written here.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ASRC_FTC: [BAR + 0A1000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | ASRC_FTC

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RW	**ASRC Frame Threshold (ASRC_FTC):** The 16 bit frame threshold value needs to be written here. Every time the frame count matches the frame threshold a snapshot of the free running timer will be taken and stored in the snapshot register. An interrupt will be generated as well. If the frame threshold is changed on the fly during operation then the following behavior is expected. Previous value = A, New value value = B If B) A : The frame counter keeps counting up to the new value. Nothing happens when the frame counter reaches the old value of A. If B (A : The frame counter resets to zero on the next frame. No interrupt or snapshot is generated in this case.

21.13.22 ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h

Frame Snapshot Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ASRC_SNPSHT: [BAR + 0A1000h] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ASRC_TIMER_SNAPSHOT

Bit Range	Default & Access	Description
31:0	00000000h RO	**ASRC Frame Snapshot (ASRC_TIMER_SNAPSHOT):** This field holds the 32 bit snapshot value. The value is noted on the clock cycle when the frame threshold matches the frame count.

21.13.23 ASRC Frame Count (ASRC_FRMCNT)—Offset 88h

Frame Count Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ASRC_FRMCNT: [BAR + 0A1000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:16) | ASRC_FRM_COUNT (bits 15:0)

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RO	**ASRC Frame Count (ASRC_FRM_COUNT):** This is the current frame count. This is a debug register and the value is noted in this register only when the LSB of the frame counter flips. If the counter is cleared when it was at an even value, the cleared value is not reflected here.

21.14 Low Power Audio I^{2}S0 Address Map

Table 236. Summary of Low Power Audio I^{2}S0 Memory Mapped I/O Registers—BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 2916	00000000h
4h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 2917	43000000h
8h	4	"SSP Status Register (SSSR)—Offset 8h" on page 2919	0000F004h
Ch	4	"SSP Interupt Test Register (SSITR)—Offset Ch" on page 2921	00000000h
10h	4	"SSP Data Register (SSDR)—Offset 10h" on page 2921	00000000h
28h	4	"SSP Time-Out Regsiter (SSTO)—Offset 28h" on page 2922	00000000h
2Ch	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 2923	00000000h
30h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 2924	00000000h
34h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 2924	00000000h
38h	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 2925	00000000h
3Ch	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 2925	00000000h
40h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 2926	000000C0h
44h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 2927	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 2928	00000000h
68h	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 2929	FFFF0000h
6Ch	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 2929	00000000h
70h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 2930	0002C604h
74h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 2931	00000000h
78h	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 2932	00000000h
7Ch	4	"ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch" on page 2933	00000000h
80h	4	"Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h" on page 2933	00000000h
84h	4	"ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h" on page 2934	00000000h
88h	4	"ASRC Frame Count (ASRC_FRMCNT)—Offset 88h" on page 2934	00000000h

21.14.1 SSP Control 0 Register (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR0: [BAR + 0A2000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MOD	ACS	RSVD	RSVD	RSVD	FRDC			TIM	RIM	NCS	EDSS	SCR												SSE	ECS	FRF		DSS			

Bit Range	Default & Access	Description
31	0b RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0b RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0b RO	**Reserved (RSVD):** Reserved.
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26:24	000b RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0b RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0b RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0b RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0b RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0b RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	00b RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0000b RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

21.14.2 SSP Control 1 Register (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSCR1: [BAR + 0A2000h] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 43000000h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TTELP	TTE	EBCEI	SCFR	ECRA	ECRB	SCLKDIR	SFRMDIR	RWOT	TRAIL	TSRE	RSRE	TINTE	PINTE	RSVD	IFS	STRF	EFWR	RFT				TFT				MWDS	SPH	SPO	LBM	TIE	RIE

Bit Range	Default & Access	Description
31	0b RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	1b RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0b RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
28	0b RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0b RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0b RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	1b RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	1b RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0b RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0b RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0b RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0b RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0b RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0b RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0b RW	**RSVD:** Reserved
16	0b RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)

Bit Range	Default & Access	Description
15	0b RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0b RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled
13:10	0000b RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0000b RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0b RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0b RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0b RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0b RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0b RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0b RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

21.14.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSSR: [BAR + 0A2000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0000F004h

31	28	24	20	16	12	8	4	0
	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	0 1 0 0

RSVD1	ASRC_Interrupt	BCE	CSS	TUR	EOC	TINT	PINT	RSVD2	RFL	TFL	ROR	RFS	TFS	BSY	RNE	TNF	RSVD3

Bit Range	Default & Access	Description
31:25	00h RO	**RSVD1:** Reserved
24	0b RW/1C	**ASRC Interrupt (ASRC_Interrupt):** The interrupt bit is set to 1 when the frame count matches the frame threshold. This is Write 1 to clear register bit.
23	0b RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0b RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0b RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0b RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0b RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0b RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	00b RO	**RSVD2:** Reserved
15:12	1111b RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0000b RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0b RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0b RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0b RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0b RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0b RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1b RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full

Bit Range	Default & Access	Description
1:0	00b RO	**RSVD3:** Reserved

21.14.4 SSP Interupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSITR: [BAR + 0A2000h] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD1																								TROR	TRFS	TTFS	RSVD2				

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD1:** Reserved
7	0b RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0b RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0b RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	00000b RO	**RSVD2:** Reserved

21.14.5 SSP Data Register (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the

register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSDR: [BAR + 0A2000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA																															

Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

21.14.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes and reads are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTO: [BAR + 0A2000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								TIMEOUT																							

Bit Range	Default & Access	Description
31:24	00h RO	**RSVD:** Reserved
23:0	000000h RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

21.14.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSPSP: [BAR + 0A2000h] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD1						FSRT	DMYSTOP		RSVD2	SFRMWDTH						SFRMDLY							DMYSTRT		STRTDLY			ETDS	SFRMP	SCMODE	

Bit Range	Default & Access	Description
31:26	000000b RO	**RSVD1:** Reserved
25	0b RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	00b RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0b RW	**RSVD2:** Reserved
21:16	000000b RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0000000b RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	00b RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	000b RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0b RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)

Bit Range	Default & Access	Description
2	0b RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	00b RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

21.14.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTSA: [BAR + 0A2000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								TTSA							

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

21.14.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSRSA: [BAR + 0A2000h] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
											RSVD																	RTSA			

Bit Range	Default & Access	Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

21.14.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTSS: [BAR + 0A2000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NMBSY														RSVD																TSS	

Bit Range	Default & Access	Description
31	0b RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0000000h RO	**RSVD:** Reserved
2:0	000b RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

21.14.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the

SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSACD: [BAR + 0A2000h] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:7	6:4	3	2:0
Value	0000 0000 0000 0000 0000 0000 0	000	0	000
Field	RSVD	ACPS	SCDB	ACDS

Bit Range	Default & Access	Description
31:7	0000000h RO	**RSVD:** Reserved
6:4	000b RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0b RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	000b RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

21.14.12 SSP Control 2 Register (SSCR2)—Offset 40h

The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR2: [BAR + 0A2000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 000000C0h

Bits	31:12	11	10	9	8	7	6	5:4	3	2	1	0
Value	0000 0000 0000 0000 0000	0	0	0	0	1	1	00	0	0	0	0
Field	RSVD0	ASRC_INTR_MASK	ASRC_FRM_CNTR_EN	ASRC_CNTR_CLR	ASRC_CNTR_EN	FIFO_EMPTY_FIX_EN	UNDRN_FIX_EN	Reserved	CLK_DEL_EN	SLV_EXT_CLK_RUN_EN	Underrun_fix_1	Underrun_fix_0

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold. Software should override this bit, since it have no reset value
10	0b RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.
9	0b RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0b RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	1b RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	1b RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5:4	00b RW	**Reserved:** This is a RW bit with no effect on IP behavior
3	0b RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0b RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0b RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0b RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

21.14.13 SSP Frame Select Register (SSFS)—Offset 44h

The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSFS: [BAR + 0A2000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000001h

Bit	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1
Field	RSVD0							FRAME_SEL

Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3:0	0001b RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

21.14.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FRAME_CNT[0-7]: [BAR + 0A2000h] + 48h + [0-7]*4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bit	31	30:28	27:25	24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0	0 0 0	0 0 0	0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Field	FCNT_EN	RSVD0		FCNT_RST	FCNT					

Bit Range	Default & Access	Description
31	0b RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0b RO	**RSVD0:** Reserved
24	0b WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	000000h RO	**Slot Frame Count (FCNT):** SSP frame count.

21.14.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOL: [BAR + 0A2000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: FFFF0000h

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RFL (bits 31:16), TFL (bits 15:0)

Bit Range	Default & Access	Description
31:16	FFFFh RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0000h RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

21.14.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SFIFOTT: [BAR + 0A2000h] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RFT (bits 31:16), TFT (bits 15:0)

Bit Range	Default & Access	Description
31:16	0000h RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0000h RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

21.14.17 SSP Control 3 Register (SSCR3)—Offset 70h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSCR3: [BAR + 0A2000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 0002C604h

Bits	Default	Field
31:18	0000 0000 0000 00	RSVD0
17	1	SYN_FIX_EN
16	0	MST_CLK_EN
15	1	STRETCH_RX
14	1	STRETCH_TX
13	0	RSVD
12	0	RSVD
11	0	I2S_VISA_EN
10	1	I2S_RX_EN
9	1	I2S_TX_EN
8	0	RSVD
7:6	00	RSVD
5	0	RSVD
4	0	I2S_RX_SS_FIX_EN
3	0	I2S_TX_SS_FIX_EN
2	1	RSVD
1	0	I2S_MODE_EN
0	0	FRM_MST_EN

Bit Range	Default & Access	Description
31:18	0b RO	**RSVD0:** Reserved
17	1b RW	**Sync Fix Enable (SYN_FIX_EN):** This is a chicken bit for enabling the synchronizer fix for clr_underrun_ssp signal. SW should preserve this bit at its default value.
16	0b RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	1b RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	1b RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.

Bit Range	Default & Access	Description
13	0b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	0b RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	1b RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	1b RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0b RO	**Reserved (RSVD):** Reserved.
7:6	00b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0b RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue, similar to PNW/CLV. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0b RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

21.14.18 SSP Control 4 Register (SSCR4)—Offset 74h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR4: [BAR + 0A2000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | TOT_FRM_PRD | RSVD

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	00h RO	**Reserved (RSVD):** Reserved.

21.14.19 SSP Control 5 Register (SSCR5)—Offset 78h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode with the Tangier fixes. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSCR5: [BAR + 0A2000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | FRM_ASRT_WIDTH | RSVD

Bit Range	Default & Access	Description
31:26	0b RO	**RSVD0:** Reserved
25:1	0000000h RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.

Bit Range	Default & Access	Description
0	0b RO	**Reserved (RSVD):** Reserved.

21.14.20 ASRC Free Running Timer (ASRC_FRT)—Offset 7Ch

This is a 32 bit free running counter that can be enabled, paused or cleared using bits in the SSCR2_XR register. The value reflected here will be noted down in the timer snapshot register when the frame count matches the frame threshold

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FRT: [BAR + 0A2000h] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:0
Default	0000 0000 0000 0000 0000 0000 0000 0000
Field	FREE_RUN_TIMER

Bit Range	Default & Access	Description
31:0	00000000h RO/V	**ASRC free running timer (FREE_RUN_TIMER):** This field reflects the value of the free running timer.

21.14.21 Frame Threshold for ASRC Frame Count (ASRC_FTC)—Offset 80h

The frame threshold value at which the timer snapshot will be taken is written here.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ASRC_FTC: [BAR + 0A2000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:16	15:0
Default	0000 0000 0000 0000	0000 0000 0000 0000
Field	RSVD0	ASRC_FTC

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RW	**ASRC Frame Threshold (ASRC_FTC):** The 16 bit frame threshold value needs to be written here. Every time the frame count matches the frame threshold a snapshot of the free running timer will be taken and stored in the snapshot register. An interrupt will be generated as well. If the frame threshold is changed on the fly during operation then the following behavior is expected. Previous value = A, New value value = B If B) A : The frame counter keeps counting up to the new value. Nothing happens when the frame counter reaches the old value of A. If B (A : The frame counter resets to zero on the next frame. No interrupt or snapshot is generated in this case.

21.14.22 ASRC Timer Snapshot (ASRC_SNPSHT)—Offset 84h

Frame Snapshot Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ASRC_SNPSHT: [BAR + 0A2000h] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ASRC_TIMER_SNAPSHOT

Bit Range	Default & Access	Description
31:0	00000000h RO	**ASRC Frame Snapshot (ASRC_TIMER_SNAPSHOT):** This field holds the 32 bit snapshot value. The value is noted on the clock cycle when the frame threshold matches the frame count.

21.14.23 ASRC Frame Count (ASRC_FRMCNT)—Offset 88h

Frame Count Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ASRC_FRMCNT: [BAR + 0A2000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
RSVD0	ASRC_FRM_COUNT

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0000h RO	**ASRC Frame Count (ASRC_FRM_COUNT):** This is the current frame count. This is a debug register and the value is noted in this register only when the LSB of the frame counter flips. If the counter is cleared when it was at an even value, the cleared value is not reflected here.

21.15 Low Power Audio DMA0 Memory Mapped IO Registers

Table 237. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_SAR_type (SAR0)—Offset 0h" on page 2939	00000000h
8h	4	"reg_DAR_type (DAR0)—Offset 8h" on page 2940	00000000h
10h	4	"reg_LLP_type (LLP0)—Offset 10h" on page 2941	00000000h
18h	4	"reg_CTL_LO_type (CTL_LO0)—Offset 18h" on page 2942	00000000h
1Ch	4	"reg_CTL_HI_type (CTL_HI0)—Offset 1Ch" on page 2943	00000000h
20h	4	"reg_SSTAT_type (SSTAT0)—Offset 20h" on page 2944	00000000h
28h	4	"reg_DSTAT_type (DSTAT0)—Offset 28h" on page 2945	00000000h
30h	4	"reg_SSTATAR_type (SSTATAR0)—Offset 30h" on page 2945	00000000h
38h	4	"reg_DSTATAR_type (DSTATAR0)—Offset 38h" on page 2946	00000000h
40h	4	"reg_CFG_LO_type (CFG_LO0)—Offset 40h" on page 2946	00000203h
44h	4	"reg_CFG_HI_type (CFG_HI0)—Offset 44h" on page 2948	00000000h
48h	4	"reg_SGR_type (SGR0)—Offset 48h" on page 2949	00000000h
50h	4	"reg_DSR_type (DSR0)—Offset 50h" on page 2950	00000000h
58h	4	"reg_SAR_type (SAR1)—Offset 58h" on page 2950	00000000h
60h	4	"reg_DAR_type (DAR1)—Offset 60h" on page 2951	00000000h
68h	4	"reg_LLP_type (LLP1)—Offset 68h" on page 2952	00000000h
70h	4	"reg_CTL_LO_type (CTL_LO1)—Offset 70h" on page 2953	00000000h
74h	4	"reg_CTL_HI_type (CTL_HI1)—Offset 74h" on page 2954	00000000h
78h	4	"reg_SSTAT_type (SSTAT1)—Offset 78h" on page 2955	00000000h
80h	4	"reg_DSTAT_type (DSTAT1)—Offset 80h" on page 2956	00000000h
88h	4	"reg_SSTATAR_type (SSTATAR1)—Offset 88h" on page 2956	00000000h
90h	4	"reg_DSTATAR_type (DSTATAR1)—Offset 90h" on page 2957	00000000h
98h	4	"reg_CFG_LO_type (CFG_LO1)—Offset 98h" on page 2957	00000203h
9Ch	4	"reg_CFG_HI_type (CFG_HI1)—Offset 9Ch" on page 2959	00000000h
A0h	4	"reg_SGR_type (SGR1)—Offset A0h" on page 2960	00000000h
A8h	4	"reg_DSR_type (DSR1)—Offset A8h" on page 2961	00000000h
B0h	4	"reg_SAR_type (SAR2)—Offset B0h" on page 2961	00000000h
B8h	4	"reg_DAR_type (DAR2)—Offset B8h" on page 2962	00000000h
C0h	4	"reg_LLP_type (LLP2)—Offset C0h" on page 2963	00000000h
C8h	4	"reg_CTL_LO_type (CTL_LO2)—Offset C8h" on page 2964	00000000h
CCh	4	"reg_CTL_HI_type (CTL_HI2)—Offset CCh" on page 2965	00000000h
D0h	4	"reg_SSTAT_type (SSTAT2)—Offset D0h" on page 2966	00000000h
D8h	4	"reg_DSTAT_type (DSTAT2)—Offset D8h" on page 2967	00000000h
E0h	4	"reg_SSTATAR_type (SSTATAR2)—Offset E0h" on page 2967	00000000h
E8h	4	"reg_DSTATAR_type (DSTATAR2)—Offset E8h" on page 2968	00000000h

Table 237. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
F0h	4	"reg_CFG_LO_type (CFG_LO2)—Offset F0h" on page 2968	00000203h
F4h	4	"reg_CFG_HI_type (CFG_HI2)—Offset F4h" on page 2970	00000000h
F8h	4	"reg_SGR_type (SGR2)—Offset F8h" on page 2971	00000000h
100h	4	"reg_DSR_type (DSR2)—Offset 100h" on page 2972	00000000h
108h	4	"reg_SAR_type (SAR3)—Offset 108h" on page 2972	00000000h
110h	4	"reg_DAR_type (DAR3)—Offset 110h" on page 2973	00000000h
118h	4	"reg_LLP_type (LLP3)—Offset 118h" on page 2974	00000000h
120h	4	"reg_CTL_LO_type (CTL_LO3)—Offset 120h" on page 2975	00000000h
124h	4	"reg_CTL_HI_type (CTL_HI3)—Offset 124h" on page 2976	00000000h
128h	4	"reg_SSTAT_type (SSTAT3)—Offset 128h" on page 2977	00000000h
130h	4	"reg_DSTAT_type (DSTAT3)—Offset 130h" on page 2978	00000000h
138h	4	"reg_SSTATAR_type (SSTATAR3)—Offset 138h" on page 2978	00000000h
140h	4	"reg_DSTATAR_type (DSTATAR3)—Offset 140h" on page 2979	00000000h
148h	4	"reg_CFG_LO_type (CFG_LO3)—Offset 148h" on page 2979	00000203h
14Ch	4	"reg_CFG_HI_type (CFG_HI3)—Offset 14Ch" on page 2981	00000000h
150h	4	"reg_SGR_type (SGR3)—Offset 150h" on page 2982	00000000h
158h	4	"reg_DSR_type (DSR3)—Offset 158h" on page 2983	00000000h
160h	4	"reg_SAR_type (SAR4)—Offset 160h" on page 2983	00000000h
168h	4	"reg_DAR_type (DAR4)—Offset 168h" on page 2984	00000000h
170h	4	"reg_LLP_type (LLP4)—Offset 170h" on page 2985	00000000h
178h	4	"reg_CTL_LO_type (CTL_LO4)—Offset 178h" on page 2986	00000000h
17Ch	4	"reg_CTL_HI_type (CTL_HI4)—Offset 17Ch" on page 2987	00000000h
180h	4	"reg_SSTAT_type (SSTAT4)—Offset 180h" on page 2988	00000000h
188h	4	"reg_DSTAT_type (DSTAT4)—Offset 188h" on page 2989	00000000h
190h	4	"reg_SSTATAR_type (SSTATAR4)—Offset 190h" on page 2989	00000000h
198h	4	"reg_DSTATAR_type (DSTATAR4)—Offset 198h" on page 2990	00000000h
1A0h	4	"reg_CFG_LO_type (CFG_LO4)—Offset 1A0h" on page 2990	00000203h
1A4h	4	"reg_CFG_HI_type (CFG_HI4)—Offset 1A4h" on page 2992	00000000h
1A8h	4	"reg_SGR_type (SGR4)—Offset 1A8h" on page 2993	00000000h
1B0h	4	"reg_DSR_type (DSR4)—Offset 1B0h" on page 2994	00000000h
1B8h	4	"reg_SAR_type (SAR5)—Offset 1B8h" on page 2994	00000000h
1C0h	4	"reg_DAR_type (DAR5)—Offset 1C0h" on page 2995	00000000h
1C8h	4	"reg_LLP_type (LLP5)—Offset 1C8h" on page 2996	00000000h
1D0h	4	"reg_CTL_LO_type (CTL_LO5)—Offset 1D0h" on page 2997	00000000h
1D4h	4	"reg_CTL_HI_type (CTL_HI5)—Offset 1D4h" on page 2998	00000000h
1D8h	4	"reg_SSTAT_type (SSTAT5)—Offset 1D8h" on page 2999	00000000h
1E0h	4	"reg_DSTAT_type (DSTAT5)—Offset 1E0h" on page 3000	00000000h
1E8h	4	"reg_SSTATAR_type (SSTATAR5)—Offset 1E8h" on page 3000	00000000h

Table 237. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
1F0h	4	"reg_DSTATAR_type (DSTATAR5)—Offset 1F0h" on page 3001	00000000h
1F8h	4	"reg_CFG_LO_type (CFG_LO5)—Offset 1F8h" on page 3001	00000203h
1FCh	4	"reg_CFG_HI_type (CFG_HI5)—Offset 1FCh" on page 3003	00000000h
200h	4	"reg_SGR_type (SGR5)—Offset 200h" on page 3004	00000000h
208h	4	"reg_DSR_type (DSR5)—Offset 208h" on page 3005	00000000h
210h	4	"reg_SAR_type (SAR6)—Offset 210h" on page 3005	00000000h
218h	4	"reg_DAR_type (DAR6)—Offset 218h" on page 3006	00000000h
220h	4	"reg_LLP_type (LLP6)—Offset 220h" on page 3007	00000000h
228h	4	"reg_CTL_LO_type (CTL_LO6)—Offset 228h" on page 3008	00000000h
22Ch	4	"reg_CTL_HI_type (CTL_HI6)—Offset 22Ch" on page 3009	00000000h
230h	4	"reg_SSTAT_type (SSTAT6)—Offset 230h" on page 3010	00000000h
238h	4	"reg_DSTAT_type (DSTAT6)—Offset 238h" on page 3011	00000000h
240h	4	"reg_SSTATAR_type (SSTATAR6)—Offset 240h" on page 3011	00000000h
248h	4	"reg_DSTATAR_type (DSTATAR6)—Offset 248h" on page 3012	00000000h
250h	4	"reg_CFG_LO_type (CFG_LO6)—Offset 250h" on page 3012	00000203h
254h	4	"reg_CFG_HI_type (CFG_HI6)—Offset 254h" on page 3014	00000000h
258h	4	"reg_SGR_type (SGR6)—Offset 258h" on page 3015	00000000h
260h	4	"reg_DSR_type (DSR6)—Offset 260h" on page 3016	00000000h
268h	4	"reg_SAR_type (SAR7)—Offset 268h" on page 3016	00000000h
270h	4	"reg_DAR_type (DAR7)—Offset 270h" on page 3017	00000000h
278h	4	"reg_LLP_type (LLP7)—Offset 278h" on page 3018	00000000h
280h	4	"reg_CTL_LO_type (CTL_LO7)—Offset 280h" on page 3019	00000000h
284h	4	"reg_CTL_HI_type (CTL_HI7)—Offset 284h" on page 3020	00000000h
288h	4	"reg_SSTAT_type (SSTAT7)—Offset 288h" on page 3021	00000000h
290h	4	"reg_DSTAT_type (DSTAT7)—Offset 290h" on page 3022	00000000h
298h	4	"reg_SSTATAR_type (SSTATAR7)—Offset 298h" on page 3022	00000000h
2A0h	4	"reg_DSTATAR_type (DSTATAR7)—Offset 2A0h" on page 3023	00000000h
2A8h	4	"reg_CFG_LO_type (CFG_LO7)—Offset 2A8h" on page 3023	00000203h
2ACh	4	"reg_CFG_HI_type (CFG_HI7)—Offset 2ACh" on page 3025	00000000h
2B0h	4	"reg_SGR_type (SGR7)—Offset 2B0h" on page 3026	00000000h
2B8h	4	"reg_DSR_type (DSR7)—Offset 2B8h" on page 3027	00000000h
2C0h	4	"reg_Raw_type (RawTfr)—Offset 2C0h" on page 3027	00000000h
2C8h	4	"reg_Raw_type (RawBlock)—Offset 2C8h" on page 3028	00000000h
2D0h	4	"reg_Raw_type (RawSrcTran)—Offset 2D0h" on page 3029	00000000h
2D8h	4	"reg_Raw_type (RawDstTran)—Offset 2D8h" on page 3029	00000000h
2E0h	4	"reg_Raw_type (RawErr)—Offset 2E0h" on page 3030	00000000h
2E8h	4	"reg_Status_type (StatusTfr)—Offset 2E8h" on page 3030	00000000h
2F0h	4	"reg_Status_type (StatusBlock)—Offset 2F0h" on page 3031	00000000h

Table 237. Summary of Low Power Audio DMA0 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
2F8h	4	"reg_Status_type (StatusSrcTran)—Offset 2F8h" on page 3032	00000000h
300h	4	"reg_Status_type (StatusDstTran)—Offset 300h" on page 3032	00000000h
308h	4	"reg_Status_type (StatusErr)—Offset 308h" on page 3033	00000000h
310h	4	"reg_Mask_type (MaskTfr)—Offset 310h" on page 3033	00000000h
318h	4	"reg_Mask_type (MaskBlock)—Offset 318h" on page 3034	00000000h
320h	4	"reg_Mask_type (MaskSrcTran)—Offset 320h" on page 3035	00000000h
328h	4	"reg_Mask_type (MaskDstTran)—Offset 328h" on page 3036	00000000h
330h	4	"reg_Mask_type (MaskErr)—Offset 330h" on page 3037	00000000h
338h	4	"reg_Clear_type (ClearTfr)—Offset 338h" on page 3037	00000000h
340h	4	"reg_Clear_type (ClearBlock)—Offset 340h" on page 3038	00000000h
348h	4	"reg_Clear_type (ClearSrcTran)—Offset 348h" on page 3039	00000000h
350h	4	"reg_Clear_type (ClearDstTran)—Offset 350h" on page 3039	00000000h
358h	4	"reg_Clear_type (ClearErr)—Offset 358h" on page 3040	00000000h
360h	4	"reg_StatusInt_type (StatusInt)—Offset 360h" on page 3040	00000000h
398h	4	"reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h" on page 3041	00000000h
3A0h	4	"reg_ChEnReg_type (ChEnReg)—Offset 3A0h" on page 3041	00000000h
3B8h	4	"reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h" on page 3042	00000000h
3BCh	4	"reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh" on page 3043	00000000h
3C0h	4	"reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h" on page 3043	00000000h
3C4h	4	"reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h" on page 3044	00000000h
400h	4	"reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h" on page 3044	00000000h
404h	4	"reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h" on page 3045	00000000h
408h	4	"reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h" on page 3046	00000000h
40Ch	4	"reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch" on page 3046	00000000h
410h	4	"reg_SAI_Error_type (SAI_ERR)—Offset 410h" on page 3047	00000000h
418h	4	"reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h" on page 3047	00000000h

21.15.1 reg_SAR_type (SAR0)—Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR0: [BAR + 98000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.2 reg_DAR_type (DAR0)—Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR0: [BAR + 98000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.3 reg_LLP_type (LLP0)—Offset 10h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP0: [BAR + 98000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.15.4 reg_CTL_LO_type (CTL_LO0)—Offset 18h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO0: [BAR + 98000h] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:29	28	27	26:22	21:20	19	18	17	16:14	13:11	10	9	8	7	6:4	3:1	0
Default	000	0	0	00000	00	0	0	0	000	000	0	0	0	0	000	000	0
Field	RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.15.5 reg_CTL_HI_type (CTL_HI0)—Offset 1Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI0: [BAR + 98000h] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

CH_CLASS | CH_WEIGHT | DONE | BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.15.6 reg_SSTAT_type (SSTAT0)—Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTAT0: [BAR + 98000h] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.15.7 reg_DSTAT_type (DSTAT0)—Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT0: [BAR + 98000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTAT																															

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.15.8 reg_SSTATAR_type (SSTATAR0)—Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR0: [BAR + 98000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.15.9 reg_DSTATAR_type (DSTATAR0)—Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR0: [BAR + 98000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.15.10 reg_CFG_LO_type (CFG_LO0)—Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO0: [BAR + 98000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bit	Default	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:22	0 0 0 0 0 0 0 0	Reserved_29_22
21	0	SRC_OPT_BL
20	0	DST_OPT_BL
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	WR_CTLHI_SNP
16	0	WR_STAT_SNP
15	0	RD_STAT_SNP
14	0	RD_LLP_SNP
13	0	WR_SNP
12	0	RD_SNP
11	0	Reserved_11
10	0	CH_DRAIN
9	1	FIFO_EMPTY
8	0	CH_SUSP
7	0	SS_UPD_EN
6	0	DS_UPD_EN
5	0	CTL_HI_UPD_EN
4	0	RSVD_4_4
3	0	HSHAKE_NP_WR
2	0	ALL_NP_WR
1	1	SRC_BURST_ALIGN
0	1	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.15.11 reg_CFG_HI_type (CFG_HI0)—Offset 44h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI0: [BAR + 98000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.15.12 reg_SGR_type (SGR0)—Offset 48h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SGR0: [BAR + 98000h] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.15.13 reg_DSR_type (DSR0)—Offset 50h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR0: [BAR + 98000h] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.15.14 reg_SAR_type (SAR1)—Offset 58h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR1: [BAR + 98000h] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.15 reg_DAR_type (DAR1)—Offset 60h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR1: [BAR + 98000h] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.16 reg_LLP_type (LLP1)—Offset 68h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP1: [BAR + 98000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC (bits 31:2), RSVD2 (bits 1:0)

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.15.17 reg_CTL_LO_type (CTL_LO1)—Offset 70h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO1: [BAR + 98000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.15.18 reg_CTL_HI_type (CTL_HI1)—Offset 74h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI1: [BAR + 98000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CH_CLASS | CH_WEIGHT | DONE | BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.15.19 reg_SSTAT_type (SSTAT1)—Offset 78h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTAT1: [BAR + 98000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.15.20 reg_DSTAT_type (DSTAT1)—Offset 80h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT1: [BAR + 98000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTAT																															

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.15.21 reg_SSTATAR_type (SSTATAR1)—Offset 88h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR1: [BAR + 98000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.15.22 reg_DSTATAR_type (DSTATAR1)—Offset 90h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR1: [BAR + 98000h] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.15.23 reg_CFG_LO_type (CFG_LO1)—Offset 98h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO1: [BAR + 98000h] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1

Bit	Field
31	RELOAD_DST
30	RELOAD_SRC
29:22	Reserved_29_22
21	SRC_OPT_BL
20	DST_OPT_BL
19	SRC_HS_POL
18	DST_HS_POL
17	WR_CTLHI_SNP
16	WR_STAT_SNP
15	RD_STAT_SNP
14	RD_LLP_SNP
13	WR_SNP
12	RD_SNP
11	Reserved_11
10	CH_DRAIN
9	FIFO_EMPTY
8	CH_SUSP
7	SS_UPD_EN
6	DS_UPD_EN
5	CTL_HI_UPD_EN
4	RSVD_4_4
3	HSHAKE_NP_WR
2	ALL_NP_WR
1	SRC_BURST_ALIGN
0	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.15.24 reg_CFG_HI_type (CFG_HI1)—Offset 9Ch

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI1: [BAR + 98000h] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DST_PER_EXT		SRC_PER_EXT		WR_ISSUE_THD										RD_ISSUE_THD										DST_PER				SRC_PER			

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.15.25 reg_SGR_type (SGR1)—Offset A0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR1: [BAR + 98000h] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.15.26 reg_DSR_type (DSR1)—Offset A8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR1: [BAR + 98000h] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.15.27 reg_SAR_type (SAR2)—Offset B0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR2: [BAR + 98000h] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.28 reg_DAR_type (DAR2)—Offset B8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR2: [BAR + 98000h] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.29 reg_LLP_type (LLP2)—Offset C0h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP2: [BAR + 98000h] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.15.30 reg_CTL_LO_type (CTL_LO2)—Offset C8h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO2: [BAR + 98000h] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD | LLP_SRC_EN | LLP_DST_EN | RSVD1 | TT_FC | RSVD2 | DST_SCATTER_EN | SRC_GATHER_EN | SRC_MSIZE | DEST_MSIZE | SINC | RSVD3 | DINC | RSVD4 | SRC_TR_WIDTH | DST_TR_WIDTH | INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.15.31 reg_CTL_HI_type (CTL_HI2)—Offset CCh

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI2: [BAR + 98000h] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

CH_CLASS | CH_WEIGHT | DONE | BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.15.32 reg_SSTAT_type (SSTAT2)—Offset D0h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT2: [BAR + 98000h] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.15.33 reg_DSTAT_type (DSTAT2)—Offset D8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT2: [BAR + 98000h] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.15.34 reg_SSTATAR_type (SSTATAR2)—Offset E0h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR2: [BAR + 98000h] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.15.35 reg_DSTATAR_type (DSTATAR2)—Offset E8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTATAR2: [BAR + 98000h] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.15.36 reg_CFG_LO_type (CFG_LO2)—Offset F0h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CFG_LO2: [BAR + 98000h] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
RELOAD_DST	RELOAD_SRC	Reserved_29_22								SRC_OPT_BL	DST_OPT_BL	SRC_HS_POL	DST_HS_POL	WR_CTLHI_SNP	WR_STAT_SNP	RD_STAT_SNP	RD_LLP_SNP	WR_SNP	RD_SNP	Reserved_11	CH_DRAIN	FIFO_EMPTY	CH_SUSP	SS_UPD_EN	DS_UPD_EN	CTL_HI_UPD_EN	RSVD_4_4	HSHAKE_NP_WR	ALL_NP_WR	SRC_BURST_ALIGN	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.15.37 reg_CFG_HI_type (CFG_HI2)—Offset F4h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CFG_HI2: [BAR + 98000h] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields (from bit 31 to bit 0): DST_PER_EXT, SRC_PER_EXT, WR_ISSUE_THD, RD_ISSUE_THD, DST_PER, SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.15.38 reg_SGR_type (SGR2)—Offset F8h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SGR2: [BAR + 98000h] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.15.39 reg_DSR_type (DSR2)—Offset 100h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR2: [BAR + 98000h] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.15.40 reg_SAR_type (SAR3)—Offset 108h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR3: [BAR + 98000h] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.41 reg_DAR_type (DAR3)—Offset 110h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DAR3: [BAR + 98000h] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.42 reg_LLP_type (LLP3)—Offset 118h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP3: [BAR + 98000h] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.15.43 reg_CTL_LO_type (CTL_LO3)—Offset 120h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO3: [BAR + 98000h] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			LLP_SRC_EN	LLP_DST_EN	RSVD1					TT_FC		RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE			DEST_MSIZE			SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH			DST_TR_WIDTH			INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.15.44 reg_CTL_HI_type (CTL_HI3)—Offset 124h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI3: [BAR + 98000h] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: CH_CLASS | CH_WEIGHT | DONE | BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.15.45 reg_SSTAT_type (SSTAT3)—Offset 128h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTAT3: [BAR + 98000h] + 128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.15.46 reg_DSTAT_type (DSTAT3)—Offset 130h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT3: [BAR + 98000h] + 130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.15.47 reg_SSTATAR_type (SSTATAR3)—Offset 138h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR3: [BAR + 98000h] + 138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.15.48 reg_DSTATAR_type (DSTATAR3)—Offset 140h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR3: [BAR + 98000h] + 140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.15.49 reg_CFG_LO_type (CFG_LO3)—Offset 148h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO3: [BAR + 98000h] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bit	Default	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:22	0 0 0 0 0 0 0 0	Reserved_29_22
21	0	SRC_OPT_BL
20	0	DST_OPT_BL
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	WR_CTLHI_SNP
16	0	WR_STAT_SNP
15	0	RD_STAT_SNP
14	0	RD_LLP_SNP
13	0	WR_SNP
12	0	RD_SNP
11	0	Reserved_11
10	0	CH_DRAIN
9	1	FIFO_EMPTY
8	0	CH_SUSP
7	0	SS_UPD_EN
6	0	DS_UPD_EN
5	0	CTL_HI_UPD_EN
4	0	RSVD_4_4
3	0	HSHAKE_NP_WR
2	0	ALL_NP_WR
1	1	SRC_BURST_ALIGN
0	1	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.15.50 reg_CFG_HI_type (CFG_HI3)—Offset 14Ch

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI3: [BAR + 98000h] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.15.51 reg_SGR_type (SGR3)—Offset 150h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR3: [BAR + 98000h] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:20	Bits 19:0
SGC	SGI

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.15.52 reg_DSR_type (DSR3)—Offset 158h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR3: [BAR + 98000h] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.15.53 reg_SAR_type (SAR4)—Offset 160h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR4: [BAR + 98000h] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.54 reg_DAR_type (DAR4)—Offset 168h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR4: [BAR + 98000h] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.55 reg_LLP_type (LLP4)—Offset 170h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP4: [BAR + 98000h] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.15.56 reg_CTL_LO_type (CTL_LO4)—Offset 178h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO4: [BAR + 98000h] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.15.57 reg_CTL_HI_type (CTL_HI4)—Offset 17Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI4: [BAR + 98000h] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CH_CLASS	CH_WEIGHT	DONE	BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.15.58 reg_SSTAT_type (SSTAT4)—Offset 180h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT4: [BAR + 98000h] + 180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.15.59 reg_DSTAT_type (DSTAT4)—Offset 188h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT4: [BAR + 98000h] + 188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.15.60 reg_SSTATAR_type (SSTATAR4)—Offset 190h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR4: [BAR + 98000h] + 190h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.15.61 reg_DSTATAR_type (DSTATAR4)—Offset 198h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTATAR4: [BAR + 98000h] + 198h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.15.62 reg_CFG_LO_type (CFG_LO4)—Offset 1A0h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CFG_LO4: [BAR + 98000h] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bit	Default	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:22	0 0 0 0 0 0 0 0	Reserved_29_22
21	0	SRC_OPT_BL
20	0	DST_OPT_BL
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	WR_CTLHI_SNP
16	0	WR_STAT_SNP
15	0	RD_STAT_SNP
14	0	RD_LLP_SNP
13	0	WR_SNP
12	0	RD_SNP
11	0	Reserved_11
10	0	CH_DRAIN
9	1	FIFO_EMPTY
8	0	CH_SUSP
7	0	SS_UPD_EN
6	0	DS_UPD_EN
5	0	CTL_HI_UPD_EN
4	0	RSVD_4_4
3	0	HSHAKE_NP_WR
2	0	ALL_NP_WR
1	1	SRC_BURST_ALIGN
0	1	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.15.63 reg_CFG_HI_type (CFG_HI4)—Offset 1A4h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CFG_HI4: [BAR + 98000h] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:30	29:28	27:18	17:8	7:4	3:0
Default	0 0	0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0
Field	DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.15.64 reg_SGR_type (SGR4)—Offset 1A8h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SGR4: [BAR + 98000h] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.15.65 reg_DSR_type (DSR4)—Offset 1B0h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR4: [BAR + 98000h] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.15.66 reg_SAR_type (SAR5)—Offset 1B8h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR5: [BAR + 98000h] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.67 reg_DAR_type (DAR5)—Offset 1C0h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR5: [BAR + 98000h] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.68 reg_LLP_type (LLP5)—Offset 1C8h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP5: [BAR + 98000h] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.15.69 reg_CTL_LO_type (CTL_LO5)—Offset 1D0h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO5: [BAR + 98000h] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:29	28	27	26:22	21:20	19	18	17	16:14	13:11	10	9	8	7	6:4	3:1	0
Default	000	0	0	00000	00	0	0	0	000	000	0	0	0	0	000	000	0
Field	RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.15.70 reg_CTL_HI_type (CTL_HI5)—Offset 1D4h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI5: [BAR + 98000h] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:29	Bits 28:18	Bit 17	Bits 16:0
CH_CLASS	CH_WEIGHT	DONE	BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.15.71 reg_SSTAT_type (SSTAT5)—Offset 1D8h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT5: [BAR + 98000h] + 1D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.15.72 reg_DSTAT_type (DSTAT5)—Offset 1E0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT5: [BAR + 98000h] + 1E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.15.73 reg_SSTATAR_type (SSTATAR5)—Offset 1E8h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR5: [BAR + 98000h] + 1E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.15.74 reg_DSTATAR_type (DSTATAR5)—Offset 1F0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR5: [BAR + 98000h] + 1F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.15.75 reg_CFG_LO_type (CFG_LO5)—Offset 1F8h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO5: [BAR + 98000h] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bit	31	30	29:22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
Field	RELOAD_DST	RELOAD_SRC	Reserved_29_22	SRC_OPT_BL	DST_OPT_BL	SRC_HS_POL	DST_HS_POL	WR_CTLHI_SNP	WR_STAT_SNP	RD_STAT_SNP	RD_LLP_SNP	WR_SNP	RD_SNP	Reserved_11	CH_DRAIN	FIFO_EMPTY	CH_SUSP	SS_UPD_EN	DS_UPD_EN	CTL_HI_UPD_EN	RSVD_4_4	HSHAKE_NP_WR	ALL_NP_WR	SRC_BURST_ALIGN	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.15.76 reg_CFG_HI_type (CFG_HI5)—Offset 1FCh

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI5: [BAR + 98000h] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DST_PER_EXT		SRC_PER_EXT		WR_ISSUE_THD										RD_ISSUE_THD										DST_PER				SRC_PER			

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.15.77 reg_SGR_type (SGR5)—Offset 200h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR5: [BAR + 98000h] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:20	Bits 19:0
SGC	SGI

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.15.78 reg_DSR_type (DSR5)—Offset 208h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR5: [BAR + 98000h] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
DSC			DSI				

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.15.79 reg_SAR_type (SAR6)—Offset 210h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR6: [BAR + 98000h] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.80 reg_DAR_type (DAR6)—Offset 218h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR6: [BAR + 98000h] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.81 reg_LLP_type (LLP6)—Offset 220h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP6: [BAR + 98000h] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.15.82 reg_CTL_LO_type (CTL_LO6)—Offset 228h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO6: [BAR + 98000h] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.15.83 reg_CTL_HI_type (CTL_HI6)—Offset 22Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI6: [BAR + 98000h] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CH_CLASS	CH_WEIGHT	DONE	BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.15.84 reg_SSTAT_type (SSTAT6)—Offset 230h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTAT6: [BAR + 98000h] + 230h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.15.85 reg_DSTAT_type (DSTAT6)—Offset 238h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT6: [BAR + 98000h] + 238h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTAT																															

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.15.86 reg_SSTATAR_type (SSTATAR6)—Offset 240h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR6: [BAR + 98000h] + 240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.15.87 reg_DSTATAR_type (DSTATAR6)—Offset 248h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR6: [BAR + 98000h] + 248h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.15.88 reg_CFG_LO_type (CFG_LO6)—Offset 250h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO6: [BAR + 98000h] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	RELOAD_DST	RELOAD_SRC	Reserved_29_22								SRC_OPT_BL	DST_OPT_BL	SRC_HS_POL	DST_HS_POL	WR_CTLHI_SNP	WR_STAT_SNP

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
Field	RD_STAT_SNP	RD_LLP_SNP	WR_SNP	RD_SNP	Reserved_11	CH_DRAIN	FIFO_EMPTY	CH_SUSP	SS_UPD_EN	DS_UPD_EN	CTL_HI_UPD_EN	RSVD_4_4	HSHAKE_NP_WR	ALL_NP_WR	SRC_BURST_ALIGN	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.15.89 reg_CFG_HI_type (CFG_HI6)—Offset 254h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI6: [BAR + 98000h] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DST_PER_EXT		SRC_PER_EXT		WR_ISSUE_THD										RD_ISSUE_THD										DST_PER				SRC_PER			

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.15.90 reg_SGR_type (SGR6)—Offset 258h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR6: [BAR + 98000h] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.15.91 reg_DSR_type (DSR6)—Offset 260h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR6: [BAR + 98000h] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.15.92 reg_SAR_type (SAR7)—Offset 268h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR7: [BAR + 98000h] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.93 reg_DAR_type (DAR7)—Offset 270h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR7: [BAR + 98000h] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.15.94 reg_LLP_type (LLP7)—Offset 278h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP7: [BAR + 98000h] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

LOC | RSVD2

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.15.95 reg_CTL_LO_type (CTL_LO7)—Offset 280h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO7: [BAR + 98000h] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			LLP_SRC_EN	LLP_DST_EN	RSVD1					TT_FC		RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE			DEST_MSIZE			SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH			DST_TR_WIDTH			INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.15.96 reg_CTL_HI_type (CTL_HI7)—Offset 284h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI7: [BAR + 98000h] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

CH_CLASS
CH_WEIGHT
DONE
BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.15.97 reg_SSTAT_type (SSTAT7)—Offset 288h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTAT7: [BAR + 98000h] + 288h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.15.98 reg_DSTAT_type (DSTAT7)—Offset 290h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT7: [BAR + 98000h] + 290h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.15.99 reg_SSTATAR_type (SSTATAR7)—Offset 298h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR7: [BAR + 98000h] + 298h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.15.100 reg_DSTATAR_type (DSTATAR7)—Offset 2A0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR7: [BAR + 98000h] + 2A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.15.101 reg_CFG_LO_type (CFG_LO7)—Offset 2A8h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO7: [BAR + 98000h] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bit	Default	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:22	0 0 0 0 0 0 0 0	Reserved_29_22
21	0	SRC_OPT_BL
20	0	DST_OPT_BL
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	WR_CTLHI_SNP
16	0	WR_STAT_SNP
15	0	RD_STAT_SNP
14	0	RD_LLP_SNP
13	0	WR_SNP
12	0	RD_SNP
11	0	Reserved_11
10	0	CH_DRAIN
9	1	FIFO_EMPTY
8	0	CH_SUSP
7	0	SS_UPD_EN
6	0	DS_UPD_EN
5	0	CTL_HI_UPD_EN
4	0	RSVD_4_4
3	0	HSHAKE_NP_WR
2	0	ALL_NP_WR
1	1	SRC_BURST_ALIGN
0	1	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.15.102 reg_CFG_HI_type (CFG_HI7)—Offset 2ACh

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI7: [BAR + 98000h] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DST_PER_EXT		SRC_PER_EXT		WR_ISSUE_THD										RD_ISSUE_THD										DST_PER				SRC_PER			

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.15.103 reg_SGR_type (SGR7)—Offset 2B0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR7: [BAR + 98000h] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.15.104 reg_DSR_type (DSR7)—Offset 2B8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR7: [BAR + 98000h] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.15.105 reg_Raw_type (RawTfr)—Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawTfr: [BAR + 98000h] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RAW							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.15.106 reg_Raw_type (RawBlock)—Offset 2C8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawBlock: [BAR + 98000h] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RAW							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.15.107 reg_Raw_type (RawSrcTran)—Offset 2D0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawSrcTran: [BAR + 98000h] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RAW							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.15.108 reg_Raw_type (RawDstTran)—Offset 2D8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawDstTran: [BAR + 98000h] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RAW							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.15.109 reg_Raw_type (RawErr)—Offset 2E0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawErr: [BAR + 98000h] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RAW							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.15.110 reg_Status_type (StatusTfr)—Offset 2E8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusTfr: [BAR + 98000h] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (bits 31:8), STATUS (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.15.111 reg_Status_type (StatusBlock)—Offset 2F0h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusBlock: [BAR + 98000h] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (bits 31:8), STATUS (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.15.112 reg_Status_type (StatusSrcTran)—Offset 2F8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

StatusSrcTran: [BAR + 98000h] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								STATUS							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.15.113 reg_Status_type (StatusDstTran)—Offset 300h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

StatusDstTran: [BAR + 98000h] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								STATUS							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.15.114 reg_Status_type (StatusErr)—Offset 308h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

StatusErr: [BAR + 98000h] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								STATUS							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.15.115 reg_Mask_type (MaskTfr)—Offset 310h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**MaskTfr:** [BAR + 98000h] + 310h
	BAR Type: PCI Configuration Register (Size: 32 bits) **BAR Reference:** [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:8	Bits 7:0
RSVD2	INT_MASK_WE	INT_MASK

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.15.116 reg_Mask_type (MaskBlock)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**MaskBlock:** [BAR + 98000h] + 318h
	BAR Type: PCI Configuration Register (Size: 32 bits) **BAR Reference:** [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD2																INT_MASK_WE								INT_MASK							

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.15.117 reg_Mask_type (MaskSrcTran)—Offset 320h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskSrcTran: [BAR + 98000h] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD2																INT_MASK_WE								INT_MASK							

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.15.118 reg_Mask_type (MaskDstTran)—Offset 328h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskDstTran: [BAR + 98000h] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:16	15:8	7:0
Default	0000 0000 0000 0000	0000 0000	0000 0000
Field	RSVD2	INT_MASK_WE	INT_MASK

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.15.119 reg_Mask_type (MaskErr)—Offset 330h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

MaskErr: [BAR + 98000h] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31:16	15:8	7:0
0000 0000 0000 0000	0000 0000	0000 0000
RSVD2	INT_MASK_WE	INT_MASK

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.15.120 reg_Clear_type (ClearTfr)—Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClearTfr: [BAR + 98000h] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (bits 31:8) | CLEAR (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.15.121 reg_Clear_type (ClearBlock)—Offset 340h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClearBlock: [BAR + 98000h] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (bits 31:8) | CLEAR (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.15.122 reg_Clear_type (ClearSrcTran)—Offset 348h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearSrcTran: [BAR + 98000h] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
RSVD (31:8)						CLEAR (7:0)		

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.15.123 reg_Clear_type (ClearDstTran)—Offset 350h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearDstTran: [BAR + 98000h] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
RSVD (31:8)						CLEAR (7:0)		

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.15.124 reg_Clear_type (ClearErr)—Offset 358h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClearErr: [BAR + 98000h] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (bits 31:8), CLEAR (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.15.125 reg_StatusInt_type (StatusInt)—Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

StatusInt: [BAR + 98000h] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (bits 31:5), ERR (bit 4), DSTT (bit 3), SRCT (bit 2), BLOCK (bit 1), TFR (bit 0)

Bit Range	Default & Access	Description
31:5	0h RO	**RSVD:** Reserved
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

21.15.126 reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DmaCfgReg: [BAR + 98000h] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD | DMA_EN

Bit Range	Default & Access	Description
31:1	0h RO	**RSVD:** Reserved
0	0h RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

21.15.127 reg_ChEnReg_type (ChEnReg)—Offset 3A0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ChEnReg: [BAR + 98000h] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD2																CH_EN_WE								CH_EN							

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**CH_EN_WE:** Channel enable write enable.
7:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

21.15.128 reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority0_LO: [BAR + 98000h] + 3B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD2										WT_CLASS_1											WT_CLASS_0										

Bit Range	Default & Access	Description
31:22	0h RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
21:11	0h RW	**WT_CLASS_1:** Class Weight 1: Value of K assigns a weight of (K+1) to Class 1. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_0:** Class Weight 0: Value of K assigns a weight of (K+1) to Class 0. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

21.15.129 reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClassPriority0_HI: [BAR + 98000h] + 3BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:23	22	21:11	10:0
Value	0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0
Field	RSVD1	STRICT_PRI	WT_CLASS_3	WT_CLASS_2

Bit Range	Default & Access	Description
31:23	0h RO	**RSVD1:** Reserved
22	0h RW	**STRICT_PRI:** If set, Higher class values will always have higher priorities than lower class values. If not set, round-robin arbitration will be used between different classes using WT_CLASS_n values.
21:11	0h RW	**WT_CLASS_3:** Class Weight 3: Value of K assigns a weight of (K+1) to Class 3. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_2:** Class Weight 2: Value of K assigns a weight of (K+1) to Class 2. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

21.15.130 reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClassPriority1_LO: [BAR + 98000h] + 3C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

RSVD2	WT_CLASS_5	WT_CLASS_4

Bit Range	Default & Access	Description
31:22	0h RO	**RSVD2:** Reserved
21:11	0h RW	**WT_CLASS_5:** Class Weight 5: Value of K assigns a weight of (K+1) to Class 5. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_4:** Class Weight 4: Value of K assigns a weight of (K+1) to Class 4. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

21.15.131 reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority1_HI: [BAR + 98000h] + 3C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

RSVD1	WT_CLASS_7	WT_CLASS_6

Bit Range	Default & Access	Description
31:22	0h RO	**RSVD1:** Reserved
21:11	0h RW	**WT_CLASS_7:** Class Weight 7: Value of K assigns a weight of (K+1) to Class 7. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_6:** Class Weight 6: Value of K assigns a weight of (K+1) to Class 6. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

21.15.132 reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

FifoPartition0_LO: [BAR + 98000h] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD2 (31:27), PARTITION_UPDATE (26), PSIZE_CH_1 (25:13), PSIZE_CH_0 (12:0)

Bit Range	Default & Access	Description
31:27	0h RO	**RSVD2:** Reserved
26	0h RW	**PARTITION_UPDATE:** SW needs to write to this bit for the partitioning assignments to take effect.
25:13	0h RW	**PSIZE_CH_1:** Partition Byte Size assigned to Channel 1. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_0:** Partition Byte Size assigned to Channel 0. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

21.15.133 reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

FifoPartition0_HI: [BAR + 98000h] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD1 (31:26), PSIZE_CH_3 (25:13), PSIZE_CH_2 (12:0)

Bit Range	Default & Access	Description
31:26	0h RO	**RSVD1:** Reserved
25:13	0h RW	**PSIZE_CH_3:** Partition Byte Size assigned to Channel 3. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

Bit Range	Default & Access	Description
12:0	0h RW	**PSIZE_CH_2:** Partition Byte Size assigned to Channel 2. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

21.15.134 reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

FifoPartition1_LO: [BAR + 98000h] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD2 | PSIZE_CH_5 | PSIZE_CH_4

Bit Range	Default & Access	Description
31:26	0h RO	**RSVD2:** Reserved
25:13	0h RW	**PSIZE_CH_5:** Partition Byte Size assigned to Channel 5. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_4:** Partition Byte Size assigned to Channel 4. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

21.15.135 reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

FifoPartition1_HI: [BAR + 98000h] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD1 | PSIZE_CH_7 | PSIZE_CH_6

Bit Range	Default & Access	Description
31:26	0h RO	**RSVD1:** Reserved
25:13	0h RW	**PSIZE_CH_7:** Partition Byte Size assigned to Channel 7. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_6:** Partition Byte Size assigned to Channel 6. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

21.15.136 reg_SAI_Error_type (SAI_ERR)—Offset 410h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAI_ERR: [BAR + 98000h] + 410h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

RSVD CH_SAI_ERR

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**CH_SAI_ERR:** 1: SAI Error occurred on Ch [n] 0: No SAI Error occurred on Ch [n] SAI_ERROR[n] is set by HW on SAI violation for channel [n]. All bits get cleared by SW when reading this register

21.15.137 reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h

GLOBAL_CFG: GLOBAL DMA Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GLOBAL_CFG: [BAR + 98000h] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

SCRATCH_PAD ERR_ILL_REG

Bit Range	Default & Access	Description
31:1	0h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future configuration and de-feature bits.
0	0b RW	**ERR_ILL_REG:** 0x1 : Issue ERR response on reading illegal (non-existing) registers 0x0 : Issue DVA response on reading illegal (non-existing) registers

21.16 Low Power Audio DMA1 Memory Mapped IO Registers

Table 238. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size	Register ID—Description	Default Value
0h	4	"reg_SAR_type (SAR0)—Offset 0h" on page 3052	00000000h
8h	4	"reg_DAR_type (DAR0)—Offset 8h" on page 3053	00000000h
10h	4	"reg_LLP_type (LLP0)—Offset 10h" on page 3054	00000000h
18h	4	"reg_CTL_LO_type (CTL_LO0)—Offset 18h" on page 3055	00000000h
1Ch	4	"reg_CTL_HI_type (CTL_HI0)—Offset 1Ch" on page 3056	00000000h
20h	4	"reg_SSTAT_type (SSTAT0)—Offset 20h" on page 3057	00000000h
28h	4	"reg_DSTAT_type (DSTAT0)—Offset 28h" on page 3058	00000000h
30h	4	"reg_SSTATAR_type (SSTATAR0)—Offset 30h" on page 3058	00000000h
38h	4	"reg_DSTATAR_type (DSTATAR0)—Offset 38h" on page 3059	00000000h
40h	4	"reg_CFG_LO_type (CFG_LO0)—Offset 40h" on page 3059	00000203h
44h	4	"reg_CFG_HI_type (CFG_HI0)—Offset 44h" on page 3061	00000000h
48h	4	"reg_SGR_type (SGR0)—Offset 48h" on page 3062	00000000h
50h	4	"reg_DSR_type (DSR0)—Offset 50h" on page 3063	00000000h
58h	4	"reg_SAR_type (SAR1)—Offset 58h" on page 3063	00000000h
60h	4	"reg_DAR_type (DAR1)—Offset 60h" on page 3064	00000000h
68h	4	"reg_LLP_type (LLP1)—Offset 68h" on page 3065	00000000h
70h	4	"reg_CTL_LO_type (CTL_LO1)—Offset 70h" on page 3066	00000000h
74h	4	"reg_CTL_HI_type (CTL_HI1)—Offset 74h" on page 3067	00000000h
78h	4	"reg_SSTAT_type (SSTAT1)—Offset 78h" on page 3068	00000000h
80h	4	"reg_DSTAT_type (DSTAT1)—Offset 80h" on page 3069	00000000h
88h	4	"reg_SSTATAR_type (SSTATAR1)—Offset 88h" on page 3069	00000000h
90h	4	"reg_DSTATAR_type (DSTATAR1)—Offset 90h" on page 3070	00000000h
98h	4	"reg_CFG_LO_type (CFG_LO1)—Offset 98h" on page 3070	00000203h
9Ch	4	"reg_CFG_HI_type (CFG_HI1)—Offset 9Ch" on page 3072	00000000h
A0h	4	"reg_SGR_type (SGR1)—Offset A0h" on page 3073	00000000h
A8h	4	"reg_DSR_type (DSR1)—Offset A8h" on page 3074	00000000h
B0h	4	"reg_SAR_type (SAR2)—Offset B0h" on page 3074	00000000h
B8h	4	"reg_DAR_type (DAR2)—Offset B8h" on page 3075	00000000h
C0h	4	"reg_LLP_type (LLP2)—Offset C0h" on page 3076	00000000h
C8h	4	"reg_CTL_LO_type (CTL_LO2)—Offset C8h" on page 3077	00000000h
CCh	4	"reg_CTL_HI_type (CTL_HI2)—Offset CCh" on page 3078	00000000h
D0h	4	"reg_SSTAT_type (SSTAT2)—Offset D0h" on page 3079	00000000h
D8h	4	"reg_DSTAT_type (DSTAT2)—Offset D8h" on page 3080	00000000h
E0h	4	"reg_SSTATAR_type (SSTATAR2)—Offset E0h" on page 3080	00000000h
E8h	4	"reg_DSTATAR_type (DSTATAR2)—Offset E8h" on page 3081	00000000h

Table 238. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
F0h	4	"reg_CFG_LO_type (CFG_LO2)—Offset F0h" on page 3081	00000203h
F4h	4	"reg_CFG_HI_type (CFG_HI2)—Offset F4h" on page 3083	00000000h
F8h	4	"reg_SGR_type (SGR2)—Offset F8h" on page 3084	00000000h
100h	4	"reg_DSR_type (DSR2)—Offset 100h" on page 3085	00000000h
108h	4	"reg_SAR_type (SAR3)—Offset 108h" on page 3085	00000000h
110h	4	"reg_DAR_type (DAR3)—Offset 110h" on page 3086	00000000h
118h	4	"reg_LLP_type (LLP3)—Offset 118h" on page 3087	00000000h
120h	4	"reg_CTL_LO_type (CTL_LO3)—Offset 120h" on page 3088	00000000h
124h	4	"reg_CTL_HI_type (CTL_HI3)—Offset 124h" on page 3089	00000000h
128h	4	"reg_SSTAT_type (SSTAT3)—Offset 128h" on page 3090	00000000h
130h	4	"reg_DSTAT_type (DSTAT3)—Offset 130h" on page 3091	00000000h
138h	4	"reg_SSTATAR_type (SSTATAR3)—Offset 138h" on page 3091	00000000h
140h	4	"reg_DSTATAR_type (DSTATAR3)—Offset 140h" on page 3092	00000000h
148h	4	"reg_CFG_LO_type (CFG_LO3)—Offset 148h" on page 3092	00000203h
14Ch	4	"reg_CFG_HI_type (CFG_HI3)—Offset 14Ch" on page 3094	00000000h
150h	4	"reg_SGR_type (SGR3)—Offset 150h" on page 3095	00000000h
158h	4	"reg_DSR_type (DSR3)—Offset 158h" on page 3096	00000000h
160h	4	"reg_SAR_type (SAR4)—Offset 160h" on page 3096	00000000h
168h	4	"reg_DAR_type (DAR4)—Offset 168h" on page 3097	00000000h
170h	4	"reg_LLP_type (LLP4)—Offset 170h" on page 3098	00000000h
178h	4	"reg_CTL_LO_type (CTL_LO4)—Offset 178h" on page 3099	00000000h
17Ch	4	"reg_CTL_HI_type (CTL_HI4)—Offset 17Ch" on page 3100	00000000h
180h	4	"reg_SSTAT_type (SSTAT4)—Offset 180h" on page 3101	00000000h
188h	4	"reg_DSTAT_type (DSTAT4)—Offset 188h" on page 3102	00000000h
190h	4	"reg_SSTATAR_type (SSTATAR4)—Offset 190h" on page 3102	00000000h
198h	4	"reg_DSTATAR_type (DSTATAR4)—Offset 198h" on page 3103	00000000h
1A0h	4	"reg_CFG_LO_type (CFG_LO4)—Offset 1A0h" on page 3103	00000203h
1A4h	4	"reg_CFG_HI_type (CFG_HI4)—Offset 1A4h" on page 3105	00000000h
1A8h	4	"reg_SGR_type (SGR4)—Offset 1A8h" on page 3106	00000000h
1B0h	4	"reg_DSR_type (DSR4)—Offset 1B0h" on page 3107	00000000h
1B8h	4	"reg_SAR_type (SAR5)—Offset 1B8h" on page 3107	00000000h
1C0h	4	"reg_DAR_type (DAR5)—Offset 1C0h" on page 3108	00000000h
1C8h	4	"reg_LLP_type (LLP5)—Offset 1C8h" on page 3109	00000000h
1D0h	4	"reg_CTL_LO_type (CTL_LO5)—Offset 1D0h" on page 3110	00000000h
1D4h	4	"reg_CTL_HI_type (CTL_HI5)—Offset 1D4h" on page 3111	00000000h
1D8h	4	"reg_SSTAT_type (SSTAT5)—Offset 1D8h" on page 3112	00000000h
1E0h	4	"reg_DSTAT_type (DSTAT5)—Offset 1E0h" on page 3113	00000000h
1E8h	4	"reg_SSTATAR_type (SSTATAR5)—Offset 1E8h" on page 3113	00000000h

Table 238. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
1F0h	4	"reg_DSTATAR_type (DSTATAR5)—Offset 1F0h" on page 3114	00000000h
1F8h	4	"reg_CFG_LO_type (CFG_LO5)—Offset 1F8h" on page 3114	00000203h
1FCh	4	"reg_CFG_HI_type (CFG_HI5)—Offset 1FCh" on page 3116	00000000h
200h	4	"reg_SGR_type (SGR5)—Offset 200h" on page 3117	00000000h
208h	4	"reg_DSR_type (DSR5)—Offset 208h" on page 3118	00000000h
210h	4	"reg_SAR_type (SAR6)—Offset 210h" on page 3118	00000000h
218h	4	"reg_DAR_type (DAR6)—Offset 218h" on page 3119	00000000h
220h	4	"reg_LLP_type (LLP6)—Offset 220h" on page 3120	00000000h
228h	4	"reg_CTL_LO_type (CTL_LO6)—Offset 228h" on page 3121	00000000h
22Ch	4	"reg_CTL_HI_type (CTL_HI6)—Offset 22Ch" on page 3122	00000000h
230h	4	"reg_SSTAT_type (SSTAT6)—Offset 230h" on page 3123	00000000h
238h	4	"reg_DSTAT_type (DSTAT6)—Offset 238h" on page 3124	00000000h
240h	4	"reg_SSTATAR_type (SSTATAR6)—Offset 240h" on page 3124	00000000h
248h	4	"reg_DSTATAR_type (DSTATAR6)—Offset 248h" on page 3125	00000000h
250h	4	"reg_CFG_LO_type (CFG_LO6)—Offset 250h" on page 3125	00000203h
254h	4	"reg_CFG_HI_type (CFG_HI6)—Offset 254h" on page 3127	00000000h
258h	4	"reg_SGR_type (SGR6)—Offset 258h" on page 3128	00000000h
260h	4	"reg_DSR_type (DSR6)—Offset 260h" on page 3129	00000000h
268h	4	"reg_SAR_type (SAR7)—Offset 268h" on page 3129	00000000h
270h	4	"reg_DAR_type (DAR7)—Offset 270h" on page 3130	00000000h
278h	4	"reg_LLP_type (LLP7)—Offset 278h" on page 3131	00000000h
280h	4	"reg_CTL_LO_type (CTL_LO7)—Offset 280h" on page 3132	00000000h
284h	4	"reg_CTL_HI_type (CTL_HI7)—Offset 284h" on page 3133	00000000h
288h	4	"reg_SSTAT_type (SSTAT7)—Offset 288h" on page 3134	00000000h
290h	4	"reg_DSTAT_type (DSTAT7)—Offset 290h" on page 3135	00000000h
298h	4	"reg_SSTATAR_type (SSTATAR7)—Offset 298h" on page 3135	00000000h
2A0h	4	"reg_DSTATAR_type (DSTATAR7)—Offset 2A0h" on page 3136	00000000h
2A8h	4	"reg_CFG_LO_type (CFG_LO7)—Offset 2A8h" on page 3136	00000203h
2ACh	4	"reg_CFG_HI_type (CFG_HI7)—Offset 2ACh" on page 3138	00000000h
2B0h	4	"reg_SGR_type (SGR7)—Offset 2B0h" on page 3139	00000000h
2B8h	4	"reg_DSR_type (DSR7)—Offset 2B8h" on page 3140	00000000h
2C0h	4	"reg_Raw_type (RawTfr)—Offset 2C0h" on page 3140	00000000h
2C8h	4	"reg_Raw_type (RawBlock)—Offset 2C8h" on page 3141	00000000h
2D0h	4	"reg_Raw_type (RawSrcTran)—Offset 2D0h" on page 3142	00000000h
2D8h	4	"reg_Raw_type (RawDstTran)—Offset 2D8h" on page 3142	00000000h
2E0h	4	"reg_Raw_type (RawErr)—Offset 2E0h" on page 3143	00000000h
2E8h	4	"reg_Status_type (StatusTfr)—Offset 2E8h" on page 3143	00000000h
2F0h	4	"reg_Status_type (StatusBlock)—Offset 2F0h" on page 3144	00000000h

Table 238. Summary of Low Power Audio DMA1 Memory Mapped I/O Registers—lpe_bridge.BAR (Continued)

Offset	Size	Register ID—Description	Default Value
2F8h	4	"reg_Status_type (StatusSrcTran)—Offset 2F8h" on page 3145	00000000h
300h	4	"reg_Status_type (StatusDstTran)—Offset 300h" on page 3145	00000000h
308h	4	"reg_Status_type (StatusErr)—Offset 308h" on page 3146	00000000h
310h	4	"reg_Mask_type (MaskTfr)—Offset 310h" on page 3146	00000000h
318h	4	"reg_Mask_type (MaskBlock)—Offset 318h" on page 3147	00000000h
320h	4	"reg_Mask_type (MaskSrcTran)—Offset 320h" on page 3148	00000000h
328h	4	"reg_Mask_type (MaskDstTran)—Offset 328h" on page 3149	00000000h
330h	4	"reg_Mask_type (MaskErr)—Offset 330h" on page 3150	00000000h
338h	4	"reg_Clear_type (ClearTfr)—Offset 338h" on page 3150	00000000h
340h	4	"reg_Clear_type (ClearBlock)—Offset 340h" on page 3151	00000000h
348h	4	"reg_Clear_type (ClearSrcTran)—Offset 348h" on page 3152	00000000h
350h	4	"reg_Clear_type (ClearDstTran)—Offset 350h" on page 3152	00000000h
358h	4	"reg_Clear_type (ClearErr)—Offset 358h" on page 3153	00000000h
360h	4	"reg_StatusInt_type (StatusInt)—Offset 360h" on page 3153	00000000h
398h	4	"reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h" on page 3154	00000000h
3A0h	4	"reg_ChEnReg_type (ChEnReg)—Offset 3A0h" on page 3154	00000000h
3B8h	4	"reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h" on page 3155	00000000h
3BCh	4	"reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh" on page 3156	00000000h
3C0h	4	"reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h" on page 3156	00000000h
3C4h	4	"reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h" on page 3157	00000000h
400h	4	"reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h" on page 3157	00000000h
404h	4	"reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h" on page 3158	00000000h
408h	4	"reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h" on page 3159	00000000h
40Ch	4	"reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch" on page 3159	00000000h
410h	4	"reg_SAI_Error_type (SAI_ERR)—Offset 410h" on page 3160	00000000h
418h	4	"reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h" on page 3160	00000000h

21.16.1 reg_SAR_type (SAR0)—Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR0: [BAR + 9C000h] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.2 reg_DAR_type (DAR0)—Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR0: [BAR + 9C000h] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.3 reg_LLP_type (LLP0)—Offset 10h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP0: [BAR + 9C000h] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.16.4 reg_CTL_LO_type (CTL_LO0)—Offset 18h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_LO0: [BAR + 9C000h] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:29	28	27	26:22	21:20	19	18	17	16:14	13:11	10	9	8	7	6:4	3:1	0
Default	0 0 0	0	0	0 0 0 0 0	0 0	0	0	0	0 0 0	0 0 0	0	0	0	0	0 0 0	0 0 0	0
Field	RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.16.5 reg_CTL_HI_type (CTL_HI0)—Offset 1Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI0: [BAR + 9C000h] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH_CLASS			CH_WEIGHT											DONE	BLOCK_TS																

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.16.6 reg_SSTAT_type (SSTAT0)—Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT0: [BAR + 9C000h] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.16.7 reg_DSTAT_type (DSTAT0)—Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT0: [BAR + 9C000h] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.16.8 reg_SSTATAR_type (SSTATAR0)—Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR0: [BAR + 9C000h] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.16.9 reg_DSTATAR_type (DSTATAR0)—Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR0: [BAR + 9C000h] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.16.10 reg_CFG_LO_type (CFG_LO0)—Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO0: [BAR + 9C000h] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 0 | 0 0 0 0 | 0 0 1 1

RELOAD_DST | RELOAD_SRC | Reserved_29_22 | SRC_OPT_BL | DST_OPT_BL | SRC_HS_POL | DST_HS_POL | WR_CTLHI_SNP | WR_STAT_SNP | RD_STAT_SNP | RD_LLP_SNP | WR_SNP | RD_SNP | Reserved_11 | CH_DRAIN | FIFO_EMPTY | CH_SUSP | SS_UPD_EN | DS_UPD_EN | CTL_HI_UPD_EN | RSVD_4_4 | HSHAKE_NP_WR | ALL_NP_WR | SRC_BURST_ALIGN | DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.16.11 reg_CFG_HI_type (CFG_HI0)—Offset 44h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI0: [BAR + 9C000h] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.16.12 reg_SGR_type (SGR0)—Offset 48h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR0: [BAR + 9C000h] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.16.13 reg_DSR_type (DSR0)—Offset 50h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR0: [BAR + 9C000h] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.16.14 reg_SAR_type (SAR1)—Offset 58h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR1: [BAR + 9C000h] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.15 reg_DAR_type (DAR1)—Offset 60h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR1: [BAR + 9C000h] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.16 reg_LLP_type (LLP1)—Offset 68h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP1: [BAR + 9C000h] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC (31:2) | RSVD2 (1:0)

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.16.17 reg_CTL_LO_type (CTL_LO1)—Offset 70h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO1: [BAR + 9C000h] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			LLP_SRC_EN	LLP_DST_EN	RSVD1					TT_FC		RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE			DEST_MSIZE			SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH			DST_TR_WIDTH			INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.16.18 reg_CTL_HI_type (CTL_HI1)—Offset 74h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI1: [BAR + 9C000h] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CH_CLASS	CH_WEIGHT	DONE	BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.16.19 reg_SSTAT_type (SSTAT1)—Offset 78h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTAT1: [BAR + 9C000h] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.16.20 reg_DSTAT_type (DSTAT1)—Offset 80h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT1: [BAR + 9C000h] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.16.21 reg_SSTATAR_type (SSTATAR1)—Offset 88h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR1: [BAR + 9C000h] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.16.22 reg_DSTATAR_type (DSTATAR1)—Offset 90h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR1: [BAR + 9C000h] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.16.23 reg_CFG_LO_type (CFG_LO1)—Offset 98h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO1: [BAR + 9C000h] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

31	30	29:22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
RELOAD_DST	RELOAD_SRC	Reserved_29_22	SRC_OPT_BL	DST_OPT_BL	SRC_HS_POL	DST_HS_POL	WR_CTLHI_SNP	WR_STAT_SNP	RD_STAT_SNP	RD_LLP_SNP	WR_SNP	RD_SNP	Reserved_11	CH_DRAIN	FIFO_EMPTY	CH_SUSP	SS_UPD_EN	DS_UPD_EN	CTL_HI_UPD_EN	RSVD_4_4	HSHAKE_NP_WR	ALL_NP_WR	SRC_BURST_ALIGN	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.16.24 reg_CFG_HI_type (CFG_HI1)—Offset 9Ch

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI1: [BAR + 9C000h] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:30	DST_PER_EXT
29:28	SRC_PER_EXT
27:18	WR_ISSUE_THD
17:8	RD_ISSUE_THD
7:4	DST_PER
3:0	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.16.25 reg_SGR_type (SGR1)—Offset A0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SGR1: [BAR + 9C000h] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.16.26 reg_DSR_type (DSR1)—Offset A8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR1: [BAR + 9C000h] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.16.27 reg_SAR_type (SAR2)—Offset B0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR2: [BAR + 9C000h] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.28 reg_DAR_type (DAR2)—Offset B8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR2: [BAR + 9C000h] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.29 reg_LLP_type (LLP2)—Offset C0h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP2: [BAR + 9C000h] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.16.30 reg_CTL_LO_type (CTL_LO2)—Offset C8h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO2: [BAR + 9C000h] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:29	28	27	26:22	21:20	19	18	17	16:14	13:11	10	9	8	7	6:4	3:1	0
Default	000	0	0	00000	00	0	0	0	000	000	0	0	0	0	000	000	0
Field	RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.16.31 reg_CTL_HI_type (CTL_HI2)—Offset CCh

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI2: [BAR + 9C000h] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	CH_CLASS							CH_WEIGHT						DONE									BLOCK_TS								

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.16.32 reg_SSTAT_type (SSTAT2)—Offset D0h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT2: [BAR + 9C000h] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.16.33 reg_DSTAT_type (DSTAT2)—Offset D8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT2: [BAR + 9C000h] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.16.34 reg_SSTATAR_type (SSTATAR2)—Offset E0h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR2: [BAR + 9C000h] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.16.35 reg_DSTATAR_type (DSTATAR2)—Offset E8h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR2: [BAR + 9C000h] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.16.36 reg_CFG_LO_type (CFG_LO2)—Offset F0h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO2: [BAR + 9C000h] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bit	31	30	29:22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
Field	RELOAD_DST	RELOAD_SRC	Reserved_29_22	SRC_OPT_BL	DST_OPT_BL	SRC_HS_POL	DST_HS_POL	WR_CTLHI_SNP	WR_STAT_SNP	RD_STAT_SNP	RD_LLP_SNP	WR_SNP	RD_SNP	Reserved_11	CH_DRAIN	FIFO_EMPTY	CH_SUSP	SS_UPD_EN	DS_UPD_EN	CTL_HI_UPD_EN	RSVD_4_4	HSHAKE_NP_WR	ALL_NP_WR	SRC_BURST_ALIGN	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.16.37 reg_CFG_HI_type (CFG_HI2)—Offset F4h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI2: [BAR + 9C000h] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:30	29:28	27:18	17:8	7:4	3:0
Default	0 0	0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0
Field	DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.16.38 reg_SGR_type (SGR2)—Offset F8h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR2: [BAR + 9C000h] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SGC (31:20)	SGI (19:0)

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.16.39 reg_DSR_type (DSR2)—Offset 100h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR2: [BAR + 9C000h] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.16.40 reg_SAR_type (SAR3)—Offset 108h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR3: [BAR + 9C000h] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.41 reg_DAR_type (DAR3)—Offset 110h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR3: [BAR + 9C000h] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.42 reg_LLP_type (LLP3)—Offset 118h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP3: [BAR + 9C000h] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.16.43 reg_CTL_LO_type (CTL_LO3)—Offset 120h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO3: [BAR + 9C000h] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Field	RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN
Bits	31:29	28	27	26:22	21:20	19	18	17	16:14	13:11	10	9	8	7	6:4	3:1	0
Default	0 0 0	0	0	0 0 0 0 0	0 0	0	0	0	0 0 0	0 0 0	0	0	0	0	0 0 0	0 0 0	0

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.16.44 reg_CTL_HI_type (CTL_HI3)—Offset 124h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI3: [BAR + 9C000h] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH_CLASS			CH_WEIGHT											DONE	BLOCK_TS																

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.16.45 reg_SSTAT_type (SSTAT3)—Offset 128h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT3: [BAR + 9C000h] + 128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.16.46 reg_DSTAT_type (DSTAT3)—Offset 130h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT3: [BAR + 9C000h] + 130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.16.47 reg_SSTATAR_type (SSTATAR3)—Offset 138h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR3: [BAR + 9C000h] + 138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.16.48 reg_DSTATAR_type (DSTATAR3)—Offset 140h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR3: [BAR + 9C000h] + 140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.16.49 reg_CFG_LO_type (CFG_LO3)—Offset 148h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO3: [BAR + 9C000h] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
RELOAD_DST	RELOAD_SRC	Reserved_29_22								SRC_OPT_BL	DST_OPT_BL	SRC_HS_POL	DST_HS_POL	WR_CTLHI_SNP	WR_STAT_SNP	RD_STAT_SNP	RD_LLP_SNP	WR_SNP	RD_SNP	Reserved_11	CH_DRAIN	FIFO_EMPTY	CH_SUSP	SS_UPD_EN	DS_UPD_EN	CTL_HI_UPD_EN	RSVD_4_4	HSHAKE_NP_WR	ALL_NP_WR	SRC_BURST_ALIGN	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.16.50 reg_CFG_HI_type (CFG_HI3)—Offset 14Ch

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI3: [BAR + 9C000h] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	30	29–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0	0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
DST_PER_EXT	SRC_PER_EXT		WR_ISSUE_THD			RD_ISSUE_THD		DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.16.51 reg_SGR_type (SGR3)—Offset 150h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR3: [BAR + 9C000h] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.16.52 reg_DSR_type (DSR3)—Offset 158h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR3: [BAR + 9C000h] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.16.53 reg_SAR_type (SAR4)—Offset 160h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR4: [BAR + 9C000h] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.54 reg_DAR_type (DAR4)—Offset 168h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR4: [BAR + 9C000h] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.55 reg_LLP_type (LLP4)—Offset 170h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP4: [BAR + 9C000h] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.16.56 reg_CTL_LO_type (CTL_LO4)—Offset 178h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO4: [BAR + 9C000h] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			LLP_SRC_EN	LLP_DST_EN	RSVD1					TT_FC		RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE			DEST_MSIZE			SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH			DST_TR_WIDTH			INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.16.57 reg_CTL_HI_type (CTL_HI4)—Offset 17Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI4: [BAR + 9C000h] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CH_CLASS | CH_WEIGHT | DONE | BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.16.58 reg_SSTAT_type (SSTAT4)—Offset 180h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT4: [BAR + 9C000h] + 180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.16.59 reg_DSTAT_type (DSTAT4)—Offset 188h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTAT4: [BAR + 9C000h] + 188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.16.60 reg_SSTATAR_type (SSTATAR4)—Offset 190h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTATAR4: [BAR + 9C000h] + 190h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.16.61 reg_DSTATAR_type (DSTATAR4)—Offset 198h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR4: [BAR + 9C000h] + 198h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTATAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.16.62 reg_CFG_LO_type (CFG_LO4)—Offset 1A0h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO4: [BAR + 9C000h] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

31		28	24	20				16				12				8				4					0
0	0	0 0 0 0 0 0 0 0		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	
RELOAD_DST	RELOAD_SRC	Reserved_29_22		SRC_OPT_BL	DST_OPT_BL	SRC_HS_POL	DST_HS_POL	WR_CTLHI_SNP	WR_STAT_SNP	RD_STAT_SNP	RD_LLP_SNP	WR_SNP	RD_SNP	Reserved_11	CH_DRAIN	FIFO_EMPTY	CH_SUSP	SS_UPD_EN	DS_UPD_EN	CTL_HI_UPD_EN	RSVD_4_4	HSHAKE_NP_WR	ALL_NP_WR	SRC_BURST_ALIGN	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.16.63 reg_CFG_HI_type (CFG_HI4)—Offset 1A4h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI4: [BAR + 9C000h] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:30	29:28	27:18	17:8	7:4	3:0
Default	0 0	0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0
Field	DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.16.64 reg_SGR_type (SGR4)—Offset 1A8h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SGR4: [BAR + 9C000h] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.16.65 reg_DSR_type (DSR4)—Offset 1B0h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSR4: [BAR + 9C000h] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.16.66 reg_SAR_type (SAR5)—Offset 1B8h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SAR5: [BAR + 9C000h] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.67 reg_DAR_type (DAR5)—Offset 1C0h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR5: [BAR + 9C000h] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.68 reg_LLP_type (LLP5)—Offset 1C8h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP5: [BAR + 9C000h] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.16.69 reg_CTL_LO_type (CTL_LO5)—Offset 1D0h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO5: [BAR + 9C000h] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			LLP_SRC_EN	LLP_DST_EN	RSVD1					TT_FC		RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE			DEST_MSIZE			SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH			DST_TR_WIDTH			INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.16.70 reg_CTL_HI_type (CTL_HI5)—Offset 1D4h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI5: [BAR + 9C000h] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CH_CLASS | CH_WEIGHT | DONE | BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.16.71 reg_SSTAT_type (SSTAT5)—Offset 1D8h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT5: [BAR + 9C000h] + 1D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.16.72 reg_DSTAT_type (DSTAT5)—Offset 1E0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT5: [BAR + 9C000h] + 1E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.16.73 reg_SSTATAR_type (SSTATAR5)—Offset 1E8h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR5: [BAR + 9C000h] + 1E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.16.74 reg_DSTATAR_type (DSTATAR5)—Offset 1F0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR5: [BAR + 9C000h] + 1F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.16.75 reg_CFG_LO_type (CFG_LO5)—Offset 1F8h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO5: [BAR + 9C000h] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
RELOAD_DST	RELOAD_SRC	Reserved_29_22								SRC_OPT_BL	DST_OPT_BL	SRC_HS_POL	DST_HS_POL	WR_CTLHI_SNP	WR_STAT_SNP	RD_STAT_SNP	RD_LLP_SNP	WR_SNP	RD_SNP	Reserved_11	CH_DRAIN	FIFO_EMPTY	CH_SUSP	SS_UPD_EN	DS_UPD_EN	CTL_HI_UPD_EN	RSVD_4_4	HSHAKE_NP_WR	ALL_NP_WR	SRC_BURST_ALIGN	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.16.76 reg_CFG_HI_type (CFG_HI5)—Offset 1FCh

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI5: [BAR + 9C000h] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31	30	29–22	21–14	13–8	7–0
Default	0	0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.16.77 reg_SGR_type (SGR5)—Offset 200h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SGR5: [BAR + 9C000h] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.16.78 reg_DSR_type (DSR5)—Offset 208h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR5: [BAR + 9C000h] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DSC | DSI

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.16.79 reg_SAR_type (SAR6)—Offset 210h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR6: [BAR + 9C000h] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.80 reg_DAR_type (DAR6)—Offset 218h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR6: [BAR + 9C000h] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.81 reg_LLP_type (LLP6)—Offset 220h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP6: [BAR + 9C000h] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														RSVD2	

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.16.82 reg_CTL_LO_type (CTL_LO6)—Offset 228h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO6: [BAR + 9C000h] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN
31:29	28	27	26:22	21:20	19	18	17	16:14	13:11	10	9	8	7	6:4	3:1	0
0 0 0	0	0	0 0 0 0 0	0 0	0	0	0	0 0 0	0 0 0	0	0	0	0	0 0 0	0 0 0	0

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.16.83 reg_CTL_HI_type (CTL_HI6)—Offset 22Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

CTL_HI6: [BAR + 9C000h] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CH_CLASS | CH_WEIGHT | DONE | BLOCK_TS

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.16.84 reg_SSTAT_type (SSTAT6)—Offset 230h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSTAT6: [BAR + 9C000h] + 230h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.16.85 reg_DSTAT_type (DSTAT6)—Offset 238h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT6: [BAR + 9C000h] + 238h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.16.86 reg_SSTATAR_type (SSTATAR6)—Offset 240h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR6: [BAR + 9C000h] + 240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.16.87 reg_DSTATAR_type (DSTATAR6)—Offset 248h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR6: [BAR + 9C000h] + 248h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.16.88 reg_CFG_LO_type (CFG_LO6)—Offset 250h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO6: [BAR + 9C000h] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bits	Default	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:22	0 0 0 0 0 0 0 0	Reserved_29_22
21	0	SRC_OPT_BL
20	0	DST_OPT_BL
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	WR_CTLHI_SNP
16	0	WR_STAT_SNP
15	0	RD_STAT_SNP
14	0	RD_LLP_SNP
13	0	WR_SNP
12	0	RD_SNP
11	0	Reserved_11
10	0	CH_DRAIN
9	1	FIFO_EMPTY
8	0	CH_SUSP
7	0	SS_UPD_EN
6	0	DS_UPD_EN
5	0	CTL_HI_UPD_EN
4	0	RSVD_4_4
3	0	HSHAKE_NP_WR
2	0	ALL_NP_WR
1	1	SRC_BURST_ALIGN
0	1	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.16.89 reg_CFG_HI_type (CFG_HI6)—Offset 254h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI6: [BAR + 9C000h] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:30	29:28	27:18	17:8	7:4	3:0
Default	0 0	0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0
Field	DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.16.90 reg_SGR_type (SGR6)—Offset 258h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SGR6: [BAR + 9C000h] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.16.91 reg_DSR_type (DSR6)—Offset 260h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR6: [BAR + 9C000h] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.16.92 reg_SAR_type (SAR7)—Offset 268h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAR7: [BAR + 9C000h] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.93 reg_DAR_type (DAR7)—Offset 270h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DAR7: [BAR + 9C000h] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Description
31:0	0h RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

21.16.94 reg_LLP_type (LLP7)—Offset 278h

Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LLP7: [BAR + 9C000h] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC (bits 31:2) | RSVD2 (bits 1:0)

Bit Range	Default & Access	Description
31:2	00000000h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	**RSVD2:** Reserved

21.16.95 reg_CTL_LO_type (CTL_LO7)—Offset 280h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_LO7: [BAR + 9C000h] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31:29	28	27	26:22	21:20	19	18	17	16:14	13:11	10	9	8	7	6:4	3:1	0
0 0 0	0	0	0 0 0 0 0	0 0	0	0	0	0 0 0	0 0 0	0	0	0	0	0 0 0	0 0 0	0
RSVD	LLP_SRC_EN	LLP_DST_EN	RSVD1	TT_FC	RSVD2	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	RSVD3	DINC	RSVD4	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Description
31:29	0h RO	**RSVD:** Reserved
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	**RSVD1:** RSVD
21:20	0h RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	**RSVD2:** Reserved
18	0h RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0h RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0h RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Description
9	0h RO	**RSVD3:** Reserved
8	0h RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	**RSVD4:** Reserved
6:4	0h RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

21.16.96 reg_CTL_HI_type (CTL_HI7)—Offset 284h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CTL_HI7: [BAR + 9C000h] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH_CLASS			CH_WEIGHT											DONE	BLOCK_TS																

Bit Range	Default & Access	Description
31:29	0h RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Description
28:18	0h RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

21.16.97 reg_SSTAT_type (SSTAT7)—Offset 288h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTAT7: [BAR + 9C000h] + 288h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

21.16.98 reg_DSTAT_type (DSTAT7)—Offset 290h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSTAT7: [BAR + 9C000h] + 290h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

21.16.99 reg_SSTATAR_type (SSTATAR7)—Offset 298h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SSTATAR7: [BAR + 9C000h] + 298h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

21.16.100 reg_DSTATAR_type (DSTATAR7)—Offset 2A0h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DSTATAR7: [BAR + 9C000h] + 2A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTATAR

Bit Range	Default & Access	Description
31:0	0h RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

21.16.101 reg_CFG_LO_type (CFG_LO7)—Offset 2A8h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_LO7: [BAR + 9C000h] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000203h

Bits	Default	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:22	0 0 0 0 0 0 0 0	Reserved_29_22
21	0	SRC_OPT_BL
20	0	DST_OPT_BL
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	WR_CTLHI_SNP
16	0	WR_STAT_SNP
15	0	RD_STAT_SNP
14	0	RD_LLP_SNP
13	0	WR_SNP
12	0	RD_SNP
11	0	Reserved_11
10	0	CH_DRAIN
9	1	FIFO_EMPTY
8	0	CH_SUSP
7	0	SS_UPD_EN
6	0	DS_UPD_EN
5	0	CTL_HI_UPD_EN
4	0	RSVD_4_4
3	0	HSHAKE_NP_WR
2	0	ALL_NP_WR
1	1	SRC_BURST_ALIGN
0	1	DST_BURST_ALIGN

Bit Range	Default & Access	Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	00h RO	**Reserved_29_22:** Reserved
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0h RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0h RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0h RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0h RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0h RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0h RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0b RO	**Reserved_11:** Reserved
10	0b RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default & Access	Description
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	**RSVD_4_4:** Reserved
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

21.16.102 reg_CFG_HI_type (CFG_HI7)—Offset 2ACh

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CFG_HI7: [BAR + 9C000h] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31	Bit 30	Bits 29:20	Bits 19:10	Bits 7:4	Bits 3:0
DST_PER_EXT	SRC_PER_EXT	WR_ISSUE_THD	RD_ISSUE_THD	DST_PER	SRC_PER

Bit Range	Default & Access	Description
31:30	0h RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0h RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

21.16.103 reg_SGR_type (SGR7)—Offset 2B0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SGR7: [BAR + 9C000h] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits 31–20	Bits 19–0
0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SGC	SGI

Bit Range	Default & Access	Description
31:20	0h RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI:** Source gather interval.

21.16.104 reg_DSR_type (DSR7)—Offset 2B8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

DSR7: [BAR + 9C000h] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Description
31:20	0h RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**DSI:** Destination scatter interval.

21.16.105 reg_Raw_type (RawTfr)—Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawTfr: [BAR + 9C000h] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (bits 31:8), RAW (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.16.106 reg_Raw_type (RawBlock)—Offset 2C8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawBlock: [BAR + 9C000h] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (bits 31:8), RAW (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.16.107 reg_Raw_type (RawSrcTran)—Offset 2D0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawSrcTran: [BAR + 9C000h] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RAW							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.16.108 reg_Raw_type (RawDstTran)—Offset 2D8h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RawDstTran: [BAR + 9C000h] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RAW							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.16.109 reg_Raw_type (RawErr)—Offset 2E0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RawErr: [BAR + 9C000h] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RAW							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**RAW:** Raw interrupt status

21.16.110 reg_Status_type (StatusTfr)—Offset 2E8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

StatusTfr: [BAR + 9C000h] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD						STATUS	

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.16.111 reg_Status_type (StatusBlock)—Offset 2F0h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

StatusBlock: [BAR + 9C000h] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD						STATUS	

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.16.112 reg_Status_type (StatusSrcTran)—Offset 2F8h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusSrcTran: [BAR + 9C000h] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								STATUS							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.16.113 reg_Status_type (StatusDstTran)—Offset 300h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

StatusDstTran: [BAR + 9C000h] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								STATUS							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.16.114 reg_Status_type (StatusErr)—Offset 308h

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

StatusErr: [BAR + 9C000h] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								STATUS							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**STATUS:** Interrupt status

21.16.115 reg_Mask_type (MaskTfr)—Offset 310h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskTfr: [BAR + 9C000h] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD2 (31:16) | INT_MASK_WE (15:8) | INT_MASK (7:0)

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.16.116 reg_Mask_type (MaskBlock)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskBlock: [BAR + 9C000h] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD2	INT_MASK_WE	INT_MASK

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.16.117 reg_Mask_type (MaskSrcTran)—Offset 320h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskSrcTran: [BAR + 9C000h] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD2	INT_MASK_WE	INT_MASK

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.16.118 reg_Mask_type (MaskDstTran)—Offset 328h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

MaskDstTran: [BAR + 9C000h] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD2 | INT_MASK_WE | INT_MASK

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.16.119 reg_Mask_type (MaskErr)—Offset 330h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MaskErr: [BAR + 9C000h] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

Bits	31:16	15:8	7:0
Default	0000 0000 0000 0000	0000 0000	0000 0000
Field	RSVD2	INT_MASK_WE	INT_MASK

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0h RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

21.16.120 reg_Clear_type (ClearTfr)—Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClearTfr: [BAR + 9C000h] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (bits 31:8), CLEAR (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.16.121 reg_Clear_type (ClearBlock)—Offset 340h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClearBlock: [BAR + 9C000h] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (bits 31:8), CLEAR (bits 7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.16.122 reg_Clear_type (ClearSrcTran)—Offset 348h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearSrcTran: [BAR + 9C000h] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (31:8), CLEAR (7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.16.123 reg_Clear_type (ClearDstTran)—Offset 350h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClearDstTran: [BAR + 9C000h] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (31:8), CLEAR (7:0)

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Description
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.16.124 reg_Clear_type (ClearErr)—Offset 358h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClearErr: [BAR + 9C000h] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								CLEAR							

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

21.16.125 reg_StatusInt_type (StatusInt)—Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

StatusInt: [BAR + 9C000h] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																											ERR	DSTT	SRCT	BLOCK	TFR

Bit Range	Default & Access	Description
31:5	0h RO	**RSVD:** Reserved
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

21.16.126 reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DmaCfgReg: [BAR + 9C000h] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																															DMA_EN

Bit Range	Default & Access	Description
31:1	0h RO	**RSVD:** Reserved
0	0h RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

21.16.127 reg_ChEnReg_type (ChEnReg)—Offset 3A0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ChEnReg: [BAR + 9C000h] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD2																CH_EN_WE								CH_EN							

Bit Range	Default & Access	Description
31:16	0h RO	**RSVD2:** Reserved
15:8	0h WO	**CH_EN_WE:** Channel enable write enable.
7:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

21.16.128 reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority0_LO: [BAR + 9C000h] + 3B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD2										WT_CLASS_1											WT_CLASS_0										

Bit Range	Default & Access	Description
31:22	0h RO	**RSVD2:** Reserved

Bit Range	Default & Access	Description
21:11	0h RW	**WT_CLASS_1:** Class Weight 1: Value of K assigns a weight of (K+1) to Class 1. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_0:** Class Weight 0: Value of K assigns a weight of (K+1) to Class 0. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

21.16.129 reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClassPriority0_HI: [BAR + 9C000h] + 3BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:23	22	21:11	10:0
RSVD1	STRICT_PRI	WT_CLASS_3	WT_CLASS_2

Bit Range	Default & Access	Description
31:23	0h RO	**RSVD1:** Reserved
22	0h RW	**STRICT_PRI:** If set, Higher class values will always have higher priorities than lower class values. If not set, round-robin arbitration will be used between different classes using WT_CLASS_n values.
21:11	0h RW	**WT_CLASS_3:** Class Weight 3: Value of K assigns a weight of (K+1) to Class 3. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_2:** Class Weight 2: Value of K assigns a weight of (K+1) to Class 2. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

21.16.130 reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ClassPriority1_LO: [BAR + 9C000h] + 3C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD2										WT_CLASS_5											WT_CLASS_4										

Bit Range	Default & Access	Description
31:22	0h RO	**RSVD2:** Reserved
21:11	0h RW	**WT_CLASS_5:** Class Weight 5: Value of K assigns a weight of (K+1) to Class 5. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_4:** Class Weight 4: Value of K assigns a weight of (K+1) to Class 4. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

21.16.131 reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ClassPriority1_HI: [BAR + 9C000h] + 3C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD1										WT_CLASS_7											WT_CLASS_6										

Bit Range	Default & Access	Description
31:22	0h RO	**RSVD1:** Reserved
21:11	0h RW	**WT_CLASS_7:** Class Weight 7: Value of K assigns a weight of (K+1) to Class 7. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0h RW	**WT_CLASS_6:** Class Weight 6: Value of K assigns a weight of (K+1) to Class 6. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

21.16.132 reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

FifoPartition0_LO: [BAR + 9C000h] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD2 | PARTITION_UPDATE | PSIZE_CH_1 | PSIZE_CH_0

Bit Range	Default & Access	Description
31:27	0h RO	**RSVD2:** Reserved
26	0h RW	**PARTITION_UPDATE:** SW needs to write to this bit for the partitioning assignments to take effect.
25:13	0h RW	**PSIZE_CH_1:** Partition Byte Size assigned to Channel 1. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_0:** Partition Byte Size assigned to Channel 0. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

21.16.133 reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

FifoPartition0_HI: [BAR + 9C000h] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD1 | PSIZE_CH_3 | PSIZE_CH_2

Bit Range	Default & Access	Description
31:26	0h RO	**RSVD1:** Reserved
25:13	0h RW	**PSIZE_CH_3:** Partition Byte Size assigned to Channel 3. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

Bit Range	Default & Access	Description
12:0	0h RW	**PSIZE_CH_2:** Partition Byte Size assigned to Channel 2. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

21.16.134 reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition1_LO: [BAR + 9C000h] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD2 (31:26), PSIZE_CH_5 (25:13), PSIZE_CH_4 (12:0)

Bit Range	Default & Access	Description
31:26	0h RO	**RSVD2:** Reserved
25:13	0h RW	**PSIZE_CH_5:** Partition Byte Size assigned to Channel 5. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_4:** Partition Byte Size assigned to Channel 4. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

21.16.135 reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FifoPartition1_HI: [BAR + 9C000h] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD1, PSIZE_CH_7, PSIZE_CH_6

Bit Range	Default & Access	Description
31:26	0h RO	**RSVD1:** Reserved
25:13	0h RW	**PSIZE_CH_7:** Partition Byte Size assigned to Channel 7. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0h RW	**PSIZE_CH_6:** Partition Byte Size assigned to Channel 6. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

21.16.136 reg_SAI_Error_type (SAI_ERR)—Offset 410h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SAI_ERR: [BAR + 9C000h] + 410h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
RSVD	CH_SAI_ERR

Bit Range	Default & Access	Description
31:8	0h RO	**RSVD:** Reserved
7:0	0h RO	**CH_SAI_ERR:** 1: SAI Error occurred on Ch [n] 0: No SAI Error occurred on Ch [n] SAI_ERROR[n] is set by HW on SAI violation for channel [n]. All bits get cleared by SW when reading this register

21.16.137 reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h

GLOBAL_CFG: GLOBAL DMA Configuration Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GLOBAL_CFG: [BAR + 9C000h] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:21, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
SCRATCH_PAD	ERR_ILL_REG

Bit Range	Default & Access	Description
31:1	0h RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future configuration and de-feature bits.
0	0b RW	**ERR_ILL_REG:** 0x1 : Issue ERR response on reading illegal (non-existing) registers 0x0 : Issue DVA response on reading illegal (non-existing) registers

22 Intel® Trusted Execution Engine (TXE)

This section describes the security components and capabilities of the Intel® Trusted Execution Engine (TXE) security co-processor.

Note: TXE firmware is required on the Bay Trail Platform as part of the PCU SPI flash image. PCU SPI must be setup in descriptor mode. For security reasons, primarily to lock PCU SPI flash access permission and OTP fue programming, TXE Manufacturing Mode must be Disabled before shipping to customers. See your Intel® representative for details.

22.1 Features

22.1.1 Security Feature

The Intel® TXE is a security co-processor responsible for supporting and handling security. Features include:

- 32-bit RISC processor
- 256KB Data/Code RAM accessible only to the Intel® TXE
- 128KB On Chip Mask ROM for storage of Intel® TXE code
- Common Timer 1-100 µS granularity, configurable interrupt (under FW control)
- Inter-Processor Communication for message passing between the Host CPU and Intel® TXE
- 64 byte input and output command buffers
- 256 byte shared payload (enables 2048-bit keys to be exchanged as part of the command)
- No Host CPU address domain access to the Intel® TXE address domain by any Host CPU address domain units
- Security controller has direct access to Host CPU address domain (Some Restrictions Apply). Multiple context DMA engine to transfer data between Host CPU address domain (System memory) and the Intel® TXE; programmable by the Intel® TXE CPU only.
- One multi-tiered FW Key Ladder and one Intel Key ladder.
- Paging DMA operations includes encryption/decryption and integrity check value (ICV) calculation. Auxiliary GPIOs to support input alert and two GP Outputs.

22.1.1.1 HW Accelerators

- DES/3DES (ECB, CBC) – 128b ABA key for 3DES Key Ladder Operations
- Three AES engines - Two fast -128 and one slow- 128/256

- Exponentiation Acceleration Unit (EAU) for modular exponentiation, modular reduction, large number addition, subtraction, and multiplication
- SHA1, SHA256/384/512, MD5

22.1.1.2 FW Utilities and Ciphers

- RSA (with EAU acceleration)
- Flash Write Enable/Disable
- Comprehensive IPC Command Set
- Chip Unique Key encryption key wrapping of other platform keys (Flash)

22.1.1.3 Downloadable FW Utilities and Ciphers

- Integrated Theft Deterrence Technology - Intel® Anti-Theft Technology (Intel® AT)
- Media Vault - content protection and distribution product specifically focused on online content for streaming and download
- One Time Programmable (OTP)

22.2 Register Map

See Chapters Section 3, "Register Access Methods" on page 69 and Section 4, "Mapping Address Spaces" on page 75 for additional information.

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22.3 Intel® TXE PCI Configuration Registers

Table 239. Summary of TXE PCI Configuration Registers—0/26/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device/Vendor ID (DEVVENDIDO)—Offset 0h" on page 3166	00108086h
4–7h	4	"Status Command (STATUSCOMMAND)—Offset 4h" on page 3166	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3167	10800000h
C–Fh	4	"CLLATHEADERBISTR (CLLATHEADERBIST)—Offset Ch" on page 3168	00000000h
10–13h	4	"SAP Agent Memory BAR (SAPAGENTBAR)—Offset 10h" on page 3168	00000000h
14–17h	4	"Bridge Memory BAR (BRIDGEBAR)—Offset 14h" on page 3169	00000000h
18h + [0-3]*4h	4	"Dummy BAR[0-3] (DUMMY_BARS[0-3])—Offset 18h, Count 4, Stride 4h" on page 3170	00000000h
2C–2Fh	4	"SUBSYSTEMID—Offset 2Ch" on page 3170	00000000h
30–33h	4	"EXPANSION_ROM_BASEADDR—Offset 30h" on page 3171	00000000h
34–37h	4	"CAPABILITYPTR—Offset 34h" on page 3171	00000080h
3C–3Fh	4	"INTERRUPTREG—Offset 3Ch" on page 3172	00000100h
40–43h	4	"SEC_FW_STS1—Offset 40h" on page 3172	00000000h
44–47h	4	"SEC_MEM_REQ—Offset 44h" on page 3175	00000000h
48–4Bh	4	"SEC_FW_STS0—Offset 48h" on page 3175	00000000h
4Ch + [0-4]*4h	4	"PCI_CONF_SEC_TO_HOST_3_7[0-4] (PCI_CONF_SEC_TO_HOST_3_7_REGS[0-4])—Offset 4Ch, Count 5, Stride 4h" on page 3177	00000000h
60–63h	4	"DID_MSG—Offset 60h" on page 3178	00000000h
64h + [0-6]*4h	4	"PCI_CONF_HOST_TO_SEC[0-6] (PCI_CONF_HOST_TO_SEC_1_7_REGS[0-6])—Offset 64h, Count 7, Stride 4h" on page 3179	00000000h
80–83h	4	"POWERCAPID—Offset 80h" on page 3179	4803A001h
84–87h	4	"PMECTRLSTATUS—Offset 84h" on page 3180	00000008h
88–8Bh	4	"CLK_GATE_DIS—Offset 88h" on page 3181	000000FFh
8C–8Fh	4	"TPM_ICR—Offset 8Ch" on page 3182	00000000h
A0–A3h	4	"MSICAP—Offset A0h" on page 3182	00000005h
A4–A7h	4	"MSIADDR—Offset A4h" on page 3183	00000000h
A8–ABh	4	"MSIDATA—Offset A8h" on page 3183	00000000h
B0–B3h	4	"IADBGCTRL—Offset B0h" on page 3184	00000000h
B4–B7h	4	"CPU_BIOS_ENV_PROTECT—Offset B4h" on page 3185	00000000h
C0–C3h	4	"SATT_BIOS_CTRL—Offset C0h" on page 3185	00001008h
C4–C7h	4	"SATT_BIOS_BA—Offset C4h" on page 3186	00000000h
C8–CBh	4	"SATT_BIOS_SIZE—Offset C8h" on page 3187	00000000h
D0–D3h	4	"SATT_TPM_CTRL (SATT_TPM_CTRL)—Offset D0h" on page 3187	00001008h
D4–D7h	4	"SATT_TPM_BA—Offset D4h" on page 3188	00000000h
D8–DBh	4	"SATT_TPM_SIZE—Offset D8h" on page 3188	00000000h
F0–F3h	4	"URRE—Offset F0h" on page 3189	00000000h
F8–FBh	4	"MANID—Offset F8h" on page 3189	00000000h

22.3.1 Device/Vendor ID (DEVVENDIDO)—Offset 0h

Device/Vendor ID. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 0h

Default: 00108086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

Bits	Field
31:23	DEVICEID_SETID
22:20	DEVICEID_CONST
19:16	DEVICEID_FUSE
15:0	VENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:23	X RO	**DEVICEID_SETID:** DIDH: Identifier assigned to the Device 26 SEC PCI device. Bits[31:23] of this register are obtained from SETID message sent by PMC
22:20	001b RO	**DEVICEID_CONST:** DIDM: Identifier assigned to the Device 26 SEC PCI device. Bits[22:20] of this register are strapped at SEC top level
19:16	X RO	**DEVICEID_FUSE[(DEVICEID_FUSE):** DIDL: Identifier assigned to the Device 26 SEC PCI device. Bits[19:16] of this register are determined by fuses
15:0	8086h RO	**VENDORID:** VID: PCI standard identification for Intel

22.3.2 Status Command (STATUSCOMMAND)—Offset 4h

Status Command. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	RSVD_31_31
30	SIGNALED_SYSTEM_ERROR_30
29	RMA
28:21	RSVD_28_21
20	CAPLIST
19	INTR_STATUS
18:11	RSVD_18_11
10	INTR_DISABLE
9	RSVD_9_9
8	SERR_EN_8
7:3	RSVD_7_3
2	BME
1	MSE
0	RSVD_0_0

Bit Range	Default & Access	Field Name (ID): Description
31	0b NA	**RESERVED (RSVD_31_31):** RESERVED BITS
30	X RW/C	**SIGNALED_SYSTEM_ERROR_30:** SERR status, write 1 to clear.
29	X RW/C	**RMA:** SERR status, write 1 to clear.
28:21	0b NA	**RESERVED (RSVD_28_21):** RESERVED BITS
20	1b RO	**CAPLIST:** CAP: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list
19	X RO	**INTR_STATUS:** IS: Reflects the state of the interrupt in the graphics device. Is set to 1 if interrupt (as determined by IIR and IER memory interface registers) is set to 1. Otherwise is set to 0
18:11	0b NA	**RESERVED (RSVD_18_11):** RESERVED BITS
10	X RW	**INTR_DISABLE:** ID: When 1, blocks the sending of a MSI interrupt and blocks the sending of a Message bus interrupt. The interrupt status is not blocked from being reflected in COMMANDSTATUS. INTR_STT. When 0, permits the sending of a MSI interrupt or Message bus interrupt. Note: Overall, a MSI interrupt is sent when the expression (COMMANDSTATUS. INTR_STT and ~COMMANDSTATUS. INTR_DIS and COMMANDSTATUS.BUS_MSTR_EN and MSI_CAPID.MSI_EN) changes from 0 to 1. Overall, a Message bus interrupt assert is sent when the expression (COMMANDSTATUS. INTR_STT and ~COMMANDSTATUS. INTR_DIS and ~MSI_CAPID.MSI_EN) changes from 0 to 1. The corresponding Message bus interrupt de-assert is sent when the expression (COMMANDSTATUS. INTR_STT and ~COMMANDSTATUS. INTR_DIS and ~MSI_CAPID.MSI_EN) changes from 1 to 0
9	0b NA	**RESERVED (RSVD_9_9):** RESERVED BITS
8	X RW	**INTR_STATUS (SERR_EN_8):** SERR enable.
7:3	0b NA	**RESERVED (RSVD_7_3):** RESERVED BITS
2	X RW	**BME:** BME: Enables GVD to function as a PCI compliant master. When 0, blocks the sending of MSI interrupts and DDR transactions. When 1, permits the sending of MSI interrupts and DDR transactions. Note: transactions to SEC paging IMR are not controlled (enabled/disabled) by this field
1	X RW	**MSE:** MSE: When set, accesses to this device's memory space is enabled. When 1, SEC will compare IOSF primary address MS bits with its BARs MS bits. If there is a match and if the IOSF command is either a MEMRD or MEMWR, SEC send the command to the destination pointed by the base address. Care should be taken in setting up SEC BARs that more than 1 match is not made as this will result in unpredictable behavior. When 0, the SEC will not select a MEMRD or MEMWR IOSF command
0	0b NA	**RESERVED (RSVD_0_0):** IOSE: Since SEC doesn't have I/O space, this bit is hard coded to 0. RESERVED BITS

22.3.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revision ID and Class Code. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 8h

Default: 10800000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 1	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
CLASS_CODES						RID	

Bit Range	Default & Access	Field Name (ID): Description
31:8	108000h RO	**CLASS_RESERVED (CLASS_CODES):** PCI Class Code
7:0	X RO	**RID:** PCI Revision ID

22.3.4 CLLATHEADERBISTR (CLLATHEADERBIST)—Offset Ch

PCI Cache Line Size, Latancy Timer, Header Type and BIST register. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:26, F:0] + Ch

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Reserved_31_24		Reserved_23_16		Reserved_15_8		CACHELINE_SIZE	

Bit Range	Default & Access	Field Name (ID): Description
31:24	X NA	**RESERVED (Reserved_31_24):** RESERVED BITS
23:16	X NA	**RESERVED (Reserved_23_16):** RESERVED BITS
15:8	X NA	**RESERVED (Reserved_15_8):** RESERVED BITS
7:0	X RO	**CACHELINE_SIZE:** CACHELINE_SIZE

22.3.5 SAP Agent Memory BAR (SAPAGENTBAR)—Offset 10h

Memory Bar of the SAP Agent. Request to this BAR will be directed to the SAP. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:26, F:0] + 10h

Default: 00000000h

Bits	31:20	19:16	15:4	3	2:1	0
Default	0000 0000 0000	0000	0000 0000 0000	0	00	0
Field	BaseAddressRegion	Reserved_19_16	Reserved_15_4	Reserved_3	Reserved_2_1	Reserved_0

Bit Range	Default & Access	Field Name (ID): Description
31:20	X RW	**BaseAddressRegion:** SAP Agent Base Address Region
19:16	X NA	**RESERVED (Reserved_19_16):** RESERVED BITS
15:4	X NA	**RESERVED (Reserved_15_4):** RESERVED BITS
3	X NA	**RESERVED (Reserved_3):** RESERVED BITS
2:1	X NA	**RESERVED (Reserved_2_1):** RESERVED BITS
0	X NA	**RESERVED (Reserved_0):** RESERVED BITS

22.3.6 Bridge Memory BAR (BRIDGEBAR)—Offset 14h

Memory Bar of the IOSF-)SAP Bridge. Request to this BAR will be directed to the Bridge configuration. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:26, F:0] + 14h

Default: 00000000h

Bits	31:20	19:1	0
Default	0000 0000 0000	000 0000 0000 0000 0000	0
Field	BaseAddressRegion	RSVD_19_0	RESRC_TYP

Bit Range	Default & Access	Field Name (ID): Description
31:20	X RW	**BaseAddressRegion:** BA: Set by the OS, these bits correspond to address signals [31:20]. SEC will compare the IOSF address (bits [31:20]) with SAP_BRIDGE_BAR.BASE_ADDR. If there is a match, and COMMANDSTATUS.MEM_SPC_EN = 1 and the IOSF command is either a MEMRD or MEMWR, SEC will send the command to its MMIO registers block. If there's no MMIO register in the accessed offset, SEC Bridge will send FFFF_FFFFh to indicate a miss on the IOSF bus
19:1	0b NA	**RESERVED (RSVD_19_0):** RESERVED BITS
0	0b RO	**RESRC_TYP:** RTE: Indicates a request for memory space

22.3.7 Dummy BAR[0-3] (DUMMY_BARS[0-3])—Offset 18h, Count 4, Stride 4h

Dummy BAR, Returns zeroes to indicate un-implemented BAR. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset[0-3]: [B:0, D:26, F:0] + 18h + [0-3]*4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD_31_0

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b NA	**RESERVED (RSVD_31_0):** RESERVED BITS

22.3.8 SUBSYSTEMID—Offset 2Ch

PCI Subsystem Identifiers. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 2Ch

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**SUBSYSTEMID:** The value in this field is programmed by the system BIOS. According to the PCI spec, only the BIOS can write it, and only once after reset. After the first write, this register becomes read-only. The content of this register may also be read (not written) from the Device 0 subsystem register address
15:0	0b RW	**SUBSYSTEMVENDORID:** The value in this field is programmed by the system BIOS. According to the PCI spec, only the BIOS can write it, and only once after reset. After the first write, this register becomes read-only. The content of this register may also be read (not written) from the Device 0 subsystem register address

22.3.9 EXPANSION_ROM_BASEADDR—Offset 30h

PCI Expansion ROM - disabled for SEC. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:26, F:0] + 30h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD_31_0																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0b NA	**RESERVED (RSVD_31_0):** RESERVED BITS, Expansion RO is disabled for SEC, therefore this field is hard coded to zero

22.3.10 CAPABILITYPTR—Offset 34h

PCI Capabilities Pointer, points to the next SEC capability which is Power management. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:26, F:0] + 34h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

RSVD_31_8 (bits 31:8), CAPPTR_POWER (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b NA	**RESERVED (RSVD_31_8):** RESERVED BITS
7:0	80h RW	**CAPPTR_POWER:** The first item in the capabilities list is at address 80h (PME)

22.3.11 INTERRUPTREG—Offset 3Ch

PCI Interrupt Register. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

RSVD_31_16 (bits 31:16), INTPIN (bits 15:8), INTLINE (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b NA	**RESERVED (RSVD_31_16):** RESERVED BITS
15:8	01h RO	**INTPIN:** IPIN: Value indicates which interrupt pin this device uses. This field is hard coded to 1h since Cedarview Device 26 is a single function device. The PCI spec requires that it use INTA#
7:0	X RW	**INTLINE:** ILIN: BIOS written value to communicate interrupt line routing information to the device driver

22.3.12 SEC_FW_STS1—Offset 40h

SeC Firmware Status Register 0. SeC FW uses this register in order to report its status to host (e.g. BIOS). Register acces control: FW=RW PMC=RO Host=RO

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 40h

Default: 00000000h

31 28	24	20 16	12 8 4 0
0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
INF_PROG_CODE	CURR_PM_EV	EXT_STAT_DAT_CURR_STATE	FUNC_RSVD_15

Bit Range	Default & Access	Field Name (ID): Description
31:28	X RW	**INF_PROG_CODE:** This field identifies the infrastructure progress code. For example, when firmware comes out of reset, this field would identify the infrastructure moving from ROM to BRINGUP to Micro Kernel to Policy module, etc. Note that this field is specific to infrastructure and does not represent the entire firmware. Refer to the Working State and Error Code fields to identify current state of the firmware. Values are as follows: 0: ROM. 1: Bringup. 2: uKernel. 3: Policy module. 4: Module loading. 6: Host communication. SeC is up and running, and host communication is established.
27:24	X RW	**CURR_PM_EV:** Status of current SeC power management event. Values as follows: 0x00: Clean Moff --) M0 wake. 0x01: Moff --) M0 wake after error. 0x02: Clean global reset. 0x03: Global Reset after an error. 0x04: Clean SeC reset. 0x05: SeC reset due to exception. 0x06: Pseudo-global reset. 0x07: Reserved. 0x08: Reserved. 0x09: Reserved. 0x0A: Reserved. 0x0B: Power cycle reset through MOff. 0x0C: Reserved. 0x0D: S0/M0 --) S0/MOff.

Bit Range	Default & Access	Field Name (ID): Description
23:16	X RW	**EXT_STAT_DAT_CURR_STATE:** The interpretation of this field's value depends on the value of field INF_PROG_CODE. For INF_PROG_CODE value of ROM, values are as follows: 0x000: Covers a number of steps early in ROM flow before entering main 0x001: Initialize memory map 0x002: Initialize the TPM Establishment bit 0x003: Initialize SusRAM 0x004: Get Fuse values 0x005: Derive chipset keys 0x006: Fuses/ Straps indicate ME disabled 0x007: Initialize HECI buffers 0x008: Find a FPT/Manifest image 0x009: Validate manifest found 0x00A: Load module found in manifest 0x00B: Transfer control over to new module 0x00C: Locate the FPT within memory 0x00D: Locate the Code partition within the FPT 0x00E: Initialize Paging logic 0x00F: Function designed to be patched wasn't prior to use. 0x010: H/W Page fault occured. 0x011: Derive chipset keys For INF_PROG_CODE value of Bringup, values are as follows: 0x00: Initialization starts 0x01: Disable the host wake event 0x02: Enabling clock gating for ME 0x03: Enabling PM ME handshaking 0x04: Flow determination start process 0x05: PMC patching process 0x06: Get the flash VSCC parameters 0x07: Set (program) the flash VSCC registers 0x08: Error reading/matching the VSCC table in the descriptor 0x09: Initialize EFFS (overlay and SDM memory management) 0x0A: Check to see if straps say ME DISABLED 0x0B: Timeout waiting for T34 0x0C: Check to see if effs say ME DISABLED 0x0D: Possibly handle BUP manufacturing override strap 0x0E: Check to see if effs say ME DISABLED 0x0F: Initialize PKTPM 0x10: Initialize MiniBLOB 0x11: Bringup in M3 0x12: Bringup in M0 0x13: Flow detection error 0x14: M3 clock switching 0x15: M3 clock switching error 0x16: M3 flash paging flow 0x17: M3 ICV recovery flow 0x18: M3 kernel load 0x19: M0 Host prep sequence 0x1A: M0 Host skip prep sequence 0x1B: ICC programming 0x1C: T34 missing - cannot program ICC 0x1D: FLEX SKU programiing 0x1E: TPM start (interface unisolation 0x1F: Waiting for DID BIOS message 0x20: Waiting for DID BIOS message failure 0x21: DID reported no errer 0x22: Enabling UMA 0x23: Enabling UMA error 0x24: Sending DID Ack to BIOS 0x25: Sending DID Ack to BIOS error 0x26: Switching clocks in M0 0x27: Switching clocks in M0 error 0x28: ME in temp disable 0x29: ME in temp disable - erorr 0x2A: ME in temp disable - exiting and UMA enabling 0x2B: ME IPK check 0x2C: ME IPK recreation 0x2D: ME IPK recreation error 0x2E: ME UMA validation for resume 0x2F: ME UMA validation for resume error 0x30: ME UMA validation for resume error, so IPK recreation 0x31: M0 PK VENOM start 0x32: M0 kernel load 0x33: PK Venom init phase 0x34: M0 PK VENOM shutdown 0x35: FIPS halt - BUP self-test error 0x36: FIPS halt - CRYPTO_DRV self-test error 0x37: FIPS halt - TLS self-test error: 0x38: FIPS halt - DT self-test error 0x39: FIPS halt - DT self-test error 0x3A: Error enabling memory acces range 0x3B: ME reset limit reached 0x3C: Two ME resets within short time detected, enter recovery 0x3D: Unknown halt reason detected, halt ME 0x3E: Validating GLUT and NFT manifest 0x3F: Reading kernel fixed data from NVAR 0x40: Reading ICC data 0x41: Zeroing out UMA 0x42: Full Fw sku running on Ignition HW sku 0x43: Error when deriving chipset keys 0x44: Bad BIOS, CPU DOA, CPU Missing 0x46: Failure in loading FTP 0x47: ME halted in BUP from Mfg ME reset 0x48: ME was reset because of MPR protection violation 0x49: BUP_T34_POLL_BEGIN 0x4A: BUP_T34_POLL_END 0x4B: BUP_HOBIT_SET 0x4C: BUP_POLL_CPURST_DEASSERT_BEGIN 0x4D: BUP_CPURST_DEASSERT_DONE 0x4E: BUP_DID_POLL_BEGIN 0x4F: BUP_DID_RECVD 0x50: BUP_ZERO_UMA_BEGIN 0x51: BUP_ZERO_UMA_DONE 0x52: BUP_DID_ACK_SENT 0x53: ICC requested a global reset after DID timeout 0x54: Perform ROSC clock frequency check 0x55: Clock check failed 0x56: CPU_RESET_DONE_ACK not received 0x57: FW build does not support the WW and/or Year specified in the fuses 0x58: ULV PCH check in progress 0x59: ULV PCH not paired with LV/ULV CPU 0x5A: VDM handshake failure 0x5B: FFS entry 0x5C: FFS exit 0x60: Error when getting a random number from TRNG 0x61: Find stack protection canary from NVAR or TRNG 0x62: VDM Get SID Message in progress 0x63: Wait for CPU to issue VLB authentication response For INF_PROG_CODE value of Kernel and Policy Module, values are as follows: 0x00: Entry into KERNEL Module 0x01: Entry into ThreadX Application Define 0x02: Exit ThreadX Application Define 0x03: Received S3 entry MSI from PMC 0x04: Received S4 entry MSI from PMC 0x05: Received S5 entry MSI from PMC 0x06: Received UPD entry MSI from PMC 0x07: Received PCR entry MSI from PMC 0x08: Received NPCR entry MSI from PMC 0x09: Received host wake MSI from PMC 0x0A: Received AC(-)DC switch 0x0B: Received DRAM Init Done 0x0C: VSCC Data not found for flash device 0x0D: VSCC Table is not valid 0x0E: Flash Partition Boundary in Chipset Descriptor is outside flash address space 0x0F: ME region cannot access the Chipset Descriptor Region 0x10: Required VSCC values for flash parts do not match 0x12: /**(State Info specified by the Exception Handler */ 0x13: /**(State Info specified by the Exception Handler */ 0x14: /**(State Info specified by the Exception Handler */ 0x15: /**(State Info specified by the Exception Handler */ 0x16: /**(State Info specified by the Exception Handler */ 0x17: /**(State Info specified by the Exception Handler */ 0x18: /**(State Info specified by the Exception Handler */ 0x19: /**(State Info specified by the Exception Handler */ 0x1A: /**(State Info specified by the Exception Handler */ 0x1B: /**(State Info specified by the Exception Handler */ For INF_PROG_CODE value of Host Communication, values are as follows: 0x00: Host communication established. Firmware is up and running.

Bit Range	Default & Access	Field Name (ID): Description
15:0	X RW	**FUNC_RSVD_15:** RESERVED BITS, writable

22.3.13 SEC_MEM_REQ—Offset 44h

SeC Firmware Memory Request. SeC FW uses this register in order to pass its main memory request to BIOS. Register acces control: FW=RW PMC=RO Host=RO

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MEM_REQ_VALID	MEM_REQ_INVALID	FUNC_RSVD_29_16														MEM_SIZE															

Bit Range	Default & Access	Field Name (ID): Description
31	X RW	**MEM_REQ_VALID:** 1: SeC is making a request for memory, the size of which is indciated by field MEM_SIZE. During early boot stages, BIOS must wait for either this bit to be set or the MEM_REQ_INVALID bit to be set before proceeding.
30	X RW	**MEM_REQ_INVALID:** 1: SeC is not making any request for memory, and MEM_SIZE field should be ignored. During early boot stages, BIOS must wait for either this bit to be set or the MEM_REQ_VALID bit to be set before proceeding.
29:16	X NA	**FUNC_RSVD_29_16:** The functionality of this field is currently reserved
15:0	X RW	**MEM_SIZE:** Memory size that SeC is expecting, in KB. Format is Little Endian (bit 0 least significant, bit 15 most significant).

22.3.14 SEC_FW_STS0—Offset 48h

SeC Firmware Status Register 0. SeC FW uses this register in order to report its status to host (e.g. BIOS). Register acces control: FW=RW PMC=RO Host=RO

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 48h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BIOS_MSG_ACK	ACK_DATA	FUNC_RSVD_24	SEC_RST_CNT	SEC_CURR_OPER_MODE	ERR_CODE	FW_UPD_IN_PROG	FW_BUP_LD_FLR	FW_INIT_COMP	SEC_CURR_OP_STATE	FPT_BAD	MANUF_MODE	SEC_CURR_WRK_STATE

Bit Range	Default & Access	Field Name (ID): Description
31:28	X RW	**BIOS_MSG_ACK:** DRAM Init Done ACK. 0x00: No ACK was written by SeC. 0x01: ACK was written by SeC.
27:25	X RW	**ACK_DATA:** DRAM Init Done ACK Data. This field contains an action which BIOS should take on receiving an ACK from SeC. 0x00: No DRAM Init Done ACK received. 0x01: Non-power cycle reset. 0x02: Power cycle reset. 0x03: Go to S3. 0x04: Go to S4. 0x05: Go to S5. 0x06: Perform Global Reset. 0x07: Continue to boot.
24	X RW	**FUNC_RSVD_24:** The functionality of this field is currently reserved
23:20	X RW	**SEC_RST_CNT:** Count of SeC Resets
19:16	X RW	**SEC_CURR_OPER_MODE:** The field indicates the firmware mode of operation during this boot cycle. The host must look at this field only after DRAM_INIT_DONE (DID) register based message unless the firmware is in ERR before sending the DID.The Operation Mode doesn't change at runtime. Possible values: 0: Normal. SeC is running in normal mode. 1: Reserved. 2: Debug mode. SeC firmware enters this operation mode when SeC firmware FLASH variable TBD is configured in FLASH to 1. Firmware stays in this mode until the SeC firmware FLASH variable TBD is set to 0. 3: Soft temporary disable. SeC firmware enters this operation mode when BIOS sends the Temporary Disable message to firmware. Firmware stays in this mode until BIOS sends a follow-up message to get SeC out of this mode. Entering this mode is not supported when the system is provisioned with Intel AT firmware. 4: SECOVR_JMPR: SeC firmware enters this operation mode when HDA_SDO asserts high. Asserting the HDA_SDO high on the rising edge of PWROK will also disable SeC and SeC applications. 5: SECOVR_HECI_MSG: SeC firmware enters this operation mode during the firmware image re-flash in the factory environments. BIOS sends the flash protection override message (HMRFPO ENABLE HECI command) and causes a global reset then SeC firmware stays in this state similar to 'Soft Temporary Disable'. Before sending End of Post message (at late POST timeframe), BIOS needs to send a HMRFPO DISABLE command if SECOVR_HECI_MSG is set. In the same boot, the user can flash an image and reset (global reset or G3- exit) the system that will cause firmware to boot with a normal mode.
15:12	X RW	**ERR_CODE:** Set to a nonzero value if the firmware has encountered a fatal error. The firmware has stopped normal operation. Encoding as follows: 0: No error. Firmware is operational in current state. 1: Uncategorized Failure. SeC firmware has experienced an uncategorized error and has disabled itself. Further details of the failure can be found in field FW_STS1.EXT_STAT_DAT. This state can only be exited by powering down or resetting the machine. 2: Reserved. 3: Image Failure. SeC firmware stored in the system flash is not valid. If supported by the platform, the host should program a full firmware image into SeC flash region through the SPI controller. After completion of the SeC flash region update, the host should generate a full system reset the platform (global reset). 4: Debug Failure. Set when more data is available to the firmware on the cause of the failure. Please refer to field FW_STS1.EXT_STAT_DAT_CURR_STATE for more details. 5: Internal ROM Error. 6: Invalid fuse configuration. 7: Failure to access SPI FLASH.
11	X RW	**FW_UPD_IN_PROG:** This bit is set when data migration is required during the Firmware-update process.

Bit Range	Default & Access	Field Name (ID): Description
10	X RW	**FW_BUP_LD_FLR:** This bit is set when firmware is not able to load BRINGUP from the fault tolerant (FT) code. When this bit set, it may or may not have the error code shown in field ERR_CODE. The reason is because the firmware can load BRINGUP from the non fault tolerant (NFT) code.
9	X RW	**FW_INIT_COMP:** When this bit is clear, firmware is still in loading process and has not made it to final steady state yet. When firmware has fully entered a stable state, this bit is set to 1 and 'Current Working State' field of this register provides the steady state of SeC.
8:6	000b RW	**SEC_CURR_OP_STATE:** This field describes the state in which SeC is currently functioning in at this moment. It's the combination of SeC power state and UMA. The field is set only upon entering the true hardware state. Values: 000b: Preboot (default) 001b: M0 with UMA. 010b: MOff. 011b: Reserved. 100b: Reserved. 101b: Reserved. 110b: Bringup. 111b: M0 without UMA but with error. If there is no memory in the system, or upon identifying an error in UMA initialization, the SeC firmware will get into this operation state.
5	X RW	**FPT_BAD:** This bit is set when the firmware discovers a bad checksum of Flash Partition Table (FPT). When this bit set, it may or may not have the error code shown in field ERR_CODE. The system can get this bit clear by flashing the proper firmware image again.
4	X RW	**MANUF_MODE:** When this bit is set, the platform is still in Manufacturing mode. Host can use this bit to inform user that the platform is NOT ready for production yet. This bit is set as long as SeC Manufacturing Mode Done bit is set to 0 or SPI flash descriptor region is not locked. For shipping machine, this bit has to be to 0.
3:0	X RW	**SEC_CURR_WRK_STATE:** This field describes the current working state of the SeC firmware. Further information about the progress within the Current Working State can be found in field SEC_FW_STS1.EXT_STS_DAT. In spoken language, the 'Current Working State' indicates what firmware is doing at this moment. Encoding is as follows: 0: Reset. SeC firmware is in a reset state. 1: Initializing. SeC firmware is initializing, the final functional state is NOT known at this time. 2: Recovery: SeC firmware is recovering from an image update failure. Upon completion of this state, SeC firmware will enter the Initializing State. The firmware will stay in recovery state until a new firmware update is run. 3: Reserved. 4: Reserved. 5: Normal. SeC firmware is operating in normal state. 6: Platform Disable Wait. SeC firmware enters this state when it pauses itself with AT fuses set to halt platform after 30 minutes wait. 7: OP State Transition. SeC firmware sets this state before starting a transition to a new operation state. 8: Reserved.

22.3.15 PCI_CONF_SEC_TO_HOST_3_7[0-4] (PCI_CONF_SEC_TO_HOST_3_7_REGS[0-4])—Offset 4Ch, Count 5, Stride 4h

PCI Configuration register - SeC to Host 3-7. The functionality of this register is currently reserved. Register acces control: FW=RW PMC=RO Host=RO

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**Offset[0-4]:** [B:0, D:26, F:0] + 4Ch + [0-4]*4h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
PCI_CONF_SEC_TO_HOST								

Bit Range	Default & Access	Field Name (ID): Description
31:0	X RW	**PCI_CONF_SEC_TO_HOST:** The functionality of this field is currently reserved

22.3.16 DID_MSG—Offset 60h

DRAM Init Done Message. BIOS uses this register in order to pass a message to SeC about the memory that it has reserved for SEC. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 60h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
DONE	STATUS	FUNC_RSVD_23_0						

Bit Range	Default & Access	Field Name (ID): Description
31:28	X RW	**DONE:** 0x00: DRAM Init not done. 0x01: DRAM Initialization Done. If STATUS field is success, this means that SATT1 register is set for SeC memory paging operation. Note that BIOS must not provide a DRAM Init Done message before setting up SATT1.
27:24	X RW	**STATUS:** 0x00: Success. 0x01: No memory in channels. 0x02: Memory Init Error.
23:0	X NA	**FUNC_RSVD_23_0:** RESERVED BITS

22.3.17 PCI_CONF_HOST_TO_SEC[0-6] (PCI_CONF_HOST_TO_SEC_1_7_REGS[0-6])—Offset 64h, Count 7, Stride 4h

PCI Configuration register - Host to SEC 1-7. The functionality of this register is currently reserved. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset[0-6]: [B:0, D:26, F:0] + 64h + [0-6]*4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field (31:0): PCI_CONF_HOST_TO_SEC_1_7

Bit Range	Default & Access	Field Name (ID): Description
31:0	X RW	**PCI_CONF_HOST_TO_SEC_1_7:** The functionality of this field is currently reserved

22.3.18 POWERCAPID—Offset 80h

Power Capability ID. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 80h

Default: 4803A001h

31			28				24				20				16				12				8				4				0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: PMESUPPORT_D3COLD (31), PMESUPPORT_D3HOT (30), PMESUPPORT_D2 (29), PMESUPPORT_D1 (28), PMESUPPORT_D0 (27), RSVD_26_19 (26:19), VERSION (18:16), NXTCAP_MSI (15:8), POWER_CAP (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**PMESUPPORT_D3COLD:** Power Capabilities Identification Bits 30,27 RW1
30	1b RW/O	**PMESUPPORT_D3HOT:** Power Capabilities Identification Bits 30,27 RW1
29	0b RO	**PMESUPPORT_D2:** Power Capabilities Identification Bits 30,27 RW1
28	0b RO	**PMESUPPORT_D1:** Power Capabilities Identification Bits 30,27 RW1
27	1b RW/O	**PMESUPPORT_D0:** Power Capabilities Identification Bits 30,27 RW1
26:19	0b NA	**RESERVED (RSVD_26_19):** RESERVED BITS
18:16	011b RO	**VERSION:** Power Capabilities Identification Bits 30,27 RW1
15:8	A0h RW/O	**NXTCAP_MSI:** A pointer to MSI capability
7:0	01h RO	**POWER_CAP:** Capability ID: 1 for power management

22.3.19 PMECTRLSTATUS—Offset 84h

PME Control and Status. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 84h

Default: 00000008h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 0 0 0

RSVD_31_16
PME_Status
RSVD_14_9
PME_En
RSVD_7_4
No_Soft_Reset
RSVD_2
POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b NA	**RESERVED (RSVD_31_16):** RESERVED BITS
15	0b RW/C	**PME_Status:** Capability ID: 1 for power management
14:9	0b NA	**RESERVED (RSVD_14_9):** RESERVED BITS
8	0b RW	**PME_En:** PME enable
7:4	0b NA	**RESERVED (RSVD_7_4):** RESERVED BITS

Bit Range	Default & Access	Field Name (ID): Description
3	1b RO	**No_Soft_Reset:** PME Control and Status
2	0b NA	**RESERVED (RSVD_2):** RESERVED BITS
1:0	X RW	**POWERSTATE:** SeC Power state - TBD

22.3.20 CLK_GATE_DIS—Offset 88h

Clock Gating Disable. Register acces control: FW=RW PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 88h

Default: 000000FFh

31–28	27–24	23–20	19–16	15–12	11–8	7	6	5	4	3	2	1	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1	1	1	1	1	1	1	1
RSVD_31_8						NFC_CG_DIS	SAP_CLKIDLE_DIS	SAP_IP_CG_DIS	SAP_CG_DIS	PRIM_XSM_CLKREQ_DIS	PRIM_CLKREQ_DIS	PRIM_CG_DIS	SB_CG_DIS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b NA	**RESERVED (RSVD_31_8):** RESERVED BITS
7	1b RW	**NFC_CG_DIS:** I2C clock gating disable
6	1b RW	**SAP_CLKIDLE_DIS:** SAP clock idle disable
5	1b RO	**SAP_IP_CG_DIS:** Functional IP clock gating disable
4	1b RW	**SAP_CG_DIS:** Functional SEC clock gating disable (Bridge and IP)
3	1b RW	**PRIM_XSM_CLKREQ_DIS:** Primary XSM clock-request disable
2	1b RW	**PRIM_CLKREQ_DIS:** IOSF Primary clock request disable
1	1b RW	**PRIM_CG_DIS:** IOSF Primary clock gating disable
0	1b RW	**SB_CG_DIS:** IOSF Sideband Bridge clock gating disable

22.3.21 TPM_ICR—Offset 8Ch

TPM Interrupt Cause Register. Acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + 8Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

TPM_REQ

Bit Range	Default & Access	Field Name (ID): Description
31:0	X RW	**TPM_REQ:** Host writes this bit to indicate a TPM message is ready for fTPM handling. A write to this register will trigger an interrupt to the SEC, in ICR 30.

22.3.22 MSICAP—Offset A0h

MSI Capability. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + A0h

Default: 00000005h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 1 0 1

RSVD_31_25 | PER_VEC_CAP | BIT_ADDR_CAP | MME | RSVD_19_17 | MSI_ENABLE | RSVD_15_8 | MSI_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b NA	**RESERVED (RSVD_31_25):** RESERVED BITS
24	X RO	**PER_VEC_CAP:** Per vector masking not supported.
23	X RO	**BIT_ADDR_CAP:** C64: 32-bit capable only
22:20	X RW	**MME:** MME: This field is RW for software compatibility, but only a single message is ever generated
19:17	0b NA	**RESERVED (RSVD_19_17):** RESERVED BITS , MMC: This device is only single message capable

Bit Range	Default & Access	Field Name (ID): Description
16	X RW	**MSI_ENABLE:** MSIE: If set, MSI is enabled and traditional interrupts are not used to generate interrupts. COMMANDSTATUS.BUS_MSTR_EN must be set for an MSI to be generated. When 0, blocks the sending of a MSI interrupt and permits the sending of a Message bus interrupt. (The interrupt status is not blocked from being reflected in the COMMANDSTATUS.INTR_STT bit.) When 1, permits sending of a MSI interrupt and blocks the sending of a Message bus interrupt. (The interrupt status is not blocked from being reflected in the COMMANDSTATUS. INTR_STT bit.)
15:8	0b RW	**RESERVED (RSVD_15_8):** Indicates this is the last item in the list
7:0	05h RO	**MSI_CAP:** CAPID: Indicates an MSI capability

22.3.23 MSIADDR—Offset A4h

MSI Address. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:26, F:0] + A4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSGADDRMSI																														RSVD_1_0	

Bit Range	Default & Access	Field Name (ID): Description
31:2	X RW	**MSGADDRMSI:** MA: Lower 32-bits of the system specified message address, always DW aligned. When the SEC issues an MSI interrupt as a MEMWR on the IOSF, the memory address corresponds to the value of this field
1:0	0b NA	**RESERVED (RSVD_1_0):** RESERVED BITS

22.3.24 MSIDATA—Offset A8h

MSI Data. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:26, F:0] + A8h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Reserved_31_16 | MSGDATAMSI

Bit Range	Default & Access	Field Name (ID): Description
31:16	X NA	**RESERVED (Reserved_31_16):** RESERVED BITS
15:0	X RW	**MSGDATAMSI:** MA: Lower 32-bits of the system specified message data, always DW aligned. When the SEC issues an MSI interrupt as a MEMWR on the IOSF, the memory address corresponds to the value of this field

22.3.25 IADBGCTRL—Offset B0h

IA Debug Control. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:26, F:0] + B0h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

DBG_STS | IADBGCTRL_LOCK | RSVD_29_2 | EXPOSE_SOCID | CPU_PUBLIC_DBG_EN

Bit Range	Default & Access	Field Name (ID): Description
31	X RO	**DBG_STS:** DBG_STS. This bit allows a user to be informed that their system is (or is at risk of) being debugged. It is up to the OEM/OS to act on this bit being set and find a way to expose it to the user. CLTAP will send a signal to SEC indicating that debug of the SOC and/or access to the CPUTAP is possible. This will be (allow_cputap_access | dfx_security_risk). Note: DBG_STS will be set in all Opt-In cases including pre-production and IDLM.
30	X RW/1L	**IADBGCTRL_LOCK:** Lock. If set, writes to bits 29:0 are dropped.
29:2	0b NA	**RESERVED (RSVD_29_2):** RESERVED BITS
1	X RW	**EXPOSE_SOCID:** Expose_SOCID. If set, software is requesting that this parts unique ID will be visible in a public SOCTAP register to JTAG (on-board or EXI). It is never exposed to IA code. This bit is locked (writes ignored) if the LOCK bit is set. This bit will written but ignored if SEC OEM-M[HONOR_IADBGCTRL]==0.

Bit Range	Default & Access	Field Name (ID): Description
0	X RW	**CPU_PUBLIC_DBG_EN:** CPUPublicDBG_EN. If set, software is requesting access be granted to the CPUTAP's public and non-protected functions. This bit is locked (writes ignored) if the LOCK bit is set. This bit will be written but ignored if SEC OEM-M[HONOR_IADBGCTRL]==0.

22.3.26 CPU_BIOS_ENV_PROTECT—Offset B4h

CPU BIO Environment Protection. Register acces control: FW=RW PMC=RO Host=RO Note: This register does not support byte- or word- granularity write. All 32 bits of this register should be written at once. To change only part of the register, a read-modify-write process should be used on all 32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:26, F:0] + B4h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD_31_4 | CPU_BIOS_ENV_ATTACKED | BIOS_RDY_FOR_EVENT | CPU_DIS_BSP_INIT | CPU_PROTECT_BIOS_ENV

Bit Range	Default & Access	Field Name (ID): Description
31:4	0b NA	**RESERVED (RSVD_31_4):** RESERVED BITS
3	X RW	**CPU_BIOS_ENV_ATTACKED:** CPU_BIOS_ENV_ATTACKED
2	X RW	**BIOS_RDY_FOR_EVENT:** BIOS_RDY_FOR_EVENT
1	X RW	**CPU_DIS_BSP_INIT:** CPU_DIS_BSP_INIT
0	X RW	**CPU_PROTECT_BIOS_ENV:** CPU_PROTECT_BIOS_ENV

22.3.27 SATT_BIOS_CTRL—Offset C0h

SEC Address Translation Table Entry no. 2 control register, used by the BIOS to configure the paging IMR related entry. Register acces control: FW=RO PMC=RO Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:26, F:0] + C0h

Default: 00001008h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	1 0 0 0

Fields: RSVD_31_13 (31:13), BRG_HOST_EN (12), BRG_BA_MSB (11:8), RSVD_7_4 (7:4), TARGET (3:1), VALID (0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b NA	**RESERVED (RSVD_31_13):** RESERVED BITS
12	1b RO	**BRG_HOST_EN:** Indicates whether or not the entry's BRG_BA is configurable by host CPU. Hard coded to 1b, to ensure host CPU only access
11:8	X RW	**BRG_BA_MSB:** 4 MS bits to be used for IOSF address, to be concatenated with the entry's BRG_BA_LSB[31:0]. This field is locked when SATT1_CTRL.ENTRY_VLD is set. Locked by entry_valid bit.
7:4	0b NA	**RESERVED (RSVD_7_4):** RESERVED BITS
3:1	100b RO	**TARGET:** The target to which the SAP transaction will be redirected: 000 - Bridge memory space 001 - Bridge PCI configuration space 010 - IOSF sideband (General) 011 - SPI via IOSF Sideband 100 - DDR via IOSF Primary Hard coded to '100' to let host configure paging IMR
0	X RW	**VALID:** Entry valid bit. This bit can be set only once (by BIOS). Once it's set to '1', it cannot be cleared, and all SAAT1 entry register fields are locked. Entry hit condition is: ENTRY_VLD and SAP_BA (= SAPAddr[+SAPSize] (SAP_BA + SAP_SIZE

22.3.28 SATT_BIOS_BA—Offset C4h

SEC address translation table entry 1 bridge base address. Register acces control: FW=RO PMC=RO Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + C4h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Fields: BRG_BA (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	X RW	**BRG_BA:** The bridge base address to be used for address translation using current SATT entry. This field is locked when SATT1_CTRL.ENTRY_VLD is set. Address calculation: FinalAddr = SAPAddr - SAP_BA + BRG_BA. Locked by entry_valid bit in SATT1_CTRL register.

22.3.29 SATT_BIOS_SIZE—Offset C8h

SEC Address Translation Table Entry no. 2 SAP Address space Size register, used by the BIOS to configure the paging IMR related entry. Register acces control: FW=RO PMC=RO Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + C8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD_31_25							SAP_SIZE																								

Bit Range	Default & Access	Field Name (ID): Description
31:25	0b NA	**RESERVED (RSVD_31_25):** RESERVED BITS
24:0	X RW	**SAP_SIZE:** The SAP-address space size that defines the address space to be translated using current SATT entry. This field is locked when SATT1_CTRL.ENTRY_VLD is set. Entry hit condition is: ENTRY_VLD and SAP_BA (= SAPAddr[+SAPSize] (SAP_BA + SAP_SIZE Locked by entry_valid bit in SATT1_CTRL register

22.3.30 SATT_TPM_CTRL (SATT_TPM_CTRL)—Offset D0h

SEC Address Translation Table Entry no. 4 control register, used by the BIOS to configure the paging IMR related entry. Register acces control: FW=RO PMC=RO Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + D0h

Default: 00001008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
RSVD_31_14																		SEC_TPM_DISABLED	BRG_HOST_EN	BRG_BA_MSB				RSVD_7_4				TARGET			VALID

Bit Range	Default & Access	Field Name (ID): Description
31:14	0b NA	**RESERVED (RSVD_31_14):** RESERVED BITS

Bit Range	Default & Access	Field Name (ID): Description
13	X RO	**SEC_TPM_DISABLED:** Indicates to the BIOS that the fTPM functionality is disabled (either by fuse or by fw).
12	1b RO	**BRG_HOST_EN:** Indicates whether or not the entry's BRG_BA is configurable by host CPU. Hard coded to 1b, to ensure host CPU only access
11:8	X RW	**BRG_BA_MSB:** 4 MS bits to be used for IOSF address, to be concatenated with the entry's BRG_BA_LSB[31:0] Locked by entry_valid bit.
7:4	0b NA	**RESERVED (RSVD_7_4):** RESERVED BITS
3:1	100b RO	**TARGET:** The target to which the SAP transaction will be redirected: 000 - Bridge memory space 001 - Bridge PCI configuration space 010 - IOSF sideband (General) 011 - SPI via IOSF Sideband 100 - DDR via IOSF Primary Hard coded to '100' to let host configure TPM
0	X RW	**VALID:** Entry valid bit. Entry hit condition is: ENTRY_VLD and SAP_BA (= SAPAddr[+SAPSize] (SAP_BA + SAP_SIZE 1'b0: SATT TPM Entry is disabled. 1'b1: SATT TPM Entry is enabled. Note: when TPM disable fuse is '1', this bit is hard coded to '0'. Asserting this bit will lock the TPM SATT entries. (CTRL, BA and SIZE).

22.3.31 SATT_TPM_BA—Offset D4h

SEC Address Translation Table Entry no. 4 SAP Address space Size register, used by the BIOS to configure the paging IMR related entry. Register acces control: FW=RO PMC=RO Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + D4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BRG_BA

Bit Range	Default & Access	Field Name (ID): Description
31:0	X RW	**BRG_BA:** The bridge base address to be used for address translation using current SATT entry. Address calculation: FinalAddr = SAPAddr - SAP_BA + BRG_BA Locked by entry_valid bit in SATT1_CTRL register..

22.3.32 SATT_TPM_SIZE—Offset D8h

SEC Address Translation Table Entry no. 4 SAP Address space Size register, used by the BIOS to configure the paging IMR related entry. Register acces control: FW=RO PMC=RO Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + D8h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD_31_13																			SAP_SIZE	RSVD_11_0											

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b NA	**RESERVED (RSVD_31_13):** RESERVED BITS
12	X RW	**SAP_SIZE:** The SAP-address space size that defines the address space to be translated using current SATT entry. Entry hit condition is:
11:0	0b NA	**RESERVED (RSVD_11_0):** RESERVED BITS

22.3.33 URRE—Offset F0h

URRE, For unsupported Request Handling. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + F0h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD_31_2																														URRE_1	URD

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b NA	**RESERVED (RSVD_31_2):** RESERVED BITS
1	X RW	**URRE_1:** DOSERR enable
0	X RW/C	**URD:** DOSERR status. Write 1 to clear.

22.3.34 MANID—Offset F8h

SEC address Manufacturing ID. Register acces control: FW=RO PMC=RW Host=RW

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:26, F:0] + F8h

Default: 00000000h

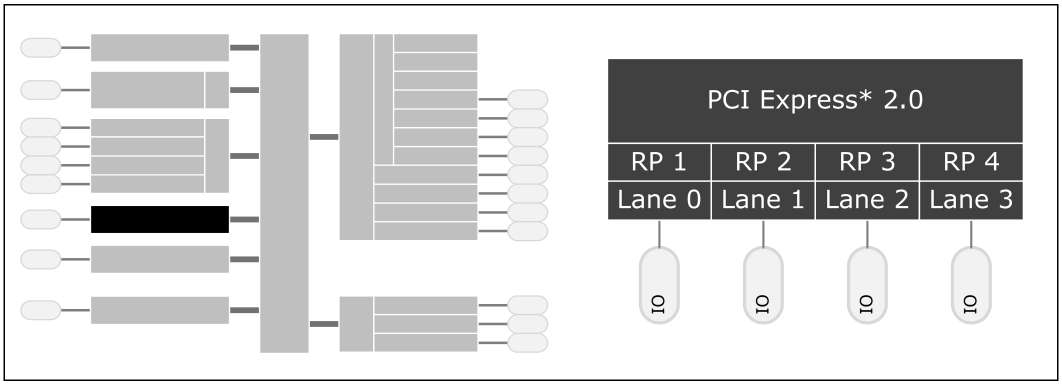
31	28	24	20	16	12	8	4	0

RSVD_31_28	DOT_PORT	MAN_ID_23_16	MAN_ID_15_8	MAN_ID_7_0
0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit Range	Default & Access	Field Name (ID): Description
31:28	X RO	**RESERVED (RSVD_31_28):** RESERVED BITS
27:24	X RO	**DOT_PORT:** Dot Portion of Process: obtained from SETID message sent by PMC
23:16	X RO	**MAN_ID_23_16:** Manufacturing Stepping ID (MSID): obtained from SETID message sent by PMC
15:8	X RO	**MAN_ID_15_8:** Manufacturing ID (MID): obtained from SETID message sent by PMC
7:0	X RO	**MAN_ID_7_0:** Process Portion of Process ID: obtained from SETID message sent by PMC

23 PCI Express* 2.0

There are four lanes and up to four PCI Express root ports, each supporting the *PCI Express* Base Specification*, Rev. 2.0 at a maximum 5 GT/s signaling rate. The root ports can be configured to support a diverse set of lane assignments.



23.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

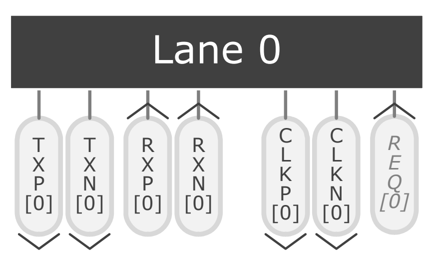
- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Note: PMC_WAKE_PCIE[3:0]# are not listed, but can be used by PCI Express* devices. Please see Section 30, "PCU – Power Management Controller (PMC)" on page 4344 for details.

Table 240. Signals

Signal Name	Direction Plat. Power	Description
PCIE_TXP[3:0] **PCIE_TXN[3:0]**	O PCIESATA	**PCI Express* Transmit** PCI Express* Ports 3:0 transmit pair (P and N) signals. Each pair makes up the transmit half of a lane.
PCIE_RXP[3:0] **PCIE_RXN[3:0]**	I PCIESATA	**PCI Express* Receive:** PCI Express* Ports 3:0 receive pair (P and N) signals. Each pair makes up the receive half of lane.
PCIE_CLKP[3:0] **PCIE_CLKN[3:0]**	O V1P0S	**PCI Express* Output Clock** 100-MHz differential clock signals. These are not owned by the PCI Express* controller, but are platform clocks found in the Integrated Clock.
PCIE_CLKREQ[3:0]#	I V1P8S	**PCI Express* Clock Request** Used for devices that need to request one of the four output clocks. Each clock request maps to the matching clock output (e.g., PCI_CLKREQ[0] maps to PCIE_CLKP/N[0]). These are not owned by the PCI Express* controller, but are platform clocks found in the Integrated Clock. *These signals are muxed and may be used by other functions.*
PCIE_RCOMP_P **PCIE_RCOMP_N**	I/O	These pins are used to connect the external resistors used for Rcomp. Please contact your Intel representative for details.

Figure 112.PCIe* 2.0 Lane 0 Signal Example



23.2 Features

- Conforms to *PCI Express* Base Specification*, Rev. 2.0
- 5.0 or 2.5 GT/s operation per root port
- Virtual Channel support for VC0
- x1, x2 and x4 link widths (auto negotiated)
- Flexible Root Port (1-4) configuration options
    — (4) x1's

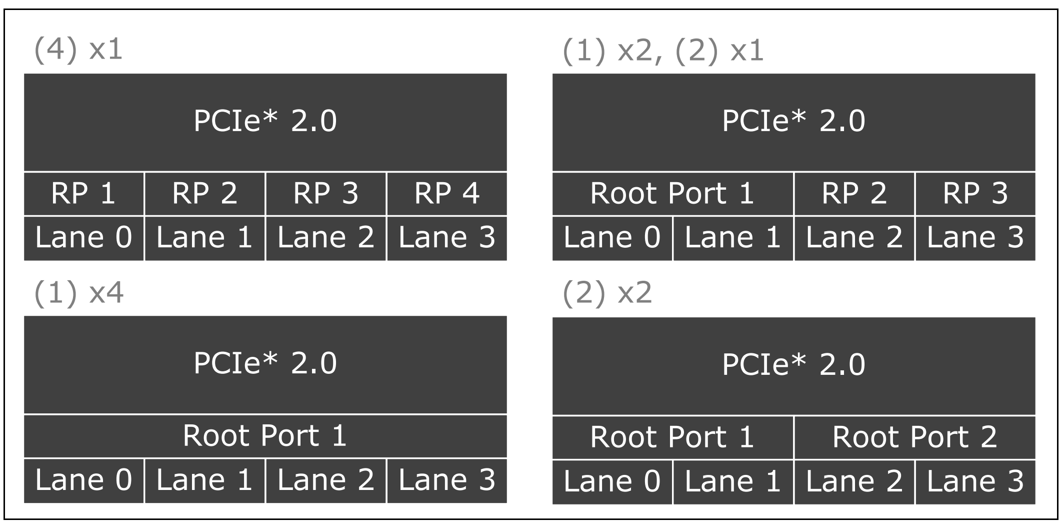
— (2) x2's
— (1) x2 plus (2) x1's
— (1) x4

- Interrupts and Events
  — Legacy (INTx) and MSI Interrupts
  — General Purpose Events
  — Express Card Hot Plug Events
  — System Error Events
- Power Management
  — Link State support for L0s, L1 and L2
  — Powered down in ACPI S3 state - L3

23.2.1 Root Port Configurations

Depending on SKU, there are up to four possible lane assignments for root ports 1-4.

Figure 113. Root Port Configuration Options



Root port configurations are set by SoftStraps stored in SPI flash, and the default option is "(4) x1". Links for each root port will train automatically to the maximum possible for each port.

Note: x2 link widths are not common. Most devices will only train to x1 or x4.

Note: PCI functions in PCI configuration space are disabled for root ports not available.

23.2.2 Interrupts and Events

A root port is capable of handling interrupts and events from an end point device. A root port can also generate its own interrupts for some events, including power management and hot plug events, but also including error events.

There are two interrupt types a root port will receive from an end point device: INTx (legacy), and MSI. MSI's are automatically passed upstream by the root port, just as other memory writes would be. INTx messages are delivered to the Legacy block's interrupt router/controller by the root port.

Events and interrupts that are handled by the root port are shown with the possible interrupts they can deliver to the interrupt decoder/router.

Table 241. Possible Interrupts Generated From Events/Packets

Packet/Event	Type	INTx	MSI	SERR	SCI	SMI	GPE
INTx	Packet	X	X				
PM_PME	Packet	X	X				
Power Management (PM)	Event	X	X		X	X	
Hot Plug (HP)	Event	X	X		X	X	
ERR_CORR	Packet			X			
ERR_NONFATAL	Packet			X			
ERR_FATAL	Packet			X			
Internal Error	Event			X			
VDM	Packet						X

Note: Table 241 lists the possible interrupts and events generated based on Packets received, or events generated in the root port. Configuration needed by software to enable the different interrupts as applicable.

When INTx interrupts are received by an end point, they are mapped to the following interrupts and sent to the interrupt decoder/router in the iLB:

Table 242. Interrupt Generated for INT[A-D] Interrupts

	INTA	INTB	INTC	INTD
Root Port 1	INTA#	INTB#	INTC#	INTD#
Root Port 2	INTD#	INTA#	INTB#	INTC#
Root Port 3	INTC#	INTD#	INTA#	INTB#
Root Port 4	INTB#	INTC#	INTD#	INTA#

Note: Interrupts generated from events within the root port are not swizzled.

23.2.2.1 Express Card Hot Plug Events

Express Card Hot Plug is available based on Presence Detection for each root port.

Note: A full Hot Plug Controller is not implemented.

Presence detection occurs when a PCI Express* device is plugged in and power is supplied. The physical layer will detect the presence of the device, and the root port will set the SLSTS.PDS and SLSTS.PDC bits.

When a device is removed and detected by the physical layer, the root port will clear the SLSTS.PDS bit, and set the SLSTS.PDC bit.

Interrupts can be generated by the root port when a hot plug event occurs. A hot plug event is defined as the transition of the SLSTS.PDC bit from 0 to 1. Software can set the SLCTL.PDE and SLTCTL.HPE bits to allow hot plug events to generate an interrupt.

If SLCTL.PDE and SLTCTL.HPE are both set, and STSTS.PDC transitions from 0 to 1, an interrupt will be generated.

23.2.2.2 System Error (SERR)

System Error events are support by both internal and external sources. See the PCI Express* Base Specification, Rev. 2.0 for details.

23.2.3 Power Management

Each root port's link supports L0s, L1, and L2/3 link states per PCI Express* Base Specification, Rev. 2.0. L2/3 is entered on entry to S3.

23.3 References

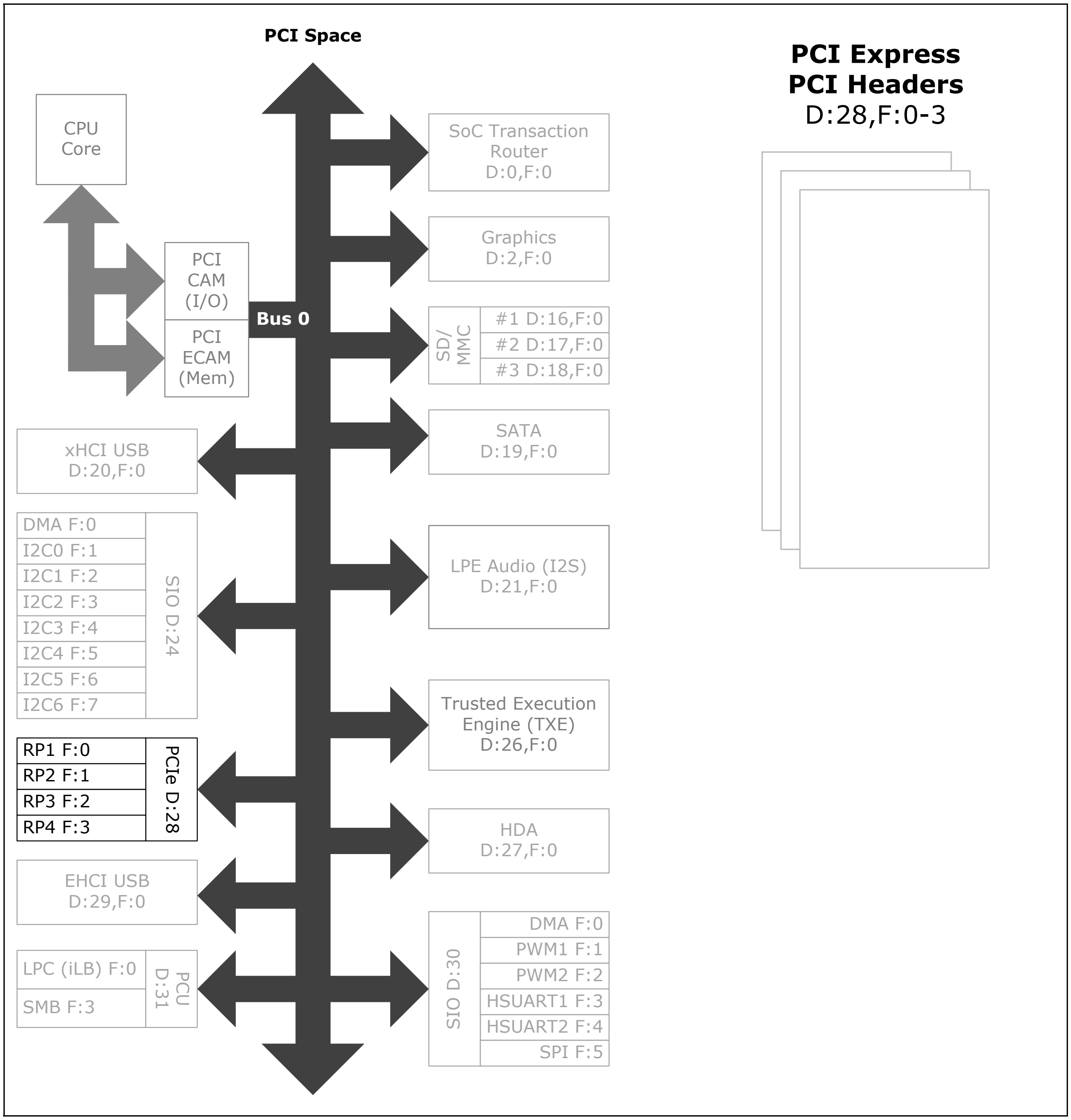
PCI Express Base Specification*, Rev. 2.0

23.4 Register Map

Each root port supports its own extended PCI bridge header in PCI configuration space. These headers are located on PCI bus 0, device 28, functions 0-3 as shown below. There are no other registers implemented by the root ports or their controller.

See Chapters Chapter 3, "Register Access Methods" and Chapter 4, "Mapping Address Spaces" for additional information.

Figure 114. PCI Express Register Map



23.5 PCI Configuration Registers

Registers listed are for function 0 (root port 1). All other root ports contain the same registers. Differences for other root ports (functions 1-3) will be noted in individual registers.

23.6 PCI Express* PCI Configuration Registers

Table 243. Summary of PCI Express* PCI Configuration Registers—0/28/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Identifiers (ID)—Offset 0h" on page 3198	00008086h
4h	4	"Device Command; Primary Status (CMD_PSTS)—Offset 4h" on page 3199	00100000h
8h	4	"Revision ID;Class Code (RID_CC)—Offset 8h" on page 3200	06040000h
Ch	4	"Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch" on page 3201	00810000h
18h	4	"Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h" on page 3201	00000000h
1Ch	4	"I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch" on page 3202	00000000h
20h	4	"Memory Base and Limit (MBL)—Offset 20h" on page 3203	00000000h
24h	4	"Prefetchable Memory Base and Limit (PMBL)—Offset 24h" on page 3204	00010001h
28h	4	"Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h" on page 3204	00000000h
2Ch	4	"Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch" on page 3205	00000000h
34h	4	"Capabilities List Pointer (CAPP)—Offset 34h" on page 3205	00000040h
3Ch	4	"Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch" on page 3206	00000000h
40h	4	"Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h" on page 3207	00428010h
44h	4	"Device Capabilities (DCAP)—Offset 44h" on page 3208	00008000h
48h	4	"Device Control; Device Status (DCTL_DSTS)—Offset 48h" on page 3209	00100000h
4Ch	4	"Link Capabilities (LCAP)—Offset 4Ch" on page 3210	00310C02h
50h	4	"Link Control; Link Status (LCTL_LSTS)—Offset 50h" on page 3211	00010000h
54h	4	"Slot Capabilities (SLCAP)—Offset 54h" on page 3213	00040060h
58h	4	"Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h" on page 3214	00000000h
5Ch	4	"Root Control (RCTL)—Offset 5Ch" on page 3215	00000000h
60h	4	"Root Status (RSTS)—Offset 60h" on page 3216	00000000h
64h	4	"Device Capabilities 2 (DCAP2)—Offset 64h" on page 3217	00080816h
68h	4	"Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h" on page 3217	00000000h
6Ch	4	"Link Capabilities 2 (LCAP2)—Offset 6Ch" on page 3218	00000000h
70h	4	"Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h" on page 3219	00000000h
74h	4	"Slot Capabilities 2 (SLCAP2)—Offset 74h" on page 3220	00000000h
78h	4	"Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h" on page 3221	00000000h
80h	4	"Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h" on page 3221	00009005h
84h	4	"Message Signaled Interrupt Message Address (MA)—Offset 84h" on page 3222	00000000h
88h	4	"Message Signaled Interrupt Message Data (MD)—Offset 88h" on page 3222	00000000h
90h	4	"Subsystem Vendor Capability (SVCAP)—Offset 90h" on page 3223	0000A00Dh
94h	4	"Subsystem Vendor IDs (SVID)—Offset 94h" on page 3223	00000000h
A0h	4	"Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h" on page 3224	C8030001h
A4h	4	"PCI Power Management Control And Status (PMCS)—Offset A4h" on page 3225	00000000h

Table 243. Summary of PCI Express* PCI Configuration Registers—0/28/0 (Continued)

Offset	Size	Register ID—Description	Default Value
F8h	4	"Manufacturer's ID (MANID)—Offset F8h" on page 3226	00000F00h
100h	4	"Advanced Error Reporting Capability Header (AECH)—Offset 100h" on page 3226	00000000h
104h	4	"Uncorrectable Error Status (UES)—Offset 104h" on page 3227	00000000h
108h	4	"Uncorrectable Error Mask (UEM)—Offset 108h" on page 3228	00000000h
10Ch	4	"Uncorrectable Error Severity (UEV)—Offset 10Ch" on page 3229	00060011h
110h	4	"Correctable Error Status (CES)—Offset 110h" on page 3230	00000000h
114h	4	"Correctable Error Mask (CEM)—Offset 114h" on page 3231	00002000h
118h	4	"Advanced Error Capabilities and Control (AECC)—Offset 118h" on page 3232	00000000h
11Ch	4	"Header Log DW1 (HL_DW1)—Offset 11Ch" on page 3232	00000000h
120h	4	"Header Log DW2 (HL_DW2)—Offset 120h" on page 3233	00000000h
124h	4	"Header Log DW3 (HL_DW3)—Offset 124h" on page 3233	00000000h
128h	4	"Header Log DW4 (HL_DW4)—Offset 128h" on page 3234	00000000h
12Ch	4	"Root Error Command (REC)—Offset 12Ch" on page 3234	00000000h
130h	4	"Root Error Status (RES)—Offset 130h" on page 3235	00000000h
134h	4	"Error Source Identification (ESID)—Offset 134h" on page 3235	00000000h
328h	4	"PCI Express Status 1 (PCIESTS1)—Offset 328h" on page 3236	00000000h
32Ch	4	"PCI Express Status 2 (PCIESTS2)—Offset 32Ch" on page 3237	00000000h
330h	4	"PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h" on page 3238	28000016h
334h	4	"PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h" on page 3239	4ABCB5BCh

23.6.1 Identifiers (ID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ID: [B:0, D:28, F:0] + 0h

Power Well: Core

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DID																VID															

Bit Range	Default & Access	Description
31:16	0000h RO/V	**Device Identification (DID):** The value of this ID is product specific.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

23.6.2 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

CMD_PSTS: [B:0, D:28, F:0] + 4h

Power Well: Core

Default: 00100000h

Bits	31	30	29	28	27	26:25	24	23	22	21	20	19	18:16	15:11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0 0	0	0	0	0	1	0	0 0 0	0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0
Field	DPE	SSE	RMA	RTA	STA	PDTS	DPD	PFBC	RSVD	PC66	CLIST	IS	RSVD_1	RSVD_2	ID	FBE	SEE	WCC	PERE	VGA_PSE	MWIE	SCE	BME	MSE	IOSE

Bit Range	Default & Access	Description
31	0b RW/C	**DPE Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0b RW/C	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0b RW/C	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0b RW/C	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0b RW/C	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	00b RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0b RW/C	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.
23	0b RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0b RO	**Reserved (RSVD):** Reserved
21	0b RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1b RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0b RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:16	000b RO	**Reserved (RSVD_1):** Reserved
15:11	00h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Description
10	0b RW/V	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0b RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0b RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0b RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0b RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0b RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0b RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0b RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0b RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0b RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0b RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

23.6.3 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RID_CC: [B:0, D:28, F:0] + 8h

Power Well: Core

Default: 06040000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BCC								SCC								PI								RID							

Bit Range	Default & Access	Description
31:24	06h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	04h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge.
15:8	00h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	00h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

23.6.4 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

CLS_PLT_HTYPE: [B:0, D:28, F:0] + Ch

Power Well: Core

Default: 00810000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Fields: RSVD (31:24), MFD (23), HTYPE (22:16), CT (15:11), RSVD_1 (10:8), LS (7:0)

Bit Range	Default & Access	Description
31:24	00h RO	**Reserved (RSVD):** Reserved
23	1b RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	01h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge.
15:11	00h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	000b RO	**Reserved (RSVD_1):** Reserved
7:0	00h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

23.6.5 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

BNUM_SLT: [B:0, D:28, F:0] + 18h

Power Well: Core

Default: 00000000h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
SLT	SBBN	SCBN	PBN

Bit Range	Default & Access	Description
31:24	00h RW/V	**Secodary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	00h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	00h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	00h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

23.6.6 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IOBL_SSTS: [B:0, D:28, F:0] + 1Ch

Power Well: Core

Default: 00000000h

31	30	29	28	27	26:25	24	23	22	21	20:16	15:12	11:8	7:4	3:0
0	0	0	0	0	0 0	0	0	0	0	0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
DPE	RSE	RMA	RTA	STA	SDTS	DPD	SFBC	RSVD	SC66	RSVD_1	IOLA	IOLC	IOBA	IOBC

Bit Range	Default & Access	Description
31	0b RW/C	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0b RW/C	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0b RW/C	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0b RW/C	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.
27	0b RW/C	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	00b RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0b RW/C	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.

Bit Range	Default & Access	Description
23	0b RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0b RO	**Reserved (RSVD):** Reserved
21	0b RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	00h RO	**Reserved (RSVD_1):** Reserved
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

23.6.7 Memory Base and Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

MBL: [B:0, D:28, F:0] + 20h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ML												RSVD				MB												RSVD_1			

Bit Range	Default & Access	Description
31:20	000h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved (RSVD):** Reserved
15:4	000h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved (RSVD_1):** Reserved

23.6.8 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMBL: [B:0, D:28, F:0] + 24h

Power Well: Core

Default: 00010001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PML												I64L				PMB												I64B			

Bit Range	Default & Access	Description
31:20	000h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	000h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

23.6.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMBU32: [B:0, D:28, F:0] + 28h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PMBU																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

23.6.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMLU32: [B:0, D:28, F:0] + 2Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PMLU																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

23.6.11 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPP: [B:0, D:28, F:0] + 34h

Power Well: Core

Default: 00000040h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
RSVD																								PTR							

Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved (RSVD):** Reserved
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h

23.6.12 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTR_BCTRL: [B:0, D:28, F:0] + 3Ch

Power Well: Core

Default: 00000000h

31:28	27	26	25	24	23	22	21	20	19	18	17	16	15:8	7:0
0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
RSVD	DTSE	DTS	SDT	PDT	FBE	SBR	MAM	V16	VE	IE	SE	PERE	IPIN	ILINE

Bit Range	Default & Access	Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27	0b RW/V	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0b RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0b RW/V	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
24	0b RW/V	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0b RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0b RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0b RW/V	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0b RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0b RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0b RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0b RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0b RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.

Bit Range	Default & Access	Description
15:8	00h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

23.6.13 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLIST_XCAP: [B:0, D:28, F:0] + 40h

Power Well: Core

Default: 00428010h

31	30	29:25	24	23:20	19:16	15:8	7:0
0	0	0 0 0 0 0	0	0 1 0 0	0 0 1 0	1 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0
RSVD	RSVD_1	IMN	SI	DT	CV	NEXT	CID

Bit Range	Default & Access	Description
31	0b RO	**Reserved (RSVD):** Reserved
30	0b RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec
29:25	00h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0b RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

23.6.14 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DCAP: [B:0, D:28, F:0] + 44h

Power Well: Core

Default: 00008000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			FLRC	CSPS		CSPV								RSVD_1		RBER	RSVD_2	RSVD_3	RSVD_4	E1AL			E0AL			ETFS	PFS		MPS		

Bit Range	Default & Access	Description
31:29	000b RO	**Reserved (RSVD):** Reserved
28	0b RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	00b RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	00h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	00b RO	**Reserved (RSVD_1):** Reserved
15	1b RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions.
14	0b RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP)
13	0b RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP)
12	0b RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP)
11:9	000b RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	000b RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0b RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	00b RO	**Phantom Functions Supported (PFS):** No phantom functions supported

Bit Range	Default & Access	Description
2:0	000b RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of 128B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

23.6.15 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DCTL_DSTS: [B:0, D:28, F:0] + 48h

Power Well: Core

Default: 00100000h

Bits	31:22	21	20	19	18	17	16	15	14:12	11	10	9	8	7:5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0	0	1	0	0	0	0	0	0 0 0	0	0	0	0	0 0 0	0	0	0	0	0
Field	RSVD	TDP	APD	URD	FED	NFED	CED	RSVD_1	MRRS	ENS	APME	PFE	ETFE	MPS	ERO	URE	FEE	NFE	CEE

Bit Range	Default & Access	Description
31:22	000h RO	**Reserved (RSVD):** Reserved
21	0b RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1b RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
19	0b RW/C	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0b RW/C	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0b RW/C	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0b RW/C	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0b RO	**Reserved (RSVD_1):** Reserved
14:12	000b RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0b RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0b RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power.

Bit Range	Default & Access	Description
9	0b RO	**Phantom Functions Enable (PFE):** Not supported
8	0b RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	000b RW	**Max Payload Size (MPS):** The root port only supports 128B max payload. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0b RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0b RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0b RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0b RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0b RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

23.6.16 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

LCAP: [B:0, D:28, F:0] + 4Ch

Power Well: Core

Default: 00310C02h

31	28	24	20	16	12	8	4	0
	0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 1	0 0 0 0	1 1 0 0	0 0 0 0	0 0 1 0

Fields (bit 31 to bit 0): PN, RSVD, LBNC, LARC, SDERC, CPM, EL1, EL0, APMS, MLW, SLS

Bit Range	Default & Access	Description
31:24	00h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h

Bit Range	Default & Access	Description
23:22	00b RO	**Reserved (RSVD):** Reserved
21	1b RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1b RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0b RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0b RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	010b RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b - Less than 1 us 001b - 1 us to less than 2 us 010b - 2 us to less than 4 us 011b - 4 us to less than 8 us 100b - 8 us to less than 16 us 101b - 16 us to less than 32 us 110b - 32 us to 64 us 111b - More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	000b RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration.
11:10	11b RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 (Reserved) 01 L0s Entry supported 10 Reserved 11 Both L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	000000b RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h
3:0	2h RO/V	**Supported Link Speeds (SLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set, else this register reports a value of 0010b.

23.6.17 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

LCTL_LSTS: [B:0, D:28, F:0] + 50h

Power Well: Core

Default: 00010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LABS	LBMS	LA	SCC	LT	RSVD	NLW						CLS				RSVD_1				LABIE	LBMIE	HAWD	ECPM	ES	CCC	RL	LD	RCBC	RSVD_2	ASPM	

Bit Range	Default & Access	Description
31	0b RW/C	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.
30	0b RW/C	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0b RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0b RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock.
27	0b RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0b RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification.
25:20	00h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link The value of this field is undefined if the link is not up.
15:12	0h RO	**Reserved (RSVD_1):** Reserved
11	0b RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0b RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0b RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b.
8	0b RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0b RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	0b RW	**Common Clock Configuration (CCC):** Reserved.

Bit Range	Default & Access	Description
5	0b WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0b RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0b RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0b RO	**Reserved (RSVD_2):** Reserved
1:0	00b RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

23.6.18 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SLCAP: [B:0, D:28, F:0] + 54h

Power Well: Core

Default: 00040060h

Bits	31:24	23:19	18	17	16:15	14:8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0	1	0	0 0	0 0 0 0 0 0 0	0	1	1	0	0	0	0	0
Field	PSN	PSN_1	NCCS	EMIP	SLS	SLV	SLV_1	HPC	HPS	PIP	AIP	MSP	PCP	ABP

Bit Range	Default & Access	Description
31:24	00h RW/O	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	00h RW/O	**Physical Slot Number (PSN_1):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1b RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0b RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	00b RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	00h RW/O	**Slot Power Limit Value (SLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.

Bit Range	Default & Access	Description
7	0b RW/O	**Slot Power Limit Value (SLV_1):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1b RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1b RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0b RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0b RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0b RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0b RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0b RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

23.6.19 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SLCTL_SLSTS: [B:0, D:28, F:0] + 58h

Power Well: Core

Default: 00000000h

Bits	31:25	24	23	22	21	20	19	18	17	16	15:13	12	11	10	9:8	7:6	5	4	3	2	1	0
Field	RSVD	DLLSC	EMIS	PDS	MS	CC	PDC	MSC	PFD	ABP	RSVD_1	DLLSCE	EMIC	PCC	PIC	AIC	HPE	CCE	PDE	MSE	PFE	ABE
Default	0000000	0	0	0	0	0	0	0	0	0	000	0	0	0	00	00	0	0	0	0	0	0

Bit Range	Default & Access	Description
31:25	00h RO	**Reserved (RSVD):** Reserved
24	0b RW/C	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0b RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0b RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0b RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.

Bit Range	Default & Access	Description
20	0b RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0b RW/C	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0b RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0b RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0b RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	000b RO	**Reserved (RSVD_1):** Reserved
12	0b RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0b RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0b RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	00b RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	00b RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0b RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0b RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..
3	0b RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0b RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0b RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0b RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

23.6.20 Root Control (RCTL)—Offset 5Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RCTL: [B:0, D:28, F:0] + 5Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																RSVD_1												PIE	SFE	SNE	SCE

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15:4	000h RO	**Reserved (RSVD_1):** Reserved
3	0b RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0b RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0b RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0b RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

23.6.21 Root Status (RSTS)—Offset 60h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RSTS: [B:0, D:28, F:0] + 60h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD														PP	PS	RID															

Bit Range	Default & Access	Description
31:18	0000h RO	**Reserved (RSVD):** Reserved
17	0b RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0b RW/C	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0000h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

23.6.22 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DCAP2: [B:0, D:28, F:0] + 64h

Power Well: Core

Default: 00080816h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0
RSVD												OBFFS		RSVD_1						LTRMS	RSVD_2						CTDS	CTRS			

Bit Range	Default & Access	Description
31:20	000h RO	**Reserved (RSVD):** Reserved
19:18	10b RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported.
17:12	00h RO	**Reserved (RSVD_1):** Reserved
11	1b RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability.
10:5	00h RO	**Reserved (RSVD_2):** Reserved
4	1b RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	6h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C [lt]-- This is supported 0111b Ranges A, B [amp] C 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

23.6.23 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DCTL2_DSTS2: [B:0, D:28, F:0] + 68h

Power Well: Core

Default: 00000000h

31	28			24				20				16				12				8				4				0			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																RSVD_1	OBFFEN		RSVD_2		LTREN	RSVD_3					CTD	CTV			

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15	0b RO	**Reserved (RSVD_1):** Reserved
14:13	00b RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	00b RO	**Reserved (RSVD_2):** Reserved
10	0b RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:5	00h RO	**Reserved (RSVD_3):** Reserved
4	0b RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

23.6.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

Size:32 bits

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

LCAP2: [B:0, D:28, F:0] + 6Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD

Bit Range	Default & Access	Description
31:0	00000000h RO	**Reserved (RSVD):** Reserved

23.6.25 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

LCTL2_LSTS2: [B:0, D:28, F:0] + 70h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD, CDL, RSVD_1, CD, CSOS, EMC, TM, SD, HASD, EC, TLS

Bit Range	Default & Access	Description
31:17	0000h RO	**Reserved (RSVD):** Reserved
16	0b RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed.
15:13	000b RO	**Reserved (RSVD_1):** Reserved
12	0b RW/P	**Compliance De-emphasis (CD):** This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b-3.5 dB 0b-6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing.
11	0b RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b.

Bit Range	Default & Access	Description
10	0b RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
9:7	000b RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0b RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0b RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.
4	0b RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b.
3:0	0h RW/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. For root port, the allowed value is: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s and 2.5GT/s Link speeds supported If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, the result is undefined. The default value of this field is the highest Link speed supported by the component (as reported in the Supported Link Speeds field of the Link Capabilities register).

23.6.26 Slot Capabilities 2 (SLCAP2)—Offset 74h

Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SLCAP2: [B:0, D:28, F:0] + 74h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																															

Bit Range	Default & Access	Description
31:0	00000000h RO	**Reserved (RSVD):** Reserved

23.6.27 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SLCTL2_SLSTS2: [B:0, D:28, F:0] + 78h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							RSVD																RSVD_1								

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15:0	0000h RO	**Reserved (RSVD_1):** Reserved

23.6.28 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MID_MC: [B:0, D:28, F:0] + 80h

Power Well: Core

Default: 00009005h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1
			RSVD					C64		MME			MMC		MSIE				NEXT								CID				

Bit Range	Default & Access	Description
31:24	00h RO	**Reserved (RSVD):** Reserved
23	0b RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.

Bit Range	Default & Access	Description
22:20	000b RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	000b RO	**Multiple Message Capable (MMC):** Only one message is required.
16	0b RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

23.6.29 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MA: [B:0, D:28, F:0] + 84h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADDR	RSVD

Bit Range	Default & Access	Description
31:2	00000000h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	00b RO	**Reserved (RSVD):** Reserved

23.6.30 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MD: [B:0, D:28, F:0] + 88h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD	DATA

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15:0	0000h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

23.6.31 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SVCAP: [B:0, D:28, F:0] + 90h

Power Well: Core

Default: 0000A00Dh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	1
RSVD																NEXT								CID							

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	0Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

23.6.32 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SVID: [B:0, D:28, F:0] + 94h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SID																SVID															

Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0000h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

23.6.33 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCAP_PMC: [B:0, D:28, F:0] + A0h

Power Well: Core

Default: C8030001h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PMES					D2S	D1S	AC			DSI	RSVD	PMEC	VS			NEXT								CID							

Bit Range	Default & Access	Description
31:27	11001b RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0b RO	**D2_Support (D2S):** The D2 state is not supported.
25	0b RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	000b RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspend well power consumption.
21	0b RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0b RO	**Reserved (RSVD):** Reserved
19	0b RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	011b RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	01h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

23.6.34 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCS: [B:0, D:28, F:0] + A4h

Power Well: Core

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DTA								BPCE	B23S	RSVD						PMES	DSC		DSEL				PMEE	RSVD_1				NSR	RSVD_2	PS	

Bit Range	Default & Access	Description
31:24	00h RO	**Data (DTA):** Reserved
23	0b RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0b RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	00h RO	**Reserved (RSVD):** Reserved
15	0b RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.
14:13	00b RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0b RW/P	**PME Enable (PMEE):** Indicates PME is enabled. This register maintains its value through S3/4/5 states.
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0b RO	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0b RO	**Reserved (RSVD_2):** Reserved
1:0	00b RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

23.6.35 Manufacturer's ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:28, F:0] + F8h

Power Well: Core

Default: 00000F00h

31:28	27:24	23:16	15:8	7:0
0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1	0 0 0 0 0 0 0 0
RSVD	DPID	SID	MID	PD

Bit Range	Default & Access	Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27:24	0h RO/V	**Dot portion of Process ID (DPID):** The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the dot as .8.
23:16	00h RO/V	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. A single Manufacturing Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step.
15:8	0Fh RO	**Manufacturing Identifier (MID):** 0Fh = Intel
7:0	00h RO/V	**Process/Dot (PD):** Indicates the current process. The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the Process (1265).

23.6.36 Advanced Error Reporting Capability Header (AECH)—Offset 100h

The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

AECH: [B:0, D:28, F:0] + 100h

Power Well: Core

Default: 00000000h

31:20	19:16	15:0
0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
NCO	CV	CID

Bit Range	Default & Access	Description
31:20	000h RO	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.

Bit Range	Default & Access	Description
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0000h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

23.6.37 Uncorrectable Error Status (UES)—Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

UES: [B:0, D:28, F:0] + 104h

Power Well: Core

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD | AVS | URE | EE | MT | RO | UC | CA | CT | FCPE | PT | RSVD_1 | SDE | DLPE | RSVD_2 | TE

Bit Range	Default & Access	Description
31:22	000h RO	**Reserved (RSVD):** Reserved
21	0b RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0b RW/1C/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0b RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0b RW/1C/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0b RW/1C/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0b RW/1C/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0b RW/1C/P	**Completor Abort Status (CA):** Indicates a completer abort was received
14	0b RW/1C/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0b RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0b RW/1C/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.

Bit Range	Default & Access	Description
11:6	00h RO	**Reserved (RSVD_1):** Reserved
5	0b RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0b RW/1C/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	000b RO	**Reserved (RSVD_2):** Reserved
0	0b RO	**Training Error Status (TE):** Not supported.

23.6.38 Uncorrectable Error Mask (UEM)—Offset 108h

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

UEM: [B:0, D:28, F:0] + 108h

Power Well: Core

Default: 00000000h

31:22	21	20	19	18	17	16	15	14	13	12	11:6	5	4	3:1	0
0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0 0 0 0 0 0	0	0	0 0 0	0
RSVD	AVS	URE	EE	MT	RO	UC	CM	CT	FCPE	PT	RSVD_1	SDE	DLPE	RSVD_2	TE

Bit Range	Default & Access	Description
31:22	000h RO	**Reserved (RSVD):** Reserved
21	0b RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0b RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0b RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0b RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0b RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0b RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0b RW/P	**Completor Abort Mask (CM):** Mask for completer abort.

Bit Range	Default & Access	Description
14	0b RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0b RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0b RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	00h RO	**Reserved (RSVD_1):** Reserved
5	0b RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0b RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	000b RO	**Reserved (RSVD_2):** Reserved
0	0b RO	**Training Error Mask (TE):** Not supported.

23.6.39 Uncorrectable Error Severity (UEV)—Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

UEV: [B:0, D:28, F:0] + 10Ch

Power Well: Core

Default: 00060011h

Bits	31:22	21	20	19	18	17	16	15	14	13	12	11:6	5	4	3:1	0
Default	0 0 0 0 0 0 0 0 0 0	0	0	0	1	1	0	0	0	0	0	0 0 0 0 0 0	0	1	0 0 0	1
Field	RSVD	AVS	URE	EE	MT	RO	UC	CA	CT	FCPE	PT	RSVD_1	SDE	DLPE	RSVD_2	TE

Bit Range	Default & Access	Description
31:22	000h RO	**Reserved (RSVD):** Reserved
21	0b RO	**ACS Violation Severity (AVS):** Reserved. Access Control Services are not supported
20	0b RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0b RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1b RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.

Bit Range	Default & Access	Description
17	1b RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0b RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0b RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0b RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0b RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0b RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	00h RO	**Reserved (RSVD_1):** Reserved
5	0b RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1b RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	000b RO	**Reserved (RSVD_2):** Reserved
0	1b RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

23.6.40 Correctable Error Status (CES)—Offset 110h

This register is only reset by a loss of core power

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CES: [B:0, D:28, F:0] + 110h

Power Well: Core

Default: 00000000h

Bits	31:14	13	12	11:9	8	7	6	5:1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0 0 0	0	0	0	0 0 0 0 0	0
Field	RSVD	ANFES	RTT	RSVD_1	RNR	BD	BT	RSVD_2	RE

Bit Range	Default & Access	Description
31:14	00000h RO	**Reserved (RSVD):** Reserved
13	0b RW/1C/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occured.
12	0b RW/1C/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.

Bit Range	Default & Access	Description
11:9	000b RO	**Reserved (RSVD_1):** Reserved
8	0b RW/1C/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0b RW/1C/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0b RW/1C/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	00h RO	**Reserved (RSVD_2):** Reserved
0	0b RW/1C/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

23.6.41 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CEM: [B:0, D:28, F:0] + 114h

Power Well: Core

Default: 00002000h

Bits	31:14	13	12	11:9	8	7	6	5:1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0 0 0	0	0	0	0 0 0 0 0	0
Field	RSVD	ANFEM	RTT	RSVD_1	RNR	BD	BT	RSVD_2	RE

Bit Range	Default & Access	Description
31:14	00000h RO	**Reserved (RSVD):** Reserved
13	1b RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0b RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	000b RO	**Reserved (RSVD_1):** Reserved
8	0b RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0b RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.

Bit Range	Default & Access	Description
6	0b RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	00h RO	**Reserved (RSVD_2):** Reserved
0	0b RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

23.6.42 Advanced Error Capabilities and Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

AECC: [B:0, D:28, F:0] + 118h

Power Well: Core

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RSVD (31:9)	ECE (8)	ECC (7)	EGE (6)	EGC (5)	FEP (4:0)

Bit Range	Default & Access	Description
31:9	000000h RO	**Reserved (RSVD):** Reserved
8	0b RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0b RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0b RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0b RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	00000b RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

23.6.43 Header Log DW1 (HL_DW1)—Offset 11Ch

Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

HL_DW1: [B:0, D:28, F:0] + 11Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DW1

Bit Range	Default & Access	Description
31:0	00000000h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

23.6.44 Header Log DW2 (HL_DW2)—Offset 120h

Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

HL_DW2: [B:0, D:28, F:0] + 120h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DW2

Bit Range	Default & Access	Description
31:0	00000000h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

23.6.45 Header Log DW3 (HL_DW3)—Offset 124h

Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

HL_DW3: [B:0, D:28, F:0] + 124h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DW3

Bit Range	Default & Access	Description
31:0	00000000h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

23.6.46 Header Log DW4 (HL_DW4)—Offset 128h

Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

HL_DW4: [B:0, D:28, F:0] + 128h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DW4																															

Bit Range	Default & Access	Description
31:0	00000000h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

23.6.47 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

REC: [B:0, D:28, F:0] + 12Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																													FERE	NERE	CERE

Bit Range	Default & Access	Description
31:3	00000000h RO	**Reserved (RSVD):** Reserved
2	0b RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0b RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0b RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

23.6.48 Root Error Status (RES)—Offset 130h

This register can track more than one error and set the 'multiple' bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RES: [B:0, D:28, F:0] + 130h

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AEMN					RSVD																				FEMR	NFEMR	FUF	MENR	ENR	MCR	CR

Bit Range	Default & Access	Description
31:27	00h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated.
26:7	00000h RO	**Reserved (RSVD):** Reserved
6	0b RW/1C/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0b RW/1C/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0b RW/1C/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	0b RW/1C/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0b RW/1C/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0b RW/1C/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0b RW/1C/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

23.6.49 Error Source Identification (ESID)—Offset 134h

Size:32 bits Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ESID: [B:0, D:28, F:0] + 134h

Power Well: Core

Default: 00000000h

Bits	31:16	15:0
Default	0000 0000 0000 0000	0000 0000 0000 0000
Field	EFNFSID	ECSID

Bit Range	Default & Access	Description
31:16	0000h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0000h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

23.6.50 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

PCIESTS1: [B:0, D:28, F:0] + 328h

Power Well: Core

Default: 00000000h

Bits	31:24	23	22:19	18:17	16	15:12	11:0
Default	0000 0000	0	000 0	00	0	0000	0000 0000 0000
Field	LTSMSTATE	RSVD	LNKSTAT	REPLAYNUM	DLLRETRY	LANESTAT	NXTTXSEQNUM

Bit Range	Default & Access	Description
31:24	00h RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. 00000: DETECTQUIET 00001: DETECTACTIVE 00010: POLLINGACTIVE 00011: POLLINGCOMPLIANCE 00100: POLLINGCONFIGURATION 00101: POLLINGSPEED 00110: CONFIGRCVRCFG 00111: CONFIGRCVRCFGLPBK 01000: CONFIGIDLE 01001: L0 01010: L0WAIT 01011: RECOVERYRCVRLOCK 01100: RECOVERYRCVRCFG 01101: RECOVERYIDLE 01110: RECOVERYIDLELPBK 01111: L1ENTRY 10000: L1IDLE 10001: L2IDLE 10010: LINKCONTROLRESET 10011: LOOPBACKENTRY 10100: LOOPBACKACTIVE 10101: LOOPBACKEXITM 10110: LOOPBACKEXITS 10111: DISABLED Note: This register field could be used by REUT software to monitor the link LTSSM substates.
23	0b RO	**Reserved (RSVD):** Reserved
22:19	0000b RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved
18:17	00b RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero.

Bit Range	Default & Access	Description
16	0b RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet.
15:12	0h RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained).
11:0	000h RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP.

23.6.51 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

PCIESTS2: [B:0, D:28, F:0] + 32Ch

Power Well: Core

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P48PNCCWSSCMES	P37PNCCWSSCMES	P26PNCCWSSCMES	P15PNCCWSSCMES	NXTRCVSEQ												RSVD				LASTACKSEQNUM											

Bit Range	Default & Access	Description
31	0b RO/V	**PCIe Port 4 Non-Common Clock With SSC Mode Enable Strap (P48PNCCWSSCMES):** '0': PCIe port 4/8 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 4/8 is enabled to operate in non-common clock mode with SSC enabled.
30	0b RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P37PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled.
29	0b RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P26PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled.
28	0b RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P15PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled.
27:16	000h RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next.
15:12	0h RO	**Reserved (RSVD):** Reserved
11:0	000h RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP.

23.6.52 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**PCIECMMPC:** [B:0, D:28, F:0] + 330h
Power Well: Core	

Default: 28000016h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
RSVD		SYM3SEL	SYM2SEL	SYM1SEL	SYM0SEL	RSVD_1		ERRLANENUM		RSVD_2						INVERT			SYMERRNUMINV			SYMERRNUM		ERRDET	SLNINVCMM		AUTOINVERT	STAT	INVEN	RSVD_3	START

Bit Range	Default & Access	Description
31:30	00b RO	**Reserved (RSVD):** Reserved
29	1b RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character
28	0b RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character
27	1b RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character
26	0b RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character
25:24	00b RO	**Reserved (RSVD_1):** Reserved
23:22	00b RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1.
21:16	00h RO	**Reserved (RSVD_2):** Reserved
15:13	000b RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated)
12:10	000b RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0
9:8	00b RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3

Bit Range	Default & Access	Description
7	0b RW/C	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation.
6:5	00b RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM
4	1b RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion
3	0b RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set.
2	1b RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted
1	1b RW	**Reserved (RSVD_3):** Reserved
0	0b RW	**CMM Start (START):** 1: Start CMM 0: Stop CMM

23.6.53 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIECMMSB: [B:0, D:28, F:0] + 334h

Power Well: Core

Default: 4ABCB5BCh

31			28				24				20				16				12				8				4				0
0	1	0	0	1	0	1	0	1	0	1	1	1	1	0	0	1	0	1	1	0	1	0	1	1	0	1	1	1	1	0	0
DATA3								DATA2								DATA1								DATA0							

Bit Range	Default & Access	Description
31:24	4Ah RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link.
23:16	BCh RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link.
15:8	B5h RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link.
7:0	BCh RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link.

23.7 PCI Express* Lane 0 Electrical Address Map

Table 244. Summary of PCI Express* Lane 0 Electrical Message Bus Registers—0xA6 (Global Offset 200h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 3241	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 3243	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 3244	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 3246	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 3246	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 3247	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 3249	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 3249	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 3250	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 3252	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 3253	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 3254	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 3256	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 3257	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 3258	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 3259	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 3261	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 3262	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 3264	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 3265	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 3266	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 3267	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 3268	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 3268	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 3269	0001C020h

23.7.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA6] + (200h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 00010080h

Bits	Default	Field
31:28	0 0 0 0	reg_txcfgchange_valid_delay_3_0
27:24	0 0 0 0	reg_txcfgchange_rst_delay_3_0
23	0	reserved500
22:18	0 0 0 0 0	reg_txcfgchange_width_4_0
17	0	reg_txcfgchange_ovrride
16	1	reg_tx2_soft_reset_n
15	0	reg_txswng_clksel
14	0	reg_rcvdetect_ovrd_
13	0	reg_rcvdetected_
12	0	reg_rcvdetectfinished_
11	0	reg_rcvdetect_pulse_width_ovrd
10:8	0 0 0	reg_rcvdetect_pulse_width_2_0
7	1	reg_tx1_soft_reset_n
6	0	reg_tx_8b10b_bypass
5	0	reg_tx_laneup
4	0	reg_left_txfifo_rst_master2
3	0	reg_right_txfifo_rst_master2
2	0	reg_plllinksynch_ovrden
1	0	reg_plllinksynch_ovrd
0	0	reg_tx1_cmmdisparity

Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd______________________:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected__________________________:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished___________________:** override for rcvdetectfinished
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass

Bit Range	Default & Access	Description
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

23.7.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword1: [Port: 0xA6] + (200h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 00600060h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	reg_txfsm_4us_delay_7_0
23	0	reg_softreset_enable
22	1	cri_rxeb_eiosenable
21	1	cri_rxdigfiltsq_enable
20	0	reg_txfsm_delay_ovrd
19:16	0 0 0 0	reg_txfsm_4us_delay_11_8
15:14	0 0	reg_pclk_rate_1_0
13:12	0 0	reg_rate_1_0
11:9	0 0 0	reg_phymode_2_0
8	0	reg_modeovren
7:6	0 1	reg_datawidth
5	1	soft_reset_n
4	0	reg_diginelben
3	0	reg_digifelben
2	0	reg_strapgroup_ovrden
1	0	reg_yank_timer_done_b_ovrd
0	0	reg_yank_timer_done_b_ovrd_en

Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down

Bit Range	Default & Access	Description
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

23.7.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword2: [Port: 0xA6] + (200h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

reg_rxpwrfsm_pibiasoff_delay_3_0 | cri_sqdbexittimer_override_3_0 | cri_sqdbentrytimer_override_5_0 | reg_rxdrcgtsqsel_1_0 | cri_reut_SlaveSideDataCheckingEn | cri_sqdbtimer_ovren | cri_rxpwrfsm_timer_ovren | reg_rxidle | cri_rxrawdata_sel | cri_dynkalign_eco3302703_mode | cri_dynkalign_eco3302703_ovren | reg_rxpwrfsm_pibiasoff_ovrride | cri_reset_kalignlck | cri_ebptrrst | cri_comdispfix | cri_forcebankhit | cri_kalignmode_1_0 | cri_skpprocdis | cri_elasticbuffer_maskdis

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode

Bit Range	Default & Access	Description
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

23.7.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA6] + (200h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 5515ACAAh

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
cri_dfx_patbuf_55_48								cri_dfx_patbuf_63_56								cri_dfx_patbuf_71_64								cri_dfx_patbuf_79_72							

Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.7.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword4: [Port: 0xA6] + (200h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	0	0	0	0	0	1
cri_dfx_patbuf_23_16								cri_dfx_patbuf_31_24								cri_dfx_patbuf_39_32								cri_dfx_patbuf_47_40							

Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.7.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword5: [Port: 0xA6] + (200h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00003E63h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1
cri_dfx_patbuftrain	cri_dfx_prbspoly_2_0			cri_dfx_patbufsize_1_0		cri_dfx_patbufloop	cri_dfx_patbufdwidth	cri_dfx_patbuftrainovr	cri_dfx_marginmode	cri_dfx_chk_sel	cri_dfx_patchken	cri_dfx_patgenen	cri_dfx_clrerrcnt	cri_dfx_lcereset	cri_dfx_lcestart	cri_dfx_patbuf_7_0								cri_dfx_patbuf_15_8							

Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.7.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA6] + (200h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: FFFFFFFFh

Bits	31:24	23:16	15:8	7:0
Default	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Field	cri_dfx_prbsseed_7_0	cri_dfx_prbsseed_15_8	cri_dfx_prbsseed_23_16	cri_dfx_prbsseed_31_24

Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

23.7.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA6] + (200h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000009h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	dfx_cri_errcnt_7_0
23:16	0 0 0 0 0 0 0 0	dfx_cri_errcnt_15_8
15	0	i_rxcaldone
14	0	dfx_cri_lcemgnerr
13	0	cri_dfx_patgen2active
12	0	dfx_cri_patbufallfail
11	0	dfx_cri_patchkactive
10	0	dfx_cri_patgenactive
9	0	dfx_cri_lcetraindone
8	0	dfx_cri_lcetrainactive
7	0	reserved501
6	0	cri_dfx_patgen2en
5:4	0 0	cri_dfx_maxerrcnt_1_0
3:0	1 0 0 1	cri_dfx_prbstraincnt_3_0

Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

23.7.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword8: [Port: 0xA6] + (200h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 000000C4h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1 0 0

reg_partial, reg_slumber, reg_tx2_cdr_override_2_0, reg_cdr_override_2_0, reg_ebuffmode, reg_usedclockchannel_1_0, reg_usedclockchannel_ovrride, reg_gbl_ovrride, reg_tx1_pclkon_inp2, reg_tx2_pclkon_inp2, reg_tx2_txenable, cri_rxeb_ptr_init_3_0, reg_powerfsm_ovrride, reg_suspend, reg_pclkcfginput, reg_useqclock, cri_rxeb_hiwater_3_0, cri_rxeb_lowater_3_0

Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed

Bit Range	Default & Access	Description
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

23.7.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword9: [Port: 0xA6] + (200h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields (bit 31 to bit 0): reserved502, reg_strapgroup_4_0, reg_powerdown_1_0, reg_pcs_txcmnkeepdisable_ovrd, reg_straplane_5_0, reg_tx1_powerdown_override, reg_tx2_powerdown_override, reg_txdatavalid, reg_txdeemp_1_0, reg_txmargin_2_0, reg_txswing, reg_txenable, reg_txterm_vcc_1_0, reg_txdetrxlpbk, reg_txelectidle, reg_txcompliance, reg_txoneszeroes, reg_latencyoptim_1_0

Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph

Bit Range	Default & Access	Description
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

23.7.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword10: [Port: 0xA6] + (200h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:28	reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0
27:24	reg_rxpwrfsm_timer_ENABLE_RX_3_0
23:20	reg_rxpwrfsm_timer_RX_SQEN_3_0
19:16	reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0
15:8	reg_clk_valid_cnt_7_0
7	reg_rxterm
6	reg_rxpolarity
5	reg_rxeqtrain
4	reg_rxsquelchen
3	cri_rxpwrfsm_sqentimer_ovrden
2	reg_rxintfltren_override
1	reg_rxintfltren_l
0	reg_clk_valid_cnt_ovrd

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

23.7.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword11: [Port: 0xA6] + (200h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0F000000h

Bits	31:30	29	28:24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9:8	7	6	5	4	3	2	1	0
Default	0 0	0	0 1 1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0
Field	reserved505	reserved506	reg_tx2_stagger_mask_4_0	i_clkbuf_iclken_ovrd	i_clkbuf_qclken_ovrd	reserved503	i_clkbuf_txclkmuxen_ovrd	reserved504	reg_tx2_cmmdisparity	reg_tx1_ctrl_override	reg_tx2_ctrl_override	reg_tx2_txterm_vcc_1	reg_tx2_txterm_vcc_0	reg_tx2_txdetrxlpbk	reg_tx2_txelectidle	reg_tx2_txcompliance	reg_tx2_txoneszeroes	reg_tx2_powerdown_1_0	o_captesten_h	i_captestout	fuse_override	i_clkbuf_ibiasen_ovrd	reg_lanedeskew_strap_ovrd	reg_lane_reverse	reg_left_txfifo_rst_master	reg_right_txfifo_rst_master

Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2

Bit Range	Default & Access	Description
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd______________:** reserved
2	0h RW	**reg_lane_reverse_________________________:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____________:** reserved
0	0h RW	**reg_right_txfifo_rst_master___________:** reserved

23.7.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword12: [Port: 0xA6] + (200h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00250F00h

Bits	Default	Field
31	0	reg_txfsm_200ns_ovrd
30:24	0 0 0 0 0 0 0	reg_txfsm_200ns_delay_6_0
23	0	reg_loadgen2txen_fall_ovrd
22:20	0 1 0	reg_tx2_stagger_mult_2_0
19	0	reg_lanestagger_by_group
18:16	1 0 1	reg_tx1_stagger_mult_2_0
15:14	0 0	reserved509
13	0	reserved510
12:8	0 1 1 1 1	reg_tx1_stagger_mask_4_0
7	0	reserved507
6	0	reg_lanestagger_strap_ovrd
5	0	reserved508
4:0	0 0 0 0 0	reg_lanestagger_strap_4_0

Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

23.7.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA6] + (200h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31	30:29	28:24	23:16	15	14:13	12:8	7:0
Default	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0
Field	visa_en	reserved512	visa_clk_sel1_4_0	visa_lane_sel1_7_0	visa_bypass	reserved511	visa_clk_sel0_4_0	visa_lane_sel0_7_0

Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

23.7.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword14: [Port: 0xA6] + (200h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 007A0018h

Bits	Default	Field
31	0	reg_clkbuf_stagger_ovrd
30	0	reg_clkbuf_stagger_cnt_10
29	0	reg_slowclk_ovrden
28:24	0 0 0 0 0	reg_txloadgenen2txen_fall_delay_4_0
23:20	0 1 1 1	o_cmlmuxsthsel_3_0
19:16	1 0 1 0	o_cmlsthsel_3_0
15:12	0 0 0 0	o_pcisel_3_0
11:8	0 0 0 0	o_pcqsel_3_0
7	0	o_phaseicen
6	0	o_phaseqcen
5	0	o_pcbypass
4	1	o_slowclocken
3	1	o_sclk250en
2:0	0 0 0	cri_kalign_com_cnt

Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

23.7.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA6] + (200h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 04100300h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Fields (bit 31 to bit 0): reg_powermode_del_cfg_fifoptrgen_2_0, reg_clkbuf_en_ovrd, o_deskewen, reserved514, reserved515, reserved516, o_obsselectlocaldown_h, o_obsselectlocalup, o_obsselectm1datadown, o_obsselectm1dataup, o_obsselecttom2_1_0, o_obsselecttom1_1_0, reg_clkbuf_stagger_cnt_1_0, reserved513, reg_clkbuf_stagger_cnt_9_2

Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

23.7.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword16: [Port: 0xA6] + (200h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

Bits	Default	Field
31	0	squelch_shunt_ovrd_en
30:28	0 0 0	squelch_shunt_cnt_2_0
27	0	reserved520
26	0	i_rxsqfsm_timersel
25	0	i_rxsq_asyncmode_h
24	1	i_rxsquelchstby_h
23:18	0 0 0 0 0 0	reserved519
17:16	0 0	cri_dfx_evenoddmask_1_0
15:12	0 0 0 0	reserved518
11:10	0 0	cri_dfx_lce2patsrc_1_0
9:8	0 0	cri_dfx_lcepatsrc_1_0
7:6	0 0	reserved517
5:4	0 0	txloadgen_ctr_val
3	0	cri_txhighpowerei_ovrden
2	0	cri_tx1highpowerei_ovrdval
1	0	cri_tx2highpowerei_ovrdval
0	1	p2_fast_exit_en

Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.

Bit Range	Default & Access	Description
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

23.7.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA6] + (200h + 44h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
oirefdfxsel_1_0		iopampsfpen_h	iopampsfnen_h	iopamppen_h	iopampnen_h	monanapgen	monubufbypassen	reserved522		reg_ivrefen	ivrefen_ovrd	reserved523			oirefcurmonsel	lrcdisable	reserved521			lrc_rdy_pulsegen	lrc_rdy_target_1_0		lrc_rdy_ovd	rxtermpmrcen	rxvgapmrcen	txpmrcen	irefpmrcen	rxtermperrcen	rxvgaperrcen	txperrcen	irefperrcen

Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode

Bit Range	Default & Access	Description
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

23.7.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA6] + (200h + 48h)

Op Codes:
0h - Read, 1h - Write

Default: 00008080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Field
31:27	reserved524
26	reg_lrc_calcsonly
25:24	adcout_9_8
23:16	adcout_7_0
15:8	adc2_9_2
7:0	adc1_9_2

Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimination filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimination filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

23.7.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA6] + (200h + 4Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00004F10h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0
iamp0calcode_7_0								cal_num				cal_start	cal_type	cal_inv	cal_rst	calclkdivsel_1_0		reserved525	calib_done	cal_fb_count				adc_acctime_1_0		adc_clksel_1_0		adcmuxsel_2_0			adcstart

Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [lyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single

Bit Range	Default & Access	Description
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

23.7.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA6] + (200h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
rxvgarccode_7_0								rxtermrccode_7_0								txrccode_7_0								irefrccode_7_0							

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

23.7.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA6] + (200h + 54h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

31 – 24	23 – 16	15 – 8	7 – 0
1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
rxvgarcscale_7_0	rxtermrcscale_7_0	txrcscale_7_0	irefrcscale_7_0

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

23.7.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA6] + (200h + 58h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31:24	23:16	15:8	7:0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	rxvgarcoffset_7_0	rxtermrcoffset_7_0	txrcoffset_7_0	irefrcoffset_7_0

Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

23.7.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA6] + (200h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h

Bits	31:24	23	22:19	18:16	15:12	11:8	7:4	3:0
Default	0 0 0 0 0 0 0 0	0	0 0 1 1	0 0 0	0 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0
Field	iclkqcfg_spare_7_0	iclkicfg_spare_7	iclkicfg_spare_6_3	iclkicfg_spare_2_0	reserved526	i_drvcfg_3_0	i_ploadcfg_3_0	ipbiasctrl_3_0

Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

23.7.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword24: [Port: 0xA6] + (200h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
reserved528								reserved527							cri_lanereset_clkgatectl	cri_lanereqforce	cri_susclkdisable_delay_4_0					cri_data_dynclkgate_mode_1_0		cri_eios_waittime_ovren	cri_eios_waittime_6_0						

Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved

Bit Range	Default & Access	Description
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (i.e. 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay .... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

23.8 PCI Express* Lane 0 Electrical Address Map

Table 245. Summary of PCI Express* Lane 0 Electrical Message Bus Registers—0xA6 (Global Offset 280h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 3271	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 3272	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 3273	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 3274	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 3275	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 3276	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 3276	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 3277	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 3278	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 3279	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 3280	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 3281	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 3283	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 3284	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 3285	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 3286	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 3287	00008A00h

23.8.1 TX_DWORD0 (tx_dword0)—Offset 0h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword0: [Port: 0xA6] + (280h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah

31			28				24				20				16				12				8				4				0
0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0
reserved504	ofrcr1main3_6_0							reserved503	reserved502							reserved501	reserved500							ofrcdrvr1r2	ofrcr1main0_6_0						

Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

23.8.2 TX_DWORD1 (tx_dword1)—Offset 4h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword1: [Port: 0xA6] + (280h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved510	ofrcr2short3_5_0	reserved509	reserved508	reserved507	reserved506	reserved505	ofrcr2short0_5_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

23.8.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (280h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 5580983Ah

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	1	1	0	1	0

Bits 31:24	Bits 23:16	Bits 15:8	Bit 7	Bits 6:0
omargin010_7_0	omargin000_7_0	ouniqtranscale_7_0	reserved511	ofrcslices_6_0

Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

23.8.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword3: [Port: 0xA6] + (280h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0C782040h

31	30	29:28	27:26	25	24	23:16	15:8	7:0
0	0	0 0	1 1	0	0	0 1 1 1 1 0 0 0	0 0 1 0 0 0 0 0	0 1 0 0 0 0 0 0
opisorate8b_h	obeacondivratio	ouniqetrangenmethod_1_0	oscaledcompmethod_1_0	odeemswinggenmethod	odownscaleampmethod	omargin101_7_0	omargin100_7_0	omargin011_7_0

Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p

Bit Range	Default & Access	Description
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

23.8.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA6] + (280h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 2B404D55h

31			28				24				20				16				12				8				4				0
0	0	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1
ow2tapdeemph9p5_7_0								ow2tapdeemph6p0_7_0								ow2tapgen2deemph3p5_7_0								ow2tapgen1deemph3p5_7_0							

Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

23.8.6 TX_DWORD5 (tx_dword5)—Offset 14h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (280h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31	30:24	23:16	15:8	7:0
Default	0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	ocalcinit	reserved515	reserved514	reserved513	reserved512

Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

23.8.7 TX_DWORD6 (tx_dword6)—Offset 18h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword6: [Port: 0xA6] + (280h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h

Bits	31	30:24	23	22:16	15	14:8	7	6:0
Default	0	0 0 1 1 1 1 1	0	0 1 0 0 0 0 0	0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0
Field	reserved520	onswbypass_6_0	reserved519	opswbypass_6_0	reserved518	reserved517	ocalccont	reserved516

Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved

Bit Range	Default & Access	Description
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

23.8.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA6] + (280h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	1

reserved527	reserved526	reserved525	reserved524	reserved523	oslrctrlr2_l_2_0	oslrctrlr2_h_2_0	reserved522	oslrctrl_l_2_0	oslrctrl_h_2_0	reserved521	or2bypass_5_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved

Bit Range	Default & Access	Description
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

23.8.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword8: [Port: 0xA6] + (280h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 0600AA80h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0

Bits	Field
31:24	ontlpdtime_7_0
23:22	ofrcdccoup_1_0
21	obypbycomp
20:16	obypdftmode_4_0
15:8	odftpisodata1_7_0
7:6	odftpisodata0_1_0
5:3	reserved529
2:0	reserved528

Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG

Bit Range	Default & Access	Description
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

23.8.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA6] + (280h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00430C06h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0
ontlstrongpulling	ontlen	ontllowrefsel_2_0			ontlhighrefsel_2_0			ofrcsatamode_1_0		otxsusclkfreq_1_0		reserved530		orcvdtctrefselnosus_1_0		orcvdtctputime_7_0								ontlputime_7_0							

Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active

Bit Range	Default & Access	Description
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

23.8.11 TX_DWORD10 (tx_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword10: [Port: 0xA6] + (280h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31:24	23:16	15:10	9	8	7	6	5	4	3:0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0	0	0	0	0	0 0 0 0
Field	isparereead_7_0	reserved532	reserved531	ircvdtctcmpout	idftcaptestsig	idftrcvdetectedtxn	idftrcvdetectedtxp	idftrcvdetectfinished	intlfinished	intlpass_3_0

Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

23.8.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA6] + (280h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00001000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
oselsparetxclkin_2_0			ofrcdotprocess_2_0			ofrcgohighzdis	ofrcgohighzen	ofrcstrongpddis	ofrcstrongpden	ofrctxclkrootdis	ofrctxclkrooten	reserved537	ofrcpwrmodel1	ofrcpwrmodel0s	ofrcpwrmodel0	ofrccmkeeppadnen	ofrccmkeeppadpen	ofrccmkeeppadndis	ofrccmkeeppadpdis	omakedeeperfifo	ofrclatencyoptim_2_0			reserved536	ofrcrcvdtcten	otxrcvdtctclkrate_1_0		reserved535	reserved534	reserved533	oneloopbacken

Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

23.8.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA6] + (280h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31:30	29:27	26	25	24	23	22	21:20	19:18	17:16	15:12	11:8	7:4	3:0
Default	0 0	0 0 0	0	0	0	0	0	0 0	0 0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Field	otxclkbypsel_1_0	ofrcdataratefit_2_0	odistxfelbpin	otxclkampbypsn	otxclkampbypsp	reserved539	odfxanamuxen	odfxanamuxsel_1_0	obs_tx_gated_supply_1_0	reserved538	oobsdigselectupn_3_0	oobsdigselectupp_3_0	oobsdigselectdownn_3_0	oobsdigselectdownp_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - dataratefit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - dataratefit must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]

Bit Range	Default & Access	Description
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

23.8.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA6] + (280h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

reserved543	ir2short3_5_0	reserved542	ir2short0_5_0	reserved541	ir1main3_6_0	reserved540	ir1main0_6_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

23.8.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (280h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 00400000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ospare1_1_0		osimmode	ontlmodepin2pin	ofrcdatapathdis	ofrcdatapathen	ofrcdrvbypdis	ofrcdrvbypen	odfttxclkcaptesten	otxdccbyps_l	ofrcnmos32idv_2_0			ofrcpmos32idv_2_0			visa_en	ovisa1_clksel_2_0			ovisa1_lanesel_3_0				ovisa_bypass	ovisa0_clksel_2_0			ovisa0_lanesel_3_0			

Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

23.8.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (280h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved551		reserved550						reserved549		reserved548						reserved547	reserved546							reserved545	reserved544						

Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

23.8.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword16: [Port: 0xA6] + (280h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 00008A00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
reserved554								reserved553								ocurconp0ei_2_0			reserved552	omediumcmpadn_1_0		omediumcmpadp_1_0		ospare3_3_0				ospare2_3_0			

Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

23.9 PCI Express* Lane 1 Electrical Address Map

Table 246. Summary of PCI Express* Lane 1 Electrical Message Bus Registers—0xA6 (Global Offset 400h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 3289	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 3291	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 3292	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 3294	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 3294	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 3295	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 3296	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 3297	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 3298	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 3300	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 3301	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 3302	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 3304	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 3305	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 3306	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 3307	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 3309	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 3310	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 3312	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 3313	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 3314	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 3315	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 3316	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 3316	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 3317	0001C020h

23.9.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA6] + (400h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 00010080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

reg_txcfgchange_valid_delay_3_0
reg_txcfgchange_rst_delay_3_0
reserved500
reg_txcfgchange_width_4_0
reg_txcfgchange_ovrride
reg_tx2_soft_reset_n
reg_txswng_clksel
reg_rcvdetect_ovrd___________________
reg_rcvdetected______________________
reg_rcvdetectfinished________________
reg_rcvdetect_pulse_width_ovrd
reg_rcvdetect_pulse_width_2_0
reg_tx1_soft_reset_n
reg_tx_8b10b_bypass
reg_tx_laneup
reg_left_txfifo_rst_master2
reg_right_txfifo_rst_master2
reg_plllinksynch_ovrden
reg_plllinksynch_ovrd
reg_tx1_cmmdisparity

Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd______________________:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected_________________________:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished__________________:** override for rcvdetectfinished
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass

Bit Range	Default & Access	Description
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

23.9.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA6] + (400h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 00600060h

Bits	Default	Field
31:24	0000 0000	reg_txfsm_4us_delay_7_0
23	0	reg_softreset_enable
22	1	cri_rxeb_eiosenable
21	1	cri_rxdigfiltsq_enable
20	0	reg_txfsm_delay_ovrd
19:16	0000	reg_txfsm_4us_delay_11_8
15:14	00	reg_pclk_rate_1_0
13:12	00	reg_rate_1_0
11:9	000	reg_phymode_2_0
8	0	reg_modeovren
7:6	01	reg_datawidth
5	1	soft_reset_n
4	0	reg_diginelben
3	0	reg_digifelben
2	0	reg_strapgroup_ovrden
1	0	reg_yank_timer_done_b_ovrd
0	0	reg_yank_timer_done_b_ovrd_en

Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down

Bit Range	Default & Access	Description
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

23.9.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword2: [Port: 0xA6] + (400h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	Default	Field
31:28	0000	reg_rxpwrfsm_pibiasoff_delay_3_0
27:24	0000	cri_sqdbexittimer_override_3_0
23:18	000000	cri_sqdbentrytimer_override_5_0
17:16	00	reg_rxdrcgtsqsel_1_0
15	0	cri_reut_SlaveSideDataCheckingEn
14	0	cri_sqdbtimer_ovren
13	0	cri_rxpwrfsm_timer_ovren
12	0	reg_rxidle
11	0	cri_rxrawdata_sel
10	0	cri_dynkalign_eco3302703_mode
9	0	cri_dynkalign_eco3302703_ovren
8	0	reg_rxpwrfsm_pibiasoff_ovrride
7	0	cri_reset_kalignlck
6	0	cri_ebptrrst
5	0	cri_comdispfix
4	0	cri_forcebankhit
3:2	00	cri_kalignmode_1_0
1	0	cri_skpprocdis
0	0	cri_elasticbuffer_maskdis

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode

Bit Range	Default & Access	Description
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

23.9.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA6] + (400h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 5515ACAAh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
cri_dfx_patbuf_55_48	cri_dfx_patbuf_63_56	cri_dfx_patbuf_71_64	cri_dfx_patbuf_79_72

Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.9.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword4: [Port: 0xA6] + (400h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h

Bits	31:24	23:16	15:8	7:0
Default	0 1 0 1 0 1 1 1	0 1 0 1 0 1 0 1	0 1 0 1 0 1 0 1	1 1 0 0 0 0 0 1
Field	cri_dfx_patbuf_23_16	cri_dfx_patbuf_31_24	cri_dfx_patbuf_39_32	cri_dfx_patbuf_47_40

Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.9.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword5: [Port: 0xA6] + (400h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00003E63h

Bits	Default	Field
31	0	cri_dfx_patbuftrain
30:28	0 0 0	cri_dfx_prbspoly_2_0
27:26	0 0	cri_dfx_patbufsize_1_0
25	0	cri_dfx_patbufloop
24	0	cri_dfx_patbufdwidth
23	0	cri_dfx_patbuftrainovr
22	0	cri_dfx_marginmode
21	0	cri_dfx_chk_sel
20	0	cri_dfx_patchken
19	0	cri_dfx_patgenen
18	0	cri_dfx_clrerrcnt
17	0	cri_dfx_lcereset
16	0	cri_dfx_lcestart
15:8	0 0 1 1 1 1 1 0	cri_dfx_patbuf_7_0
7:0	0 1 1 0 0 0 1 1	cri_dfx_patbuf_15_8

Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.9.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword6: [Port: 0xA6] + (400h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: FFFFFFFFh

Bits	31:24	23:16	15:8	7:0
Default	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Field	cri_dfx_prbsseed_7_0	cri_dfx_prbsseed_15_8	cri_dfx_prbsseed_23_16	cri_dfx_prbsseed_31_24

Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

23.9.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword7: [Port: 0xA6] + (400h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000009h

Bits	31:24	23:16	15	14	13	12	11	10	9	8	7	6	5:4	3:0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0 0	1 0 0 1
Field	dfx_cri_errcnt_7_0	dfx_cri_errcnt_15_8	i_rxcaldone	dfx_cri_lcemgnerr	cri_dfx_patgen2active	dfx_cri_patbufallfail	dfx_cri_patchkactive	dfx_cri_patgenactive	dfx_cri_lcetraindone	dfx_cri_lcetrainactive	reserved501	cri_dfx_patgen2en	cri_dfx_maxerrcnt_1_0	cri_dfx_prbstraincnt_3_0

Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

23.9.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword8: [Port: 0xA6] + (400h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 000000C4h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0
reg_partial	reg_slumber	reg_tx2_cdr_override_2_0			reg_cdr_override_2_0			reg_ebuffmode	reg_usedclockchannel_1_0		reg_usedclockchannel_ovrride	reg_gbl_ovrride	reg_tx1_pclkon_inp2	reg_tx2_pclkon_inp2	reg_tx2_txenable	cri_rxeb_ptr_init_3_0				reg_powerfsm_ovrride	reg_suspend	reg_pclkcfginput	reg_useqclock	cri_rxeb_hiwater_3_0				cri_rxeb_lowater_3_0			

Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed

Bit Range	Default & Access	Description
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

23.9.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA6] + (400h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	30:26	25:24	23	22:18	17	16	15	14:13	12:10	9	8	7:6	5	4	3	2	1:0
reserved502	reg_strapgroup_4_0	reg_powerdown_1_0	reg_pcs_txcmnkeepdisable_ovrd	reg_straplane_5_0	reg_tx1_powerdown_override	reg_tx2_powerdown_override	reg_txdatavalid	reg_txdeemp_1_0	reg_txmargin_2_0	reg_txswing	reg_txenable	reg_txterm_vcc_1_0	reg_txdetrxlpbk	reg_txelectidle	reg_txcompliance	reg_txoneszeroes	reg_latencyoptim_1_0
0	0 0 0 0 0	0 0	0	0 0 0 0 0	0	0	0	0 0	0 0 0	0	0	0 0	0	0	0	0	0 0

Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph

Bit Range	Default & Access	Description
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

23.9.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword10: [Port: 0xA6] + (400h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	Default	Field
31:28	0 0 0 0	reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0
27:24	0 0 0 0	reg_rxpwrfsm_timer_ENABLE_RX_3_0
23:20	0 0 0 0	reg_rxpwrfsm_timer_RX_SQEN_3_0
19:16	0 0 0 0	reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0
15:8	0 0 0 0 0 0 0 0	reg_clk_valid_cnt_7_0
7	0	reg_rxterm
6	0	reg_rxpolarity
5	0	reg_rxeqtrain
4	0	reg_rxsquelchen
3	0	cri_rxpwrfsm_sqentimer_ovrden
2	0	reg_rxintfltren_override
1	0	reg_rxintfltren_l
0	0	reg_clk_valid_cnt_ovrd

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

23.9.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword11: [Port: 0xA6] + (400h + 2Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0F000000h

Bit(s)	Default	Field
31:30	0 0	reserved505
29	0	reserved506
28:24	0 1 1 1 1	reg_tx2_stagger_mask_4_0
23	0	i_clkbuf_iclken_ovrd
22	0	i_clkbuf_qclken_ovrd
21	0	reserved503
20	0	i_clkbuf_txclkmuxen_ovrd
19	0	reserved504
18	0	reg_tx2_cmmdisparity
17	0	reg_tx1_ctrl_override
16	0	reg_tx2_ctrl_override
15	0	reg_tx2_txterm_vcc_1
14	0	reg_tx2_txterm_vcc_0
13	0	reg_tx2_txdetrxlpbk
12	0	reg_tx2_txelectidle
11	0	reg_tx2_txcompliance
10	0	reg_tx2_txoneszeroes
9:8	0 0	reg_tx2_powerdown_1_0
7	0	o_captesten_h
6	0	i_captestout
5	0	fuse_override
4	0	i_clkbuf_ibiasen_ovrd
3	0	reg_lanedeskew_strap_ovrd
2	0	reg_lane_reverse
1	0	reg_left_txfifo_rst_master
0	0	reg_right_txfifo_rst_master

Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2

Bit Range	Default & Access	Description
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd______________:** reserved
2	0h RW	**reg_lane_reverse________________________:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____________:** reserved
0	0h RW	**reg_right_txfifo_rst_master___________:** reserved

23.9.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword12: [Port: 0xA6] + (400h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00250F00h

Bits	Default	Field
31	0	reg_txfsm_200ns_ovrd
30:24	0 0 0 0 0 0 0	reg_txfsm_200ns_delay_6_0
23	0	reg_loadgen2txen_fall_ovrd
22:20	0 1 0	reg_tx2_stagger_mult_2_0
19	0	reg_lanestagger_by_group
18:16	1 0 1	reg_tx1_stagger_mult_2_0
15:14	0 0	reserved509
13	0	reserved510
12:8	0 1 1 1 1	reg_tx1_stagger_mask_4_0
7	0	reserved507
6	0	reg_lanestagger_strap_ovrd
5	0	reserved508
4:0	0 0 0 0 0	reg_lanestagger_strap_4_0

Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

23.9.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword13: [Port: 0xA6] + (400h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31	30:29	28:24	23:16	15	14:13	12:8	7:0
Default	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0
Field	visa_en	reserved512	visa_clk_sel1_4_0	visa_lane_sel1_7_0	visa_bypass	reserved511	visa_clk_sel0_4_0	visa_lane_sel0_7_0

Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

23.9.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword14: [Port: 0xA6] + (400h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 007A0018h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bits	Field
31	reg_clkbuf_stagger_ovrd
30	reg_clkbuf_stagger_cnt_10
29	reg_slowclk_ovrden
28:24	reg_txloadgenen2txen_fall_delay_4_0
23:20	o_cmlmuxsthsel_3_0
19:16	o_cmlsthsel_3_0
15:12	o_pcisel_3_0
11:8	o_pcqsel_3_0
7	o_phaseicen
6	o_phaseqcen
5	o_pcbypass
4	o_slowclocken
3	o_sclk250en
2:0	cri_kalign_com_cnt

Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

23.9.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword15: [Port: 0xA6] + (400h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 04100300h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
reg_powermode_del_cfg_fifoptrgen_2_0			reg_clkbuf_en_ovrd	o_deskewen	reserved514	reserved515	reserved516	o_obsselectlocaldown_h	o_obsselectlocalup	o_obsselectm1datadown	o_obsselectm1dataup	o_obsselecttom2_1_0		o_obsselecttom1_1_0		reg_clkbuf_stagger_cnt_1_0		reserved513						reg_clkbuf_stagger_cnt_9_2							

Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

23.9.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA6] + (400h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

Field	Bits	Default bits
squelch_shunt_ovrd_en	31	0
squelch_shunt_cnt_2_0	30:28	0 0 0
reserved520	27	0
i_rxsqfsm_timersel	26	0
i_rxsq_asyncmode_h	25	0
i_rxsquelchstby_h	24	1
reserved519	23:18	0 0 0 0 0 0
cri_dfx_evenoddmask_1_0	17:16	0 0
reserved518	15:12	0 0 0 0
cri_dfx_lce2patsrc_1_0	11:10	0 0
cri_dfx_lcepatsrc_1_0	9:8	0 0
reserved517	7:6	0 0
txloadgen_ctr_val	5:4	0 0
cri_txhighpowerei_ovrden	3	0
cri_tx1highpowerei_ovrdval	2	0
cri_tx2highpowerei_ovrdval	1	0
p2_fast_exit_en	0	1

Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.

Bit Range	Default & Access	Description
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

23.9.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA6] + (400h + 44h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

oirefdfxsel_1_0	iopampsfpen_h	iopampsfnen_h	iopamppen_h	iopampnen_h	monanapgen	monubufbypassen	reserved522	reg_ivrefen	ivrefen_ovrd	reserved523	oirefcurmonsel	lrcdisable	reserved521	lrc_rdy_pulsegen	lrc_rdy_target_1_0	lrc_rdy_ovd	rxtermpmrcen	rxvgapmrcen	txpmrcen	irefpmrcen	rxtermpercen	rxvgaperrcen	txperrcen	irefperrcen

Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode

Bit Range	Default & Access	Description
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

23.9.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA6] + (400h + 48h)

Op Codes:
0h - Read, 1h - Write

Default: 00008080h

Bits	31:27	26	25:24	23:16	15:8	7:0
Default	0 0 0 0 0	0	0 0	0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
Field	reserved524	reg_lrc_calcsonly	adcout_9_8	adcout_7_0	adc2_9_2	adc1_9_2

Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimination filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimination filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

23.9.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA6] + (400h + 4Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00004F10h

31 28 24 20 16 12 8 4 0

iamp0calcode_7_0	cal_num	cal_start	cal_type	cal_inv	cal_rst	calclkdivsel_1_0	reserved525	calib_done	cal_fb_count	adc_acctime_1_0	adc_clksel_1_0	adcmuxsel_2_0	adcstart
0 0 0 0 0 0 0 0	0 0 0 0	0	0	0	0	0 1	0	0	1 1 1 1	0 0	0 1	0 0 0	0

Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [lyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single

Bit Range	Default & Access	Description
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

23.9.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA6] + (400h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

Bits	31:24	23:16	15:8	7:0
Default	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0
Field	rxvgarccode_7_0	rxtermrccode_7_0	txrccode_7_0	irefrccode_7_0

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

23.9.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA6] + (400h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
rxvgarcscale_7_0								rxtermrcscale_7_0								txrcscale_7_0								irefrcscale_7_0							

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

23.9.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword22: [Port: 0xA6] + (400h + 58h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
rxvgarcoffset_7_0	rxtermrcoffset_7_0	txrcoffset_7_0	irefrcoffset_7_0

Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

23.9.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword23: [Port: 0xA6] + (400h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h

31:24	23	22:19	18:16	15:12	11:8	7:4	3:0
0 0 0 0 0 0 0 0	0	0 0 1 1	0 0 0	0 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0
iclkqcfg_spare_7_0	iclkicfg_spare_7	iclkicfg_spare_6_3	iclkicfg_spare_2_0	reserved526	i_drvcfg_3_0	i_ploadcfg_3_0	ipbiasctrl_3_0

Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

23.9.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword24: [Port: 0xA6] + (400h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Field
31:24	reserved528
23:17	reserved527
16	cri_lanereset_clkgatectl
15	cri_lanereqforce
14:10	cri_susclkdisable_delay_4_0
9:8	cri_data_dynclkgate_mode_1_0
7	cri_eios_waittime_ovren
6:0	cri_eios_waittime_6_0

Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved

Bit Range	Default & Access	Description
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (i.e. 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay .... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

23.10 PCI Express* Lane 1 Electrical Address Map

Table 247. Summary of PCI Express* Lane 1 Electrical Message Bus Registers—0xA6 (Global Offset 480h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 3319	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 3320	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 3321	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 3321	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 3323	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 3323	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 3324	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 3325	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 3326	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 3326	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 3327	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 3328	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 3330	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 3331	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 3332	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 3333	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 3334	00008A00h

23.10.1 TX_DWORD0 (tx_dword0)—Offset 0h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA6] + (480h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah

31			28				24				20				16				12				8				4				0
0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0
reserved504	ofrcr1main3_6_0							reserved503	reserved502							reserved501	reserved500							ofrcdrvr1r2	ofrcr1main0_6_0						

Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

23.10.2 TX_DWORD1 (tx_dword1)—Offset 4h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA6] + (480h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h

Bits 31:28	Bits 27:24	Bits 23:20	Bits 19:16	Bits 15:12	Bits 11:8	Bits 7:4	Bits 3:0
0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Field
31:30	reserved510
29:24	ofrcr2short3_5_0
23:22	reserved509
21:16	reserved508
15:14	reserved507
13:8	reserved506
7:6	reserved505
5:0	ofrcr2short0_5_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

23.10.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (480h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 5580983Ah

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	1	1	0	1	0

Fields (bits 31:24) omargin010_7_0; (23:16) omargin000_7_0; (15:8) ouniqtranscale_7_0; (7) reserved511; (6:0) ofrcslices_6_0

Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

23.10.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA6] + (480h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0C782040h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	1	1	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
Field	opisorate8b_h	obeacondivratio	ouniqetrangenmethod_1_0		oscaledcompmethod_1_0		odeemswinggenmethod	odownscaleampmethod	omargin101_7_0								omargin100_7_0								omargin011_7_0							

Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

23.10.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA6] + (480h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 2B404D55h

31			28				24				20				16				12				8				4				0
0	0	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1
ow2tapdeemph9p5_7_0								ow2tapdeemph6p0_7_0								ow2tapgen2deemph3p5_7_0								ow2tapgen1deemph3p5_7_0							

Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

23.10.6 TX_DWORD5 (tx_dword5)—Offset 14h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (480h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ocalcinit	reserved515							reserved514								reserved513								reserved512							

Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

23.10.7 TX_DWORD6 (tx_dword6)—Offset 18h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword6: [Port: 0xA6] + (480h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved520	onswbypass_6_0							reserved519	opswbypass_6_0							reserved518	reserved517							ocalccont	reserved516						

Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively

Bit Range	Default & Access	Description
6:0	0h RO	**reserved516:** reserved

23.10.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword7: [Port: 0xA6] + (480h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	1
reserved527		reserved526			reserved525			reserved524	reserved523	oslrctrlr2_l_2_0			oslrctrlr2_h_2_0			reserved522		oslrctrl_l_2_0			oslrctrl_h_2_0			reserved521		or2bypass_5_0					

Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

23.10.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword8: [Port: 0xA6] + (480h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 0600AA80h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
ontlpdtime_7_0								ofrcdccoup_1_0		obypbycomp	obypdftmode_4_0					odftpisodata1_7_0								odftpisodata0_1_0		reserved529			reserved528		

Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

23.10.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA6] + (480h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00430C06h

31	30	29:27	26:24	23:22	21:20	19:18	17:16	15:8	7:0
0	0	0 0 0	0 0 0	0 1	0 0	0 0	1 1	0 0 0 0 1 1 0 0	0 0 0 0 0 1 1 0
ontlstrongpulling	ontlen	ontllowrefsel_2_0	ontlhighrefsel_2_0	ofrcsatamode_1_0	otxsusclkfreq_1_0	reserved530	orcvdtctrefselnosus_1_0	orcvdtctputime_7_0	ontlputime_7_0

Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

23.10.11 TX_DWORD10 (tx_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword10: [Port: 0xA6] + (480h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ispareread_7_0								reserved532								reserved531						ircvdtctcmpout	idftcaptestsig	idftrcvdetectedtxn	idftrcvdetectedtxp	idftrcvdetectfinished	intlfinished	intlpass_3_0			

Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

23.10.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword11: [Port: 0xA6] + (480h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00001000h

Bits	Default	Field
31:29	0 0 0	oselsparetxclkin_2_0
28:26	0 0 0	ofrcdotprocess_2_0
25	0	ofrcgohighzdis
24	0	ofrcgohighzen
23	0	ofrcstrongpddis
22	0	ofrcstrongpden
21	0	ofrctxclkrootdis
20	0	ofrctxclkrooten
19	0	reserved537
18	0	ofrcpwrmodel1
17	0	ofrcpwrmodel0s
16	0	ofrcpwrmodel0
15	0	ofrccmkeeppadnen
14	0	ofrccmkeeppadpen
13	0	ofrccmkeeppadndis
12	1	ofrccmkeeppadpdis
11	0	omakedeeperfifo
10:8	0 0 0	ofrclatencyoptim_2_0
7	0	reserved536
6	0	ofrcrcvdtcten
5:4	0 0	otxrcvdtctclkrate_1_0
3	0	reserved535
2	0	reserved534
1	0	reserved533
0	0	oneloopbacken

Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.

Bit Range	Default & Access	Description
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

23.10.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword12: [Port: 0xA6] + (480h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	Default	Field
31:30	0 0	otxclkbypsel_1_0
29:27	0 0 0	ofrcdataratefit_2_0
26	0	odistxfelbpin
25	0	otxclkampbypsn
24	0	otxclkampbypsp
23	0	reserved539
22	0	odfxanamuxen
21:20	0 0	odfxanamuxsel_1_0
19:18	0 0	obs_tx_gated_supply_1_0
17:16	0 0	reserved538
15:12	0 0 0 0	oobsdigselectupn_3_0
11:8	0 0 0 0	oobsdigselectupp_3_0
7:4	0 0 0 0	oobsdigselectdownn_3_0
3:0	0 0 0 0	oobsdigselectdownp_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - dataratefit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - dataratefit must be '11'

Bit Range	Default & Access	Description
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

23.10.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword13: [Port: 0xA6] + (480h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:30	reserved543
29:24	ir2short3_5_0
23:22	reserved542
21:16	ir2short0_5_0
15	reserved541
14:8	ir1main3_6_0
7	reserved540
6:0	ir1main0_6_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

23.10.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (480h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 00400000h

Bits	31:30	29	28	27	26	25	24	23	22	21:19	18:16	15	14:12	11:8	7	6:4	3:0
Default	0 0	0	0	0	0	0	0	0	1	0 0 0	0 0 0	0	0 0 0	0 0 0 0	0	0 0 0	0 0 0 0
Field	ospare1_1_0	osimmode	ontlmodepin2pin	ofrcdatapathdis	ofrcdatapathen	ofrcdrvbypdis	ofrcdrvbypen	odfttxclkcaptesten	otxdccbyps_l	ofrcnmos32idv_2_0	ofrcpmos32idv_2_0	visa_en	ovisa1_clksel_2_0	ovisa1_lanesel_3_0	ovisa_bypass	ovisa0_clksel_2_0	ovisa0_lanesel_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers

Bit Range	Default & Access	Description
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

23.10.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (480h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved551		reserved550						reserved549		reserved548						reserved547	reserved546							reserved545	reserved544						

Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

23.10.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword16: [Port: 0xA6] + (480h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 00008A00h

Bits	31:24	23:16	15:13	12	11:10	9:8	7:4	3:0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0	0	1 0	1 0	0 0 0 0	0 0 0 0
Field	reserved554	reserved553	ocurconp0ei_2_0	reserved552	omediumcmpadn_1_0	omediumcmpadp_1_0	ospare3_3_0	ospare2_3_0

Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved

Bit Range	Default & Access	Description
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

23.11 PCI Express* Lane 2 Electrical Address Map

Table 248. Summary of PCI Express* Lane 2 Electrical Message Bus Registers—0xA6 (Global Offset 600h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 3337	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 3339	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 3340	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 3342	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 3342	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 3343	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 3345	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 3345	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 3346	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 3348	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 3349	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 3350	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 3352	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 3353	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 3354	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 3355	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 3357	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 3358	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 3360	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 3361	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 3362	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 3363	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 3364	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 3364	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 3365	0001C020h

23.11.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword0: [Port: 0xA6] + (600h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 00010080h

Bits	31:28	27:24	23	22:18	17	16	15	14	13	12	11	10:8	7	6	5	4	3	2	1	0
Default	0 0 0 0	0 0 0 0	0	0 0 0 0 0	0	1	0	0	0	0	0	0 0 0	1	0	0	0	0	0	0	0
Field	reg_txcfgchange_valid_delay_3_0	reg_txcfgchange_rst_delay_3_0	reserved500	reg_txcfgchange_width_4_0	reg_txcfgchange_ovrride	reg_tx2_soft_reset_n	reg_txswng_clksel	reg_rcvdetect_ovrd	reg_rcvdetected	reg_rcvdetectfinished	reg_rcvdetect_pulse_width_ovrd	reg_rcvdetect_pulse_width_2_0	reg_tx1_soft_reset_n	reg_tx_8b10b_bypass	reg_tx_laneup	reg_left_txfifo_rst_master2	reg_right_txfifo_rst_master2	reg_plllinksynch_ovrden	reg_plllinksynch_ovrd	reg_tx1_cmmdisparity

Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd______________________:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected__________________________:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished___________________:** override for rcvdetectfinished
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass

Bit Range	Default & Access	Description
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

23.11.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA6] + (600h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 00600060h

Bits	Default bits	Field
31:24	0 0 0 0 0 0 0 0	reg_txfsm_4us_delay_7_0
23	0	reg_softreset_enable
22	1	cri_rxeb_eiosenable
21	1	cri_rxdigfiltsq_enable
20	0	reg_txfsm_delay_ovrd
19:16	0 0 0 0	reg_txfsm_4us_delay_11_8
15:14	0 0	reg_pclk_rate_1_0
13:12	0 0	reg_rate_1_0
11:9	0 0 0	reg_phymode_2_0
8	0	reg_modeovren
7:6	0 1	reg_datawidth
5	1	soft_reset_n
4	0	reg_diginelben
3	0	reg_digifelben
2	0	reg_strapgroup_ovrden
1	0	reg_yank_timer_done_b_ovrd
0	0	reg_yank_timer_done_b_ovrd_en

Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down

Bit Range	Default & Access	Description
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

23.11.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword2: [Port: 0xA6] + (600h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reg_rxpwrfsm_pibiasoff_delay_3_0				cri_sqdbexittimer_override_3_0				cri_sqdbentrytimer_override_5_0						reg_rxdrcgtsqsel_1_0		cri_reut_SlaveSideDataCheckingEn	cri_sqdbtimer_ovren	cri_rxpwrfsm_timer_ovren	reg_rxidle	cri_rxrawdata_sel	cri_dynkalign_eco3302703_mode	cri_dynkalign_eco3302703_ovren	reg_rxpwrfsm_pibiasoff_ovrride	cri_reset_kalignlck	cri_ebptrrst	cri_comdispfix	cri_forcebankhit	cri_kalignmode_1_0		cri_skpprocdis	cri_elasticbuffer_maskdis

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode

Bit Range	Default & Access	Description
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

23.11.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA6] + (600h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 5515ACAAh

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
cri_dfx_patbuf_55_48								cri_dfx_patbuf_63_56								cri_dfx_patbuf_71_64								cri_dfx_patbuf_79_72							

Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.11.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword4: [Port: 0xA6] + (600h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h

31:24	23:16	15:8	7:0
0 1 0 1 0 1 1 1	0 1 0 1 0 1 0 1	0 1 0 1 0 1 0 1	1 1 0 0 0 0 0 1
cri_dfx_patbuf_23_16	cri_dfx_patbuf_31_24	cri_dfx_patbuf_39_32	cri_dfx_patbuf_47_40

Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.11.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword5: [Port: 0xA6] + (600h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00003E63h

31	30:28	27:26	25	24	23	22	21	20	19	18	17	16	15:8	7:0
0	0 0 0	0 0	0	0	0	0	0	0	0	0	0	0	0 0 1 1 1 1 1 0	0 1 1 0 0 0 1 1
cri_dfx_patbuftrain	cri_dfx_prbspoly_2_0	cri_dfx_patbufsize_1_0	cri_dfx_patbufloop	cri_dfx_patbufdwidth	cri_dfx_patbuftrainovr	cri_dfx_marginmode	cri_dfx_chk_sel	cri_dfx_patchken	cri_dfx_patgenen	cri_dfx_clrerrcnt	cri_dfx_lcereset	cri_dfx_lcestart	cri_dfx_patbuf_7_0	cri_dfx_patbuf_15_8

Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.11.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA6] + (600h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: FFFFFFFFh

Bits	31:24	23:16	15:8	7:0
Default	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Field	cri_dfx_prbsseed_7_0	cri_dfx_prbsseed_15_8	cri_dfx_prbsseed_23_16	cri_dfx_prbsseed_31_24

Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

23.11.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA6] + (600h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000009h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	dfx_cri_errcnt_7_0
23:16	0 0 0 0 0 0 0 0	dfx_cri_errcnt_15_8
15	0	i_rxcaldone
14	0	dfx_cri_lcemgnerr
13	0	cri_dfx_patgen2active
12	0	dfx_cri_patbufallfail
11	0	dfx_cri_patchkactive
10	0	dfx_cri_patgenactive
9	0	dfx_cri_lcetraindone
8	0	dfx_cri_lcetrainactive
7	0	reserved501
6	0	cri_dfx_patgen2en
5:4	0 0	cri_dfx_maxerrcnt_1_0
3:0	1 0 0 1	cri_dfx_prbstraincnt_3_0

Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

23.11.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword8: [Port: 0xA6] + (600h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 000000C4h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0
reg_partial	reg_slumber	reg_tx2_cdr_override_2_0			reg_cdr_override_2_0			reg_ebuffmode	reg_usedclockchannel_1_0		reg_usedclockchannel_ovrride	reg_gbl_ovrride	reg_tx1_pclkon_inp2	reg_tx2_pclkon_inp2	reg_tx2_txenable	cri_rxeb_ptr_init_3_0				reg_powerfsm_ovrride	reg_suspend	reg_pclkcfginput	reg_useqclock	cri_rxeb_hiwater_3_0				cri_rxeb_lowater_3_0			

Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed

Bit Range	Default & Access	Description
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

23.11.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA6] + (600h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved502, reg_strapgroup_4_0, reg_powerdown_1_0, reg_pcs_txcmnkeepdisable_ovrd, reg_straplane_5_0, reg_tx1_powerdown_override, reg_tx2_powerdown_override, reg_txdatavalid, reg_txdeemp_1_0, reg_txmargin_2_0, reg_txswing, reg_txenable, reg_txterm_vcc_1_0, reg_txdetrxlpbk, reg_txelectidle, reg_txcompliance, reg_txoneszeroes, reg_latencyoptim_1_0

Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph

Bit Range	Default & Access	Description
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

23.11.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword10: [Port: 0xA6] + (600h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	Default	Field
31:28	0 0 0 0	reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0
27:24	0 0 0 0	reg_rxpwrfsm_timer_ENABLE_RX_3_0
23:20	0 0 0 0	reg_rxpwrfsm_timer_RX_SQEN_3_0
19:16	0 0 0 0	reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0
15:8	0 0 0 0 0 0 0 0	reg_clk_valid_cnt_7_0
7	0	reg_rxterm
6	0	reg_rxpolarity
5	0	reg_rxeqtrain
4	0	reg_rxsquelchen
3	0	cri_rxpwrfsm_sqentimer_ovrden
2	0	reg_rxintfltren_override
1	0	reg_rxintfltren_l
0	0	reg_clk_valid_cnt_ovrd

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

23.11.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword11: [Port: 0xA6] + (600h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0F000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved505		reserved506	reg_tx2_stagger_mask_4_0					i_clkbuf_iclken_ovrd	i_clkbuf_qclken_ovrd	reserved503	i_clkbuf_txclkmuxen_ovrd	reserved504	reg_tx2_cmmdisparity	reg_tx1_ctrl_override	reg_tx2_ctrl_override	reg_tx2_txterm_vcc_1	reg_tx2_txterm_vcc_0	reg_tx2_txdetrxlpbk	reg_tx2_txelectidle	reg_tx2_txcompliance	reg_tx2_txoneszeroes	reg_tx2_powerdown_1_0		o_captesten_h	i_captestout	fuse_override	i_clkbuf_ibiasen_ovrd	reg_lanedeskew_strap_ovrd	reg_lane_reverse	reg_left_txfifo_rst_master	reg_right_txfifo_rst_master

Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2

Bit Range	Default & Access	Description
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd______________:** reserved
2	0h RW	**reg_lane_reverse_________________________:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____________:** reserved
0	0h RW	**reg_right_txfifo_rst_master___________:** reserved

23.11.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword12: [Port: 0xA6] + (600h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00250F00h

Bits	Default	Field
31	0	reg_txfsm_200ns_ovrd
30:24	0 0 0 0 0 0 0	reg_txfsm_200ns_delay_6_0
23	0	reg_loadgen2txen_fall_ovrd
22:20	0 1 0	reg_tx2_stagger_mult_2_0
19	0	reg_lanestagger_by_group
18:16	1 0 1	reg_tx1_stagger_mult_2_0
15:14	0 0	reserved509
13	0	reserved510
12:8	0 1 1 1 1	reg_tx1_stagger_mask_4_0
7	0	reserved507
6	0	reg_lanestagger_strap_ovrd
5	0	reserved508
4:0	0 0 0 0 0	reg_lanestagger_strap_4_0

Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

23.11.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA6] + (600h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31	30:29	28:24	23:16	15	14:13	12:8	7:0
Default	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0 0 0 0 0	0 0 0 0 0 0 0 0
Field	visa_en	reserved512	visa_clk_sel1_4_0	visa_lane_sel1_7_0	visa_bypass	reserved511	visa_clk_sel0_4_0	visa_lane_sel0_7_0

Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

23.11.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword14: [Port: 0xA6] + (600h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 007A0018h

Bits	Value	Field
31	0	reg_clkbuf_stagger_ovrd
30	0	reg_clkbuf_stagger_cnt_10
29	0	reg_slowclk_ovrden
28:24	0 0 0 0 0	reg_txloadgenen2txen_fall_delay_4_0
23:20	0 1 1 1	o_cmlmuxsthsel_3_0
19:16	1 0 1 0	o_cmlsthsel_3_0
15:12	0 0 0 0	o_pcisel_3_0
11:8	0 0 0 0	o_pcqsel_3_0
7	0	o_phaseicen
6	0	o_phaseqcen
5	0	o_pcbypass
4	1	o_slowclocken
3	1	o_sclk250en
2:0	0 0 0	cri_kalign_com_cnt

Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

23.11.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA6] + (600h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 04100300h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Field
31:29	reg_powermode_del_cfg_fifoptrgen_2_0
28	reg_clkbuf_en_ovrd
27	o_deskewen
26	reserved514
25	reserved515
24	reserved516
23	o_obsselectlocaldown_h
22	o_obsselectlocalup
21	o_obsselectm1datadown
20	o_obsselectm1dataup
19:18	o_obsselecttom2_1_0
17:16	o_obsselecttom1_1_0
15:14	reg_clkbuf_stagger_cnt_1_0
13:8	reserved513
7:0	reg_clkbuf_stagger_cnt_9_2

Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

23.11.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword16: [Port: 0xA6] + (600h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

Bits	Default	Field
31	0	squelch_shunt_ovrd_en
30:28	0 0 0	squelch_shunt_cnt_2_0
27	0	reserved520
26	0	i_rxsqfsm_timersel
25	0	i_rxsq_asyncmode_h
24	1	i_rxsquelchstby_h
23:18	0 0 0 0 0 0	reserved519
17:16	0 0	cri_dfx_evenoddmask_1_0
15:12	0 0 0 0	reserved518
11:10	0 0	cri_dfx_lce2patsrc_1_0
9:8	0 0	cri_dfx_lcepatsrc_1_0
7:6	0 0	reserved517
5:4	0 0	txloadgen_ctr_val
3	0	cri_txhighpowerei_ovrden
2	0	cri_tx1highpowerei_ovrdval
1	0	cri_tx2highpowerei_ovrdval
0	1	p2_fast_exit_en

Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.

Bit Range	Default & Access	Description
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

23.11.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword17: [Port: 0xA6] + (600h + 44h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

Bits	31:30	29	28	27	26	25	24	23:22	21	20	19:17	16	15	14:12	11	10:9	8	7	6	5	4	3	2	1	0
Default	0 0	0	0	0	0	0	1	0 0	0	0	0 0 0	0	0	0 0 0	0	0 0	0	0	0	0	0	0	0	0	1
Field	oirefdfxsel_1_0	iopampsfpen_h	iopampsfnen_h	iopamppen_h	iopampnen_h	monanapgen	monubufbypassen	reserved522	reg_ivrefen	ivrefen_ovrd	reserved523	oirefcurmonsel	lrcdisable	reserved521	lrc_rdy_pulsegen	lrc_rdy_target_1_0	lrc_rdy_ovd	rxtermpmrcen	rxvgapmrcen	txpmrcen	irefpmrcen	rxtermpercen	rxvgaperrcen	txperrcen	irefpercen

Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode

Bit Range	Default & Access	Description
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

23.11.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword18: [Port: 0xA6] + (600h + 48h)

Op Codes:
0h - Read, 1h - Write

Default: 00008080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Field
31:27	reserved524
26	reg_lrc_calcsonly
25:24	adcout_9_8
23:16	adcout_7_0
15:8	adc2_9_2
7:0	adc1_9_2

Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimination filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimination filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

23.11.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA6] + (600h + 4Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00004F10h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0
iamp0calcode_7_0								cal_num				cal_start	cal_type	cal_inv	cal_rst	calclkdivsel_1_0		reserved525	calib_done	cal_fb_count				adc_acctime_1_0		adc_clksel_1_0		adcmuxsel_2_0			adcstart

Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [lyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single

Bit Range	Default & Access	Description
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

23.11.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA6] + (600h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
rxvgarccode_7_0	rxtermrccode_7_0	txrccode_7_0	irefrccode_7_0

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

23.11.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA6] + (600h + 54h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

rxvgarcscale_7_0	rxtermrcscale_7_0	txrcscale_7_0	irefrcscale_7_0

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

23.11.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA6] + (600h + 58h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	31:24	23:16	15:8	7:0
Value	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	rxvgarcoffset_7_0	rxtermrcoffset_7_0	txrcoffset_7_0	irefrcoffset_7_0

Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

23.11.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA6] + (600h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h

Bits	31:24	23	22:19	18:16	15:12	11:8	7:4	3:0
Value	0 0 0 0 0 0 0 0	0	0 0 1 1	0 0 0	0 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0
Field	iclkqcfg_spare_7_0	iclkicfg_spare_7	iclkicfg_spare_6_3	iclkicfg_spare_2_0	reserved526	i_drvcfg_3_0	i_ploadcfg_3_0	ipbiasctrl_3_0

Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

23.11.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword24: [Port: 0xA6] + (600h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Field
31:24	reserved528
23:17	reserved527
16	cri_lanereset_clkgatectl
15	cri_lanereqforce
14:10	cri_susclkdisable_delay_4_0
9:8	cri_data_dynclkgate_mode_1_0
7	cri_eios_waittime_ovren
6:0	cri_eios_waittime_6_0

Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved

Bit Range	Default & Access	Description
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (i.e. 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay .... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

23.12 PCI Express* Lane 2 Electrical Address Map

Table 249. Summary of PCI Express* Lane 2 Electrical Message Bus Registers—0xA6 (Global Offset 680h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 3367	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 3368	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 3369	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 3369	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 3371	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 3371	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 3372	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 3373	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 3374	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 3374	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 3375	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 3376	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 3378	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 3379	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 3380	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 3381	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 3382	00008A00h

23.12.1 TX_DWORD0 (tx_dword0)—Offset 0h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA6] + (680h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0

Bits	Field
31	reserved504
30:24	ofrcr1main3_6_0
23	reserved503
22:16	reserved502
15	reserved501
14:8	reserved500
7	ofrcdrvr1r2
6:0	ofrcr1main0_6_0

Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

23.12.2 TX_DWORD1 (tx_dword1)—Offset 4h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword1: [Port: 0xA6] + (680h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved510		ofrcr2short3_5_0						reserved509		reserved508						reserved507		reserved506						reserved505		ofrcr2short0_5_0					

Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

23.12.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (680h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 5580983Ah

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	1	1	0	1	0

omargin010_7_0	omargin000_7_0	ouniqtranscale_7_0	reserved511	ofrcslices_6_0

Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

23.12.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA6] + (680h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0C782040h

opisorate8b_h	obeacondivratio	ouniqetrangenmethod_1_0	oscaledcompmethod_1_0	odeemswinggenmethod	odownscaleampmethod	omargin101_7_0	omargin100_7_0	omargin011_7_0
31	30	29:28	27:26	25	24	23:16	15:8	7:0
0	0	0 0	1 1	0	0	0 1 1 1 1 0 0 0	0 0 1 0 0 0 0 0	0 1 0 0 0 0 0 0

Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

23.12.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA6] + (680h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 2B404D55h

31:24	23:16	15:8	7:0
0 0 1 0 1 0 1 1	0 1 0 0 0 0 0 0	0 1 0 0 1 1 0 1	0 1 0 1 0 1 0 1
ow2tapdeemph9p5_7_0	ow2tapdeemph6p0_7_0	ow2tapgen2deemph3p5_7_0	ow2tapgen1deemph3p5_7_0

Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

23.12.6 TX_DWORD5 (tx_dword5)—Offset 14h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (680h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	30:24	23:16	15:8	7:0
0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
ocalcinit	reserved515	reserved514	reserved513	reserved512

Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

23.12.7 TX_DWORD6 (tx_dword6)—Offset 18h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword6: [Port: 0xA6] + (680h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved520	onswbypass_6_0							reserved519	opswbypass_6_0							reserved518	reserved517							ocalccont	reserved516						

Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively

Bit Range	Default & Access	Description
6:0	0h RO	**reserved516:** reserved

23.12.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA6] + (680h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	1

reserved527 | reserved526 | reserved525 | reserved524 | reserved523 | oslrctrlr2_l_2_0 | oslrctrlr2_h_2_0 | reserved522 | oslrctrl_l_2_0 | oslrctrl_h_2_0 | reserved521 | or2bypass_5_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

23.12.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword8: [Port: 0xA6] + (680h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 0600AA80h

Bits	31:24	23:22	21	20:16	15:8	7:6	5:3	2:0
Value	0 0 0 0 0 1 1 0	0 0	0	0 0 0 0 0	1 0 1 0 1 0 1 0	1 0	0 0 0	0 0 0
Field	ontlpdtime_7_0	ofrcdccoup_1_0	obypbycomp	obypdftmode_4_0	odftpisodata1_7_0	odftpisodata0_1_0	reserved529	reserved528

Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

23.12.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword9: [Port: 0xA6] + (680h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00430C06h

31	30	29:27	26:24	23:22	21:20	19:18	17:16	15:8	7:0
0	0	000	000	01	00	00	11	0000 1100	0000 0110
ontlstrongpulling	ontlen	ontllowrefsel_2_0	ontlhighrefsel_2_0	ofrcsatamode_1_0	otxsusclkfreq_1_0	reserved530	orcvdtctrefselnosus_1_0	orcvdtctputime_7_0	ontlputime_7_0

Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

23.12.11 TX_DWORD10 (tx_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword10: [Port: 0xA6] + (680h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

isparereread_7_0	reserved532	reserved531	ircvdtctcmpout	idftcaptestsig	idftrcvdetectedtxn	idftrcvdetectedtxp	idftrcvdetectfinished	intlfinished	intlpass_3_0

Bit Range	Default & Access	Description
31:24	X RO	**isparereread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

23.12.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword11: [Port: 0xA6] + (680h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00001000h

Bits	Default	Field
31:29	000	oselsparetxclkin_2_0
28:26	000	ofrcdotprocess_2_0
25	0	ofrcgohighzdis
24	0	ofrcgohighzen
23	0	ofrcstrongpddis
22	0	ofrcstrongpden
21	0	ofrctxclkrootdis
20	0	ofrctxclkrooten
19	0	reserved537
18	0	ofrcpwrmodel1
17	0	ofrcpwrmodel0s
16	0	ofrcpwrmodel0
15	0	ofrccmkeeppadnen
14	0	ofrccmkeeppadpen
13	0	ofrccmkeeppadndis
12	1	ofrccmkeeppadpdis
11	0	omakedeeperfifo
10:8	000	ofrclatencyoptim_2_0
7	0	reserved536
6	0	ofrcrcvdtcten
5:4	00	otxrcvdtctclkrate_1_0
3	0	reserved535
2	0	reserved534
1	0	reserved533
0	0	oneloopbacken

Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.

Bit Range	Default & Access	Description
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

23.12.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword12: [Port: 0xA6] + (680h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

otxclkbypsel_1_0	ofrcdataratefit_2_0	odistxfelbpin	otxclkampbypsn	otxclkampbypsp	reserved539	odfxanamuxen	odfxanamuxsel_1_0	obs_tx_gated_supply_1_0	reserved538	oobsdigselectupn_3_0	oobsdigselectupp_3_0	oobsdigselectdownn_3_0	oobsdigselectdownp_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - dataratefit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - dataratefit must be '11'

Bit Range	Default & Access	Description
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

23.12.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA6] + (680h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved543		ir2short3_5_0						reserved542		ir2short0_5_0						reserved541	ir1main3_6_0							reserved540	ir1main0_6_0						

Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

23.12.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (680h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 00400000h

Bits	Default	Field
31:30	0 0	ospare1_1_0
29	0	osimmode
28	0	ontlmodepin2pin
27	0	ofrcdatapathdis
26	0	ofrcdatapathen
25	0	ofrcdrvbypdis
24	0	ofrcdrvbypen
23	0	odfttxclkcaptesten
22	1	otxdccbyps_l
21:19	0 0 0	ofrcnmos32idv_2_0
18:16	0 0 0	ofrcpmos32idv_2_0
15	0	visa_en
14:12	0 0 0	ovisa1_clksel_2_0
11:8	0 0 0 0	ovisa1_lanesel_3_0
7	0	ovisa_bypass
6:4	0 0 0	ovisa0_clksel_2_0
3:0	0 0 0 0	ovisa0_lanesel_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers

Bit Range	Default & Access	Description
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

23.12.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (680h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved551		reserved550						reserved549		reserved548						reserved547	reserved546							reserved545	reserved544						

Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

23.12.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword16: [Port: 0xA6] + (680h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 00008A00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
reserved554								reserved553								ocurconp0ei_2_0			reserved552	omediumcmpadn_1_0		omediumcmpadp_1_0		ospare3_3_0				ospare2_3_0			

Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved

Bit Range	Default & Access	Description
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

23.13 PCI Express* Lane 3 Electrical Address Map

Table 250. Summary of PCI Express* Lane 3 Electrical Message Bus Registers—0xA6 (Global Offset 800h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 3385	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 3387	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 3388	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 3390	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 3390	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 3391	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 3393	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 3393	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 3394	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 3396	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 3397	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 3398	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 3400	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 3401	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 3402	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 3403	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 3405	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 3406	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 3408	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 3409	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 3410	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 3411	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 3412	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 3412	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 3413	0001C020h

23.13.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA6] + (800h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 00010080h

31:28	27:24	23	22:18	17	16	15	14	13	12	11	10:8	7	6	5	4	3	2	1	0
0 0 0 0	0 0 0 0	0	0 0 0 0 0	0	1	0	0	0	0	0	0 0 0	1	0	0	0	0	0	0	0
reg_txcfgchange_valid_delay_3_0	reg_txcfgchange_rst_delay_3_0	reserved500	reg_txcfgchange_width_4_0	reg_txcfgchange_ovrride	reg_tx2_soft_reset_n	reg_txswng_clksel	reg_rcvdetect_ovrd___	reg_rcvdetected___	reg_rcvdetectfinished___	reg_rcvdetect_pulse_width_ovrd	reg_rcvdetect_pulse_width_2_0	reg_tx1_soft_reset_n	reg_tx_8b10b_bypass	reg_tx_laneup	reg_left_txfifo_rst_master2	reg_right_txfifo_rst_master2	reg_plllinksynch_ovrden	reg_plllinksynch_ovrd	reg_tx1_cmmdisparity

Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd________________________:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected___________________________:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished____________________:** override for rcvdetectfinished
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass

Bit Range	Default & Access	Description
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

23.13.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA6] + (800h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 00600060h

Bits	Default	Field
31:24	0000 0000	reg_txfsm_4us_delay_7_0
23	0	reg_softreset_enable
22	1	cri_rxeb_eiosenable
21	1	cri_rxdigfiltsq_enable
20	0	reg_txfsm_delay_ovrd
19:16	0000	reg_txfsm_4us_delay_11_8
15:14	00	reg_pclk_rate_1_0
13:12	00	reg_rate_1_0
11:9	000	reg_phymode_2_0
8	0	reg_modeovren
7:6	01	reg_datawidth
5	1	soft_reset_n
4	0	reg_diginelben
3	0	reg_digifelben
2	0	reg_strapgroup_ovrden
1	0	reg_yank_timer_done_b_ovrd
0	0	reg_yank_timer_done_b_ovrd_en

Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down

Bit Range	Default & Access	Description
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

23.13.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword2: [Port: 0xA6] + (800h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reg_rxpwrfsm_pibiasoff_delay_3_0	cri_sqdbexittimer_override_3_0	cri_sqdbentrytimer_override_5_0	reg_rxdrcgtsqsel_1_0	cri_reut_SlaveSideDataCheckingEn	cri_sqdbtimer_ovren	cri_rxpwrfsm_timer_ovren	reg_rxidle	cri_rxrawdata_sel	cri_dynkalign_eco3302703_mode	cri_dynkalign_eco3302703_ovren	reg_rxpwrfsm_pibiasoff_ovrride	cri_reset_kalignlck	cri_ebptrrst	cri_comdispfix	cri_forcebankhit	cri_kalignmode_1_0	cri_skpprocdis	cri_elasticbuffer_maskdis

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode

Bit Range	Default & Access	Description
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

23.13.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA6] + (800h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 5515ACAAh

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
cri_dfx_patbuf_55_48								cri_dfx_patbuf_63_56								cri_dfx_patbuf_71_64								cri_dfx_patbuf_79_72							

Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.13.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword4: [Port: 0xA6] + (800h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 1 0 1	0 1 1 1	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	1 1 0 0	0 0 0 1

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
cri_dfx_patbuf_23_16	cri_dfx_patbuf_31_24	cri_dfx_patbuf_39_32	cri_dfx_patbuf_47_40

Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.13.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword5: [Port: 0xA6] + (800h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00003E63h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	1 1 1 0	0 1 1 0	0 0 1 1

Bits	Field
31	cri_dfx_patbuftrain
30:28	cri_dfx_prbspoly_2_0
27:26	cri_dfx_patbufsize_1_0
25	cri_dfx_patbufloop
24	cri_dfx_patbufdwidth
23	cri_dfx_patbuftrainovr
22	cri_dfx_marginmode
21	cri_dfx_chk_sel
20	cri_dfx_patchken
19	cri_dfx_patgenen
18	cri_dfx_clrerrcnt
17	cri_dfx_lcereset
16	cri_dfx_lcestart
15:8	cri_dfx_patbuf_7_0
7:0	cri_dfx_patbuf_15_8

Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

23.13.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA6] + (800h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: FFFFFFFFh

Bits	31:24	23:16	15:8	7:0
Default	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Field	cri_dfx_prbsseed_7_0	cri_dfx_prbsseed_15_8	cri_dfx_prbsseed_23_16	cri_dfx_prbsseed_31_24

Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

23.13.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA6] + (800h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000009h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	dfx_cri_errcnt_7_0
23:16	0 0 0 0 0 0 0 0	dfx_cri_errcnt_15_8
15	0	i_rxcaldone
14	0	dfx_cri_lcemgnerr
13	0	cri_dfx_patgen2active
12	0	dfx_cri_patbufallfail
11	0	dfx_cri_patchkactive
10	0	dfx_cri_patgenactive
9	0	dfx_cri_lcetraindone
8	0	dfx_cri_lcetrainactive
7	0	reserved501
6	0	cri_dfx_patgen2en
5:4	0 0	cri_dfx_maxerrcnt_1_0
3:0	1 0 0 1	cri_dfx_prbstraincnt_3_0

Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

23.13.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA6] + (800h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 000000C4h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0
reg_partial	reg_slumber	reg_tx2_cdr_override_2_0			reg_cdr_override_2_0			reg_ebuffmode	reg_usedclockchannel_1_0		reg_usedclockchannel_ovrride	reg_gbl_ovrride	reg_tx1_pclkon_inp2	reg_tx2_pclkon_inp2	reg_tx2_txenable	cri_rxeb_ptr_init_3_0				reg_powerfsm_ovrride	reg_suspend	reg_pclkcfginput	reg_useqclock	cri_rxeb_hiwater_3_0				cri_rxeb_lowater_3_0			

Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed

Bit Range	Default & Access	Description
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

23.13.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword9: [Port: 0xA6] + (800h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

reserved502 | reg_strapgroup_4_0 | reg_powerdown_1_0 | reg_pcs_txcmnkeepdisable_ovrd | reg_straplane_5_0 | reg_tx1_powerdown_override | reg_tx2_powerdown_override | reg_txdatavalid | reg_txdeemp_1_0 | reg_txmargin_2_0 | reg_txswing | reg_txenable | reg_txterm_vcc_1_0 | reg_txdetrxlpbk | reg_txelectidle | reg_txcompliance | reg_txoneszeroes | reg_latencyoptim_1_0

Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph

Bit Range	Default & Access	Description
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

23.13.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword10: [Port: 0xA6] + (800h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	Default	Field
31:28	0 0 0 0	reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0
27:24	0 0 0 0	reg_rxpwrfsm_timer_ENABLE_RX_3_0
23:20	0 0 0 0	reg_rxpwrfsm_timer_RX_SQEN_3_0
19:16	0 0 0 0	reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0
15:8	0 0 0 0 0 0 0 0	reg_clk_valid_cnt_7_0
7	0	reg_rxterm
6	0	reg_rxpolarity
5	0	reg_rxeqtrain
4	0	reg_rxsquelchen
3	0	cri_rxpwrfsm_sqentimer_ovrden
2	0	reg_rxintfltren_override
1	0	reg_rxintfltren_l
0	0	reg_clk_valid_cnt_ovrd

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

23.13.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword11: [Port: 0xA6] + (800h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0F000000h

Bits	31:30	29	28:24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9:8	7	6	5	4	3	2	1	0
Default	0 0	0	0 1 1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0
Field	reserved505	reserved506	reg_tx2_stagger_mask_4_0	i_clkbuf_iclken_ovrd	i_clkbuf_qclken_ovrd	reserved503	i_clkbuf_txclkmuxen_ovrd	reserved504	reg_tx2_cmmdisparity	reg_tx1_ctrl_override	reg_tx2_ctrl_override	reg_tx2_txterm_vcc_1	reg_tx2_txterm_vcc_0	reg_tx2_txdetrxlpbk	reg_tx2_txelectidle	reg_tx2_txcompliance	reg_tx2_txoneszeroes	reg_tx2_powerdown_1_0	o_captesten_h	i_captestout	fuse_override	i_clkbuf_ibiasen_ovrd	reg_lanedeskew_strap_ovrd	reg_lane_reverse	reg_left_txfifo_rst_master	reg_right_txfifo_rst_master

Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2

Bit Range	Default & Access	Description
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd______________:** reserved
2	0h RW	**reg_lane_reverse_________________________:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____________:** reserved
0	0h RW	**reg_right_txfifo_rst_master___________:** reserved

23.13.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword12: [Port: 0xA6] + (800h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00250F00h

Bits	Default	Field
31	0	reg_txfsm_200ns_ovrd
30:24	0 0 0 0 0 0 0	reg_txfsm_200ns_delay_6_0
23	0	reg_loadgen2txen_fall_ovrd
22:20	0 1 0	reg_tx2_stagger_mult_2_0
19	0	reg_lanestagger_by_group
18:16	1 0 1	reg_tx1_stagger_mult_2_0
15:14	0 0	reserved509
13	0	reserved510
12:8	0 1 1 1 1	reg_tx1_stagger_mask_4_0
7	0	reserved507
6	0	reg_lanestagger_strap_ovrd
5	0	reserved508
4:0	0 0 0 0 0	reg_lanestagger_strap_4_0

Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

23.13.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

Type: Message Bus Register
(Size: 32 bits)

pcs_dword13: [Port: 0xA6] + (800h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	visa_en
30:29	reserved512
28:24	visa_clk_sel1_4_0
23:16	visa_lane_sel1_7_0
15	visa_bypass
14:13	reserved511
12:8	visa_clk_sel0_4_0
7:0	visa_lane_sel0_7_0

Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

23.13.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword14: [Port: 0xA6] + (800h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 007A0018h

Bits	Value	Field
31	0	reg_clkbuf_stagger_ovrd
30	0	reg_clkbuf_stagger_cnt_10
29	0	reg_slowclk_ovrden
28:24	0 0 0 0 0	reg_txloadgenen2txen_fall_delay_4_0
23:20	0 1 1 1	o_cmlmuxsthsel_3_0
19:16	1 0 1 0	o_cmlsthsel_3_0
15:12	0 0 0 0	o_pcisel_3_0
11:8	0 0 0 0	o_pcqsel_3_0
7	0	o_phaseicen
6	0	o_phaseqcen
5	0	o_pcbypass
4	1	o_slowclocken
3	1	o_sclk250en
2:0	0 0 0	cri_kalign_com_cnt

Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

23.13.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA6] + (800h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 04100300h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Field
31:29	reg_powermode_del_cfg_fifoptrgen_2_0
28	reg_clkbuf_en_ovrd
27	o_deskewen
26	reserved514
25	reserved515
24	reserved516
23	o_obsselectlocaldown_h
22	o_obsselectlocalup
21	o_obsselectm1datadown
20	o_obsselectm1dataup
19:18	o_obsselecttom2_1_0
17:16	o_obsselecttom1_1_0
15:14	reg_clkbuf_stagger_cnt_1_0
13:8	reserved513
7:0	reg_clkbuf_stagger_cnt_9_2

Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.

Bit Range	Default & Access	Description
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

23.13.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA6] + (800h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

Bits	Default	Field
31	0	squelch_shunt_ovrd_en
30:28	000	squelch_shunt_cnt_2_0
27	0	reserved520
26	0	i_rxsqfsm_timersel
25	0	i_rxsq_asyncmode_h
24	1	i_rxsquelchstby_h
23:18	000000	reserved519
17:16	00	cri_dfx_evenoddmask_1_0
15:12	0000	reserved518
11:10	00	cri_dfx_lce2patsrc_1_0
9:8	00	cri_dfx_lcepatsrc_1_0
7:6	00	reserved517
5:4	00	txloadgen_ctr_val
3	0	cri_txhighpowerei_ovrden
2	0	cri_tx1highpowerei_ovrdval
1	0	cri_tx2highpowerei_ovrdval
0	1	p2_fast_exit_en

Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.

Bit Range	Default & Access	Description
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

23.13.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA6] + (800h + 44h)

Op Codes:
0h - Read, 1h - Write

Default: 01000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
oirefdfxsel_1_0		iopampsfpen_h	iopampsfnen_h	iopamppen_h	iopampnen_h	monanapgen	monubufbypassen	reserved522		reg_ivrefen	ivrefen_ovrd	reserved523			oirefcurmonsel	lrcdisable	reserved521			lrc_rdy_pulsegen	lrc_rdy_target_1_0		lrc_rdy_ovd	rxtermpmrcen	rxvgapmrcen	txpmrcen	irefpmrcen	rxtermpercen	rxvgaperrcen	txperrcen	irefpercen

Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode

Bit Range	Default & Access	Description
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

23.13.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA6] + (800h + 48h)

Op Codes:
0h - Read, 1h - Write

Default: 00008080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits 31:27	Bit 26	Bits 25:24	Bits 23:16	Bits 15:8	Bits 7:0
reserved524	reg_lrc_calcsonly	adcout_9_8	adcout_7_0	adc2_9_2	adc1_9_2

Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimination filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimination filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

23.13.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA6] + (800h + 4Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00004F10h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0
iamp0calcode_7_0								cal_num				cal_start	cal_type	cal_inv	cal_rst	calclkdivsel_1_0		reserved525	calib_done	cal_fb_count				adc_acctime_1_0		adc_clksel_1_0		adcmuxsel_2_0			adcstart

Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [lyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single

Bit Range	Default & Access	Description
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

23.13.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA6] + (800h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h

31			28				24				20				16				12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
rxvgarccode_7_0								rxtermrccode_7_0								txrccode_7_0								irefrccode_7_0							

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

23.13.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA6] + (800h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
rxvgarcscale_7_0								rxtermrcscale_7_0								txrcscale_7_0								irefrcscale_7_0							

Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

23.13.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA6] + (800h + 58h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
rxvgarcoffset_7_0	rxtermrcoffset_7_0	txrcoffset_7_0	irefrcoffset_7_0

Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

23.13.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA6] + (800h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h

31:24	23	22:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0 0 0 0 0	0	0 0 1	1 0 0 0	0 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0
iclkqcfg_spare_7_0	iclkicfg_spare_7	iclkicfg_spare_6_3	iclkicfg_spare_2_0	reserved526	i_drvcfg_3_0	i_ploadcfg_3_0	ipbiasctrl_3_0

Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

23.13.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword24: [Port: 0xA6] + (800h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits 31:24	Bits 23:17	Bit 16	Bit 15	Bits 14:10	Bits 9:8	Bit 7	Bits 6:0
reserved528	reserved527	cri_lanereset_clkgatectl	cri_lanereqforce	cri_susclkdisable_delay_4_0	cri_data_dynclkgate_mode_1_0	cri_eios_waittime_ovren	cri_eios_waittime_6_0

Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved

Bit Range	Default & Access	Description
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (i.e. 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay .... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

23.14 PCI Express* Lane 3 Electrical Address Map

Table 251. Summary of PCI Express* Lane 3 Electrical Message Bus Registers—0xA6 (Global Offset 880h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 3415	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 3416	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 3417	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 3417	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 3419	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 3419	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 3420	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 3421	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 3422	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 3422	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 3423	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 3424	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 3426	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 3427	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 3428	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 3429	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 3430	00008A00h

23.14.1 TX_DWORD0 (tx_dword0)—Offset 0h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA6] + (880h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah

31			28				24				20				16				12				8				4				0
0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0
reserved504	ofrcr1main3_6_0							reserved503	reserved502							reserved501	reserved500							ofrcdrvr1r2	ofrcr1main0_6_0						

Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

23.14.2 TX_DWORD1 (tx_dword1)—Offset 4h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA6] + (880h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields (bit 31 to bit 0): reserved510, ofrcr2short3_5_0, reserved509, reserved508, reserved507, reserved506, reserved505, ofrcr2short0_5_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

23.14.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (880h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 5580983Ah

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	1	1	0	1	0
omargin010_7_0								omargin000_7_0								ouniqtranscale_7_0								reserved511	ofrcslices_6_0						

Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

23.14.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA6] + (880h + Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0C782040h

31			28				24				20				16				12				8				4				0
0	0	0	0	1	1	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0

opisorate8b_h	obeacondivratio	ouniqetrangenmethod_1_0	oscaledcompmethod_1_0	odeemswinggenmethod	odownscaleampmethod	omargin101_7_0	omargin100_7_0	omargin011_7_0

Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

23.14.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA6] + (880h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 2B404D55h

31			28				24				20				16				12				8				4				0
0	0	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
ow2tapdeemph9p5_7_0	ow2tapdeemph6p0_7_0	ow2tapgen2deemph3p5_7_0	ow2tapgen1deemph3p5_7_0

Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

23.14.6 TX_DWORD5 (tx_dword5)—Offset 14h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (880h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 31	Bits 30:24	Bits 23:16	Bits 15:8	Bits 7:0
ocalcinit	reserved515	reserved514	reserved513	reserved512

Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

23.14.7 TX_DWORD6 (tx_dword6)—Offset 18h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword6: [Port: 0xA6] + (880h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved520	onswbypass_6_0							reserved519	opswbypass_6_0							reserved518	reserved517							ocalccont	reserved516						

Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively

Bit Range	Default & Access	Description
6:0	0h RO	**reserved516:** reserved

23.14.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword7: [Port: 0xA6] + (880h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	1

reserved527	reserved526	reserved525	reserved524	reserved523	oslrctrlr2_l_2_0	oslrctrlr2_h_2_0	reserved522	oslrctrl_l_2_0	oslrctrl_h_2_0	reserved521	or2bypass_5_0

Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

23.14.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword8: [Port: 0xA6] + (880h + 20h)

Op Codes:
0h - Read, 1h - Write

Default: 0600AA80h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
ontlpdtime_7_0								ofrcdccoup_1_0		obypbycomp	obypdftmode_4_0					odftpisodata1_7_0								odftpisodata0_1_0		reserved529			reserved528		

Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

23.14.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA6] + (880h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00430C06h

31	30	29:27	26:24	23:22	21:20	19:18	17:16	15:8	7:0
0	0	0 0 0	0 0 0	0 1	0 0	0 0	1 1	0 0 0 0 1 1 0 0	0 0 0 0 0 1 1 0
ontlstrongpulling	ontlen	ontllowrefsel_2_0	ontlhighrefsel_2_0	ofrcsatamode_1_0	otxsusclkfreq_1_0	reserved530	orcvdtctrefselnosus_1_0	orcvdtctputime_7_0	ontlputime_7_0

Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

23.14.11 TX_DWORD10 (tx_dword10)—Offset 28h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword10: [Port: 0xA6] + (880h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits 31:24	Bits 23:16	Bits 15:10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bits 3:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	0	0	0	0	0	0 0 0 0
ispareread_7_0	reserved532	reserved531	ircvdtctcmpout	idftcaptestsig	idftrcvdetectedtxn	idftrcvdetectedtxp	idftrcvdetectfinished	intlfinished	intlpass_3_0

Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

23.14.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA6] + (880h + 2Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00001000h

Bits	Default	Field
31:29	0 0 0	oselsparetxclkin_2_0
28:26	0 0 0	ofrcdotprocess_2_0
25	0	ofrcgohighzdis
24	0	ofrcgohighzen
23	0	ofrcstrongpddis
22	0	ofrcstrongpden
21	0	ofrctxclkrootdis
20	0	ofrctxclkrooten
19	0	reserved537
18	0	ofrcpwrmodel1
17	0	ofrcpwrmodel0s
16	0	ofrcpwrmodel0
15	0	ofrccmkeeppadnen
14	0	ofrccmkeeppadpen
13	0	ofrccmkeeppadndis
12	1	ofrccmkeeppadpdis
11	0	omakedeeperfifo
10:8	0 0 0	ofrclatencyoptim_2_0
7	0	reserved536
6	0	ofrcrcvdtcten
5:4	0 0	otxrcvdtctclkrate_1_0
3	0	reserved535
2	0	reserved534
1	0	reserved533
0	0	oneloopbacken

Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.

Bit Range	Default & Access	Description
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

23.14.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword12: [Port: 0xA6] + (880h + 30h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

Bits	Default	Field
31:30	0 0	otxclkbypsel_1_0
29:27	0 0 0	ofrcdataratefit_2_0
26	0	odistxfelbpin
25	0	otxclkampbypsn
24	0	otxclkampbypsp
23	0	reserved539
22	0	odfxanamuxen
21:20	0 0	odfxanamuxsel_1_0
19:18	0 0	obs_tx_gated_supply_1_0
17:16	0 0	reserved538
15:12	0 0 0 0	oobsdigselectupn_3_0
11:8	0 0 0 0	oobsdigselectupp_3_0
7:4	0 0 0 0	oobsdigselectdownn_3_0
3:0	0 0 0 0	oobsdigselectdownp_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - dataratefit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - dataratefit must be '11'

Bit Range	Default & Access	Description
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

23.14.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

Type: Message Bus Register
(Size: 32 bits)

tx_dword13: [Port: 0xA6] + (880h + 34h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved543		ir2short3_5_0						reserved542		ir2short0_5_0						reserved541	ir1main3_6_0							reserved540	ir1main0_6_0						

Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

23.14.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (880h + 38h)

Op Codes:
0h - Read, 1h - Write

Default: 00400000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:30	ospare1_1_0
29	osimmode
28	ontlmodepin2pin
27	ofrcdatapathdis
26	ofrcdatapathen
25	ofrcdrvbypdis
24	ofrcdrvbypen
23	odfttxclkcaptesten
22	otxdccbyps_l
21:19	ofrcnmos32idv_2_0
18:16	ofrcpmos32idv_2_0
15	visa_en
14:12	ovisa1_clksel_2_0
11:8	ovisa1_lanesel_3_0
7	ovisa_bypass
6:4	ovisa0_clksel_2_0
3:0	ovisa0_lanesel_3_0

Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers

Bit Range	Default & Access	Description
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

23.14.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (880h + 3Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:30	reserved551
29:24	reserved550
23:22	reserved549
21:16	reserved548
15	reserved547
14:8	reserved546
7	reserved545
6:0	reserved544

Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

23.14.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword16: [Port: 0xA6] + (880h + 40h)

Op Codes:
0h - Read, 1h - Write

Default: 00008A00h

Bits	31:24	23:16	15:13	12	11:10	9:8	7:4	3:0
Value	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 0 0	0	1 0	1 0	0 0 0 0	0 0 0 0
Field	reserved554	reserved553	ocurconp0ei_2_0	reserved552	omediumcmpadn_1_0	omediumcmpadp_1_0	ospare3_3_0	ospare2_3_0

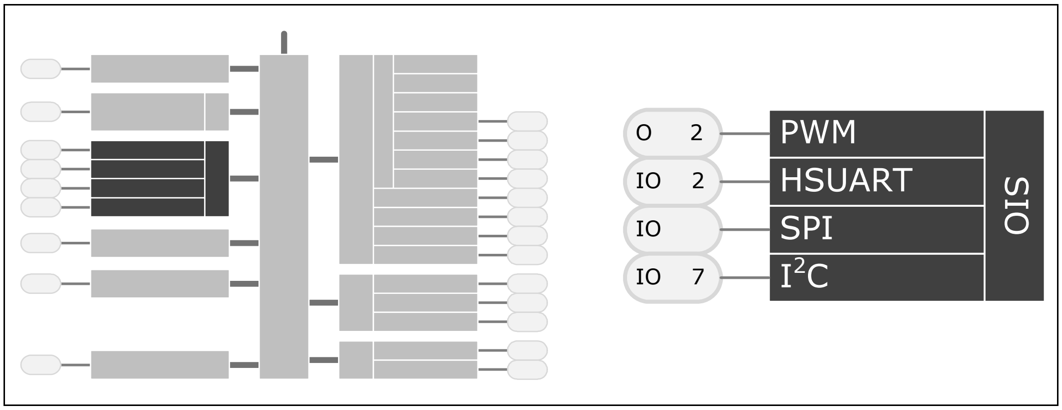
Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved

Bit Range	Default & Access	Description
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

24 Serial IO (SIO) Overview

The Serial I/O (SIO) is a collection of hardware blocks that implement simple but key serial I/O interfaces for platform usage. These hardware blocks include:

- SIO - I²C Interface
- SIO – High Speed UART
- SIO - Serial Peripheral Interface (SPI)
- SIO – Pulse Width Modulation (PWM)



24.1 Serial I/O (SIO) Register Map

Refer to Chapter 3, “Register Access Methods” and Chapter 4, “Mapping Address Spaces” for additional information.

§

24.2 SIO DMA PCI Configuration Registers for SPI, HSUART, PWM

Table 252. Summary of DMA 1 PCI Configuration Registers—0/30/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3433	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3434	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3435	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3435	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 3436	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3437	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3437	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3438	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3438	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3439	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3439	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3440	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 3441	00000000h

24.2.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

24.2.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:0] + 4h

Default: 00100000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

24.2.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:0] + 8h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
CLASS_CODES						RID	

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

24.2.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:0] + Ch

Default: 00800000h

31:24	23	22:16	15:8	7:0
0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

24.2.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 10h

Default: 00000000h

31:12	11:4	3	2:1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0
BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

24.2.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR1																				SIZEINDICATOR1								PREFETCHABLE1	TYPE1		MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

24.2.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

24.2.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
EXPANSION_ROM_BASE																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

24.2.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 34h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:8	Bits 7:0
Reserved0	CAPPTR_POWER

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

24.2.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:0] + 3Ch

Default: 00000100h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	

Bits 31:24	Bits 23:16	Bits 15:12	Bits 11:8	Bits 7:0
MAX_LAT	MIN_GNT	Reserved0	INTPIN	INTLINE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

24.2.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:0] + 80h

Default: 00030001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

24.2.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:0] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

24.2.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

24.3 SIO DMA Memory Mapped I/O Registers for SPI, HSUART, PWM

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Source Address Register for Channel 0 - Low (SAR0_LO)—Offset 0h" on page 3451	00000000h
4–7h	4	"Source Address Register for Channel 0 - High (SAR0_HI)—Offset 4h" on page 3452	00000000h
8–Bh	4	"Destination Address Register for Channel 0 - Low (DAR0_LO)—Offset 8h" on page 3452	00000000h
C–Fh	4	"Destination Address Register for Channel 0 - High (DAR0_HI)—Offset Ch" on page 3453	00000000h
10–13h	4	"Linked List Pointer Register for Channel 0 - Low (LLP0_LO)—Offset 10h" on page 3453	00000000h
14–17h	4	"Linked List Pointer Register for Channel 0 - High (LLP0_HI)—Offset 14h" on page 3454	00000000h
18–1Bh	4	"Control Register for Channel 0 - Low (CTL0_LO)—Offset 18h" on page 3454	00304801h
1C–1Fh	4	"Control Register for Channel 0 - High (CTL0_HI)—Offset 1Ch" on page 3456	00000002h
20–23h	4	"Source Status Register for Channel 0 - Low (SSTAT0_LO)—Offset 20h" on page 3457	00000000h
24–27h	4	"Source Status Register for Channel 0 - High (SSTAT0_HI)—Offset 24h" on page 3457	00000000h
28–2Bh	4	"Dest Status Register for Channel 0 - Low (DSTAT0_LO)—Offset 28h" on page 3458	00000000h
2C–2Fh	4	"Dest Status Register for Channel 0 - High (DSTAT0_HI)—Offset 2Ch" on page 3458	00000000h
30–33h	4	"Source Status Address Register for Channel 0 - Low (SSTATAR0_LO)—Offset 30h" on page 3459	00000000h
34–37h	4	"Source Status Address Register for Channel 0 - High (SSTATAR0_HI)—Offset 34h" on page 3459	00000000h
38–3Bh	4	"Dest Status Address Register for Channel 0 - Low (DSTATAR0_LO)—Offset 38h" on page 3460	00000000h
3C–3Fh	4	"Dest Status Address Register for Channel 0 - High (DSTATAR0_HI)—Offset 3Ch" on page 3460	00000000h
40–43h	4	"Configuration Register for Channel 0 - Low (CFG0_LO)—Offset 40h" on page 3461	00000E00h
44–47h	4	"Configuration Register for Channel 0 - High (CFG0_HI)—Offset 44h" on page 3462	00000004h
48–4Bh	4	"Source Gather Register for Channel 0 - Low (SGR0_LO)—Offset 48h" on page 3463	00000000h
4C–4Fh	4	"Source Gather Register for Channel 0 - High (SGR0_HI)—Offset 4Ch" on page 3464	00000000h
50–53h	4	"Destination Scatter Register for Channel 0 - Low (DSR0_LO)—Offset 50h" on page 3464	00000000h
54–57h	4	"Dest Scatter Register for Channel 0 - High (DSR0_HI)—Offset 54h" on page 3465	00000000h
58–5Bh	4	"Source Address Register for Channel 1 - Low (SAR1_LO)—Offset 58h" on page 3465	00000000h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5C–5Fh	4	"Source Address Register for Channel 1 - High (SAR1_HI)—Offset 5Ch" on page 3465	00000000h
60–63h	4	"Destination Address Register for Channel 1 - Low (DAR1_LO)—Offset 60h" on page 3466	00000000h
64–67h	4	"Destination Address Register for Channel 1 - High (DAR1_HI)—Offset 64h" on page 3466	00000000h
68–6Bh	4	"Linked List Pointer Register for Channel 1 - Low (LLP1_LO)—Offset 68h" on page 3467	00000000h
6C–6Fh	4	"Linked List Pointer Register for Channel 1 - High (LLP1_HI)—Offset 6Ch" on page 3467	00000000h
70–73h	4	"Control Register for Channel 1 - Low (CTL1_LO)—Offset 70h" on page 3468	00304801h
74–77h	4	"Control Register for Channel 1 - High (CTL1_HI)—Offset 74h" on page 3469	00000002h
78–7Bh	4	"Source Status Register for Channel 1 - Low (SSTAT1_LO)—Offset 78h" on page 3470	00000000h
7C–7Fh	4	"Source Status Register for Channel 1 - High (SSTAT1_HI)—Offset 7Ch" on page 3470	00000000h
80–83h	4	"Dest Status Register for Channel 1 - Low (DSTAT1_LO)—Offset 80h" on page 3471	00000000h
84–87h	4	"Dest Status Register for Channel 1 - High (DSTAT1_HI)—Offset 84h" on page 3471	00000000h
88–8Bh	4	"Source Status Address Register for Channel 1 - Low (SSTATAR1_LO)—Offset 88h" on page 3472	00000000h
8C–8Fh	4	"Source Status Address Register for Channel 1 - High (SSTATAR1_HI)—Offset 8Ch" on page 3472	00000000h
90–93h	4	"Dest Status Address Register for Channel 1 - Low (DSTATAR1_LO)—Offset 90h" on page 3473	00000000h
94–97h	4	"Dest Status Address Register for Channel 1 - High (DSTATAR1_HI)—Offset 94h" on page 3473	00000000h
98–9Bh	4	"Configuration Register for Channel 1 - Low (CFG1_LO)—Offset 98h" on page 3473	00000E20h
9C–9Fh	4	"Configuration Register for Channel 1 - High (CFG1_HI)—Offset 9Ch" on page 3475	00000004h
A0–A3h	4	"Source Gather Register for Channel 1 - Low (SGR1_LO)—Offset A0h" on page 3476	00000000h
A4–A7h	4	"Source Gather Register for Channel 1 - High (SGR1_HI)—Offset A4h" on page 3476	00000000h
A8–ABh	4	"Destination Scatter Register for Channel 1 - Low (DSR1_LO)—Offset A8h" on page 3477	00000000h
AC–AFh	4	"Dest Scatter Register for Channel 1 - High (DSR1_HI)—Offset ACh" on page 3477	00000000h
B0–B3h	4	"Source Address Register for Channel 2 - Low (SAR2_LO)—Offset B0h" on page 3478	00000000h
B4–B7h	4	"Source Address Register for Channel 2 - High (SAR2_HI)—Offset B4h" on page 3478	00000000h
B8–BBh	4	"Destination Address Register for Channel 2 - Low (DAR2_LO)—Offset B8h" on page 3478	00000000h
BC–BFh	4	"Destination Address Register for Channel 2 - High (DAR2_HI)—Offset BCh" on page 3479	00000000h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C0–C3h	4	"Linked List Pointer Register for Channel 2 - Low (LLP2_LO)—Offset C0h" on page 3479	00000000h
C4–C7h	4	"Linked List Pointer Register for Channel 2 - High (LLP2_HI)—Offset C4h" on page 3480	00000000h
C8–CBh	4	"Control Register for Channel 2 - Low (CTL2_LO)—Offset C8h" on page 3480	00304801h
CC–CFh	4	"Control Register for Channel 2 - High (CTL2_HI)—Offset CCh" on page 3482	00000002h
D0–D3h	4	"Source Status Register for Channel 2 - Low (SSTAT2_LO)—Offset D0h" on page 3482	00000000h
D4–D7h	4	"Source Status Register for Channel 2 - High (SSTAT2_HI)—Offset D4h" on page 3483	00000000h
D8–DBh	4	"Dest Status Register for Channel 2 - Low (DSTAT2_LO)—Offset D8h" on page 3483	00000000h
DC–DFh	4	"Dest Status Register for Channel 2 - High (DSTAT2_HI)—Offset DCh" on page 3484	00000000h
E0–E3h	4	"Source Status Address Register for Channel 2 - Low (SSTATAR2_LO)—Offset E0h" on page 3484	00000000h
E4–E7h	4	"Source Status Address Register for Channel 2 - High (SSTATAR2_HI)—Offset E4h" on page 3485	00000000h
E8–EBh	4	"Dest Status Address Register for Channel 2 - Low (DSTATAR2_LO)—Offset E8h" on page 3485	00000000h
EC–EFh	4	"Dest Status Address Register for Channel 2 - High (DSTATAR2_HI)—Offset ECh" on page 3486	00000000h
F0–F3h	4	"Configuration Register for Channel 2 - Low (CFG2_LO)—Offset F0h" on page 3486	00000E40h
F4–F7h	4	"Configuration Register for Channel 2 - High (CFG2_HI)—Offset F4h" on page 3487	00000004h
F8–FBh	4	"Source Gather Register for Channel 2 - Low (SGR2_LO)—Offset F8h" on page 3488	00000000h
FC–FFh	4	"Source Gather Register for Channel 2 - High (SGR2_HI)—Offset FCh" on page 3489	00000000h
100–103h	4	"Destination Scatter Register for Channel 2 - Low (DSR2_LO)—Offset 100h" on page 3489	00000000h
104–107h	4	"Dest Scatter Register for Channel 2 - High (DSR2_HI)—Offset 104h" on page 3490	00000000h
108–10Bh	4	"Source Address Register for Channel 3 - Low (SAR3_LO)—Offset 108h" on page 3490	00000000h
10C–10Fh	4	"Source Address Register for Channel 3 - High (SAR3_HI)—Offset 10Ch" on page 3491	00000000h
110–113h	4	"Destination Address Register for Channel 3 - Low (DAR3_LO)—Offset 110h" on page 3491	00000000h
114–117h	4	"Destination Address Register for Channel 3 - High (DAR3_HI)—Offset 114h" on page 3492	00000000h
118–11Bh	4	"Linked List Pointer Register for Channel 3 - Low (LLP3_LO)—Offset 118h" on page 3492	00000000h
11C–11Fh	4	"Linked List Pointer Register for Channel 3 - High (LLP3_HI)—Offset 11Ch" on page 3493	00000000h
120–123h	4	"Control Register for Channel 3 - Low (CTL3_LO)—Offset 120h" on page 3493	00304801h
124–127h	4	"Control Register for Channel 3 - High (CTL3_HI)—Offset 124h" on page 3495	00000002h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
128–12Bh	4	"Source Status Register for Channel 3 - Low (SSTAT3_LO)—Offset 128h" on page 3495	00000000h
12C–12Fh	4	"Source Status Register for Channel 3 - High (SSTAT3_HI)—Offset 12Ch" on page 3496	00000000h
130–133h	4	"Dest Status Register for Channel 3 - Low (DSTAT3_LO)—Offset 130h" on page 3496	00000000h
134–137h	4	"Dest Status Register for Channel 3 - High (DSTAT3_HI)—Offset 134h" on page 3497	00000000h
138–13Bh	4	"Source Status Address Register for Channel 3 - Low (SSTATAR3_LO)—Offset 138h" on page 3497	00000000h
13C–13Fh	4	"Source Status Address Register for Channel 3 - High (SSTATAR3_HI)—Offset 13Ch" on page 3498	00000000h
140–143h	4	"Dest Status Address Register for Channel 3 - Low (DSTATAR3_LO)—Offset 140h" on page 3498	00000000h
144–147h	4	"Dest Status Address Register for Channel 3 - High (DSTATAR3_HI)—Offset 144h" on page 3499	00000000h
148–14Bh	4	"Configuration Register for Channel 3 - Low (CFG3_LO)—Offset 148h" on page 3499	00000E60h
14C–14Fh	4	"Configuration Register for Channel 3 - High (CFG3_HI)—Offset 14Ch" on page 3500	00000004h
150–153h	4	"Source Gather Register for Channel 3 - Low (SGR3_LO)—Offset 150h" on page 3501	00000000h
154–157h	4	"Source Gather Register for Channel 3 - High (SGR3_HI)—Offset 154h" on page 3502	00000000h
158–15Bh	4	"Destination Scatter Register for Channel 3 - Low (DSR3_LO)—Offset 158h" on page 3502	00000000h
15C–15Fh	4	"Dest Scatter Register for Channel 3 - High (DSR3_HI)—Offset 15Ch" on page 3503	00000000h
160–163h	4	"Source Address Register for Channel 4 - Low (SAR4_LO)—Offset 160h" on page 3503	00000000h
164–167h	4	"Source Address Register for Channel 4 - High (SAR4_HI)—Offset 164h" on page 3504	00000000h
168–16Bh	4	"Destination Address Register for Channel 4 - Low (DAR4_LO)—Offset 168h" on page 3504	00000000h
16C–16Fh	4	"Destination Address Register for Channel 4 - High (DAR4_HI)—Offset 16Ch" on page 3505	00000000h
170–173h	4	"Linked List Pointer Register for Channel 4 - Low (LLP4_LO)—Offset 170h" on page 3505	00000000h
174–177h	4	"Linked List Pointer Register for Channel 4 - High (LLP4_HI)—Offset 174h" on page 3506	00000000h
178–17Bh	4	"Control Register for Channel 4 - Low (CTL4_LO)—Offset 178h" on page 3506	00304801h
17C–17Fh	4	"Control Register for Channel 4 - High (CTL4_HI)—Offset 17Ch" on page 3507	00000002h
180–183h	4	"Source Status Register for Channel 4 - Low (SSTAT4_LO)—Offset 180h" on page 3508	00000000h
184–187h	4	"Source Status Register for Channel 4 - High (SSTAT4_HI)—Offset 184h" on page 3508	00000000h
188–18Bh	4	"Dest Status Register for Channel 4 - Low (DSTAT4_LO)—Offset 188h" on page 3509	00000000h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
18C–18Fh	4	"Dest Status Register for Channel 4 - High (DSTAT4_HI)—Offset 18Ch" on page 3509	00000000h
190–193h	4	"Source Status Address Register for Channel 4 - Low (SSTATAR4_LO)—Offset 190h" on page 3510	00000000h
194–197h	4	"Source Status Address Register for Channel 4 - High (SSTATAR4_HI)—Offset 194h" on page 3510	00000000h
198–19Bh	4	"Dest Status Address Register for Channel 4 - Low (DSTATAR4_LO)—Offset 198h" on page 3511	00000000h
19C–19Fh	4	"Dest Status Address Register for Channel 4 - High (DSTATAR4_HI)—Offset 19Ch" on page 3511	00000000h
1A0–1A3h	4	"Configuration Register for Channel 4 - Low (CFG4_LO)—Offset 1A0h" on page 3512	00000E80h
1A4–1A7h	4	"Configuration Register for Channel 4 - High (CFG4_HI)—Offset 1A4h" on page 3513	00000004h
1A8–1ABh	4	"Source Gather Register for Channel 4 - Low (SGR4_LO)—Offset 1A8h" on page 3514	00000000h
1AC–1AFh	4	"Source Gather Register for Channel 4 - High (SGR4_HI)—Offset 1ACh" on page 3515	00000000h
1B0–1B3h	4	"Destination Scatter Register for Channel 4 - Low (DSR4_LO)—Offset 1B0h" on page 3515	00000000h
1B4–1B7h	4	"Dest Scatter Register for Channel 4 - High (DSR4_HI)—Offset 1B4h" on page 3515	00000000h
1B8–1BBh	4	"Source Address Register for Channel 5 - Low (SAR5_LO)—Offset 1B8h" on page 3516	00000000h
1BC–1BFh	4	"Source Address Register for Channel 5 - High (SAR5_HI)—Offset 1BCh" on page 3516	00000000h
1C0–1C3h	4	"Destination Address Register for Channel 5 - Low (DAR5_LO)—Offset 1C0h" on page 3517	00000000h
1C4–1C7h	4	"Destination Address Register for Channel 5 - High (DAR5_HI)—Offset 1C4h" on page 3517	00000000h
1C8–1CBh	4	"Linked List Pointer Register for Channel 5 - Low (LLP5_LO)—Offset 1C8h" on page 3518	00000000h
1CC–1CFh	4	"Linked List Pointer Register for Channel 5 - High (LLP5_HI)—Offset 1CCh" on page 3518	00000000h
1D0–1D3h	4	"Control Register for Channel 5 - Low (CTL5_LO)—Offset 1D0h" on page 3519	00304801h
1D4–1D7h	4	"Control Register for Channel 5 - High (CTL5_HI)—Offset 1D4h" on page 3520	00000002h
1D8–1DBh	4	"Source Status Register for Channel 5 - Low (SSTAT5_LO)—Offset 1D8h" on page 3521	00000000h
1DC–1DFh	4	"Source Status Register for Channel 5 - High (SSTAT5_HI)—Offset 1DCh" on page 3521	00000000h
1E0–1E3h	4	"Dest Status Register for Channel 5 - Low (DSTAT5_LO)—Offset 1E0h" on page 3522	00000000h
1E4–1E7h	4	"Dest Status Register for Channel 5 - High (DSTAT5_HI)—Offset 1E4h" on page 3522	00000000h
1E8–1EBh	4	"Source Status Address Register for Channel 5 - Low (SSTATAR5_LO)—Offset 1E8h" on page 3523	00000000h
1EC–1EFh	4	"Source Status Address Register for Channel 5 - High (SSTATAR5_HI)—Offset 1ECh" on page 3523	00000000h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F0–1F3h	4	"Dest Status Address Register for Channel 5 - Low (DSTATAR5_LO)—Offset 1F0h" on page 3524	00000000h
1F4–1F7h	4	"Dest Status Address Register for Channel 5 - High (DSTATAR5_HI)—Offset 1F4h" on page 3524	00000000h
1F8–1FBh	4	"Configuration Register for Channel 5 - Low (CFG5_LO)—Offset 1F8h" on page 3524	00000EA0h
1FC–1FFh	4	"Configuration Register for Channel 5 - High (CFG5_HI)—Offset 1FCh" on page 3526	00000004h
200–203h	4	"Source Gather Register for Channel 5 - Low (SGR5_LO)—Offset 200h" on page 3527	00000000h
204–207h	4	"Source Gather Register for Channel 5 - High (SGR5_HI)—Offset 204h" on page 3527	00000000h
208–20Bh	4	"Destination Scatter Register for Channel 5 - Low (DSR5_LO)—Offset 208h" on page 3528	00000000h
20C–20Fh	4	"Dest Scatter Register for Channel 5 - High (DSR5_HI)—Offset 20Ch" on page 3528	00000000h
210–213h	4	"Source Address Register for Channel 6 - Low (SAR6_LO)—Offset 210h" on page 3529	00000000h
214–217h	4	"Source Address Register for Channel 6 - High (SAR6_HI)—Offset 214h" on page 3529	00000000h
218–21Bh	4	"Destination Address Register for Channel 6 - Low (DAR6_LO)—Offset 218h" on page 3530	00000000h
21C–21Fh	4	"Destination Address Register for Channel 6 - High (DAR6_HI)—Offset 21Ch" on page 3530	00000000h
220–223h	4	"Linked List Pointer Register for Channel 6 - Low (LLP6_LO)—Offset 220h" on page 3531	00000000h
224–227h	4	"Linked List Pointer Register for Channel 6 - High (LLP6_HI)—Offset 224h" on page 3531	00000000h
228–22Bh	4	"Control Register for Channel 6 - Low (CTL6_LO)—Offset 228h" on page 3532	00304801h
22C–22Fh	4	"Control Register for Channel 6 - High (CTL6_HI)—Offset 22Ch" on page 3533	00000002h
230–233h	4	"Source Status Register for Channel 6 - Low (SSTAT6_LO)—Offset 230h" on page 3534	00000000h
234–237h	4	"Source Status Register for Channel 6 - High (SSTAT6_HI)—Offset 234h" on page 3534	00000000h
238–23Bh	4	"Dest Status Register for Channel 6 - Low (DSTAT6_LO)—Offset 238h" on page 3535	00000000h
23C–23Fh	4	"Dest Status Register for Channel 6 - High (DSTAT6_HI)—Offset 23Ch" on page 3535	00000000h
240–243h	4	"Source Status Address Register for Channel 6 - Low (SSTATAR6_LO)—Offset 240h" on page 3536	00000000h
244–247h	4	"Source Status Address Register for Channel 6 - High (SSTATAR6_HI)—Offset 244h" on page 3536	00000000h
248–24Bh	4	"Dest Status Address Register for Channel 6 - Low (DSTATAR6_LO)—Offset 248h" on page 3537	00000000h
24C–24Fh	4	"Dest Status Address Register for Channel 6 - High (DSTATAR6_HI)—Offset 24Ch" on page 3537	00000000h
250–253h	4	"Configuration Register for Channel 6 - Low (CFG6_LO)—Offset 250h" on page 3538	00000EC0h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
254–257h	4	"Configuration Register for Channel 6 - High (CFG6_HI)—Offset 254h" on page 3539	00000004h
258–25Bh	4	"Source Gather Register for Channel 6 - Low (SGR6_LO)—Offset 258h" on page 3540	00000000h
25C–25Fh	4	"Source Gather Register for Channel 6 - High (SGR6_HI)—Offset 25Ch" on page 3540	00000000h
260–263h	4	"Destination Scatter Register for Channel 6 - Low (DSR6_LO)—Offset 260h" on page 3541	00000000h
264–267h	4	"Dest Scatter Register for Channel 6 - High (DSR6_HI)—Offset 264h" on page 3541	00000000h
268–26Bh	4	"Source Address Register for Channel 7 - Low (SAR7_LO)—Offset 268h" on page 3542	00000000h
26C–26Fh	4	"Source Address Register for Channel 7 - High (SAR7_HI)—Offset 26Ch" on page 3542	00000000h
270–273h	4	"Destination Address Register for Channel 7 - Low (DAR7_LO)—Offset 270h" on page 3543	00000000h
274–277h	4	"Destination Address Register for Channel 7 - High (DAR7_HI)—Offset 274h" on page 3543	00000000h
278–27Bh	4	"Linked List Pointer Register for Channel 7 - Low (LLP7_LO)—Offset 278h" on page 3544	00000000h
27C–27Fh	4	"Linked List Pointer Register for Channel 7 - High (LLP7_HI)—Offset 27Ch" on page 3544	00000000h
280–283h	4	"Control Register for Channel 7 - Low (CTL7_LO)—Offset 280h" on page 3545	00304801h
284–287h	4	"Control Register for Channel 7 - High (CTL7_HI)—Offset 284h" on page 3546	00000002h
288–28Bh	4	"Source Status Register for Channel 7 - Low (SSTAT7_LO)—Offset 288h" on page 3547	00000000h
28C–28Fh	4	"Source Status Register for Channel 7 - High (SSTAT7_HI)—Offset 28Ch" on page 3547	00000000h
290–293h	4	"Dest Status Register for Channel 7 - Low (DSTAT7_LO)—Offset 290h" on page 3548	00000000h
294–297h	4	"Dest Status Register for Channel 7 - High (DSTAT7_HI)—Offset 294h" on page 3548	00000000h
298–29Bh	4	"Source Status Address Register for Channel 7 - Low (SSTATAR7_LO)—Offset 298h" on page 3549	00000000h
29C–29Fh	4	"Source Status Address Register for Channel 7 - High (SSTATAR7_HI)—Offset 29Ch" on page 3549	00000000h
2A0–2A3h	4	"Dest Status Address Register for Channel 7 - Low (DSTATAR7_LO)—Offset 2A0h" on page 3550	00000000h
2A4–2A7h	4	"Dest Status Address Register for Channel 7 - High (DSTATAR7_HI)—Offset 2A4h" on page 3550	00000000h
2A8–2ABh	4	"Configuration Register for Channel 7 - Low (CFG7_LO)—Offset 2A8h" on page 3551	00000EE0h
2AC–2AFh	4	"Configuration Register for Channel 7 - High (CFG7_HI)—Offset 2ACh" on page 3552	00000004h
2B0–2B3h	4	"Source Gather Register for Channel 7 - Low (SGR7_LO)—Offset 2B0h" on page 3553	00000000h
2B4–2B7h	4	"Source Gather Register for Channel 7 - High (SGR7_HI)—Offset 2B4h" on page 3553	00000000h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2B8–2BBh	4	"Destination Scatter Register for Channel 7 - Low (DSR7_LO)—Offset 2B8h" on page 3554	00000000h
2BC–2BFh	4	"Dest Scatter Register for Channel 7 - High (DSR7_HI)—Offset 2BCh" on page 3554	00000000h
2C0–2C3h	4	"Interrupt Raw Status Registers - Low (RawTfr_LO)—Offset 2C0h" on page 3555	00000000h
2C4–2C7h	4	"Interrupt Raw Status Registers - High (RawTfr_HI)—Offset 2C4h" on page 3556	00000000h
2C8–2CBh	4	"Interrupt Raw Status Registers - Low (RawBlock_LO)—Offset 2C8h" on page 3556	00000000h
2CC–2CFh	4	"Interrupt Raw Status Registers - High (RawBlock_HI)—Offset 2CCh" on page 3557	00000000h
2D0–2D3h	4	"Interrupt Raw Status Registers - Low (RawSrcTran_LO)—Offset 2D0h" on page 3557	00000000h
2D4–2D7h	4	"Interrupt Raw Status Registers - High (RawSrcTran_HI)—Offset 2D4h" on page 3558	00000000h
2D8–2DBh	4	"Interrupt Raw Status Registers - Low (RawDstTran_LO)—Offset 2D8h" on page 3558	00000000h
2DC–2DFh	4	"Interrupt Raw Status Registers - High (RawDstTran_HI)—Offset 2DCh" on page 3559	00000000h
2E0–2E3h	4	"Interrupt Raw Status Registers - Low (RawErr_LO)—Offset 2E0h" on page 3559	00000000h
2E4–2E7h	4	"Interrupt Raw Status Registers - High (RawErr_HI)—Offset 2E4h" on page 3560	00000000h
2E8–2EBh	4	"Interrupt Status Registers - Low (StatusTfr_LO)—Offset 2E8h" on page 3560	00000000h
2EC–2EFh	4	"Interrupt Status Registers - High (StatusTfr_HI)—Offset 2ECh" on page 3561	00000000h
2F0–2F3h	4	"Interrupt Status Registers - Low (StatusBlock_LO)—Offset 2F0h" on page 3561	00000000h
2F4–2F7h	4	"Interrupt Status Registers - High (StatusBlock_HI)—Offset 2F4h" on page 3562	00000000h
2F8–2FBh	4	"Interrupt Status Registers - Low (StatusSrcTran_LO)—Offset 2F8h" on page 3562	00000000h
2FC–2FFh	4	"Interrupt Status Registers - High (StatusSrcTran_HI)—Offset 2FCh" on page 3563	00000000h
300–303h	4	"Interrupt Status Registers - Low (StatusDstTran_LO)—Offset 300h" on page 3563	00000000h
304–307h	4	"Interrupt Status Registers - High (StatusDstTran_HI)—Offset 304h" on page 3564	00000000h
308–30Bh	4	"Interrupt Status Registers - Low (StatusErr_LO)—Offset 308h" on page 3564	00000000h
30C–30Fh	4	"Interrupt Status Registers - High (StatusErr_HI)—Offset 30Ch" on page 3565	00000000h
310–313h	4	"Interrupt Mask Registers - Low (MaskTfr_LO)—Offset 310h" on page 3565	00000000h
314–317h	4	"Interrupt Mask Registers - High (MaskTfr_HI)—Offset 314h" on page 3566	00000000h
318–31Bh	4	"Interrupt Mask Registers - Low (MaskBlock_LO)—Offset 318h" on page 3566	00000000h
31C–31Fh	4	"Interrupt Mask Registers - High (MaskBlock_HI)—Offset 31Ch" on page 3567	00000000h
320–323h	4	"Interrupt Mask Registers - Low (MaskSrcTran_LO)—Offset 320h" on page 3567	00000000h
324–327h	4	"Interrupt Mask Registers - High (MaskSrcTran_HI)—Offset 324h" on page 3568	00000000h
328–32Bh	4	"Interrupt Mask Registers - Low (MaskDstTran_LO)—Offset 328h" on page 3568	00000000h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
32C–32Fh	4	"Interrupt Mask Registers - High (MaskDstTran_HI)—Offset 32Ch" on page 3569	00000000h
330–333h	4	"Interrupt Mask Registers - Low (MaskErr_LO)—Offset 330h" on page 3569	00000000h
334–337h	4	"Interrupt Mask Registers - High (MaskErr_HI)—Offset 334h" on page 3570	00000000h
338–33Bh	4	"Interrupt Clear Registers - Low (ClearTfr_LO)—Offset 338h" on page 3570	00000000h
33C–33Fh	4	"Interrupt Clear Registers - High (ClearTfr_HI)—Offset 33Ch" on page 3571	00000000h
340–343h	4	"Interrupt Clear Registers - Low (ClearBlock_LO)—Offset 340h" on page 3572	00000000h
344–347h	4	"Interrupt Clear Registers (ClearBlock_HI)—Offset 344h" on page 3572	00000000h
348–34Bh	4	"Interrupt Clear Registers - Low (ClearSrcTran_LO)—Offset 348h" on page 3573	00000000h
34C–34Fh	4	"Interrupt Clear RegistersClearSrc - High (ClearSrcTran_HI)—Offset 34Ch" on page 3573	00000000h
350–353h	4	"Interrupt Clear Registers - Low (ClearDstTran_LO)—Offset 350h" on page 3574	00000000h
354–357h	4	"Interrupt Clear Registers - High (ClearDstTran_HI)—Offset 354h" on page 3574	00000000h
358–35Bh	4	"Interrupt Clear Registers - Low (ClearErr_LO)—Offset 358h" on page 3575	00000000h
35C–35Fh	4	"Interrupt Clear Registers - High (ClearErr_HI)—Offset 35Ch" on page 3575	00000000h
360–363h	4	"Combined Interrupt Status Register - Low (StatusInt_LO)—Offset 360h" on page 3576	00000000h
364–367h	4	"Combined Interrupt Status Register - High (StatusInt_HI)—Offset 364h" on page 3576	00000000h
368–36Bh	4	"Source Software Transaction Request Register - Low (ReqSrcReg_LO)—Offset 368h" on page 3577	00000000h
36C–36Fh	4	"Source Software Transaction Request Register - High (ReqSrcReg_HI)—Offset 36Ch" on page 3578	00000000h
370–373h	4	"Destination Software Transaction Request Register - Low (ReqDstReg_LO)—Offset 370h" on page 3578	00000000h
374–377h	4	"Destination Software Transaction Request Register - High (ReqDstReg_HI)—Offset 374h" on page 3579	00000000h
378–37Bh	4	"Single Source Software Transaction Request Register - Low (SglRqSrcReg_LO)—Offset 378h" on page 3579	00000000h
37C–37Fh	4	"Single Source Software Transaction Request Register - High (SglRqSrcReg_HI)—Offset 37Ch" on page 3580	00000000h
380–383h	4	"Single Destination Software Transaction Request Register - Low (SglRqDstReg_LO)—Offset 380h" on page 3581	00000000h
384–387h	4	"Single Destination Software Transaction Request Register - High (SglRqDstReg_HI)—Offset 384h" on page 3581	00000000h
388–38Bh	4	"Last Source Transaction Request Register - Low (LstSrcReg_LO)—Offset 388h" on page 3582	00000000h
38C–38Fh	4	"Last Source Transaction Request Register - High (LstSrcReg_HI)—Offset 38Ch" on page 3582	00000000h
390–393h	4	"Last Destination Transaction Request Register - Low (LstDstReg_LO)—Offset 390h" on page 3583	00000000h
394–397h	4	"Last Destination Transaction Request Register - High (LstDstReg_HI)—Offset 394h" on page 3584	00000000h
398–39Bh	4	"DW_ahb_dmac Configuration Register - Low (DmaCfgReg_LO)—Offset 398h" on page 3584	00000000h
39C–39Fh	4	"DW_ahb_dmac Configuration Register - High (DmaCfgReg_HI)—Offset 39Ch" on page 3585	00000000h

Table 253. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3A0–3A3h	4	"DW_ahb_dmac Channel Enable Register - Low (ChEnReg_LO)—Offset 3A0h" on page 3585	00000000h
3A4–3A7h	4	"DW_ahb_dmac Channel Enable Register - High (ChEnReg_HI)—Offset 3A4h" on page 3586	00000000h
3A8–3ABh	4	"DW_ahb_dmac ID Register - Low (DmaIdReg_LO)—Offset 3A8h" on page 3586	C0CAC01Ah
3AC–3AFh	4	"DW_ahb_dmac ID Register - High (DmaIdReg_HI)—Offset 3ACh" on page 3587	00000000h
3B0–3B3h	4	"DW_ahb_dmac Test Register - Low (DmaTestReg_LO)—Offset 3B0h" on page 3587	00000000h
3B4–3B7h	4	"DW_ahb_dmac Test Register - High (DmaTestReg_HI)—Offset 3B4h" on page 3588	00000000h
3C8–3CBh	4	"DW_ahb_dmac Component Parameters Register 6 - Low (DMA_COMP_PARAMS_6_LO)—Offset 3C8h" on page 3588	00000000h
3CC–3CFh	4	"DW_ahb_dmac Component Parameters Register 6 - High (DMA_COMP_PARAMS_6_HI)—Offset 3CCh" on page 3589	38220300h
3D0–3D3h	4	"DW_ahb_dmac Component Parameters Register 5 - Low (DMA_COMP_PARAMS_5_LO)—Offset 3D0h" on page 3591	38220300h
3D4–3D7h	4	"DW_ahb_dmac Component Parameters Register 5 - High (DMA_COMP_PARAMS_5_HI)—Offset 3D4h" on page 3594	38220300h
3D8–3DBh	4	"DW_ahb_dmac Component Parameters Register 4 - Low (DMA_COMP_PARAMS_4_LO)—Offset 3D8h" on page 3596	38220300h
3DC–3DFh	4	"DW_ahb_dmac Component Parameters Register 4 - High (DMA_COMP_PARAMS_4_HI)—Offset 3DCh" on page 3599	38220300h
3E0–3E3h	4	"DW_ahb_dmac Component Parameters Register 3 - Low (DMA_COMP_PARAMS_3_LO)—Offset 3E0h" on page 3601	38220300h
3E4–3E7h	4	"DW_ahb_dmac Component Parameters Register 3 - High (DMA_COMP_PARAMS_3_HI)—Offset 3E4h" on page 3604	38220300h
3E8–3EBh	4	"DW_ahb_dmac Component Parameters Register 2 - Low (DMA_COMP_PARAMS_2_LO)—Offset 3E8h" on page 3606	38220300h
3EC–3EFh	4	"DW_ahb_dmac Component Parameters Register 2 - High (DMA_COMP_PARAMS_2_HI)—Offset 3ECh" on page 3608	00000000h
3F0–3F3h	4	"DW_ahb_dmac Component Parameters Register 1 - Low (DMA_COMP_PARAMS_1_LO)—Offset 3F0h" on page 3611	AAAAAAAAh
3F4–3F7h	4	"DW_ahb_dmac Component Parameters Register 1 - High (DMA_COMP_PARAMS_1_HI)—Offset 3F4h" on page 3612	37000F04h
3F8–3FBh	4	"DMA Component ID RegisterDma - Low (DmaCompsID_LO)—Offset 3F8h" on page 3614	44571110h
3FC–3FFh	4	"DMA Component ID Register - High (DmaCompsID_HI)—Offset 3FCh" on page 3615	3231362Ah

24.3.1 Source Address Register for Channel 0 - Low (SAR0_LO)—Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current AHB transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.3.2 Source Address Register for Channel 0 - High (SAR0_HI)—Offset 4h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.3 Destination Address Register for Channel 0 - Low (DAR0_LO)—Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before thestart of the DMA transfer. While the DMA transfer is inprogress, this register is updated to reflect the destination address of the current AHB transfer.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.3.4 Destination Address Register for Channel 0 - High (DAR0_HI)—Offset Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.5 Linked List Pointer Register for Channel 0 - Low (LLP0_LO)—Offset 10h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

LOC | LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.3.6 Linked List Pointer Register for Channel 0 - High (LLP0_HI)—Offset 14h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.7 Control Register for Channel 0 - Low (CTL0_LO)—Offset 18h

This register contains fields that control the DMA transfer. **Note:** You need to program this register prior to enabling the channel.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Fields (bit 31 to bit 0): Undefined_ | LLP_SRC_EN | LLP_DST_EN | SMS | DMS | TT_FC | Undefined | DST_SCATTER_EN | SRC_GATHER_EN | SRC_MSIZE | DEST_MSIZE | SINC | DINC | SRC_TR_WIDTH | DST_TR_WIDTH | INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** The following transfer types are supported. • Memory to Memory • Memory to Peripheral • Peripheral to Memory • Peripheral to Peripheral Flow Control can be assigned to the DW_ahb_dmac, the source peripheral, or the destination peripheral.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Number of data items, each of width CTLx.SRC_TR_WIDTH, to be read from the source every time a source burst transaction request is made from either the corresponding hardware or software handshaking interface.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Number of data items, each of width CTLx.DST_TR_WIDTH, to be written to the destination every time a destination burst transaction request is made from either the corresponding hardware or software handshaking interface.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.3.8 Control Register for Channel 0 - High (CTL0_HI)—Offset 1Ch

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Undefined_ (31:13) | DONE (12) | BLOCK_TS (11:0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** If status write-back is enabled, the upper word of the control register, CTLx[63:32], is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTLx.DONE bit to see when a block transfer is complete. The LLI CTLx.DONE bit should be cleared when the linked lists are set up in memory, prior to enabling the channel. LLI accesses are always 32-bit accesses (Hsize = 2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.3.9 Source Status Register for Channel 0 - Low (SSTAT0_LO)—Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.3.10 Source Status Register for Channel 0 - High (SSTAT0_HI)—Offset 24h

Refer to the description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.11 Dest Status Register for Channel 0 - Low (DSTAT0_LO)—Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI before the start of the next block. For conditions under which the destination status information is fetched, refer to the abovementioned spec.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

24.3.12 Dest Status Register for Channel 0 - High (DSTAT0_HI)—Offset 2Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.13 Source Status Address Register for Channel 0 - Low (SSTATAR0_LO)—Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.14 Source Status Address Register for Channel 0 - High (SSTATAR0_HI)—Offset 34h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.15 Dest Status Address Register for Channel 0 - Low (DSTATAR0_LO)—Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.16 Dest Status Address Register for Channel 0 - High (DSTATAR0_HI)—Offset 3Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.17 Configuration Register for Channel 0 - Low (CFG0_LO)—Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. **Note:** You need to program this register prior to enabling the channel.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
RELOAD_DST	RELOAD_SRC	MAX_ABRST										SRC_HS_POL	DST_HS_POL	LOCK_B	LOCK_CH	LOCK_B_L		LOCK_CH_L		HS_SEL_SRC	HS_SEL_DST	FIFO_EMPTY	CH_SUSP	CH_PRIOR			Undefined				

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	0h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.3.18 Configuration Register for Channel 0 - High (CFG0_HI)—Offset 44h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 31:15	Bits 14:11	Bits 10:7	Bit 6	Bit 5	Bits 4:2	Bit 1	Bit 0
Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.3.19 Source Gather Register for Channel 0 - Low (SGR0_LO)—Offset 48h

The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer.

24.3.20 Source Gather Register for Channel 0 - High (SGR0_HI)—Offset 4Ch

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.21 Destination Scatter Register for Channel 0 - Low (DSR0_LO)—Offset 50h

The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC | DSI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary, when scatter mode is enabled for the destination transfer.

24.3.22 Dest Scatter Register for Channel 0 - High (DSR0_HI)—Offset 54h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.23 Source Address Register for Channel 1 - Low (SAR1_LO)—Offset 58h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.3.24 Source Address Register for Channel 1 - High (SAR1_HI)—Offset 5Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.25 Destination Address Register for Channel 1 - Low (DAR1_LO)—Offset 60h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.3.26 Destination Address Register for Channel 1 - High (DAR1_HI)—Offset 64h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.27 Linked List Pointer Register for Channel 1 - Low (LLP1_LO)—Offset 68h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.3.28 Linked List Pointer Register for Channel 1 - High (LLP1_HI)—Offset 6Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.29 Control Register for Channel 1 - Low (CTL1_LO)—Offset 70h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 1 1 | 0 0 0 0 | 0 1 0 0 | 1 0 0 0 | 0 0 0 0 | 0 0 0 1

Undefined_ | LLP_SRC_EN | LLP_DST_EN | SMS | DMS | TT_FC | Undefined | DST_SCATTER_EN | SRC_GATHER_EN | SRC_MSIZE | DEST_MSIZE | SINC | DINC | SRC_TR_WIDTH | DST_TR_WIDTH | INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.3.30 Control Register for Channel 1 - High (CTL1_HI)—Offset 74h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
									Undefined_										DONE						BLOCK_TS						

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled, to indicate the block size.

24.3.31 Source Status Register for Channel 1 - Low (SSTAT1_LO)—Offset 78h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.3.32 Source Status Register for Channel 1 - High (SSTAT1_HI)—Offset 7Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.33 Dest Status Register for Channel 1 - Low (DSTAT1_LO)—Offset 80h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest. status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

24.3.34 Dest Status Register for Channel 1 - High (DSTAT1_HI)—Offset 84h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.35 Source Status Address Register for Channel 1 - Low (SSTATAR1_LO)—Offset 88h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.36 Source Status Address Register for Channel 1 - High (SSTATAR1_HI)—Offset 8Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.37 Dest Status Address Register for Channel 1 - Low (DSTATAR1_LO)—Offset 90h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.38 Dest Status Address Register for Channel 1 - High (DSTATAR1_HI)—Offset 94h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.39 Configuration Register for Channel 1 - Low (CFG1_LO)—Offset 98h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E20h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0
RELOAD_DST	RELOAD_SRC	MAX_ABRST										SRC_HS_POL	DST_HS_POL	LOCK_B	LOCK_CH	LOCK_B_L		LOCK_CH_L		HS_SEL_SRC	HS_SEL_DST	FIFO_EMPTY	CH_SUSP	CH_PRIOR				Undefined			

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	1h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.3.40 Configuration Register for Channel 1 - High (CFG1_HI)—Offset 9Ch

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.3.41 Source Gather Register for Channel 1 - Low (SGR1_LO)—Offset A0h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.3.42 Source Gather Register for Channel 1 - High (SGR1_HI)—Offset A4h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.43 Destination Scatter Register for Channel 1 - Low (DSR1_LO)—Offset A8h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.3.44 Dest Scatter Register for Channel 1 - High (DSR1_HI)—Offset ACh

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.45 Source Address Register for Channel 2 - Low (SAR2_LO)—Offset B0h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.3.46 Source Address Register for Channel 2 - High (SAR2_HI)—Offset B4h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.47 Destination Address Register for Channel 2 - Low (DAR2_LO)—Offset B8h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.3.48 Destination Address Register for Channel 2 - High (DAR2_HI)—Offset BCh

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.49 Linked List Pointer Register for Channel 2 - Low (LLP2_LO)—Offset C0h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC | LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.3.50 Linked List Pointer Register for Channel 2 - High (LLP2_HI)—Offset C4h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.51 Control Register for Channel 2 - Low (CTL2_LO)—Offset C8h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Undefined_ | LLP_SRC_EN | LLP_DST_EN | SMS | DMS | TT_FC | Undefined | DST_SCATTER_EN | SRC_GATHER_EN | SRC_MSIZE | DEST_MSIZE | SINC | DINC | SRC_TR_WIDTH | DST_TR_WIDTH | INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.3.52 Control Register for Channel 2 - High (CTL2_HI)—Offset CCh

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Undefined_ | DONE | BLOCK_TS

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.3.53 Source Status Register for Channel 2 - Low (SSTAT2_LO)—Offset D0h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register.

24.3.54 Source Status Register for Channel 2 - High (SSTAT2_HI)—Offset D4h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.55 Dest Status Register for Channel 2 - Low (DSTAT2_LO)—Offset D8h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

24.3.56 Dest Status Register for Channel 2 - High (DSTAT2_HI)—Offset DCh

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.57 Source Status Address Register for Channel 2 - Low (SSTATAR2_LO)—Offset E0h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.58 Source Status Address Register for Channel 2 - High (SSTATAR2_HI)—Offset E4h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.59 Dest Status Address Register for Channel 2 - Low (DSTATAR2_LO)—Offset E8h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.60 Dest Status Address Register for Channel 2 - High (DSTATAR2_HI)—Offset ECh

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Field: Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.61 Configuration Register for Channel 2 - Low (CFG2_LO)—Offset F0h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E40h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 0	0 1 0 0	0 0 0 0

Fields: RELOAD_DST (31), RELOAD_SRC (30), MAX_ABRST (29:20), SRC_HS_POL (19), DST_HS_POL (18), LOCK_B (17), LOCK_CH (16), LOCK_B_L (15:14), LOCK_CH_L (13:12), HS_SEL_SRC (11), HS_SEL_DST (10), FIFO_EMPTY (9), CH_SUSP (8), CH_PRIOR (7:5), Undefined (4:0)

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.

Bit Range	Default & Access	Field Name (ID): Description
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	2h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.3.62 Configuration Register for Channel 2 - High (CFG2_HI)—Offset F4h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 31:15	Bits 14:11	Bits 10:7	Bit 6	Bit 5	Bits 4:2	Bit 1	Bit 0
Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.3.63 Source Gather Register for Channel 2 - Low (SGR2_LO)—Offset F8h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SGC | SGI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.3.64 Source Gather Register for Channel 2 - High (SGR2_HI)—Offset FCh

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.65 Destination Scatter Register for Channel 2 - Low (DSR2_LO)—Offset 100h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC | DSI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.3.66 Dest Scatter Register for Channel 2 - High (DSR2_HI)—Offset 104h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 104h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.67 Source Address Register for Channel 3 - Low (SAR3_LO)—Offset 108h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.3.68 Source Address Register for Channel 3 - High (SAR3_HI)—Offset 10Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.69 Destination Address Register for Channel 3 - Low (DAR3_LO)—Offset 110h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.3.70 Destination Address Register for Channel 3 - High (DAR3_HI)—Offset 114h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 114h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.71 Linked List Pointer Register for Channel 3 - Low (LLP3_LO)—Offset 118h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.3.72 Linked List Pointer Register for Channel 3 - High (LLP3_HI)—Offset 11Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 11Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.73 Control Register for Channel 3 - Low (CTL3_LO)—Offset 120h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Undefined_	LLP_SRC_EN	LLP_DST_EN	SMS	DMS	TT_FC	Undefined	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	DINC	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.3.74 Control Register for Channel 3 - High (CTL3_HI)—Offset 124h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Undefined_ (31:13) | DONE (12) | BLOCK_TS (11:0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.3.75 Source Status Register for Channel 3 - Low (SSTAT3_LO)—Offset 128h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.3.76 Source Status Register for Channel 3 - High (SSTAT3_HI)—Offset 12Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 12Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.77 Dest Status Register for Channel 3 - Low (DSTAT3_LO)—Offset 130h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.3.78 Dest Status Register for Channel 3 - High (DSTAT3_HI)—Offset 134h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 134h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.79 Source Status Address Register for Channel 3 - Low (SSTATAR3_LO)—Offset 138h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.80 Source Status Address Register for Channel 3 - High (SSTATAR3_HI)—Offset 13Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 13Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.81 Dest Status Address Register for Channel 3 - Low (DSTATAR3_LO)—Offset 140h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.82 Dest Status Address Register for Channel 3 - High (DSTATAR3_HI)—Offset 144h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 144h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.83 Configuration Register for Channel 3 - Low (CFG3_LO)—Offset 148h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E60h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0

Fields: RELOAD_DST, RELOAD_SRC, MAX_ABRST, SRC_HS_POL, DST_HS_POL, LOCK_B, LOCK_CH, LOCK_B_L, LOCK_CH_L, HS_SEL_SRC, HS_SEL_DST, FIFO_EMPTY, CH_SUSP, CH_PRIOR, Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.

Bit Range	Default & Access	Field Name (ID): Description
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	3h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.3.84 Configuration Register for Channel 3 - High (CFG3_HI)—Offset 14Ch

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced, when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.3.85 Source Gather Register for Channel 3 - Low (SGR3_LO)—Offset 150h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SGC | SGI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.3.86 Source Gather Register for Channel 3 - High (SGR3_HI)—Offset 154h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 154h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.87 Destination Scatter Register for Channel 3 - Low (DSR3_LO)—Offset 158h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC | DSI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.3.88 Dest Scatter Register for Channel 3 - High (DSR3_HI)—Offset 15Ch

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 15Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.89 Source Address Register for Channel 4 - Low (SAR4_LO)—Offset 160h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.3.90 Source Address Register for Channel 4 - High (SAR4_HI)—Offset 164h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 164h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.91 Destination Address Register for Channel 4 - Low (DAR4_LO)—Offset 168h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.3.92 Destination Address Register for Channel 4 - High (DAR4_HI)—Offset 16Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 16Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.93 Linked List Pointer Register for Channel 4 - Low (LLP4_LO)—Offset 170h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.3.94 Linked List Pointer Register for Channel 4 - High (LLP4_HI)—Offset 174h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 174h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.95 Control Register for Channel 4 - Low (CTL4_LO)—Offset 178h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Fields: Undefined_, LLP_SRC_EN, LLP_DST_EN, SMS, DMS, TT_FC, Undefined, DST_SCATTER_EN, SRC_GATHER_EN, SRC_MSIZE, DEST_MSIZE, SINC, DINC, SRC_TR_WIDTH, DST_TR_WIDTH, INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.3.96 Control Register for Channel 4 - High (CTL4_HI)—Offset 17Ch

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Fields: Undefined_ (31:13), DONE (12), BLOCK_TS (11:0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.3.97 Source Status Register for Channel 4 - Low (SSTAT4_LO)—Offset 180h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: SSTAT (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register.

24.3.98 Source Status Register for Channel 4 - High (SSTAT4_HI)—Offset 184h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 184h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.99 Dest Status Register for Channel 4 - Low (DSTAT4_LO)—Offset 188h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.3.100 Dest Status Register for Channel 4 - High (DSTAT4_HI)—Offset 18Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.101 Source Status Address Register for Channel 4 - Low (SSTATAR4_LO)—Offset 190h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 190h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.102 Source Status Address Register for Channel 4 - High (SSTATAR4_HI)—Offset 194h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 194h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.103 Dest Status Address Register for Channel 4 - Low (DSTATAR4_LO)—Offset 198h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 198h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTATAR																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.104 Dest Status Address Register for Channel 4 - High (DSTATAR4_HI)—Offset 19Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 19Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0																					

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.105 Configuration Register for Channel 4 - Low (CFG4_LO)—Offset 1A0h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E80h

Bits	Value	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:20	0 0 0 0 0 0 0 0 0 0	MAX_ABRST
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	LOCK_B
16	0	LOCK_CH
15:14	0 0	LOCK_B_L
13:12	0 0	LOCK_CH_L
11	1	HS_SEL_SRC
10	1	HS_SEL_DST
9	1	FIFO_EMPTY
8	0	CH_SUSP
7:5	1 0 0	CH_PRIOR
4:0	0 0 0 0 0	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	4h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.3.106 Configuration Register for Channel 4 - High (CFG4_HI)—Offset 1A4h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.3.107 Source Gather Register for Channel 4 - Low (SGR4_LO)—Offset 1A8h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.3.108 Source Gather Register for Channel 4 - High (SGR4_HI)—Offset 1ACh

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.109 Destination Scatter Register for Channel 4 - Low (DSR4_LO)—Offset 1B0h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC (31:20) | DSI (19:0)

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.3.110 Dest Scatter Register for Channel 4 - High (DSR4_HI)—Offset 1B4h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.111 Source Address Register for Channel 5 - Low (SAR5_LO)—Offset 1B8h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.3.112 Source Address Register for Channel 5 - High (SAR5_HI)—Offset 1BCh

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.113 Destination Address Register for Channel 5 - Low (DAR5_LO)—Offset 1C0h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAR																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.3.114 Destination Address Register for Channel 5 - High (DAR5_HI)—Offset 1C4h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.115 Linked List Pointer Register for Channel 5 - Low (LLP5_LO)—Offset 1C8h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC | LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.3.116 Linked List Pointer Register for Channel 5 - High (LLP5_HI)—Offset 1CCh

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.117 Control Register for Channel 5 - Low (CTL5_LO)—Offset 1D0h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 1 0 0	1 0 0 0	0 0 0 0	0 0 0 1	

Fields: Undefined_ | LLP_SRC_EN | LLP_DST_EN | SMS | DMS | TT_FC | Undefined | DST_SCATTER_EN | SRC_GATHER_EN | SRC_MSIZE | DEST_MSIZE | SINC | DINC | SRC_TR_WIDTH | DST_TR_WIDTH | INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.3.118 Control Register for Channel 5 - High (CTL5_HI)—Offset 1D4h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Undefined_ | DONE | BLOCK_TS

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.3.119 Source Status Register for Channel 5 - Low (SSTAT5_LO)—Offset 1D8h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.3.120 Source Status Register for Channel 5 - High (SSTAT5_HI)—Offset 1DCh

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.121 Dest Status Register for Channel 5 - Low (DSTAT5_LO)—Offset 1E0h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.3.122 Dest Status Register for Channel 5 - High (DSTAT5_HI)—Offset 1E4h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.123 Source Status Address Register for Channel 5 - Low (SSTATAR5_LO)—Offset 1E8h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.124 Source Status Address Register for Channel 5 - High (SSTATAR5_HI)—Offset 1ECh

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.125 Dest Status Address Register for Channel 5 - Low (DSTATAR5_LO)—Offset 1F0h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.126 Dest Status Address Register for Channel 5 - High (DSTATAR5_HI)—Offset 1F4h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.127 Configuration Register for Channel 5 - Low (CFG5_LO)—Offset 1F8h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EA0h

Bits	31	30	29:20	19	18	17	16	15:14	13:12	11	10	9	8	7:5	4:0
Default	0	0	0 0 0 0 0 0 0 0 0 0	0	0	0	0	0 0	0 0	1	1	1	0	1 0 1	0 0 0 0 0
Field	RELOAD_DST	RELOAD_SRC	MAX_ABRST	SRC_HS_POL	DST_HS_POL	LOCK_B	LOCK_CH	LOCK_B_L	LOCK_CH_L	HS_SEL_SRC	HS_SEL_DST	FIFO_EMPTY	CH_SUSP	CH_PRIOR	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface, and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking

Bit Range	Default & Access	Field Name (ID): Description
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	5h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.3.128 Configuration Register for Channel 5 - High (CFG5_HI)—Offset 1FCh

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h

31	28	24	20	16	12	8	4
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0

Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the FIFO depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.3.129 Source Gather Register for Channel 5 - Low (SGR5_LO)—Offset 200h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.3.130 Source Gather Register for Channel 5 - High (SGR5_HI)—Offset 204h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 204h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.131 Destination Scatter Register for Channel 5 - Low (DSR5_LO)—Offset 208h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC | DSI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.3.132 Dest Scatter Register for Channel 5 - High (DSR5_HI)—Offset 20Ch

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.133 Source Address Register for Channel 6 - Low (SAR6_LO)—Offset 210h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.3.134 Source Address Register for Channel 6 - High (SAR6_HI)—Offset 214h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 214h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.135 Destination Address Register for Channel 6 - Low (DAR6_LO)—Offset 218h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.3.136 Destination Address Register for Channel 6 - High (DAR6_HI)—Offset 21Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 21Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.137 Linked List Pointer Register for Channel 6 - Low (LLP6_LO)—Offset 220h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC | LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.3.138 Linked List Pointer Register for Channel 6 - High (LLP6_HI)—Offset 224h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 224h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

Bits	31:0
Default	0000 0000 0000 0000 0000 0000 0000 0000
Field	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.139 Control Register for Channel 6 - Low (CTL6_LO)—Offset 228h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h

Bits	31:29	28	27	26:25	24:23	22:20	19	18	17	16:14	13:11	10:9	8:7	6:4	3:1	0
Default	000	0	0	00	00	011	0	0	0	001	001	00	00	000	000	1
Field	Undefined_	LLP_SRC_EN	LLP_DST_EN	SMS	DMS	TT_FC	Undefined	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	DINC	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.3.140 Control Register for Channel 6 - High (CTL6_HI)—Offset 22Ch

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Fields: Undefined_ (31:13), DONE (12), BLOCK_TS (11:0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.3.141 Source Status Register for Channel 6 - Low (SSTAT6_LO)—Offset 230h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 230h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.3.142 Source Status Register for Channel 6 - High (SSTAT6_HI)—Offset 234h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 234h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.143 Dest Status Register for Channel 6 - Low (DSTAT6_LO)—Offset 238h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 238h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.3.144 Dest Status Register for Channel 6 - High (DSTAT6_HI)—Offset 23Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 23Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.145 Source Status Address Register for Channel 6 - Low (SSTATAR6_LO)—Offset 240h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.146 Source Status Address Register for Channel 6 - High (SSTATAR6_HI)—Offset 244h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 244h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.147 Dest Status Address Register for Channel 6 - Low (DSTATAR6_LO)—Offset 248h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 248h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.148 Dest Status Address Register for Channel 6 - High (DSTATAR6_HI)—Offset 24Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.149 Configuration Register for Channel 6 - Low (CFG6_LO)—Offset 250h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EC0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0

Bits	Field
31	RELOAD_DST
30	RELOAD_SRC
29:20	MAX_ABRST
19	SRC_HS_POL
18	DST_HS_POL
17	LOCK_B
16	LOCK_CH
15:14	LOCK_B_L
13:12	LOCK_CH_L
11	HS_SEL_SRC
10	HS_SEL_DST
9	FIFO_EMPTY
8	CH_SUSP
7:5	CH_PRIOR
4:0	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	6h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.3.150 Configuration Register for Channel 6 - High (CFG6_HI)—Offset 254h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0

Fields (bit 31 to bit 0): Undefined (31:15), DEST_PER (14:11), SRC_PER (10:7), SS_UPD_EN (6), DS_UPD_EN (5), PROTCTL (4:2), FIFO_MODE (1), FCMODE (0)

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.3.151 Source Gather Register for Channel 6 - Low (SGR6_LO)—Offset 258h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.3.152 Source Gather Register for Channel 6 - High (SGR6_HI)—Offset 25Ch

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 25Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.153 Destination Scatter Register for Channel 6 - Low (DSR6_LO)—Offset 260h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC (bits 31:20), DSI (bits 19:0)

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.3.154 Dest Scatter Register for Channel 6 - High (DSR6_HI)—Offset 264h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 264h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.155 Source Address Register for Channel 7 - Low (SAR7_LO)—Offset 268h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.3.156 Source Address Register for Channel 7 - High (SAR7_HI)—Offset 26Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 26Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.157 Destination Address Register for Channel 7 - Low (DAR7_LO)—Offset 270h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.3.158 Destination Address Register for Channel 7 - High (DAR7_HI)—Offset 274h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 274h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.159 Linked List Pointer Register for Channel 7 - Low (LLP7_LO)—Offset 278h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

LOC | LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.3.160 Linked List Pointer Register for Channel 7 - High (LLP7_HI)—Offset 27Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 27Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field (31:0): Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.161 Control Register for Channel 7 - Low (CTL7_LO)—Offset 280h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Fields: Undefined_ (31:29), LLP_SRC_EN (28), LLP_DST_EN (27), SMS (26:25), DMS (24:23), TT_FC (22:20), Undefined (19), DST_SCATTER_EN (18), SRC_GATHER_EN (17), SRC_MSIZE (16:14), DEST_MSIZE (13:11), SINC (10:9), DINC (8:7), SRC_TR_WIDTH (6:4), DST_TR_WIDTH (3:1), INT_EN (0)

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.3.162 Control Register for Channel 7 - High (CTL7_HI)—Offset 284h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Undefined_ (31:13)	DONE (12)	BLOCK_TS (11:0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.3.163 Source Status Register for Channel 7 - Low (SSTAT7_LO)—Offset 288h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 288h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.3.164 Source Status Register for Channel 7 - High (SSTAT7_HI)—Offset 28Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 28Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.165 Dest Status Register for Channel 7 - Low (DSTAT7_LO)—Offset 290h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 290h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSTAT																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.3.166 Dest Status Register for Channel 7 - High (DSTAT7_HI)—Offset 294h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 294h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.167 Source Status Address Register for Channel 7 - Low (SSTATAR7_LO)—Offset 298h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 298h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31-0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.168 Source Status Address Register for Channel 7 - High (SSTATAR7_HI)—Offset 29Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 29Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31-0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.169 Dest Status Address Register for Channel 7 - Low (DSTATAR7_LO)—Offset 2A0h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.3.170 Dest Status Address Register for Channel 7 - High (DSTATAR7_HI)—Offset 2A4h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.3.171 Configuration Register for Channel 7 - Low (CFG7_LO)—Offset 2A8h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EE0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0	0
RELOAD_DST	RELOAD_SRC	MAX_ABRST										SRC_HS_POL	DST_HS_POL	LOCK_B	LOCK_CH	LOCK_B_L		LOCK_CH_L		HS_SEL_SRC	HS_SEL_DST	FIFO_EMPTY	CH_SUSP	CH_PRIOR			Undefined				

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	7h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.3.172 Configuration Register for Channel 7 - High (CFG7_HI)—Offset 2ACh

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	

Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.3.173 Source Gather Register for Channel 7 - Low (SGR7_LO)—Offset 2B0h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.3.174 Source Gather Register for Channel 7 - High (SGR7_HI)—Offset 2B4h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.175 Destination Scatter Register for Channel 7 - Low (DSR7_LO)—Offset 2B8h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC | DSI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.3.176 Dest Scatter Register for Channel 7 - High (DSR7_HI)—Offset 2BCh

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.177 Interrupt Raw Status Registers - Low (RawTfr_LO)—Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel; for example, RawTfr[2] is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | RAW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.3.178 Interrupt Raw Status Registers - High (RawTfr_HI)—Offset 2C4h

Refer to the description for Interrupt Raw Status Registers - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31–0
0000 0000 0000 0000 0000 0000 0000 0000
Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.179 Interrupt Raw Status Registers - Low (RawBlock_LO)—Offset 2C8h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31–8	7–0
0000 0000 0000 0000 0000 0000	0000 0000
Undefined	RAW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.3.180 Interrupt Raw Status Registers - High (RawBlock_HI)—Offset 2CCh

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.181 Interrupt Raw Status Registers - Low (RawSrcTran_LO)—Offset 2D0h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | RAW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.3.182 Interrupt Raw Status Registers - High (RawSrcTran_HI)—Offset 2D4h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.183 Interrupt Raw Status Registers - Low (RawDstTran_LO)—Offset 2D8h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | RAW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.3.184 Interrupt Raw Status Registers - High (RawDstTran_HI)—Offset 2DCh

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.185 Interrupt Raw Status Registers - Low (RawErr_LO)—Offset 2E0h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

RAW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.3.186 Interrupt Raw Status Registers - High (RawErr_HI)—Offset 2E4h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.187 Interrupt Status Registers - Low (StatusTfr_LO)—Offset 2E8h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined | STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.3.188 Interrupt Status Registers - High (StatusTfr_HI)—Offset 2ECh

All interrupt events from all channels are stored in these Interrupt Status registers after masking: StatusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel; for example, StatusTfr[2] is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DW_ahb_dmac.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

Bits	31:0
Value	0000 0000 0000 0000 0000 0000 0000 0000
Field	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.189 Interrupt Status Registers - Low (StatusBlock_LO)—Offset 2F0h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

Bits	31:8	7:0
Value	0000 0000 0000 0000 0000 0000	0000 0000
Field	Undefined	STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.3.190 Interrupt Status Registers - High (StatusBlock_HI)—Offset 2F4h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.191 Interrupt Status Registers - Low (StatusSrcTran_LO)—Offset 2F8h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (31:8), STATUS (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.3.192 Interrupt Status Registers - High (StatusSrcTran_HI)—Offset 2FCh

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:0
Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.193 Interrupt Status Registers - Low (StatusDstTran_LO)—Offset 300h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
Undefined	STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.3.194 Interrupt Status Registers - High (StatusDstTran_HI)—Offset 304h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 304h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.195 Interrupt Status Registers - Low (StatusErr_LO)—Offset 308h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:8), STATUS (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.3.196 Interrupt Status Registers - High (StatusErr_HI)—Offset 30Ch

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.197 Interrupt Mask Registers - Low (MaskTfr_LO)—Offset 310h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Undefined (bits 31:16) | INT_MASK_WE (bits 15:8) | INT_MASK (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h RW	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

24.3.198 Interrupt Mask Registers - High (MaskTfr_HI)—Offset 314h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 314h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.199 Interrupt Mask Registers - Low (MaskBlock_LO)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel; for example, MaskTfr[2] is the mask bit for the Channel 2 transfer complete interrupt.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | INT_MASK_WE | INT_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**INT_MASK:** Interrupt Mask • 0 = masked • 1 = unmasked

24.3.200 Interrupt Mask Registers - High (MaskBlock_HI)—Offset 31Ch

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 31Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field: Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.201 Interrupt Mask Registers - Low (MaskSrcTran_LO)—Offset 320h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Undefined (bits 31:16), INT_MASK_WE (bits 15:8), INT_MASK (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

24.3.202 Interrupt Mask Registers - High (MaskSrcTran_HI)—Offset 324h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 324h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.203 Interrupt Mask Registers - Low (MaskDstTran_LO)—Offset 328h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | INT_MASK_WE | INT_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

24.3.204 Interrupt Mask Registers - High (MaskDstTran_HI)—Offset 32Ch

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 32Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.205 Interrupt Mask Registers - Low (MaskErr_LO)—Offset 330h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:16	Bits 15:8	Bits 7:0
Undefined	INT_MASK_WE	INT_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

24.3.206 Interrupt Mask Registers - High (MaskErr_HI)—Offset 334h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 334h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:0
Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.207 Interrupt Clear Registers - Low (ClearTfr_LO)—Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel; for example, ClearTfr[2] is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
Undefined	CLEAR

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.3.208 Interrupt Clear Registers - High (ClearTfr_HI)—Offset 33Ch

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 33Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:0
Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.209 Interrupt Clear Registers - Low (ClearBlock_LO)—Offset 340h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																								CLEAR							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.3.210 Interrupt Clear Registers (ClearBlock_HI)—Offset 344h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 344h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.211 Interrupt Clear Registers - Low (ClearSrcTran_LO)—Offset 348h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:8); CLEAR (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.3.212 Interrupt Clear RegistersClearSrc - High (ClearSrcTran_HI)—Offset 34Ch

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.213 Interrupt Clear Registers - Low (ClearDstTran_LO)—Offset 350h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																								CLEAR							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.3.214 Interrupt Clear Registers - High (ClearDstTran_HI)—Offset 354h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 354h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.215 Interrupt Clear Registers - Low (ClearErr_LO)—Offset 358h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:8) | CLEAR (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.3.216 Interrupt Clear Registers - High (ClearErr_HI)—Offset 35Ch

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 35Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.217 Combined Interrupt Status Register - Low (StatusInt_LO)—Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																											ERR	DSTT	SRCT	BLOCK	TFR

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RW	**Undefined:** Reserved.
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register.
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

24.3.218 Combined Interrupt Status Register - High (StatusInt_HI)—Offset 364h

Refer to the description for register StatusInt_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 364h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.219 Source Software Transaction Request Register - Low (ReqSrcReg_LO)—Offset 368h

A bit is assigned for each channel in this register. ReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 368h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																SRC_REQ_WE								SRC_REQ							

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Source Req Write Enable (SRC_REQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Source Request (SRC_REQ):** A channel SRC_REQ bit is written only if the corresponding channel write enable bit in the SRC_REQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

24.3.220 Source Software Transaction Request Register - High (ReqSrcReg_HI)—Offset 36Ch

A bit is assigned for each channel in this register. ReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 36Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.221 Destination Software Transaction Request Register - Low (ReqDstReg_LO)—Offset 370h

A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 370h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | DST_REQ_WE | DST_REQ

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h WO	**Destination Request Write Enable (DST_REQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Request (DST_REQ):** A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

24.3.222 Destination Software Transaction Request Register - High (ReqDstReg_HI)—Offset 374h

A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 374h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.223 Single Source Software Transaction Request Register - Low (SglRqSrcReg_LO)—Offset 378h

A bit is assigned for each channel in this register. SglReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 378h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | SRC_SGLREQ_WE | SRC_SGLREQ

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Source Req Write Enable (SRC_SGLREQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Source Single Request (SRC_SGLREQ):** A channel SRC_SGLREQ bit is written only if the corresponding channel write enable bit in the SRC_SGLREQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

24.3.224 Single Source Software Transaction Request Register - High (SglRqSrcReg_HI)—Offset 37Ch

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 37Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.225 Single Destination Software Transaction Request Register - Low (SglRqDstReg_LO)—Offset 380h

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 380h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16	Bits 15:8	Bits 7:0
Undefined	DST_SGLREQ_WE	DST_SGLREQ

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Destination Request Write Enable (DST_SGLREQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Single or Burst Request (DST_SGLREQ):** A channel DST_SGLREQ bit is written only if the corresponding channel write enable bit in the DST_SGLREQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

24.3.226 Single Destination Software Transaction Request Register - High (SglRqDstReg_HI)—Offset 384h

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 384h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:0
Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.227 Last Source Transaction Request Register - Low (LstSrcReg_LO)—Offset 388h

A bit is assigned for each channel in this register. LstSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n, or when the source of channel n is not a flow controller. A channel LSTSRC bit is written only if the corresponding channel write enable bit in the LSTSRC_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 388h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

Bits	31:16	15:8	7:0
Value	0000 0000 0000 0000	0000 0000	0000 0000
Field	Undefined	LSTSRC_WE	LSTSRC

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Last Source Transaction Request Write Enable (LSTSRC_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Last Source Transaction Request (LSTSRC):** • 0 = Not last transaction in current block • 1 = Last transaction in current block

24.3.228 Last Source Transaction Request Register - High (LstSrcReg_HI)—Offset 38Ch

Refer to description for Last Source Transaction Request Register - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.229 Last Destination Transaction Request Register - Low (LstDstReg_LO)—Offset 390h

A bit is assigned for each channel in this register. LstDstReg[n] is ignored when software handshaking is not enabled for the destination of channel n or when the destination of channel n is not a flow controller. A channel LSTDST bit is written only if the corresponding channel write enable bit in the LSTDST_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 390h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | LSTDST_WE | LSTDST

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Last Destination Transaction Request Write Enable (LSTDST_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Last Transaction Request (LSTDST):** • 0 = Not last transaction in current block • 1 = Last transaction in current block

24.3.230 Last Destination Transaction Request Register - High (LstDstReg_HI)—Offset 394h

Refer to description for Last Destination Transaction Request Register - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 394h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.231 DW_ahb_dmac Configuration Register - Low (DmaCfgReg_LO)—Offset 398h

This register is used to enable the DW_ahb_dmac, which must be done before any channel activity can begin.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined DMA_EN

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RW	**Undefined:** Reserved.
0	0h RW	**DW_ahb_dmac Enable Bit (DMA_EN):** • 0 = DW_ahb_dmac Disabled • 1 = DW_ahb_dmac Enabled

24.3.232 DW_ahb_dmac Configuration Register - High (DmaCfgReg_HI)—Offset 39Ch

Refer to description for DW_ahb_dmac Configuration Register - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 39Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.233 DW_ahb_dmac Channel Enable Register - Low (ChEnReg_LO)—Offset 3A0h

This is the DW_ahb_dmac Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive; it can then enable an inactive channel with the required priority.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | CH_EN_WE | CH_EN

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Channel Enable Write Enable (CH_EN_WE):** The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE (this bit), is asserted on the same AHB write transfer.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel; clearing this bit disables the channel. • 0 = Disable the Channel • 1 = Enable the Channel

24.3.234 DW_ahb_dmac Channel Enable Register - High (ChEnReg_HI)—Offset 3A4h

Refer to the description for DW_ahb_dmac Channel Enable Register - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.235 DW_ahb_dmac ID Register - Low (DmaIdReg_LO)—Offset 3A8h

This is a read-only register that reads back the coreConsultant-configured hardcoded ID number, DMAH_ID_NUM.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: C0CAC01Ah

31			28				24				20				16				12				8				4				0
1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	1	0

DMA_ID

Bit Range	Default & Access	Field Name (ID): Description
31:0	c0cac01ah RO	**Hardcoded DW_ahb_dmac Peripheral ID (DMA_ID):** coreConsultantconfigured hardcoded ID number DMAH_ID_NUM.

24.3.236 DW_ahb_dmac ID Register - High (DmaIdReg_HI)—Offset 3ACh

Refer to the description of DW_ahb_dmac ID Register - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.237 DW_ahb_dmac Test Register - Low (DmaTestReg_LO)—Offset 3B0h

This register is used to put the AHB slave interface into test mode, during which the readback value of the writable registers match the value written, assuming the DW_ahb_dmac configuration has not optimized the same registers. In normal operation, the readback value of some registers is a function of the DW_ahb_dmac state, and does not match the value written.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

TEST_SLV_IF

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RW	**Undefined:** Reserved.
0	0h RW	**TEST_SLV_IF:** Puts the AHB slave interface into test mode. In this mode, the readback value of the writable registers always matches the value written. This bit does not allow writing to read-only registers. • 0 = Normal mode • 1 = Test mode

24.3.238 DW_ahb_dmac Test Register - High (DmaTestReg_HI)—Offset 3B4h

Refer to the description of DW_ahb_dmac Test Register - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.239 DW_ahb_dmac Component Parameters Register 6 - Low (DMA_COMP_PARAMS_6_LO)—Offset 3C8h

Refer to the description for DW_ahb_dmac Component Parameters Register 6 - High.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.3.240 DW_ahb_dmac Component Parameters Register 6 - High (DMA_COMP_PARAMS_6_HI)—Offset 3CCh

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 7. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
Undefined	CH7_FIFO_DEPTH			CH7_SMS			CH7_LMS			CH7_DMS			CH7_MAX_MULT_SIZE			CH7_FC		CH7_HC_LLP	CH7_CTL_WB_EN	CH7_MULTI_BLK_EN	CH7_LOCK_EN	CH7_SRC_GAT_EN	CH7_DST_SCA_EN	CH7_STAT_SRC	CH7_STAT_DST	CH7_STW			CH7_DTW		

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH7_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH7_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH7_SMS:** The value of this register is derived from the DMAH_CH7_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH7_LMS:** The value of this register is derived from the DMAH_CH7_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
21:19	4h RO	**CH7_DMS:** The value of this register is derived from the DMAH_CH7_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH7_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH7_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH7_FC:** The value of this register is derived from the DMAH_CH7_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH7_HC_LLP:** The value of this register is derived from the DMAH_CH7_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH7_CTL_WB_EN:** The value of this register is derived from the DMAH_CH7_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH7_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH7_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH7_LOCK_EN:** The value of this register is derived from the DMAH_CH7_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH7_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH7_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH7_DST_SCA_EN:** The value of this register is derived from the DMAH_CH7_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH7_STAT_SRC:** The value of this register is derived from the DMAH_CH7_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**CH7_STAT_DST:** The value of this register is derived from the DMAH_CH7_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH7_STW:** The value of this register is derived from the DMAH_CH7_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH7_DTW:** The value of this register is derived from the DMAH_CH7_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.3.241 DW_ahb_dmac Component Parameters Register 5 - Low (DMA_COMP_PARAMS_5_LO)—Offset 3D0h

Refer to the description for DW_ahb_dmac Component Parameters Register 5 - High.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h

Bits	Default	Field
31	0	Undefined
30:28	0 1 1	CH6_FIFO_DEPTH
27:25	1 0 0	CH6_SMS
24:22	0 0 0	CH6_LMS
21:19	1 0 0	CH6_DMS
18:16	0 1 0	CH6_MAX_MULT_SIZE
15:14	0 0	CH6_FC
13	0	CH6_HC_LLP
12	0	CH6_CTL_WB_EN
11	0	CH6_MULTI_BLK_EN
10	0	CH6_LOCK_EN
9	1	CH6_SRC_GAT_EN
8	1	CH6_DST_SCA_EN
7	0	CH6_STAT_SRC
6	0	CH6_STAT_DST
5:3	0 0 0	CH6_STW
2:0	0 0 0	CH6_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
30:28	3h RO	**CH6_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH6_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH6_SMS:** The value of this register is derived from the DMAH_CH6_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH6_LMS:** The value of this register is derived from the DMAH_CH6_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH6_DMS:** The value of this register is derived from the DMAH_CH6_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH6_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH6_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH6_FC:** The value of this register is derived from the DMAH_CH6_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH6_HC_LLP:** The value of this register is derived from the DMAH_CH6_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH6_CTL_WB_EN:** The value of this register is derived from the DMAH_CH6_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**CH6_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH6_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH6_LOCK_EN:** The value of this register is derived from the DMAH_CH6_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH6_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH6_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH6_DST_SCA_EN:** The value of this register is derived from the DMAH_CH6_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH6_STAT_SRC:** The value of this register is derived from the DMAH_CH6_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH6_STAT_DST:** The value of this register is derived from the DMAH_CH6_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH6_STW:** The value of this register is derived from the DMAH_CH6_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH6_DTW:** The value of this register is derived from the DMAH_CH6_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.3.242 DW_ahb_dmac Component Parameters Register 5 - High (DMA_COMP_PARAMS_5_HI)—Offset 3D4h

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 5 and Channel 6. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h

31			28				24				20				16				12				8				4				0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Fields (bit 31 to bit 0): Undefined, CH5_FIFO_DEPTH, CH5_SMS, CH5_LMS, CH5_DMS, CH5_MAX_MULT_SIZE, CH5_FC, CH5_HC_LLP, CH5_CTL_WB_EN, CH5_MULTI_BLK_EN, CH5_LOCK_EN, CH5_SRC_GAT_EN, CH5_DST_SCA_EN, CH5_STAT_SRC, CH5_STAT_DST, CH5_STW, CH5_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH5_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH5_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH5_SMS:** The value of this register is derived from the DMAH_CH5_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH5_LMS:** The value of this register is derived from the DMAH_CH5_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
21:19	4h RO	**CH5_DMS:** The value of this register is derived from the DMAH_CH5_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH5_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH5_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH5_FC:** The value of this register is derived from the DMAH_CH5_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH5_HC_LLP:** The value of this register is derived from the DMAH_CH5_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH5_CTL_WB_EN:** The value of this register is derived from the DMAH_CH5_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH5_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH5_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH5_LOCK_EN:** The value of this register is derived from the DMAH_CH5_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH5_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH5_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH5_DST_SCA_EN:** The value of this register is derived from the DMAH_CH5_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH5_STAT_SRC:** The value of this register is derived from the DMAH_CH5_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**CH5_STAT_DST:** The value of this register is derived from the DMAH_CH5_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH5_STW:** The value of this register is derived from the DMAH_CH5_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH5_DTW:** The value of this register is derived from the DMAH_CH5_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.3.243 DW_ahb_dmac Component Parameters Register 4 - Low (DMA_COMP_PARAMS_4_LO)—Offset 3D8h

Refer to the description for DW_ahb_dmac Component Parameters Register 4 - High.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D8h

BAR Type: PCI Configuration Register (Size: 32 bits)

BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h

Bits	Default	Field
31	0	Undefined
30:28	0 1 1	CH4_FIFO_DEPTH
27:25	1 0 0	CH4_SMS
24:22	0 0 0	CH4_LMS
21:19	1 0 0	CH4_DMS
18:16	0 1 0	CH4_MAX_MULT_SIZE
15:14	0 0	CH4_FC
13	0	CH4_HC_LLP
12	0	CH4_CTL_WB_EN
11	0	CH4_MULTI_BLK_EN
10	0	CH4_LOCK_EN
9	1	CH4_SRC_GAT_EN
8	1	CH4_DST_SCA_EN
7	0	CH4_STAT_SRC
6	0	CH4_STAT_DST
5:3	0 0 0	CH4_STW
2:0	0 0 0	CH4_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
30:28	3h RO	**CH4_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH4_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH4_SMS:** The value of this register is derived from the DMAH_CH4_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH4_LMS:** The value of this register is derived from the DMAH_CH4_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH4_DMS:** The value of this register is derived from the DMAH_CH4_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH4_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH4_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH4_FC:** The value of this register is derived from the DMAH_CH4_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH4_HC_LLP:** The value of this register is derived from the DMAH_CH4_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH4_CTL_WB_EN:** The value of this register is derived from the DMAH_CH4_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**CH4_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH4_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH4_LOCK_EN:** The value of this register is derived from the DMAH_CH4_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH4_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH4_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH4_DST_SCA_EN:** The value of this register is derived from the DMAH_CH4_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH4_STAT_SRC:** The value of this register is derived from the DMAH_CH4_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH4_STAT_DST:** The value of this register is derived from the DMAH_CH4_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH4_STW:** The value of this register is derived from the DMAH_CH4_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH4_DTW:** The value of this register is derived from the DMAH_CH4_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.3.244 DW_ahb_dmac Component Parameters Register 4 - High (DMA_COMP_PARAMS_4_HI)—Offset 3DCh

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 3 and Channel 4. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h

Undefined	CH3_FIFO_DEPTH	CH3_SMS	CH3_LMS	CH3_DMS	CH3_MAX_MULT_SIZE	CH3_FC	CH3_HC_LLP	CH3_CTL_WB_EN	CH3_MULTI_BLK_EN	CH3_LOCK_EN	CH3_SRC_GAT_EN	CH3_DST_SCA_EN	CH3_STAT_SRC	CH3_STAT_DST	CH3_STW	CH3_DTW
0	0 1 1	1 0 0	0 0 0	1 0 0	0 1 0	0 0	0	0	0	0	1	1	0	0	0 0 0	0 0 0
31	30:28	27:25	24:22	21:19	18:16	15:14	13	12	11	10	9	8	7	6	5:3	2:0

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH3_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH3_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH3_SMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH3_LMS:** The value of this register is derived from the DMAH_CH3_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
21:19	4h RO	**CH3_DMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH3_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH3_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH3_FC:** The value of this register is derived from the DMAH_CH3_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH3_HC_LLP:** The value of this register is derived from the DMAH_CH3_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH3_CTL_WB_EN:** The value of this register is derived from the DMAH_CH3_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH3_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH3_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH3_LOCK_EN:** The value of this register is derived from the DMAH_CH3_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH3_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH3_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH3_DST_SCA_EN:** The value of this register is derived from the DMAH_CH3_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH3_STAT_SRC:** he value of this register is derived from the DMAH_CH3_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**CH3_STAT_DST:** The value of this register is derived from the DMAH_CH3_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH3_STW:** The value of this register is derived from the DMAH_CH3_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH3_DTW:** The value of this register is derived from the DMAH_CH3_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.3.245 DW_ahb_dmac Component Parameters Register 3 - Low (DMA_COMP_PARAMS_3_LO)—Offset 3E0h

Refer to the description for DW_ahb_dmac Component Parameters Register 3 - High.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h

31			28				24				20				16				12				8				4				0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Field
31	Undefined
30:28	CH2_FIFO_DEPTH
27:25	CH2_SMS
24:22	CH2_LMS
21:19	CH2_DMS
18:16	CH2_MAX_MULT_SIZE
15:14	CH2_FC
13	CH2_HC_LLP
12	CH2_CTL_WB_EN
11	CH2_MULTI_BLK_EN
10	CH2_LOCK_EN
9	CH2_SRC_GAT_EN
8	CH2_DST_SCA_EN
7	CH2_STAT_SRC
6	CH2_STAT_DST
5:3	CH2_STW
2:0	CH2_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
30:28	3h RO	**CH2_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH2_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH2_SMS:** The value of this register is derived from the DMAH_CH2_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH2_LMS:** The value of this register is derived from the DMAH_CH2_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH2_DMS:** The value of this register is derived from the DMAH_CH2_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH2_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH2_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH2_FC:** The value of this register is derived from the DMAH_CH2_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH2_HC_LLP:** The value of this register is derived from the DMAH_CH2_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH2_CTL_WB_EN:** The value of this register is derived from the DMAH_CH2_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**CH2_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH2_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to the spec. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH2_LOCK_EN:** The value of this register is derived from the DMAH_CH2_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH2_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH2_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH2_DST_SCA_EN:** The value of this register is derived from the DMAH_CH2_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH2_STAT_SRC:** The value of this register is derived from the DMAH_CH2_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH2_STAT_DST:** The value of this register is derived from the DMAH_CH2_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH2_STW:** The value of this register is derived from the DMAH_CH2_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH2_DTW:** The value of this register is derived from the DMAH_CH2_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.3.246 DW_ahb_dmac Component Parameters Register 3 - High (DMA_COMP_PARAMS_3_HI)—Offset 3E4h

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 1 and Channel 2. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 1 1	1 0 0 0	0 0 1 0	0 0 1 0	0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0

31	30:28	27:25	24:22	21:19	18:16	15:14	13	12	11	10	9	8	7	6	5:3	2:0
Undefined	CH1_FIFO_DEPTH	CH1_SMS	CH1_LMS	CH1_DMS	CH1_MAX_MULT_SIZE	CH1_FC	CH1_HC_LLP	CH1_CTL_WB_EN	CH1_MULTI_BLK_EN	CH1_LOCK_EN	CH1_SRC_GAT_EN	CH1_DST_SCA_EN	CH1_STAT_SRC	CH1_STAT_DST	CH1_STW	CH1_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH1_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH1_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH1_SMS:** The value of this register is derived from the DMAH_CH1_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH1_LMS:** The value of this register is derived from the DMAH_CH1_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
21:19	4h RO	**CH1_DMS:** The value of this register is derived from the DMAH_CH1_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH1_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH1_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH1_FC:** The value of this register is derived from the DMAH_CH1_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH1_HC_LLP:** The value of this register is derived from the DMAH_CH1_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH1_CTL_WB_EN:** The value of this register is derived from the DMAH_CH1_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH1_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH1_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH1_LOCK_EN:** The value of this register is derived from the DMAH_CH1_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH1_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH1_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH1_DST_SCA_EN:** The value of this register is derived from the DMAH_CH1_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH1_STAT_SRC:** The value of this register is derived from the DMAH_CH1_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**CH1_STAT_DST:** The value of this register is derived from the DMAH_CH1_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH1_STW:** The value of this register is derived from the DMAH_CH1_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH1_DTW:** The value of this register is derived from the DMAH_CH1_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.3.247 DW_ahb_dmac Component Parameters Register 2 - Low (DMA_COMP_PARAMS_2_LO)—Offset 3E8h

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h

31			28				24				20				16				12				8				4				0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
Undefined	CH0_FIFO_DEPTH			CH0_SMS			CH0_LMS			CH0_DMS			CH0_MAX_MULT_SIZE			CH0_FC		CH0_HC_LLP	CH0_CTL_WB_EN	CH0_MULTI_BLK_EN	CH0_LOCK_EN	CH0_SRC_GAT_EN	CH0_DST_SCA_EN	CH0_STAT_SRC	CH0_STAT_DST	CH0_STW			CH0_DTW		

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
30:28	3h RO	**CH0_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH0_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH0_SMS:** The value of this register is derived from the DMAH_CH0_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH0_LMS:** The value of this register is derived from the DMAH_CH0_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH0_DMS:** The value of this register is derived from the DMAH_CH0_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH0_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH0_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH0_FC:** The value of this register is derived from the DMAH_CH0_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH0_HC_LLP:** The value of this register is derived from the DMAH_CH0_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH0_CTL_WB_EN:** The value of this register is derived from the DMAH_CH0_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**CH0_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH0_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH0_LOCK_EN:** The value of this register is derived from the DMAH_CH0_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH0_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH0_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH0_DST_SCA_EN:** The value of this register is derived from the DMAH_CH0_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH0_STAT_SRC:** The value of this register is derived from the DMAH_CH0_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH0_STAT_DST:** The value of this register is derived from the DMAH_CH0_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH0_STW:** Refer to the description for bit field DMA_COMP_PARAMS_2_LO.CH0_DTW
2:0	0h RO	**CH0_DTW:** The value of this register is derived from the DMAH_CH0_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.3.248 DW_ahb_dmac Component Parameters Register 2 - High (DMA_COMP_PARAMS_2_HI)—Offset 3ECh

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
CH7_MULTI_BLK_TYPE	CH6_MULTI_BLK_TYPE	CH5_MULTI_BLK_TYPE	CH4_MULTI_BLK_TYPE	CH3_MULTI_BLK_TYPE	CH2_MULTI_BLK_TYPE	CH1_MULTI_BLK_TYPE	CH0_MULTI_BLK_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**CH7_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
27:24	0h RO	**CH6_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
23:20	0h RO	**CH5_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
19:16	0h RO	**CH4_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**CH3_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
11:8	0h RO	**CH2_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
7:4	0h RO	**CH1_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
3:0	0h RO	**CH0_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP

24.3.249 DW_ahb_dmac Component Parameters Register 1 - Low (DMA_COMP_PARAMS_1_LO)—Offset 3F0h

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: AAAAAAAAh

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0
CH7_MAX_BLK_SIZE	CH6_MAX_BLK_SIZE	CH5_MAX_BLK_SIZE	CH4_MAX_BLK_SIZE	CH3_MAX_BLK_SIZE	CH2_MAX_BLK_SIZE	CH1_MAX_BLK_SIZE	CH0_MAX_BLK_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:28	ah RO	**CH7_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. • 0h = 3 • 1h = 7 • 2h = 15 • 3h = 31 • 4h = 63 • 5h = 127 • 6h = 255 • 7h = 511 • 8h = 1023 • 9h = 2047 • Ah = 4095
27:24	ah RO	**CH6_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
23:20	ah RO	**CH5_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
19:16	ah RO	**CH4_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
15:12	ah RO	**CH3_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
11:8	ah RO	**CH2_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
7:4	ah RO	**CH1_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
3:0	ah RO	**CH0_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.

24.3.250 DW_ahb_dmac Component Parameters Register 1 - High (DMA_COMP_PARAMS_1_HI)—Offset 3F4h

Refer to the description for DW_ahb_dmac Component Parameters Register 1 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 37000F04h

31			28				24				20				16				12				8				4				0
0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0

Fields (bit 31 to bit 0): Undefined, STATIC_ENDIAN_SELECT, ADD_ENCODED_PARAMS, NUM_HS_INT, M4_HDATA_WIDTH, M3_HDATA_WIDTH, M2_HDATA_WIDTH, M1_HDATA_WIDTH, S_HDATA_WIDTH, NUM_MASTER_INT, NUM_CHANNELS, Undefined0, MABRST, INTR_IO, BIG_ENDIAN

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Undefined:** Reserved.
29	1h RO	**STATIC_ENDIAN_SELECT:** The value of this register is derived from the DMAH_STATIC_ENDIAN_SELECT coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE
28	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the DMAH_ADD_ENCODED_PARAMS coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE
27:23	0eh RO	**NUM_HS_INT:** The value of this register is derived from the DMAH_NUM_HS_INT coreConsultant parameter. For a description of this parameter, refer to page 102. • 0h0 = 0 • to • 1h0 = 16
22:21	0h RO	**M4_HDATA_WIDTH:** The value of this register is derived from the DMAH_M4_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits

Bit Range	Default & Access	Field Name (ID): Description
20:19	0h RO	**M3_HDATA_WIDTH:** The value of this register is derived from the DMAH_M3_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
18:17	0h RO	**M2_HDATA_WIDTH:** The value of this register is derived from the DMAH_M2_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
16:15	0h RO	**M1_HDATA_WIDTH:** The value of this register is derived from the DMAH_M1_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
14:13	0h RO	**S_HDATA_WIDTH:** The value of this register is derived from the DMAH_S_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
12:11	01h RO	**NUM_MASTER_INT:** The value of this register is derived from the DMAH_NUM_MASTER_INT coreConsultant parameter. For a description of this parameter, refer to page 102. 0h = 1 to 3h = 4
10:8	7h RO	**NUM_CHANNELS:** The value of this register is derived from the DMAH_NUM_CHANNELS coreConsultant parameter. For a description of this parameter, refer to page 102. 0h = 1 to 7h = 8
7:4	0h RW	**Undefined0:** Reserved.
3	0h RO	**MABRST:** The value of this register is derived from the DMAH_MABRST coreConsultant parameter. For a description of this parameter, refer to page 103. • 0 = FALSE • 1 = TRUE
2:1	2h RO	**INTR_IO:** The value of this register is derived from the DMAH_INTR_IO coreConsultant parameter. For a description of this parameter, refer to page 103. • 0h = ALL • 1h = TYPE • 2h = COMBINED • 3h = reserved
0	0h RO	**BIG_ENDIAN:** The value of this register is derived from the DMAH_BIG_ENDIAN coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE

24.3.251 DMA Component ID RegisterDma - Low (DmaCompsID_LO)—Offset 3F8h

This is the DW_ahb_dmac Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 44571110h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

DMA_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44571110h RO	**Designware Component Type (DMA_COMP_TYPE):** Designware Component Type number = 0x44_57_11_10. This assigned unique hex value is constant and is derived from the two ASCII letters -DW- followed by a 32-bit unsigned number.

24.3.252 DMA Component ID Register - High (DmaCompsID_HI)—Offset 3FCh

This is the DW_ahb_dmac Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 3231362Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	1	0	1	1	0	0	0	1	0	1	0	1	0

DMA_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3231362ah RO	**Version of the Component (DMA_COMP_VERSION):** Reserved.

24.4 SIO DMA PCI Configuration Registers for I^2C

Table 254. Summary of SIO DMA 2 PCI Configuration Registers—0/24/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3616	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3617	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3618	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3618	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 3619	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3620	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3620	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3621	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3621	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3622	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3622	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3623	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 3624	00000000h

24.4.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:0] + 0h

Default: 00008086h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 0 0 0 | 0 0 0 0 | 1 0 0 0 | 0 1 1 0

DEVICEID | VENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

24.4.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**Offset:** [B:0, D:24, F:0] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

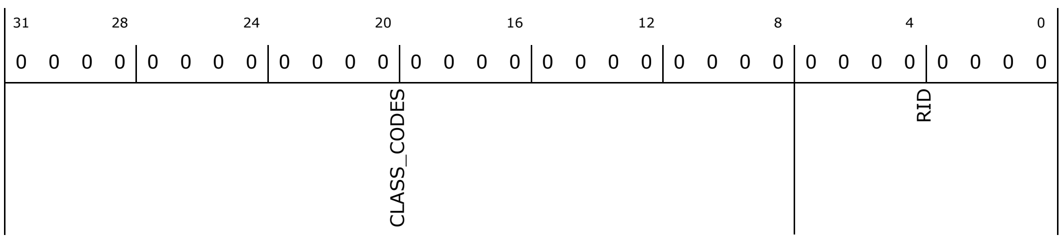
24.4.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

24.4.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:0] + Ch

Default: 00800000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved0								MULFNDEV	HEADERTYPE							LATTIMER								CACHELINE_SIZE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

24.4.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:0] + 10h

Default: 00000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	BASEADDR																				SIZEINDICATOR								PREFETCHABLE	TYPE		MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

24.4.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

24.4.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SUBSYSTEMID

SUBSYSTEMVENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

24.4.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

24.4.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 34h

Default: 00000000h

31:8	7:0
0000 0000 0000 0000 0000 0000	0000 0000
Reserved0	CAPPTR_POWER

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

24.4.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 3Ch

Default: 00000100h

31:24	23:16	15:12	11:8	7:0
0000 0000	0000 0000	0000	0001	0000 0000
MAX_LAT	MIN_GNT	Reserved0	INTPIN	INTLINE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

24.4.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 80h

Default: 00030001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields (bit 31 to bit 0): PMESUPPORT | Reserved0 | VERSION | NXTCAP | POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

24.4.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Fields (bit 31 to bit 0): Reserved0 | PMESTATUS | Reserved1 | PMEENABLE | Reserved2 | NO_SOFT_RESET | Reserved3 | POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

24.4.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

24.5 SIO DMA Memory Mapped I/O Registers for I2C

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Source Address Register for Channel 0 - Low (SAR0_LO)—Offset 0h" on page 3635	00000000h
4–7h	4	"Source Address Register for Channel 0 - High (SAR0_HI)—Offset 4h" on page 3635	00000000h
8–Bh	4	"Destination Address Register for Channel 0 - Low (DAR0_LO)—Offset 8h" on page 3636	00000000h
C–Fh	4	"Destination Address Register for Channel 0 - High (DAR0_HI)—Offset Ch" on page 3636	00000000h
10–13h	4	"Linked List Pointer Register for Channel 0 - Low (LLP0_LO)—Offset 10h" on page 3637	00000000h
14–17h	4	"Linked List Pointer Register for Channel 0 - High (LLP0_HI)—Offset 14h" on page 3637	00000000h
18–1Bh	4	"Control Register for Channel 0 - Low (CTL0_LO)—Offset 18h" on page 3638	00304801h
1C–1Fh	4	"Control Register for Channel 0 - High (CTL0_HI)—Offset 1Ch" on page 3639	00000002h
20–23h	4	"Source Status Register for Channel 0 - Low (SSTAT0_LO)—Offset 20h" on page 3640	00000000h
24–27h	4	"Source Status Register for Channel 0 - High (SSTAT0_HI)—Offset 24h" on page 3640	00000000h
28–2Bh	4	"Dest Status Register for Channel 0 - Low (DSTAT0_LO)—Offset 28h" on page 3641	00000000h
2C–2Fh	4	"Dest Status Register for Channel 0 - High (DSTAT0_HI)—Offset 2Ch" on page 3641	00000000h
30–33h	4	"Source Status Address Register for Channel 0 - Low (SSTATAR0_LO)—Offset 30h" on page 3642	00000000h
34–37h	4	"Source Status Address Register for Channel 0 - High (SSTATAR0_HI)—Offset 34h" on page 3642	00000000h
38–3Bh	4	"Dest Status Address Register for Channel 0 - Low (DSTATAR0_LO)—Offset 38h" on page 3643	00000000h
3C–3Fh	4	"Dest Status Address Register for Channel 0 - High (DSTATAR0_HI)—Offset 3Ch" on page 3643	00000000h
40–43h	4	"Configuration Register for Channel 0 - Low (CFG0_LO)—Offset 40h" on page 3644	00000E00h
44–47h	4	"Configuration Register for Channel 0 - High (CFG0_HI)—Offset 44h" on page 3645	00000004h
48–4Bh	4	"Source Gather Register for Channel 0 - Low (SGR0_LO)—Offset 48h" on page 3646	00000000h
4C–4Fh	4	"Source Gather Register for Channel 0 - High (SGR0_HI)—Offset 4Ch" on page 3647	00000000h
50–53h	4	"Destination Scatter Register for Channel 0 - Low (DSR0_LO)—Offset 50h" on page 3647	00000000h
54–57h	4	"Dest Scatter Register for Channel 0 - High (DSR0_HI)—Offset 54h" on page 3648	00000000h
58–5Bh	4	"Source Address Register for Channel 1 - Low (SAR1_LO)—Offset 58h" on page 3648	00000000h
5C–5Fh	4	"Source Address Register for Channel 1 - High (SAR1_HI)—Offset 5Ch" on page 3649	00000000h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
60–63h	4	"Destination Address Register for Channel 1 - Low (DAR1_LO)—Offset 60h" on page 3649	00000000h
64–67h	4	"Destination Address Register for Channel 1 - High (DAR1_HI)—Offset 64h" on page 3650	00000000h
68–6Bh	4	"Linked List Pointer Register for Channel 1 - Low (LLP1_LO)—Offset 68h" on page 3650	00000000h
6C–6Fh	4	"Linked List Pointer Register for Channel 1 - High (LLP1_HI)—Offset 6Ch" on page 3651	00000000h
70–73h	4	"Control Register for Channel 1 - Low (CTL1_LO)—Offset 70h" on page 3651	00304801h
74–77h	4	"Control Register for Channel 1 - High (CTL1_HI)—Offset 74h" on page 3652	00000002h
78–7Bh	4	"Source Status Register for Channel 1 - Low (SSTAT1_LO)—Offset 78h" on page 3653	00000000h
7C–7Fh	4	"Source Status Register for Channel 1 - High (SSTAT1_HI)—Offset 7Ch" on page 3653	00000000h
80–83h	4	"Dest Status Register for Channel 1 - Low (DSTAT1_LO)—Offset 80h" on page 3654	00000000h
84–87h	4	"Dest Status Register for Channel 1 - High (DSTAT1_HI)—Offset 84h" on page 3654	00000000h
88–8Bh	4	"Source Status Address Register for Channel 1 - Low (SSTATAR1_LO)—Offset 88h" on page 3655	00000000h
8C–8Fh	4	"Source Status Address Register for Channel 1 - High (SSTATAR1_HI)—Offset 8Ch" on page 3655	00000000h
90–93h	4	"Dest Status Address Register for Channel 1 - Low (DSTATAR1_LO)—Offset 90h" on page 3656	00000000h
94–97h	4	"Dest Status Address Register for Channel 1 - High (DSTATAR1_HI)—Offset 94h" on page 3656	00000000h
98–9Bh	4	"Configuration Register for Channel 1 - Low (CFG1_LO)—Offset 98h" on page 3657	00000E20h
9C–9Fh	4	"Configuration Register for Channel 1 - High (CFG1_HI)—Offset 9Ch" on page 3658	00000004h
A0–A3h	4	"Source Gather Register for Channel 1 - Low (SGR1_LO)—Offset A0h" on page 3659	00000000h
A4–A7h	4	"Source Gather Register for Channel 1 - High (SGR1_HI)—Offset A4h" on page 3660	00000000h
A8–ABh	4	"Destination Scatter Register for Channel 1 - Low (DSR1_LO)—Offset A8h" on page 3660	00000000h
AC–AFh	4	"Dest Scatter Register for Channel 1 - High (DSR1_HI)—Offset ACh" on page 3661	00000000h
B0–B3h	4	"Source Address Register for Channel 2 - Low (SAR2_LO)—Offset B0h" on page 3661	00000000h
B4–B7h	4	"Source Address Register for Channel 2 - High (SAR2_HI)—Offset B4h" on page 3662	00000000h
B8–BBh	4	"Destination Address Register for Channel 2 - Low (DAR2_LO)—Offset B8h" on page 3662	00000000h
BC–BFh	4	"Destination Address Register for Channel 2 - High (DAR2_HI)—Offset BCh" on page 3663	00000000h
C0–C3h	4	"Linked List Pointer Register for Channel 2 - Low (LLP2_LO)—Offset C0h" on page 3663	00000000h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C4–C7h	4	"Linked List Pointer Register for Channel 2 - High (LLP2_HI)—Offset C4h" on page 3664	00000000h
C8–CBh	4	"Control Register for Channel 2 - Low (CTL2_LO)—Offset C8h" on page 3664	00304801h
CC–CFh	4	"Control Register for Channel 2 - High (CTL2_HI)—Offset CCh" on page 3665	00000002h
D0–D3h	4	"Source Status Register for Channel 2 - Low (SSTAT2_LO)—Offset D0h" on page 3666	00000000h
D4–D7h	4	"Source Status Register for Channel 2 - High (SSTAT2_HI)—Offset D4h" on page 3666	00000000h
D8–DBh	4	"Dest Status Register for Channel 2 - Low (DSTAT2_LO)—Offset D8h" on page 3667	00000000h
DC–DFh	4	"Dest Status Register for Channel 2 - High (DSTAT2_HI)—Offset DCh" on page 3667	00000000h
E0–E3h	4	"Source Status Address Register for Channel 2 - Low (SSTATAR2_LO)—Offset E0h" on page 3668	00000000h
E4–E7h	4	"Source Status Address Register for Channel 2 - High (SSTATAR2_HI)—Offset E4h" on page 3668	00000000h
E8–EBh	4	"Dest Status Address Register for Channel 2 - Low (DSTATAR2_LO)—Offset E8h" on page 3669	00000000h
EC–EFh	4	"Dest Status Address Register for Channel 2 - High (DSTATAR2_HI)—Offset ECh" on page 3669	00000000h
F0–F3h	4	"Configuration Register for Channel 2 - Low (CFG2_LO)—Offset F0h" on page 3670	00000E40h
F4–F7h	4	"Configuration Register for Channel 2 - High (CFG2_HI)—Offset F4h" on page 3671	00000004h
F8–FBh	4	"Source Gather Register for Channel 2 - Low (SGR2_LO)—Offset F8h" on page 3672	00000000h
FC–FFh	4	"Source Gather Register for Channel 2 - High (SGR2_HI)—Offset FCh" on page 3673	00000000h
100–103h	4	"Destination Scatter Register for Channel 2 - Low (DSR2_LO)—Offset 100h" on page 3673	00000000h
104–107h	4	"Dest Scatter Register for Channel 2 - High (DSR2_HI)—Offset 104h" on page 3674	00000000h
108–10Bh	4	"Source Address Register for Channel 3 - Low (SAR3_LO)—Offset 108h" on page 3674	00000000h
10C–10Fh	4	"Source Address Register for Channel 3 - High (SAR3_HI)—Offset 10Ch" on page 3675	00000000h
110–113h	4	"Destination Address Register for Channel 3 - Low (DAR3_LO)—Offset 110h" on page 3675	00000000h
114–117h	4	"Destination Address Register for Channel 3 - High (DAR3_HI)—Offset 114h" on page 3676	00000000h
118–11Bh	4	"Linked List Pointer Register for Channel 3 - Low (LLP3_LO)—Offset 118h" on page 3676	00000000h
11C–11Fh	4	"Linked List Pointer Register for Channel 3 - High (LLP3_HI)—Offset 11Ch" on page 3677	00000000h
120–123h	4	"Control Register for Channel 3 - Low (CTL3_LO)—Offset 120h" on page 3677	00304801h
124–127h	4	"Control Register for Channel 3 - High (CTL3_HI)—Offset 124h" on page 3678	00000002h
128–12Bh	4	"Source Status Register for Channel 3 - Low (SSTAT3_LO)—Offset 128h" on page 3679	00000000h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
12C–12Fh	4	"Source Status Register for Channel 3 - High (SSTAT3_HI)—Offset 12Ch" on page 3679	00000000h
130–133h	4	"Dest Status Register for Channel 3 - Low (DSTAT3_LO)—Offset 130h" on page 3680	00000000h
134–137h	4	"Dest Status Register for Channel 3 - High (DSTAT3_HI)—Offset 134h" on page 3680	00000000h
138–13Bh	4	"Source Status Address Register for Channel 3 - Low (SSTATAR3_LO)—Offset 138h" on page 3681	00000000h
13C–13Fh	4	"Source Status Address Register for Channel 3 - High (SSTATAR3_HI)—Offset 13Ch" on page 3681	00000000h
140–143h	4	"Dest Status Address Register for Channel 3 - Low (DSTATAR3_LO)—Offset 140h" on page 3682	00000000h
144–147h	4	"Dest Status Address Register for Channel 3 - High (DSTATAR3_HI)—Offset 144h" on page 3682	00000000h
148–14Bh	4	"Configuration Register for Channel 3 - Low (CFG3_LO)—Offset 148h" on page 3683	00000E60h
14C–14Fh	4	"Configuration Register for Channel 3 - High (CFG3_HI)—Offset 14Ch" on page 3684	00000004h
150–153h	4	"Source Gather Register for Channel 3 - Low (SGR3_LO)—Offset 150h" on page 3685	00000000h
154–157h	4	"Source Gather Register for Channel 3 - High (SGR3_HI)—Offset 154h" on page 3686	00000000h
158–15Bh	4	"Destination Scatter Register for Channel 3 - Low (DSR3_LO)—Offset 158h" on page 3686	00000000h
15C–15Fh	4	"Dest Scatter Register for Channel 3 - High (DSR3_HI)—Offset 15Ch" on page 3687	00000000h
160–163h	4	"Source Address Register for Channel 4 - Low (SAR4_LO)—Offset 160h" on page 3687	00000000h
164–167h	4	"Source Address Register for Channel 4 - High (SAR4_HI)—Offset 164h" on page 3688	00000000h
168–16Bh	4	"Destination Address Register for Channel 4 - Low (DAR4_LO)—Offset 168h" on page 3688	00000000h
16C–16Fh	4	"Destination Address Register for Channel 4 - High (DAR4_HI)—Offset 16Ch" on page 3689	00000000h
170–173h	4	"Linked List Pointer Register for Channel 4 - Low (LLP4_LO)—Offset 170h" on page 3689	00000000h
174–177h	4	"Linked List Pointer Register for Channel 4 - High (LLP4_HI)—Offset 174h" on page 3690	00000000h
178–17Bh	4	"Control Register for Channel 4 - Low (CTL4_LO)—Offset 178h" on page 3690	00304801h
17C–17Fh	4	"Control Register for Channel 4 - High (CTL4_HI)—Offset 17Ch" on page 3691	00000002h
180–183h	4	"Source Status Register for Channel 4 - Low (SSTAT4_LO)—Offset 180h" on page 3692	00000000h
184–187h	4	"Source Status Register for Channel 4 - High (SSTAT4_HI)—Offset 184h" on page 3692	00000000h
188–18Bh	4	"Dest Status Register for Channel 4 - Low (DSTAT4_LO)—Offset 188h" on page 3693	00000000h
18C–18Fh	4	"Dest Status Register for Channel 4 - High (DSTAT4_HI)—Offset 18Ch" on page 3693	00000000h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
190–193h	4	"Source Status Address Register for Channel 4 - Low (SSTATAR4_LO)—Offset 190h" on page 3694	00000000h
194–197h	4	"Source Status Address Register for Channel 4 - High (SSTATAR4_HI)—Offset 194h" on page 3694	00000000h
198–19Bh	4	"Dest Status Address Register for Channel 4 - Low (DSTATAR4_LO)—Offset 198h" on page 3695	00000000h
19C–19Fh	4	"Dest Status Address Register for Channel 4 - High (DSTATAR4_HI)—Offset 19Ch" on page 3695	00000000h
1A0–1A3h	4	"Configuration Register for Channel 4 - Low (CFG4_LO)—Offset 1A0h" on page 3696	00000E80h
1A4–1A7h	4	"Configuration Register for Channel 4 - High (CFG4_HI)—Offset 1A4h" on page 3697	00000004h
1A8–1ABh	4	"Source Gather Register for Channel 4 - Low (SGR4_LO)—Offset 1A8h" on page 3698	00000000h
1AC–1AFh	4	"Source Gather Register for Channel 4 - High (SGR4_HI)—Offset 1ACh" on page 3699	00000000h
1B0–1B3h	4	"Destination Scatter Register for Channel 4 - Low (DSR4_LO)—Offset 1B0h" on page 3699	00000000h
1B4–1B7h	4	"Dest Scatter Register for Channel 4 - High (DSR4_HI)—Offset 1B4h" on page 3700	00000000h
1B8–1BBh	4	"Source Address Register for Channel 5 - Low (SAR5_LO)—Offset 1B8h" on page 3700	00000000h
1BC–1BFh	4	"Source Address Register for Channel 5 - High (SAR5_HI)—Offset 1BCh" on page 3701	00000000h
1C0–1C3h	4	"Destination Address Register for Channel 5 - Low (DAR5_LO)—Offset 1C0h" on page 3701	00000000h
1C4–1C7h	4	"Destination Address Register for Channel 5 - High (DAR5_HI)—Offset 1C4h" on page 3702	00000000h
1C8–1CBh	4	"Linked List Pointer Register for Channel 5 - Low (LLP5_LO)—Offset 1C8h" on page 3702	00000000h
1CC–1CFh	4	"Linked List Pointer Register for Channel 5 - High (LLP5_HI)—Offset 1CCh" on page 3703	00000000h
1D0–1D3h	4	"Control Register for Channel 5 - Low (CTL5_LO)—Offset 1D0h" on page 3703	00304801h
1D4–1D7h	4	"Control Register for Channel 5 - High (CTL5_HI)—Offset 1D4h" on page 3704	00000002h
1D8–1DBh	4	"Source Status Register for Channel 5 - Low (SSTAT5_LO)—Offset 1D8h" on page 3705	00000000h
1DC–1DFh	4	"Source Status Register for Channel 5 - High (SSTAT5_HI)—Offset 1DCh" on page 3705	00000000h
1E0–1E3h	4	"Dest Status Register for Channel 5 - Low (DSTAT5_LO)—Offset 1E0h" on page 3706	00000000h
1E4–1E7h	4	"Dest Status Register for Channel 5 - High (DSTAT5_HI)—Offset 1E4h" on page 3706	00000000h
1E8–1EBh	4	"Source Status Address Register for Channel 5 - Low (SSTATAR5_LO)—Offset 1E8h" on page 3707	00000000h
1EC–1EFh	4	"Source Status Address Register for Channel 5 - High (SSTATAR5_HI)—Offset 1ECh" on page 3707	00000000h
1F0–1F3h	4	"Dest Status Address Register for Channel 5 - Low (DSTATAR5_LO)—Offset 1F0h" on page 3708	00000000h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F4–1F7h	4	"Dest Status Address Register for Channel 5 - High (DSTATAR5_HI)—Offset 1F4h" on page 3708	00000000h
1F8–1FBh	4	"Configuration Register for Channel 5 - Low (CFG5_LO)—Offset 1F8h" on page 3709	00000EA0h
1FC–1FFh	4	"Configuration Register for Channel 5 - High (CFG5_HI)—Offset 1FCh" on page 3710	00000004h
200–203h	4	"Source Gather Register for Channel 5 - Low (SGR5_LO)—Offset 200h" on page 3711	00000000h
204–207h	4	"Source Gather Register for Channel 5 - High (SGR5_HI)—Offset 204h" on page 3712	00000000h
208–20Bh	4	"Destination Scatter Register for Channel 5 - Low (DSR5_LO)—Offset 208h" on page 3712	00000000h
20C–20Fh	4	"Dest Scatter Register for Channel 5 - High (DSR5_HI)—Offset 20Ch" on page 3713	00000000h
210–213h	4	"Source Address Register for Channel 6 - Low (SAR6_LO)—Offset 210h" on page 3713	00000000h
214–217h	4	"Source Address Register for Channel 6 - High (SAR6_HI)—Offset 214h" on page 3713	00000000h
218–21Bh	4	"Destination Address Register for Channel 6 - Low (DAR6_LO)—Offset 218h" on page 3714	00000000h
21C–21Fh	4	"Destination Address Register for Channel 6 - High (DAR6_HI)—Offset 21Ch" on page 3714	00000000h
220–223h	4	"Linked List Pointer Register for Channel 6 - Low (LLP6_LO)—Offset 220h" on page 3715	00000000h
224–227h	4	"Linked List Pointer Register for Channel 6 - High (LLP6_HI)—Offset 224h" on page 3715	00000000h
228–22Bh	4	"Control Register for Channel 6 - Low (CTL6_LO)—Offset 228h" on page 3716	00304801h
22C–22Fh	4	"Control Register for Channel 6 - High (CTL6_HI)—Offset 22Ch" on page 3717	00000002h
230–233h	4	"Source Status Register for Channel 6 - Low (SSTAT6_LO)—Offset 230h" on page 3718	00000000h
234–237h	4	"Source Status Register for Channel 6 - High (SSTAT6_HI)—Offset 234h" on page 3718	00000000h
238–23Bh	4	"Dest Status Register for Channel 6 - Low (DSTAT6_LO)—Offset 238h" on page 3719	00000000h
23C–23Fh	4	"Dest Status Register for Channel 6 - High (DSTAT6_HI)—Offset 23Ch" on page 3719	00000000h
240–243h	4	"Source Status Address Register for Channel 6 - Low (SSTATAR6_LO)—Offset 240h" on page 3720	00000000h
244–247h	4	"Source Status Address Register for Channel 6 - High (SSTATAR6_HI)—Offset 244h" on page 3720	00000000h
248–24Bh	4	"Dest Status Address Register for Channel 6 - Low (DSTATAR6_LO)—Offset 248h" on page 3721	00000000h
24C–24Fh	4	"Dest Status Address Register for Channel 6 - High (DSTATAR6_HI)—Offset 24Ch" on page 3721	00000000h
250–253h	4	"Configuration Register for Channel 6 - Low (CFG6_LO)—Offset 250h" on page 3722	00000EC0h
254–257h	4	"Configuration Register for Channel 6 - High (CFG6_HI)—Offset 254h" on page 3723	00000004h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
258–25Bh	4	"Source Gather Register for Channel 6 - Low (SGR6_LO)—Offset 258h" on page 3724	00000000h
25C–25Fh	4	"Source Gather Register for Channel 6 - High (SGR6_HI)—Offset 25Ch" on page 3724	00000000h
260–263h	4	"Destination Scatter Register for Channel 6 - Low (DSR6_LO)—Offset 260h" on page 3725	00000000h
264–267h	4	"Dest Scatter Register for Channel 6 - High (DSR6_HI)—Offset 264h" on page 3725	00000000h
268–26Bh	4	"Source Address Register for Channel 7 - Low (SAR7_LO)—Offset 268h" on page 3726	00000000h
26C–26Fh	4	"Source Address Register for Channel 7 - High (SAR7_HI)—Offset 26Ch" on page 3726	00000000h
270–273h	4	"Destination Address Register for Channel 7 - Low (DAR7_LO)—Offset 270h" on page 3727	00000000h
274–277h	4	"Destination Address Register for Channel 7 - High (DAR7_HI)—Offset 274h" on page 3727	00000000h
278–27Bh	4	"Linked List Pointer Register for Channel 7 - Low (LLP7_LO)—Offset 278h" on page 3728	00000000h
27C–27Fh	4	"Linked List Pointer Register for Channel 7 - High (LLP7_HI)—Offset 27Ch" on page 3728	00000000h
280–283h	4	"Control Register for Channel 7 - Low (CTL7_LO)—Offset 280h" on page 3729	00304801h
284–287h	4	"Control Register for Channel 7 - High (CTL7_HI)—Offset 284h" on page 3730	00000002h
288–28Bh	4	"Source Status Register for Channel 7 - Low (SSTAT7_LO)—Offset 288h" on page 3731	00000000h
28C–28Fh	4	"Source Status Register for Channel 7 - High (SSTAT7_HI)—Offset 28Ch" on page 3731	00000000h
290–293h	4	"Dest Status Register for Channel 7 - Low (DSTAT7_LO)—Offset 290h" on page 3732	00000000h
294–297h	4	"Dest Status Register for Channel 7 - High (DSTAT7_HI)—Offset 294h" on page 3732	00000000h
298–29Bh	4	"Source Status Address Register for Channel 7 - Low (SSTATAR7_LO)—Offset 298h" on page 3733	00000000h
29C–29Fh	4	"Source Status Address Register for Channel 7 - High (SSTATAR7_HI)—Offset 29Ch" on page 3733	00000000h
2A0–2A3h	4	"Dest Status Address Register for Channel 7 - Low (DSTATAR7_LO)—Offset 2A0h" on page 3734	00000000h
2A4–2A7h	4	"Dest Status Address Register for Channel 7 - High (DSTATAR7_HI)—Offset 2A4h" on page 3734	00000000h
2A8–2ABh	4	"Configuration Register for Channel 7 - Low (CFG7_LO)—Offset 2A8h" on page 3735	00000EE0h
2AC–2AFh	4	"Configuration Register for Channel 7 - High (CFG7_HI)—Offset 2ACh" on page 3736	00000004h
2B0–2B3h	4	"Source Gather Register for Channel 7 - Low (SGR7_LO)—Offset 2B0h" on page 3737	00000000h
2B4–2B7h	4	"Source Gather Register for Channel 7 - High (SGR7_HI)—Offset 2B4h" on page 3737	00000000h
2B8–2BBh	4	"Destination Scatter Register for Channel 7 - Low (DSR7_LO)—Offset 2B8h" on page 3738	00000000h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2BC–2BFh	4	"Dest Scatter Register for Channel 7 - High (DSR7_HI)—Offset 2BCh" on page 3738	00000000h
2C0–2C3h	4	"Interrupt Raw Status Registers - Low (RawTfr_LO)—Offset 2C0h" on page 3739	00000000h
2C4–2C7h	4	"Interrupt Raw Status Registers - High (RawTfr_HI)—Offset 2C4h" on page 3740	00000000h
2C8–2CBh	4	"Interrupt Raw Status Registers - Low (RawBlock_LO)—Offset 2C8h" on page 3740	00000000h
2CC–2CFh	4	"Interrupt Raw Status Registers - High (RawBlock_HI)—Offset 2CCh" on page 3741	00000000h
2D0–2D3h	4	"Interrupt Raw Status Registers - Low (RawSrcTran_LO)—Offset 2D0h" on page 3741	00000000h
2D4–2D7h	4	"Interrupt Raw Status Registers - High (RawSrcTran_HI)—Offset 2D4h" on page 3742	00000000h
2D8–2DBh	4	"Interrupt Raw Status Registers - Low (RawDstTran_LO)—Offset 2D8h" on page 3742	00000000h
2DC–2DFh	4	"Interrupt Raw Status Registers - High (RawDstTran_HI)—Offset 2DCh" on page 3743	00000000h
2E0–2E3h	4	"Interrupt Raw Status Registers - Low (RawErr_LO)—Offset 2E0h" on page 3743	00000000h
2E4–2E7h	4	"Interrupt Raw Status Registers - High (RawErr_HI)—Offset 2E4h" on page 3744	00000000h
2E8–2EBh	4	"Interrupt Status Registers - Low (StatusTfr_LO)—Offset 2E8h" on page 3744	00000000h
2EC–2EFh	4	"Interrupt Status Registers - High (StatusTfr_HI)—Offset 2ECh" on page 3745	00000000h
2F0–2F3h	4	"Interrupt Status Registers - Low (StatusBlock_LO)—Offset 2F0h" on page 3745	00000000h
2F4–2F7h	4	"Interrupt Status Registers - High (StatusBlock_HI)—Offset 2F4h" on page 3746	00000000h
2F8–2FBh	4	"Interrupt Status Registers - Low (StatusSrcTran_LO)—Offset 2F8h" on page 3746	00000000h
2FC–2FFh	4	"Interrupt Status Registers - High (StatusSrcTran_HI)—Offset 2FCh" on page 3747	00000000h
300–303h	4	"Interrupt Status Registers - Low (StatusDstTran_LO)—Offset 300h" on page 3747	00000000h
304–307h	4	"Interrupt Status Registers - High (StatusDstTran_HI)—Offset 304h" on page 3748	00000000h
308–30Bh	4	"Interrupt Status Registers - Low (StatusErr_LO)—Offset 308h" on page 3748	00000000h
30C–30Fh	4	"Interrupt Status Registers - High (StatusErr_HI)—Offset 30Ch" on page 3749	00000000h
310–313h	4	"Interrupt Mask Registers - Low (MaskTfr_LO)—Offset 310h" on page 3749	00000000h
314–317h	4	"Interrupt Mask Registers - High (MaskTfr_HI)—Offset 314h" on page 3750	00000000h
318–31Bh	4	"Interrupt Mask Registers - Low (MaskBlock_LO)—Offset 318h" on page 3750	00000000h
31C–31Fh	4	"Interrupt Mask Registers - High (MaskBlock_HI)—Offset 31Ch" on page 3751	00000000h
320–323h	4	"Interrupt Mask Registers - Low (MaskSrcTran_LO)—Offset 320h" on page 3751	00000000h
324–327h	4	"Interrupt Mask Registers - High (MaskSrcTran_HI)—Offset 324h" on page 3752	00000000h
328–32Bh	4	"Interrupt Mask Registers - Low (MaskDstTran_LO)—Offset 328h" on page 3752	00000000h
32C–32Fh	4	"Interrupt Mask Registers - High (MaskDstTran_HI)—Offset 32Ch" on page 3753	00000000h
330–333h	4	"Interrupt Mask Registers - Low (MaskErr_LO)—Offset 330h" on page 3753	00000000h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
334–337h	4	"Interrupt Mask Registers - High (MaskErr_HI)—Offset 334h" on page 3754	00000000h
338–33Bh	4	"Interrupt Clear Registers - Low (ClearTfr_LO)—Offset 338h" on page 3754	00000000h
33C–33Fh	4	"Interrupt Clear Registers - High (ClearTfr_HI)—Offset 33Ch" on page 3755	00000000h
340–343h	4	"Interrupt Clear Registers - Low (ClearBlock_LO)—Offset 340h" on page 3756	00000000h
344–347h	4	"Interrupt Clear Registers (ClearBlock_HI)—Offset 344h" on page 3756	00000000h
348–34Bh	4	"Interrupt Clear Registers - Low (ClearSrcTran_LO)—Offset 348h" on page 3757	00000000h
34C–34Fh	4	"Interrupt Clear RegistersClearSrc - High (ClearSrcTran_HI)—Offset 34Ch" on page 3757	00000000h
350–353h	4	"Interrupt Clear Registers - Low (ClearDstTran_LO)—Offset 350h" on page 3758	00000000h
354–357h	4	"Interrupt Clear Registers - High (ClearDstTran_HI)—Offset 354h" on page 3758	00000000h
358–35Bh	4	"Interrupt Clear Registers - Low (ClearErr_LO)—Offset 358h" on page 3759	00000000h
35C–35Fh	4	"Interrupt Clear Registers - High (ClearErr_HI)—Offset 35Ch" on page 3759	00000000h
360–363h	4	"Combined Interrupt Status Register - Low (StatusInt_LO)—Offset 360h" on page 3760	00000000h
364–367h	4	"Combined Interrupt Status Register - High (StatusInt_HI)—Offset 364h" on page 3760	00000000h
368–36Bh	4	"Source Software Transaction Request Register - Low (ReqSrcReg_LO)—Offset 368h" on page 3761	00000000h
36C–36Fh	4	"Source Software Transaction Request Register - High (ReqSrcReg_HI)—Offset 36Ch" on page 3762	00000000h
370–373h	4	"Destination Software Transaction Request Register - Low (ReqDstReg_LO)—Offset 370h" on page 3762	00000000h
374–377h	4	"Destination Software Transaction Request Register - High (ReqDstReg_HI)—Offset 374h" on page 3763	00000000h
378–37Bh	4	"Single Source Software Transaction Request Register - Low (SglRqSrcReg_LO)—Offset 378h" on page 3763	00000000h
37C–37Fh	4	"Single Source Software Transaction Request Register - High (SglRqSrcReg_HI)—Offset 37Ch" on page 3764	00000000h
380–383h	4	"Single Destination Software Transaction Request Register - Low (SglRqDstReg_LO)—Offset 380h" on page 3765	00000000h
384–387h	4	"Single Destination Software Transaction Request Register - High (SglRqDstReg_HI)—Offset 384h" on page 3765	00000000h
388–38Bh	4	"Last Source Transaction Request Register - Low (LstSrcReg_LO)—Offset 388h" on page 3766	00000000h
38C–38Fh	4	"Last Source Transaction Request Register - High (LstSrcReg_HI)—Offset 38Ch" on page 3766	00000000h
390–393h	4	"Last Destination Transaction Request Register - Low (LstDstReg_LO)—Offset 390h" on page 3767	00000000h
394–397h	4	"Last Destination Transaction Request Register - High (LstDstReg_HI)—Offset 394h" on page 3768	00000000h
398–39Bh	4	"DW_ahb_dmac Configuration Register - Low (DmaCfgReg_LO)—Offset 398h" on page 3768	00000000h
39C–39Fh	4	"DW_ahb_dmac Configuration Register - High (DmaCfgReg_HI)—Offset 39Ch" on page 3769	00000000h
3A0–3A3h	4	"DW_ahb_dmac Channel Enable Register - Low (ChEnReg_LO)—Offset 3A0h" on page 3769	00000000h

Table 255. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3A4–3A7h	4	"DW_ahb_dmac Channel Enable Register - High (ChEnReg_HI)—Offset 3A4h" on page 3770	00000000h
3A8–3ABh	4	"DW_ahb_dmac ID Register - Low (DmaIdReg_LO)—Offset 3A8h" on page 3770	C0CAC01Ah
3AC–3AFh	4	"DW_ahb_dmac ID Register - High (DmaIdReg_HI)—Offset 3ACh" on page 3771	00000000h
3B0–3B3h	4	"DW_ahb_dmac Test Register - Low (DmaTestReg_LO)—Offset 3B0h" on page 3771	00000000h
3B4–3B7h	4	"DW_ahb_dmac Test Register - High (DmaTestReg_HI)—Offset 3B4h" on page 3772	00000000h
3C8–3CBh	4	"DW_ahb_dmac Component Parameters Register 6 - Low (DMA_COMP_PARAMS_6_LO)—Offset 3C8h" on page 3772	00000000h
3CC–3CFh	4	"DW_ahb_dmac Component Parameters Register 6 - High (DMA_COMP_PARAMS_6_HI)—Offset 3CCh" on page 3773	38220300h
3D0–3D3h	4	"DW_ahb_dmac Component Parameters Register 5 - Low (DMA_COMP_PARAMS_5_LO)—Offset 3D0h" on page 3775	38220300h
3D4–3D7h	4	"DW_ahb_dmac Component Parameters Register 5 - High (DMA_COMP_PARAMS_5_HI)—Offset 3D4h" on page 3778	38220300h
3D8–3DBh	4	"DW_ahb_dmac Component Parameters Register 4 - Low (DMA_COMP_PARAMS_4_LO)—Offset 3D8h" on page 3780	38220300h
3DC–3DFh	4	"DW_ahb_dmac Component Parameters Register 4 - High (DMA_COMP_PARAMS_4_HI)—Offset 3DCh" on page 3783	38220300h
3E0–3E3h	4	"DW_ahb_dmac Component Parameters Register 3 - Low (DMA_COMP_PARAMS_3_LO)—Offset 3E0h" on page 3785	38220300h
3E4–3E7h	4	"DW_ahb_dmac Component Parameters Register 3 - High (DMA_COMP_PARAMS_3_HI)—Offset 3E4h" on page 3788	38220300h
3E8–3EBh	4	"DW_ahb_dmac Component Parameters Register 2 - Low (DMA_COMP_PARAMS_2_LO)—Offset 3E8h" on page 3790	38220300h
3EC–3EFh	4	"DW_ahb_dmac Component Parameters Register 2 - High (DMA_COMP_PARAMS_2_HI)—Offset 3ECh" on page 3792	00000000h
3F0–3F3h	4	"DW_ahb_dmac Component Parameters Register 1 - Low (DMA_COMP_PARAMS_1_LO)—Offset 3F0h" on page 3795	AAAAAAAAh
3F4–3F7h	4	"DW_ahb_dmac Component Parameters Register 1 - High (DMA_COMP_PARAMS_1_HI)—Offset 3F4h" on page 3796	37000F04h
3F8–3FBh	4	"DMA Component ID RegisterDma - Low (DmaCompsID_LO)—Offset 3F8h" on page 3798	44571110h
3FC–3FFh	4	"DMA Component ID Register - High (DmaCompsID_HI)—Offset 3FCh" on page 3799	3231362Ah

24.5.1 Source Address Register for Channel 0 - Low (SAR0_LO)—Offset 0h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current AHB transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAR																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.5.2 Source Address Register for Channel 0 - High (SAR0_HI)—Offset 4h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.3 Destination Address Register for Channel 0 - Low (DAR0_LO)—Offset 8h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before thestart of the DMA transfer. While the DMA transfer is inprogress, this register is updated to reflect the destination address of the current AHB transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.5.4 Destination Address Register for Channel 0 - High (DAR0_HI)—Offset Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.5 Linked List Pointer Register for Channel 0 - Low (LLP0_LO)—Offset 10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: LOC (bits 31:2), LMS (bits 1:0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.5.6 Linked List Pointer Register for Channel 0 - High (LLP0_HI)—Offset 14h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.7 Control Register for Channel 0 - Low (CTL0_LO)—Offset 18h

This register contains fields that control the DMA transfer. **Note:** You need to program this register prior to enabling the channel.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Undefined_	LLP_SRC_EN	LLP_DST_EN	SMS	DMS	TT_FC	Undefined	DST_SCATTER_EN	SRC_GATHER_EN	SRC_MSIZE	DEST_MSIZE	SINC	DINC	SRC_TR_WIDTH	DST_TR_WIDTH	INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** The following transfer types are supported. • Memory to Memory • Memory to Peripheral • Peripheral to Memory • Peripheral to Peripheral Flow Control can be assigned to the DW_ahb_dmac, the source peripheral, or the destination peripheral.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Number of data items, each of width CTLx.SRC_TR_WIDTH, to be read from the source every time a source burst transaction request is made from either the corresponding hardware or software handshaking interface.

Bit Range	Default & Access	Field Name (ID): Description
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Number of data items, each of width CTLx.DST_TR_WIDTH, to be written to the destination every time a destination burst transaction request is made from either the corresponding hardware or software handshaking interface.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.5.8 Control Register for Channel 0 - High (CTL0_HI)—Offset 1Ch

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Undefined_ | DONE | BLOCK_TS

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** If status write-back is enabled, the upper word of the control register, CTLx[63:32], is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTLx.DONE bit to see when a block transfer is complete. The LLI CTLx.DONE bit should be cleared when the linked lists are set up in memory, prior to enabling the channel. LLI accesses are always 32-bit accesses (Hsize = 2) aligned to 32-bit boundaries and cannot be changed or programmed to anything other than 32-bit.

Bit Range	Default & Access	Field Name (ID): Description
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.5.9 Source Status Register for Channel 0 - Low (SSTAT0_LO)—Offset 20h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.5.10 Source Status Register for Channel 0 - High (SSTAT0_HI)—Offset 24h

Refer to the description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.11 Dest Status Register for Channel 0 - Low (DSTAT0_LO)—Offset 28h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI before the start of the next block. For conditions under which the destination status information is fetched, refer to the abovementioned spec.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

24.5.12 Dest Status Register for Channel 0 - High (DSTAT0_HI)—Offset 2Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.13 Source Status Address Register for Channel 0 - Low (SSTATAR0_LO)—Offset 30h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.14 Source Status Address Register for Channel 0 - High (SSTATAR0_HI)—Offset 34h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.15 Dest Status Address Register for Channel 0 - Low (DSTATAR0_LO)—Offset 38h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.16 Dest Status Address Register for Channel 0 - High (DSTATAR0_HI)—Offset 3Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.17 Configuration Register for Channel 0 - Low (CFG0_LO)—Offset 40h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. **Note:** You need to program this register prior to enabling the channel.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E00h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
RELOAD_DST	RELOAD_SRC	MAX_ABRST										SRC_HS_POL	DST_HS_POL	LOCK_B	LOCK_CH	LOCK_B_L		LOCK_CH_L		HS_SEL_SRC	HS_SEL_DST	FIFO_EMPTY	CH_SUSP	CH_PRIOR			Undefined				

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	0h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.5.18 Configuration Register for Channel 0 - High (CFG0_HI)—Offset 44h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h

Bits	31:15	14:11	10:7	6	5	4:2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0	0	1 0 0	0	0
Field	Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.5.19 Source Gather Register for Channel 0 - Low (SGR0_LO)—Offset 48h

The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer.

24.5.20 Source Gather Register for Channel 0 - High (SGR0_HI)—Offset 4Ch

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.21 Destination Scatter Register for Channel 0 - Low (DSR0_LO)—Offset 50h

The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC (bits 31:20) | DSI (bits 19:0)

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary, when scatter mode is enabled for the destination transfer.

24.5.22 Dest Scatter Register for Channel 0 - High (DSR0_HI)—Offset 54h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.23 Source Address Register for Channel 1 - Low (SAR1_LO)—Offset 58h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.5.24 Source Address Register for Channel 1 - High (SAR1_HI)—Offset 5Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.25 Destination Address Register for Channel 1 - Low (DAR1_LO)—Offset 60h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.5.26 Destination Address Register for Channel 1 - High (DAR1_HI)—Offset 64h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.27 Linked List Pointer Register for Channel 1 - Low (LLP1_LO)—Offset 68h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC | LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.5.28 Linked List Pointer Register for Channel 1 - High (LLP1_HI)—Offset 6Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.29 Control Register for Channel 1 - Low (CTL1_LO)—Offset 70h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Undefined_, LLP_SRC_EN, LLP_DST_EN, SMS, DMS, TT_FC, Undefined, DST_SCATTER_EN, SRC_GATHER_EN, SRC_MSIZE, DEST_MSIZE, SINC, DINC, SRC_TR_WIDTH, DST_TR_WIDTH, INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.5.30 Control Register for Channel 1 - High (CTL1_HI)—Offset 74h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h

31	28			24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Fields: Undefined_ (31:13), DONE (12), BLOCK_TS (11:0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled, to indicate the block size.

24.5.31 Source Status Register for Channel 1 - Low (SSTAT1_LO)—Offset 78h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28			24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: SSTAT (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.5.32 Source Status Register for Channel 1 - High (SSTAT1_HI)—Offset 7Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.33 Dest Status Register for Channel 1 - Low (DSTAT1_LO)—Offset 80h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4			0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest. status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

24.5.34 Dest Status Register for Channel 1 - High (DSTAT1_HI)—Offset 84h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.35 Source Status Address Register for Channel 1 - Low (SSTATAR1_LO)—Offset 88h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.36 Source Status Address Register for Channel 1 - High (SSTATAR1_HI)—Offset 8Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.37 Dest Status Address Register for Channel 1 - Low (DSTATAR1_LO)—Offset 90h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.38 Dest Status Address Register for Channel 1 - High (DSTATAR1_HI)—Offset 94h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field: Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.39 Configuration Register for Channel 1 - Low (CFG1_LO)—Offset 98h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E20h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0

Fields: RELOAD_DST (31), RELOAD_SRC (30), MAX_ABRST (29:20), SRC_HS_POL (19), DST_HS_POL (18), LOCK_B (17), LOCK_CH (16), LOCK_B_L (15:14), LOCK_CH_L (13:12), HS_SEL_SRC (11), HS_SEL_DST (10), FIFO_EMPTY (9), CH_SUSP (8), CH_PRIOR (7:5), Undefined (4:0)

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	1h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.5.40 Configuration Register for Channel 1 - High (CFG1_HI)—Offset 9Ch

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Field
31:15	Undefined
14:11	DEST_PER
10:7	SRC_PER
6	SS_UPD_EN
5	DS_UPD_EN
4:2	PROTCTL
1	FIFO_MODE
0	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.5.41 Source Gather Register for Channel 1 - Low (SGR1_LO)—Offset A0h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.5.42 Source Gather Register for Channel 1 - High (SGR1_HI)—Offset A4h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.43 Destination Scatter Register for Channel 1 - Low (DSR1_LO)—Offset A8h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC (bits 31:20), DSI (bits 19:0)

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.5.44 Dest Scatter Register for Channel 1 - High (DSR1_HI)—Offset ACh

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.45 Source Address Register for Channel 2 - Low (SAR2_LO)—Offset B0h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.5.46 Source Address Register for Channel 2 - High (SAR2_HI)—Offset B4h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.47 Destination Address Register for Channel 2 - Low (DAR2_LO)—Offset B8h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.5.48 Destination Address Register for Channel 2 - High (DAR2_HI)—Offset BCh

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.49 Linked List Pointer Register for Channel 2 - Low (LLP2_LO)—Offset C0h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

LOC | LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.5.50 Linked List Pointer Register for Channel 2 - High (LLP2_HI)—Offset C4h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.51 Control Register for Channel 2 - Low (CTL2_LO)—Offset C8h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Fields: Undefined_, LLP_SRC_EN, LLP_DST_EN, SMS, DMS, TT_FC, Undefined, DST_SCATTER_EN, SRC_GATHER_EN, SRC_MSIZE, DEST_MSIZE, SINC, DINC, SRC_TR_WIDTH, DST_TR_WIDTH, INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.5.52 Control Register for Channel 2 - High (CTL2_HI)—Offset CCh

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Field	Undefined_																			DONE	BLOCK_TS											

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.5.53 Source Status Register for Channel 2 - Low (SSTAT2_LO)—Offset D0h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	SSTAT																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register.

24.5.54 Source Status Register for Channel 2 - High (SSTAT2_HI)—Offset D4h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.55 Dest Status Register for Channel 2 - Low (DSTAT2_LO)—Offset D8h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register.

24.5.56 Dest Status Register for Channel 2 - High (DSTAT2_HI)—Offset DCh

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.57 Source Status Address Register for Channel 2 - Low (SSTATAR2_LO)—Offset E0h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.58 Source Status Address Register for Channel 2 - High (SSTATAR2_HI)—Offset E4h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.59 Dest Status Address Register for Channel 2 - Low (DSTATAR2_LO)—Offset E8h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.60 Dest Status Address Register for Channel 2 - High (DSTATAR2_HI)—Offset ECh

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.61 Configuration Register for Channel 2 - Low (CFG2_LO)—Offset F0h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E40h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0

RELOAD_DST, RELOAD_SRC, MAX_ABRST, SRC_HS_POL, DST_HS_POL, LOCK_B, LOCK_CH, LOCK_B_L, LOCK_CH_L, HS_SEL_SRC, HS_SEL_DST, FIFO_EMPTY, CH_SUSP, CH_PRIOR, Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	2h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.5.62 Configuration Register for Channel 2 - High (CFG2_HI)—Offset F4h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Field
31:15	Undefined
14:11	DEST_PER
10:7	SRC_PER
6	SS_UPD_EN
5	DS_UPD_EN
4:2	PROTCTL
1	FIFO_MODE
0	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.5.63 Source Gather Register for Channel 2 - Low (SGR2_LO)—Offset F8h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31:20	19:0
0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SGC	SGI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.5.64 Source Gather Register for Channel 2 - High (SGR2_HI)—Offset FCh

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.65 Destination Scatter Register for Channel 2 - Low (DSR2_LO)—Offset 100h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC | DSI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.5.66 Dest Scatter Register for Channel 2 - High (DSR2_HI)—Offset 104h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 104h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.67 Source Address Register for Channel 3 - Low (SAR3_LO)—Offset 108h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.5.68 Source Address Register for Channel 3 - High (SAR3_HI)—Offset 10Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.69 Destination Address Register for Channel 3 - Low (DAR3_LO)—Offset 110h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.5.70 Destination Address Register for Channel 3 - High (DAR3_HI)—Offset 114h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 114h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.71 Linked List Pointer Register for Channel 3 - Low (LLP3_LO)—Offset 118h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC | LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.5.72 Linked List Pointer Register for Channel 3 - High (LLP3_HI)—Offset 11Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 11Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Field: Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.73 Control Register for Channel 3 - Low (CTL3_LO)—Offset 120h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h

Bits 31–0: 0 0 0 0 | 0 0 0 0 | 0 0 1 1 | 0 0 0 0 | 0 1 0 0 | 1 0 0 0 | 0 0 0 0 | 0 0 0 1

Fields (31 to 0): Undefined_, LLP_SRC_EN, LLP_DST_EN, SMS, DMS, TT_FC, Undefined, DST_SCATTER_EN, SRC_GATHER_EN, SRC_MSIZE, DEST_MSIZE, SINC, DINC, SRC_TR_WIDTH, DST_TR_WIDTH, INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.5.74 Control Register for Channel 3 - High (CTL3_HI)—Offset 124h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Undefined_																			DONE	BLOCK_TS											

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.5.75 Source Status Register for Channel 3 - Low (SSTAT3_LO)—Offset 128h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 128h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTAT																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.5.76 Source Status Register for Channel 3 - High (SSTAT3_HI)—Offset 12Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 12Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.77 Dest Status Register for Channel 3 - Low (DSTAT3_LO)—Offset 130h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 130h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.5.78 Dest Status Register for Channel 3 - High (DSTAT3_HI)—Offset 134h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 134h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.79 Source Status Address Register for Channel 3 - Low (SSTATAR3_LO)—Offset 138h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 138h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.80 Source Status Address Register for Channel 3 - High (SSTATAR3_HI)—Offset 13Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 13Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.81 Dest Status Address Register for Channel 3 - Low (DSTATAR3_LO)—Offset 140h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 140h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.82 Dest Status Address Register for Channel 3 - High (DSTATAR3_HI)—Offset 144h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 144h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

Bits	31–0
Value	0000 0000 0000 0000 0000 0000 0000 0000
Field	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.83 Configuration Register for Channel 3 - Low (CFG3_LO)—Offset 148h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E60h

Bits	Value	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:20	0000000000	MAX_ABRST
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	LOCK_B
16	0	LOCK_CH
15:14	00	LOCK_B_L
13:12	00	LOCK_CH_L
11	1	HS_SEL_SRC
10	1	HS_SEL_DST
9	1	FIFO_EMPTY
8	0	CH_SUSP
7:5	011	CH_PRIOR
4:0	00000	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	3h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.5.84 Configuration Register for Channel 3 - High (CFG3_HI)—Offset 14Ch

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h

Bits	31:15	14:11	10:7	6	5	4:2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0	0	0	1 0 0	0	0
Field	Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced, when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.5.85 Source Gather Register for Channel 3 - Low (SGR3_LO)—Offset 150h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.5.86 Source Gather Register for Channel 3 - High (SGR3_HI)—Offset 154h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 154h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Undefined							

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.87 Destination Scatter Register for Channel 3 - Low (DSR3_LO)—Offset 158h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
DSC			DSI				

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.5.88 Dest Scatter Register for Channel 3 - High (DSR3_HI)—Offset 15Ch

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 15Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.89 Source Address Register for Channel 4 - Low (SAR4_LO)—Offset 160h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.5.90 Source Address Register for Channel 4 - High (SAR4_HI)—Offset 164h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 164h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.91 Destination Address Register for Channel 4 - Low (DAR4_LO)—Offset 168h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.5.92 Destination Address Register for Channel 4 - High (DAR4_HI)—Offset 16Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 16Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.93 Linked List Pointer Register for Channel 4 - Low (LLP4_LO)—Offset 170h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.5.94 Linked List Pointer Register for Channel 4 - High (LLP4_HI)—Offset 174h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 174h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.95 Control Register for Channel 4 - Low (CTL4_LO)—Offset 178h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 1 0 0	1 0 0 0	0 0 0 0	0 0 0 1	

Fields (from bit 31 to bit 0): Undefined_, LLP_SRC_EN, LLP_DST_EN, SMS, DMS, TT_FC, Undefined, DST_SCATTER_EN, SRC_GATHER_EN, SRC_MSIZE, DEST_MSIZE, SINC, DINC, SRC_TR_WIDTH, DST_TR_WIDTH, INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.5.96 Control Register for Channel 4 - High (CTL4_HI)—Offset 17Ch

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Undefined_																			DONE	BLOCK_TS											

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.5.97 Source Status Register for Channel 4 - Low (SSTAT4_LO)—Offset 180h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 180h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTAT																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register.

24.5.98 Source Status Register for Channel 4 - High (SSTAT4_HI)—Offset 184h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 184h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.99 Dest Status Register for Channel 4 - Low (DSTAT4_LO)—Offset 188h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 188h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.5.100 Dest Status Register for Channel 4 - High (DSTAT4_HI)—Offset 18Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.101 Source Status Address Register for Channel 4 - Low (SSTATAR4_LO)—Offset 190h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 190h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.102 Source Status Address Register for Channel 4 - High (SSTATAR4_HI)—Offset 194h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 194h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.103 Dest Status Address Register for Channel 4 - Low (DSTATAR4_LO)—Offset 198h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 198h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.104 Dest Status Address Register for Channel 4 - High (DSTATAR4_HI)—Offset 19Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 19Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.105 Configuration Register for Channel 4 - Low (CFG4_LO)—Offset 1A0h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E80h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0

RELOAD_DST, RELOAD_SRC, MAX_ABRST, SRC_HS_POL, DST_HS_POL, LOCK_B, LOCK_CH, LOCK_B_L, LOCK_CH_L, HS_SEL_SRC, HS_SEL_DST, FIFO_EMPTY, CH_SUSP, CH_PRIOR, Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	4h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.5.106 Configuration Register for Channel 4 - High (CFG4_HI)—Offset 1A4h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.5.107 Source Gather Register for Channel 4 - Low (SGR4_LO)—Offset 1A8h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.5.108 Source Gather Register for Channel 4 - High (SGR4_HI)—Offset 1ACh

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.109 Destination Scatter Register for Channel 4 - Low (DSR4_LO)—Offset 1B0h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.5.110 Dest Scatter Register for Channel 4 - High (DSR4_HI)—Offset 1B4h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [BAR] + 1B4h
	BAR Type: PCI Configuration Register (Size: 32 bits) **BAR Reference:** [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.111 Source Address Register for Channel 5 - Low (SAR5_LO)—Offset 1B8h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [BAR] + 1B8h
	BAR Type: PCI Configuration Register (Size: 32 bits) **BAR Reference:** [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.5.112 Source Address Register for Channel 5 - High (SAR5_HI)—Offset 1BCh

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.113 Destination Address Register for Channel 5 - Low (DAR5_LO)—Offset 1C0h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.5.114 Destination Address Register for Channel 5 - High (DAR5_HI)—Offset 1C4h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.115 Linked List Pointer Register for Channel 5 - Low (LLP5_LO)—Offset 1C8h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC LMS

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.5.116 Linked List Pointer Register for Channel 5 - High (LLP5_HI)—Offset 1CCh

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.117 Control Register for Channel 5 - Low (CTL5_LO)—Offset 1D0h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Undefined_, LLP_SRC_EN, LLP_DST_EN, SMS, DMS, TT_FC, Undefined, DST_SCATTER_EN, SRC_GATHER_EN, SRC_MSIZE, DEST_MSIZE, SINC, DINC, SRC_TR_WIDTH, DST_TR_WIDTH, INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.5.118 Control Register for Channel 5 - High (CTL5_HI)—Offset 1D4h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Undefined_ | DONE | BLOCK_TS

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.5.119 Source Status Register for Channel 5 - Low (SSTAT5_LO)—Offset 1D8h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.5.120 Source Status Register for Channel 5 - High (SSTAT5_HI)—Offset 1DCh

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.121 Dest Status Register for Channel 5 - Low (DSTAT5_LO)—Offset 1E0h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.5.122 Dest Status Register for Channel 5 - High (DSTAT5_HI)—Offset 1E4h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.123 Source Status Address Register for Channel 5 - Low (SSTATAR5_LO)—Offset 1E8h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.124 Source Status Address Register for Channel 5 - High (SSTATAR5_HI)—Offset 1ECh

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.125 Dest Status Address Register for Channel 5 - Low (DSTATAR5_LO)—Offset 1F0h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.126 Dest Status Address Register for Channel 5 - High (DSTATAR5_HI)—Offset 1F4h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:0: Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.127 Configuration Register for Channel 5 - Low (CFG5_LO)—Offset 1F8h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EA0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	0	0	0	0

Bits	Field
31	RELOAD_DST
30	RELOAD_SRC
29:20	MAX_ABRST
19	SRC_HS_POL
18	DST_HS_POL
17	LOCK_B
16	LOCK_CH
15:14	LOCK_B_L
13:12	LOCK_CH_L
11	HS_SEL_SRC
10	HS_SEL_DST
9	FIFO_EMPTY
8	CH_SUSP
7:5	CH_PRIOR
4:0	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface, and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	5h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.5.128 Configuration Register for Channel 5 - High (CFG5_HI)—Offset 1FCh

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Fields: Undefined | DEST_PER | SRC_PER | SS_UPD_EN | DS_UPD_EN | PROTCTL | FIFO_MODE | FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the FIFO depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.5.129 Source Gather Register for Channel 5 - Low (SGR5_LO)—Offset 200h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.

Bit Range	Default & Access	Field Name (ID): Description
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.5.130 Source Gather Register for Channel 5 - High (SGR5_HI)—Offset 204h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 204h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.131 Destination Scatter Register for Channel 5 - Low (DSR5_LO)—Offset 208h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC (bits 31:20), DSI (bits 19:0)

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.5.132 Dest Scatter Register for Channel 5 - High (DSR5_HI)—Offset 20Ch

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.133 Source Address Register for Channel 6 - Low (SAR6_LO)—Offset 210h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.5.134 Source Address Register for Channel 6 - High (SAR6_HI)—Offset 214h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 214h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.135 Destination Address Register for Channel 6 - Low (DAR6_LO)—Offset 218h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.5.136 Destination Address Register for Channel 6 - High (DAR6_HI)—Offset 21Ch

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 21Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.137 Linked List Pointer Register for Channel 6 - Low (LLP6_LO)—Offset 220h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOC																														LMS	

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.5.138 Linked List Pointer Register for Channel 6 - High (LLP6_HI)—Offset 224h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 224h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.139 Control Register for Channel 6 - Low (CTL6_LO)—Offset 228h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Fields: Undefined_ (31:29), LLP_SRC_EN (28), LLP_DST_EN (27), SMS (26:25), DMS (24:23), TT_FC (22:20), Undefined (19), DST_SCATTER_EN (18), SRC_GATHER_EN (17), SRC_MSIZE (16:14), DEST_MSIZE (13:11), SINC (10:9), DINC (8:7), SRC_TR_WIDTH (6:4), DST_TR_WIDTH (3:1), INT_EN (0)

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.5.140 Control Register for Channel 6 - High (CTL6_HI)—Offset 22Ch

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Undefined_ | DONE | BLOCK_TS

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.5.141 Source Status Register for Channel 6 - Low (SSTAT6_LO)—Offset 230h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 230h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SSTAT																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.5.142 Source Status Register for Channel 6 - High (SSTAT6_HI)—Offset 234h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 234h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.143 Dest Status Register for Channel 6 - Low (DSTAT6_LO)—Offset 238h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 238h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.5.144 Dest Status Register for Channel 6 - High (DSTAT6_HI)—Offset 23Ch

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 23Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.145 Source Status Address Register for Channel 6 - Low (SSTATAR6_LO)—Offset 240h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 240h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.146 Source Status Address Register for Channel 6 - High (SSTATAR6_HI)—Offset 244h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 244h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.147 Dest Status Address Register for Channel 6 - Low (DSTATAR6_LO)—Offset 248h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 248h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.148 Dest Status Address Register for Channel 6 - High (DSTATAR6_HI)—Offset 24Ch

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.149 Configuration Register for Channel 6 - Low (CFG6_LO)—Offset 250h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EC0h

Bits	Default	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:20	0 0 0 0 0 0 0 0 0 0	MAX_ABRST
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	LOCK_B
16	0	LOCK_CH
15:14	0 0	LOCK_B_L
13:12	0 0	LOCK_CH_L
11	1	HS_SEL_SRC
10	1	HS_SEL_DST
9	1	FIFO_EMPTY
8	0	CH_SUSP
7:5	1 1 0	CH_PRIOR
4:0	0 0 0 0 0	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	6h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.5.150 Configuration Register for Channel 6 - High (CFG6_HI)—Offset 254h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	

Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.5.151 Source Gather Register for Channel 6 - Low (SGR6_LO)—Offset 258h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SGC												SGI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.5.152 Source Gather Register for Channel 6 - High (SGR6_HI)—Offset 25Ch

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 25Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.153 Destination Scatter Register for Channel 6 - Low (DSR6_LO)—Offset 260h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSC | DSI

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.5.154 Dest Scatter Register for Channel 6 - High (DSR6_HI)—Offset 264h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 264h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.155 Source Address Register for Channel 7 - Low (SAR7_LO)—Offset 268h

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Source Address of DMA Transfer (SAR):** Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

24.5.156 Source Address Register for Channel 7 - High (SAR7_HI)—Offset 26Ch

Refer to the description for register Source Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 26Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.157 Destination Address Register for Channel 7 - Low (DAR7_LO)—Offset 270h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Current Destination Address of DMA Transfer (DAR):** Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

24.5.158 Destination Address Register for Channel 7 - High (DAR7_HI)—Offset 274h

Refer to the description for register Destination Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 274h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.159 Linked List Pointer Register for Channel 7 - Low (LLP7_LO)—Offset 278h

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LOC (bits 31:2), LMS (bits 1:0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0h RW	**List Master Select (LMS):** Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

24.5.160 Linked List Pointer Register for Channel 7 - High (LLP7_HI)—Offset 27Ch

Refer to the description for register Linked List Pointer Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 27Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.161 Control Register for Channel 7 - Low (CTL7_LO)—Offset 280h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Fields (bit 31 to bit 0): Undefined_, LLP_SRC_EN, LLP_DST_EN, SMS, DMS, TT_FC, Undefined, DST_SCATTER_EN, SRC_GATHER_EN, SRC_MSIZE, DEST_MSIZE, SINC, DINC, SRC_TR_WIDTH, DST_TR_WIDTH, INT_EN

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Undefined_:** RESERVED
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0h RW	**Source Master Select (SMS):** Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0h RW	**Destination Master Select (DMS):** Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	3h RW	**Transfer Type and Flow Control (TT_FC):** Refer to description for CTL0_LO.TT_FC.
19	0h RW	**Undefined:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Destination Scatter Enable Bit (DST_SCATTER_EN):** • 0 = disabled • 1 = enabled
17	0h RW	**Source Gather Enable Bit (SRC_GATHER_EN):** • 0 = disabled • 1 = enabled
16:14	1h RW	**Source Burst Transaction Length (SRC_MSIZE):** Refer to the description of CTL0_LO.SRC_MSIZE.
13:11	1h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Refer to the description for CTL0_LO.DEST_MSIZE.
10:9	0h RW	**Source Address Increment (SINC):** • 00 = Increment • 01 = Decrement • 1x = No change
8:7	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. • 00 = Increment • 01 = Decrement • 1x = No change
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	1h RW	**Interrupt Enable Bit (INT_EN):** If set, then all interrupt-generating sources are enabled.

24.5.162 Control Register for Channel 7 - High (CTL7_HI)—Offset 284h

Refer to the register description for Control Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h

Bits	31:13	12	11:0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0 0 0 0 1 0
Field	Undefined_	DONE	BLOCK_TS

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**Undefined_:** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Done Bit (DONE):** Refer to the description of CTL0_HI.DONE.
11:0	2h RW	**Block Transfer Size (BLOCK_TS):** When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

24.5.163 Source Status Register for Channel 7 - Low (SSTAT7_LO)—Offset 288h

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 288h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hw from the addrx pointed to by SSTATAR0 register

24.5.164 Source Status Register for Channel 7 - High (SSTAT7_HI)—Offset 28Ch

Refer to the register description for Source Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.165 Dest Status Register for Channel 7 - Low (DSTAT7_LO)—Offset 290h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 290h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTAT

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Dest status information retrieved by hw from the addrx pointed to by DSTATAR0 register

24.5.166 Dest Status Register for Channel 7 - High (DSTAT7_HI)—Offset 294h

Refer to the register description for Dest Status Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 294h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.167 Source Status Address Register for Channel 7 - Low (SSTATAR7_LO)—Offset 298h

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 298h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR:** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.168 Source Status Address Register for Channel 7 - High (SSTATAR7_HI)—Offset 29Ch

Refer to the description for register Source Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 29Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.169 Dest Status Address Register for Channel 7 - Low (DSTATAR7_LO)—Offset 2A0h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSTATAR

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR (SSTATAR):** Pointer from where the hw can fetch the source status information registered in SSTAT0.

24.5.170 Dest Status Address Register for Channel 7 - High (DSTATAR7_HI)—Offset 2A4h

Refer to the description for register Dest Status Address Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** RESERVED

24.5.171 Configuration Register for Channel 7 - Low (CFG7_LO)—Offset 2A8h

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EE0h

Bits	Default	Field
31	0	RELOAD_DST
30	0	RELOAD_SRC
29:20	0 0 0 0 0 0 0 0 0 0	MAX_ABRST
19	0	SRC_HS_POL
18	0	DST_HS_POL
17	0	LOCK_B
16	0	LOCK_CH
15:14	0 0	LOCK_B_L
13:12	0 0	LOCK_CH_L
11	1	HS_SEL_SRC
10	1	HS_SEL_DST
9	1	FIFO_EMPTY
8	0	CH_SUSP
7:5	1 1 1	CH_PRIOR
4:0	0 0 0 0 0	Undefined

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Automatic Destination Reload (RELOAD_DST):** The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0h RW	**Automatic Source Reload (RELOAD_SRC):** The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0h RW	**Maximum AMBA Burst Length (MAX_ABRST):** Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0h RW	**Source Handshaking Interface Polarity (SRC_HS_POL):** • 0 = Active high • 1 = Active low
18	0h RW	**Destination Handshaking Interface Polarity (DST_HS_POL):** • 0 = Active high • 1 = Active low
17	0h RW	**Bus Lock Bit (LOCK_B):** When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0h RW	**Channel Lock Bit (LOCK_CH):** When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0h RW	**Bus Lock Level (LOCK_B_L):** Indicates the duration over which CFGx.LOCK_B bit applies. • 00 = Over complete DMA transfer • 01 = Over complete DMA block transfer • 1x = Over complete DMA transaction
13:12	0h RW	**Channel Lock Level (LOCK_CH_L):** Indicates the duration over which CFGx.LOCK_CH bit applies. • 00 = DMA transfer • 01 = DMA block transfer • 1x = DMA transaction

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**Source Software or Hardware Handshaking Select (HS_SEL_SRC):** • 0 = HW handshaking • 1 = SW handshaking
10	1h RW	**Destination Software or Hardware Handshaking Select (HS_SEL_DST):** • 0 = HW handshaking • 1 = SW handshaking
9	1h RO	**FIFO_EMPTY:** Indicates whether there is data left in the channel FIFO.
8	0h RW	**Channel Suspend (CH_SUSP):** Suspends all DMA transfers from source until this bit is cleared.
7:5	7h RW	**Channel Priority (CH_PRIOR):** Priority of 7 is the highest priority.
4:0	0h RW	**Undefined:** RESERVED

24.5.172 Configuration Register for Channel 7 - High (CFG7_HI)—Offset 2ACh

Refer to the register description for Configuration Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Undefined	DEST_PER	SRC_PER	SS_UPD_EN	DS_UPD_EN	PROTCTL	FIFO_MODE	FCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Undefined:** Reserved.
14:11	0h RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0h RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0h RW	**Source Status Update Enable (SS_UPD_EN):** Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Destination Status Update Enable (DS_UPD_EN):** Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	1h RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0h RW	**FIFO Mode Select (FIFO_MODE):** Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. • 0 = Space/data available for single AHB transfer of the specified transfer width. • 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0h RW	**Flow Control Mode (FCMODE):** Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. • 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. • 1 = Source transaction requests are not serviced until a destination transaction request occurs.

24.5.173 Source Gather Register for Channel 7 - Low (SGR7_LO)—Offset 2B0h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
SGC			SGI				

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Source Gather Count (SGC):** Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**Source Gather Interval (SGI):** Refer to the description for SGR0_LO.SGI.

24.5.174 Source Gather Register for Channel 7 - High (SGR7_HI)—Offset 2B4h

Refer to the register description for Source Gather Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.175 Destination Scatter Register for Channel 7 - Low (DSR7_LO)—Offset 2B8h

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DSC												DSI																			

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Dest Scatter Count (DSC):** Destination contiguous transfer count between successive scatter boundaries.
19:0	0h RW	**Dest Scatter Interval (DSI):** Refer to the description for DSR0_LO.DSI.

24.5.176 Dest Scatter Register for Channel 7 - High (DSR7_HI)—Offset 2BCh

Refer to the register description for Destination Scatter Register for Channel 0 - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.177 Interrupt Raw Status Registers - Low (RawTfr_LO)—Offset 2C0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel; for example, RawTfr[2] is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:8) | RAW (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.5.178 Interrupt Raw Status Registers - High (RawTfr_HI)—Offset 2C4h

Refer to the description for Interrupt Raw Status Registers - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.179 Interrupt Raw Status Registers - Low (RawBlock_LO)—Offset 2C8h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | RAW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.5.180 Interrupt Raw Status Registers - High (RawBlock_HI)—Offset 2CCh

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.181 Interrupt Raw Status Registers - Low (RawSrcTran_LO)—Offset 2D0h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Undefined (31:8), RAW (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.5.182 Interrupt Raw Status Registers - High (RawSrcTran_HI)—Offset 2D4h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.183 Interrupt Raw Status Registers - Low (RawDstTran_LO)—Offset 2D8h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

RAW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.5.184 Interrupt Raw Status Registers - High (RawDstTran_HI)—Offset 2DCh

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.185 Interrupt Raw Status Registers - Low (RawErr_LO)—Offset 2E0h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | RAW

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RW	**Raw Interrupt Status (RAW):** Reserved.

24.5.186 Interrupt Raw Status Registers - High (RawErr_HI)—Offset 2E4h

Refer to the description of the register with short name RawTfr_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:0: Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.187 Interrupt Status Registers - Low (StatusTfr_LO)—Offset 2E8h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:8: Undefined; Bits 7:0: STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.5.188 Interrupt Status Registers - High (StatusTfr_HI)—Offset 2ECh

All interrupt events from all channels are stored in these Interrupt Status registers after masking: StatusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel; for example, StatusTfr[2] is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DW_ahb_dmac.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.189 Interrupt Status Registers - Low (StatusBlock_LO)—Offset 2F0h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined | STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.5.190 Interrupt Status Registers - High (StatusBlock_HI)—Offset 2F4h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.191 Interrupt Status Registers - Low (StatusSrcTran_LO)—Offset 2F8h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.5.192 Interrupt Status Registers - High (StatusSrcTran_HI)—Offset 2FCh

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.193 Interrupt Status Registers - Low (StatusDstTran_LO)—Offset 300h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:8), STATUS (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.5.194 Interrupt Status Registers - High (StatusDstTran_HI)—Offset 304h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 304h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.195 Interrupt Status Registers - Low (StatusErr_LO)—Offset 308h

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | STATUS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h RO	**Interrupt Status (STATUS):** Reserved.

24.5.196 Interrupt Status Registers - High (StatusErr_HI)—Offset 30Ch

Refer to the description for register StatusTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.197 Interrupt Mask Registers - Low (MaskTfr_LO)—Offset 310h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | INT_MASK_WE | INT_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h RW	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

24.5.198 Interrupt Mask Registers - High (MaskTfr_HI)—Offset 314h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 314h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.199 Interrupt Mask Registers - Low (MaskBlock_LO)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel; for example, MaskTfr[2] is the mask bit for the Channel 2 transfer complete interrupt.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:16), INT_MASK_WE (bits 15:8), INT_MASK (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**INT_MASK:** Interrupt Mask • 0 = masked • 1 = unmasked

24.5.200 Interrupt Mask Registers - High (MaskBlock_HI)—Offset 31Ch

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 31Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Undefined							

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.201 Interrupt Mask Registers - Low (MaskSrcTran_LO)—Offset 320h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Undefined				INT_MASK_WE		INT_MASK	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

24.5.202 Interrupt Mask Registers - High (MaskSrcTran_HI)—Offset 324h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 324h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.203 Interrupt Mask Registers - Low (MaskDstTran_LO)—Offset 328h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined | INT_MASK_WE | INT_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

24.5.204 Interrupt Mask Registers - High (MaskDstTran_HI)—Offset 32Ch

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 32Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.205 Interrupt Mask Registers - Low (MaskErr_LO)—Offset 330h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:16	Bits 15:8	Bits 7:0
Undefined	INT_MASK_WE	INT_MASK

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Interrupt Mask (INT_MASK):** • 0 = masked • 1 = unmasked

24.5.206 Interrupt Mask Registers - High (MaskErr_HI)—Offset 334h

Refer to the description for register MaskBlock_LO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 334h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:0
Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.207 Interrupt Clear Registers - Low (ClearTfr_LO)—Offset 338h

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel; for example, ClearTfr[2] is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																								CLEAR							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.5.208 Interrupt Clear Registers - High (ClearTfr_HI)—Offset 33Ch

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 33Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.209 Interrupt Clear Registers - Low (ClearBlock_LO)—Offset 340h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																								CLEAR							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.5.210 Interrupt Clear Registers (ClearBlock_HI)—Offset 344h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 344h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.211 Interrupt Clear Registers - Low (ClearSrcTran_LO)—Offset 348h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:8); CLEAR (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.5.212 Interrupt Clear RegistersClearSrc - High (ClearSrcTran_HI)—Offset 34Ch

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 34Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.213 Interrupt Clear Registers - Low (ClearDstTran_LO)—Offset 350h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:8), CLEAR (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.5.214 Interrupt Clear Registers - High (ClearDstTran_HI)—Offset 354h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 354h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.215 Interrupt Clear Registers - Low (ClearErr_LO)—Offset 358h

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																								CLEAR							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Undefined:** Reserved.
7:0	0h WO	**Clear Interrupt Status (CLEAR):** Interrupt clear. • 0 = no effect • 1 = clear interrupt

24.5.216 Interrupt Clear Registers - High (ClearErr_HI)—Offset 35Ch

Refer to the description for register ClearTfr_HI.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 35Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Undefined																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.217 Combined Interrupt Status Register - Low (StatusInt_LO)—Offset 360h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Undefined	ERR	DSTT	SRCT	BLOCK	TFR

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RW	**Undefined:** Reserved.
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register.
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

24.5.218 Combined Interrupt Status Register - High (StatusInt_HI)—Offset 364h

Refer to the description for register StatusInt_LO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 364h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Undefined							

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.219 Source Software Transaction Request Register - Low (ReqSrcReg_LO)—Offset 368h

A bit is assigned for each channel in this register. ReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 368h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Undefined				SRC_REQ_WE		SRC_REQ	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Source Req Write Enable (SRC_REQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Source Request (SRC_REQ):** A channel SRC_REQ bit is written only if the corresponding channel write enable bit in the SRC_REQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

24.5.220 Source Software Transaction Request Register - High (ReqSrcReg_HI)—Offset 36Ch

A bit is assigned for each channel in this register. ReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 36Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Undefined (31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.221 Destination Software Transaction Request Register - Low (ReqDstReg_LO)—Offset 370h

A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 370h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Undefined (31:16), DST_REQ_WE (15:8), DST_REQ (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h WO	**Destination Request Write Enable (DST_REQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Request (DST_REQ):** A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

24.5.222 Destination Software Transaction Request Register - High (ReqDstReg_HI)—Offset 374h

A bit is assigned for each channel in this register. ReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 374h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.223 Single Source Software Transaction Request Register - Low (SglRqSrcReg_LO)—Offset 378h

A bit is assigned for each channel in this register. SglReqSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 378h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Undefined				SRC_SGLREQ_WE		SRC_SGLREQ	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Source Req Write Enable (SRC_SGLREQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Source Single Request (SRC_SGLREQ):** A channel SRC_SGLREQ bit is written only if the corresponding channel write enable bit in the SRC_SGLREQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

24.5.224 Single Source Software Transaction Request Register - High (SglRqSrcReg_HI)—Offset 37Ch

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 37Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Undefined							

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.225 Single Destination Software Transaction Request Register - Low (SglRqDstReg_LO)—Offset 380h

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 380h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
Undefined				DST_SGLREQ_WE		DST_SGLREQ		

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Destination Request Write Enable (DST_SGLREQ_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Single or Burst Request (DST_SGLREQ):** A channel DST_SGLREQ bit is written only if the corresponding channel write enable bit in the DST_SGLREQ_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

24.5.226 Single Destination Software Transaction Request Register - High (SglRqDstReg_HI)—Offset 384h

A bit is assigned for each channel in this register. SglReqDstReg[n] is ignored when software handshaking is not enabled for the source of channel n.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 384h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
Undefined								

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.227 Last Source Transaction Request Register - Low (LstSrcReg_LO)—Offset 388h

A bit is assigned for each channel in this register. LstSrcReg[n] is ignored when software handshaking is not enabled for the source of channel n, or when the source of channel n is not a flow controller. A channel LSTSRC bit is written only if the corresponding channel write enable bit in the LSTSRC_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

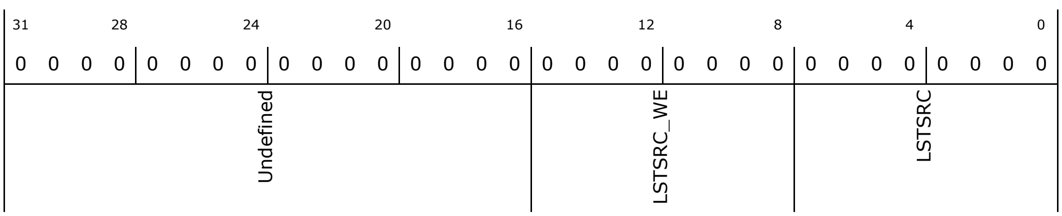
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 388h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Last Source Transaction Request Write Enable (LSTSRC_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Last Source Transaction Request (LSTSRC):** • 0 = Not last transaction in current block • 1 = Last transaction in current block

24.5.228 Last Source Transaction Request Register - High (LstSrcReg_HI)—Offset 38Ch

Refer to description for Last Source Transaction Request Register - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.229 Last Destination Transaction Request Register - Low (LstDstReg_LO)—Offset 390h

A bit is assigned for each channel in this register. LstDstReg[n] is ignored when software handshaking is not enabled for the destination of channel n or when the destination of channel n is not a flow controller. A channel LSTDST bit is written only if the corresponding channel write enable bit in the LSTDST_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 390h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | LSTDST_WE | LSTDST

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Last Destination Transaction Request Write Enable (LSTDST_WE):** • 0 = write disabled • 1 = write enabled
7:0	0h RW	**Destination Last Transaction Request (LSTDST):** • 0 = Not last transaction in current block • 1 = Last transaction in current block

24.5.230 Last Destination Transaction Request Register - High (LstDstReg_HI)—Offset 394h

Refer to description for Last Destination Transaction Request Register - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 394h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.231 DW_ahb_dmac Configuration Register - Low (DmaCfgReg_LO)—Offset 398h

This register is used to enable the DW_ahb_dmac, which must be done before any channel activity can begin.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined | DMA_EN

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RW	**Undefined:** Reserved.
0	0h RW	**DW_ahb_dmac Enable Bit (DMA_EN):** • 0 = DW_ahb_dmac Disabled • 1 = DW_ahb_dmac Enabled

24.5.232 DW_ahb_dmac Configuration Register - High (DmaCfgReg_HI)—Offset 39Ch

Refer to description for DW_ahb_dmac Configuration Register - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 39Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:0: Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.233 DW_ahb_dmac Channel Enable Register - Low (ChEnReg_LO)—Offset 3A0h

This is the DW_ahb_dmac Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive; it can then enable an inactive channel with the required priority.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:16: Undefined; Bits 15:8: CH_EN_WE; Bits 7:0: CH_EN

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Undefined:** Reserved.
15:8	0h WO	**Channel Enable Write Enable (CH_EN_WE):** The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE (this bit), is asserted on the same AHB write transfer.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel; clearing this bit disables the channel. • 0 = Disable the Channel • 1 = Enable the Channel

24.5.234 DW_ahb_dmac Channel Enable Register - High (ChEnReg_HI)—Offset 3A4h

Refer to the description for DW_ahb_dmac Channel Enable Register - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.235 DW_ahb_dmac ID Register - Low (DmaIdReg_LO)—Offset 3A8h

This is a read-only register that reads back the coreConsultant-configured hardcoded ID number, DMAH_ID_NUM.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: C0CAC01Ah

31			28				24				20				16				12				8				4				0
1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	1	0

DMA_ID

Bit Range	Default & Access	Field Name (ID): Description
31:0	c0cac01ah RO	**Hardcoded DW_ahb_dmac Peripheral ID (DMA_ID):** coreConsultantconfigured hardcoded ID number DMAH_ID_NUM.

24.5.236 DW_ahb_dmac ID Register - High (DmaIdReg_HI)—Offset 3ACh

Refer to the description of DW_ahb_dmac ID Register - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.237 DW_ahb_dmac Test Register - Low (DmaTestReg_LO)—Offset 3B0h

This register is used to put the AHB slave interface into test mode, during which the readback value of the writable registers match the value written, assuming the DW_ahb_dmac configuration has not optimized the same registers. In normal operation, the readback value of some registers is a function of the DW_ahb_dmac state, and does not match the value written.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined (bits 31:1); TEST_SLV_IF (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RW	**Undefined:** Reserved.
0	0h RW	**TEST_SLV_IF:** Puts the AHB slave interface into test mode. In this mode, the readback value of the writable registers always matches the value written. This bit does not allow writing to read-only registers. • 0 = Normal mode • 1 = Test mode

24.5.238 DW_ahb_dmac Test Register - High (DmaTestReg_HI)—Offset 3B4h

Refer to the description of DW_ahb_dmac Test Register - Low.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.239 DW_ahb_dmac Component Parameters Register 6 - Low (DMA_COMP_PARAMS_6_LO)—Offset 3C8h

Refer to the description for DW_ahb_dmac Component Parameters Register 6 - High.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undefined

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Undefined:** Reserved.

24.5.240 DW_ahb_dmac Component Parameters Register 6 - High (DMA_COMP_PARAMS_6_HI)—Offset 3CCh

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 7. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Field
31	Undefined
30:28	CH7_FIFO_DEPTH
27:25	CH7_SMS
24:22	CH7_LMS
21:19	CH7_DMS
18:16	CH7_MAX_MULT_SIZE
15:14	CH7_FC
13	CH7_HC_LLP
12	CH7_CTL_WB_EN
11	CH7_MULTI_BLK_EN
10	CH7_LOCK_EN
9	CH7_SRC_GAT_EN
8	CH7_DST_SCA_EN
7	CH7_STAT_SRC
6	CH7_STAT_DST
5:3	CH7_STW
2:0	CH7_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH7_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH7_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH7_SMS:** The value of this register is derived from the DMAH_CH7_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH7_LMS:** The value of this register is derived from the DMAH_CH7_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
21:19	4h RO	**CH7_DMS:** The value of this register is derived from the DMAH_CH7_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH7_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH7_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH7_FC:** The value of this register is derived from the DMAH_CH7_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH7_HC_LLP:** The value of this register is derived from the DMAH_CH7_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH7_CTL_WB_EN:** The value of this register is derived from the DMAH_CH7_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH7_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH7_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH7_LOCK_EN:** The value of this register is derived from the DMAH_CH7_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH7_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH7_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH7_DST_SCA_EN:** The value of this register is derived from the DMAH_CH7_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH7_STAT_SRC:** The value of this register is derived from the DMAH_CH7_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**CH7_STAT_DST:** The value of this register is derived from the DMAH_CH7_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH7_STW:** The value of this register is derived from the DMAH_CH7_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH7_DTW:** The value of this register is derived from the DMAH_CH7_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.5.241 DW_ahb_dmac Component Parameters Register 5 - Low (DMA_COMP_PARAMS_5_LO)—Offset 3D0h

Refer to the description for DW_ahb_dmac Component Parameters Register 5 - High.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h

Bits	Value	Field
31	0	Undefined
30:28	011	CH6_FIFO_DEPTH
27:25	100	CH6_SMS
24:22	000	CH6_LMS
21:19	100	CH6_DMS
18:16	010	CH6_MAX_MULT_SIZE
15:14	00	CH6_FC
13	0	CH6_HC_LLP
12	0	CH6_CTL_WB_EN
11	0	CH6_MULTI_BLK_EN
10	0	CH6_LOCK_EN
9	1	CH6_SRC_GAT_EN
8	1	CH6_DST_SCA_EN
7	0	CH6_STAT_SRC
6	0	CH6_STAT_DST
5:3	000	CH6_STW
2:0	000	CH6_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
30:28	3h RO	**CH6_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH6_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH6_SMS:** The value of this register is derived from the DMAH_CH6_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH6_LMS:** The value of this register is derived from the DMAH_CH6_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH6_DMS:** The value of this register is derived from the DMAH_CH6_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH6_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH6_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH6_FC:** The value of this register is derived from the DMAH_CH6_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH6_HC_LLP:** The value of this register is derived from the DMAH_CH6_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH6_CTL_WB_EN:** The value of this register is derived from the DMAH_CH6_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**CH6_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH6_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH6_LOCK_EN:** The value of this register is derived from the DMAH_CH6_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH6_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH6_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH6_DST_SCA_EN:** The value of this register is derived from the DMAH_CH6_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH6_STAT_SRC:** The value of this register is derived from the DMAH_CH6_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH6_STAT_DST:** The value of this register is derived from the DMAH_CH6_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH6_STW:** The value of this register is derived from the DMAH_CH6_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH6_DTW:** The value of this register is derived from the DMAH_CH6_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.5.242 DW_ahb_dmac Component Parameters Register 5 - High (DMA_COMP_PARAMS_5_HI)—Offset 3D4h

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 5 and Channel 6. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h

31			28				24				20				16				12				8				4				0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
Undefined	CH5_FIFO_DEPTH			CH5_SMS			CH5_LMS			CH5_DMS			CH5_MAX_MULT_SIZE			CH5_FC		CH5_HC_LLP	CH5_CTL_WB_EN	CH5_MULTI_BLK_EN	CH5_LOCK_EN	CH5_SRC_GAT_EN	CH5_DST_SCA_EN	CH5_STAT_SRC	CH5_STAT_DST	CH5_STW			CH5_DTW		

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH5_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH5_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH5_SMS:** The value of this register is derived from the DMAH_CH5_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH5_LMS:** The value of this register is derived from the DMAH_CH5_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
21:19	4h RO	**CH5_DMS:** The value of this register is derived from the DMAH_CH5_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH5_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH5_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH5_FC:** The value of this register is derived from the DMAH_CH5_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH5_HC_LLP:** The value of this register is derived from the DMAH_CH5_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH5_CTL_WB_EN:** The value of this register is derived from the DMAH_CH5_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH5_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH5_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH5_LOCK_EN:** The value of this register is derived from the DMAH_CH5_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH5_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH5_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH5_DST_SCA_EN:** The value of this register is derived from the DMAH_CH5_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH5_STAT_SRC:** The value of this register is derived from the DMAH_CH5_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**CH5_STAT_DST:** The value of this register is derived from the DMAH_CH5_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH5_STW:** The value of this register is derived from the DMAH_CH5_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH5_DTW:** The value of this register is derived from the DMAH_CH5_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.5.243 DW_ahb_dmac Component Parameters Register 4 - Low (DMA_COMP_PARAMS_4_LO)—Offset 3D8h

Refer to the description for DW_ahb_dmac Component Parameters Register 4 - High.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h

31			28				24				20				16				12				8				4				0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Fields (bit 31 to bit 0): Undefined, CH4_FIFO_DEPTH, CH4_SMS, CH4_LMS, CH4_DMS, CH4_MAX_MULT_SIZE, CH4_FC, CH4_HC_LLP, CH4_CTL_WB_EN, CH4_MULTI_BLK_EN, CH4_LOCK_EN, CH4_SRC_GAT_EN, CH4_DST_SCA_EN, CH4_STAT_SRC, CH4_STAT_DST, CH4_STW, CH4_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
30:28	3h RO	**CH4_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH4_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH4_SMS:** The value of this register is derived from the DMAH_CH4_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH4_LMS:** The value of this register is derived from the DMAH_CH4_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH4_DMS:** The value of this register is derived from the DMAH_CH4_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH4_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH4_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH4_FC:** The value of this register is derived from the DMAH_CH4_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH4_HC_LLP:** The value of this register is derived from the DMAH_CH4_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH4_CTL_WB_EN:** The value of this register is derived from the DMAH_CH4_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**CH4_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH4_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH4_LOCK_EN:** The value of this register is derived from the DMAH_CH4_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH4_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH4_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH4_DST_SCA_EN:** The value of this register is derived from the DMAH_CH4_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH4_STAT_SRC:** The value of this register is derived from the DMAH_CH4_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH4_STAT_DST:** The value of this register is derived from the DMAH_CH4_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH4_STW:** The value of this register is derived from the DMAH_CH4_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH4_DTW:** The value of this register is derived from the DMAH_CH4_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.5.244 DW_ahb_dmac Component Parameters Register 4 - High (DMA_COMP_PARAMS_4_HI)—Offset 3DCh

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 3 and Channel 4. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
Undefined	CH3_FIFO_DEPTH			CH3_SMS			CH3_LMS			CH3_DMS			CH3_MAX_MULT_SIZE			CH3_FC		CH3_HC_LLP	CH3_CTL_WB_EN	CH3_MULTI_BLK_EN	CH3_LOCK_EN	CH3_SRC_GAT_EN	CH3_DST_SCA_EN	CH3_STAT_SRC	CH3_STAT_DST	CH3_STW			CH3_DTW		

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH3_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH3_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH3_SMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH3_LMS:** The value of this register is derived from the DMAH_CH3_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
21:19	4h RO	**CH3_DMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH3_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH3_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH3_FC:** The value of this register is derived from the DMAH_CH3_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH3_HC_LLP:** The value of this register is derived from the DMAH_CH3_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH3_CTL_WB_EN:** The value of this register is derived from the DMAH_CH3_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH3_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH3_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH3_LOCK_EN:** The value of this register is derived from the DMAH_CH3_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH3_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH3_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH3_DST_SCA_EN:** The value of this register is derived from the DMAH_CH3_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH3_STAT_SRC:** he value of this register is derived from the DMAH_CH3_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**CH3_STAT_DST:** The value of this register is derived from the DMAH_CH3_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH3_STW:** The value of this register is derived from the DMAH_CH3_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH3_DTW:** The value of this register is derived from the DMAH_CH3_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.5.245 DW_ahb_dmac Component Parameters Register 3 - Low (DMA_COMP_PARAMS_3_LO)—Offset 3E0h

Refer to the description for DW_ahb_dmac Component Parameters Register 3 - High.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h

Bits	Value	Field
31	0	Undefined
30:28	0 1 1	CH2_FIFO_DEPTH
27:25	1 1 0	CH2_SMS
24:22	0 0 0	CH2_LMS
21:19	0 1 0	CH2_DMS
18:16	0 1 0	CH2_MAX_MULT_SIZE
15:14	0 0	CH2_FC
13	0	CH2_HC_LLP
12	0	CH2_CTL_WB_EN
11	0	CH2_MULTI_BLK_EN
10	0	CH2_LOCK_EN
9	1	CH2_SRC_GAT_EN
8	1	CH2_DST_SCA_EN
7	0	CH2_STAT_SRC
6	0	CH2_STAT_DST
5:3	0 0 0	CH2_STW
2:0	0 0 0	CH2_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
30:28	3h RO	**CH2_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH2_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH2_SMS:** The value of this register is derived from the DMAH_CH2_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH2_LMS:** The value of this register is derived from the DMAH_CH2_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH2_DMS:** The value of this register is derived from the DMAH_CH2_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH2_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH2_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH2_FC:** The value of this register is derived from the DMAH_CH2_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH2_HC_LLP:** The value of this register is derived from the DMAH_CH2_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH2_CTL_WB_EN:** The value of this register is derived from the DMAH_CH2_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**CH2_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH2_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to the spec. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH2_LOCK_EN:** The value of this register is derived from the DMAH_CH2_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH2_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH2_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH2_DST_SCA_EN:** The value of this register is derived from the DMAH_CH2_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH2_STAT_SRC:** The value of this register is derived from the DMAH_CH2_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH2_STAT_DST:** The value of this register is derived from the DMAH_CH2_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH2_STW:** The value of this register is derived from the DMAH_CH2_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH2_DTW:** The value of this register is derived from the DMAH_CH2_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.5.246 DW_ahb_dmac Component Parameters Register 3 - High (DMA_COMP_PARAMS_3_HI)—Offset 3E4h

This is a constant read-only register that contains encoded information about the component parameter settings for Channel 1 and Channel 2. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
Undefined	CH1_FIFO_DEPTH			CH1_SMS			CH1_LMS			CH1_DMS			CH1_MAX_MULT_SIZE			CH1_FC		CH1_HC_LLP	CH1_CTL_WB_EN	CH1_MULTI_BLK_EN	CH1_LOCK_EN	CH1_SRC_GAT_EN	CH1_DST_SCA_EN	CH1_STAT_SRC	CH1_STAT_DST	CH1_STW			CH1_DTW		

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.
30:28	3h RO	**CH1_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH1_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH1_SMS:** The value of this register is derived from the DMAH_CH1_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH1_LMS:** The value of this register is derived from the DMAH_CH1_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
21:19	4h RO	**CH1_DMS:** The value of this register is derived from the DMAH_CH1_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH1_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH1_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH1_FC:** The value of this register is derived from the DMAH_CH1_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH1_HC_LLP:** The value of this register is derived from the DMAH_CH1_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH1_CTL_WB_EN:** The value of this register is derived from the DMAH_CH1_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
11	0h RO	**CH1_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH1_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH1_LOCK_EN:** The value of this register is derived from the DMAH_CH1_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH1_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH1_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH1_DST_SCA_EN:** The value of this register is derived from the DMAH_CH1_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH1_STAT_SRC:** The value of this register is derived from the DMAH_CH1_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**CH1_STAT_DST:** The value of this register is derived from the DMAH_CH1_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH1_STW:** The value of this register is derived from the DMAH_CH1_STW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
2:0	0h RO	**CH1_DTW:** The value of this register is derived from the DMAH_CH1_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.5.247 DW_ahb_dmac Component Parameters Register 2 - Low (DMA_COMP_PARAMS_2_LO)—Offset 3E8h

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h

Bits	Value	Field
31	0	Undefined
30:28	0 1 1	CH0_FIFO_DEPTH
27:25	1 0 0	CH0_SMS
24:22	0 0 0	CH0_LMS
21:19	1 0 0	CH0_DMS
18:16	0 1 0	CH0_MAX_MULT_SIZE
15:14	0 0	CH0_FC
13	0	CH0_HC_LLP
12	0	CH0_CTL_WB_EN
11	0	CH0_MULTI_BLK_EN
10	0	CH0_LOCK_EN
9	1	CH0_SRC_GAT_EN
8	1	CH0_DST_SCA_EN
7	0	CH0_STAT_SRC
6	0	CH0_STAT_DST
5:3	0 0 0	CH0_STW
2:0	0 0 0	CH0_DTW

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Undefined:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
30:28	3h RO	**CH0_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH0_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 8 • 1h = 16 • 2h = 32 • 3h = 64 • 4h = 128
27:25	4h RO	**CH0_SMS:** The value of this register is derived from the DMAH_CH0_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
24:22	0h RO	**CH0_LMS:** The value of this register is derived from the DMAH_CH0_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
21:19	4h RO	**CH0_DMS:** The value of this register is derived from the DMAH_CH0_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = MASTER_1 • 1h = MASTER_2 • 2h = MASTER_3 • 3h = MASTER_4 • 4h = NO_HARDCODE
18:16	2h RO	**CH0_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH0_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. • 0h = 4 • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved
15:14	0h RO	**CH0_FC:** The value of this register is derived from the DMAH_CH0_FC coreConsultant parameter. For a description of this parameter, refer to page 107. • 0h = DMA • 1h = SRC • 2h = DST • 3h = ANY
13	0h RO	**CH0_HC_LLP:** The value of this register is derived from the DMAH_CH0_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. • 0 = FALSE • 1 = TRUE
12	0h RO	**CH0_CTL_WB_EN:** The value of this register is derived from the DMAH_CH0_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**CH0_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH0_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. • 0 = FALSE • 1 = TRUE
10	0h RO	**CH0_LOCK_EN:** The value of this register is derived from the DMAH_CH0_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. • 0 = FALSE • 1 = TRUE
9	1h RO	**CH0_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH0_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
8	1h RO	**CH0_DST_SCA_EN:** The value of this register is derived from the DMAH_CH0_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. • 0 = FALSE • 1 = TRUE
7	0h RO	**CH0_STAT_SRC:** The value of this register is derived from the DMAH_CH0_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
6	0h RO	**CH0_STAT_DST:** The value of this register is derived from the DMAH_CH0_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. • 0 = FALSE • 1 = TRUE
5:3	0h RO	**CH0_STW:** Refer to the description for bit field DMA_COMP_PARAMS_2_LO.CH0_DTW
2:0	0h RO	**CH0_DTW:** The value of this register is derived from the DMAH_CH0_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. • 0h = NO_HARDCODE • 1h = 8 • 2h = 16 • 3h = 32 • 4h = 64 • 5h = 128 • 6h = 256 • 7h = reserved

24.5.248 DW_ahb_dmac Component Parameters Register 2 - High (DMA_COMP_PARAMS_2_HI)—Offset 3ECh

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CH7_MULTI_BLK_TYPE				CH6_MULTI_BLK_TYPE				CH5_MULTI_BLK_TYPE				CH4_MULTI_BLK_TYPE				CH3_MULTI_BLK_TYPE				CH2_MULTI_BLK_TYPE				CH1_MULTI_BLK_TYPE				CH0_MULTI_BLK_TYPE			

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**CH7_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
27:24	0h RO	**CH6_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
23:20	0h RO	**CH5_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
19:16	0h RO	**CH4_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**CH3_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
11:8	0h RO	**CH2_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
7:4	0h RO	**CH1_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP
3:0	0h RO	**CH0_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. • 0h = NO_HARDCODE • 1h = CONT_RELOAD • 2h = RELOAD_CONT • 3h = RELOAD_RELOAD • 4h = CONT_LLP • 5h = RELOAD_LLP • 6h = LLP_CONT • 7h = LLP_RELOAD • 8h = LLP_LLP

24.5.249 DW_ahb_dmac Component Parameters Register 1 - Low (DMA_COMP_PARAMS_1_LO)—Offset 3F0h

This is a constant read-only register that contains encoded information about the component parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: AAAAAAAAh

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0
CH7_MAX_BLK_SIZE	CH6_MAX_BLK_SIZE	CH5_MAX_BLK_SIZE	CH4_MAX_BLK_SIZE	CH3_MAX_BLK_SIZE	CH2_MAX_BLK_SIZE	CH1_MAX_BLK_SIZE	CH0_MAX_BLK_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:28	ah RO	**CH7_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. • 0h = 3 • 1h = 7 • 2h = 15 • 3h = 31 • 4h = 63 • 5h = 127 • 6h = 255 • 7h = 511 • 8h = 1023 • 9h = 2047 • Ah = 4095
27:24	ah RO	**CH6_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
23:20	ah RO	**CH5_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
19:16	ah RO	**CH4_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
15:12	ah RO	**CH3_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
11:8	ah RO	**CH2_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
7:4	ah RO	**CH1_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.
3:0	ah RO	**CH0_MAX_BLK_SIZE:** Refer to the description for DMA_COMP_PARAMS_1_LO.CH7_MAX_BLK_SIZE.

24.5.250 DW_ahb_dmac Component Parameters Register 1 - High (DMA_COMP_PARAMS_1_HI)—Offset 3F4h

Refer to the description for DW_ahb_dmac Component Parameters Register 1 - Low.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 37000F04h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0
Undefined		STATIC_ENDIAN_SELECT	ADD_ENCODED_PARAMS	NUM_HS_INT					M4_HDATA_WIDTH		M3_HDATA_WIDTH		M2_HDATA_WIDTH		M1_HDATA_WIDTH		S_HDATA_WIDTH		NUM_MASTER_INT		NUM_CHANNELS			Undefined0				MABRST	INTR_IO		BIG_ENDIAN

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Undefined:** Reserved.
29	1h RO	**STATIC_ENDIAN_SELECT:** The value of this register is derived from the DMAH_STATIC_ENDIAN_SELECT coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE
28	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the DMAH_ADD_ENCODED_PARAMS coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE
27:23	0eh RO	**NUM_HS_INT:** The value of this register is derived from the DMAH_NUM_HS_INT coreConsultant parameter. For a description of this parameter, refer to page 102. • 0h0 = 0 • to • 1h0 = 16
22:21	0h RO	**M4_HDATA_WIDTH:** The value of this register is derived from the DMAH_M4_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits

Bit Range	Default & Access	Field Name (ID): Description
20:19	0h RO	**M3_HDATA_WIDTH:** The value of this register is derived from the DMAH_M3_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
18:17	0h RO	**M2_HDATA_WIDTH:** The value of this register is derived from the DMAH_M2_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
16:15	0h RO	**M1_HDATA_WIDTH:** The value of this register is derived from the DMAH_M1_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
14:13	0h RO	**S_HDATA_WIDTH:** The value of this register is derived from the DMAH_S_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. • 0h = 32 bits • 1h = 64 bits • 2h = 128 bits • 3h = 256 bits
12:11	01h RO	**NUM_MASTER_INT:** The value of this register is derived from the DMAH_NUM_MASTER_INT coreConsultant parameter. For a description of this parameter, refer to page 102. 0h = 1 to 3h = 4
10:8	7h RO	**NUM_CHANNELS:** The value of this register is derived from the DMAH_NUM_CHANNELS coreConsultant parameter. For a description of this parameter, refer to page 102. 0h = 1 to 7h = 8
7:4	0h RW	**Undefined0:** Reserved.
3	0h RO	**MABRST:** The value of this register is derived from the DMAH_MABRST coreConsultant parameter. For a description of this parameter, refer to page 103. • 0 = FALSE • 1 = TRUE
2:1	2h RO	**INTR_IO:** The value of this register is derived from the DMAH_INTR_IO coreConsultant parameter. For a description of this parameter, refer to page 103. • 0h = ALL • 1h = TYPE • 2h = COMBINED • 3h = reserved
0	0h RO	**BIG_ENDIAN:** The value of this register is derived from the DMAH_BIG_ENDIAN coreConsultant parameter. For a description of this parameter, refer to page 104. • 0 = FALSE • 1 = TRUE

24.5.251 DMA Component ID RegisterDma - Low (DmaCompsID_LO)—Offset 3F8h

This is the DW_ahb_dmac Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 44571110h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

DMA_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44571110h RO	**Designware Component Type (DMA_COMP_TYPE):** Designware Component Type number = 0x44_57_11_10. This assigned unique hex value is constant and is derived from the two ASCII letters -DW- followed by a 32-bit unsigned number.

24.5.252 DMA Component ID Register - High (DmaCompsID_HI)—Offset 3FCh

This is the DW_ahb_dmac Component Version register, which is a read-only register that specifies the version of the packaged component in the upper 32 bits and the component type in the lower 32 bits.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 3231362Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	1	0	1	1	0	0	0	1	0	1	0	1	0

DMA_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3231362ah RO	**Version of the Component (DMA_COMP_VERSION):** Reserved.

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24.6 SIO PWM 0 Memory Mapped I/O Registers

Table 256. Summary of PWM 0 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"PWM Control Register (PWMCTRL)—Offset 0h" on page 3800	00010000h
804–807h	4	"Software Reset (RESETS)—Offset 804h" on page 3801	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 3801	00000010h

24.6.1 PWM Control Register (PWMCTRL)—Offset 0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00010000h

31	30	29:24	23:8	7:0
0	0	0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
PWM_ENABLE	PWM_SW_UPDATE	RSVD0	PWM_BASE_UNIT	PWM_ON_TIME_DIVISOR

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PWM Enable (PWM_ENABLE):** • 0 = Disable PWM Output • 1 = Enable PWM Output
30	0b RW	**PWM Software Update (PWM_SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. • 0 = No updates pending • 1 = Update pending
29:24	0b RO	**RSVD0:** Reserved
23:8	0100h RW	**PWM Base Unit (PWM_BASE_UNIT):** Base unit register. Unsigned 8 integer bits, 8 fraction bits. Used to determine PWM output frequency.
7:0	00h RW	**PWM On Time Divisor (PWM_ON_TIME_DIVISOR):** PWM duty cycle = PWM_on-time_divisor/256.

24.6.2 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																														reset_apb	reset_func

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

24.6.3 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
RSVD0																										gpo3	gpo2	gpo1	reset_e	sleep_enable	power_enable

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RO	**RSVD0:** Reserved
5	0h RW	**gpo3:** not applicable
4	1h RW	**gpo2:** not applicable

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**gpo1:** not applicable
2	0h RW	**reset_e:** not applicable
1	0h RW	**sleep_enable:** not applicable
0	0h RW	**power_enable:** not applicable

24.7 SIO PWM 1 PCI Configuration Registers

Table 257. Summary of PWM 1 PCI Configuration Registers—0/30/2

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3803	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3804	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3805	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3805	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 3806	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3807	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3807	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3808	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3808	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3809	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3809	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3810	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 3811	00000000h

24.7.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

Bits 31:16: DEVICEID; Bits 15:0: VENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

24.7.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:2] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0	SSE	RMA	RTA	STA	Reserved1	CAPLIST	INTR_STATUS	Reserved2	Reserved3	INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5	BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

24.7.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
CLASS_CODES	RID

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

24.7.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + Ch

Default: 00800000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0								MULFNDEV	HEADERTYPE							LATTIMER								CACHELINE_SIZE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

24.7.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR																				SIZEINDICATOR								PREFETCHABLE	TYPE		MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

24.7.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR1																				SIZEINDICATOR1								PREFETCHABLE1	TYPE1		MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

24.7.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SUBSYSTEMID | SUBSYSTEMVENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

24.7.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:2] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

24.7.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:2] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:8	7:0
Reserved0	CAPPTR_POWER

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

24.7.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:2] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

31:24	23:16	15:12	11:8	7:0
MAX_LAT	MIN_GNT	Reserved0	INTPIN	INTLINE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

24.7.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:2] + 80h

Default: 00030001h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	

PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

24.7.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:2] + 84h

Default: 00000008h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	

Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

24.7.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

24.8 sSIO PWM 1 Memory Mapped I/O Registers

Table 258. Summary of PWM 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"PWM Control Register (PWMCTRL)—Offset 0h" on page 3812	00010000h
804–807h	4	"Software Reset (RESETS)—Offset 804h" on page 3813	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 3813	00000010h

24.8.1 PWM Control Register (PWMCTRL)—Offset 0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PWM_ENABLE	PWM_SW_UPDATE	RSVD0						PWM_BASE_UNIT																PWM_ON_TIME_DIVISOR							

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**PWM Enable (PWM_ENABLE):** • 0 = Disable PWM Output • 1 = Enable PWM Output
30	0b RW	**PWM Software Update (PWM_SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. • 0 = No updates pending • 1 = Update pending
29:24	0b RO	**RSVD0:** Reserved
23:8	0100h RW	**PWM Base Unit (PWM_BASE_UNIT):** Base unit register. Unsigned 8 integer bits, 8 fraction bits. Used to determine PWM output frequency.
7:0	00h RW	**PWM On Time Divisor (PWM_ON_TIME_DIVISOR):** PWM duty cycle = PWM_on-time_divisor/256.

24.8.2 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reserved (31:2), reset_apb (1), reset_func (0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

24.8.3 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Fields: RSVD0 (31:6), gpo3 (5), gpo2 (4), gpo1 (3), reset_e (2), sleep_enable (1), power_enable (0)

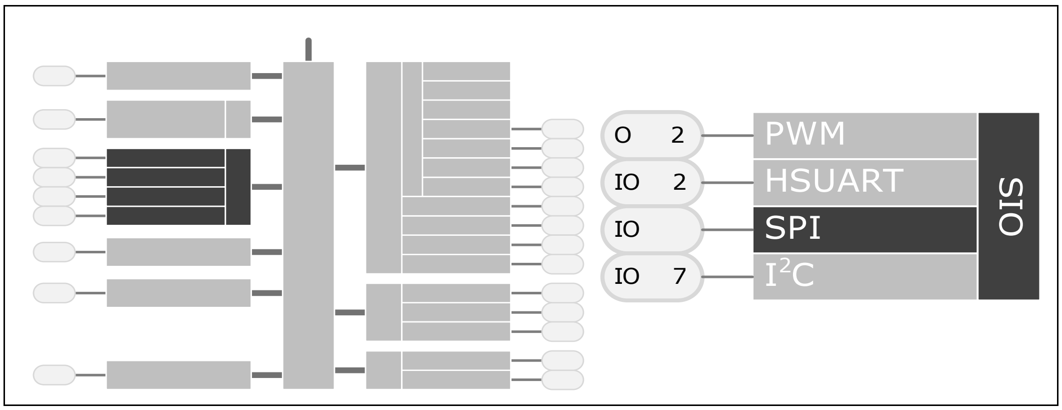
Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RO	**RSVD0:** Reserved
5	0h RW	**gpo3:** not applicable
4	1h RW	**gpo2:** not applicable

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**gpo1:** not applicable
2	0h RW	**reset_e:** not applicable
1	0h RW	**sleep_enable:** not applicable
0	0h RW	**power_enable:** not applicable

25 SIO - Serial Peripheral Interface (SPI)

The Serial I/O implements one SPI controller that supports master mode.

Note: This SPI controller does not support platform firmware (BIOS). See the SPI controller in the PCU instead.



25.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Figure 115.SPI Interface Signals (Sheet 1 of 2)

Signal Name	Direction Plat. Power	Description
SIO_SPI_CLK	I/O V1P8S	**SPI Serial Clock**

Figure 115.SPI Interface Signals (Sheet 2 of 2)

Signal Name	Direction Plat. Power	Description
SIO_SPI_CS#	I/O V1P8S	**SPI Chip Select** SPI Chip Select is active low.
SIO_SPI_MOSI	O V1P8S	**SPI Master Output Slave Input**
SIO_SPI_MISO	I V1P8S	**SPI Slave Output Master Input**

25.2 Features

The following is a list of SPI features:

- Single interrupt line
  - Could be assigned to interrupt PCI INT [A] or ACPISIO INT[1]
- Configurable frame format, clock polarity and clock phase
- supporting one SPI peripheral only
- Supports master mode only
- Receive and transit buffers are both 256x32bits
  - The receive buffer has only 1 water mark
  - The transmit buffer has 2 water marks
- Supports up to 15 Mbps

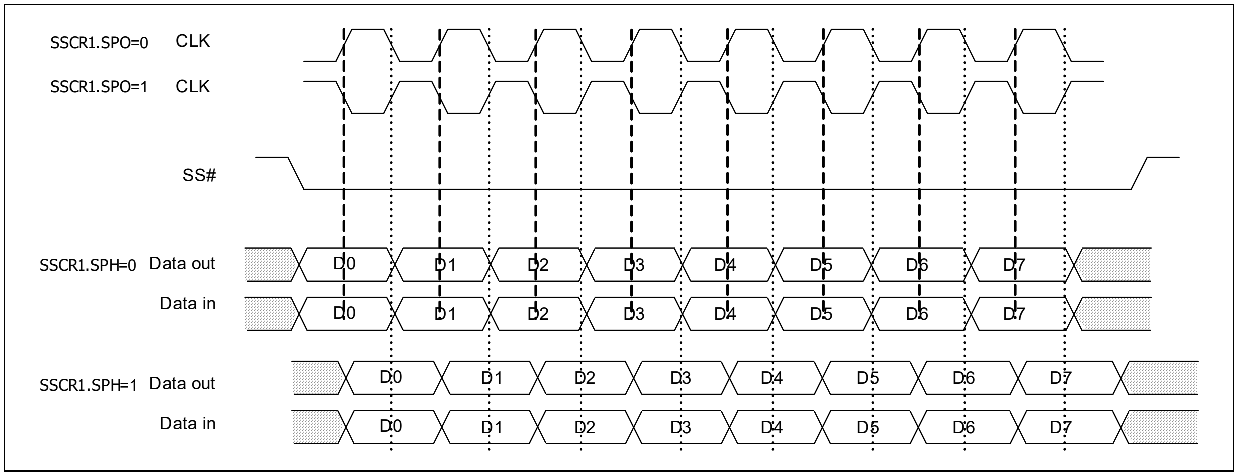
25.2.1 Clock Phase and Polarity

SPI clock phase and clock polarity overview.

- The SSCR1.SPO polarity setting bit determines whether the serial transfer occurs on the rising edge of the clock or the falling edge of the clock.
  - When SSCR1.SPO = 0, the inactive or idle state of SIO_SPI_CLK is low.
  - When SSCR1.SPO = 1, the inactive or idle state of SIO_SPI_CLK is high.
- The SSCR1.SPH phase setting bit selects the relationship of the serial clock with the slave select signal.
  - When SSCR1.SPH = 0, SIO_SPI_CLK is inactive until one cycle after the start of a frame and active until 1/2 cycle after the end of a frame.
  - When SSCR1.SPH = 1, SIO_SPI_CLK is inactive until 1/2 cycle after the start of a frame and active until one cycle after the end of a frame.

Below figure shows an 8-bit data transfer with different phase and polarity settings.

Figure 116.Clock Phase and Polarity



- In a single frame transfer, the SPI controller supports all four possible combinations for the serial clock phase and polarity.

25.2.2 Mode Numbers

The combinations of polarity and phases are referred to as modes which are commonly numbered according to the following convention, with SSCR1.SPO as the high order bit and SSCR1.SPH as the low order bit.

Table 259. SPI Modes

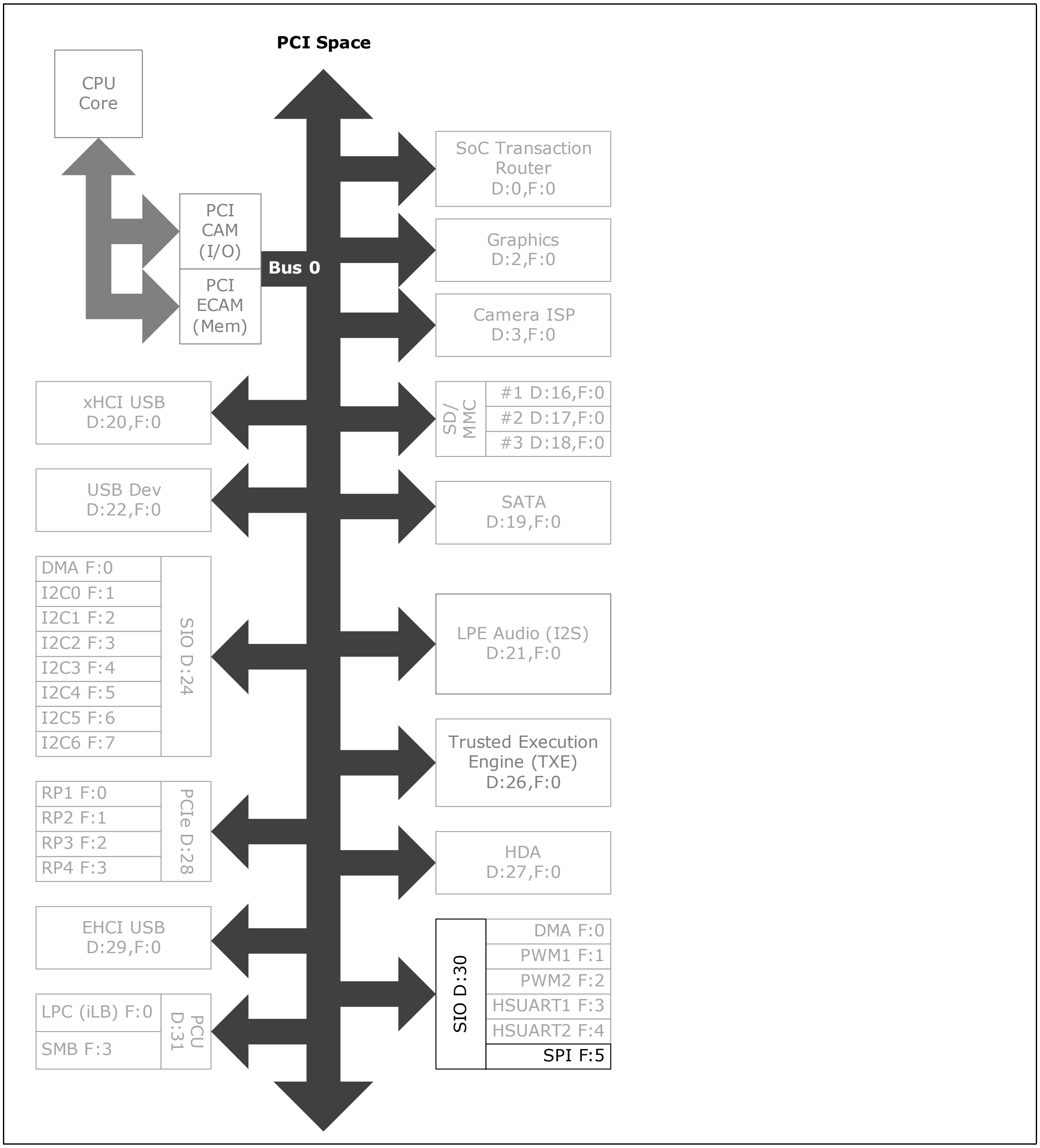
Mode	SSCR1.SPO	SSCR1.SPH
0	0	0
1	0	1
2	1	0
3	1	1

25.2.3 Frame Direction

The SSCR1.SFRMDIR bit is a read-write bit that determines whether the SSP is the master or slave with respect to driving the SSPSFRM. When SSCR1.SFRMDIR=0, the SSP generates the SSPSFRM internally, acts as the master and drives it. When SSCR1.SFRMDIR=1, the SSP acts as the slave and receives the SSPSFRM signal from an external device. When the SSP is to be configured as a slave to the frame, the external device driving frame must wait until the SSSR.CSS bit is cleared after enabling the SSP before asserting frame (i.e. not external clock cycles are needed, the external device just needs to wait a certain amount of time before asserting frame). When the GPIO alternate function is selected for the SSP, this bit has precedence over the GPIO direction bit (i.e. if SFRMDIR=1, the GPIO is an input, and if SFRMDIR=0, then the pin is an output). Therefore, the SCLKDIR and SFRMDIR bits should be written to before the GPIO direction bits (to prevent any possible contention of the SSPSCLK or SSPSFRM pins). Also, when the SCLKDIR bit is set, the SSCR0.NCS and SSCR0.ECS bits must be cleared.

25.3 Register Map

Figure 117. SIO - SPI Register Map



§

25.4 SIO SPI PCI Configuration Registers

Table 260. Summary of SPI PCI Configuration Registers—0/30/5

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3820	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3820	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3822	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3822	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 3823	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3823	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3824	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3825	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3825	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3826	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3826	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3827	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 3828	00000000h

25.4.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

25.4.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:5] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

25.4.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:5] + 8h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

CLASS_CODES | RID

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

25.4.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:5] + Ch

Default: 00800000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 1 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved0 | MULFNDEV | HEADERTYPE | LATTIMER | CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

25.4.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

25.4.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BASEADDR1 | SIZEINDICATOR1 | PREFETCHABLE1 | TYPE1 | MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

25.4.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SUBSYSTEMID | SUBSYSTEMVENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

25.4.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:5] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

25.4.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:5] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0 (bits 31:8) | CAPPTR_POWER (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

25.4.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 3Ch

Default: 00000100h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 0 0 0

MAX_LAT | MIN_GNT | Reserved0 | INTPIN | INTLINE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

25.4.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 80h

Default: 00030001h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1

PMESUPPORT | Reserved0 | VERSION | NXTCAP | POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

25.4.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Reserved0																PMESTATUS	Reserved1						PMEENABLE	Reserved2				NO_SOFT_RESET	Reserved3	POWERSTATE	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

25.4.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

25.5 SIO SPI Memory Mapped I/O Registers

Table 261. Summary of SPI Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Control Register 0 (SSCR0)—Offset 0h" on page 3829	00000000h
4–7h	4	"SSP Control Register 1 (SSCR1)—Offset 4h" on page 3831	00000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 3833	0000F004h
C–Fh	4	"SSP Interrupt Test Register (SSITR)—Offset Ch" on page 3834	00000000h
10–13h	4	"SSP Data (SSDR)—Offset 10h" on page 3835	00000000h
28–2Bh	4	"SSP Time Out (SSTO)—Offset 28h" on page 3836	00000000h
2C–2Fh	4	"SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch" on page 3836	00000000h
30–33h	4	"SSP TX Time Slot Active (SSTSA)—Offset 30h" on page 3837	00000000h
34–37h	4	"SSP RX Time Slot Active (SSRSA)—Offset 34h" on page 3838	00000000h
38–3Bh	4	"SSP Time Slot Status (SSTSS)—Offset 38h" on page 3838	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 3839	00000000h
40–43h	4	"I2S Transmit FIFO (ITF)—Offset 40h" on page 3840	00000000h
44–47h	4	"SPI Transmit FIFO (SITF)—Offset 44h" on page 3841	00000000h
48–4Bh	4	"SPI Receive FIFO (SIRF)—Offset 48h" on page 3841	00000000h
400–403h	4	"Private Clock Params (PRV_CLOCK_PARAMS)—Offset 400h" on page 3842	00000000h
404–407h	4	"Software Reset (RESETS)—Offset 404h" on page 3842	00000000h
408–40Bh	4	"General Purpose Register (GENERAL)—Offset 408h" on page 3843	00000010h
40C–40Fh	4	"reg_SSP_REG (SSP_REG)—Offset 40Ch" on page 3844	00000000h
418–41Bh	4	"reg_SPI_CS_CTRL_REG (SPI_CS_CTRL)—Offset 418h" on page 3845	00000000h

25.5.1 SSP Control Register 0 (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

Bits	31	30	29	28	27–24	23	22	21	20	19–8	7	6	5–4	3–0
Default	0	0	0	0	0000	0	0	0	0	000000000000	0	0	00	0000
Field	MOD	ACS	RSVD	RSVD	FRDC	TIM	RIM	NCS	EDSS	SCR	SSE	ECS	FRF	DSS

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**Mode (MOD):** • 0 = Normal SSP Mode • 1 = Network Mode
30	0b RW	**Audio Clock Select (ACS):** • 0 = Clock selection is determined by the NCS and ECS bits • 1 = Audio Clock (and Audio Clock Divider) are used to create the SSP's serial clock (SSPSCLK)
29	0b RO	**Reserved (RSVD):** Reserved.
28:27	00b RO	**RSVD:** Reserved
26:24	000b RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0b RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** • 0 = TUR events will generate an SSP interrupt • 1 = TUR events will not generate an SSP interrupt
22	0b RW	**Receive FIFO Over Run Interrupt Mask (RIM):** • 0 = ROR events will generate an SSP interrupt • 1 = ROR events will not generate an SSP interrupt
21	0b RW	**Network Clock Select (NCS):** • 0 = Clock selection is determined by ECS bit • 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0b RW	**Extended Data Size Select (EDSS):** • 0 = A zero is prepended to the DSS value, which sets the DSS range from 4-16 bits • 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	000h RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b RW	**Synchronous Serial Port Enable (SSE):** • 0 = SSP operation disabled • 1 = SSP operation enabled
6	0b RW	**External Clock Select (ECS):** • 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) • 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	00b RW	**Frame Format (FRF):** • 00 = Motorola Serial Peripheral Interface (SPI) • 01 = Texas Instruments Synchronous Serial Protocol (SSP) • 10 = National Semiconductor Microwire • 11 = Programmable Serial Protocol (PSP)
3:0	0000b RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

25.5.2 SSP Control Register 1 (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TTELP	TTE	EBCEI	SCFR	ECRA	ECRB	SCLKDIR	SFRMDIR	RWOT	TRAIL	TSRE	RSRE	TINTE	PINTE	RSVD	IFS	STRF	EFWR	RFT				TFT				MWDS	SPH	SPO	LBM	TIE	RIE

Bit Range	Default & Access	Field Name (ID): Description
31	0b RW	**TXD Tristate Enable on Last Phase (TTELP):** • 0 = TXD line will be tristated on same clock edge as TXD is to be flopped • 1 = TXD line will be tristated clock edge after TXD is to be flopped
30	0b RW	**TXD Tristate Enable (TTE):** • 0 = TXD line will not be tristated • 1 = TXD line will be tristated when no transmitting data
29	0b RW	**Enable Bit Count Error Interrupt (EBCEI):** • 0 = Interrupt due to a bit count error is disabled • 1 = Interrupt due to a bit count error is enabled
28	0b RW	**Slave Clock Free Running (SCFR):** • 0 = clock input to SSPSCLK is continuously running • 1 = clock input to SSPSCLK is only active durring transfers
27	0b RW	**Enable Clock Request A (ECRA):** • 0 = clock request from other SSP is disabled • 1 = clock request from other SSP is enabled
26	0b RW	**Enable Clock Request B (ECRB):** • 0 = clock request from other SSP is disabled • 1 = clock request from other SSP is enabled
25	0b RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** • 0 = Master mode, SSP drives SSPSCLK • 1 = Slave mode, SSP recieves SSPSCLK
24	0b RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** • 0 = Master mode, SSP drives SSPSFRM • 1 = Slave mode, SSP receives SSPSFRM
23	0b RW	**Receive With Out Transmit (RWOT):** • 0 = Transmit/Receive mode • 1 = Receive without Transmit mode
22	0b RW	**Trailing Byte (TRAIL):** • 0 = Processor based, trailing bytes are handled by processor • 1 = DMA based, trailing bytes are handled by DMA

Bit Range	Default & Access	Field Name (ID): Description
21	0b RW	**Transmit Service Request Enable (TSRE):** • 0 = DMA Service Request is disabled • 1 = DMA Service Request is enabled
20	0b RW	**Receive Service Request Enable (RSRE):** • 0 = DMA Service Request is disabled • 1 = DMA Service Request is enabled
19	0b RW	**Receiver Time-out Interrupt Enable (TINTE):** • 0 = Receiver Time-out interrupts are disabled • 1 = Receiver Time-out interrupts are enabled
18	0b RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** • 0 = Peripheral Trailing Byte Interrupts are disabled • 1 = Peripheral Trailing Byte Interrupts are enabled
17	0b RW	**RSVD:** Reserved
16	0b RW	**Invert Frame Signal (IFS):** • 0 = Frame polarity is determined by SSP format and PSP polarity bits. • 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format and PSP polarity bits).
15	0b RW	**STRF:** Select FIFO for EFWR (test mode bit) (when EFWR=1) • 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) • 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0b RW	**Enable FIFO Write/Read (EFWR):** Test mode bit. • 0 = FIFO write/read special function is disabled (normal SSP operational mode) • 1 = FIFO write/read special function is enabled
13:10	0000b RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
9:6	0000b RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
5	0b RW	**Microwire Transmit Data Size (MWDS):** • 0 = 8-bit command words are transmitted • 1 = 16-bit command words are transmitted
4	0b RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** • 0 = SSPSCLK is inactive one cycle at the start of a frame and cycle at the end of a frame • 1 = SSPSCLK is inactive cycle at the start of a frame and one cycle at the end of a frame
3	0b RW	**Motorola SPI SSPSCLK Polarity Setting (SPO):** • 0 = The inactive or idle state of SSPSCLK is low • 1 = The inactive or idle state of SSPSCLK is high
2	0b RW	**Loop-Back Mode (LBM):** Test mode bit. • 0 = Normal serial port operation enabled • 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0b RW	**Transmit FIFO Interrupt Enable (TIE):** • 0 = Transmit FIFO level interrupt is disabled • 1 = Transmit FIFO level interrupt is enabled

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Receive FIFO Interrupt Enable (RIE):** • 0 = Receive FIFO level interrupt is disabled • 1 = Receive FIFO level interrupt is enabled

25.5.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 0000F004h

Bits	31:24	23	22	21	20	19	18	17:16	15:12	11:8	7	6	5	4	3	2	1:0
Default	0 0 0 0 0 0 0 0	0	0	0	0	0	0	0 0	1 1 1 1	0 0 0 0	0	0	0	0	0	1	0 0
Field	RSVD1	BCE	CSS	TUR	EOC	TINT	PINT	RSVD2	RFL	TFL	ROR	RFS	TFS	BSY	RNE	TNF	RSVD3

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RSVD1:** Reserved
23	0b RW1C	**Bit Count Error (BCE):** • 0 = SSP has not experienced a bit count error • 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0b RO	**Clock Synchronization Status (CSS):** • 0 = SSP is ready for slave clock operations • 1 = SSP is currently busy synchronizing slave mode signals
21	0b RW1C	**Transmit FIFO Under Run (TUR):** • 0 = Transmit FIFO has not experienced an under run • 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0b RW1C	**End of Chain (EOC):** • 0 = DMA has not signaled an end of chain condition • 1 = DMA has signaled an end of chain condition
19	0b RW1C	**Receiver Time-out Interrupt (TINT):** • 0 = No receiver time-out pending • 1 = Receiver time-out pending
18	0b RW1C	**Peripheral Trailing Byte Interrupt (PINT):** • 0 = No peripheral trailing byte interrupt pending • 1 = Peripheral trailing byte interrupt pending

Bit Range	Default & Access	Field Name (ID): Description
17:16	00b RO	**RSVD2:** Reserved
15:12	1111b RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. **Note:** When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit.
11:8	0000b RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. **Note:** When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit.
7	0b RW1C	**Receive FIFO Overrun (ROR):** • 0 = Receive FIFO has not experienced an overrun • 1 = Attempted data write to full receive FIFO, request interrupt
6	0b RO	**Receive FIFO Service Request (RFS):** • 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled • 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0b RO	**Transmit FIFO Service Request (TFS):** • 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled • 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0b RO	**SSP Busy (BSY):** • 0 = SSP is idle or disabled • 1 = SSP currently transmitting or receiving a frame
3	0b RO	**Receive FIOF Not Empty (RNE):** • 0 = Receive FIFO is empty • 1 = Receive FIFO is not empty
2	1b RO	**Transmit FIFO Not Full (TNF):** • 0 = Transmit FIFO is full • 1 = Transmit FIFO is not full
1:0	00b RO	**RSVD3:** Reserved

25.5.4 SSP Interrupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD1																								TROR	TRFS	TTFS	RSVD2				

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**RSVD1:** Reserved
7	0b RW	**Test Receive FIFO Overrun (TROR):** • 0 = No receive FIFO overrun service request • 1 = Generates non-maskable interrupt to CPU. No DMA request is generated.
6	0b RW	**Test Receive FIFO Service Request (TRFS):** • 0 = No receive FIFO service request • 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0b RW	**Test Transmit FIFO Service Request (TTFS):** • 0 = No transmit FIFO service request pending • 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	00000b RO	**RSVD2:** Reserved

25.5.5 SSP Data (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

DATA

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**DATA:** Data word to be written to/read from transmit/receive FIFO.

25.5.6 SSP Time Out (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RSVD (31:24) | TIMEOUT (23:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**RSVD:** Reserved
23:0	000000h RW	**Timeout Value (TIMEOUT):** This is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency.

25.5.7 SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

RSVD1	FSRT	DMYSTOP	RSVD2	SFRMWDTH	SFRMDLY	DMYSTRT	STRTDLY	ETDS	SFRMP	SCMODE

Bit Range	Default & Access	Field Name (ID): Description
31:26	000000b RO	**RSVD1:** Reserved
25	0b RW	**Frame Sync Relative Timing Bit (FSRT):** • 0 = Next frame is asserted after the end of the T4 timing • 1 = Next frame is asserted with the LSB of the previous frame
24:23	00b RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data.
22	0b RW	**RSVD2:** Reserved
21:16	000000b RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38).
15:9	0000000b RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74).
8:7	00b RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs, after STRTDLY is complete, that precede the transmit/receive data.
6:4	000b RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods).
3	0b RW	**End of Transfer Data State (ETDS):** • 0 = Low • 1 = Last value (bit 0)
2	0b RW	**Serial Frame Polarity (SFRMP):** • 0 = SSPSFRM is active low • 1 = SSPSFRM is active high
1:0	00b RW	**Serial Bit-rate Clock Mode (SCMODE):** • 00 = Data driven (falling), Data sampled (rising), Idle state (low) • 01 = Data driven (rising), Data sampled (falling), Idle state (low) • 10 = Data driven (rising), Data sampled (falling), Idle state (high) • 11 = Data driven (falling), Data sampled (rising), Idle state (high)

25.5.8 SSP TX Time Slot Active (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in. They are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								TTSA							

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**TX Time Slot Active (TTSA):** • 0 = SSP will not transmit data in this time slot • 1 = SSP will transmit data in this time slot

25.5.9 SSP RX Time Slot Active (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in. They are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																								RTSA							

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**RSVD:** Reserved
7:0	00h RW	**RX Time Slot Active (RTSA):** • 0 = SSP will not receive data in this time slot • 1 = SSP will receive data in this time slot

25.5.10 SSP Time Slot Status (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NMBSY	RSVD																												TSS		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Network Mode Busy (NMBSY):** • 0 = No frame is currently active (in network mode only) • 1 = SSP is in network mode and a frame is currently active
30:3	0000000h RO	**RSVD:** Reserved
2:0	000b RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active.

25.5.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																									ACPS			SCDB	ACDS		

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	000b RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit. • 000b = 5.622MHz • 001b = 11.345MHz • 010b = 12.235MHz • 011b = 14.857MHz • 100b = 32.842MHz • 101b = 48.000MHz • 110b, 111b = Reserved
3	0b RW	**SYSCLK Divider Bypass (SCDB):** • 0 = SYSCLK is divided by 4 before being sent to SSP • 1 = SYSCLK is not divided before being sent to SSP
2:0	000b RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

25.5.12 I2S Transmit FIFO (ITF)—Offset 40h

The I2S Transmit FIFO register is for writing the water mark for the I2S transmit FIFO, and also for reading the number of entries in the I2S transmit FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

Bits	31	30:20	19:10	9:0
Field	RSVD	ITFL	LWMTF	HWMTF
Default	0	000 0000 0000	00 0000 0000	00 0000 0000

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**RSVD:** Reserved
30:20	0b RO	**I2S Transmit FIFO Level (ITFL):** Number of entries in I2S Transmit FIFO.
19:10	0b RW	**Low Water Mark Transmit FIFO (LWMTF):** Set the low water mark of the I2S transmit FIFO.
9:0	0b RW	**High Water Mark Transmit FIFO (HWMTF):** Set the high water mark of the I2S transmit FIFO.

25.5.13 SPI Transmit FIFO (SITF)—Offset 44h

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RSVD	SITFL	LWMTF	HWMTF

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**RSVD:** Reserved
24:16	0b RO	**SPI Transmit FIFO Level (SITFL):** Number of entries in SPI Transmit FIFO.
15:8	0b RW	**Low Water Mark Transmit FIFO (LWMTF):** Set the low water mark of the SPI transmit FIFO.
7:0	0b RW	**High Water Mark Transmit FIFO (HWMTF):** Set the high water mark of the SPI transmit FIFO.

25.5.14 SPI Receive FIFO (SIRF)—Offset 48h

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO, and also for reading the number of entries in the SPI receive FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RSVD	SIRFL	WMRF

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16:8	0b RO	**SPI Receive FIFO Level (SIRFL):** Number of entries in SPI Receive FIFO.
7:0	0b RW	**WMRF:** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO.

25.5.15 Private Clock Params (PRV_CLOCK_PARAMS)—Offset 400h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
clk_update	n_val															m_val															clk_en

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**clk_update:** Update the clock divider after seeting new m and n values.
30:16	0h RW	**N_VAL (n_val):** n value for the m over n divider.
15:1	0h RW	**M_VAL (m_val):** m value for the m over n divider.
0	0h RW	**clk_en:** clk en of the m over n divider.

25.5.16 Software Reset (RESETS)—Offset 404h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Fields: reserved (31:2), reset_func (1), reset_apb (0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved
1	0h RW	**reset_func:** Reset the func clock domain.
0	0h RW	**reset_apb:** Reset the apb domain.

25.5.17 General Purpose Register (GENERAL)—Offset 408h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000010h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0

Fields: RSVD0 (31:26), spi_terminate_tx_on_rx_full_disable (25), spi1_dma_rxto_holdoff_disable (24), RSVD1 (23:7), gpo3 (6), gpo2 (5), gpo1 (4), reset_e (3), sleep_enable (2), power_enable (1:0)

Bit Range	Default & Access	Field Name (ID): Description
31:26	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**spi_terminate_tx_on_rx_full_disable:** disable terminate tx when rx full
24	0h RW	**spi1_dma_rxto_holdoff_disable:** disable dma hold off
23:6	0b RO	**RSVD1:** Reserved
5	0h RW	**gpo3:** Not applicable.
4	1h RW	**gpo2:** Not applicable.
3	0h RW	**gpo1:** Not applicable.
2	0h RW	**reset_e:** Not applicable.
1	0h RW	**sleep_enable:** Not applicable.
0	0h RW	**power_enable:** Not applicable.

25.5.18 reg_SSP_REG (SSP_REG)—Offset 40Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																												gpio_sspsclken	brg_pio_r	ILB_CKBIT	disable_ssp_dma_finish

Bit Range	Default & Access	Field Name (ID): Description
31:4	0b RO	**RSVD0:** Reserved
3	0h RW	**gpio_sspsclken:** Not applicable.
2	0h RW	**brg_pio_r:** Not applicable.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**ILB_CKBIT:** This bit field is a legacy (chicken bit) bug fix established in previous Intel projects. The driver should set this bit to 0b to ensure correct operation.
0	0h RW	**disable_ssp_dma_finish:** disable ssp dma finish

25.5.19 reg_SPI_CS_CTRL_REG (SPI_CS_CTRL)—Offset 418h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

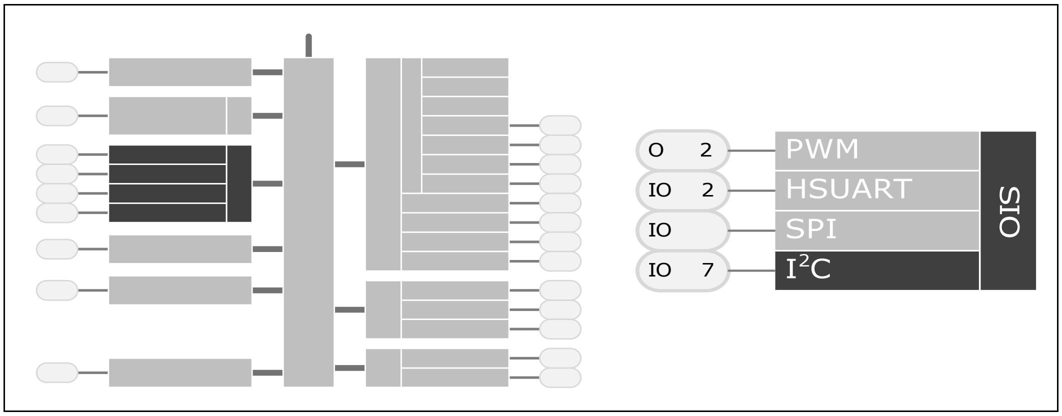
Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																														spi_cs_state	spi_cs_mode

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**reserved:** reserved
1	0h RW	**spi_cs_state:** SW override of CS line in SW mode for spi.
0	0h RW	**spi_cs_mode:** Selects HW mode or SW mode for chip select for spi.

26 SIO - I²C Interface

The SoC supports 7 instances of I²C controller. Both 7-bit and 10-bit addressing modes are supported. These controllers operate in master mode only.



26.1 Signal Descriptions

I²C is a two-wire bus for inter-IC communication. Data and clock signals carry information between the connected devices. The following is the I²C Interface. The SoC supports 7 I²C interfaces for general purpose to control external devices. The I²C signals are muxed over GPIOs.

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 262. I²C[6:0] Signals

Signal Name	Direction Plat. Power	Description
SIO_I2C[6:0]_DATA	I/O V1P8S	**I²C Serial Data** *These signals are muxed and may be used by other functions.*
SIO_I2C[6:0]_CLK	I/O V1P8S	**I²C Serial Clock** *These signals are muxed and may be used by other functions.*

26.2 Features

26.2.1 I²C Protocol

The I²C bus is a two-wire serial interface, consisting of a serial data line and a serial clock. These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a "transmitter" or "receiver," depending on the function of the device. Devices are considered slaves when performing data transfers, as the SoC will always be a Master. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

- The SoC is always the I²C master; and it supports multi-master mode.
- The SoC can support clock stretching by slave devices.
- The SIO_I2Cx_DATA line is a bidirectional signal and changes only while the SIO_I2Cx_CLK line is low, except for STOP, START, and RESTART conditions.
- The output drivers are open-drain or open-collector to perform wire-AND functions on the bus.
- The maximum number of devices on the bus is limited by the maximum capacitance specification of 400 pF
- Refer to Chapter 9, "Electrical Specifications" for details.
- Data is transmitted in byte packages.

26.2.2 I²C Modes of Operation

The I²C module can operate in the following modes:

- Standard mode (with a bit rate up to 100 Kb/s)
- Fast mode (with a bit rate up to 400 Kb/s)
- Fast-mode Plus (Fm+, with a bit rate up to 1 Mb/s)
- High-speed mode (Hs-mode, with a bit rate up to 3.4 Mb/s)

Note: Higher speeds require tuning of the analog buffers. Please work with your BIOS vendor to incorporate.

The I²C can communicate with devices only using these modes as long as they are attached to the bus. Additionally, high speed mode, fast mode plus and fast mode devices are downward compatible.

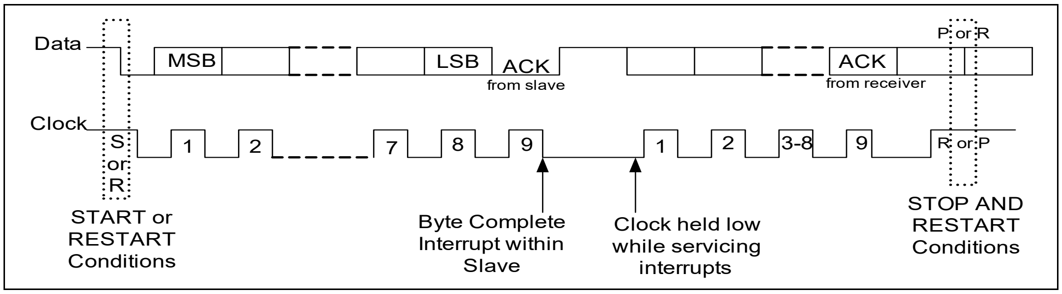
- High-speed mode devices can communicate with fast mode and standard mode devices in a mixed speed bus system.
- Fast mode devices can communicate with standard mode devices in a 0–100 Kb/s I²C bus system.

However, according to the I²C specification, standard mode devices are not upward compatible and should not be incorporated in a fast-mode I²C bus system since they cannot follow the higher transfer rate and unpredictable states would occur.

26.2.3 Functional Description

- The I²C master is responsible for generating the clock and controlling the transfer of data.
- The slave is responsible for either transmitting or receiving data to/from the master.
- The acknowledgment of data is sent by the device that is receiving data, which can be either a master or a slave.
- Each slave has a unique address that is determined by the system designer:
  - When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W), to determine if the master wants to transmit data or receive data from the slave.
  - The slave then sends an acknowledge (ACK) pulse after the address.
- If the master (master-transmitter) is writing to the slave (slave-receiver)
  - The receiver gets one byte of data.
  - This transaction continues until the master terminates the transmission with a STOP condition.
- If the master is reading from a slave (master-receiver)
  - The slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse.
  - This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition. This behavior is illustrated in below figure.

Figure 118. Data Transfer on the I²C Bus



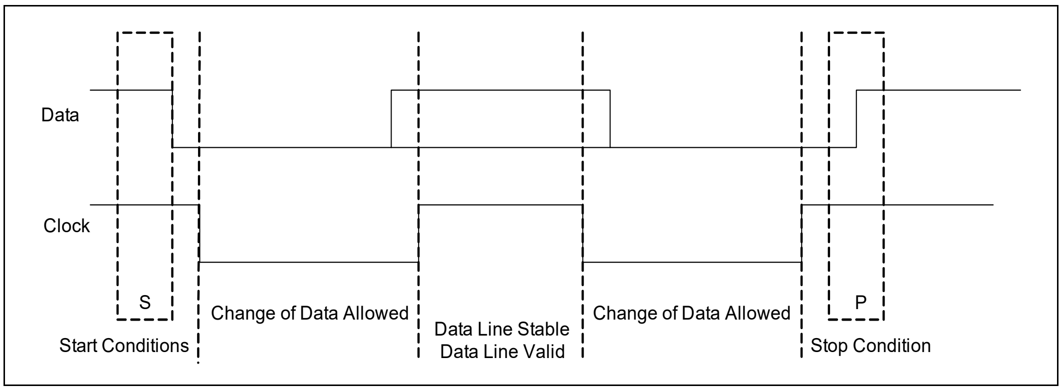
26.2.3.1 START and STOP Conditions

When the bus is idle, both the clock and data signals are pulled high through external pull-up resistors on the bus.

When the master wants to start a transmission on the bus, the master issues a START condition.

- This is defined to be a high-to-low transition of the data signal while the clock is high.
- When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the data line while the clock is high. Figure 119 shows the timing of the START and STOP conditions.
- When data is being transmitted on the bus, the data line must be stable when the clock is high.

Figure 119.START and STOP Conditions



The signal transitions for the START/STOP conditions, as depicted above, reflect those observed at the output of the master driving the I^2C bus. Care should be taken when observing the data/clock signals at the input of the slave(s), because unequal line delays may result in an incorrect data/clock timing relationship.

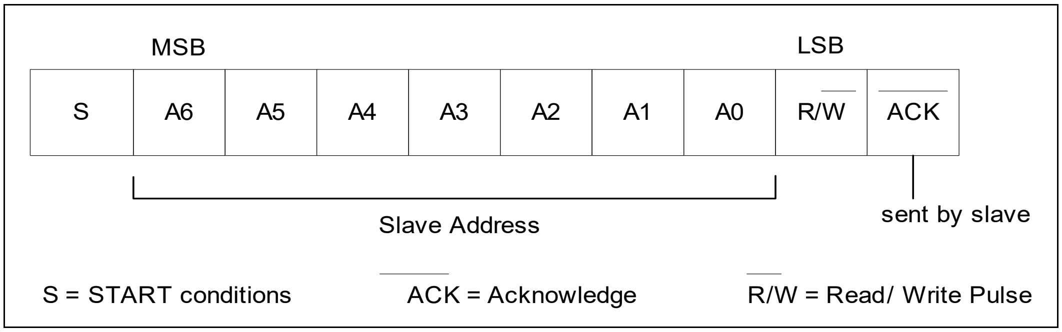
26.2.3.2 Addressing Slave Protocol

There are two address formats—seven-bit address format and 10-bit address format.

Seven-bit Address Format

- During the seven-bit address format, the first seven bits (bits 7:1) of the first byte set the slave address and the LSB bit (bit 0) is the R/W bit as shown in Figure 120.
- When bit 0 (R/W) is set to 0, the master writes to the slave. When bit 0 (R/W) is set to 1, the master reads from the slave.

Figure 120.Seven-Bit Address Format



Ten-bit Address Format

- During 10-bit addressing, 2 bytes are transferred to set the 10-bit address. The transfer of the first byte contains the following bit definition.
  — The first five bits (bits 7:3) notify the slaves that this is a 10-bit transfer. The next two bits (bits 2:1) set the slaves address bits 9:8, and the LSB bit (bit 0) is the RW bit.
  — The second byte transferred sets bits 7:0 of the slave address.
  — Figure 121 shows the 10-bit address format, and Table 263 defines the special purpose and reserved first byte addresses.

Figure 121.Ten-Bit Address Format

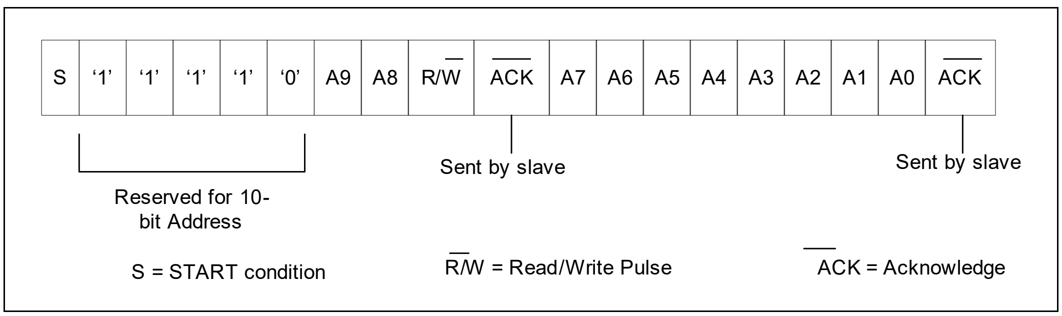


Table 263. I^2C Definition of Bits in First Byte (Sheet 1 of 2)

Slave Address	RW Bit	Description
0000 000	0	**General Call Address**—The I^2C controller places the data in the receive buffer and issues a General Call interrupt.
0000 000	1	**START byte**—For more details, refer to I^2C bus specification section 3.15.
0000 001	X	**CBUS address**—I^2C controller ignores these accesses.
0000 010	X	**Reserved**
0000 011	X	**Reserved**

Table 263. I²C Definition of Bits in First Byte (Sheet 2 of 2)

Slave Address	RW Bit	Description
0000 1XX	X	**High-speed master code**
1111 1XX	X	**Reserved**
1111 0XX	X	**Ten (10)-bit slave addressing**

26.2.3.3 Transmit and Receive Protocol

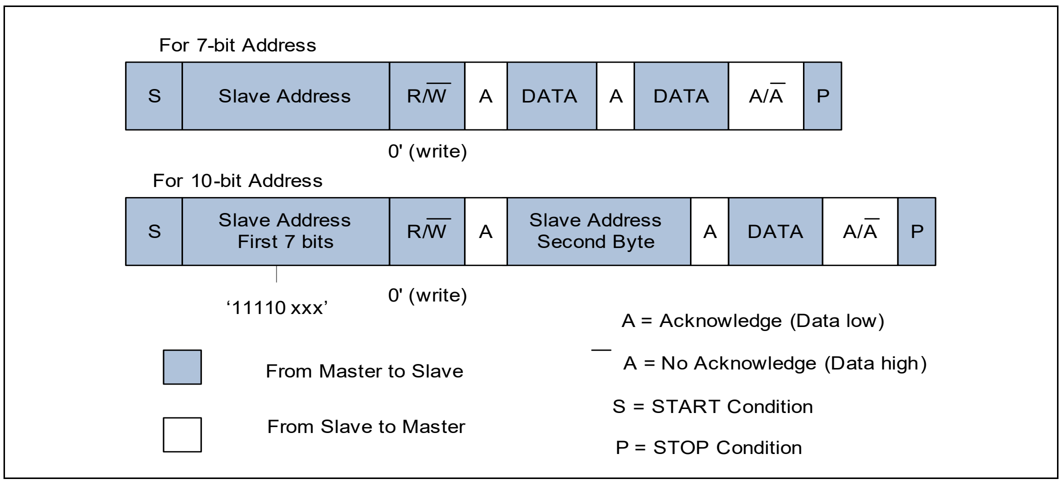
The master can initiate data transmission and reception to/from the bus, acting as either a master-transmitter or master-receiver. A slave responds to requests from the master by either transmitting data or receiving data to/from the bus, acting as either a slave-transmitter or slave-receiver, respectively.

Master-Transmitter and Slave-Receiver

All data is transmitted in byte format, with no limit on the number of bytes transferred per data transfer. After the master sends the address and RW bit or the master transmits a byte of data to the slave, the slave-receiver must respond with the acknowledge signal (ACK). When a slave-receiver does not respond with an ACK pulse, the master aborts the transfer by issuing a STOP condition. The slave must leave the data line high so that the master can abort the transfer.

If the master-transmitter is transmitting data as shown in Figure 122, then the slave-receiver responds to the master-transmitter with an acknowledge pulse after every byte of data is received.

Figure 122. Master Transmitter Protocol

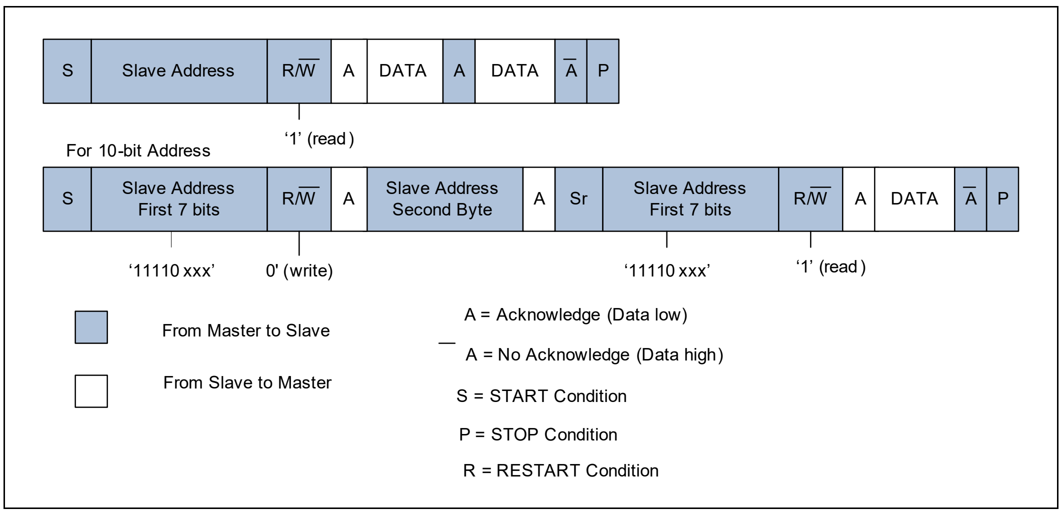


Master-Receiver and Slave-Transmitter

If the master is receiving data as shown in Figure 123, the master responds to the Slave-Transmitter with an acknowledge pulse after a byte of data has been received, except for the last byte. This is the way the Master-Receiver notifies the Slave-Transmitter that this is the last byte. The Slave-Transmitter relinquishes the data line after detecting the No Acknowledge (NACK) so that the master can issue a STOP condition.

When a master does not want to relinquish the bus with a STOP condition, the master can issue a RESTART condition. This is identical to a START condition except it occurs after the ACK pulse. The master can then communicate with the same slave.

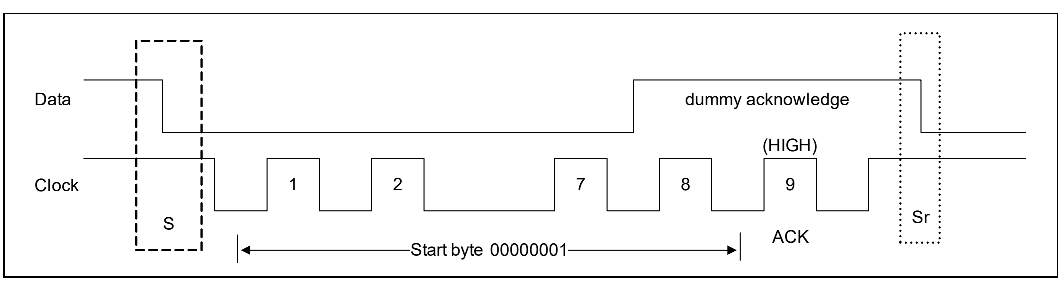
Figure 123. Master Receiver Protocol



26.2.3.4 START BYTE Transfer Protocol

The START BYTE Transfer protocol is set up for systems that do not have an on-board dedicated I^{2}C hardware module. When the I^{2}C controller is a master, it supports the generation of START BYTE transfers at the beginning of every transfer in case a slave device requires it. This protocol consists of 7 '0's being transmitted followed by a 1, as illustrated in Figure 124. This allows the processor that is polling the bus to under-sample the address phase until 0s are detected. Once the microcontroller detects a 0, it switches from the under sampling rate to the correct rate of the master.

Figure 124. START Byte Transfer



The START BYTE procedure is as follows:

1. Master generates a START condition.
2. Master transmits the START byte (0000 0001).
3. Master transmits the ACK clock pulse. (Present only to conform with the byte handling format used on the bus.)
4. No slave sets the ACK signal to 0.
5. Master generates a RESTART (R) condition.

A hardware receiver does not respond to the START BYTE because it is a reserved address and resets after the RESTART condition is generated.

26.3 Use

26.3.1 Master Mode Operation

To use the I^2C controller as a master, perform the following steps:

1. Disable the I^2C controller by writing 0 (zero) to IC_ENABLE.ENABLE.
2. Write to the IC_CON register to set the maximum speed mode supported for slave operation IC_CON.SPEED and to specify whether the I^2C controller starts its transfers in 7/10 bit addressing mode when the device is a slave (IC_CON.IC_10BITADDR_SLAVE).
3. Write to the IC_TAR register the address of the I^2C device to be addressed. It also indicates whether a General Call or a START BYTE command is going to be performed by I^2C. The desired speed of the I^2C controller master-initiated transfers, either 7-bit or 10-bit addressing, is controlled by the IC_TAR.IC_10BITADDR_MASTER bit field.
4. Write to the IC_HS_MADDR register the desired master code for the I^2C controller. The master code is programmer-defined.
5. Enable the I^2C controller by writing a 1 in IC_ENABLE.
6. Now write the transfer direction and data to be sent to the IC_DATA_CMD register. If the IC_DATA_CMD register is written before the I^2C controller is enabled, the data and commands are lost as the buffers are kept cleared when the I^2C controller is not enabled.

The I^2C controller supports updating of the IC_TAR.IC_TAR and IC_TAR.IC_10BITADDR_MASTER. The IC_TAR register can be written to provided the following conditions are met:

- The I^2C controller is not enabled (IC_ENABLE.ENABLE=0)

The I^2C controller supports switching back and forth between reading and writing based on what is written in IC_CMD register. To transmit data, write the data to be written to the lower byte of the I^2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD). The IC_DATA_CMD.CMD should be written to 0 for I^2C write operations. Subsequently, a read command may be issued by writing "don't cares" to IC_DATA_CMD.DAT register bits, and a 1 should be written to the IC_DATA_CMD.CMD bit.

26.3.2 Disabling the I^2C Controller

The register IC_ENABLE allows software to unambiguously determine when the hardware has completely shutdown in response to the IC_ENABLE.ENABLE register being cleared from 1 to 0.

Procedure

1. Define a timer interval (t_{i2c_poll}) equal to 10 times the signaling period for the highest I^2C transfer speed used in the system and supported by the I^2C controller. For example, if the highest I^2C transfer mode is 400Kb/s, then this t_{i2c_poll} is 25 µs.
2. Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.
3. Execute a blocking thread/process/function that prevents any further I^2C master transactions to be started by software, but allows any pending transfers to be completed.
4. The variable POLL_COUNT is initialized to zero (0).
5. Clear IC_ENABLE.ENABLE to zero (0).
6. Read the IC_ENABLE_STATUS.IC_EN bit. Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.
7. If IC_ENABLE_STATUS.IC_EN is 1, then sleep for t_{i2c_poll} and proceed to the previous step. Otherwise, exit with a relevant success code.

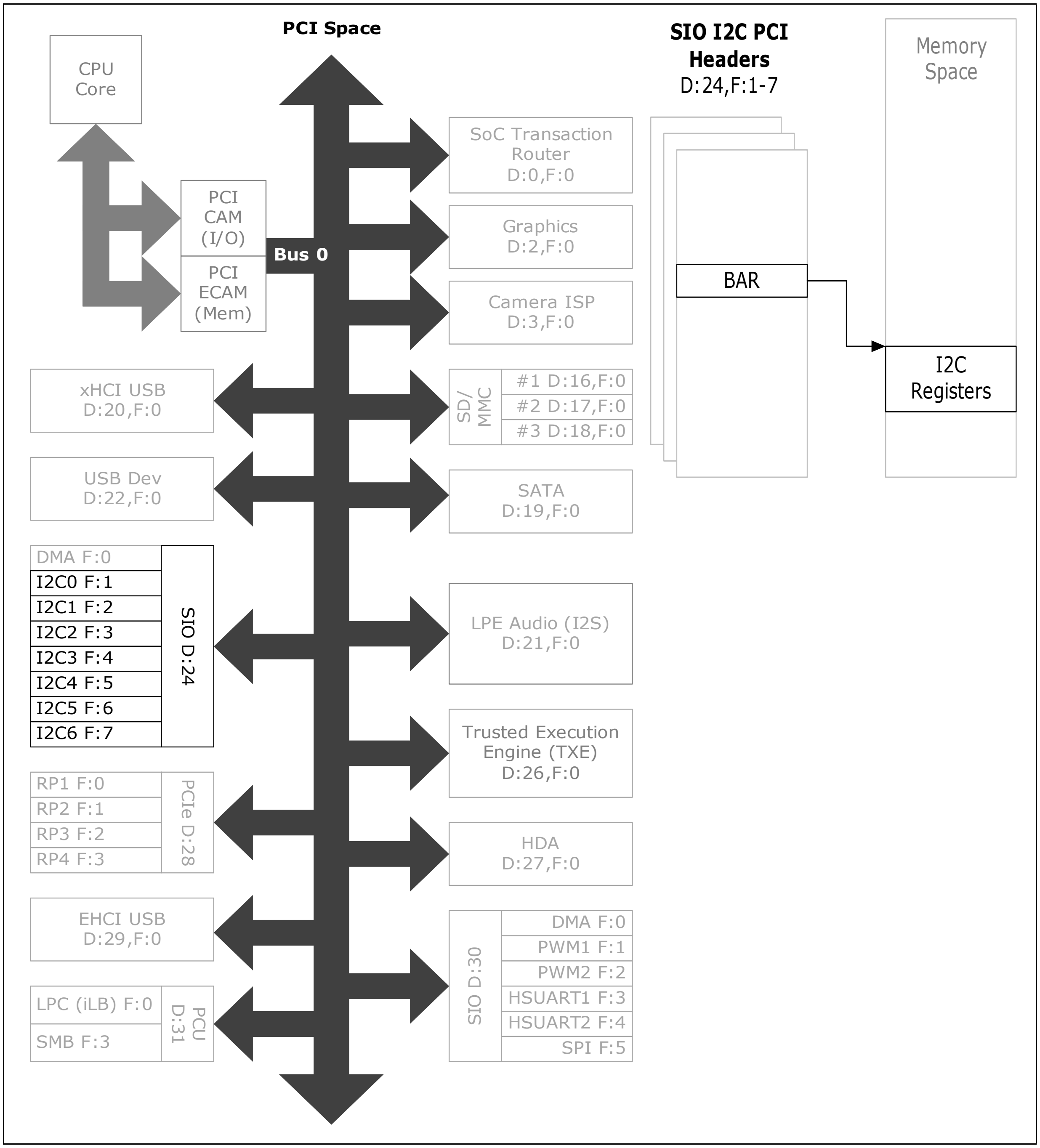
26.4 References

I^2C-Bus Specification and User Manual, Revision 03: http://ics.nxp.com/support/documents/interface/pdf/i2c.bus.specification.pdf

26.5 Register Map

Refer to Chapter 3, "Register Access Methods" and Chapter 4, "Mapping Address Spaces" for additional information.

Figure 125. SIO - I²C Register Map



§

26.6 SIO I^{2}C 0 PCI Configuration Registers

Table 264. Summary of I^{2}C 0 PCI Configuration Registers—0/24/1

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3856	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3857	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3858	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3858	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 3859	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3860	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3860	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3861	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3861	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3862	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3862	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3863	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 3864	00000000h

26.6.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

DEVICEID (bits 31:16) VENDORID (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

26.6.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

26.6.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:1] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLASS_CODES (31:8)	RID (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

26.6.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:1] + Ch

Default: 00800000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0								MULFNDEV	HEADERTYPE							LATTIMER								CACHELINE_SIZE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

26.6.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR																				SIZEINDICATOR								PREFETCHABLE	TYPE		MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

26.6.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 14h

Default: 00000000h

31 28 24 20 16 12 8 4 0

BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

26.6.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

26.6.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
EXPANSION_ROM_BASE																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

26.6.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 34h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Reserved0						CAPPTR_POWER	

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

26.6.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:24, F:1] + 3Ch

Default: 00000100h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0
MAX_LAT		MIN_GNT		Reserved0	INTPIN	INTLINE	

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

26.6.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:24, F:1] + 80h

Default: 00030001h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1

PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

26.6.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 84h

Default: 00000008h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 0 0 0

Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

26.6.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)   **Offset:** [B:0, D:24, F:1] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

26.7 SIO I^2C 0 Memory Mapped I/O Registers

Table 265. Summary of I^2C 0 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 3867	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 3868	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 3869	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 3869	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 3870	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 3871	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 3872	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 3872	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 3873	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 3873	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 3874	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 3875	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 3876	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 3877	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 3878	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 3879	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 3879	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 3880	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 3880	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 3881	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 3881	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 3882	00000000h
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 3882	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 3883	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 3883	00000000h

Table 265. Summary of I^2C 0 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 3884	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 3884	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 3885	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 3886	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 3887	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 3887	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 3888	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 3889	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 3890	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 3891	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 3892	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 3892	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 3893	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 3894	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 3894	00000000h
A0–A3h	4	"IC_FS_SPKLEN—Offset A0h" on page 3895	00000005h
A4–A7h	4	"IC_HS_SPKLEN—Offset A4h" on page 3896	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 3897	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 3898	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 3898	44570140h
800–803h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 3899	00000000h
804–807h	4	"Software Reset (RESETS)—Offset 804h" on page 3899	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 3900	55000000h
818–81Bh	4	"I2C_ACK_COUNT—Offset 818h" on page 3901	00000000h
820–823h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 3902	00000000h
824–827h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 3903	00000000h

26.7.1 I2C Control Register (IC_CON)—Offset 0h

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000007Fh

Bits	31:7	6	5	4	3	2:1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	1	1	1	1 1	1
Field	Reserved_7_31	IC_SLAVE_DISABLE	IC_RESTART_EN	IC_10BITADDR_MASTER_rd_only	IC_10BITADDR_SLAVE	SPEED	MASTER_MODE

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. 0: slave is enabled 1: slave is disabled
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE. 01: Standard Mode (0 to 100 kbit/s) 10: Fast mode (<= 400 Kbit/s) 11: High speed mode (<= 3.4 Mbit/s)

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to 1, then bit 6 should also be set to 1. 0: Master disabled 1: Master Enabled

26.7.2 I2C Target Address Register (IC_TAR)—Offset 4h

Writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
- OR
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND
- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00001055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Field
31:13	Reserved_13_31
12	IC_10BITADDR_MASTER
11	SPECIAL
10	GC_OR_START
9:0	IC_TAR

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. • 0: 7-bit addressing • 1: 10-bit addressing

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

26.7.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Reserved_10_31 (bits 31:10) | IC_SAR (bits 9:0)

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.7.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 31:3	Bits 2:0
Reserved_3_31	IC_HS_MAR

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.7.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:11	Bit 10	Bit 9	Bit 8	Bits 7:0
Reserved_11_31	RESTART	STOP	CMD	DAT

Bit Range	Default & Access	Field Name (ID): Description
31:11	0b RW	**Reserved_11_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

26.7.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000190h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 0 0 1	0 0 0 0
Reserved_16_31				IC_SS_SCL_HCNT			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.7.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 000001D6h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Reserved_16_31 (bits 31:16); IC_SS_SCL_LCNT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.7.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000003Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Reserved_16_31 (bits 31:16); IC_FS_SCL_HCNT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.7.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000082h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 1 0	

Bits 31:16	Bits 15:0
Reserved_16_31	IC_FS_SCL_LCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.7.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000000Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Reserved_16_31																IC_HS_SCL_HCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.7.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000020h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0
Field	Reserved_16_31				IC_HS_SCL_LCNT			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.7.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	R_GEN_CALL	R_START_DET	R_STOP_DET	R_ACTIVITY	R_RX_DONE	R_TX_ABRT	R_RD_REQ	R_TX_EMPTY	R_TX_OVER	R_RX_FULL	R_RX_OVER	R_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

26.7.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 000008FFh

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0	0	1	1	1	1	1	1	1	1
Field	Reserved_12_31	M_GEN_CALL	M_START_DET	M_STOP_DET	M_ACTIVITY	M_RX_DONE	M_TX_ABRT	M_RD_REQ	M_TX_EMPTY	M_TX_OVER	M_RX_FULL	M_RX_OVER	M_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

26.7.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31–12	11	10	9	8	7	6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_12_31	GEN_CALL	START_DET	STOP_DET	ACTIVITY	RX_DONE	TX_ABRT	RD_REQ	TX_EMPTY	TX_OVER	RX_FULL	RX_OVER	RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

26.7.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Reserved_8_31 (bits 31:8); RX_TL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.7.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits 31:8	Bits 7:0
Reserved_8_31	TX_TL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.7.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_INTR (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

26.7.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_RX_UNDER (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

26.7.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31

CLR_RX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

26.7.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31

CLR_TX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

26.7.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_RD_REQ

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

26.7.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_TX_ABRT

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

26.7.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_RX_DONE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

26.7.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

26.7.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_STOP_DET

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

26.7.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_START_DET

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

26.7.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_GEN_CALL

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

26.7.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_2_31 | ABORT | ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

26.7.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Reserved_7_31																									SLV_ACTIVITY	MST_ACTIVITY	RFF	RFNE	TFE	TFNF	ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

26.7.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_9_31 (bits 31:9), TXFLR (bits 8:0)

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

26.7.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_9_31 | RXFLR

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

26.7.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implementedone cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0. The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Reserved_16_31 | IC_SDA_HOLD

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

26.7.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

Bits	Default	Field
31:24	00000000	TX_FLUSH_CNT
23:17	0000000	Reserved_17_23
16	0	ABRT_USER_ABRT
15	0	ABRT_SLVRD_INTX
14	0	ABRT_SLV_ARBLOST
13	0	ABRT_SLVFLUSH_TXFIFO
12	0	ARB_LOST
11	0	ABRT_MASTER_DIS
10	0	ABRT_10B_RD_NORSTRT
9	0	ABRT_SBYTE_NORSTRT
8	0	ABRT_HS_NORSTRT
7	0	ABRT_SBYTE_ACKDET
6	0	ABRT_HS_ACKDET
5	0	ABRT_GCALL_READ
4	0	ABRT_GCALL_NOACK
3	0	ABRT_TXDATA_NOACK
2	0	ABRT_10ADDR2_NOACK
1	0	ABRT_10ADDR1_NOACK
0	0	ABRT_7B_ADDR_NOACK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

26.7.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | NACK

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

26.7.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_2_31 | TDMAE | RDMAE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

26.7.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
Reserved_8_31	DMATDL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

26.7.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_8_31																								DMARDL							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

26.7.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. **NOTE:** The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000064h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Reserved_8_31																								SDA_SETUP							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

26.7.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Reserved_1_31																															ACK_GEN_CALL

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

26.7.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:3	Bit 2	Bit 1	Bit 0
Reserved_3_31	SLV_RX_DATA_LOST	SLV_DISABLED_WHILE_BUSY	IC_EN

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

26.7.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000005h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits 31:8	Bits 7:0
Reserved_8_31	IC_FS_SPKLEN

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.7.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Reserved_8_31 (bits 31:8) | IC_HS_SPKLEN (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.7.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00FFFFEEh

Bits	Value	Field
31:24	0 0 0 0 0 0 0 0	Reserved_24_31
23:16	1 1 1 1 1 1 1 1	TX_BUFFER_DEPTH
15:8	1 1 1 1 1 1 1 1	RX_BUFFER_DEPTH
7	1	ADD_ENCODED_PARAMS
6	1	HAS_DMA
5	1	INTR_IO
4	0	HC_COUNT_VALUES
3:2	1 1	MAX_SPEED_MODE
1:0	1 0	APB_DATA_WIDTH

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

26.7.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 3131352Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0

IC_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

26.7.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 44570140h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

IC_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

26.7.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:1) | hs_source_clock (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

26.7.47 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved (bits 31:2) | reset_apb (bit 1) | reset_func (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

26.7.48 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 55000000h

Bits	31	30	29	28	27	26	25	24	23:10	9	8	7	6	5	4	3:0
Default	0	1	0	1	0	1	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0 0 0 0
Field	sda_mux_sel	sda_signal_state	scl_mux_sel	scl_signal_state	sda_rd_pre_drive	sda_rd_post_drive	scl_rd_pre_drive	scl_rd_post_drive	Reserved	i2c_fix_ctrl_1680	i2c_fix_ctrl_0770	i2c_fix_ctrl_1699	i2c_374798_fix_disable	i2c_374609_fix_disable	i2c_tx_lastbyte_flag	reserved

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

26.7.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

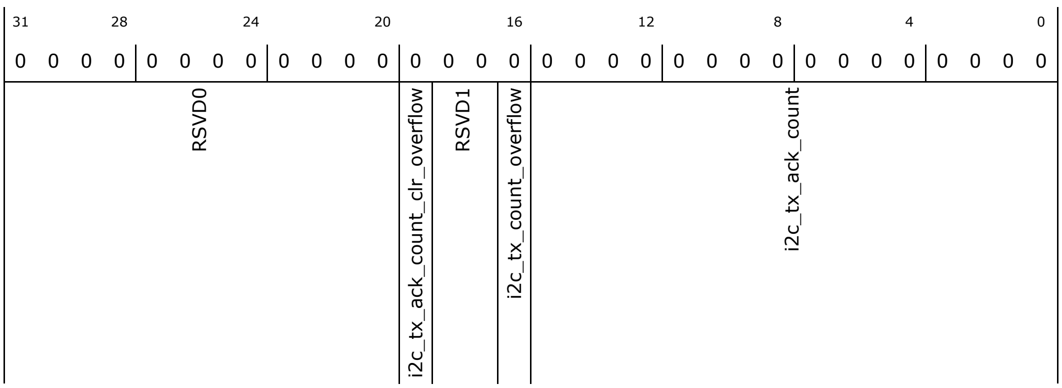
Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

26.7.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved | i2c_tx_complete_interrupt_mask | i2c_tx_completion_interrupt

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

26.7.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | i2c_tx_complete_intr_clr

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

26.8 SIO I^{2}C 1 PCI Configuration Registers

Table 266. Summary of I^{2}C 1 PCI Configuration Registers—0/24/2

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3904	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3905	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3906	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3907	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 3908	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3908	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3909	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3910	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3910	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3911	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3911	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3912	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 3913	00000000h

26.8.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 0h

Default: 00008086h

31 28 24 20 16 12 8 4 0
0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 0 0 0 | 0 0 0 0 | 1 0 0 0 | 0 1 1 0
DEVICEID VENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

26.8.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

26.8.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:2] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CLASS_CODES																								RID							

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

26.8.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + Ch

Default: 00800000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0								MULFNDEV	HEADERTYPE							LATTIMER								CACHELINE_SIZE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

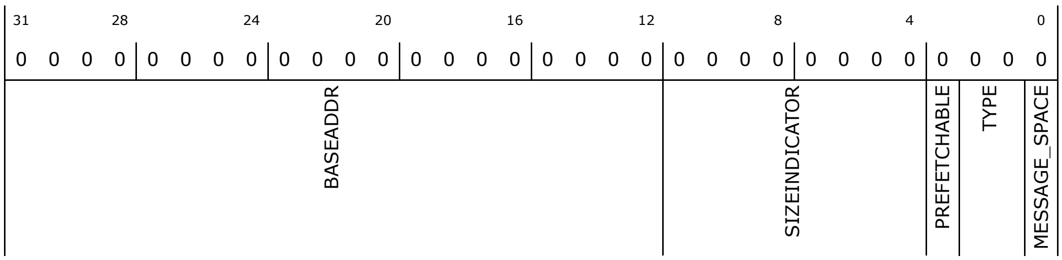
26.8.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

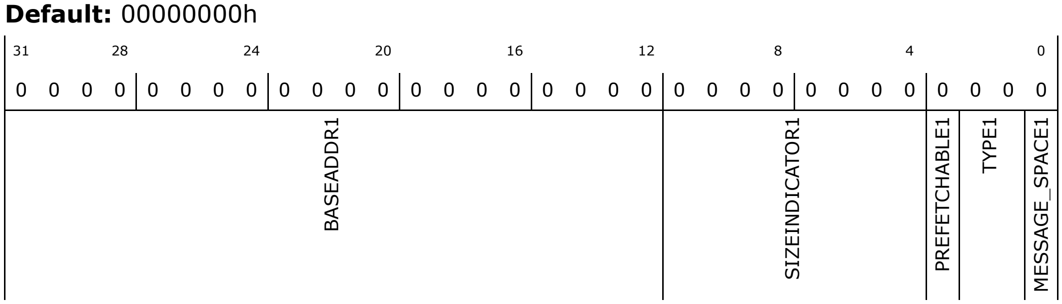
26.8.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:2] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

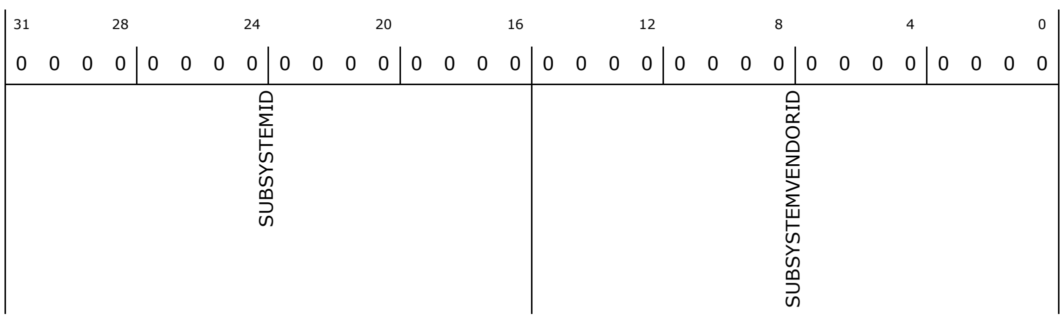
26.8.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

26.8.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:2] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

26.8.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:2] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0 | CAPPTR_POWER

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

26.8.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:2] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
MAX_LAT								MIN_GNT								Reserved0				INTPIN				INTLINE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

26.8.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:2] + 80h

Default: 00030001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PMESUPPORT					Reserved0								VERSION			NXTCAP								POWER_CAP							

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

26.8.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:2] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Reserved0																PMESTATUS	Reserved1						PMEENABLE	Reserved2				NO_SOFT_RESET	Reserved3	POWERSTATE	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

26.8.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

26.9 SIO I²C 1 PCI Configuration Registers

Table 267. Summary of I²C 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 3916	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 3917	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 3918	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 3918	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 3919	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 3920	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 3920	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 3921	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 3922	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 3922	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 3923	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 3924	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 3925	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 3926	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 3927	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 3928	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 3928	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 3929	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 3929	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 3930	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 3930	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 3931	00000000h
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 3931	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 3932	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 3932	00000000h

Table 267. Summary of I^{2}C 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 3933	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 3933	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 3934	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 3934	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 3935	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 3936	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 3937	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 3937	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 3939	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 3940	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 3940	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 3941	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 3942	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 3943	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 3943	00000000h
A0–A3h	4	"IC_FS_SPKLEN—Offset A0h" on page 3944	00000005h
A4–A7h	4	"IC_HS_SPKLEN—Offset A4h" on page 3945	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 3946	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 3947	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 3947	44570140h
800–803h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 3948	00000000h
804–807h	4	"Software Reset (RESETS)—Offset 804h" on page 3948	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 3949	55000000h
818–81Bh	4	"I2C_ACK_COUNT—Offset 818h" on page 3950	00000000h
820–823h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 3951	00000000h
824–827h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 3952	00000000h

26.9.1 I2C Control Register (IC_CON)—Offset 0h

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000007Fh

Bits	31:7	6	5	4	3	2:1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	1	1	1	1 1	1
Field	Reserved_7_31	IC_SLAVE_DISABLE	IC_RESTART_EN	IC_10BITADDR_MASTER_rd_only	IC_10BITADDR_SLAVE	SPEED	MASTER_MODE

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

26.9.2 I2C Target Address Register (IC_TAR)—Offset 4h

Writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND
- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00001055h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 1 0 1 | 0 1 0 1

Reserved_13_31 | IC_10BITADDR_MASTER | SPECIAL | GC_OR_START | IC_TAR

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

26.9.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000055h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1	0 1 0 1

Bits 31:10	Bits 9:0
Reserved_10_31	IC_SAR

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.9.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Bits 31:3	Bits 2:0
Reserved_3_31	IC_HS_MAR

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.9.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_11_31																					RESTART	STOP	CMD	DAT							

Bit Range	Default & Access	Field Name (ID): Description
31:11	0b RW	**Reserved_11_31:** Reserved.
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

26.9.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000190h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_SS_SCL_HCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.9.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 000001D6h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 1 1 0 1 | 0 1 1 0

Reserved_16_31	IC_SS_SCL_LCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.9.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000003Ch

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 1 | 1 1 0 0

Reserved_16_31	IC_FS_SCL_HCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.9.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Reserved_16_31																IC_FS_SCL_LCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.9.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000000Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Reserved_16_31 (bits 31:16) | IC_HS_SCL_HCNT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.9.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Reserved_16_31 (bits 31:16) | IC_HS_SCL_LCNT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.9.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	R_GEN_CALL	R_START_DET	R_STOP_DET	R_ACTIVITY	R_RX_DONE	R_TX_ABRT	R_RD_REQ	R_TX_EMPTY	R_TX_OVER	R_RX_FULL	R_RX_OVER	R_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

26.9.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 000008FFh

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0000 0000 0000 0000 0000	1	0	0	0	1	1	1	1	1	1	1	1
Field	Reserved_12_31	M_GEN_CALL	M_START_DET	M_STOP_DET	M_ACTIVITY	M_RX_DONE	M_TX_ABRT	M_RD_REQ	M_TX_EMPTY	M_TX_OVER	M_RX_FULL	M_RX_OVER	M_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

26.9.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	GEN_CALL	START_DET	STOP_DET	ACTIVITY	RX_DONE	TX_ABRT	RD_REQ	TX_EMPTY	TX_OVER	RX_FULL	RX_OVER	RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

26.9.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Reserved_8_31																								RX_TL							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.9.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Fields: Reserved_8_31 (bits 31:8), TX_TL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.9.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_1_31 (bits 31:1), CLR_INTR (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

26.9.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															Reserved_1_31																CLR_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

26.9.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															Reserved_1_31																CLR_RX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

26.9.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_TX_OVER (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

26.9.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_RD_REQ (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

26.9.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
Reserved_1_31	CLR_TX_ABRT

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

26.9.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
Reserved_1_31	CLR_RX_DONE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

26.9.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1_31																															CLR_ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

26.9.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1_31																															CLR_STOP_DET

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

26.9.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_START_DET

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

26.9.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_GEN_CALL

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

26.9.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_2_31 | ABORT | ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

26.9.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Reserved_7_31																									SLV_ACTIVITY	MST_ACTIVITY	RFF	RFNE	TFE	TFNF	ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

26.9.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_9_31 (bits 31:9)	TXFLR (bits 8:0)

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

26.9.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_9_31 (bits 31:9)	RXFLR (bits 8:0)

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

26.9.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implementedone cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0. The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1

Bits 31:16	Bits 15:0
Reserved_16_31	IC_SDA_HOLD

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

26.9.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same

manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

Bits	31:24	23:17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	TX_FLUSH_CNT	Reserved_17_23	ABRT_USER_ABRT	ABRT_SLVRD_INTX	ABRT_SLV_ARBLOST	ABRT_SLVFLUSH_TXFIFO	ARB_LOST	ABRT_MASTER_DIS	ABRT_10B_RD_NORSTRT	ABRT_SBYTE_NORSTRT	ABRT_HS_NORSTRT	ABRT_SBYTE_ACKDET	ABRT_HS_ACKDET	ABRT_GCALL_READ	ABRT_GCALL_NOACK	ABRT_TXDATA_NOACK	ABRT_10ADDR2_NOACK	ABRT_10ADDR1_NOACK	ABRT_7B_ADDR_NOACK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

26.9.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1), NACK (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

26.9.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_2_31																														TDMAE	RDMAE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

26.9.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_8_31 | DMATDL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

26.9.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_8_31 | DMARDL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

26.9.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. **NOTE:** The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000064h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Reserved_8_31																								SDA_SETUP							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

26.9.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 31:1: Reserved_1_31; Bit 0: ACK_GEN_CALL

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

26.9.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3	2	1	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0
Reserved_3_31								SLV_RX_DATA_LOST	SLV_DISABLED_WHILE_BUSY	IC_EN

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

26.9.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000005h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1
Reserved_8_31						IC_FS_SPKLEN	

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.9.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Reserved_8_31 | IC_HS_SPKLEN

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.9.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00FFFFEEh

Bits	31:24	23:16	15:8	7	6	5	4	3:2	1:0
Value	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1	1	1	0	1 1	1 0
Field	Reserved_24_31	TX_BUFFER_DEPTH	RX_BUFFER_DEPTH	ADD_ENCODED_PARAMS	HAS_DMA	INTR_IO	HC_COUNT_VALUES	MAX_SPEED_MODE	APB_DATA_WIDTH

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

26.9.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 3131352Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0

IC_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

26.9.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 44570140h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

IC_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

26.9.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD0 | hs_source_clock

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

26.9.47 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

reserved | reset_apb | reset_func

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

26.9.48 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 55000000h

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sda_mux_sel	sda_signal_state	scl_mux_sel	scl_signal_state	sda_rd_pre_drive	sda_rd_post_drive	scl_rd_pre_drive	scl_rd_post_drive	Reserved														i2c_fix_ctrl_1680	i2c_fix_ctrl_0770	i2c_fix_ctrl_1699	i2c_374798_fix_disable	i2c_374609_fix_disable	i2c_tx_lastbyte_flag	reserved			

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

26.9.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

RSVD0	i2c_tx_ack_count_clr_overflow	RSVD1	i2c_tx_count_overflow	i2c_tx_ack_count

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

26.9.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved																														i2c_tx_complete_interrupt_mask	i2c_tx_completion_interrupt

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

26.9.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:1)

i2c_tx_complete_intr_clr (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

26.10 SIO I²C 2 PCI Configuration Registers

Table 268. Summary of I²C 2 PCI Configuration Registers—0/24/3

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3953	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 3954	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3955	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3955	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 3956	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 3957	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3958	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3959	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3959	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3960	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3960	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3961	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 3962	00000000h

26.10.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
							DEVICEID																VENDORID								

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

26.10.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

26.10.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 8h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

31:8	7:0
CLASS_CODES	RID

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

26.10.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + Ch

Default: 00800000h

Field	Bits	Default
Reserved0	31:24	0 0 0 0 0 0 0 0
MULFNDEV	23	1
HEADERTYPE	22:16	0 0 0 0 0 0 0
LATTIMER	15:8	0 0 0 0 0 0 0 0
CACHELINE_SIZE	7:0	0 0 0 0 0 0 0 0

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

26.10.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:3] + 10h

Default: 00000000h

Field	Bits	Default
BASEADDR	31:12	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SIZEINDICATOR	11:4	0 0 0 0 0 0 0 0
PREFETCHABLE	3	0
TYPE	2:1	0 0
MESSAGE_SPACE	0	0

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

26.10.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:4	Bit 3	Bits 2:1	Bit 0
BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

26.10.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

26.10.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 30h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

26.10.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 34h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved0 | CAPPTR_POWER

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

26.10.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 3Ch

Default: 00000100h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0

31:24	23:16	15:12	11:8	7:0
MAX_LAT	MIN_GNT	Reserved0	INTPIN	INTLINE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

26.10.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 80h

Default: 00030001h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

31:27	26:19	18:16	15:8	7:0
PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

26.10.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 84h

Default: 00000008h

Bits	31:16	15	14:9	8	7:4	3	2	1:0
Value	0000 0000 0000 0000	0	000 000	0	0000	1	0	00
Field	Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

26.10.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:3] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

26.11 SIO I^2C 2 Memory Mapped I/O Registers

Table 269. Summary of I^2C 2 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 3965	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 3966	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 3967	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 3967	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 3968	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 3969	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 3969	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 3970	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 3971	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 3971	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 3972	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 3973	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 3974	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 3975	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 3976	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 3977	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 3977	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 3978	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 3978	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 3979	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 3979	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 3980	00000000h
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 3980	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 3981	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 3981	00000000h

Table 269. Summary of I^{2}C 2 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64–67h	4	“Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h” on page 3982	00000000h
68–6Bh	4	“Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h” on page 3982	00000000h
6C–6Fh	4	“I2C Enable Register (IC_ENABLE)—Offset 6Ch” on page 3983	00000000h
70–73h	4	“I2C Status Register (IC_STATUS)—Offset 70h” on page 3983	00000006h
74–77h	4	“I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h” on page 3984	00000000h
78–7Bh	4	“I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h” on page 3985	00000000h
7C–7Fh	4	“I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch” on page 3986	00000001h
80–83h	4	“I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h” on page 3986	00000000h
84–87h	4	“Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h” on page 3988	00000000h
88–8Bh	4	“DMA Control Register (IC_DMA_CR)—Offset 88h” on page 3989	00000000h
8C–8Fh	4	“DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch” on page 3989	00000000h
90–93h	4	“I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h” on page 3990	00000000h
94–97h	4	“I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h” on page 3991	00000064h
98–9Bh	4	“I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h” on page 3992	00000001h
9C–9Fh	4	“I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch” on page 3992	00000000h
A0–A3h	4	“IC_FS_SPKLEN—Offset A0h” on page 3993	00000005h
A4–A7h	4	“IC_HS_SPKLEN—Offset A4h” on page 3994	00000002h
F4–F7h	4	“Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h” on page 3995	00FFFFEEh
F8–FBh	4	“I2C Component Version Register (IC_COMP_VERSION)—Offset F8h” on page 3996	3131352Ah
FC–FFh	4	“I2C Component Type Register (IC_COMP_TYPE)—Offset FCh” on page 3996	44570140h
800–803h	4	“reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h” on page 3997	00000000h
804–807h	4	“Software Reset (RESETS)—Offset 804h” on page 3997	00000000h
808–80Bh	4	“General Purpose Register (GENERAL)—Offset 808h” on page 3998	55000000h
818–81Bh	4	“I2C_ACK_COUNT—Offset 818h” on page 3999	00000000h
820–823h	4	“I2C_TX_COMPLETE_INTR_STAT—Offset 820h” on page 4000	00000000h
824–827h	4	“reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h” on page 4001	00000000h

26.11.1 I2C Control Register (IC_CON)—Offset 0h

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000007Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
												Reserved_7_31													IC_SLAVE_DISABLE	IC_RESTART_EN	IC_10BITADDR_MASTER_rd_only	IC_10BITADDR_SLAVE	SPEED		MASTER_MODE

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

26.11.2 I2C Target Address Register (IC_TAR)—Offset 4h

Writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND
- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00001055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1

Bits 31:13	Bit 12	Bit 11	Bit 10	Bits 9:0
Reserved_13_31	IC_10BITADDR_MASTER	SPECIAL	GC_OR_START	IC_TAR

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

26.11.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Fields: Reserved_10_31 (bits 31:10), IC_SAR (bits 9:0)

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.11.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: Reserved_3_31 (bits 31:3), IC_HS_MAR (bits 2:0)

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.11.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:11	Bit 10	Bit 9	Bit 8	Bits 7:0
Reserved_11_31	RESTART	STOP	CMD	DAT

Bit Range	Default & Access	Field Name (ID): Description
31:11	0b RW	**Reserved_11_31:** Reserved.
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

26.11.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000190h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0
Reserved_16_31																IC_SS_SCL_HCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.11.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 000001D6h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Reserved_16_31 (bits 31:16) | IC_SS_SCL_LCNT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.11.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000003Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Reserved_16_31 (bits 31:16) | IC_FS_SCL_HCNT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.11.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Reserved_16_31 (bits 31:16); IC_FS_SCL_LCNT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.11.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000000Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Reserved_16_31																IC_HS_SCL_HCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.11.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Reserved_16_31																IC_HS_SCL_LCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.11.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

Bit	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	R_GEN_CALL	R_START_DET	R_STOP_DET	R_ACTIVITY	R_RX_DONE	R_TX_ABRT	R_RD_REQ	R_TX_EMPTY	R_TX_OVER	R_RX_FULL	R_RX_OVER	R_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

26.11.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 000008FFh

Bit	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0	0	1	1	1	1	1	1	1	1
Field	Reserved_12_31	M_GEN_CALL	M_START_DET	M_STOP_DET	M_ACTIVITY	M_RX_DONE	M_TX_ABRT	M_RD_REQ	M_TX_EMPTY	M_TX_OVER	M_RX_FULL	M_RX_OVER	M_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

26.11.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31–12	11	10	9	8	7	6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_12_31	GEN_CALL	START_DET	STOP_DET	ACTIVITY	RX_DONE	TX_ABRT	RD_REQ	TX_EMPTY	TX_OVER	RX_FULL	RX_OVER	RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

26.11.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000010h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0
Reserved_8_31						RX_TL	

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.11.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000010h

Bit	31:8	7:0
Value	0000 0000 0000 0000 0000 0000	0001 0000
Field	Reserved_8_31	TX_TL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.11.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

Bit	31:1	0
Value	0000 0000 0000 0000 0000 0000 0000 000	0
Field	Reserved_1_31	CLR_INTR

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

26.11.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

26.11.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_RX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

26.11.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1)
CLR_TX_OVER (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

26.11.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1)
CLR_RD_REQ (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

26.11.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_TX_ABRT (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

26.11.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_RX_DONE (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

26.11.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_1_31 (bits 31:1), CLR_ACTIVITY (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

26.11.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_1_31 (bits 31:1), CLR_STOP_DET (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

26.11.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1), CLR_START_DET (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

26.11.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1), CLR_GEN_CALL (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

26.11.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_2_31 (31:2), ABORT (1), ENABLE (0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

26.11.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Reserved_7_31																									SLV_ACTIVITY	MST_ACTIVITY	RFF	RFNE	TFE	TFNF	ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

26.11.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_9_31																							TXFLR								

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

26.11.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_9_31																							RXFLR								

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

26.11.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implementedone cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0. The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Reserved_16_31																IC_SDA_HOLD															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

26.11.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same

manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields (bit 31 to 0): TX_FLUSH_CNT, Reserved_17_23, ABRT_USER_ABRT, ABRT_SLVRD_INTX, ABRT_SLV_ARBLOST, ABRT_SLVFLUSH_TXFIFO, ARB_LOST, ABRT_MASTER_DIS, ABRT_10B_RD_NORSTRT, ABRT_SBYTE_NORSTRT, ABRT_HS_NORSTRT, ABRT_SBYTE_ACKDET, ABRT_HS_ACKDET, ABRT_GCALL_READ, ABRT_GCALL_NOACK, ABRT_TXDATA_NOACK, ABRT_10ADDR2_NOACK, ABRT_10ADDR1_NOACK, ABRT_7B_ADDR_NOACK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

26.11.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															Reserved_1_31																NACK

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

26.11.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0
0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_2_31 | TDMAE | RDMAE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

26.11.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31 28 24 20 16 12 8	4 0
0000 0000 0000 0000 0000 0000	0000 0000
Reserved_8_31	DMATDL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

26.11.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31 28 24 20 16 12 8	4 0
0000 0000 0000 0000 0000 0000	0000 0000
Reserved_8_31	DMARDL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

26.11.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. **NOTE:** The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000064h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits 31:8	Bits 7:0
Reserved_8_31	SDA_SETUP

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

26.11.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: Reserved_1_31 (bits 31:1), ACK_GEN_CALL (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

26.11.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_3_31 (bits 31:3), SLV_RX_DATA_LOST (bit 2), SLV_DISABLED_WHILE_BUSY (bit 1), IC_EN (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

26.11.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000005h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Fields: Reserved_8_31 (bits 31:8), IC_FS_SPKLEN (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.11.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Fields: Reserved_8_31 (bits 31:8), IC_HS_SPKLEN (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.11.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00FFFFEEh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
Reserved_24_31								TX_BUFFER_DEPTH								RX_BUFFER_DEPTH								ADD_ENCODED_PARAMS	HAS_DMA	INTR_IO	HC_COUNT_VALUES	MAX_SPEED_MODE		APB_DATA_WIDTH	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

26.11.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 3131352Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0

IC_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

26.11.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 44570140h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

IC_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

26.11.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD0 | hs_source_clock

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

26.11.47 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

reserved | reset_apb | reset_func

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

26.11.48 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 55000000h

Bits	31	30	29	28	27	26	25	24	23:10	9	8	7	6	5	4	3:0
Default	0	1	0	1	0	1	0	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0 0 0 0
Field	sda_mux_sel	sda_signal_state	scl_mux_sel	scl_signal_state	sda_rd_pre_drive	sda_rd_post_drive	scl_rd_pre_drive	scl_rd_post_drive	Reserved	i2c_fix_ctrl_1680	i2c_fix_ctrl_0770	i2c_fix_ctrl_1699	i2c_374798_fix_disable	i2c_374609_fix_disable	i2c_tx_lastbyte_flag	reserved

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

26.11.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

Bits	31:20	19	18:17	16	15:0
Default	0000 0000 0000	0	0 0	0	0000 0000 0000 0000
Field	RSVD0	i2c_tx_ack_count_clr_overflow	RSVD1	i2c_tx_count_overflow	i2c_tx_ack_count

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

26.11.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved																														i2c_tx_complete_interrupt_mask	i2c_tx_completion_interrupt

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

26.11.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

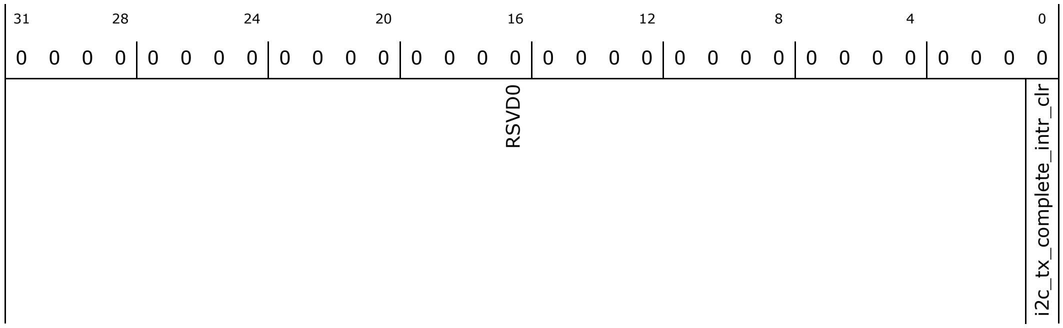
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

26.12 SIO I²C 3 PCI Configuration Registers

Table 270. Summary of I²C 3 PCI Configuration Registers—0/24/4

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4002	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 4003	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4004	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4004	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 4005	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 4006	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4006	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4007	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4008	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4008	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4009	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4010	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 4011	00000000h

26.12.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

26.12.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:4] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

26.12.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:4] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLASS_CODES	RID

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

26.12.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:4] + Ch

Default: 00800000h

Bits	31:24	23	22:16	15:8	7:0
Default	0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

26.12.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:4] + 10h

Default: 00000000h

Bits	31:12	11:4	3	2:1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0
Field	BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

26.12.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 14h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

26.12.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 2Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
SUBSYSTEMID				SUBSYSTEMVENDORID				

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

26.12.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 30h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
EXPANSION_ROM_BASE								

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

26.12.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:4] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved0 (31:8), CAPPTR_POWER (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

26.12.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:4] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fields: MAX_LAT (31:24), MIN_GNT (23:16), Reserved0 (15:12), INTPIN (11:8), INTLINE (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

26.12.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 80h

Default: 00030001h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP
31:27	26:19	18:16	15:8	7:0

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

26.12.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:4] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	31:16	15	14:9	8	7:4	3	2	1:0
Field	Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

26.12.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

26.13 SIO I^{2}C 3 Memory Mapped I/O Registers

Table 271. Summary of I^{2}C 3 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4014	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4015	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4016	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4016	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4017	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4018	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 4018	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4019	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4020	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4020	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4021	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4022	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4023	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4024	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4025	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4026	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4026	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4027	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4027	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4028	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4028	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4029	00000000h
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4029	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4030	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4030	00000000h

Table 271. Summary of I^{2}C 3 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4031	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4031	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4032	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4032	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4033	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4034	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4035	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4035	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4037	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4038	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4038	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4039	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4040	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4040	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4041	00000000h
A0–A3h	4	"IC_FS_SPKLEN—Offset A0h" on page 4042	00000005h
A4–A7h	4	"IC_HS_SPKLEN—Offset A4h" on page 4043	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4044	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4045	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4045	44570140h
800–803h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 4046	00000000h
804–807h	4	"Software Reset (RESETS)—Offset 804h" on page 4046	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 4047	55000000h
818–81Bh	4	"I2C_ACK_COUNT—Offset 818h" on page 4048	00000000h
820–823h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 4049	00000000h
824–827h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4050	00000000h

26.13.1 I2C Control Register (IC_CON)—Offset 0h

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000007Fh

31:7	6	5	4	3	2:1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	1	1	1	1 1	1
Reserved_7_31	IC_SLAVE_DISABLE	IC_RESTART_EN	IC_10BITADDR_MASTER_rd_only	IC_10BITADDR_SLAVE	SPEED	MASTER_MODE

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

26.13.2 I2C Target Address Register (IC_TAR)—Offset 4h

Writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND
- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00001055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1

Fields: Reserved_13_31 (31:13), IC_10BITADDR_MASTER (12), SPECIAL (11), GC_OR_START (10), IC_TAR (9:0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

26.13.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Reserved_10_31 | IC_SAR

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.13.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Reserved_3_31 | IC_HS_MAR

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.13.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

Bits	31:11	10	9	8	7:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0 0 0 0 0 0 0 0
Field	Reserved_11_31	RESTART	STOP	CMD	DAT

Bit Range	Default & Access	Field Name (ID): Description
31:11	0b RW	**Reserved_11_31:** Reserved.
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

26.13.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000190h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Reserved_16_31 (bits 31:16); IC_SS_SCL_HCNT (bits 15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.13.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 000001D6h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0
Reserved_16_31																IC_SS_SCL_LCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.13.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000003Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Reserved_16_31																IC_FS_SCL_HCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.13.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_FS_SCL_LCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.13.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000000Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Reserved_16_31	IC_HS_SCL_HCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.13.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Reserved_16_31	IC_HS_SCL_LCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.13.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_12_31																				R_GEN_CALL	R_START_DET	R_STOP_DET	R_ACTIVITY	R_RX_DONE	R_TX_ABRT	R_RD_REQ	R_TX_EMPTY	R_TX_OVER	R_RX_FULL	R_RX_OVER	R_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

26.13.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 000008FFh

31:12	11	10	9	8	7	6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0	0	1	1	1	1	1	1	1	1
Reserved_12_31	M_GEN_CALL	M_START_DET	M_STOP_DET	M_ACTIVITY	M_RX_DONE	M_TX_ABRT	M_RD_REQ	M_TX_EMPTY	M_TX_OVER	M_RX_FULL	M_RX_OVER	M_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

26.13.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31:12	11	10	9	8	7	6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_12_31	GEN_CALL	START_DET	STOP_DET	ACTIVITY	RX_DONE	TX_ABRT	RD_REQ	TX_EMPTY	TX_OVER	RX_FULL	RX_OVER	RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

26.13.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits 31:8	Bits 7:0
Reserved_8_31	RX_TL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.13.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits 31:8	Bits 7:0
Reserved_8_31	TX_TL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.13.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
Reserved_1_31	CLR_INTR

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

26.13.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1_31																															CLR_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

26.13.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1_31																															CLR_RX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

26.13.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															Reserved_1_31																CLR_TX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

26.13.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
															Reserved_1_31																CLR_RD_REQ

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

26.13.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 CLR_TX_ABRT

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

26.13.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 CLR_RX_DONE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

26.13.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_1_31 (bits 31:1), CLR_ACTIVITY (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

26.13.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_1_31 (bits 31:1), CLR_STOP_DET (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

26.13.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
Reserved_1_31	CLR_START_DET

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

26.13.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
Reserved_1_31	CLR_GEN_CALL

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

26.13.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
														Reserved_2_31																ABORT	ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

26.13.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000006h

Bit	31:7	6	5	4	3	2	1	0
Default	0000 0000 0000 0000 0000 0000 0	0	0	0	0	1	1	0
Field	Reserved_7_31	SLV_ACTIVITY	MST_ACTIVITY	RFF	RFNE	TFE	TFNF	ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

26.13.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_9_31 (bits 31:9), TXFLR (bits 8:0)

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

26.13.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_9_31 (bits 31:9), RXFLR (bits 8:0)

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

26.13.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implementedone cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0. The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 31:16	Bits 15:0
Reserved_16_31	IC_SDA_HOLD

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

26.13.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same

manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

Bits	Default	Field
31:24	0000 0000	TX_FLUSH_CNT
23:17	0000 000	Reserved_17_23
16	0	ABRT_USER_ABRT
15	0	ABRT_SLVRD_INTX
14	0	ABRT_SLV_ARBLOST
13	0	ABRT_SLVFLUSH_TXFIFO
12	0	ARB_LOST
11	0	ABRT_MASTER_DIS
10	0	ABRT_10B_RD_NORSTRT
9	0	ABRT_SBYTE_NORSTRT
8	0	ABRT_HS_NORSTRT
7	0	ABRT_SBYTE_ACKDET
6	0	ABRT_HS_ACKDET
5	0	ABRT_GCALL_READ
4	0	ABRT_GCALL_NOACK
3	0	ABRT_TXDATA_NOACK
2	0	ABRT_10ADDR2_NOACK
1	0	ABRT_10ADDR1_NOACK
0	0	ABRT_7B_ADDR_NOACK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

26.13.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
Reserved_1_31	NACK

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

26.13.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_2_31	TDMAE	RDMAE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

26.13.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_8_31																								DMATDL							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

26.13.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_8_31																								DMARDL							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

26.13.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. **NOTE:** The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000064h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Reserved_8_31																								SDA_SETUP							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

26.13.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Reserved_1_31 (bits 31:1) ACK_GEN_CALL (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

26.13.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

Bit	31–3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0
Field	Reserved_3_31	SLV_RX_DATA_LOST	SLV_DISABLED_WHILE_BUSY	IC_EN

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

26.13.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000005h

Bit	31–8	7–0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 1
Field	Reserved_8_31	IC_FS_SPKLEN

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.13.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Reserved_8_31 (bits 31:8), IC_HS_SPKLEN (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.13.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00FFFFEEh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
Reserved_24_31								TX_BUFFER_DEPTH								RX_BUFFER_DEPTH								ADD_ENCODED_PARAMS	HAS_DMA	INTR_IO	HC_COUNT_VALUES	MAX_SPEED_MODE		APB_DATA_WIDTH	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

26.13.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 3131352Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0

IC_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

26.13.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 44570140h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

IC_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

26.13.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD0 (bits 31:1), hs_source_clock (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

26.13.47 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reserved (bits 31:2), reset_apb (bit 1), reset_func (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

26.13.48 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 55000000h

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sda_mux_sel	sda_signal_state	scl_mux_sel	scl_signal_state	sda_rd_pre_drive	sda_rd_post_drive	scl_rd_pre_drive	scl_rd_post_drive	Reserved														i2c_fix_ctrl_1680	i2c_fix_ctrl_0770	i2c_fix_ctrl_1699	i2c_374798_fix_disable	i2c_374609_fix_disable	i2c_tx_lastbyte_flag	reserved			

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

26.13.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | i2c_tx_ack_count_clr_overflow | RSVD1 | i2c_tx_count_overflow | i2c_tx_ack_count

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

26.13.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

Bits	31:2	1	0
Default	0000 0000 0000 0000 0000 0000 0000 00	0	0
Field	Reserved	i2c_tx_complete_interrupt_mask	i2c_tx_completion_interrupt

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

26.13.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:1	Bit 0
RSVD0	i2c_tx_complete_intr_clr

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

26.14 SIO I^2C 4 PCI Configuration Registers

Table 272. Summary of I^2C 4 PCI Configuration Registers—0/24/5

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4051	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 4052	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4053	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4054	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 4055	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 4055	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4056	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4056	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4057	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4057	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4058	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4059	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 4060	00000000h

26.14.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

26.14.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:5] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

26.14.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:5] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLASS_CODES | RID

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

26.14.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + Ch

Default: 00800000h

31 28 24		20 16	12 8	4 0
0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

26.14.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:5] + 10h

Default: 00000000h

Bits	31:12	11:4	3	2:1	0
Default	0000 0000 0000 0000 0000	0000 0000	0	00	0
Field	BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

26.14.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:5] + 14h

Default: 00000000h

Bits	31:12	11:4	3	2:1	0
Default	0000 0000 0000 0000 0000	0000 0000	0	00	0
Field	BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

26.14.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

26.14.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

26.14.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0

CAPPTR_POWER

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

26.14.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 3Ch

Default: 00000100h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 0 0 0

MAX_LAT | MIN_GNT | Reserved0 | INTPIN | INTLINE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

26.14.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 80h

Default: 00030001h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 1 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1

PMESUPPORT | Reserved0 | VERSION | NXTCAP | POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

26.14.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 84h

Default: 00000008h

31:16	15	14:9	8	7:4	3	2	1:0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0	0	0 0 0 0	1	0	0 0
Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

26.14.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

26.15 SIO I^2C 4 Memory Mapped I/O Registers

Table 273. Summary of I^2C 4 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4063	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4064	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4065	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4065	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4066	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4067	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 4067	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4068	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4069	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4069	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4070	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4071	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4072	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4073	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4074	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4075	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4075	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4076	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4076	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4077	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4077	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4078	00000000h
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4078	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4079	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4079	00000000h

Table 273. Summary of I²C 4 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4080	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4080	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4081	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4081	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4082	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4083	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4084	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4084	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4086	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4087	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4087	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4088	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4089	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4090	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4090	00000000h
A0–A3h	4	"IC_FS_SPKLEN—Offset A0h" on page 4091	00000005h
A4–A7h	4	"IC_HS_SPKLEN—Offset A4h" on page 4092	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4093	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4094	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4094	44570140h
800–803h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 4095	00000000h
804–807h	4	"Software Reset (RESETS)—Offset 804h" on page 4095	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 4096	55000000h
818–81Bh	4	"I2C_ACK_COUNT—Offset 818h" on page 4097	00000000h
820–823h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 4098	00000000h
824–827h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4099	00000000h

26.15.1 I2C Control Register (IC_CON)—Offset 0h

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000007Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
Reserved_7_31																									IC_SLAVE_DISABLE	IC_RESTART_EN	IC_10BITADDR_MASTER_rd_only	IC_10BITADDR_SLAVE	SPEED		MASTER_MODE

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

26.15.2 I2C Target Address Register (IC_TAR)—Offset 4h

Writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND
- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00001055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1
Reserved_13_31																			IC_10BITADDR_MASTER	SPECIAL	GC_OR_START	IC_TAR									

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

26.15.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Reserved_10_31 | IC_SAR

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.15.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Reserved_3_31 | IC_HS_MAR

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.15.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_11_31 | RESTART | STOP | CMD | DAT

Bit Range	Default & Access	Field Name (ID): Description
31:11	0b RW	**Reserved_11_31:** Reserved.
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

26.15.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000190h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_SS_SCL_HCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.15.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 000001D6h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_SS_SCL_LCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.15.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000003Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_FS_SCL_HCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.15.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000082h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 1 0
Field	Reserved_16_31				IC_FS_SCL_LCNT			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.15.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000000Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Reserved_16_31																IC_HS_SCL_HCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.15.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Reserved_16_31																IC_HS_SCL_LCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.15.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

Bit	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	R_GEN_CALL	R_START_DET	R_STOP_DET	R_ACTIVITY	R_RX_DONE	R_TX_ABRT	R_RD_REQ	R_TX_EMPTY	R_TX_OVER	R_RX_FULL	R_RX_OVER	R_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

26.15.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 000008FFh

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0	0	1	1	1	1	1	1	1	1
Field	Reserved_12_31	M_GEN_CALL	M_START_DET	M_STOP_DET	M_ACTIVITY	M_RX_DONE	M_TX_ABRT	M_RD_REQ	M_TX_EMPTY	M_TX_OVER	M_RX_FULL	M_RX_OVER	M_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

26.15.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0000 0000 0000 0000 0000	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	GEN_CALL	START_DET	STOP_DET	ACTIVITY	RX_DONE	TX_ABRT	RD_REQ	TX_EMPTY	TX_OVER	RX_FULL	RX_OVER	RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

26.15.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Reserved_8_31 (bits 31:8) | RX_TL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.15.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Reserved_8_31																								TX_TL							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.15.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1_31																															CLR_INTR

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

26.15.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1), CLR_RX_UNDER (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

26.15.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1), CLR_RX_OVER (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

26.15.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1); CLR_TX_OVER (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

26.15.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1); CLR_RD_REQ (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

26.15.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_TX_ABRT

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

26.15.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_RX_DONE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

26.15.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_ACTIVITY (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

26.15.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_STOP_DET (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

26.15.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1), CLR_START_DET (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

26.15.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1), CLR_GEN_CALL (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

26.15.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_2_31																														ABORT	ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

26.15.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Reserved_7_31																									SLV_ACTIVITY	MST_ACTIVITY	RFF	RFNE	TFE	TFNF	ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

26.15.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_9_31 | TXFLR

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

26.15.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_9_31 | RXFLR

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

26.15.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implementedone cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0. The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 31:16	Bits 15:0
Reserved_16_31	IC_SDA_HOLD

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

26.15.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same

manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

Bits	Default	Field
31:24	0 0 0 0 0 0 0 0	TX_FLUSH_CNT
23:17	0 0 0 0 0 0 0	Reserved_17_23
16	0	ABRT_USER_ABRT
15	0	ABRT_SLVRD_INTX
14	0	ABRT_SLV_ARBLOST
13	0	ABRT_SLVFLUSH_TXFIFO
12	0	ARB_LOST
11	0	ABRT_MASTER_DIS
10	0	ABRT_10B_RD_NORSTRT
9	0	ABRT_SBYTE_NORSTRT
8	0	ABRT_HS_NORSTRT
7	0	ABRT_SBYTE_ACKDET
6	0	ABRT_HS_ACKDET
5	0	ABRT_GCALL_READ
4	0	ABRT_GCALL_NOACK
3	0	ABRT_TXDATA_NOACK
2	0	ABRT_10ADDR2_NOACK
1	0	ABRT_10ADDR1_NOACK
0	0	ABRT_7B_ADDR_NOACK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

26.15.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | NACK (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

26.15.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_2_31																														TDMAE	RDMAE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

26.15.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_8_31 (bits 31:8), DMATDL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

26.15.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_8_31 (bits 31:8), DMARDL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

26.15.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. **NOTE:** The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000064h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Reserved_8_31																								SDA_SETUP							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

26.15.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	

Fields: Reserved_1_31 (bits 31:1), ACK_GEN_CALL (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

26.15.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_3_31																													SLV_RX_DATA_LOST	SLV_DISABLED_WHILE_BUSY	IC_EN

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

26.15.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000005h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
Reserved_8_31																								IC_FS_SPKLEN							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.15.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Reserved_8_31																								IC_HS_SPKLEN							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.15.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00FFFFEEh

Bits	31:24	23:16	15:8	7	6	5	4	3:2	1:0
Value	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1	1	1	0	1 1	1 0
Field	Reserved_24_31	TX_BUFFER_DEPTH	RX_BUFFER_DEPTH	ADD_ENCODED_PARAMS	HAS_DMA	INTR_IO	HC_COUNT_VALUES	MAX_SPEED_MODE	APB_DATA_WIDTH

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

26.15.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 3131352Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0

IC_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

26.15.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 44570140h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

IC_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

26.15.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

Bits	31:1	0
Default	0000 0000 0000 0000 0000 0000 0000 000	0
Field	RSVD0	hs_source_clock

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

26.15.47 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

Bits	31:2	1	0
Default	0000 0000 0000 0000 0000 0000 0000 00	0	0
Field	reserved	reset_apb	reset_func

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

26.15.48 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 55000000h

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sda_mux_sel	sda_signal_state	scl_mux_sel	scl_signal_state	sda_rd_pre_drive	sda_rd_post_drive	scl_rd_pre_drive	scl_rd_post_drive	Reserved														i2c_fix_ctrl_1680	i2c_fix_ctrl_0770	i2c_fix_ctrl_1699	i2c_374798_fix_disable	i2c_374609_fix_disable	i2c_tx_lastbyte_flag	reserved			

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

26.15.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

Bits	31:20	19	18:17	16	15:0
Default	0000 0000 0000	0	00	0	0000 0000 0000 0000
Field	RSVD0	i2c_tx_ack_count_clr_overflow	RSVD1	i2c_tx_count_overflow	i2c_tx_ack_count

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

26.15.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved																														i2c_tx_complete_interrupt_mask	i2c_tx_completion_interrupt

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

26.15.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:1); i2c_tx_complete_intr_clr (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

26.16 SIO I²C 5 PCI Configuration Registers

Table 274. Summary of I²C 5 PCI Configuration Registers—0/24/6

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4100	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 4101	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4102	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4103	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 4104	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 4104	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4105	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4106	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4106	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4107	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4107	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4108	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 4109	00000000h

26.16.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

26.16.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 4h

Default: 00100000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

26.16.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLASS_CODES (bits 31:8) | RID (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

26.16.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + Ch

Default: 00800000h

31:24	23	22:16	15:8	7:0
0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

26.16.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

26.16.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 14h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

26.16.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
SUBSYSTEMID	SUBSYSTEMVENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

26.16.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

26.16.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0 (bits 31:8) | CAPPTR_POWER (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

26.16.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
MAX_LAT								MIN_GNT								Reserved0				INTPIN				INTLINE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

26.16.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 80h

Default: 00030001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PMESUPPORT					Reserved0								VERSION			NXTCAP								POWER_CAP							

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

26.16.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 84h

Default: 00000008h

31 28 24 20 16	15	14 12	8	7 4	3	2	1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0 0 0	0	0 0 0 0	1	0	0 0
Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

26.16.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

26.17 SIO I^2C 5 Memory Mapped I/O Registers

Table 275. Summary of I^2C 5 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4112	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4113	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4114	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4114	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4115	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4116	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 4116	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4117	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4118	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4118	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4119	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4120	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4121	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4122	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4123	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4124	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4124	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4125	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4125	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4126	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4126	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4127	00000000h
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4127	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4128	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4128	00000000h

Table 275. Summary of I^{2}C 5 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4129	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4129	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4130	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4130	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4131	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4132	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4133	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4133	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4135	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4136	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4136	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4137	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4138	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4139	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4139	00000000h
A0–A3h	4	"IC_FS_SPKLEN—Offset A0h" on page 4140	00000005h
A4–A7h	4	"IC_HS_SPKLEN—Offset A4h" on page 4141	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4142	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4143	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4143	44570140h
800–803h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 4144	00000000h
804–807h	4	"Software Reset (RESETS)—Offset 804h" on page 4144	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 4145	55000000h
818–81Bh	4	"I2C_ACK_COUNT—Offset 818h" on page 4146	00000000h
820–823h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 4147	00000000h
824–827h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4148	00000000h

26.17.1 I2C Control Register (IC_CON)—Offset 0h

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000007Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
Reserved_7_31																									IC_SLAVE_DISABLE	IC_RESTART_EN	IC_10BITADDR_MASTER_rd_only	IC_10BITADDR_SLAVE	SPEED		MASTER_MODE

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

26.17.2 I2C Target Address Register (IC_TAR)—Offset 4h

Writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND
- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00001055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1
Reserved_13_31																			IC_10BITADDR_MASTER	SPECIAL	GC_OR_START	IC_TAR									

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

26.17.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Reserved_10_31 (bits 31:10), IC_SAR (bits 9:0)

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.17.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Reserved_3_31 (bits 31:3), IC_HS_MAR (bits 2:0)

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.17.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_11_31																					RESTART	STOP	CMD	DAT							

Bit Range	Default & Access	Field Name (ID): Description
31:11	0b RW	**Reserved_11_31:** Reserved.
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

26.17.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000190h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0
Reserved_16_31																IC_SS_SCL_HCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.17.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 000001D6h

31 · 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 1 0 1	0 1 1 0
Reserved_16_31				IC_SS_SCL_LCNT			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.17.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000003Ch

31 · 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	1 1 0 0
Reserved_16_31				IC_FS_SCL_HCNT			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.17.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_FS_SCL_LCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.17.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000000Ch

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 0 0	

Bits 31:16	Bits 15:0
Reserved_16_31	IC_HS_SCL_HCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.17.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000020h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	

Bits 31:16	Bits 15:0
Reserved_16_31	IC_HS_SCL_LCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.17.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	R_GEN_CALL	R_START_DET	R_STOP_DET	R_ACTIVITY	R_RX_DONE	R_TX_ABRT	R_RD_REQ	R_TX_EMPTY	R_TX_OVER	R_RX_FULL	R_RX_OVER	R_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

26.17.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 000008FFh

Bit	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0	0	1	1	1	1	1	1	1	1
Field	Reserved_12_31	M_GEN_CALL	M_START_DET	M_STOP_DET	M_ACTIVITY	M_RX_DONE	M_TX_ABRT	M_RD_REQ	M_TX_EMPTY	M_TX_OVER	M_RX_FULL	M_RX_OVER	M_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

26.17.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	GEN_CALL	START_DET	STOP_DET	ACTIVITY	RX_DONE	TX_ABRT	RD_REQ	TX_EMPTY	TX_OVER	RX_FULL	RX_OVER	RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

26.17.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits 31:8	Bits 7:0
Reserved_8_31	RX_TL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.17.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Fields: Reserved_8_31 (bits 31:8); TX_TL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.17.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_1_31 (bits 31:1); CLR_INTR (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

26.17.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

26.17.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_RX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

26.17.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Bits 31:1	Bit 0
Reserved_1_31	CLR_TX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

26.17.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Bits 31:1	Bit 0
Reserved_1_31	CLR_RD_REQ

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

26.17.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 CLR_TX_ABRT

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

26.17.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 CLR_RX_DONE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

26.17.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1_31																															CLR_ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

26.17.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_1_31																															CLR_STOP_DET

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

26.17.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1); CLR_START_DET (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

26.17.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1); CLR_GEN_CALL (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

26.17.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_2_31 | ABORT | ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

26.17.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Reserved_7_31																									SLV_ACTIVITY	MST_ACTIVITY	RFF	RFNE	TFE	TFNF	ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

26.17.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_9_31 (bits 31:9), TXFLR (bits 8:0)

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

26.17.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_9_31 (bits 31:9), RXFLR (bits 8:0)

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

26.17.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implementedone cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0. The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Reserved_16_31																IC_SDA_HOLD															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

26.17.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same

manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TX_FLUSH_CNT								Reserved_17_23							ABRT_USER_ABRT	ABRT_SLVRD_INTX	ABRT_SLV_ARBLOST	ABRT_SLVFLUSH_TXFIFO	ARB_LOST	ABRT_MASTER_DIS	ABRT_10B_RD_NORSTRT	ABRT_SBYTE_NORSTRT	ABRT_HS_NORSTRT	ABRT_SBYTE_ACKDET	ABRT_HS_ACKDET	ABRT_GCALL_READ	ABRT_GCALL_NOACK	ABRT_TXDATA_NOACK	ABRT_10ADDR2_NOACK	ABRT_10ADDR1_NOACK	ABRT_7B_ADDR_NOACK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

26.17.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

Bits	31:1	0
Default	0000000000000000000000000000000	0
Field	Reserved_1_31	NACK

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

26.17.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

Bits	31:2	1	0
Default	0000 0000 0000 0000 0000 0000 0000 00	0	0
Field	Reserved_2_31	TDMAE	RDMAE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

26.17.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_8_31 | DMATDL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

26.17.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_8_31 | DMARDL

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

26.17.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. **NOTE:** The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000064h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Reserved_8_31																								SDA_SETUP							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

26.17.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fields: Reserved_1_31 (bits 31:1), ACK_GEN_CALL (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

26.17.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:3	Bit 2	Bit 1	Bit 0
Reserved_3_31	SLV_RX_DATA_LOST	SLV_DISABLED_WHILE_BUSY	IC_EN

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

26.17.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000005h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits 31:8	Bits 7:0
Reserved_8_31	IC_FS_SPKLEN

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.17.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Reserved_8_31																								IC_HS_SPKLEN								

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.17.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00FFFFEEh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
Reserved_24_31								TX_BUFFER_DEPTH								RX_BUFFER_DEPTH								ADD_ENCODED_PARAMS	HAS_DMA	INTR_IO	HC_COUNT_VALUES	MAX_SPEED_MODE		APB_DATA_WIDTH	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

26.17.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 3131352Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0

IC_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

26.17.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 44570140h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

IC_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

26.17.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:1), hs_source_clock (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

26.17.47 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved (bits 31:2), reset_apb (bit 1), reset_func (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

26.17.48 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 55000000h

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sda_mux_sel	sda_signal_state	scl_mux_sel	scl_signal_state	sda_rd_pre_drive	sda_rd_post_drive	scl_rd_pre_drive	scl_rd_post_drive	Reserved														i2c_fix_ctrl_1680	i2c_fix_ctrl_0770	i2c_fix_ctrl_1699	i2c_374798_fix_disable	i2c_374609_fix_disable	i2c_tx_lastbyte_flag	reserved			

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

26.17.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0	i2c_tx_ack_count_clr_overflow	RSVD1	i2c_tx_count_overflow	i2c_tx_ack_count

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

26.17.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved																														i2c_tx_complete_interrupt_mask	i2c_tx_completion_interrupt

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

26.17.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:1); i2c_tx_complete_intr_clr (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

26.18 SIO I^2C 6 PCI Configuration Registers

Table 276. Summary of I^2C 6 PCI Configuration Registers—0/24/7

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4149	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 4150	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4151	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4151	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 4152	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 4153	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4153	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4154	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4155	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4155	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4156	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4157	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 4158	00000000h

26.18.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 0h

Default: 00008086h

31	28	24	20	16	12	8	4
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 1 1 0
DEVICEID				VENDORID			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

26.18.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 4h

Default: 00100000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

31	30	29	28	27	26:21	20	19	18:16	15:11	10	9	8	7:3	2	1	0
Reserved0	SSE	RMA	RTA	STA	Reserved1	CAPLIST	INTR_STATUS	Reserved2	Reserved3	INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5	BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

26.18.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:8	7:0
CLASS_CODES	RID

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

26.18.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + Ch

Default: 00800000h

31:24	23	22:16	15:8	7:0
0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

26.18.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)   **Offset:** [B:0, D:24, F:7] + 10h

Default: 00000000h

31:12	11:4	3	2:1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0
BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

26.18.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 14h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

26.18.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SUBSYSTEMID																SUBSYSTEMVENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

26.18.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
EXPANSION_ROM_BASE																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

26.18.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0	CAPPTR_POWER

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

26.18.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

MAX_LAT	MIN_GNT	Reserved0	INTPIN	INTLINE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

26.18.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**Offset:** [B:0, D:24, F:7] + 80h

Default: 00030001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

26.18.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:24, F:7] + 84h

Default: 00000008h

Bits	31:16	15	14:9	8	7:4	3	2	1:0
Default	0000 0000 0000 0000	0	000000	0	0000	1	0	00
Field	Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

26.18.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:24, F:7] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

26.19 SIO I²C 6 Memory Mapped I/O Registers

Table 277. Summary of I²C 6 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4161	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4162	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4163	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4163	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4164	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4165	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h" on page 4165	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4166	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4167	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4167	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4168	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4169	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4170	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4171	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4172	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4173	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4173	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4174	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4174	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4175	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4175	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4176	00000000h
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4176	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4177	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4177	00000000h

Table 277. Summary of I²C 6 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4178	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4178	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4179	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4179	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4180	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4181	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4182	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4182	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4184	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4185	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4185	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4186	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4187	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4188	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4188	00000000h
A0–A3h	4	"IC_FS_SPKLEN—Offset A0h" on page 4189	00000005h
A4–A7h	4	"IC_HS_SPKLEN—Offset A4h" on page 4190	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4191	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4192	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4192	44570140h
800–803h	4	"reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h" on page 4193	00000000h
804–807h	4	"Software Reset (RESETS)—Offset 804h" on page 4193	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 4194	55000000h
818–81Bh	4	"I2C_ACK_COUNT—Offset 818h" on page 4195	00000000h
820–823h	4	"I2C_TX_COMPLETE_INTR_STAT—Offset 820h" on page 4196	00000000h
824–827h	4	"reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4197	00000000h

26.19.1 I2C Control Register (IC_CON)—Offset 0h

This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000007Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Fields (bit 31 to bit 0): Reserved_7_31, IC_SLAVE_DISABLE, IC_RESTART_EN, IC_10BITADDR_MASTER_rd_only, IC_10BITADDR_SLAVE, SPEED, MASTER_MODE

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	1h RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	1h RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register.
3	1h RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.
2:1	3h RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	1h RW	**MASTER MODE (MASTER_MODE):** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

26.19.2 I2C Target Address Register (IC_TAR)—Offset 4h

Writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE is set to 0)
-
- OR
-
- DW_apb_i2c is enabled (IC_ENABLE=1)
- AND
- DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0)
- AND
- DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1)
- AND
- There are NO entries in the TX FIFO (IC_STATUS[2]=1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00001055h

Bits 31, 28, 24, 20, 16, 12, 8, 4, 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 1 0 1 | 0 1 0 1

Fields: Reserved_13_31 (31:13), IC_10BITADDR_MASTER (12), SPECIAL (11), GC_OR_START (10), IC_TAR (9:0)

Bit Range	Default & Access	Field Name (ID): Description
31:13	0b RW	**Reserved_13_31:** Reserved.
12	1h RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master.
11	0h RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. • 0 = ignore bit 10 GC_OR_START and use IC_TAR normally • 1 = perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.
9:0	55h RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

26.19.3 I2C Slave Address Register (IC_SAR)—Offset 8h

The IC SAR Address Register holds the slave address when the I2C is operating as a slave.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000055h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Reserved_10_31 | IC_SAR

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RW	**Reserved_10_31:** Reserved.
9:0	55h RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.19.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

Note: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Reserved_3_31 | IC_HS_MAR

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2:0	1h RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.19.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

This is the register written to by the CPU when filling the TX FIFO, and read from by the CPU when retrieving bytes from RX FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

Bits	31:11	10	9	8	7:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0 0 0 0 0 0 0 0
Field	Reserved_11_31	RESTART	STOP	CMD	DAT

Bit Range	Default & Access	Field Name (ID): Description
31:11	0b RW	**Reserved_11_31:** Reserved.
10	0h RW	**RESTART:** This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1. 1 If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. 0 If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	0h RW	**STOP:** This bit determines whether STOP is generated after a data byte is sent or received.
8	0h RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It only controls the direction when it acts as a master. • 1 = Read • 0 = Write

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. When you read this register, however, these bits return the value of data received on the DW_apb_i2c interface.

26.19.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000190h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_SS_SCL_HCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	190h RW	**Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.19.7 Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT)—Offset 18h

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 000001D6h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_SS_SCL_LCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	01d6h RW	**Standard Speed I2C Clock SCL Low Count Register (IC_SS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.19.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000003Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits 31:16	Bits 15:0
Reserved_16_31	IC_FS_SCL_HCNT

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	003ch RW	**Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.19.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000082h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Reserved_16_31																IC_FS_SCL_LCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0082h RW	**Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.19.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and, if attempted, results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000000Ch

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Reserved_16_31																IC_HS_SCL_HCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	000ch RW	**High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.19.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

This register must be set before any I2C bus transaction can take place, to ensure proper I/O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only if IC_MAX_SPEED_MODE!= high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and, if attempted, results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte can be programmed.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Reserved_16_31																IC_HS_SCL_LCNT															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved.
15:0	0020h RW	**High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT):** This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

26.19.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

Bits	31:12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
Field	Reserved_12_31	R_GEN_CALL	R_START_DET	R_STOP_DET	R_ACTIVITY	R_RX_DONE	R_TX_ABRT	R_RD_REQ	R_TX_EMPTY	R_TX_OVER	R_RX_FULL	R_RX_OVER	R_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**R_GEN_CALL:** Set only when a General Call address is received and acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.
10	0h RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0h RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface, regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0h RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0h RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0h RO	**R_TX_ABRT:** This bit indicates whether DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0h RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0h RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH, and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0h RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0h RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

26.19.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits. This register is active low.

- 0 masks the interrupt
- 1 unmasks the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 000008FFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1
Reserved_12_31																				M_GEN_CALL	M_START_DET	M_STOP_DET	M_ACTIVITY	M_RX_DONE	M_TX_ABRT	M_RD_REQ	M_TX_EMPTY	M_TX_OVER	M_RX_FULL	M_RX_OVER	M_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	1h RW	**M_GEN_CALL:** See description of M_TX_EMPTY bit field.
10	0h RW	**M_START_DET:** See description of M_TX_EMPTY bit field.
9	0h RW	**M_STOP_DET:** See description of M_TX_EMPTY bit field.
8	0h RW	**M_ACTIVITY:** See description of M_TX_EMPTY bit field.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**M_RX_DONE:** See description of M_TX_EMPTY bit field.
6	1h RW	**M_TX_ABRT:** See description of M_TX_EMPTY bit field.
5	1h RW	**M_RD_REQ:** See description of M_TX_EMPTY bit field.
4	1h RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register. **Reset value:** 12h8ff
3	1h RW	**M_TX_OVER:** See description of M_TX_EMPTY bit field.
2	1h RW	**M_RX_FULL:** See description of M_TX_EMPTY bit field.
1	1h RW	**M_RX_OVER:** See description of M_TX_EMPTY bit field.
0	1h RW	**M_RX_UNDER:** See description of M_TX_EMPTY bit field.

26.19.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked -- so they always show the true status of the DW_apb_i2c.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_12_31	GEN_CALL	START_DET	STOP_DET	ACTIVITY	RX_DONE	TX_ABRT	RD_REQ	TX_EMPTY	TX_OVER	RX_FULL	RX_OVER	RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:12	0b RW	**Reserved_12_31:** Reserved.
11	0h RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT.
10	0h RO	**START_DET:** Same as in reg_IC_INTR_STAT.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**STOP_DET:** Same as in reg_IC_INTR_STAT.
8	0h RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT.
7	0h RO	**RX_DONE:** Same as in reg_IC_INTR_STAT.
6	0h RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT.
5	0h RO	**RD_REQ:** Same as in reg_IC_INTR_STAT.
4	0h RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT.
3	0h RO	**TX_OVER:** Same as in reg_IC_INTR_STAT.
2	0h RO	**RX_FULL:** Same as in reg_IC_INTR_STAT.
1	0h RO	**RX_OVER:** Same as in reg_IC_INTR_STAT.
0	0h RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT.

26.19.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000010h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Reserved_8_31 (bits 31:8) | RX_TL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Receive FIFO Threshold Level (RX_TL):** The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.19.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000010h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	

Reserved_8_31	TX_TL
31:8	7:0

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	10h RW	**Transmit FIFO Threshold Level (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

26.19.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Reserved_1_31	CLR_INTR
31:1	0

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

26.19.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_RX_UNDER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

26.19.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_RX_OVER

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

26.19.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_TX_OVER (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

26.19.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | CLR_RD_REQ (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

26.19.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_TX_ABRT

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

26.19.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_1_31 | CLR_RX_DONE

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

26.19.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

26.19.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_STOP_DET

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

26.19.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_START_DET

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

26.19.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 | CLR_GEN_CALL

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	0h RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

26.19.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

Bits	31:2	1	0
Default	0000 0000 0000 0000 0000 0000 0000 00	0	0
Field	Reserved_2_31	ABORT	ENABLE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved
1	0h WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0h RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. • 0 = Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) • 1 = Enables DW_apb_i2c

26.19.29 I2C Status Register (IC_STATUS)—Offset 70h

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. The following occurs when the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Reserved_7_31																									SLV_ACTIVITY	MST_ACTIVITY	RFF	RFNE	TFE	TFNF	ACTIVITY

Bit Range	Default & Access	Field Name (ID): Description
31:7	0b RW	**Reserved_7_31:** Reserved.
6	0h RO	**Slave FSM Activity Status (SLV_ACTIVITY):** When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0h RO	**Master FSM Activity Status (MST_ACTIVITY):** When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0h RO	**ACTIVITY:** I2C Activity Status

26.19.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort -- that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_9_31																							TXFLR								

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

26.19.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

This register contains the number of valid data entries in the receive FIFO buffer. The register is cleared by the following methods:

- The I2C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved_9_31																							RXFLR								

Bit Range	Default & Access	Field Name (ID): Description
31:9	0b RW	**Reserved_9_31:** Reserved
8:0	0h RO	**Receive FIFO Level (RXFLR):** Contains the number of valid data entries in the receive FIFO.

26.19.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of ic_clk period. The value programmed must be greater than the minimum hold time in each mode for the value to be implementedone cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when IC_ENABLE=0. The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000001h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1
Reserved_16_31				IC_SDA_HOLD			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0b RW	**Reserved_16_31:** Reserved
15:0	1h RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

26.19.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same

manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TX_FLUSH_CNT								Reserved_17_23							ABRT_USER_ABRT	ABRT_SLVRD_INTX	ABRT_SLV_ARBLOST	ABRT_SLVFLUSH_TXFIFO	ARB_LOST	ABRT_MASTER_DIS	ABRT_10B_RD_NORSTRT	ABRT_SBYTE_NORSTRT	ABRT_HS_NORSTRT	ABRT_SBYTE_ACKDET	ABRT_HS_ACKDET	ABRT_GCALL_READ	ABRT_GCALL_NOACK	ABRT_TXDATA_NOACK	ABRT_10ADDR2_NOACK	ABRT_10ADDR1_NOACK	ABRT_7B_ADDR_NOACK

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0b RW	**Reserved_17_23:** Reserved
16	0h RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0h RO	**ABRT_SLVRD_INTX:** 1 = When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0h RO	**ABRT_SLV_ARBLOST:** 1 = Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0h RO	**ABRT_SLVFLUSH_TXFIFO:** 1 = Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0h RO	**ARB_LOST:** 1 = Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS:** 1 = User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0h RO	**ABRT_HS_NORSTRT:** 1 = The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET:** 1 = Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**ABRT_HS_ACKDET:** 1 = Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h RO	**ABRT_GCALL_READ:** 1 = DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK:** 1 = DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK:** 1 = This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK:** 1 = Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK:** 1 = Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK:** 1 = Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

26.19.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. A write can occur on this register if either of the following conditions are met.

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)

NOTE = The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_1_31 (bits 31:1) | NACK (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Generate NACK (NACK):** This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. • 1 = generate NACK after data byte received • 0 = generate NACK/ACK normally

26.19.35 DMA Control Register (IC_DMA_CR)—Offset 88h

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the registers address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved_2_31 | TDMAE | RDMAE

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RW	**Reserved_2_31:** Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. • 0 = Transmit DMA disabled • 1 = Transmit DMA enabled
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. • 0 = Receive DMA disabled • 1 = Receive DMA enabled

26.19.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_8_31 (bits 31:8), DMATDL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

26.19.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals(IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist, writing to its address has no effect, and reading from its address returns zero.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved_8_31 (bits 31:8), DMARDL (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Receive Data Level (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

26.19.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL -- relative to SDA changing -- by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2. **NOTE:** The length of setup time is calculated using [(IC_SDA_SETUP - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000064h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Reserved_8_31																								SDA_SETUP							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	64h RW	**SDA Setup (SDA_SETUP):** It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

26.19.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [BAR] + 98h
	BAR Type: PCI Configuration Register (Size: 32 bits) **BAR Reference:** [B:0, D:24, F:7] + 10h

Default: 00000001h

Bits	31:1	0
Default	0000 0000 0000 0000 0000 0000 0000 000	1
Field	Reserved_1_31	ACK_GEN_CALL

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RW	**Reserved_1_31:** Reserved.
0	1h RW	**ACK General Call (ACK_GEN_CALL):** When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

26.19.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE register is set from 1 to 0, that is, when DW_apb_i2c is disabled.

- If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
- If IC_ENABLE has been set to 0, bits 2:1 will only be valid as soon as bit 0 is read as 0.

NOTE = When IC_ENABLE has been written with 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [BAR] + 9Ch
	BAR Type: PCI Configuration Register (Size: 32 bits) **BAR Reference:** [B:0, D:24, F:7] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved_3_31 (bits 31:3), SLV_RX_DATA_LOST (bit 2), SLV_DISABLED_WHILE_BUSY (bit 1), IC_EN (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RW	**Reserved_3_31:** Reserved.
2	0h RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0h RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0h RO	**ic_en Status (IC_EN):** This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

26.19.41 IC_FS_SPKLEN—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. The relevant I2C requirement is tSP (Table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000005h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Fields: Reserved_8_31 (bits 31:8), IC_FS_SPKLEN (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	5h RW	**IC_FS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.19.42 IC_HS_SPKLEN—Offset A4h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I2C requirement is tSP (Table 6) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31:8	Bits 7:0
Reserved_8_31	IC_HS_SPKLEN

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RW	**Reserved_8_31:** Reserved.
7:0	2h RW	**IC_HS_SPKLEN:** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression on page 52. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

26.19.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00FFFFEEh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
Reserved_24_31								TX_BUFFER_DEPTH								RX_BUFFER_DEPTH								ADD_ENCODED_PARAMS	HAS_DMA	INTR_IO	HC_COUNT_VALUES	MAX_SPEED_MODE		APB_DATA_WIDTH	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RW	**Reserved_24_31:** Reserved.
23:16	ffh RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	ffh RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	1h RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	1h RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	1h RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0h RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	3h RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	2h RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

26.19.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 3131352Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0

IC_COMP_VERSION

Bit Range	Default & Access	Field Name (ID): Description
31:0	3131352ah RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes.

26.19.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 44570140h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

IC_COMP_TYPE

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570140h RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

26.19.46 reg_CLOCK_PARAMS (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																															hs_source_clock

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz (LPT-LP compatible) 1 -133MHz (high-speed operation compatible)

26.19.47 Software Reset (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																														reset_apb	reset_func

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

26.19.48 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 55000000h

31			28				24				20				16				12				8				4				0
0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sda_mux_sel	sda_signal_state	scl_mux_sel	scl_signal_state	sda_rd_pre_drive	sda_rd_post_drive	scl_rd_pre_drive	scl_rd_post_drive	Reserved														i2c_fix_ctrl_1680	i2c_fix_ctrl_0770	i2c_fix_ctrl_1699	i2c_374798_fix_disable	i2c_374609_fix_disable	i2c_tx_lastbyte_flag	reserved			

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**sda_mux_sel:** Reserved.
30	1h RW	**sda_signal_state:** Reserved.
29	0h RW	**scl_mux_sel:** Reserved.
28	1h RW	**scl_signal_state:** Reserved.
27	0h RO	**sda_rd_pre_drive:** Reserved.
26	1h RO	**sda_rd_post_drive:** Reserved.
25	0h RO	**scl_rd_pre_drive:** Reserved.
24	1h RO	**scl_rd_post_drive:** Reserved.
23:10	0h RO	**Reserved:** Reserved
9	0h RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0h RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0h RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0h RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0h RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0h RW	**reserved:** reserved

26.19.49 I2C_ACK_COUNT—Offset 818h

TX transaction counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:20	RSVD0
19	i2c_tx_ack_count_clr_overflow
18:17	RSVD1
16	i2c_tx_count_overflow
15:0	i2c_tx_ack_count

Bit Range	Default & Access	Field Name (ID): Description
31:20	0b RO	**RSVD0:** Reserved
19	0h RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0b RO	**RSVD1:** Reserved
16	0h RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0h RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

26.19.50 I2C_TX_COMPLETE_INTR_STAT—Offset 820h

TX transaction has finished interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

Bits	31:2	1	0
Default	0000 0000 0000 0000 0000 0000 0000 00	0	0
Field	Reserved	i2c_tx_complete_interrupt_mask	i2c_tx_completion_interrupt

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved:** Reserved
1	0h RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0h RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

26.19.51 reg_I2C_TX_COMPLETE_INTR_CLR (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

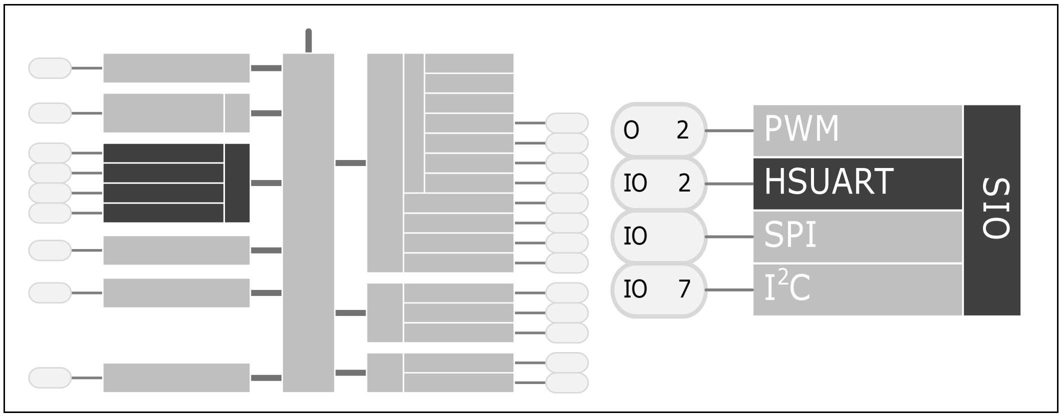
RSVD0

i2c_tx_complete_intr_clr

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

27 SIO – High Speed UART

The SoC implements two instances of high speed UART controller that support baud rates between 300 and 3686400. Hardware flow control is also supported.



27.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 278. UART 1 Interface Signals

Signal Name	Direction Plat. Power	Description
SIO_UART1_RXD	I V1P8S	**High-speed UART receive data input**: *This signal is muxed and may be used by other functions.*
SIO_UART1_TXD	O V1P8S	**High-speed UART transmit data:** *This signal is muxed and may be used by other functions.*
SIO_UART1_RTS#	O V1P8S	**High-speed UART request to send:** *This signal is muxed and may be used by other functions.*
SIO_UART1_CTS#	I V1P8S	**High-speed UART clear to send:** *This signal is muxed and may be used by other functions.*

Table 279. UART 2 Interface Signals

Signal Name	Direction Plat. Power	Description
SIO_UART2_RXD	I V1P8S	**High-speed UART receive data input:** *This signal is muxed and may be used by other functions.*
SIO_UART2_TXD	O V1P8S	**High-speed UART transmit data:** *This signal is muxed and may be used by other functions.*
SIO_UART2_RTS#	O V1P8S	**High-speed UART request to send:** *This signal is muxed and may be used by other functions.*
SIO_UART2_CTS#	I V1P8S	**High-speed UART clear to send:** *This signal is muxed and may be used by other functions.*

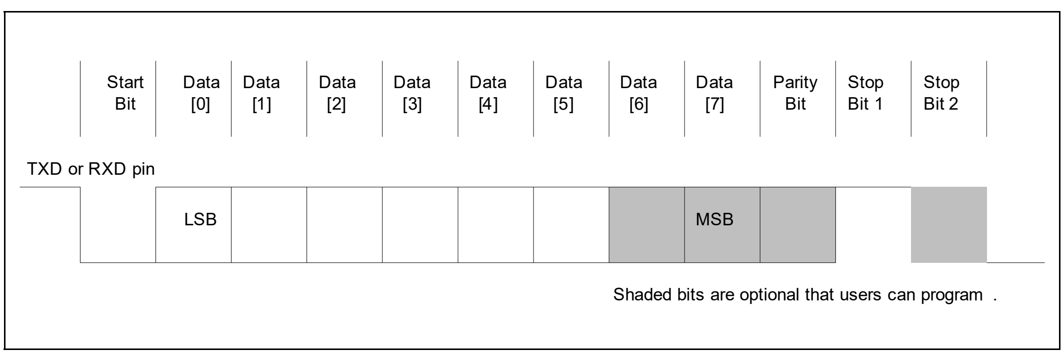
27.2 Features

27.2.1 UART Function

The UART transmits and receives data in bit frames as shown in Figure 126.

- Each data frame is between 7 and 12 bits long, depending on the size of data programmed and if parity and stop bits are enabled.
- The frame begins with a start bit that is represented by a high-to-low transition.
- Next, 5 to 8 bits of data are transmitted, beginning with the least significant bit. An optional parity bit follows, which is set if even parity is enabled and an odd number of ones exist within the data byte; or, if odd parity is enabled and the data byte contains an even number of ones.
- The data frame ends with one, one-and-one-half, or two stop bits (as programmed by users), which is represented by one or two successive bit periods of a logic one.

Figure 126. UART Data Transfer Flow



Each UART has a Transmit FIFO and a Receive FIFO and each holds 64 characters of data. There are two separate methods for moving data into/out of the FIFOs—Interrupts and Polling.

27.2.2 Clock and Reset

The BAUD rate generates from serial clock (**Sclock**) frequency which is based on a fixed base/system clock (**Fbase**) of 100 MHz processed through an M/N divider. M/N divider settings are found in the HSUART's PRV_CLOCK_PARAMS register. **Sclock** frequency = (Fbase*M)/N. Some useful Sclock frequencies and related M/N values are shown below:

Table 280. Sclock Frequencies from M/N Settings

M Value	N Value	Sclock
288 (0x120)	15625 (0x3D09)	1.84320 MHz
1024 (0x400)	3125 (0xC35)	32.7680 MHz
9216 (0x2400)	15625 (0x3D09)	58.9824 MHz

27.2.3 Baud Rate Generator

The baud rates for the UARTs are generated with from the serial clock frequency (Sclock) by programming the DLH and DLL registers as a divisor. The hexadecimal value of the **divisor** is (IER_DLH[7:0]<<8) | RBR_THR_DLL[7:0].

Fbase is the system clock frequency in Hz (100,000,000 in decimal when the system clock frequency is 100 MHz.).

The output baud rate is as follows:

— **baud rate** = (Sclock) / (16 * divisor)

Table 281. Baud Rates Achievable with Different DLAB Settings

DLH,DLL Divisor	DLH,DLL Divisor Hexadecimal	Baud Rate
Sclock = 1.84320 MHz		
1	0001	115200
2	0002	57600
3	0003	38400
6	0006	19200
12	000C	9600
24	0018	4800
48	0030	2400
192	00C0	600
384	0180	300
Sclock = 58.9824 MHz		
4	0004	921600
8	0008	460800
16	0010	230400
24	0018	153600
Sclock = 32.768 MHz		
8	0008	256000
16	0010	128000

27.3 Use

Each UART has a transmit FIFO and a receive FIFO, each FIFO holding 64 characters of data. Three separate methods move data into and out of the FIFOs: interrupts, DMA, and polled.

27.3.1 DMA Mode Operation

27.3.1.1 Receiver DMA

The data transfer from the HSUART to host memory is controlled by the DMA write channel. To configure the channel in write mode, channel direction in the channel control register needs to be programmed to "1". The software need to program the descriptor start address register, descriptor transfer size register, and descriptor control register before starting the channel using the channel active bit in the channel control register.

27.3.1.2 Transmit DMA

The data transfer from host memory to HSUART is controlled by DMA read channel. To configure the channel in read mode, channel direction in the channel control register needs to be programmed to "0". The software need to program the descriptor start address register, descriptor transfer size register, and descriptor control register before starting the channel using the channel active bit in the channel control register.

27.3.1.3 Removing Trailing Bytes in DMA Mode

When the number of entries in the Receive FIFO is less than its trigger level, and no additional data is received, the remaining bytes are called Trailing bytes. These are DMAed out by the DMA as it has visibility into the FIFO Occupancy register.

27.3.2 FIFO Polled-Mode Operation

With the FIFOs enabled (IIR_FCR.IID0_FIFOE bit set to 1), clearing IER_DLH[7] and IER_DLH[4:0] puts the serial port in the FIFO Polled Operation mode. Because the receiver and the transmitter are controlled separately, either one or both can be in Polled Operation mode. In this mode, software checks Receiver and Transmitter status using the Line Status Register (LSR). The processor polls the following bits for Receive and Transmit Data Service.

27.3.2.1 Receive Data Service

The processor checks data ready (LSR.DR) bit which is set when 1 or more bytes remains in the Receive FIFO or Receive Buffer Register (RBR_THR_DLL).

27.3.2.2 Transmit Data Service

The processor checks transmit data request LSR.THRE bit, which is set when the transmitter needs data.

The processor can also check transmitter empty LSR.TEMT, which is set when the Transmit FIFO or Holding register is empty.

27.3.2.3 Autoflow Control

Autoflow Control uses Clear-to-Send (nCTS) and Request-to-Send (nRTS) signals to automatically control the flow of data between the UART and external modem. When autoflow is enabled, the remote device is not allowed to send data unless the UART asserts nRTS low. If the UART de-asserts nRTS while the remote device is sending data, the remote device is allowed to send one additional byte after nRTS is deasserted. An overflow could occur if the remote device violates this rule. Likewise, the UART is not allowed to transmit data unless the remote device asserts nCTS low. This feature increases system efficiency and eliminates the possibility of a Receive FIFO Overflow error due to long interrupt latency.

Autoflow mode can be used in two ways: Full autoflow, automating both nCTS and nRTS, and half autoflow, automating only nCTS. Full Autoflow is enabled by writing a 1 to bits 1 and 5 of the Modem Control Register (MCR). Auto-nCTS-Only mode is enabled by writing a 1 to bit 5 and a 0 to bit 1 of the MCR register.

27.3.2.4 RTS (UART Output)

When in full autoflow mode, nRTS is asserted when the UART FIFO is ready to receive data from the remote transmitter. This occurs when the amount of data in the Receive FIFO is below the programmable threshold value. When the amount of data in the Receive FIFO reaches the programmable threshold, nRTS is de-asserted. It will be asserted once again when enough bytes are removed from the FIFO to lower the data level below the threshold.

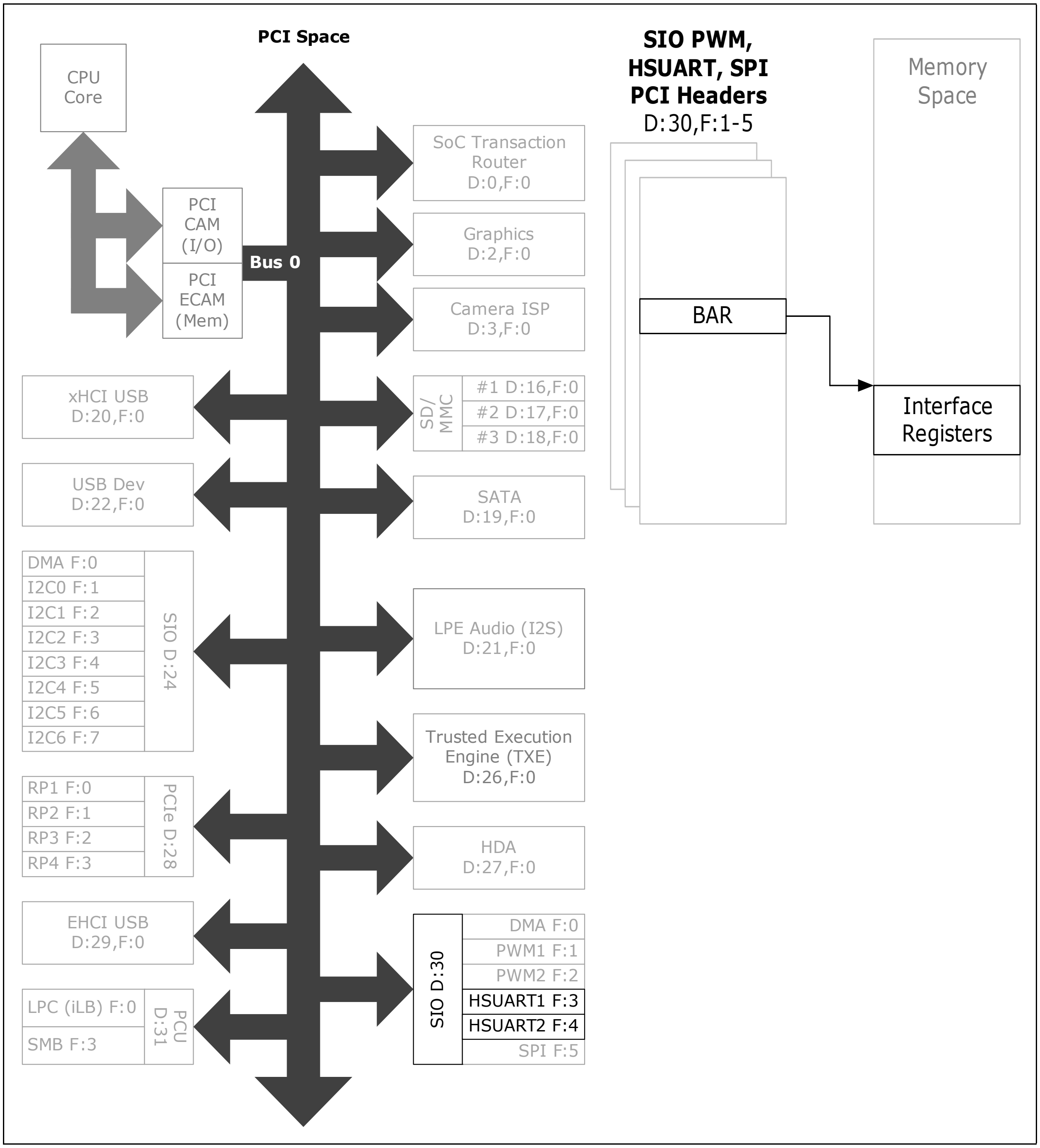
27.3.2.5 CTS (UART Input)

When in Full or Half-Autoflow mode, nCTS is asserted by the remote receiver when the receiver is ready to receive data from the UART. The UART checks nCTS before sending the next byte of data and will not transmit the byte until nCTS is low. If nCTS goes high while the transfer of a byte is in progress, the transmitter will complete this byte.

27.4 Register Map

Refer to Chapter 3, "Register Access Methods" and Chapter 4, "Mapping Address Spaces" for additional information.

Figure 127. SIO - HSUART Register Map



§

27.5 SIO HSUART 0 PCI Configuration Registers

Table 282. Summary of HSUART 0 PCI Configuration Registers—0/30/3

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4204	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 4205	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4206	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4206	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 4207	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 4208	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4208	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4209	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4209	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4210	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4210	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4211	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 4212	00000000h

27.5.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

27.5.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:3] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

27.5.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:3] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLASS_CODES (bits 31:8), RID (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

27.5.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:3] + Ch

Default: 00800000h

31	28				24				20				16				12				8				4						0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:24	Bit 23	Bits 22:16	Bits 15:8	Bits 7:0
Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

27.5.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	28				24				20				16				12				8				4						0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:12	Bits 11:4	Bit 3	Bits 2:1	Bit 0
BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

27.5.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BASEADDR1																				SIZEINDICATOR1								PREFETCHABLE1	TYPE1		MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

27.5.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 2Ch

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
SUBSYSTEMID				SUBSYSTEMVENDORID			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

27.5.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 30h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
EXPANSION_ROM_BASE							

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

27.5.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0 (31:8), CAPPTR_POWER (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

27.5.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

MAX_LAT (31:24), MIN_GNT (23:16), Reserved0 (15:12), INTPIN (11:8), INTLINE (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

27.5.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 80h

Default: 00030001h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

31:27	26:19	18:16	15:8	7:0
PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

27.5.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 84h

Default: 00000008h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

31:16	15	14:9	8	7:4	3	2	1:0
Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

27.5.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:3] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

27.6 SIO HSUART 0 Memory Mapped I/O Registers

Table 283. Summary of HSUART 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Receive Buffer Register/Transmit Holding Register/Divisor Latch (Low). (RBR_THR_DLL)—Offset 0h" on page 4214	00000000h
4–7h	4	"Divisor Latch (High)/ Interrupt Enable Register. (IER_DLH)—Offset 4h" on page 4215	00000000h
8–Bh	4	"Interrupt Identification Register and FIFO Control Register. (IIR_FCR)—Offset 8h" on page 4216	00000001h
C–Fh	4	"Line Control Register (LCR)—Offset Ch" on page 4217	00000000h
10–13h	4	"Modem Control Register (MCR)—Offset 10h" on page 4218	00000000h
14–17h	4	"Line Status Register (LSR)—Offset 14h" on page 4219	00000060h
18–1Bh	4	"Modem Status Register (MSR)—Offset 18h" on page 4221	00000000h
1C–1Fh	4	"Scratchpad Register (SCR)—Offset 1Ch" on page 4222	00000000h
30–33h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h" on page 4223	00000000h
34–37h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h" on page 4224	00000000h
38–3Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h" on page 4224	00000000h
3C–3Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch" on page 4225	00000000h
40–43h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h" on page 4225	00000000h
44–47h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h" on page 4226	00000000h
48–4Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h" on page 4226	00000000h
4C–4Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch" on page 4227	00000000h
50–53h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h" on page 4227	00000000h
54–57h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h" on page 4228	00000000h
58–5Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h" on page 4228	00000000h
5C–5Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch" on page 4229	00000000h
60–63h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h" on page 4229	00000000h
64–67h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h" on page 4230	00000000h
68–6Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h" on page 4230	00000000h
6C–6Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch" on page 4231	00000000h
70–73h	4	"FIFO Access Register (FAR)—Offset 70h" on page 4231	00000000h

Table 283. Summary of HSUART 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
74–77h	4	"Transmit FIFO Read (TFR)—Offset 74h" on page 4232	00000000h
78–7Bh	4	"Receive FIFO Write (RFW)—Offset 78h" on page 4232	00000000h
7C–7Fh	4	"UART Status Register (USR)—Offset 7Ch" on page 4233	00000006h
80–83h	4	"Transmit FIFO Level (TFL)—Offset 80h" on page 4234	00000000h
84–87h	4	"Receive FIFO Level (RFL)—Offset 84h" on page 4234	00000000h
88–8Bh	4	"Software Reset Register (SRR)—Offset 88h" on page 4235	00000000h
8C–8Fh	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 4235	00000000h
90–93h	4	"Shadow Break Control Register (SBCR)—Offset 90h" on page 4236	00000000h
94–97h	4	"Shadow DMA Mode (SDMAM)—Offset 94h" on page 4237	00000000h
98–9Bh	4	"Shadow FIFO Enable (SFE)—Offset 98h" on page 4237	00000000h
9C–9Fh	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 4235	00000000h
A0–A3h	4	"Shadow TX Empty Trigger (STET)—Offset A0h" on page 4238	00000000h
A4–A7h	4	"Halt TX (HTX)—Offset A4h" on page 4239	00000000h
A8–ABh	4	"DMA Software Acknowledge (DMASA)—Offset A8h" on page 4239	00000000h
F4–F7h	4	"Component Parameter Register (CPR)—Offset F4h" on page 4240	00043F32h
F8–FBh	4	"UART Component Version (UCV)—Offset F8h" on page 4241	3330382Ah
FC–FFh	4	"Component Type Register (CTR)—Offset FCh" on page 4242	44570110h
800–803h	4	"Private Clock Params (PRV_CLOCK_PARAMS)—Offset 800h" on page 4242	00000000h
804–807h	4	"Software Resets (RESETS)—Offset 804h" on page 4243	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 4243	00000050h
818–81Bh	4	"UART_BYTE_COUNT—Offset 818h" on page 4244	00000000h
820–823h	4	"UART_OVERFLOW_INTR_STAT—Offset 820h" on page 4245	00000000h

27.6.1 Receive Buffer Register/Transmit Holding Register/Divisor Latch (Low). (RBR_THR_DLL)—Offset 0h

Register is used for different purposes depending on the mode. See description details

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

Bits	31:8	7:0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Field	RSVD0	rbr_thr_dll

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**rbr_thr_dll:** RBR[7:0] (Receive Buffer Register) (Read Only): Data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs. THR[7:0] (Transmit Holding Register) (Write Only): Data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. DLL[7:0] (Divisor Latch Low) (Read-Write): Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. this register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest HSUart clock should be allowed to pass before transmitting or receiving data.

27.6.2 Divisor Latch (High)/ Interrupt Enable Register. (IER_DLH)—Offset 4h

Register bits [7:0] is used for different purposes depending on the mode. DLH (Divisor Latch High) Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest HSUart clock should be allowed to pass before transmitting or receiving data.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								PTIME_dlh7	RSVD1			EDSSI_dlh3	ELSI_dhl2	ETBEI_dlh1	ERBFI_dlh0

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**PTIME_dlh7:** PTIME (PTIME) This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled
6:4	0b RO	**RSVD1:** Reserved
3	0h RW	**EDSSI_dlh3:** EDSSI (Enable Modem Status Interrupt) This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled
2	0h RW	**ELSI_dhl2:** ELSI (Enable Line Status Interrupt) This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled
1	0h RW	**ETBEI_dlh1:** ETBEI (Enable Transmit Holding Register Empty Interrupt) This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled
0	0h RW	**ERBFI_dlh0:** ERBFI (Enable Received Data Available Interrupt) This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled

27.6.3 Interrupt Identification Register and FIFO Control Register. (IIR_FCR)—Offset 8h

Register is used for different purposes depending on the mode. See description details Interrupt ID [3:0] 0001: No Interrupt Pending 0110: Receiver Line Status (1st Priority) 0100: Receiver Data Available (2nd Priority) 1100: Character Timeout (2nd Priority) 0010: THR Empty (3rd Priority) 0000: Modem Status (4th Priority) 0111: Busy Detect Indication (5th Priority)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
RSVD0																								RCVR		TET		DMAM	XFIFOR	RFIFOR	FIFOE

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:6	0h RW	**FIFOSE_RCVR (RCVR):** FIFOSE (FIFOs Enabled) This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. The following trigger levels are supported: • 00 = 1 character in the FIFO • 01 = FIFO full • 10 = FIFO full • 11 = FIFO 2 less than full
5:4	0h RW	**Res_TET (TET):** TX Empty Trigger. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. The following trigger levels are supported: • 00 = FIFO empty • 01 = 2 characters in the FIFO • 10 = FIFO full • 11 = FIFO full
3	0h RW	**IID3_DMAM (DMAM):** DMA Mode. Reserved
2	0h RW	**IID2_XFIFOR (XFIFOR):** XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h RW	**IID1_RFIFOR (RFIFOR):** RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	1h RW	**IID0_FIFO Enable (FIFOE):** This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset

27.6.4 Line Control Register (LCR)—Offset Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								DLAB	Break	RSVD1	EPS	PEN	STOP	DLS	

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Divisor Latch Access Bit (DLAB):** This bit is used to enable reading and writing of the Divisor Latch register(DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**Break Control Bit (Break):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0b RO	**RSVD1:** Reserved
4	0h RW	**Even Parity Select (EPS):** This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	0h RW	**Parity Enable (PEN):** This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. • 0 = parity disabled • 1 = parity enabled
2	0h RW	**Number of Stop Bits (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. • 0 = 1 stop bit • 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	0h RW	**Data Length Select (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected are as follows: • 00 = 5 bits • 01 = 6 bits • 10 = 7 bits • 11 = 8 bits

27.6.5 Modem Control Register (MCR)—Offset 10h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																										AFCE	LoopBack	OUT2	OUT1	RTS	DTR

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RO	**RSVD0:** Reserved
5	0h RW	**Auto Flow Control Enable (AFCE):** When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, • 0 = Auto Flow Control Mode disabled • 1 = Auto Flow Control Mode enabled Reset Value: 0x0
4	0h RW	**LoopBack Bit (LoopBack):** This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. Reset Value: 0x0
3	0h RW	**Output2 (OUT2):** This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: • 0 = out2_n de-asserted (logic 1) • 1 = out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
2	0h RW	**Output1 (OUT1):** This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: • 0 = out1_n de-asserted (logic 1) • 1 = out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
1	0h RW	**Request to Send (RTS):** This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
0	0h RW	**Data Terminal Ready (DTR):** This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: • 0 = dtr_n de-asserted (logic 1) • 1 = dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

27.6.6 Line Status Register (LSR)—Offset 14h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000060h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
RSVD0																								RFE	TEMT	THRE	BI	FE	PE	OE	DR

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Receiver FIFO Error Bit (RFE):** This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. • 0 = no error in RX FIFO • 1 = error in RX FIFO This bit is cleared when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. Reset Value: 0x0
6	1h RW	**Transmitter Empty Bit (TEMT):** If FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. Reset Value: 0x1
5	1h RW	**Transmit Holding Register Empty Bit (THRE):** If THRE mode is disabled (IER[7] set to zero), this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE mode is enabled and and FIFOs enabled (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. Reset Value: 0x1
4	0h RW	**Break Interrupt Bit (BI):** This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	0h RW	**Framing Error Bit (FE):** This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). • 0 = no framing error • 1 = framing error Reading the LSR clears the FE bit. Reset Value: 0x0
2	0h RW	**Parity Error Bit (PE):** This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). • 0 = no parity error • 1 = parity error Reading the LSR clears the PE bit. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Overrun Error Bit (OE):** This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. • 0 = no overrun error • 1 = overrun error Reading the LSR clears the OE bit. Reset Value: 0x0
0	0h RW	**Data Ready Bit (DR):** This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. • 0 = no data ready • 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. Reset Value: 0x0

27.6.7 Modem Status Register (MSR)—Offset 18h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31–8	7	6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
RSVD0	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Data Carrier Detect (DCD):** This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted, it is an indication that the carrier has been detected by the modem or data set. • 0 = dcd_n input is de-asserted (logic 1) • 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Reset Value: 0x0
6	0h RW	**Ring Indicator (RI):** This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. • 0 = ri_n input is de-asserted (logic 1) • 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Data Set Ready (DSR):** This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. • 0 = dsr_n input is de-asserted (logic 1) • 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Reset Value: 0x0
4	0h RW	**Clear to Send (CTS):** This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted, it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. • 0 = cts_n input is de-asserted (logic 1) • 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Reset Value: 0x0
3	0h RW	**Delta Data Carrier Detect (DDCD):** This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. • 0 = no change on dcd_n since last read of MSR • 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Reset Value: 0x0
2	0h RW	**Trailing Edge of Ring Indicator (TERI):** This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. • 0 = no change on ri_n since last read of MSR • 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Reset Value: 0x0
1	0h RW	**Delta Data Set Ready (DDSR):** This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. • 0 = no change on dsr_n since last read of MSR • 1 = change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Reset Value: 0x0
0	0h RW	**Delta Clear to Send (DCTS):** This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. • 0 = no change on cts_n since last read of MSR • 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note that if the DCTS bit is not set, the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Reset Value: 0x0

27.6.8 Scratchpad Register (SCR)—Offset 1Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								scr							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**scr:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart. Reset Value: 0x0

27.6.9 Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr0							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr0:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data are lost. An overrun error also occurs. Reset Value: 0x0

27.6.10 Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
											RSVD0																srbr_sthr1				

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr1:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.11 Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
											RSVD0																srbr_sthr2				

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr2:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.12 Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

Bits	31:8	7:0
Default	0000 0000 0000 0000 0000 0000	0000 0000
Field	RSVD0	srbr_sthr3

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr3:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.13 Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

Bits	31:8	7:0
Default	0000 0000 0000 0000 0000 0000	0000 0000
Field	RSVD0	srbr_sthr4

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr4:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.14 Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD0						srbr_sthr5	

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr5:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.15 Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD0						srbr_sthr6	

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr6:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.16 Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD0 | srbr_sthr7

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr7:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.17 Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD0 | srbr_sthr8

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr8:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.18 Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr9							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr9:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.19 Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr10							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr10:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.20 Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr11							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr11:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.21 Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr12							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr12:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.22 Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:8) | srbr_sthr13 (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr13:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.23 Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:8) | srbr_sthr14 (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr14:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.24 Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:8), srbr_sthr15 (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr15:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.6.25 FIFO Access Register (FAR)—Offset 70h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:1), srbr_sthr (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**srbr_sthr:** Writes have no effect when FIFO_ACCESS == No, always readable. This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. • 0 = FIFO access mode disabled • 1 = FIFO access mode enabled Note that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

27.6.26 Transmit FIFO Read (TFR)—Offset 74h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								tfr							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**Transmit FIFO Read (tfr):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

27.6.27 Receive FIFO Write (RFW)—Offset 78h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																						RFFE	RFPE	RFWD							

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RO	**RSVD0:** Reserved
9	0h RW	**Receive FIFO Framing Error (RFFE):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR. Reset Value: 0x0
8	0h RW	**Receive FIFO Parity Error (RFPE):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR. Reset Value: 0x0
7:0	0h RW	**Receive FIFO Write Data (RFWD):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. Reset Value: 0x0

27.6.28 UART Status Register (USR)—Offset 7Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000006h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD0																											RFF	RFNE	TFE	TFNF	BUSY

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RO	**RSVD0:** Reserved
4	0h RW	**Receive FIFO Full (RFF):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. • 0 = Receive FIFO not full • 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full. Reset Value: 0x0
3	0h RW	**Receive FIFO Not Empty (RFNE):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. • 0 = Receive FIFO is empty • 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty. Reset Value: 0x0
2	1h RW	**Transmit FIFO Empty (TFE):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. • 0 = Transmit FIFO is not empty • 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty. Reset Value: 0x1

Bit Range	Default & Access	Field Name (ID): Description
1	1h RW	**Transmit FIFO Not Full (TFNF):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. • 0 = Transmit FIFO is full • 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full. Reset Value: 0x1
0	0h RW	**UART Busy (BUSY):** Reserved

27.6.29 Transmit FIFO Level (TFL)—Offset 80h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																											tfl				

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RO	**RSVD0:** Reserved
4:0	0h RW	**Transmit FIFO Level (tfl):** This indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

27.6.30 Receive FIFO Level (RFL)—Offset 84h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																											rfl				

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Receive FIFO Level (rfl):** This indicates the number of data entries in the receive FIFO. Reset Value: 0x0

27.6.31 Software Reset Register (SRR)—Offset 88h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																													XFR	RFR	UR

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RO	**RSVD0:** Reserved
2	0h RW	**XMIT FIFO Reset (XFR):** This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
1	0h RW	**RCVR FIFO Reset (RFR):** This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
0	0h RW	**UART Reset (UR):** This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset. Reset Value: 0x0

27.6.32 Shadow Request to Send (SRTS)—Offset 8Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | srts

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow Request to Send (srts):** This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

27.6.33 Shadow Break Control Register (SBCR)—Offset 90h

This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | sbcb

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow Break Control Bit (sbcb):** Reserved.

27.6.34 Shadow DMA Mode (SDMAM)—Offset 94h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD0 (bits 31:1), sdmam (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow DMA Mode (sdmam):** This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). • 0 = mode 0 • 1 = mode 1 Reset Value: 0x0

27.6.35 Shadow FIFO Enable (SFE)—Offset 98h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD0 (bits 31:1), sfe (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow FIFO Enable (sfe):** This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

27.6.36 Shadow RCVR Trigger (SRT)—Offset 9Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0

Bits 31:2	Bits 1:0
RSVD0	srt

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RO	**RSVD0:** Reserved
1:0	0h RW	**Shadow RCVR Trigger (srt):** This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: • 00 = 1 character in the FIFO • 01 = FIFO full • 10 = FIFO full • 11 = FIFO 2 less than full Reset Value: 0x0

27.6.37 Shadow TX Empty Trigger (STET)—Offset A0h

This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported:

- 00 = FIFO empty
- 01 = 2 characters in the FIFO
- 10 = FIFO full
- 11 = FIFO full

Reset Value: 0x0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (31:2), stet (1:0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RO	**RSVD0:** Reserved
1:0	0h RW	**stet:** Shadow TX Empty Trigger

27.6.38 Halt TX (HTX)—Offset A4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (31:1), htx (0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**htx:** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. • 0 = Halt TX disabled • 1 = Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation. Reset Value: 0x0

27.6.39 DMA Software Acknowledge (DMASA)—Offset A8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																															dmasa

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**dmasa:** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when DMA_EXTRA == No.

27.6.40 Component Parameter Register (CPR)—Offset F4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00043F32h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	0	0	1	1	0	0	1	0
RSVD0								FIFO_MODE								RSVD1		DMA_EXTRA	UART_ADD_ENCODED_PARAMS	SHADOW	FIFO_STAT	FIFO_ACCESS	ADDITIONAL_FEAT	SIR_LP_MODE	SIR_MODE	THRE_MODE	AFCE_MODE	RSVD2		APB_DATA_WIDTH	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RSVD0:** Reserved
23:16	4h RO	**FIFO MODE (FIFO_MODE):** • 0x00 = 0 • 0x01 = 16 • 0x02 = 32 • to • 0x80 = 2048 • 0x81- 0xff = reserved
15:14	0b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
13	1h RO	**DMA EXTRA (DMA_EXTRA):** • 0 = FALSE • 1 = TRUE
12	1h RO	**UART ADD ENCODED PARAMS (UART_ADD_ENCODED_PARAMS):** • 0 = FALSE, • 1 = TRUE
11	1h RO	**SHADOW:** • 0 = FALSE, • 1 = TRUE
10	1h RO	**FIFO STAT (FIFO_STAT):** • 0 = FALSE, • 1 = TRUE
9	1h RO	**FIFO ACCESS (FIFO_ACCESS):** • 0 = FALSE, • 1 = TRUE
8	1h RO	**ADDITIONAL FEAT (ADDITIONAL_FEAT):** • 0 = FALSE, • 1 = TRUE
7	0h RO	**SIR LP MODE (SIR_LP_MODE):** • 0 = FALSE, • 1 = TRUE
6	0h RO	**SIR MODE (SIR_MODE):** • 0 = FALSE, • 1 = TRUE
5	1h RO	**THRE MODE (THRE_MODE):** • 0 = FALSE, • 1 = TRUE
4	1h RO	**AFCE MODE (AFCE_MODE):** • 0 = FALSE, • 1 = TRUE
3:2	0b RO	**RSVD2:** Reserved
1:0	2h RO	**APB DATA WIDTH (APB_DATA_WIDTH):** • 00 = 8 bits • 01 = 16 bits • 10 = 32 bits • 11 = reserved

27.6.41 UART Component Version (UCV)—Offset F8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 3330382Ah

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0	1	0	1	0

UART

Bit Range	Default & Access	Field Name (ID): Description
31:0	3330382ah RO	**UART:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*. Reset Value: See the releases table in the AMBA 2 release notes.

27.6.42 Component Type Register (CTR)—Offset FCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 44570110h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

PeripheralID

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO	**Peripheral ID (PeripheralID):** This register contains the peripherals identification code. Reset Value: 0x44570110

27.6.43 Private Clock Params (PRV_CLOCK_PARAMS)—Offset 800h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

clk_update | n_val | m_val | clk_en

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**clk_update:** update the clock divider after seeting new m and n values
30:16	0h RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0h RW	**M_VAL (m_val):** m value for the m over n divider
0	0h RW	**clk_en:** clk en of the m over n divider

27.6.44 Software Resets (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																														reset_apb	reset_func

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

27.6.45 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000050h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1	0 0 0 0	

RSVD0	gpo1	gater_override	gpo3	gpo2	uart_374646_fix_disable	reset_e	sleep_enable	power_enable

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**gpo1:** not applicable
6	1h RW	**gater_override:** not applicable
5	0h RW	**gpo3:** not applicable
4	1h RW	**gpo2:** This bit indicates whether the UART clock req will be dynamic or controlled by the UART clock en: • 1 = controlled by the clk en • 0 = dynamic Default value = 1
3	0h RW	**uart_374646_fix_disable:** Disable rts_n override
2	0h RW	**reset_e:** not applicable
1	0h RW	**sleep_enable:** not applicable
0	0h RW	**power_enable:** not applicable

27.6.46 UART_BYTE_COUNT—Offset 818h

Transaction counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reseved (31:16); uart_tx_byte_count (15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**reserved (reseved):** reserved
15:0	0h RO	**uart_tx_byte_count:** UART transaction counter

27.6.47 UART_OVERFLOW_INTR_STAT—Offset 820h

Overflow interrupt

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reserved (31:2); uart_overflow_intr_mask (1); uart_overflow_intr (0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**reserved:** reserved
1	0h RW	**uart1_overflow_intr_mask (uart_overflow_intr_mask):** Mask the overflow intr
0	0h RO	**uart_overflow_intr:** Indicate there was count overflow

27.7 PCU PMC Memory Mapped I/O Registers

Table 284. Summary of PCU iLB PMC Memory Mapped I/O Registers—PMC_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"PRSTS - Power and Reset Status (PRSTS)—Offset 0h" on page 4247	00000000h
8h	4	"PM_CFG - Power Management Configuration (PMC_CFG)—Offset 8h" on page 4248	00000000h
Ch	4	"VLV_PM_STS - VLV Power Management Status (VLV_PM_STS)—Offset Ch" on page 4249	00000000h
10h	4	"MTPMC - Message to PMC (MTPMC)—Offset 10h" on page 4251	00000000h
20h	4	"General PM Configuration 1 (GEN_PMCON1)—Offset 20h" on page 4251	00004004h
24h	4	"General PM Configuration 2 (GEN_PMCON2)—Offset 24h" on page 4254	00000000h
28h	4	"MFPMC - Message from PMC (MFPMC)—Offset 28h" on page 4255	00000000h
2Ch	4	"SEC_STS - SEC Status (SEC_STS)—Offset 2Ch" on page 4256	00000000h
30h	4	"Configured Revision ID (CRID)—Offset 30h" on page 4256	00000000h
34h	4	"Function Disable (FUNC_DIS)—Offset 34h" on page 4257	00000000h
38h	4	"Function Disable 2 (FUNC_DIS_2)—Offset 38h" on page 4258	00000000h
3Ch	4	"S0ix wake enable (S0IX_WAKE_EN)—Offset 3Ch" on page 4258	00FFFFFFh
40h	4	"S0ix wake Status (S0IX_WAKE_STS)—Offset 40h" on page 4260	00000000h
44h	4	"S0ix control (S0IX_CTL)—Offset 44h" on page 4261	00000050h
48h	4	"ETR - Extended Test Mode Register (ETR)—Offset 48h" on page 4262	00230000h
50h	4	"VLT - Voltage Detect Register (VLT)—Offset 50h" on page 4263	00000000h
58h	4	"GPIO_ROUT - GPIO_ROUT register (GPIO_ROUT)—Offset 58h" on page 4263	00000000h
60h	4	"PLT_CLK_CTL_0 - Platform Clock Control 0 (PLT_CLK_CTL_0)—Offset 60h" on page 4264	00000003h
64h	4	"PLT_CLK_CTL_1 - Platform Clock Control 1 (PLT_CLK_CTL_1)—Offset 64h" on page 4265	00000003h
68h	4	"PLT_CLK_CTL_2 - Platform Clock Control 2 (PLT_CLK_CTL_2)—Offset 68h" on page 4265	00000003h
6Ch	4	"PLT_CLK_CTL_3 - Platform Clock Control 3 (PLT_CLK_CTL_3)—Offset 6Ch" on page 4266	00000003h
70h	4	"PLT_CLK_CTL_4 - Platform Clock Control 4 (PLT_CLK_CTL_4)—Offset 70h" on page 4266	00000003h
74h	4	"PLT_CLK_CTL_5 - Platform Clock Control 5 (PLT_CLK_CTL_5)—Offset 74h" on page 4267	00000003h
80h	4	"S0IR_TMR - S0I Ready Residency Timer (S0IR_TMR)—Offset 80h" on page 4268	00000000h
84h	4	"S0I1_TMR - S0I1 Residency Timer (S0I1_TMR)—Offset 84h" on page 4268	00000000h
88h	4	"S0I2_TMR - S0I2 Residency Timer (S0I2_TMR)—Offset 88h" on page 4269	00000000h
8Ch	4	"S0I3_TMR - S0I3 Residency Timer (S0I3_TMR)—Offset 8Ch" on page 4269	00000000h
90h	4	"S0_TMR - S0 Residency Timer (S0_TMR)—Offset 90h" on page 4270	00000000h
98h	4	"PSS - Power island Power Status (PSS)—Offset 98h" on page 4270	00000000h
A0h	4	"D3_STS_0 - D3 Status register 0 (D3_STS_0)—Offset A0h" on page 4271	00000000h
A4h	4	"D3_STS_1 - D3 Status register 1 (D3_STS_1)—Offset A4h" on page 4271	00000000h

Table 284. Summary of PCU iLB PMC Memory Mapped I/O Registers—PMC_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
A8h	4	"D3_STDBY_STS_0 - D3 Standby Status register 0 (D3_STDBY_STS_0)—Offset A8h" on page 4272	00000000h
ACh	4	"D3_STDBY_STS_1 - D3 Standby Status register 1 (D3_STDBY_STS_1)—Offset ACh" on page 4272	00000000h
B0h	4	"MTPMC_1 - Message to PMC 1 (MTPMC_1)—Offset B0h" on page 4273	00000000h
B4h	4	"MTPMC_2 - Message to PMC 2 (MTPMC_2)—Offset B4h" on page 4274	00000000h
B8h	4	"MTPMC_3 - Message to PMC 3 (MTPMC_3)—Offset B8h" on page 4274	00000000h
BCh	4	"MTPMC_4 - Message to PMC 4 (MTPMC_4)—Offset BCh" on page 4275	00000000h
C0h	4	"PME Status 0 - Status bit for PME messages (PME_STS)—Offset C0h" on page 4275	00000000h
C4h	4	"GPE Level Edge mode (GPE_LEVEL_EDGE)—Offset C4h" on page 4276	00000000h
C8h	4	"GPE polarity mode (GPE_POLARITY)—Offset C8h" on page 4276	00000000h
CCh	4	"Lock Register (LOCK)—Offset CCh" on page 4277	00000000h
D0h	4	"Virtual UART register (VUART1)—Offset D0h" on page 4277	00000000h
D4h	4	"Virtual UART register (VUART2)—Offset D4h" on page 4278	00000000h
D8h	4	"Virtual UART register (VUART3)—Offset D8h" on page 4278	00000000h
DCh	4	"Virtual UART register (VUART4)—Offset DCh" on page 4279	00000000h

27.7.1 PRSTS - Power and Reset Status (PRSTS)—Offset 0h

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well is down, they are marked as suspend well bits. All suspend well bits in this register are reset by global reset#.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PRSTS: [PMC_BASE_ADDRESS] + 0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31:24	23:16	15	14:12	11	10	9	8	7	6	5	4	3:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0 0	0	0	0	0	0	0	0	0	0 0 0 0
pmc_prodid	pmc_revid	pmc_wdt_sts	reserved	code_copied_sts	reserved1	code_load_to	pmc_op_sts	sec_gblrst_sts	sec_wdt_sts	wol_ovr_wk_sts	pmc_host_wake_sts	reserved2

Bit Range	Default & Access	Description
31:24	0b RO	**Power Management Controller Product ID (PMC_PRODID) (pmc_prodid):** This field communicates the Product Family of the power management functionality
23:16	0b RO	**Power Management Controller Revision ID (PMC_REVID) (pmc_revid):** This field communicates the implementation revision of the power management functionality.
15	0b RW	**PMC Watchdog Timer Status (PMC_WDT_STS) (pmc_wdt_sts):** This bit will be set to '1' when the PMC Watch Dog Timer triggers a reset. It will be cleared by a write of '1' by software.
14:12	0b RO	**reserved:** Reserved.
11	0b RO	**Code Copied Over Status (CODE_COPIED_STS) (code_copied_sts):** The SOC sets this bit when PMC code is successfully authenticated and loaded from the flash
10	0b RO	**reserved (reserved1):** Reserved.
9	0b RO	**Code Load Timeout Status (CODE_LOAD_TO) (code_load_to):** The SOC sets this bit if the loading function fails to complete within a reasonable time limit. This bit remains valid after a PMC Code load is attempted until the next global reset
8	0b RO	**PMC Operational Status (PMC_OP_STS) (pmc_op_sts):** The SOC sets this bit when the PMC becomes operational after completing the Code Load. BIOS must wait for this bit to be set before performing resets or sleep events. This bit remains valid after a PMC Code load until the next global reset
7	0b RW	**SEC Watch Dog Timer Status (SEC_GBLRST_STS) (sec_gblrst_sts):** This bit will be set to '1' when the SEC FW triggers a reset. It will be cleared by a write of '1' by software.
6	0b RW	**SEC Watch Dog Timer Status (SEC_WDT_STS) (sec_wdt_sts):** This bit will be set to '1' when the SEC Watch Dog Timer triggers a reset. It will be cleared by a write of '1' by software.
5	0b RW	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS) (wol_ovr_wk_sts):** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4	0b RW	**PMC_HOST_WAKE_STS (PMC_HOST_WAKE_STS) (pmc_host_wake_sts):** The SOC Power Management Controller sets this bit if it wakes the host for reasons other than typical host-visible wake events. This status bit provides information to BIOS that the PMC caused the wake.
3:0	0b RO	**reserved2:** Reserved.

27.7.2 PM_CFG - Power Management Configuration (PMC_CFG)—Offset 8h

This register contains misc. fields used to configure the SOC's power management behavior.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PMC_CFG: [PMC_BASE_ADDRESS] + 8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

reserved	sps	no_reboot	sx_ent_to_en	reserved2	timing_t581

Bit Range	Default & Access	Description
31:6	0b RO	**reserved:** Reserved.
5	0b RW	**Shutdown Policy Select (SPS) (sps):** When cleared (default) the SOC will drive INIT# in response to the shutdown Message. When set to 1, SOC will treat the shutdown message similar to receiving a CF9h I/O write, and will drive PMU_PLTRST active. . BIOS guide note: This register is reset any time PMU_PLTRST asserts.
4	0b RW	**No Reboot (NO_REBOOT) (no_reboot):** This bit is set when the No Reboot strap is sampled high on COREPWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.
3	0b RW	**S1/3/4/5 Entry Timeout Enable (SX_ENT_TO_EN) (sx_ent_to_en):** This policy bit determines whether the SOC will apply a timeout to the S1/S3/S4/S5 entry flow. If this timeout is enabled and the entry flow appears to be hung, the SOC will trigger a straight-to-S5 global reset. Encodings: 0: Timeout disabled (default) 1: Timeout enabled reset_type=RSMRST_B
2	0b RO	**reserved (reserved2):** Reserved.
1:0	0b RW	**Timing t581 (TIMING_T581) (timing_t581):** This field configures the t581 timing involved in the power down flow (CPU Power Good indication inactive to PLL Enable inactive). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms reset_type=Resume Well Reset#

27.7.3 VLV_PM_STS - VLV Power Management Status (VLV_PM_STS)—Offset Ch

This register contains misc. fields used to record events pertaining to SOC power management. Unless otherwise indicated, all RWC bits are cleared with a write of 1 by software.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VLV_PM_STS: [PMC_BASE_ADDRESS] + Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

reserved	pmc_msg_full_sts	pmc_msg_4_full_sts	pmc_msg_3_full_sts	pmc_msg_2_full_sts	pmc_msg_1_full_sts	reserved1	code_req	reserved2	hpr_ent_to	sx_ent_to	reserved3

Bit Range	Default & Access	Description
31:25	0b RO	**reserved:** Reserved.
24	0b RO	**PMC Message Full Status (PMC_MSG_FULL_STS) (pmc_msg_full_sts):** 'This bit gets set to 1b automatically when the MTPMC register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
23	0b RO	**PMC Message 4 Full Status (PMC_MSG_4_FULL_STS) (pmc_msg_4_full_sts):** This bit gets set to 1b automatically when the Message to PMC 4 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
22	0b RO	**PMC Message 3 Full Status (PMC_MSG_3_FULL_STS) (pmc_msg_3_full_sts):** This bit gets set to 1b automatically when the Message to PMC 3 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
21	0b RO	**PMC Message 2 Full Status (PMC_MSG_2_FULL_STS) (pmc_msg_2_full_sts):** This bit gets set to 1b automatically when the Message to PMC 2 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
20	0b RO	**PMC Message 1 Full Status (PMC_MSG_1_FULL_STS) (pmc_msg_1_full_sts):** This bit gets set to 1b automatically when the Message to PMC 1 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
19:9	0b RO	**reserved1:** Reserved.
8	0b RO	**Code Requested (CODE_REQ) (code_req):** PMC will set this bit when SEC unit requests exclusion from power flows
7:3	0b RO	**reserved2:** Reserved.
2	0b RW	**Host Partition Reset Entry Timeout (HPR_ENT_TO) (hpr_ent_to):** This bit is set to '1' to record that a global reset was triggered by a timeout during Host partition reset entry sequence.
1	0b RW	**S3/4/5 Entry Timeout (SX_ENT_TO) (sx_ent_to):** This bit is set to '1' to record that a global reset was triggered by a timeout during an S3, S4, or S5 entry sequence.
0	0b RO	**reserved3:** Reserved.

27.7.4 MTPMC - Message to PMC (MTPMC)—Offset 10h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

MTPMC: [PMC_BASE_ADDRESS] + 10h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Field: mtpmc

Bit Range	Default & Access	Description
31:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to any of the bytes in this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. In the case of a message that involves a response from the PMC (such as a PMC XRAM read), the host must also consume any data returned by the PMC in the Message from PMC register (MFPMC) before initiating another message

27.7.5 General PM Configuration 1 (GEN_PMCON1)—Offset 20h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GEN_PMCON1: [PMC_BASE_ADDRESS] + 20h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00004004h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	0 1 0 0	

Fields (bit 31 to bit 0): reserved1, uart_en, disb, RSVD0, mem_sr, srs, cts, ms4v, reserved3, pwr_flr, pme_b0_s5_dis, sus_pwr_flr, wol_en_ovrd, dis_slp_x_strch_sus_up, slp_s3_min_asst_wdth, gen_rst_sts, rtc_reserved, swsmi_ratesel, s4maw, s4ase, rps, reserved, ag3e

Bit Range	Default & Access	Description
31:25	0b RO	**reserved1:** Reserved.
24	0b RW	**UART Enable (UART_EN) (uart_en):** When set, PMC enables UART debug port

Bit Range	Default & Access	Description
23	0b RW	**DRAM Initialization Scratchpad Bit (DISB) (disb):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by the assertion of the RSMRST_B pin.
22	0b RO	**RSVD0:** Reserved
21	0b RO	**Memory Placed in Self-Refresh (MEM_SR) (mem_sr):** This bit will be set to 1 if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry and exit - successful Host partition reset without power cycle This bit will be cleared whenever the SOC begins a transition out of S0. Note: This bit should not be consulted upon wake from S1, as that state does not involve the same type of handshake or placing memory into Self-Refresh. It is assumed that software is already aware that memory context is not impacted by S1 and therefore does not need to check this bit. reset_type=global reset
20	0b RW	**System Reset Status (SRS) (srs):** SOC sets this bit when the PMU_RESETBUTTON_B# button is pressed. BIOS is expected to read this bit and clear it if it is set. This bit is also reset by RSMRST_B and CF9h resets. reset_type=Resume Well Reset#
19	0b RW	**CPU Thermal Trip Status (CTS) (cts):** This bit is set when the SOC thermal trip active while the system is in a valid state to honor the pin. This bit is also reset by RSMRST_B and CF9h resets. It is not reset by the shutdown and reboot associated with the thermal trip event. reset_type=Resume Well Reset#
18	0b RW	**Minimum PMU_SLP_S4_B Assertion Width Violation Status (MS4V) (ms4v):** Hardware sets this bit when the PMU_SLP_S4_B assertion width is less than the time programmed in the PMU_SLP_S4_B Minimum Assertion Width field. The SOC begins the timer when PMU_SLP_S4_B pin is asserted during S4/S5 entry, or when the RSMRST_B input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the PMU_SLP_S4_B Assertion Stretch Enable and the Disable-SLP_X-Stretching-After-SUS-Power-Failure bits. This bit is reset by the assertion of the RSMRST_B pin, but can be set in some cases before the default value is readable. reset_type=RSMRST_B
17	0b RO	**reserved3:** Reserved.
16	0b RW	**COREPWROK Failure (PWR_FLR) (pwr_flr):** Intel SOC sets this bit any time COREPWROK goes low if the system was in an S0 or S1 state. The bit will be cleared only by software writing a 1 back to the bit or by SUS well power loss. reset_type=global reset
15	0b RW	**PME B0 S5 Disable (PME_B0_S5_DIS) (pme_b0_s5_dis):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake N = Don't wake B0 = PME_B0_EN OV = WOL Enable Override B0/OV | S1/S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the SRTCRST_B pin. reset_type=SRTCRST_B
14	1b RW	**SUS Well Power Failure (SUS_PWR_FLR) (sus_pwr_flr):** This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST_B assertion. Software writes a 1 to this bit to clear it. This bit is in the SUS well, and defaults to '1' based on RSMRST_B assertion (not cleared by any type of reset). Implementation Note: RSMRST_B is an asynchronous set term to this bit. reset_type=RSMRST_B

Bit Range	Default & Access	Description
13	0b RW	**WOL Enable Override (WOL_EN_OVRD) (wol_en_ovrd):** When this bit is set to 1, the integrated LAN is enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0a_EN register. This allows the system BIOS to enable Wake-On-LAN regardless of the policies selected through the operating system. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) When this bit is cleared to 0, the wake-on-LAN policies are determined by OS-visible bits. This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by the SRTCRST_B pin reset_type=SRTCRST_B
12	0b RW	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP) (dis_slp_x_strch_sus_up):** When this bit is set to 1, all SLP_* pin stretching is disabled when powering up after a SUS well power loss. When this bit is left at 0, SLP_* stretching will be performed after SUS power failure as enabled in various other fields. Note that if this bit is a 0, SLP_* stretch timers start on SUS well power up (the SOC has no ability to count stretch time while the SUS well is powered down). Setting this bit can therefore prevent long delays after SUS power loss which may be common in mobile platforms and in manufacturing flow testing, while still allowing for the full power cycling during S3, S4 and S5 states. If the platform guarantees minimum SUS power down residence in other ways, an additional SOC-induced delay is not needed or wanted. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the SRTCRST_B pin.
11:10	0b RW	**PMU_SLP_S3_B Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH) (slp_s3_min_asst_wdth):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S3_B signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the RSMRST_B pin. reset_type=RSMRST_B
9	0b RW	**General Reset Status (GEN_RST_STS) (gen_rst_sts):** This bit is set by hardware whenever PMU_PLTRST asserts for any reason other than going into a software-entered sleep state (via PM1_CNT.SLP_EN write). This bit is an optional tool to help BIOS determine when a reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determing what action to take based on reading PM1_STS.WAK_STS = '1'. If GEN_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect SOC operation in any way, and can therefore be left set if BIOS chooses not to use it. This bit is set by global reset. reset_type=global reset
8	0b RW	**RTC_reserved (rtc_reserved):** reset_type=SRTCRST_B
7:6	0b RW	**SWSMI Rate Select (SWSMI_RATESEL) (swsmi_ratesel):** This 2-bit value indicates when the SWSMI timer will time out. Valid values are: 00 1.5ms +/- 0.6ms 01 16ms +/- 4ms 10 32ms +/- 4ms 11 64ms +/- 4ms These bits are not cleared by any type of reset except SRTCRST_B.
5:4	0b RW	**PMU_SLP_S4_B Minimum Assertion Width (S4MAW) (s4maw):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S4_B signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: - 11: 1 second - 10: 2 seconds - 01: 3 seconds - 00: 4 seconds This value is used in two ways: 1. If the PMU_SLP_S4_B assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the PMU_SLP_S4_B signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failure bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. SRTCRST_B forces this field to the conservative default state (00b). reset_type=SRTCRST_B

Bit Range	Default & Access	Description
3	0b RW	**PMU_SLP_S4_B Assertion Stretch Enable (S4ASE) (s4ase):** When set to 1, the PMU_SLP_S4_B pin will minimally assert for the time specified in bits 5:4 of this register. This bit is provided so that all DIMMs in the system can deterministically detect a power-cycle event for proper initialization. Note that there are behavioral changes that may be noticeable to the end-user when this bit is set. Resume times from S4 and S5 and power-up times from G3 may be delayed by several seconds. Cases in which this feature may not be desirable and therefore keeping the bit cleared are: - A customer decides the user confusion due to the hardware delay is a bigger issue than the potential DRAM issue - A customer decides the software status bit solution is adequate - A different DRAM type is used or the platform provides an external solution to solve the power-cycling issue - Validation regressions are impacted by the delay (especially after RSMRST_B deassertion) - Avoid potential resume time WHQL violations This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by SRTCRST_B. reset_type=SRTCRST_B
2	1b RW	**RTC_PWR_STS (RPS) (rps):** Intel SOC will set this bit to 1 when RTEST_B indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset. reset_type=RTEST_B
1	0b RO	**reserved:** Reserved.
0	0b RW	**AFTERG3_EN (AG3E) (ag3e):** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by SRTCRST_B assertion. reset_type=SRTCRST_B

27.7.6 General PM Configuration 2 (GEN_PMCON2)—Offset 24h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GEN_PMCON2: [PMC_BASE_ADDRESS] + 24h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31:19	reserved4
18	slpsx_str_pol_lock
17:11	reserved3
10	bios_pci_exp_en
9	pwrbtn_lvl
8:5	reserved1
4	smi_lock
3:2	reserved
1:0	per_smi_sel

Bit Range	Default & Access	Description
31:19	0b RO	**reserved (reserved4):** Reserved.

Bit Range	Default & Access	Description
18	0b RW	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK) (slpsx_str_pol_lock):** When set to 1, this bit locks down the following fields: - GEN_PMCON_1.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON_1.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_1.S4MAW - GEN_PMCON_1.S4ASE Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.
17:11	0b RO	**reserved (reserved3):** Reserved.
10	0b RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN) (bios_pci_exp_en):** This bit acts as a global enable for the SCI associated with the PCI express ports. If this bit is not set, then the various PCI Express ports cannot cause the PCI_EXP_STS bit to go active.
9	0b RO	**Power Button Level (PWRBTN_LVL) (pwrbtn_lvl):** This read-only bit indicates the current state of the PMU_PWRBTN_B signal. 1= High, 0 = Low. The value reflected in this bit is the debounced PMU_PWRBTN_B pin value that is seen at the output of a 16ms debouncer.
8:5	0b RO	**reserved (reserved1):** Reserved.
4	0b RW	**SMI Lock (SMI_LOCK) (smi_lock):** When this bit is set, writes to the GBL_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by PMU_PLTRST).
3:2	0b RO	**reserved:** Reserved.
1:0	0b RW	**Period SMI Select (PER_SMI_SEL) (per_smi_sel):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (default), 01 = 32 seconds, 10 = 16 seconds, 11 = 8 seconds Tolerance for the timer is +/- 1 second.

27.7.7 MFPMC - Message from PMC (MFPMC)—Offset 28h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MFPMC: [PMC_BASE_ADDRESS] + 28h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

mfpmc_bits

Bit Range	Default & Access	Description
31:0	0b RW	**Message from PMC (MFPMC) (mfpmc_bits):** The data in this register is typically updated in response to a host write to the MTPMC register.

27.7.8 SEC_STS - SEC Status (SEC_STS)—Offset 2Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SEC_STS: [PMC_BASE_ADDRESS] + 2Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:4	Bits 3:0
reserved	sec_exclusion_cause

Bit Range	Default & Access	Description
31:4	0b RO	**reserved:** Reserved.
3:0	0b RW	**SEC_EXCLUSION_CAUSE (sec_exclusion_cause):** The cause associated with SeC setting requesting exclusion from power flows in SEC_EXCLUSION_REQ field. 0000b: SeC FW Fault Tolerant Initialization failed. 0001b: SeC FLASH Descriptor Override invoked. 0010b: SeC disabled using SW means (such as OEM setting). 0011b: Post-boot SeC applications not supported. 0100b: ROM BIST failure. 0101b: Fuse unit completed with unsupported request for group 1. 0110b: Invalid fuses bit at line 3 of group 1 fuses wasn't written with value 0. 0111b: DRAM Initializaiton by BIOS failed. Other values reserved.

27.7.9 Configured Revision ID (CRID)—Offset 30h

Note: Configure by Bios Code. Please contact Intel representative if you have questions on CRID support

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRID: [PMC_BASE_ADDRESS] + 30h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:2	Bits 1:0
reserved	rid_sel

Bit Range	Default & Access	Description
31:2	0b RO	**reserved:** Reserved.
1:0	0b RW	**RID Select(RID_SEL) (rid_sel):** Software writes this field to select the Revision ID reflected in PCI config space. The decoding is: 00 - Revision ID 01 - CRID 0 10 - CRID 1 11 - CRID 2 Once written, this field can only be cleared by a platform reset. reset_type=PMU_PLTRST

27.7.10 Function Disable (FUNC_DIS)—Offset 34h

BIOS uses this register to disable specific function. Upon writing this register PMC will set the corresponding Function Disable bit in the PSF

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FUNC_DIS: [PMC_BASE_ADDRESS] + 34h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

func_dis_bits

Bit Range	Default & Access	Description
31:0	0b RW	**FUNC_DIS_BITS (func_dis_bits):** When a bit is set, the corresponding function should be disabled. 31 LPSS2_F7_Disable LPSS2 Function7 (I2C#7) Disable. 1'b1: Disable 1'b0: Enable 30 LPSS2_F6_Disable LPSS2 Function6 (I2C#6) Disable. 1'b1: Disable 1'b0: Enable 29 LPSS2_F5_Disable LPSS2 Function5 (I2C#5) Disable. 1'b1: Disable 1'b0: Enable 28 LPSS2_F4_Disable LPSS2 Function4 (I2C#4) Disable. 1'b1: Disable 1'b0: Enable 27 LPSS2_F3_Disable LPSS2 Function3 (I2C#3) Disable. 1'b1: Disable 1'b0: Enable 26 LPSS2_F2_Disable LPSS2 Function2 (I2C#2) Disable. 1'b1: Disable 1'b0: Enable 25 LPSS2_F1_Disable LPSS2 Function1 (I2C#1) Disable. 1'b1: Disable 1'b0: Enable 24 LPSS2_F0_Disable LPSS2 Function0 (DMA) Disable. 1'b1: Disable 1'b0: Enable 23 PCIe_P3_Disable PCIe Port3 Disable. 1'b1: Disable 1'b0: Enable 22 PCIe_P2_Disable PCIe Port2 Disable. 1'b1: Disable 1'b0: Enable 21 PCIe_P1_Disable PCIe Port1 Disable. 1'b1: Disable 1'b0: Enable 20 PCIe_P0_Disable PCIe Port0 Disable. 1'b1: Disable 1'b0: Enable 19 Reserved2 reserved 18 USB_Disable USB2 (EHCI) Disable. 1'b1: Disable 1'b0: Enable 17 SATA_Disable SATA Disable. 1'b1: Disable 1'b0: Enable 16 LAN_Disable LAN Disable. 1'b1: Disable 1'b0: Enable 15 USH_Disable USH Disable. 1'b1: Disable 1'b0: Enable 14 OTG_Disable OTG Disable. 1'b1: Disable 1'b0: Enable 13 LPE_Disable LPE Disable. 1'b1: Disable 1'b0: Enable 12 HDA_Disable HDA Disable. 1'b1: Disable 1'b0: Enable 11 SCC_MIPI_Disable MIPI-HSI Disable. 1'b1: Disable 1'b0: Enable 10 SCC_SDCARD_Disable SDCARD Disable. 1'b1: Disable 1'b0: Enable 9 SCC_SDIO_Disable SDIO Disable. 1'b1: Disable 1'b0: Enable 8 SCC_eMMC_Disable eMMC Disable. 1'b1: Disable 1'b0: Enable 7 LPSS1_F7_Disable Reserved for LPSS1 function 7 6 LPSS1_F6_Disable Reserved for LPSS1 function 6 5 LPSS1_F5_Disable PSS1 Function5 (SPI) Disable. 1'b1: Disable 1'b0: Enable 4 LPSS1_F4_Disable LPSS1 Function4 (HSUART#2) Disable. 1'b1: Disable 1'b0: Enable 3 LPSS1_F3_Disable LPSS1 Function3 (HSUART#1) Disable. 1'b1: Disable 1'b0: Enable 2 LPSS1_F2_Disable LPSS1 Function2 (PWM#2) Disable. 1'b1: Disable 1'b0: Enable 1 LPSS1_F1_Disable LPSS1 Function1 (PWM#1) Disable. 1'b1: Disable 1'b0: Enable 0 LPSS1_F0_Disable LPSS1 Function0 (DMA) Disable. 1'b1: Disable 1'b0: Enable

27.7.11 Function Disable 2 (FUNC_DIS_2)—Offset 38h

BIOS uses this register to disable specific function. Upon writing this register PMC will set the corresponding Function Disable bit in the PSF

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FUNC_DIS_2: [PMC_BASE_ADDRESS] + 38h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																													ush_ss_phy_dis	otg_ss_phy_dis	smb_dis

Bit Range	Default & Access	Description
31:3	0b RO	**RSVD0:** Reserved
2	0b RW	**USH_SS_PHY_DIS (ush_ss_phy_dis):** When this bit is set, USH Super Speed PHY should be disabled.
1	0b RW	**OTG_SS_PHY_DIS (otg_ss_phy_dis):** When this bit is set, OTG Super Speed PHY should be disabled.
0	0b RW	**SMB_DIS (smb_dis):** When this bit is set, SMB function should be disabled.

27.7.12 S0ix wake enable (S0IX_WAKE_EN)—Offset 3Ch

This register contains wake enable bit per S0ix wake event. Note: Common wake events with sleep sates have their wake enables in the ACPI space.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0IX_WAKE_EN: [PMC_BASE_ADDRESS] + 3Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00FFFFFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
reserved								wake_en_23	wake_en_22	wake_en_21	wake_en_20	wake_en_19	wake_en_18	wake_en_17	wake_en_16	wake_en_15	wake_en_14	wake_en_13	wake_en_12	wake_en_11	wake_en_10	wake_en_9	wake_en_8	wake_en_7	wake_en_6	wake_en_5	wake_en_4	wake_en_3	wake_en_2	wake_en_1	wake_en_0

Bit Range	Default & Access	Description
31:24	0b RO	**Reserved (reserved):** Reserved.
23	1b RW	**WAKE_EN_23 (wake_en_23):** wake enable bit 23 - Spare bit
22	1b RW	**WAKE_EN_22 (wake_en_22):** wake enable bit 22 - Spare bit
21	1b RW	**WAKE_EN_21 (wake_en_21):** wake enable bit 21 - Spare bit
20	1b RW	**WAKE_EN_20 (wake_en_20):** wake enable bit 20 - Shared IRQ from GPSS
19	1b RW	**WAKE_EN_19 (wake_en_19):** wake enable bit 19 - Ored dedicated IRQs from GPSC
18	1b RW	**WAKE_EN_18 (wake_en_18):** wake enable bit 18 - Ored dedicated IRQs from GPSS
17	1b RW	**WAKE_EN_17 (wake_en_17):** wake enable bit 17 - Wake LAN
16	1b RW	**WAKE_EN_16 (wake_en_16):** wake enable bit 16 - Pending NMI
15	1b RW	**WAKE_EN_15 (wake_en_15):** wake enable bit 15 - SCI
14	1b RW	**WAKE_EN_14 (wake_en_14):** wake enable bit 14 - SMI
13	1b RW	**WAKE_EN_13 (wake_en_13):** wake enable bit 13 - OTG wake
12	1b RW	**WAKE_EN_12 (wake_en_12):** wake enable bit 12 - AONT Si03 wake
11	1b RW	**WAKE_EN_11 (wake_en_11):** wake enable bit 11 - AONT Si02 wake
10	1b RW	**WAKE_EN_10 (wake_en_10):** wake enable bit 10 - AONT Si01 wake
9	1b RW	**WAKE_EN_9 (wake_en_9):** wake enable bit 9 - IOAPIC delivery status
8	1b RW	**WAKE_EN_8 (wake_en_8):** wake enable bit 8 - Shared IRQ from GPNC
7	1b RW	**WAKE_EN_7 (wake_en_7):** wake enable bit 7 - GPE from GPSS
6	1b RW	**WAKE_EN_6 (wake_en_6):** wake enable bit 6 - GPE from GPSC
5	1b RW	**WAKE_EN_5 (wake_en_5):** wake enable bit 5 - Shared IRQ from GPSC
4	1b RW	**WAKE_EN_4 (wake_en_4):** wake enable bit 4 - LPC Clock run
3	1b RW	**WAKE_EN_3 (wake_en_3):** wake enable bit 3 - SEC Timers
2	1b RW	**WAKE_EN_2 (wake_en_2):** wake enable bit 2 - LPE IPC

Bit Range	Default & Access	Description
1	1b RW	**WAKE_EN_1 (wake_en_1):** wake enable bit 1 - LPE wake
0	1b RW	**WAKE_EN_0 (wake_en_0):** wake enable bit 0 - NFC wake

27.7.13 S0ix wake Status (S0IX_WAKE_STS)—Offset 40h

This register contains wake status bits per S0ix wake event. Note: Common wake events with sleep sates have their wake enables in the ACPI space.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0IX_WAKE_STS: [PMC_BASE_ADDRESS] + 40h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved								wake_sts_23	wake_sts_22	wake_sts_21	wake_sts_20	wake_sts_19	wake_sts_18	wake_sts_17	wake_sts_16	wake_sts_15	wake_sts_14	wake_sts_13	wake_sts_12	wake_sts_11	wake_sts_10	wake_sts_9	wake_sts_8	wake_sts_7	wake_sts_6	wake_sts_5	wake_sts_4	wake_sts_3	wake_sts_2	wake_sts_1	wake_sts_0

Bit Range	Default & Access	Description
31:24	0b RO	**Reserved (reserved):** Reserved.
23	0b RW	**WAKE_STS_23 (wake_sts_23):** wake status bit 23 - Spare bit
22	0b RW	**WAKE_STS_22 (wake_sts_22):** wake status bit 22 - Spare bit
21	0b RW	**WAKE_STS_21 (wake_sts_21):** wake status bit 21 - Spare bit
20	0b RW	**WAKE_STS_20 (wake_sts_20):** wake status bit 20- Shared IRQ from GPSS
19	0b RW	**WAKE_STS_19 (wake_sts_19):** wake status bit 19 - Ored dedicated IRQs from GPSC
18	0b RW	**WAKE_STS_18 (wake_sts_18):** wake status bit 18 - Ored dedicated IRQs from GPSS
17	0b RW	**WAKE_STS_17 (wake_sts_17):** wake status bit 17 - Wake LAN
16	0b RW	**WAKE_STS_16 (wake_sts_16):** wake status bit 16 - Pending NMI
15	0b RW	**WAKE_STS_15 (wake_sts_15):** wake status bit 15 - SCI

Bit Range	Default & Access	Description
14	0b RW	**WAKE_STS_14 (wake_sts_14):** wake status bit 14 - SMI
13	0b RW	**WAKE_STS_13 (wake_sts_13):** wake status bit 13 - OTG wake
12	0b RW	**WAKE_STS_12 (wake_sts_12):** wake status bit 12 - AONT Si03 wake
11	0b RW	**WAKE_STS_11 (wake_sts_11):** wake status bit 11 - AONT Si02 wake
10	0b RW	**WAKE_STS_10 (wake_sts_10):** wake status bit 10 - AONT Si01 wake
9	0b RW	**WAKE_STS_9 (wake_sts_9):** wake status bit 9 - IOAPIC delivery status
8	0b RW	**WAKE_STS_8 (wake_sts_8):** wake status bit 8 - Shared IRQ from GPNC
7	0b RW	**WAKE_STS_7 (wake_sts_7):** wake status bit 7 - GPE from GPSS
6	0b RW	**WAKE_STS_6 (wake_sts_6):** wake status bit 6- GPE from GPSC
5	0b RW	**WAKE_STS_5 (wake_sts_5):** wake status bit 5 - Shared IRQ from GPSC
4	0b RW	**WAKE_STS_4 (wake_sts_4):** wake status bit 4 - LPC Clock run
3	0b RW	**WAKE_STS_3 (wake_sts_3):** wake status bit 3 - SEC Timers
2	0b RW	**WAKE_STS_2 (wake_sts_2):** wake status bit 2 - LPE IPC
1	0b RW	**WAKE_STS_1 (wake_sts_1):** wake status bit 1 - LPE wake
0	0b RW	**WAKE_STS_0 (wake_sts_0):** wake status bit 0 - NFC wake

27.7.14 S0ix control (S0IX_CTL)—Offset 44h

This register contains S0ix miscellaneous controls

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

S0IX_CTL: [PMC_BASE_ADDRESS] + 44h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000050h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Default	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1	0 0 0 0
Field	reserved	reserved	reserved	reserved	reserved	reserved	s0ix_rail_ramp	s0ix_rail_ramp

Bit Range	Default & Access	Description
31:8	0b RO	**Reserved (reserved):** Reserved.
7:0	50h RW	**S0IX_RAIL_RAMP (s0ix_rail_ramp):** specifies S0IX rail ramp time

27.7.15 ETR - Extended Test Mode Register (ETR)—Offset 48h

This register resides in the resume well. All bits except bit[23:16] are reset by internal Resume Well Reset. Bit[23:16] are reset by RSMRST_B only.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

ETR: [PMC_BASE_ADDRESS] + 48h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00230000h

Bits	31	30:23	22	21	20	19	18	17:16	15:0
Default	0	0 0 0 0 0 0 0 0	0	1	0	0	0	1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Field	cf9lock	reserved	ltr_def	ignore_hpet	cf9gr	reserved1	cworwre	max_s0ix	reserved2

Bit Range	Default & Access	Description
31	0b RW	**CF9h Lockdown (CF9LOCK) (cf9lock):** When set, this will lock the CF9h-Global-Reset bit. When set, this register locks itself. This register is reset by a CF9h reset.
30:23	0b RO	**reserved:** Reserved.
22	0b RW	**LTR default (LTR_DEF) (ltr_def):** When this bit is cleared, PMC will assume low LTR by default. When set, PMC will assume high LTR by default
21	1b RW	**Ignore HPET When going to S0i2 (IGNORE_HPET) (ignore_hpet):** When this bit is set, PMC will not check for HPET disabled before going to S0i2
20	0b RW	**CF9h Global Reset (CF9GR) (cf9gr):** When this bit is set, a CF9h write of 6h or Eh will cause a Global Reset of the Host partition. If this bit is cleared, a CF9h write of 6h or Eh will only reset the Host partition. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS. When this bit is set, the hardware assumes that bit 18 (CF9h Without Resume Well Reset Enable) is cleared. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset. reset_type=RSMRST_B

Bit Range	Default & Access	Description
19	0b RO	**reserved (reserved1):** Reserved.
18	0b RW	**CF9h Without Resume Well Reset Enable (CWORWRE) (cworwre):** When this bit is set, a CF9h write of 6h or Eh will not cause internal Resume Well Reset (WrsmrstB) to be asserted and thus resume well logic will maintain its state. When this bit is cleared, CF9h write of 6h or Eh will also reset resume well logic. This bit is to be used when a second reset through CF9 write is desired upon power up or after resume from low power states. This bit has to be set prior to the write to CF9 register and has to be cleared upon completing the reset. Failing to do so prevents resume well registers from being reset in the future CF9 writes. reset_type=RSMRST_B
17:16	11b RW	**MAX_S0IX (MAX_S0IX (max_s0ix):** Indicated the maximum S0i state SOC can go
15:0	0b RO	**reserved (reserved2):** Reserved.

27.7.16 VLT - Voltage Detect Register (VLT)—Offset 50h

This register reflects the Voltage detect fuses.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

VLT: [PMC_BASE_ADDRESS] + 50h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																								vlt_fuses							

Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RO	**VLT Fuses (VLT_FUSES) (vlt_fuses):** These bits reflects the Voltage detect fuses

27.7.17 GPIO_ROUT - GPIO_ROUT register (GPIO_ROUT)—Offset 58h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GPIO_ROUT: [PMC_BASE_ADDRESS] + 58h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

gpio_rout

Bit Range	Default & Access	Description
31:0	0b RW	**GPIO Rout (GPIO_ROUT) (gpio_rout):** Bits [15:0] determines GPIO SUS events rout. Bits [31:16] determines GPIO CORE events rout. Bits [1:0] determines GPIO SUS event 0. Bits [3:2] determines GPIO SUS event 1 and so on. Bits [17:16] determines GPIO CORE event 0. Bits [19:18] determines GPIO CORE event 1 and so on. If the corresponding GPIO is implemented and is set to an input, a '1' in the GP_LVL bit can be routed to cause an interrupt. If the GPIO is not set to an input, this field has no effect. * 00 No effect (or GPIO unimplemented), * 01 SMI# (if corresponding ALT_GPIO_SMI bit also set), * 10 SCI (if corresponding GPE0a_EN bit also set), * 11 Reserved If the system is in an S0-S5 state and if the GPE0a_EN bit is also set, then the GPIO can cause a Wake event, even if the GPIO is NOT routed to cause an interrupt. Exception: If the system is in S5 state due to a powerbutton override, then the GPIO's will not cause wake events. Note: Core well GPIO's are not capable of waking the system from sleep states where the core well is not powered.

27.7.18 PLT_CLK_CTL_0 - Platform Clock Control 0 (PLT_CLK_CTL_0)—Offset 60h

This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_0: [PMC_BASE_ADDRESS] + 60h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

reserved5 | clk_freq | clk_ctl

Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

27.7.19 PLT_CLK_CTL_1 - Platform Clock Control 1 (PLT_CLK_CTL_1)—Offset 64h

This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_1: [PMC_BASE_ADDRESS] + 64h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	
reserved5																													clk_freq	clk_ctl	

Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

27.7.20 PLT_CLK_CTL_2 - Platform Clock Control 2 (PLT_CLK_CTL_2)—Offset 68h

This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_2: [PMC_BASE_ADDRESS] + 68h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	
reserved5																													clk_freq	clk_ctl	

Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.

Bit Range	Default & Access	Description
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

27.7.21 PLT_CLK_CTL_3 - Platform Clock Control 3 (PLT_CLK_CTL_3)—Offset 6Ch

This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PLT_CLK_CTL_3: [PMC_BASE_ADDRESS] + 6Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
reserved5																													clk_freq	clk_ctl	

Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

27.7.22 PLT_CLK_CTL_4 - Platform Clock Control 4 (PLT_CLK_CTL_4)—Offset 70h

This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PLT_CLK_CTL_4: [PMC_BASE_ADDRESS] + 70h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
reserved5																													clk_freq	clk_ctl	

Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

27.7.23 PLT_CLK_CTL_5 - Platform Clock Control 5 (PLT_CLK_CTL_5)—Offset 74h

This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PLT_CLK_CTL_5: [PMC_BASE_ADDRESS] + 74h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
reserved5																													clk_freq	clk_ctl	

Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

27.7.24 S0IR_TMR - S0I Ready Residency Timer (S0IR_TMR)—Offset 80h

This timer acumulates time spent in S0I Ready state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0IR_TMR: [PMC_BASE_ADDRESS] + 80h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rtime																															

Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I Ready state, in units of 32 uS

27.7.25 S0I1_TMR - S0I1 Residency Timer (S0I1_TMR)—Offset 84h

This timer acumulates time spent in S0I1 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0I1_TMR: [PMC_BASE_ADDRESS] + 84h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rtime																															

Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I1 state, in units of 32 uS

27.7.26 S0I2_TMR - S0I2 Residency Timer (S0I2_TMR)—Offset 88h

This timer acumulates time spent in S0I2 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0I2_TMR: [PMC_BASE_ADDRESS] + 88h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

rtime

Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I2 state, in units of 32 uS

27.7.27 S0I3_TMR - S0I3 Residency Timer (S0I3_TMR)—Offset 8Ch

This timer acumulates time spent in S0I3 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0I3_TMR: [PMC_BASE_ADDRESS] + 8Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

rtime

Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I3 state, in units of 32 uS

27.7.28 S0_TMR - S0 Residency Timer (S0_TMR)—Offset 90h

This timer acumulates time spent in S0 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0_TMR: [PMC_BASE_ADDRESS] + 90h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

rtime

Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0 state, in units of 32 uS

27.7.29 PSS - Power island Power Status (PSS)—Offset 98h

This register reflects the power status for each physical power island controlled by PMC. note it doesnt reflect the tap override values

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PSS: [PMC_BASE_ADDRESS] + 98h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved | pg_sts

Bit Range	Default & Access	Description
31:18	0b RO	**reserved:** Reserved.
17:0	0b RO	**PG_STS (POWER GATE status) (pg_sts):** reflects the power gate status of all power islands 0 - power island is powered on. 1 - power island is powered off bits mapping: 0 - GBE 1 - SATA 2 - HDA 3 - SEC 4 - PCIE 5 - LPSS 6 - LPE 7 - DFX 8 - USH control 9 - USH SUS 10 - USH VCCS 11 - USH VCCA 12 - OTG control 13 - OTG VCCS 14 - OTG VCCACLK 15 - OTG VCCA 16 - USB 17 - USB SUS

27.7.30 D3_STS_0 - D3 Status register 0 (D3_STS_0)—Offset A0h

This register reflects D3 status of functions

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STS_0: [PMC_BASE_ADDRESS] + A0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

d3_sts (bits 31:0)

Bit Range	Default & Access	Description
31:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - MIPI 12 - HDA 13 - LPE 14 - OTG 15 - USH 16 - GBE 17 - SATA 18 - USB 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7

27.7.31 D3_STS_1 - D3 Status register 1 (D3_STS_1)—Offset A4h

This register reflects D3 status of functions

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STS_1: [PMC_BASE_ADDRESS] + A4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved (bits 31:2), d3_sts (bits 1:0)

Bit Range	Default & Access	Description
31:2	0b RO	**reserved:** Reserved.
1:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - SMB 1 - USH Super speed PHY 2 - OTG Super speed PHY 3 - DFX

27.7.32 D3_STDBY_STS_0 - D3 Standby Status register 0 (D3_STDBY_STS_0)—Offset A8h

This register reflects D3 status of functions at the moment standby ready message received

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STDBY_STS_0: [PMC_BASE_ADDRESS] + A8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Field: d3_sts (bits 31:0)

Bit Range	Default & Access	Description
31:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - MIPI 12 - HDA 13 - LPE 14 - OTG 15 - USH 16 - GBE 17 - SATA 18 - HDA 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7

27.7.33 D3_STDBY_STS_1 - D3 Standby Status register 1 (D3_STDBY_STS_1)—Offset ACh

This register reflects D3 status of functions at the moment Standby Ready Message was received

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STDBY_STS_1: [PMC_BASE_ADDRESS] + ACh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: reserved (bits 31:2), psf_idle_sts (bit 1), d3_sts (bit 0)

Bit Range	Default & Access	Description
31:3	0b RO	**reserved:** Reserved.
2	0b RO	**PSF IDLE (status) (psf_idle_sts):** Reflect if S0IX flow was stoped because PSF isnt IDLE
1:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - SMB 1 - USH Super speed PHY 2 - OTG Super speed PHY 3 - DFX

27.7.34 MTPMC_1 - Message to PMC 1 (MTPMC_1)—Offset B0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

MTPMC_1: [PMC_BASE_ADDRESS] + B0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

Bits	31:8	7:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0	0	0
Field	reserved	mtpmc	lock_exi	ush_exi_en	otg_exi_en

Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:3	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS
2	0b RW	**LOCK EXI (lock_exi):** This field locks the ush_exi_en and otg_exi_en fields. The lock is soft lock, meaning register value will be changed but FW will keep the value on inturnal register GP1[2] until warm reset
1	0b RW	**USH_EXI_Enable (ush_exi_en):** A write to this field causes an interrupt to the PMC. The PMC FW will read the contents of this register and will set pcu_ush_exi_enable_xttnfwh signal. This will prevent USH PIMA power down upon S0IX entery. The host must wait until the PMC has taken action, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS. This field will be copied to FW internal register and it will hold the value until global reset.
0	0b RW	**OTG_EXI_Enable (otg_exi_en):** A write to this field causes an interrupt to the PMC. The PMC FW will read the contents of this register and will set pcu_otg_exi_enable_xttnfwh signal. This will prevent OTG PIMA power down upon S0IX entery. The host must wait until the PMC has taken action, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS. This field will be copied to FW internal register and it will hold the value until global reset

27.7.35 MTPMC_2 - Message to PMC 2 (MTPMC_2)—Offset B4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

MTPMC_2: [PMC_BASE_ADDRESS] + B4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																								mtpmc							

Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_2_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

27.7.36 MTPMC_3 - Message to PMC 3 (MTPMC_3)—Offset B8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

MTPMC_3: [PMC_BASE_ADDRESS] + B8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																								mtpmc							

Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_3_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

27.7.37 MTPMC_4 - Message to PMC 4 (MTPMC_4)—Offset BCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

MTPMC_4: [PMC_BASE_ADDRESS] + BCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																								mtpmc							

Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_4_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

27.7.38 PME Status 0 - Status bit for PME messages (PME_STS)—Offset C0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

PME_STS: [PMC_BASE_ADDRESS] + C0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																				pme_sts											

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11:0	0b RO	**PME Status (pme_sts):** when set PME was recived from the following agents 0 = GBE 1 = HDA 2 = SATA 3 = SCCSDIO 4 = SCCSDCARD 5 = LPSDIO1; 6 = SECEP 7 = LPE 8 = LPSDIO2 9 = OTG 10 = SCCEMMC 11 = SCCMIPIHSI

27.7.39 GPE Level Edge mode (GPE_LEVEL_EDGE)—Offset C4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GPE_LEVEL_EDGE: [PMC_BASE_ADDRESS] + C4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:16) | gpe_level_edge (bits 15:0)

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0b RW	**Edge Level mode (gpe_level_edge):** When set GPE is in level mode when clear GPE is in edge mode gpe_level_edge[15:8] used for GPIO Core gpe_level_edge[7:0] used for GPIO SUS

27.7.40 GPE polarity mode (GPE_POLARITY)—Offset C8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

GPE_POLARITY: [PMC_BASE_ADDRESS] + C8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:16) | gpe_polarity (bits 15:0)

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0b RW	**Polarity (gpe_polarity):** When set GPE is active high when clear GPE is active low gpe_polarity[15:8] used for GPIO Core gpe_polarity[7:0] used for GPIO SUS

27.7.41 Lock Register (LOCK)—Offset CCh

Register Field Lock bit -- GEN_PMCON1 PME_B0_S5_DIS LOCK.Sx_WAKE GEN_PMCON1 WOL_EN_OVRD LOCK.Sx_WAKE GEN_PMCON1 AG3E LOCK.Sx_WAKE GEN_PMCON2 BIOS_PCI_EXP_EN LOCK.PCIE GEN_PMCON2 PER_SMI_SEL LOCK.PER_SMI FUNC_DIS all LOCK.FUNC_DIS FUNC_DIS_2 all LOCK.FUNC_DIS S0IX_WAKE_EN all LOCK.SOIX S0IX_CTL S0IX_RAIL_RAMP LOCK.SOIX ETR IGNORE_HPET LOCK.SOIX ETR MAX_S0IX LOCK.SOIX GPIO_ROUT all LOCK.GPIO_ROUT PLT_CLK_CTL_0 all LOCK.PLT_CLK PLT_CLK_CTL_1 all LOCK.PLT_CLK PLT_CLK_CTL_2 all LOCK.PLT_CLK PLT_CLK_CTL_3 all LOCK.PLT_CLK PLT_CLK_CTL_4 all LOCK.PLT_CLK PLT_CLK_CTL_5 all LOCK.PLT_CLK

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LOCK: [PMC_BASE_ADDRESS] + CCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

Bits	31:7	6	5	4	3	2	1	0
Default	0000 0000 0000 0000 0000 0000 0	0	0	0	0	0	0	0
Field	RSVD0	sx_wake	pcie	per_smi	func_dis	s0ix	gpio_rout	plt_clk

Bit Range	Default & Access	Description
31:7	0b RO	**RSVD0:** Reserved
6	0b RW	**SX_WAKE lock (sx_wake):** Reserved.
5	0b RW	**PCIE lock (pcie):** Reserved.
4	0b RW	**PER_SMI lock (per_smi):** Reserved.
3	0b RW	**FUNC_DIS (func_dis):** Reserved.
2	0b RW	**S0IX lock (s0ix):** Reserved.
1	0b RW	**GPIO_ROUT lock (gpio_rout):** Reserved.
0	0b RW	**PLT_CLK lock (plt_clk):** Reserved.

27.7.42 Virtual UART register (VUART1)—Offset D0h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

VUART1: [PMC_BASE_ADDRESS] + D0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
vuart																															

Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

27.7.43 Virtual UART register (VUART2)—Offset D4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

VUART2: [PMC_BASE_ADDRESS] + D4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
vuart																															

Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

27.7.44 Virtual UART register (VUART3)—Offset D8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

VUART3: [PMC_BASE_ADDRESS] + D8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
vuart																															

Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

27.7.45 Virtual UART register (VUART4)—Offset DCh

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

VUART4: [PMC_BASE_ADDRESS] + DCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

vuart

Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

27.8 SIO HSUART 1 PCI Configuration Registers

Table 285. Summary of HSUART 1 PCI Configuration Registers—0/30/4

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4280	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 4280	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4282	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4282	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 4283	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 4283	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4284	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4285	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4285	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4286	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4286	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4287	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 4288	00000000h

27.8.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

27.8.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:4] + 4h

Default: 00100000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

27.8.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:4] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: CLASS_CODES (bits 31:8), RID (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

27.8.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits) **Offset:** [B:0, D:30, F:4] + Ch

Default: 00800000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: Reserved0 (bits 31:24), MULFNDEV (bit 23), HEADERTYPE (bits 22:16), LATTIMER (bits 15:8), CACHELINE_SIZE (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

27.8.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:4] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:12	11:4	3	2:1	0
BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

27.8.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:4] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:12	11:4	3	2:1	0
BASEADDR1	SIZEINDICATOR1	PREFETCHABLE1	TYPE1	MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

27.8.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 2Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16	15:0
SUBSYSTEMID	SUBSYSTEMVENDORID

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

27.8.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 30h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXPANSION_ROM_BASE

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

27.8.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 34h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved0 (bits 31:8) | CAPPTR_POWER (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

27.8.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 3Ch

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
MAX_LAT								MIN_GNT								Reserved0				INTPIN				INTLINE							

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

27.8.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 80h

Default: 00030001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PMESUPPORT					Reserved0								VERSION			NXTCAP								POWER_CAP							

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

27.8.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Reserved0																PMESTATUS	Reserved1						PMEENABLE	Reserved2				NO_SOFT_RESET	Reserved3	POWERSTATE	

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

27.8.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:4] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

27.9 SIO HSUART 0 Memory Mapped I/O Registers

Table 286. Summary of HSUART 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Receive Buffer Register/Transmit Holding Register/Divisor Latch (Low). (RBR_THR_DLL)—Offset 0h" on page 4290	00000000h
4–7h	4	"Divisor Latch (High)/ Interrupt Enable Register. (IER_DLH)—Offset 4h" on page 4291	00000000h
8–Bh	4	"Interrupt Identification Register and FIFO Control Register. (IIR_FCR)—Offset 8h" on page 4292	00000001h
C–Fh	4	"Line Control Register (LCR)—Offset Ch" on page 4293	00000000h
10–13h	4	"Modem Control Register (MCR)—Offset 10h" on page 4294	00000000h
14–17h	4	"Line Status Register (LSR)—Offset 14h" on page 4295	00000060h
18–1Bh	4	"Modem Status Register (MSR)—Offset 18h" on page 4297	00000000h
1C–1Fh	4	"Scratchpad Register (SCR)—Offset 1Ch" on page 4298	00000000h
30–33h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h" on page 4299	00000000h
34–37h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h" on page 4300	00000000h
38–3Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h" on page 4300	00000000h
3C–3Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch" on page 4301	00000000h
40–43h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h" on page 4301	00000000h
44–47h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h" on page 4302	00000000h
48–4Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h" on page 4302	00000000h
4C–4Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch" on page 4303	00000000h
50–53h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h" on page 4303	00000000h
54–57h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h" on page 4304	00000000h
58–5Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h" on page 4304	00000000h
5C–5Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch" on page 4305	00000000h
60–63h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h" on page 4305	00000000h
64–67h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h" on page 4306	00000000h
68–6Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h" on page 4306	00000000h
6C–6Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch" on page 4307	00000000h
70–73h	4	"FIFO Access Register (FAR)—Offset 70h" on page 4307	00000000h

Table 286. Summary of HSUART 1 Memory Mapped I/O Registers—BAR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
74–77h	4	"Transmit FIFO Read (TFR)—Offset 74h" on page 4308	00000000h
78–7Bh	4	"Receive FIFO Write (RFW)—Offset 78h" on page 4308	00000000h
7C–7Fh	4	"UART Status Register (USR)—Offset 7Ch" on page 4309	00000006h
80–83h	4	"Transmit FIFO Level (TFL)—Offset 80h" on page 4310	00000000h
84–87h	4	"Receive FIFO Level (RFL)—Offset 84h" on page 4310	00000000h
88–8Bh	4	"Software Reset Register (SRR)—Offset 88h" on page 4311	00000000h
8C–8Fh	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 4311	00000000h
90–93h	4	"Shadow Break Control Register (SBCR)—Offset 90h" on page 4312	00000000h
94–97h	4	"Shadow DMA Mode (SDMAM)—Offset 94h" on page 4313	00000000h
98–9Bh	4	"Shadow FIFO Enable (SFE)—Offset 98h" on page 4313	00000000h
9C–9Fh	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 4311	00000000h
A0–A3h	4	"Shadow TX Empty Trigger (STET)—Offset A0h" on page 4314	00000000h
A4–A7h	4	"Halt TX (HTX)—Offset A4h" on page 4315	00000000h
A8–ABh	4	"DMA Software Acknowledge (DMASA)—Offset A8h" on page 4315	00000000h
F4–F7h	4	"Component Parameter Register (CPR)—Offset F4h" on page 4316	00043F32h
F8–FBh	4	"UART Component Version (UCV)—Offset F8h" on page 4317	3330382Ah
FC–FFh	4	"Component Type Register (CTR)—Offset FCh" on page 4318	44570110h
800–803h	4	"Private Clock Params (PRV_CLOCK_PARAMS)—Offset 800h" on page 4318	00000000h
804–807h	4	"Software Resets (RESETS)—Offset 804h" on page 4319	00000000h
808–80Bh	4	"General Purpose Register (GENERAL)—Offset 808h" on page 4319	00000050h
818–81Bh	4	"UART_BYTE_COUNT—Offset 818h" on page 4320	00000000h
820–823h	4	"UART_OVERFLOW_INTR_STAT—Offset 820h" on page 4321	00000000h

27.9.1 Receive Buffer Register/Transmit Holding Register/Divisor Latch (Low). (RBR_THR_DLL)—Offset 0h

Register is used for different purposes depending on the mode. See description details

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
RSVD0	rbr_thr_dll

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**rbr_thr_dll:** RBR[7:0] (Receive Buffer Register) (Read Only): Data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs. THR[7:0] (Transmit Holding Register) (Write Only): Data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. DLL[7:0] (Divisor Latch Low) (Read-Write): Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. this register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest HSUart clock should be allowed to pass before transmitting or receiving data.

27.9.2 Divisor Latch (High)/ Interrupt Enable Register. (IER_DLH)—Offset 4h

Register bits [7:0] is used for different purposes depending on the mode. DLH (Divisor Latch High) Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest HSUart clock should be allowed to pass before transmitting or receiving data.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RSVD0	PTIME_dlh7	RSVD1	EDSSI_dlh3	ELSI_dhl2	ETBEI_dlh1	ERBFI_dlh0

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**PTIME_dlh7:** PTIME (PTIME) This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled
6:4	0b RO	**RSVD1:** Reserved
3	0h RW	**EDSSI_dlh3:** EDSSI (Enable Modem Status Interrupt) This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled
2	0h RW	**ELSI_dhl2:** ELSI (Enable Line Status Interrupt) This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled
1	0h RW	**ETBEI_dlh1:** ETBEI (Enable Transmit Holding Register Empty Interrupt) This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled
0	0h RW	**ERBFI_dlh0:** ERBFI (Enable Received Data Available Interrupt) This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled

27.9.3 Interrupt Identification Register and FIFO Control Register. (IIR_FCR)—Offset 8h

Register is used for different purposes depending on the mode. See description details Interrupt ID [3:0] 0001: No Interrupt Pending 0110: Receiver Line Status (1st Priority) 0100: Receiver Data Available (2nd Priority) 1100: Character Timeout (2nd Priority) 0010: THR Empty (3rd Priority) 0000: Modem Status (4th Priority) 0111: Busy Detect Indication (5th Priority)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000001h

Bits	31:8	7:6	5:4	3	2	1	0
Default	0000 0000 0000 0000 0000 0000	00	00	0	0	0	1
Field	RSVD0	RCVR	TET	DMAM	XFIFOR	RFIFOR	FIFOE

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:6	0h RW	**FIFOSE_RCVR (RCVR):** FIFOSE (FIFOs Enabled) This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. The following trigger levels are supported: • 00 = 1 character in the FIFO • 01 = FIFO full • 10 = FIFO full • 11 = FIFO 2 less than full
5:4	0h RW	**Res_TET (TET):** TX Empty Trigger. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. The following trigger levels are supported: • 00 = FIFO empty • 01 = 2 characters in the FIFO • 10 = FIFO full • 11 = FIFO full
3	0h RW	**IID3_DMAM (DMAM):** DMA Mode. Reserved
2	0h RW	**IID2_XFIFOR (XFIFOR):** XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h RW	**IID1_RFIFOR (RFIFOR):** RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	1h RW	**IID0_FIFO Enable (FIFOE):** This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset

27.9.4 Line Control Register (LCR)—Offset Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

Bits	31:8	7	6	5	4	3	2	1:0
Default	0000 0000 0000 0000 0000 0000	0	0	0	0	0	0	00
Field	RSVD0	DLAB	Break	RSVD1	EPS	PEN	STOP	DLS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Divisor Latch Access Bit (DLAB):** This bit is used to enable reading and writing of the Divisor Latch register(DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	0h RW	**Break Control Bit (Break):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0b RO	**RSVD1:** Reserved
4	0h RW	**Even Parity Select (EPS):** This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	0h RW	**Parity Enable (PEN):** This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. • 0 = parity disabled • 1 = parity enabled
2	0h RW	**Number of Stop Bits (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. • 0 = 1 stop bit • 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	0h RW	**Data Length Select (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected are as follows: • 00 = 5 bits • 01 = 6 bits • 10 = 7 bits • 11 = 8 bits

27.9.5 Modem Control Register (MCR)—Offset 10h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSVD0	AFCE	LoopBack	OUT2	OUT1	RTS	DTR

Bit Range	Default & Access	Field Name (ID): Description
31:6	0b RO	**RSVD0:** Reserved
5	0h RW	**Auto Flow Control Enable (AFCE):** When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, • 0 = Auto Flow Control Mode disabled • 1 = Auto Flow Control Mode enabled Reset Value: 0x0
4	0h RW	**LoopBack Bit (LoopBack):** This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. Reset Value: 0x0
3	0h RW	**Output2 (OUT2):** This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: • 0 = out2_n de-asserted (logic 1) • 1 = out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
2	0h RW	**Output1 (OUT1):** This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: • 0 = out1_n de-asserted (logic 1) • 1 = out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
1	0h RW	**Request to Send (RTS):** This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
0	0h RW	**Data Terminal Ready (DTR):** This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: • 0 = dtr_n de-asserted (logic 1) • 1 = dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

27.9.6 Line Status Register (LSR)—Offset 14h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000060h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
RSVD0																								RFE	TEMT	THRE	BI	FE	PE	OE	DR

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Receiver FIFO Error Bit (RFE):** This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. • 0 = no error in RX FIFO • 1 = error in RX FIFO This bit is cleared when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. Reset Value: 0x0
6	1h RW	**Transmitter Empty Bit (TEMT):** If FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. Reset Value: 0x1
5	1h RW	**Transmit Holding Register Empty Bit (THRE):** If THRE mode is disabled (IER[7] set to zero), this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE mode is enabled and and FIFOs enabled (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. Reset Value: 0x1
4	0h RW	**Break Interrupt Bit (BI):** This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	0h RW	**Framing Error Bit (FE):** This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). • 0 = no framing error • 1 = framing error Reading the LSR clears the FE bit. Reset Value: 0x0
2	0h RW	**Parity Error Bit (PE):** This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). • 0 = no parity error • 1 = parity error Reading the LSR clears the PE bit. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Overrun Error Bit (OE):** This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. • 0 = no overrun error • 1 = overrun error Reading the LSR clears the OE bit. Reset Value: 0x0
0	0h RW	**Data Ready Bit (DR):** This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. • 0 = no data ready • 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. Reset Value: 0x0

27.9.7 Modem Status Register (MSR)—Offset 18h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

Bits	31:8	7	6	5	4	3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
Field	RSVD0	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**Data Carrier Detect (DCD):** This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted, it is an indication that the carrier has been detected by the modem or data set. • 0 = dcd_n input is de-asserted (logic 1) • 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Reset Value: 0x0
6	0h RW	**Ring Indicator (RI):** This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. • 0 = ri_n input is de-asserted (logic 1) • 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Data Set Ready (DSR):** This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. • 0 = dsr_n input is de-asserted (logic 1) • 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Reset Value: 0x0
4	0h RW	**Clear to Send (CTS):** This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted, it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. • 0 = cts_n input is de-asserted (logic 1) • 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Reset Value: 0x0
3	0h RW	**Delta Data Carrier Detect (DDCD):** This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. • 0 = no change on dcd_n since last read of MSR • 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Reset Value: 0x0
2	0h RW	**Trailing Edge of Ring Indicator (TERI):** This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. • 0 = no change on ri_n since last read of MSR • 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Reset Value: 0x0
1	0h RW	**Delta Data Set Ready (DDSR):** This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. • 0 = no change on dsr_n since last read of MSR • 1 = change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Reset Value: 0x0
0	0h RW	**Delta Clear to Send (DCTS):** This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. • 0 = no change on cts_n since last read of MSR • 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note that if the DCTS bit is not set, the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Reset Value: 0x0

27.9.8 Scratchpad Register (SCR)—Offset 1Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								scr							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**scr:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart. Reset Value: 0x0

27.9.9 Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr0							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr0:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data are lost. An overrun error also occurs. Reset Value: 0x0

27.9.10 Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr1							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr1:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.11 Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr2							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr2:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.12 Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:8) | srbr_sthr3 (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr3:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.13 Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (bits 31:8) | srbr_sthr4 (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr4:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.14 Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr5							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr5:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.15 Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr6							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr6:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.16 Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr7							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr7:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.17 Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								srbr_sthr8							

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr8:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.18 Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
RSVD0	srbr_sthr9

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr9:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.19 Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
RSVD0	srbr_sthr10

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr10:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.20 Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD0 (bits 31:8), srbr_sthr11 (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr11:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.21 Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD0 (bits 31:8), srbr_sthr12 (bits 7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr12:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.22 Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (31:8)	srbr_sthr13 (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr13:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.23 Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (31:8)	srbr_sthr14 (7:0)

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr14:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.24 Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch

Refer to bit field description for SRBR_STHR0.srbr_sthr0.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | srbr_sthr15

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**srbr_sthr15:** Refer to bit field description for SRBR_STHR0.srbr_sthr0.

27.9.25 FIFO Access Register (FAR)—Offset 70h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 | srbr_sthr

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**srbr_sthr:** Writes have no effect when FIFO_ACCESS == No, always readable. This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. • 0 = FIFO access mode disabled • 1 = FIFO access mode enabled Note that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

27.9.26 Transmit FIFO Read (TFR)—Offset 74h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:8	Bits 7:0
RSVD0	tfr

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7:0	0h RW	**Transmit FIFO Read (tfr):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

27.9.27 Receive FIFO Write (RFW)—Offset 78h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:10	Bit 9	Bit 8	Bits 7:0
RSVD0	RFFE	RFPE	RFWD

Bit Range	Default & Access	Field Name (ID): Description
31:10	0b RO	**RSVD0:** Reserved
9	0h RW	**Receive FIFO Framing Error (RFFE):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR. Reset Value: 0x0
8	0h RW	**Receive FIFO Parity Error (RFPE):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR. Reset Value: 0x0
7:0	0h RW	**Receive FIFO Write Data (RFWD):** These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. Reset Value: 0x0

27.9.28 UART Status Register (USR)—Offset 7Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD0																											RFF	RFNE	TFE	TFNF	BUSY

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RO	**RSVD0:** Reserved
4	0h RW	**Receive FIFO Full (RFF):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. • 0 = Receive FIFO not full • 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full. Reset Value: 0x0
3	0h RW	**Receive FIFO Not Empty (RFNE):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. • 0 = Receive FIFO is empty • 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty. Reset Value: 0x0
2	1h RW	**Transmit FIFO Empty (TFE):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. • 0 = Transmit FIFO is not empty • 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty. Reset Value: 0x1

Bit Range	Default & Access	Field Name (ID): Description
1	1h RW	**Transmit FIFO Not Full (TFNF):** This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. • 0 = Transmit FIFO is full • 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full. Reset Value: 0x1
0	0h RW	**UART Busy (BUSY):** Reserved

27.9.29 Transmit FIFO Level (TFL)—Offset 80h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

RSVD0 (31:5)	tfl (4:0)

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RO	**RSVD0:** Reserved
4:0	0h RW	**Transmit FIFO Level (tfl):** This indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

27.9.30 Receive FIFO Level (RFL)—Offset 84h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

RSVD0 (31:5)	rfl (4:0)

Bit Range	Default & Access	Field Name (ID): Description
31:5	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Receive FIFO Level (rfl):** This indicates the number of data entries in the receive FIFO. Reset Value: 0x0

27.9.31 Software Reset Register (SRR)—Offset 88h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																													XFR	RFR	UR

Bit Range	Default & Access	Field Name (ID): Description
31:3	0b RO	**RSVD0:** Reserved
2	0h RW	**XMIT FIFO Reset (XFR):** This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
1	0h RW	**RCVR FIFO Reset (RFR):** This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
0	0h RW	**UART Reset (UR):** This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset. Reset Value: 0x0

27.9.32 Shadow Request to Send (SRTS)—Offset 8Ch

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																															srts

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow Request to Send (srts):** This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

27.9.33 Shadow Break Control Register (SBCR)—Offset 90h

This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																															sbcb

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow Break Control Bit (sbcb):** Reserved.

27.9.34 Shadow DMA Mode (SDMAM)—Offset 94h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																															sdmam

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow DMA Mode (sdmam):** This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). • 0 = mode 0 • 1 = mode 1 Reset Value: 0x0

27.9.35 Shadow FIFO Enable (SFE)—Offset 98h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																															sfe

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**Shadow FIFO Enable (sfe):** This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

27.9.36 Shadow RCVR Trigger (SRT)—Offset 9Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																														srt	

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RO	**RSVD0:** Reserved
1:0	0h RW	**Shadow RCVR Trigger (srt):** This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: • 00 = 1 character in the FIFO • 01 = FIFO full • 10 = FIFO full • 11 = FIFO 2 less than full Reset Value: 0x0

27.9.37 Shadow TX Empty Trigger (STET)—Offset A0h

This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported:

- 00 = FIFO empty
- 01 = 2 characters in the FIFO
- 10 = FIFO full
- 11 = FIFO full

Reset Value: 0x0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: RSVD0 (bits 31:2), stet (bits 1:0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0b RO	**RSVD0:** Reserved
1:0	0h RW	**stet:** Shadow TX Empty Trigger

27.9.38 Halt TX (HTX)—Offset A4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: RSVD0 (bits 31:1), htx (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**htx:** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. • 0 = Halt TX disabled • 1 = Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation. Reset Value: 0x0

27.9.39 DMA Software Acknowledge (DMASA)—Offset A8h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																															dmasa

Bit Range	Default & Access	Field Name (ID): Description
31:1	0b RO	**RSVD0:** Reserved
0	0h RW	**dmasa:** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when DMA_EXTRA == No.

27.9.40 Component Parameter Register (CPR)—Offset F4h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00043F32h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	0	0	1	1	0	0	1	0
RSVD0								FIFO_MODE								RSVD1		DMA_EXTRA	UART_ADD_ENCODED_PARAMS	SHADOW	FIFO_STAT	FIFO_ACCESS	ADDITIONAL_FEAT	SIR_LP_MODE	SIR_MODE	THRE_MODE	AFCE_MODE	RSVD2		APB_DATA_WIDTH	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0b RO	**RSVD0:** Reserved
23:16	4h RO	**FIFO MODE (FIFO_MODE):** • 0x00 = 0 • 0x01 = 16 • 0x02 = 32 • to • 0x80 = 2048 • 0x81- 0xff = reserved
15:14	0b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
13	1h RO	**DMA EXTRA (DMA_EXTRA):** • 0 = FALSE • 1 = TRUE
12	1h RO	**UART ADD ENCODED PARAMS (UART_ADD_ENCODED_PARAMS):** • 0 = FALSE, • 1 = TRUE
11	1h RO	**SHADOW:** • 0 = FALSE, • 1 = TRUE
10	1h RO	**FIFO STAT (FIFO_STAT):** • 0 = FALSE, • 1 = TRUE
9	1h RO	**FIFO ACCESS (FIFO_ACCESS):** • 0 = FALSE, • 1 = TRUE
8	1h RO	**ADDITIONAL FEAT (ADDITIONAL_FEAT):** • 0 = FALSE, • 1 = TRUE
7	0h RO	**SIR LP MODE (SIR_LP_MODE):** • 0 = FALSE, • 1 = TRUE
6	0h RO	**SIR MODE (SIR_MODE):** • 0 = FALSE, • 1 = TRUE
5	1h RO	**THRE MODE (THRE_MODE):** • 0 = FALSE, • 1 = TRUE
4	1h RO	**AFCE MODE (AFCE_MODE):** • 0 = FALSE, • 1 = TRUE
3:2	0b RO	**RSVD2:** Reserved
1:0	2h RO	**APB DATA WIDTH (APB_DATA_WIDTH):** • 00 = 8 bits • 01 = 16 bits • 10 = 32 bits • 11 = reserved

27.9.41 UART Component Version (UCV)—Offset F8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 3330382Ah

31			28				24				20				16				12				8				4				0
0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0	1	0	1	0

UART (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	3330382ah RO	**UART:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*. Reset Value: See the releases table in the AMBA 2 release notes.

27.9.42 Component Type Register (CTR)—Offset FCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 44570110h

31			28				24				20				16				12				8				4				0
0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

PeripheralID (bits 31:0)

Bit Range	Default & Access	Field Name (ID): Description
31:0	44570110h RO	**Peripheral ID (PeripheralID):** This register contains the peripherals identification code. Reset Value: 0x44570110

27.9.43 Private Clock Params (PRV_CLOCK_PARAMS)—Offset 800h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

clk_update (bit 31), n_val (bits 30:16), m_val (bits 15:1), clk_en (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**clk_update:** update the clock divider after seeting new m and n values
30:16	0h RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0h RW	**M_VAL (m_val):** m value for the m over n divider
0	0h RW	**clk_en:** clk en of the m over n divider

27.9.44 Software Resets (RESETS)—Offset 804h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																														reset_apb	reset_func

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Reserved (reserved):** Reserved.
1	0h RW	**reset_apb:** reset the apb domain
0	0h RW	**reset_func:** reset the func clock domain

27.9.45 General Purpose Register (GENERAL)—Offset 808h

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000050h

31:8	7	6	5	4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0	1	0	0	0	0
RSVD0	gpo1	gater_override	gpo3	gpo2	uart_374646_fix_disable	reset_e	sleep_enable	power_enable

Bit Range	Default & Access	Field Name (ID): Description
31:8	0b RO	**RSVD0:** Reserved
7	0h RW	**gpo1:** not applicable
6	1h RW	**gater_override:** not applicable
5	0h RW	**gpo3:** not applicable
4	1h RW	**gpo2:** This bit indicates whether the UART clock req will be dynamic or controlled by the UART clock en: • 1 = controlled by the clk en • 0 = dynamic Default value = 1
3	0h RW	**uart_374646_fix_disable:** Disable rts_n override
2	0h RW	**reset_e:** not applicable
1	0h RW	**sleep_enable:** not applicable
0	0h RW	**power_enable:** not applicable

27.9.46 UART_BYTE_COUNT—Offset 818h

Transaction counter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reseved (31:16) | uart_tx_byte_count (15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**reserved (reseved):** reserved
15:0	0h RO	**uart_tx_byte_count:** UART transaction counter

27.9.47 UART_OVERFLOW_INTR_STAT—Offset 820h

Overflow interrupt

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h

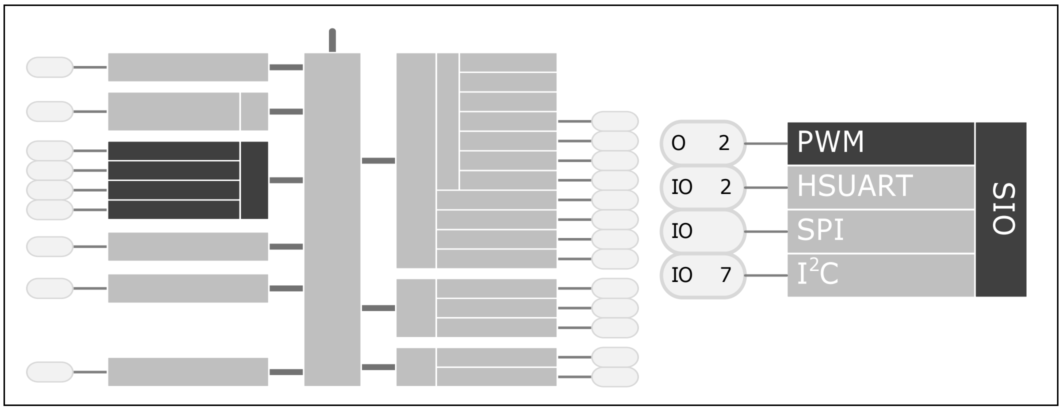
31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved (31:2) | uart_overflow_intr_mask (1) | uart_overflow_intr (0)

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**reserved:** reserved
1	0h RW	**uart1_overflow_intr_mask (uart_overflow_intr_mask):** Mask the overflow intr
0	0h RO	**uart_overflow_intr:** Indicate there was count overflow

28 SIO – Pulse Width Modulation (PWM)

The Pulse Width Modulation block allows control the frequency and duty cycle of an output signal. The SoC has 2 instances of the PWM interface.



28.1 Signal Descriptions

Please see Chapter 2, “Physical Interfaces” for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal’s function

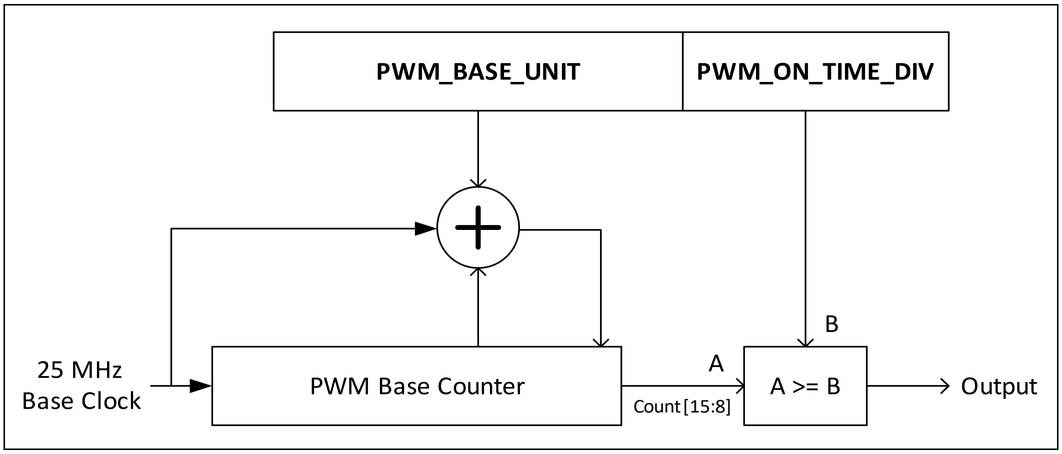
Figure 128.PWM Signals

Signal Name	Direction Plat. Power	Description
SIO_PWM[0]	O V1P8S	Pulse Width Modulation output 0.
SIO_PWM[1]	O V1P8S	Pulse Width Modulation output 1.

28.2 Features

The software controls the PWM block by updating the PWMCTRL register and setting the PWMCTRL.PWM_SW_UPDATE bit whenever a change in frequency or duty cycle of the PWM output signal is required. The PWM block applies the new settings at the start of the next output cycle and resets the PWMCTRL.PWM_SW_UPDATE bit. The SoC uses a 25 MHz base clock rate for the PWM counter. See Figure 129 for PWM block diagram:

Figure 129.PWM Block Diagram



There are two controls of the PWM output:

- **Frequency** is controlled by the PWMCTRL.PWM_BASE_UNIT register. The PWMCTRL.PWM_BASE_UNIT value is added to the 16 bit PWM counter every base clock cycle. The counter roll-over/overflow marks the start of a new cycle and resets the counter to the value in PWMCTRL.PWM_BASE_UNIT.
- **Duty Cycle** is controlled by the PWMCTRL.PWM_ON_TIME_DIVISOR setting (0 to 255). When the 16 bit PWM counter is less than PWM_ON_TIME_DIVISOR * 256, the PWM output is low (0). When the 16 bit PWM counter is equal to or greater than PWM_ON_TIME_DIVISOR * 256, the PWM output is high (1).

The PWM block is clocked by the 25 MHz oscillator clock. The output frequency can be estimated with the equation:

- Target frequency = 25 MHz / CEILING(65536/PWM_BASE_UNIT)
  Note that the larger the value of base_unit, the larger the error that the PWM output frequency will have with respect to the equation above. For example any Base_unit_value/256 > 128 will result in 12.5 MHz max frequency. Any value between 86 and 128 will result in 8.33 MHz output frequency. And accordingly the larger the base_unit value the smaller duty cycle resolution. Maximum duty cycle resolution is 8 bits.

Table 287 illustrates the output frequency and duty-cycle resolution for different settings of the base_unit_value (when using 25 MHz oscillator clock).

Table 287. Example PWM Output Frequency and Resolution

Target Frequency	Base Unit Value Register	Base 25 MHz Cycle Count	Duty Cycle Resolution
12.5 MHz	>=128 * 256	1	no resolution
1.07 MHz	11 * 256	23	<8 bit resolution
488 kHz	5 * 256	51	<8 bit resolution
97.6 kHz	1 * 256	256	8 resolution
48.4 kHz	0.5 * 256	512	>= 8 bit resolution
0	0	0	Flat 0 output

28.3 Use

28.3.1 PWM Programming Sequence

For first time activation, follow sequence:

1. Program the counter value PWMCTRL.PWM_BASE_UNIT and PWMCTRL.PWM_ON_TIME_DIVISOR
2. Set the PWMCTRL.PWM_SW_UPDATE bit
3. Enable PWM output by setting the PWMCTRL.PWM_ENABLE bit

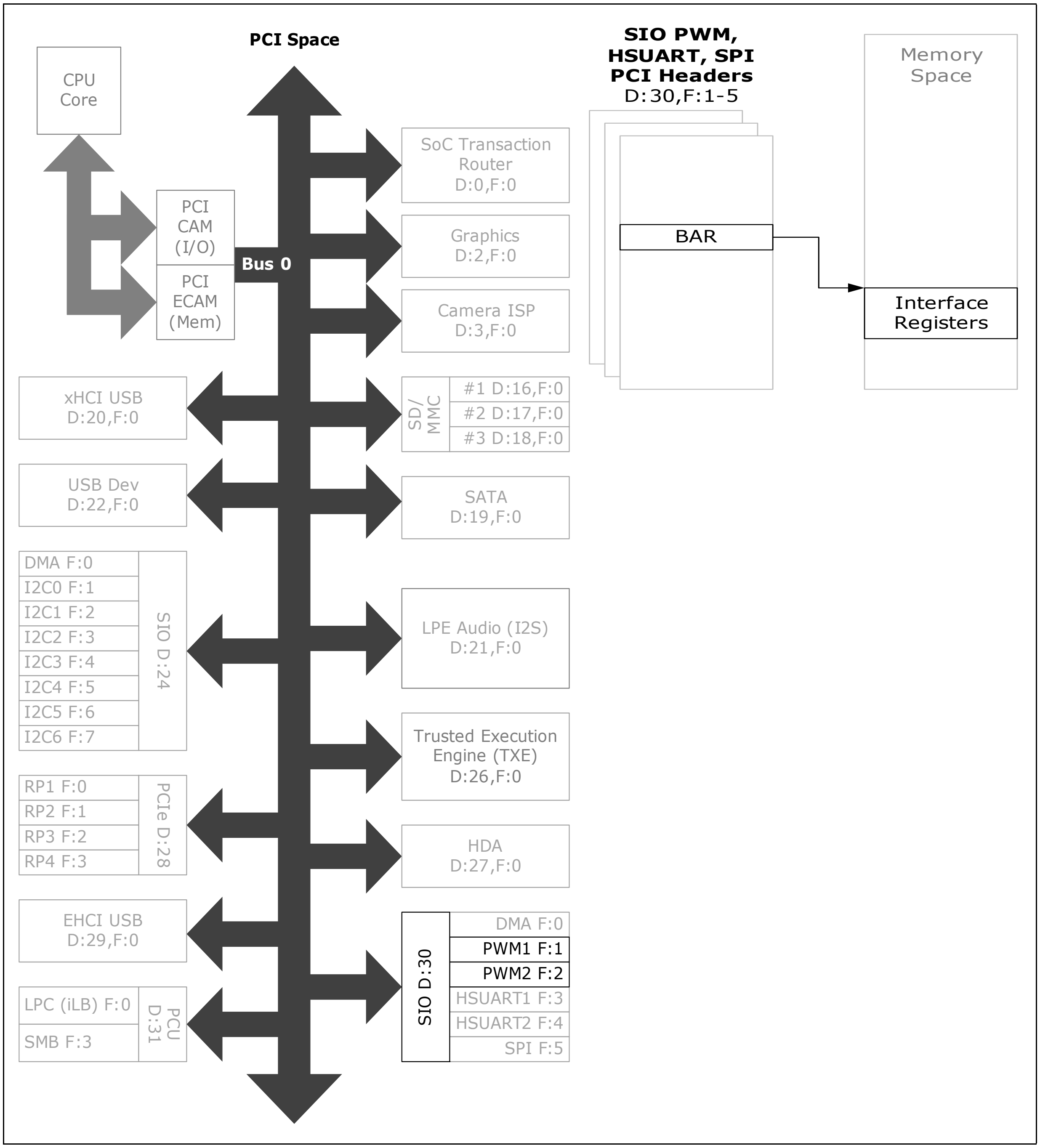
For update on the fly, follow sequence:

1. Program the counter value PWMCTRL.PWM_BASE_UNIT and PWMCTRL.PWM_ON_TIME_DIVISOR
2. Set the update bit PWMCTRL.PWM_SW_UPDATE

28.4 Register Map

Refer to Chapter 3, "Register Access Methods" and Chapter 4, "Mapping Address Spaces" for additional information.

Figure 130.SIO - PWM Register Map



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28.5 SIO PWM 0 PCI Configuration Registers

Table 288. Summary of PWM 0 PCI Configuration Registers—0/30/1

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4326	00008086h
4–7h	4	"Status and Command (STATUSCOMMAND)—Offset 4h" on page 4327	00100000h
8–Bh	4	"Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4328	00000000h
C–Fh	4	"Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4328	00800000h
10–13h	4	"Base Address Register (BAR)—Offset 10h" on page 4329	00000000h
14–17h	4	"Base Address Register 1 (BAR1)—Offset 14h" on page 4330	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4330	00000000h
30–33h	4	"Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4331	00000000h
34–37h	4	"Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4331	00000000h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4332	00000100h
80–83h	4	"PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4332	00030001h
84–87h	4	"PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4333	00000008h
F8–FBh	4	"Manufacturer ID (MANID)—Offset F8h" on page 4334	00000000h

28.5.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DEVICEID																VENDORID															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Device ID (DEVICEID):** Device ID identifies the particular AHB device. This is tied to a strap at the top level.
15:0	8086h RO	**Vendor ID (VENDORID):** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap at the top level.

28.5.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 4h

Default: 00100000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved0	SSE	RMA	RTA	STA	Reserved1						CAPLIST	INTR_STATUS	Reserved2			Reserved3					INTR_DISABLE	Reserved4	SERR_ENABLE	Reserved5					BME	MSE	Reserved6

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved0:** Reserved.
30	0h RW/1C	**SSE:** Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port.
27	0h RW/1C	**STA:** Reserved.
26:21	00h RO	**Reserved1:** Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required, then this bit should be tied to 0.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0h RO	**Reserved2:** Reserved.
15:11	00h RO	**Reserved3:** Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, i.e. Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.
9	0h RO	**Reserved4:** Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** If both SERR# Enable and the Unsupported Request Reporting Enable(URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7:3	00h RO	**Reserved5:** Reserved.
2	0h RW	**Bus Master Enable (BME):** If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master.
1	0h RW	**Memory Space Enable (MSE):** This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled.
0	0h RO	**Reserved6:** Reserved.

28.5.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:8	7:0
CLASS_CODES	RID

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	00h RO	**Revision ID (RID):** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

28.5.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + Ch

Default: 00800000h

31:24	23	22:16	15:8	7:0
0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Reserved0	MULFNDEV	HEADERTYPE	LATTIMER	CACHELINE_SIZE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Reserved0:** Reserved.
23	1h RO	**Multi Function Device (MULFNDEV):** This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. • 1 = multifunction device • 0 = single function device
22:16	00h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	00h RO	**Latency Timer (LATTIMER):** Does not apply to PCI Express. Hardwired to 00h.
7:0	00h RW	**Cache Line Size (CACHELINE_SIZE):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

28.5.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 10h

Default: 00000000h

31:12	11:4	3	2:1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0	0 0	0
BASEADDR	SIZEINDICATOR	PREFETCHABLE	TYPE	MESSAGE_SPACE

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address (BASEADDR):** Base address of the AHB device memory space. Taken from Strap values as 1.s
11:4	00h RO	**Size Indicator Read Only (SIZEINDICATOR):** Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0. Indicates this BAR is present in the memory space.

28.5.6 Base Address Register 1 (BAR1)—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)   **Offset:** [B:0, D:30, F:1] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BASEADDR1 | SIZEINDICATOR1 | PREFETCHABLE1 | TYPE1 | MESSAGE_SPACE1

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Register 1 (BASEADDR1):** BAR1 of the LPIO device.
11:4	00h RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not.
2:1	0h RO	**Type (TYPE1):** 00 Indicates BAR lies in 32 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0. Indicates this BAR is present in the memory space.

28.5.7 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)   **Offset:** [B:0, D:30, F:1] + 2Ch

Default: 00000000h

31 … 28	27 … 24	23 … 20	19 … 16	15 … 12	11 … 8	7 … 4	3 … 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
SUBSYSTEMID				SUBSYSTEMVENDORID			

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O	**Subsystem ID (SUBSYSTEMID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register, make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0000h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

28.5.8 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:1] + 30h

Default: 00000000h

31 … 28	27 … 24	23 … 20	19 … 16	15 … 12	11 … 8	7 … 4	3 … 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
EXPANSION_ROM_BASE							

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION_ROM_BASE:** Reserved.

28.5.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:30, F:1] + 34h

Default: 00000000h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Reserved0 | CAPPTR_POWER

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Reserved0:** Reserved.
7:0	00h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

28.5.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 3Ch

Default: 00000100h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1 | 0 0 0 0 | 0 0 0 0

MAX_LAT | MIN_GNT | Reserved0 | INTPIN | INTLINE

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max_Lat (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
23:16	00h RO	**Min_Gnt (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.
15:12	0h RO	**Reserved0:** Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW	**Interrupt Line (INTLINE):** Bridge does not use this field directly. It is used to tell software which interrupt line the interrupt pin is connected to.

28.5.11 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 80h

Default: 00030001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

PMESUPPORT	Reserved0	VERSION	NXTCAP	POWER_CAP

Bit Range	Default & Access	Field Name (ID): Description
31:27	00h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. • bit(11) X XXX1b - PME# can be asserted from D0. • bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. • bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. • bit(14) X 1XXXb - PME# can be asserted from D3hot. • bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	00h RO	**Reserved0:** Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	01h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

28.5.12 PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 84h

Default: 00000008h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Reserved0	PMESTATUS	Reserved1	PMEENABLE	Reserved2	NO_SOFT_RESET	Reserved3	POWERSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PMESTATUS):** • 0 = Software clears the bit by writing a 1 to it. • 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register).
14:9	00h RO	**Reserved1:** Reserved.
8	0h RW	**PME Enable (PMEENABLE):** A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0h RO	**Reserved2:** Reserved.
3	1h RO	**No_Soft_Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	**Reserved3:** Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: • 00 = D0 state • 11 = D3HOT state • Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

28.5.13 Manufacturer ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MANID

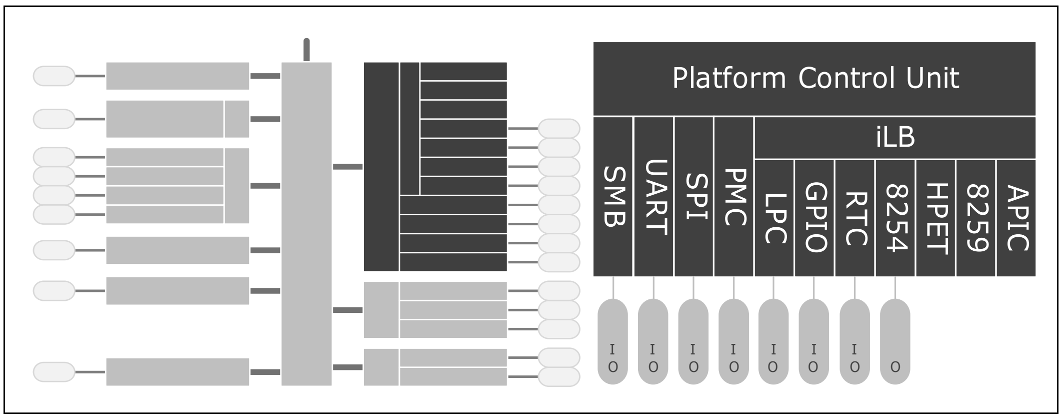
Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**Manufacturer ID (MANID):** This register is brought out as straps to the top level.

29 Platform Controller Unit (PCU) Overview

The Platform Controller Unit (PCU) is a collection of HW blocks that are critical for implementing a Windows* compatible platform. These HW blocks include:

- PCU – Power Management Controller (PMC)
- PCU – Serial Peripheral Interface (SPI)
  — For boot FW and system configuration data Flash storage
- PCU – Universal Asynchronous Receiver/Transmitter (UART)PCU – System Management Bus (SMBus)
- PCU – Intel® Legacy Block (iLB) Overview

The PCU also implements some high level configuration features for BIOS/EFI boot.



29.1 Features

The key features of the individual blocks are as follows:

- Universal Asynchronous Receiver/Transmitter (UART)
  — 16550 controller compliant
  — Reduced Signal Count: TX and RX only
  — COM1 interface
- Serial Peripheral Interface (SPI)
  — For one or two SPI Flash, of up to 16MB size each, only. No other SPI peripherals are supported.
  — Stores boot FW and system configuration data

- Supports frequencies of 20 MHz, 33MHz and 50MHz.

- Power Management Controller (PMC)
  - Controls many of the power management features present in the SoC.
- Intel Legacy Block (iLB)
  - Supports legacy PC platform features
  - Sub-blocks include LPC, GPIO, 8259 PIC, IO-APIC, 8254 timers, HPET timers and the RTC.

§

29.2 PCU iLB LPC Port 80h I/O Registers

Table 289. Summary of PCU iLB LPC Port 80h I/O Registers—

Offset	Size	Register ID—Description	Default Value
80h	1	"PC80—Offset 80h" on page 4337	00h
81h	1	"PC81—Offset 81h" on page 4338	00h
82h	1	"PC82—Offset 82h" on page 4338	00h
83h	1	"PC83—Offset 83h" on page 4338	00h
84h	1	"PC84—Offset 84h" on page 4339	00h
85h	1	"PC85—Offset 85h" on page 4339	00h
86h	1	"PC86—Offset 86h" on page 4340	00h
87h	1	"PC87—Offset 87h" on page 4340	00h
88h	1	"PC88—Offset 88h" on page 4340	00h
89h	1	"PC89—Offset 89h" on page 4341	00h
8Ah	1	"PC8A—Offset 8Ah" on page 4341	00h
8Bh	1	"PC8B—Offset 8Bh" on page 4342	00h
8Ch	1	"PC8C—Offset 8Ch" on page 4342	00h
8Dh	1	"PC8D—Offset 8Dh" on page 4342	00h
8Eh	1	"PC8E—Offset 8Eh" on page 4343	00h
8Fh	1	"PC8F—Offset 8Fh" on page 4343	00h

29.2.1 PC80—Offset 80h

Post Code 80 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC80: 80h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PC80REG							

Bit Range	Default & Access	Description
7:0	0h RW	**PC80REG:** Post Code 80 regsiter

29.2.2 PC81—Offset 81h

Post Code 81 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC81: 81h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PC81REG							

Bit Range	Default & Access	Description
7:0	X RW	**PC81REG:** Post Code 81 regsiter

29.2.3 PC82—Offset 82h

Post Code 82 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC82: 82h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PC82REG							

Bit Range	Default & Access	Description
7:0	X RW	**PC82REG:** Post Code 82 regsiter

29.2.4 PC83—Offset 83h

Post Code 83 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC83: 83h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PC83REG							

Bit Range	Default & Access	Description
7:0	X RW	**PC83REG:** Post Code 83 regsiter

29.2.5 PC84—Offset 84h

Post Code 84 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC84: 84h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PC84REG							

Bit Range	Default & Access	Description
7:0	X RW	**PC80REG (PC84REG):** Post Code 84 regsiter

29.2.6 PC85—Offset 85h

Post Code 85 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC85: 85h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PC85REG							

Bit Range	Default & Access	Description
7:0	X RW	**PC85REG:** Post Code 85 regsiter

29.2.7 PC86—Offset 86h

Post Code 86 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC86: 86h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PC86REG							

Bit Range	Default & Access	Description
7:0	X RW	**PC86REG:** Post Code 86 regsiter

29.2.8 PC87—Offset 87h

Post Code 87 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC87: 87h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PC87REG							

Bit Range	Default & Access	Description
7:0	X RW	**PC87REG:** Post Code 87 regsiter

29.2.9 PC88—Offset 88h

Post Code 88 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC88: 88h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							

Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

29.2.10 PC89—Offset 89h

Post Code 89 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC89: 89h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							

Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

29.2.11 PC8A—Offset 8Ah

Post Code 8A regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC8A: 8Ah

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							

Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

29.2.12 PC8B—Offset 8Bh

Post Code 8B regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC8B: 8Bh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							

Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

29.2.13 PC8C—Offset 8Ch

Post Code 8C regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC8C: 8Ch

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							

Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

29.2.14 PC8D—Offset 8Dh

Post Code 8D regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC8D: 8Dh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							

Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

29.2.15 PC8E—Offset 8Eh

Post Code 8E regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC8E: 8Eh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							

Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

29.2.16 PC8F—Offset 8Fh

Post Code 8F regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

PC8F: 8Fh

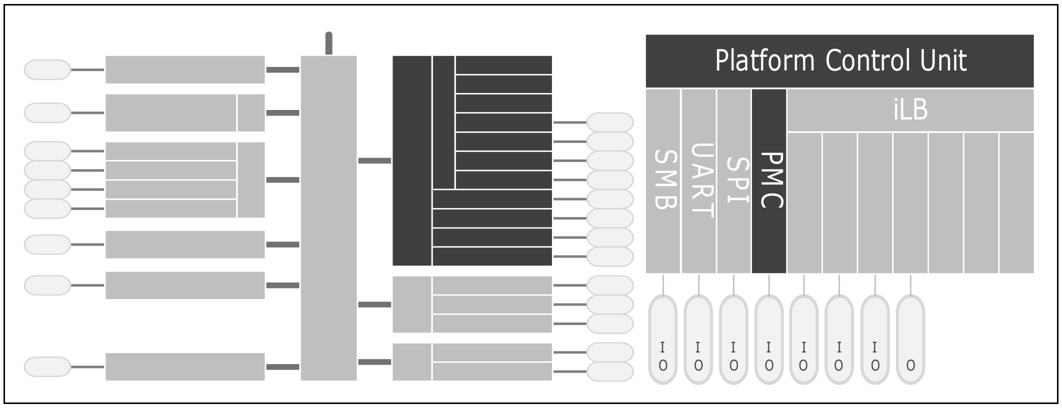
Default: 00h

7			4				0
0	0	0	0	0	0	0	0
Reserved							

Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

30 PCU – Power Management Controller (PMC)

The Power Management Controller (PMC) controls many of the power management features present in the SoC.



30.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 290. PMC Signals (Sheet 1 of 3)

Signal Name	Direction Plat. Power	Description
PMC_ACPRESENT	I V1P8A	**AC Present:** This input pin indicates when the platform is plugged into AC power.
PMC_BATLOW#	I V1P8A	**Battery Low:** An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from the S5 state. This signal can also be enabled to cause an SMI# when asserted. In configurations without a battery, this signal should be tied high to V1P8_S5.

Table 290. PMC Signals (Sheet 2 of 3)

Signal Name	Direction Plat. Power	Description
PMC_CORE_PWROK	I VRTC	**Core Power OK:** When asserted, this signal is an indication to the SoC that all of its core power rails have been stable for 10 ms. It can be driven asynchronously. When it is negated, the SoC asserts PMC_PLTRST#. **NOTE:** It is required that the power rails associated with PCI Express (typically the 3.3V, 5V, and 12V core well rails) have been valid for 99 ms prior to PMC_CORE_PWROK assertion in order to comply with the 100 ms T_{PVPERL} PCI Express 2.0 specification on PMC_PLTRST# deassertion. **NOTE:** PMC_CORE_PWROK must not glitch, even if PMC_RSMRST# is low.
PMC_PLTRST#	O V1P8A	**Platform Reset:** The SoC asserts this signal to reset devices on the platform. The SoC asserts the signal during power-up and when software initiates a reset sequence through the Reset Control (RST_CNT) register when RST_CNT.sys_rst=1b.
PMC_PWRBTN#	I V1P8A	**Power Button:** The signal will cause SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If the signal is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S3 & S4 states. This signal has an internal pull-up resistor and has an internal ~16 ms de-bounce on the input.
PMC_RSMRST#	I VRTC	**Resume Well Reset:** Used for resetting the resume well. An external RC circuit is required to guarantee that the resume well power is valid prior to this signal going high.
PMC_RSTBTN#	I V1P8S	**System Reset:** This signal forces an internal reset after being debounced (~16 ms).
PMC_SLP_S3#	O V1P8A	**S3 Sleep Control:** This signal is for power plane control. It can be used to control system power when it is in a S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
PMC_SLP_S4#	O V1P8A	**S4 Sleep Control:** This signal is for power plane control. It can be used to control system power when it is in a S4 (Suspend to Disk) or S5 (Soft Off) state.
PMC_SUS_STAT#	O V1P8A	**Suspend Status:** This signal is asserted by the SoC to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. *This signal is muxed and may be used by other functions.*

Table 290. PMC Signals (Sheet 3 of 3)

Signal Name	Direction Plat. Power	Description
PMC_SUSCLK	O V1P8A	**Suspend Clock:** This 32 kHz clock is an output of the RTC generator circuit for use by other chips for refresh clock. *This signal is muxed and may be used by other functions.*
PMC_SUSPWRDNACK	O V1P8A	**Suspend Power Down Acknowledge:** Asserted by the SoC on S0 to S4/5 transition when it does not require its Suspend well to be powered. This pin requires a pull-up to UNCORE_V1P8_G3. *This signal is muxed and may be used by other functions.*
PMC_WAKE_PCIE[3:0]#	I V1P8A	**PCI Express* Port [3:0] Wake Event:** Sideband wake signal on PCI Express asserted by a component requesting wake up. *This signal is muxed and may be used by other functions.*
PMC_PLT_CLK[5:0]	O V1P8S	**Platform Clocks:** Configurable single ended clocks, configurable to 25 MHz. *This signal is muxed and may be used by other functions.*

30.2 Features

30.2.1 Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The GEN_PMCON1.AG3E bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). There are only two possible events that will wake the system after a power failure.

- **PMC_PWRBTN#:** PMC_PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PM1_STS_EN.PWRBTN_STS bit is reset. When the SoC exits G3 after power returns (PMC_RSMRST# goes high), the PMC_PWRBTN# signal is already high (because the suspend plane goes high before PMC_RSMRST# goes high) and the PM1_STS_EN.PWRBTN_STS bit is 0b.
- **RTC Alarm:** The PM1_STS_EN.RTC_EN bit is in the RTC well and is preserved after a power loss. Like PM1_STS_EN.PWRBTN_STS the PM1_STS_EN.RTC_STS bit is cleared when PMC_RSMRST# goes low.

The SoC monitors both PMC_CORE_PWROK and PMC_RSMRST# to detect for power failures. If PMC_CORE_PWROK goes low, the GEN_PMCON1.PWR_FLR bit is set. If PMC_RSMRST# goes low, GEN_PMCON1.SUS_PWR_FLR is set.

Table 291. Transitions Due to Power Failure

State at Power Failure	GEN_PMCON1.AG3E bit	Transition When Power Returns
S0, S3	1 0	S5 S0
S4	1 0	S4 S0
S5	1 0	S5 S0

30.2.2 Event Input Signals and Their Usage

The SoC has various input signals that trigger specific events. This section describes those signals and how they should be used.

30.2.3 PCI Express* WAKE# Signal and PME Event Message

PCI Express ports can wake the platform from any sleep state (S3, S4, or S5) using the PMC_WAKE_PCIE[3:0]# pins.

Note: PMC_WAKE_PCIE[3:0]# functionality is disabled by setting PM1_STS_EN.PCIEXP_WAKE_DIS to 1b.

PCI Express ports have the ability to cause PME using messages. When a PME message is received, the SoC will set the GPE0a_STS.PCI_EXP_STS bit.

30.2.3.1 PMC_PWRBTN# (Power Button)

The PMC_PWRBTN# signal operates as a "Fixed Power Button" as described in the Advanced Configuration and Power Interface specification. The signal has a 16 ms debounce on the input. The state transition descriptions are included in Table 292. Note that the transitions start as soon as the PMC_PWRBTN# is pressed (but after the debounce logic), and does not depend on when the power button is released.

Note: During the time that the PMC_SLP_S4# signal is stretched for the minimum assertion width (if enabled), the power button is not a wake event. Refer to note below for more details.

Table 292. Transitions Due to Power Button

Present State	Event	Transition/Action	Comment
S0/Cx	PMC_PWRBTN# goes low	SCI generated (depending on PM1_CNT.SCI_EN and PM1_STS_EN.PWRBTN_EN)	Software typically initiates a Sleep state
S3–S4/ S5	PMC_PWRBTN# goes low	Wake Event. Transitions to S0 state	Standard wakeup
G3	PMC_PWRBTN# pressed	None	No effect since no power Not latched nor detected
S0, S3–S4	PMC_PWRBTN# held low for at least 4 consecutive seconds	Unconditional transition to S5 state	No dependence on processor or any other subsystem

Power Button Override Function

If PMC_PWRBTN# is observed active for at least four consecutive seconds, the state machine should unconditionally transition to the S5 state, regardless of present state (S0–S4), even if the PMC_CORE_PWROK is not active. In this case, the transition to the G2/S5 state should not depend on any particular response from the processor nor any similar dependency from any other subsystem.

The PMC_ PWRBTN# status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable using the GEN_PMCON2.PWRBTN_LVL bit.

Note: The 4-second PMC_PWRBTN# assertion should only be used if a system lock-up has occurred. The 4-second timer starts counting when the SoC is in a S0 state. If the PMC_PWRBTN# signal is asserted and held active when the system is in a suspend state (S3–S4), the assertion causes a wake event. Once the system has resumed to the S0 state, the 4-second timer starts.

Note: During the time that the SLP_S4# signal is stretched for the minimum assertion width (if enabled by GEN_PMCON1.S4ASE), the power button is not a wake event. As a result, it is conceivable that the user will press and continue to hold the power button waiting for the system to awake. Since a 4-second press of the power button is already defined as an unconditional power down, the power button timer will be forced to inactive while the power-cycle timer is in progress. Once the power-cycle timer has expired, the power button awakes the system. Once the minimum PMC_SLP_S4# power cycle expires, the power button must be pressed for another 4 to 5 seconds to create the override condition to S5.

30.2.3.2 Sleep Button

The Advanced Configuration and Power Interface specification defines an optional sleep button. It differs from the power button in that it only is a request to go from S0 to S3–S4 (not S5). Also, in an S5 state, the power button can wake the system, but the sleep button cannot.

Although the SoC does not include a specific signal designated as a sleep button, one of the GPIO signals can be used to create a "Control Method" sleep button. See the Advanced Configuration and Power Interface specification for implementation details.

30.2.3.3 PME_B0 (PCI Power Management Event Bus 0)

The GPE0a_STS.PME_B0_STS bit exists to implement PME#-like functionality for any internal device on Bus 0 with PCI power management capabilities.

30.2.3.4 PMC_RSTBTN# Signal

When the PMC_RSTBTN# pin is detected as active after the 16 ms debounce logic, the SoC attempts to perform a "graceful" reset, by waiting for the relevant internal devices to signal their idleness. If all devices are idle when the pin is detected active, the reset occurs immediately; otherwise, a counter starts. If at any point during the count all devices go idle the reset occurs. If the counter expires and any device is still active, a reset is forced upon the system even though activity is still occurring.

Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the PMC_RSTBTN# input remains asserted or not. It cannot occur again until PMC_RSTBTN# has been detected inactive after the debounce logic, and the system is back to a full S0 state with PMC_PLTRST# inactive. Note that if RST_CNT.FULL_RST is set then PMC_RSTBTN# will result in a Host Reset with Power Cycle.

30.2.4 System Power Planes

The system has several independent power planes, as described in Table 293. Note that when a particular power plane is shut off, it should go to a 0 V level.

Table 293. System Power Planes (Sheet 1 of 2)

Plane	Controlled By	Description
CPU	PMC_SLP_S3#	The SLP_S3# signal can be used to cut the CORE_VCC_S3 rail completely.
Main	PMC_SLP_S3#	When SLP_S3# goes active, power can be shut off to any circuit not required to wake the system from the S3 state. Since the S3 state requires that the memory context be preserved, power must be retained to the main memory. Devices on LPC bus, PCI-Express, and SATA will typically be shut when the Main power plane is shut, although they may have small subsections powered.

Table 293. System Power Planes (Sheet 2 of 2)

Plane	Controlled By	Description
Devices and Memory	PMC_SLP_S4#	When PMC_SLP_S4# goes active, power can be shut off to any circuit not required to wake the system from the S4/S5. Since the memory context does not need to be preserved in the S4/S5 state, the power to the memory can also be shut down. S4 and S5 requests are treated the same so no PMC_SLP_S5# signal is implemented.
Devices	Implementation Specific	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.
Suspend	PMC_SUSPWRDNACK	The suspend power planes are generally left on whenever the system has a charged main battery or is plugged in to AC power, even in S4/5. In some cases, it may be preferable to disable the suspend power planes in S4/S5 states to save additional power. This requires some external logic (such as an embedded controller) to decide on the appropriate power plane control actions and ensure that a wake event is still possible (such as the power button).

30.2.4.1 Power Plane Control with PMC_SLP_S3#, PMC_SLP_S4#

The PMC_SLP_S3# output signal can be used to cut power to the system core supply, since it only goes active for the Suspend-to-RAM state (typically mapped to ACPI S3). Power must be maintained to the SoC suspend well, and to any other circuits that need to generate wake signals from the Suspend-to-RAM state. During S3 (Suspend-to-RAM) all signals attached to powered down plans will be tri-stated or driven low, unless they are pulled using a pull-up resistor.Cutting power to the core may be done using the power supply, or by external FETs on the motherboard.

The PMC_SLP_S4# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done using the power supply, or by external FETs on the motherboard.

30.2.4.2 PMC_SLP_S4# and Suspend-To-RAM Sequencing

The PMC_SLP_S4# signal should be used to remove power to system memory. The PMC_SLP_S4# logic in the SoC provides a mechanism to fully cycle the power to the DRAM and/or detect if the power is not cycled for a minimum time.

Note: To use the minimum DRAM power-down feature that is enabled by the GEN_PMCON1.S4ASE bit, the DRAM power must be controlled by the PMC_SLP_S4# signal.

30.2.4.3 PMC_CORE_PWROK Signal

When asserted, PMC_CORE_PWROK is an indication to the SoC that its core well power rails are powered and stable. PMC_CORE_PWROK can be driven asynchronously. When PMC_CORE_PWROK is low, the SoC asynchronously asserts PMC_PLTRST#. PMC_CORE_PWROK must not glitch, even if PMC_RSMRST# is low.

It is required that the power rails associated with PCI Express have been valid for 99 ms prior to PWROK assertion in order to comply with the 100 ms T_{PVPERL} PCI Express 2.0 specification on PMC_PLTRST# deassertion.

Note: PMC_RSTBTN# is recommended for implementing the system reset button. This saves external logic that is needed if the PMC_CORE_PWROK input is used. Additionally, it allows for better handling of the processor resets and avoids improperly reporting power failures.

30.2.4.4 PMC_BATLOW# (Battery Low)

The PMC_BATLOW# input can inhibit waking from S3, S4, and S5 states if there is not sufficient power. It also causes an SMI if the system is already in an S0 state.

30.2.5 SMI#/SCI Generation

Upon any enabled SMI event taking place while the SMI_EN.EOS bit is set, the SoC will clear the EOS bit and assert SMI to the CPU core, which will cause it to enter SMM space. SMI assertion is performed using a Virtual Legacy Wire (VLW) message. Prior system generations (those based upon legacy processors) used an actual SMI# pin.

Once the SMI message has been delivered, the SoC takes no action on behalf of active SMI events until Host software sets the End of SMI (EOS) bit. At that point, if any SMI events are still active, the SoC will send another SMI message.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts IRQs[11:9] or IRQs[23:20]. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRQ or not. The interrupt remains asserted until all SCI sources are removed.

Table 294 shows which events can cause an SMI and SCI. Note that some events can be programmed to cause either an SMI or SCI. The usage of the event for SCI (instead of SMI) is typically associated with an ACPI-based system. Each SMI or SCI source has a corresponding enable and status bit.

Table 294. Causes of SMI and SCI (Sheet 1 of 3)

Event	Status Indication[1]	Enable Condition	Interrupt Result			
			SMI_EN. GBL_SMI_EN=1b		SMI_EN. GBL_SMI_EN=0b	
			PM1_CNT .SCI_EN= 1b	PM1_CNT .SCI_EN= 0b	PM1_CNT. SCI_EN= 1b	PM1_CNT. SCI_EN=0 b
Power Button Override[3]	PM1_STS_EN. PWRBTNOR_STS	None	SCI	None	SCI	None
RTC Alarm	PM1_STS_EN. RTC_STS	PM1_STS_EN_EN. RTC_EN=1b	SCI	SMI	SCI	None
Power Button Press	PM1_STS_EN. PWRBTN_STS	PM1_STS_EN_EN. PWRBTN_EN=1b	SCI	None	SCI	None
SMI_EN.BIOS_RLS bit written to 1b[4]	PM1_STS_EN. GBL_STS	PM1_STS_EN_EN. GBL_EN=1b	SCI			
ACPI Timer overflow (2.34 seconds)	PM1_STS_EN. TMROF_STS	PM1_STS_EN_EN. TMROF_EN =1b	SCI	SMI	SCI	None
GPI[n][9]	GPE0a_STS. CORE_GPIO_STS[n][2] or GPE0a_STS. SUS_GPIO_STS[n][2]	GPIO_ROUT[n] = 10b & GPE0a_EN. CORE_GPIO_EN[n][2]=1b or GPE0a_EN. SUS_GPIO_EN[n][2]=1b	SCI	None	SCI	None
Internal, Bus 0, PME-Capable Agents (PME_B0)	GPE0a_STS. PME_B0_STS	GPE0_EN. PME_B0_EN=1b	SCI	SMI	SCI	None
BATLOW# pin goes low	GPE0a_STS. BATLOW_STS#	GPE0_EN. BATLOW_EN=1b	SCI	SMI	SCI	None
PCI Express GPE messages	GPE0a_STS. HOT_PLUG_STS	GPE0_EN. HOT_PLUG_EN=1b	SCI	None	SCI	None
Software Generated GPE	GPE0a_STS. SWGPE_STS	GPE0_EN. SWGPE_EN=1b	SCI	SMI	SCI	None
PCI Express Hot Plug SCI Message	GPE0a_STS. HOT_PLUG_STS	GPE0_EN. HOT_PLUG_EN=1b	SCI	None	SCI	None
ASSERT_SCI message from PCIe	GPE0a_STS. PCI_EXP_STS	None (enabled by PCIe controller)	SCI	None	SCI	None

Table 294. Causes of SMI and SCI (Sheet 2 of 3)

Event	Status Indication[1]	Enable Condition	Interrupt Result			
			SMI_EN. GBL_SMI_EN=1b		SMI_EN. GBL_SMI_EN=0b	
			PM1_CNT .SCI_EN= 1b	PM1_CNT .SCI_EN= 0b	PM1_CNT. SCI_EN= 1b	PM1_CNT. SCI_EN=0 b
Write to APM register	SMI_STS.apm_sts	SMI_EN.apmc_en = 1'b1	SMI	SMI	None	None
DOSCI message from P-Unit	GPE0a_STS.punit_sci_sts	None (enabled by P-Unit)	SCI	None	SCI	None
DOSMI message from P-Unit	SMI_STS.punit_sci_sts	None (enabled by P-Unit)	SMI	SMI	None	None
DOSCI message from GUNIT[5]	GPE0a_STS. GUNIT_STS	None (enabled by G-Unit[8])	SCI	None	SCI	None
ASSERT_SMI message from SPI[5]	SMI_STS. SPI_SMI_STS	None (enabled by SPI controller)	SMI		None	
ASSERT_SMI message from PCIe[5]	SMI_STS. PCI_EXP_SMI_STS	None (enabled by PCIe controller)	SMI		None	
ASSERT_IS_SMI message from USB	SMI_STS. USB_IS_STS	SMI_EN. USB_IS_SMI_EN =1b	SMI		None	
ASSERT_SMI message from USB	SMI_STS.USB_STS	SMI_EN. USB_SMI_EN=1b	SMI		None	
ASSERT_SMI message from iLB[5]	SMI_STS. ILB_SMI_STS	None (enabled by iLB)	SMI		None	
Periodic timer expires	SMI_STS. PERIODIC_STS	SMI_EN. PERIODIC_EN=1b	SMI		None	
WDT first expiration	SMI_STS.TCO_STS	SMI_EN.TCO_EN =1b	SMI		None	
64 ms timer expires	SMI_STS. SWSMI_TMR_STS	SMI_EN. SWSMI_TMR_EN =1b	SMI		None	
PM1_CNT.SLP_EN bit written to 1b	SMI_STS. SMI_ON_SLP_EN_STS	SMI_EN. SMI_ON_SLP_EN =1b	Sync SMI[6]		None	
PM1_CNT.GBL_RLS written to 1b	SMI_STS.BIOS_STS	SMI_EN. BIOS_EN=1b	Sync SMI[6]		None	
DOSMI message from GUNIT[5]	SMI_STS. GUNIT_SMI_STS	None (enabled by G-Unit[8])	SMI		None	
ASSERT_IS_SMI message from iLB[5]	SMI_STS. ILB_SMI_STS	None (enabled by iLB)	Sync SMI[7]		None	

Table 294. Causes of SMI and SCI (Sheet 3 of 3)

Event	Status Indication[1]	Enable Condition	Interrupt Result			
			SMI_EN.GBL_SMI_EN=1b		SMI_EN.GBL_SMI_EN=0b	
			PM1_CNT.SCI_EN=1b	PM1_CNT.SCI_EN=0b	PM1_CNT.SCI_EN=1b	PM1_CNT.SCI_EN=0b
ASSERT_IS_SMI message from PCIe[5]	SMI_STS.PCI_EXP_SMI_STS	None (enabled by PCIe controller)	SMI		None	
PMC_WAKE_PCIE[3:0]# Assertion	GPE0a_STS.PCIE_WAKE[3:0]_STS	GPE0a_STS.PCIE_WAKE[3:0]_EN = 1b	SCI	None	SCI	None
GPI[n][10]	ALT_GPIO_SMI.CORE_GPIO_SMI_STS[n][2] or ALT_GPIO_SMI.SUS_GPIO_SMI_STS[n][2]	GPIO_ROUT[n]=01b & ALT_GPIO_SMI.CORE_GPIO_SMI_EN[n][2]=1b or ALT_GPIO_SMI.SUS_GPIO_SMI_EN[n][2]=1b	SMI		None	
USB Per-Port Registers Write Enable bit is changed from 0b to 1b	UPRWC.WE_STS & SMI_STS.USB_IS_STS	UPRWC.WE_SMI_E=1b & SMI_EN.USB_IS_SMI_EN=1b	Sync SMI[6]		None	

NOTES:

1. Most of the status bits (except otherwise is noted) are set according to event occurrence regardless to the enable bit.
2. GPIO status bits are set only if enable criteria is true. GPIO_ROUT[n]=10b & GPE0a_EN.x_GPIO_EN[n] for GPE0a_STS.x_GPIO_STS[n] (SCI). GPIO_ROUT[n]=01b & ALT_GPIO_SMI. x_GPIO_SMI_EN[n]=1b for ALT_GPIO_SMI.x_GPIO_SMI_STS[n] (SMI).
3. When power button override occurs, the system will transition immediately to S5. The SCI will only occur after the next wake to S0 if the residual status bit (PM1_STS_EN.PWRBTNOR_STS) is not cleared prior to setting PM1_CNT.SCI_EN.
4. PM1_STS_EN.GBL_STS being set will cause an SCI, even if the PM1_CNT.SCI_EN bit is not set. Software must take great care not to set the SMI_ENBIOS_RLS bit (which causes PM1_STS_EN.GBL_STS to be set) if the SCI handler is not in place.
5. No enable bits for these SCI/SMI messages in the PMC. Enable capability should be implemented in the source unit.
6. Sync SMI has the same message opcode toward T-Unit. Special treatment regarding this Sync SMI is holding completion to host till SYNC_SMI_ACK message is received from T-Unit.
7. Sync SMI has the same message opcode toward T-Unit. Special treatment regarding this Sync SMI is holding the SSMI_ACK message to iLB till SYNC_SMI_ACK message is received from T-Unit.
8. The G-Unit is an internal functional sub-block which forms part of the graphics functional block.
9. The GPE0a_STS.CORE_GPIO_STS[31:24] & GPE0a_EN.CORE_GPIO_EN[31:24] register bits correspond to GPIO_S0_SC[7:0]. GPE0a_STS.SUS_GPIO_STS[23:16] & GPE0a_EN.SUS_GPIO_EN[23:16] correspond to GPIO_S5[7:0].
10. The ALT_GPIO_SMI.CORE_GPIO_SMI_STS[31:24] & ALT_GPIO_SMI.CORE_GPIO_SMI_EN[15:8] register bits correspond to GPIO_S0_SC[7:0]. ALT_GPIO_SMI.SUS_GPIO_SMI_STS[23:16] & ALT_GPIO_SMI.SUS_GPIO_SMI_EN[7:0] correspond to GPIO_S5[7:0].

30.2.6 Platform Clock Support

The SoC supports up to 6 clocks (PMC_PLT_CLK[5:0])with a frequency of either 19.2 MHz or 25 MHz. These clocks are available for general system use, where appropriate and each have Control & Frequency register fields associated with them.

Note: Intel recommends 25 MHz. 19.2 MHz is not validated.

30.2.7 INIT# (Initialization) Generation

The INIT# functionality is implemented as a 'virtual wire' internal to the SoC rather than a discrete signal. This virtual wire is asserted based on any one of the events described in below table. When any of these events occur, INIT# is asserted for 16 PCI clocks and then driven high.

INIT#, when asserted, resets integer registers inside the CPU cores without affecting its internal caches or floating-point registers. The cores then begin execution at the power on Reset vector configured during power on configuration.

Table 295. INIT# Assertion Causes

Cause	Comment
PORT92.INIT_NOW transitions from 0b to1b.	
RST_CNT.SYS_RST = 0b and RST_CNT.RST_CPU transitions from 0b to 1b	

30.3 USB Per-Port Register Write Control

The PMC contains the UPRWC.USB_PER_PORT_WE (USB Per-Port Registers Write Enable) bit. When this bit is written from 0b to 1b, the UPRWC.WE_STS (Write Enable Status) bit is asserted. This transaction initiates sync-SMI if the UPRWC.WE_SMIEN (Write Enable SMI Enable) bit and the SMI_EN.USB_IS_SMI_EN (USB Intel Specific SMI Enable) bit are set to 1b.

30.4 References

Advanced Configuration and Power Interface Specification, Revision 3.0: http://www.acpi.info/

30.5 Register Map

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30.6 PCU PMC IO Registers

Table 296. Summary of PCI iLB PMC I/O Registers

Offset	Size	Register ID—Description	Default Value
92h	1	"PORT92: Init Register (PORT92)—Offset 92h" on page 4356	00h
B2h	1	"APM Register (APM)—Offset B2h" on page 4357	00h
B3h	1	"APM_STS Register (APM_STS)—Offset B3h" on page 4357	00h
CF9h	1	"RST_CNT: Reset Control Register (RST_CNT)—Offset CF9h" on page 4358	00h

30.6.1 PORT92: Init Register (PORT92)—Offset 92h

Access Method

Type: I/O Register
(Size: 8 bits)

PORT92: 92h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
reserved						alt_a20_gate	init_now

Bit Range	Default & Access	Description
7:2	0b RO	**reserved:** Reserved.
1	0b RW	**ALT_A20_GATE - Alternate A20 Gate (alt_a20_gate):** Legacy bit - kept just in case DOS expects it to be read/write
0	0b RW	**INIT_NOW (init_now):** When this bit transitions from a 0 to a 1, PMC will sent an INIT# VLW to T-Unit

30.6.2 APM Register (APM)—Offset B2h

Access Method

Type: I/O Register
(Size: 8 bits)

APM: B2h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
apm_reg							

Bit Range	Default & Access	Description
7:0	0b RW	**APM_Register (apm_reg):** TBD

30.6.3 APM_STS Register (APM_STS)—Offset B3h

Access Method

Type: I/O Register
(Size: 8 bits)

APM_STS: B3h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
apm_sts							

Bit Range	Default & Access	Description
7:0	0b RW	**APM_STS (apm_sts):** Advanced Power Managment Status Port. used to pass data between the OS and the SMI handler. Basically, this is scratchpad register and is not effected by any other register or function (other than a PCI reset)

30.6.4 RST_CNT: Reset Control Register (RST_CNT)—Offset CF9h

Access Method

Type: I/O Register
(Size: 8 bits)

RST_CNT: CF9h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
reserved				full_rst	rst_cpu	sys_rst	reserved1

Bit Range	Default & Access	Description
7:4	0b RO	**reserved:** Reserved.
3	0b RW	**Full Reset (FULL_RST) (full_rst):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PMC will do a full reset, including driving PMU_SLP_S3_B and PMU_SLP_S4_B active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (PMU_SLP_S3/4_B assertion) in response to PMU_RESETBUTTON_B, COREPWROK, and Watchdog timer reset sources.
2	0b RW	**Reset CPU (RST_CPU) (rst_cpu):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0b RW	**System Reset (SYS_RST) (sys_rst):** Ths bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PMC will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PMC will force PCI reset active for about 1 ms, however the PMU_SLP_S3_B and PMU_SLP_S4_B signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0b RO	**reserved1:** Reserved.

30.7 PCU iLB PMC I/O Registers

Table 297. Summary of PCU iLB PMC I/O Registers—ACPI_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"PM1_STS_EN - Power Management 1 Status and enable (PM1_STS_EN)—Offset 0h" on page 4359	00000000h
4h	4	"PM1_CNT - Power Management 1 Control (PM1_CNT)—Offset 4h" on page 4362	00000000h
8h	4	"PM1_TMR - Power Management 1 Timer (PM1_TMR)—Offset 8h" on page 4363	00000000h
20h	4	"GPE0a_STS - General Purpose Event 0 Status (GPE0a_STS)—Offset 20h" on page 4363	00000000h
28h	4	"GPE0a_EN - General Purpose Event 0 Enables (GPE0a_EN)—Offset 28h" on page 4366	00000000h
30h	4	"SMI_EN - SMI Control and Enable (SMI_EN)—Offset 30h" on page 4367	00000002h
34h	4	"SMI_STS - SMI Status Register (SMI_STS)—Offset 34h" on page 4368	00000000h
38h	4	"ALT_GPIO_SMI - Alternate GPIO SMI Status and Enable Register. (ALT_GPIO_SMI)—Offset 38h" on page 4370	00000000h
3Ch	4	"UPRWC - USB Per-Port Registers Write Control (UPRWC)—Offset 3Ch" on page 4371	00000000h
40h	4	"GPE_CTRL - General Purpose Event Control (GPE_CTRL)—Offset 40h" on page 4372	00000000h
50h	4	"PM2A_CNT_BLK - PM2a Control Block (PM2A_CNT_BLK)—Offset 50h" on page 4372	00000000h
60h	4	"TCO_RLD: TCO Reload Register (TCO_RLD)—Offset 60h" on page 4373	00000000h
64h	4	"TCO_STS: TCO Timer Status (TCO_STS)—Offset 64h" on page 4373	00000000h
68h	4	"TCO1_CNT: TCO Timer Control (TCO1_CNT)—Offset 68h" on page 4374	00000000h
70h	4	"TCO_TMR: TCO Timer Register (TCO_TMR)—Offset 70h" on page 4375	00040000h

30.7.1 PM1_STS_EN - Power Management 1 Status and enable (PM1_STS_EN)—Offset 0h

Access Method

Type: I/O Register
(Size: 32 bits)

PM1_STS_EN: [ACPI_BASE_ADDRESS] + 0h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

Bit(s)	Default	Field
31	0	reserved4
30	0	pciexp_wake_dis
29	0	usb_clkless_en
28:27	0 0	reserved5
26	0	rtc_en
25	0	reserved6
24	0	pwrbtn_en
23:22	0 0	reserved7
21	0	gbl_en
20:17	0 0 0 0	reserved8
16	0	tmrof_en
15	0	wak_sts
14	0	pciexp_wake_sts
13	0	usb_clkless_sts
12	0	reserved
11	0	pwrbtnor_sts
10	0	rtc_sts
9	0	reserved1
8	0	pwrbtn_sts
7:6	0 0	reserved2
5	0	gbl_sts
4:1	0 0 0 0	rserved3
0	0	tmrof_sts

Bit Range	Default & Access	Description
31	0b RO	**reserved4:** Reserved.
30	0b RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS) (pciexp_wake_dis):** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. reset_type=Resume Well Reset#
29	0b RW	**USB clockless Wake Enable (USB_CLKLESS_EN) (usb_clkless_en):** This bit enables the inputs to the USB_CLKLESS_STS bit in the PM1 Status register to wake the system. Modification of this bit has no impact on the value of the USB_CLKLESS_STS bit. reset_type=Resume Well Reset#
28:27	0b RO	**reserved5:** Reserved.
26	0b RW	**RTC Alarm Enable (RTC_EN) (rtc_en):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit: RTC_EN SCI_EN Effect when RTC_STS is set 0 x No SMI# or SCI. If system was in S1-S5, no wake even occurs. 1 0 SMI#. If system was in S1-S5, then a wake event occurs before the SMI#. 1 1 SCI. If system was in S1-S5, then a wake event occurs before the SCI. Note: This bit needs to be backed by the RTC well to allow an RTC event to wake after a power failure. In addition to being reset by SRTCRST_B assertion, PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
25	0b RO	**reserved6:** Reserved.
24	0b RW	**Power Button Enable (PWRBTN_EN) (pwrbtn_en):** This bit is the power button enable. It works in conjunction with the SCI_EN bit: PWRBTN_EN SCI_EN Effect when PWRBTN_STS is set 0 x No SMI# or SCI. 1 0 SMI#. 1 1 SCI. NOTE: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event. reset_type=Resume Well Reset#
23:22	0b RO	**reserved7:** Reserved.
21	0b RW	**Global Enable (GBL_EN) (gbl_en):** The global enable bit. When both the GBL_EN and the GBL_STS are set, PMC generates an SCI. reset_type=PMU_PLTRST_B
20:17	0b RO	**reserved8:** Reserved.
16	0b RW	**Timer Overflow Interrupt Enable (TMROF_EN) (tmrof_en):** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit: TMROF_EN SCI_EN Effect when TMROF_STS is set 0 x No SMI# or SCI. . 1 0 SMI#. 1 1 SCI. reset_type=PMU_PLTRST_B
15	0b RW	**Wake Status (WAK_STS) (wak_sts):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Wake event occurs. Upon setting this bit, the PMC will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case This is based on discussions with Microsoft. That behavior is not in the ACPI spec. reset_type=RSMRST_B

Bit Range	Default & Access	Description
14	0b RW	**PCI Express Wake Status (PCIEXP_WAKE_STS) (pciexp_wake_sts):** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pins (PMU_WAKE_B, PCI_WAKE1_B, PCI_WAKE2_B, PCI_WAKE3_B) being active, or one or more of the PCI Express ports being in beacon state, or recept of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independant of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If one of the WAKE# pins is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain Power Management active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not auatomatically wake. reset_type=pmc_global_rst_b
13	0b RW	**USB clockless Wake Status (USB_CLKLESS_STS) (usb_clkless_sts):** This bit is set by hardware to indicate that the system woke due to change in USB serial lines. This bit is set independant of the USB_CLKLESS_EN bit. Software writes a 1 to clear this bit. reset_type=pmc_global_rst_b
12	0b RO	**reserved:** Reserved.
11	0b RW	**Power Button Override (PWRBTNOR_STS) (pwrbtnor_sts):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST_B. Thus, this bit is preserved through power failures. Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated. reset_type=SRTCRST_B
10	0b RW	**RTC Status (RTC_STS) (rtc_sts):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. reset_type=RSMRST_B
9	0b RO	**reserved1:** Reserved.
8	0b RW	**Power Button Status (PWRBTN_STS) (pwrbtn_sts):** This bit is set when the PMU_PWRBTN_B signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If the PMU_PWRBTN_B signal is held low for more than 4 seconds, the PMC clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PMU_PWRBTN_B is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PMU_PWRBTN_B pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PMU_PWRBTN_B signal must go inactive and active again to set the PWRBTN_STS bit. Note that the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit. reset_type=RSMRST_B
7:6	0b RO	**reserved2:** Reserved.
5	0b RW	**GBL Status (GBL_STS) (gbl_sts):** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. reset_type=PMU_PLTRST_B
4:1	0b RO	**reserved3 (rserved3):** reserved

Bit Range	Default & Access	Description
0	0b RW	**Timer Overflow Status (TMROF_STS) (tmrof_sts):** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. reset_type=PMU_PLTRST_B

30.7.2 PM1_CNT - Power Management 1 Control (PM1_CNT)—Offset 4h

Access Method

Type: I/O Register
(Size: 32 bits)

PM1_CNT: [ACPI_BASE_ADDRESS] + 4h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31	28	24	20	16	12	8	4	0

0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

reserved	slp_en	slp_typ	reserved1	gbl_rls	bm_rld	sci_en

Bit Range	Default & Access	Description
31:14	0b RO	**reserved:** Reserved.
13	0b WO	**Sleep Enable (SLP_EN) (slp_en):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	0b RW	**Sleep Type (SLP_TYP) (slp_typ):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are reset by SRTCRST_B only. Bits Mode Typical Mapping 000 ON S0 001 Puts CPU in S1 state. S1 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5
9:3	0b RO	**reserved1:** Reserved.
2	0b RW	**GBL_RLS (GBL_RLS) (gbl_rls):** This bit is used by the ACPI software to raise an event to the BIOS software. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events. This bit always reads as 0.
1	0b RW	**BM_RLD (BM_RLD) (bm_rld):** This bit is treated as a scratchpad bit
0	0b RW	**SCI Enable (SCI_EN) (sci_en):** SCI Enable (SCI_EN): Selects the SCI interrupt or the SMI# for various events. When this bit is 1, then the events will generate an SCI interrupt. When this bit is 0, these events will generate an SMI#.

30.7.3 PM1_TMR - Power Management 1 Timer (PM1_TMR)—Offset 8h

Access Method

Type: I/O Register
(Size: 32 bits)

PM1_TMR: [ACPI_BASE_ADDRESS] + 8h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

Bits	31:24	23:0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Field	reserved	tmr_val

Bit Range	Default & Access	Description
31:24	0b RO	**reserved:** Reserved.
23:0	0b RO	**Timer Value (TMR_VAL) (tmr_val):** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a Platform reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

30.7.4 GPE0a_STS - General Purpose Event 0 Status (GPE0a_STS)—Offset 20h

Note: This register is symmetrical to the General Purpose Event 0a Enable Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the PMC will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PMC will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set. CLARIFICATION: Bits 15:0 should not be reset by CF9 write. Bits 31:16 are reset by CF9h full resets. reset_type=RSMRST_B

Access Method

Type: I/O Register
(Size: 32 bits)

GPE0a_STS: [ACPI_BASE_ADDRESS] + 20h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

Bits	Default	Field
31	0	core_gpio_sts7
30	0	core_gpio_sts6
29	0	core_gpio_sts5
28	0	core_gpio_sts4
27	0	core_gpio_sts3
26	0	core_gpio_sts2
25	0	core_gpio_sts1
24	0	core_gpio_sts0
23	0	sus_gpio_sts7
22	0	sus_gpio_sts6
21	0	sus_gpio_sts5
20	0	sus_gpio_sts4
19	0	sus_gpio_sts3
18	0	sus_gpio_sts2
17	0	sus_gpio_sts1
16	0	sus_gpio_sts0
15:14	0 0	reserved4
13	0	pme_b0_sts
12:11	0 0	reserved3
10	0	batlow_sts
9	0	pci_exp_sts
8	0	pcie_wake3_sts
7	0	pcie_wake2_sts
6	0	pcie_wake1_sts
5	0	gunit_sci_sts
4	0	punit_sci_sts
3	0	pcie_wake0_sts
2	0	swgpe_sts
1	0	hot_plug_sts
0	0	reserved

Bit Range	Default & Access	Description
31	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts7):** These bits are set any time the corresponding Core GPIO is set up as an input and the corresponding GPIO signal is asserted. Core GPIO pins are: SATA_GP0 (GPIO core 0) SATA_GP1 (GPIO core 1) SATA_LEDN (GPIO core 2) PCIE_CLKREQ0B (GPIO core 3) PCIE_CLKREQ1B (GPIO core 4) PCIE_CLKREQ2B (GPIO core 5) PCIE_CLKREQ3B (GPIO core 6) PCIE_CLKREQ4B (GPIO core 7) If the corresponding enable bit is set in the GPE0a_EN register, then when the CORE_GPIO_STS[n] bit is set, an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPIO. These bits are sticky bits and are cleared by writing a 1 back to this bit position. reset_type=Resume Well Reset#
30	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts6):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
29	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts5):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
28	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts4):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
27	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts3):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
26	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts2):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
25	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts1):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
24	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts0):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
23	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts7):** These bits are set any time the corresponding Sus GPIO is set up as an input and the corresponding GPIO signal is asserted. Sus GPIO pins are GPIO_SUS0-7. If the corresponding enable bit is set in the GPE0a_EN register, then when the SUS_GPIO_STS[n] bit is set: * If the system is in an S3-S5 state, the event will also wake the system. * If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. reset_type=Resume Well Reset#
22	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts6):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
21	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts5):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
20	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts4):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
19	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts3):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
18	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts2):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
17	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts1):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
16	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts0):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
15:14	0b RO	**reserved (reserved4):** Reserved.

Bit Range	Default & Access	Description
13	0b RW	**Power Management Event Bus 0 Status (PME_B0_STS) (pme_b0_sts):** This bit will be set to 1 by the PMC when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - HD Audio - SATA - USB
12:11	0b RO	**reserved (reserved3):** Reserved.
10	0b RW	**Battery Low Status (BATLOW_STS) (batlow_sts):** This bit will be set to 1 by hardware when the PMU_BATLOW_B signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved.
9	0b RW	**PCI Express Status (PCI_EXP_STS) (pci_exp_sts):** This bit will be set to 1 by hardware to indicate that: - The PME event message was received on one or more of the PCI-Express Ports Note: The PCI PMU_WAKE_B pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds.
8	0b RW	**PCI Express Wake3 Status (PCIE_WAKE3_STS) (pcie_wake3_sts):** This bit is set by hardware to indicate that the PCI_WAKE3_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE3_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
7	0b RW	**PCI Express Wake2 Status (PCIE_WAKE2_STS) (pcie_wake2_sts):** This bit is set by hardware to indicate that the PCI_WAKE2_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE2_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
6	0b RW	**PCI Express Wake1 Status (PCIE_WAKE1_STS) (pcie_wake1_sts):** This bit is set by hardware to indicate that the PCI_WAKE1_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE1_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
5	0b RW	**GUNIT SCI status (GUNIT_SCI_STS) (gunit_sci_sts):** This bit will be set if the Graphics Unit requests SCI
4	0b RW	**PUNIT SCI status (PUNIT_SCI_STS) (punit_sci_sts):** This bit will be set if the Power Management Unit requests SCI
3	0b RW	**PCI Express Wake0 Status (PCIE_WAKE0_STS) (pcie_wake0_sts):** This bit is set by hardware to indicate that the PMU_WAKE_B pin was asserted. Software writes a 1 to clear this bit. If PMU_WAKE_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
2	0b RW	**Software GPE Status (SWGPE_STS) (swgpe_sts):** The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit.
1	0b RO	**Hot Plug Status (HOT_PLUG_STS) (hot_plug_sts):** This bit is set to 1 by hardware when a PCI-Express hotplug event occurs. This will cause an SCI if the HOT_PLUG_EN and SCI_EN bits are set. This bit is cleared by writing a 1 to this bit position. The following events cause this bit to set - Assert_GPE message received from any of the PCI_E ports in the SOC - Assert_HPGPE message received from any of the PCI_E ports in the SOC
0	0b RO	**reserved:** Reserved.

30.7.5 GPE0a_EN - General Purpose Event 0 Enables (GPE0a_EN)—Offset 28h

Note: This register is symmetrical to the General Purpose Event 0a Status Register. reset_type=Resume Well Reset#

Access Method

Type: I/O Register
(Size: 32 bits)

GPE0a_EN: [ACPI_BASE_ADDRESS] + 28h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

Bits	31:24	23:16	15:14	13	12:11	10	9	8	7	6	5:4	3	2	1	0
Default	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0	0	0 0	0	0	0	0	0	0 0	0	0	0	0
Field	core_gpio_en	sus_gpio_en	reserved3	pme_b0_en	reserved2	batlow_en	pci_exp_en	pcie_wake3_en	pcie_wake2_en	pcie_wake1_en	reserved1	pcie_wake0_en	swgpe_en	hot_plug_en	reserved

Bit Range	Default & Access	Description
31:24	0b RW	**CORE GPIO Enable (CORE_GPIO_EN) (core_gpio_en):** These bits enable the corresponding CORE_GPIO_STS[n] bits being set to cause an SCI and/or wake event.
23:16	0b RW	**SUS GPIO Enable (SUS_GPIO_EN) (sus_gpio_en):** These bits enable the corresponding SUS_GPIO_STS[n] bits being set to cause an SCI and/or wake event.
15:14	0b RO	**reserved (reserved3):** Reserved.
13	0b RW	**PME_B0 Enable (PME_B0_EN) (pme_b0_en):** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
12:11	0b RO	**reserved (reserved2):** Reserved.
10	0b RW	**Low Battery Enable (BATLOW_EN) (batlow_en):** This bit enables the PMU_BATLOW_B signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the PMU_BATLOW_B signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
9	0b RW	**PCI Express Enable (PCI_EXP_EN) (pci_exp_en):** Enables the PMC to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports, to cause an SCI due to wake/PME events
8	0b RW	**PCI Express Wake3 Enable (PCIE_WAKE3_EN) (pcie_wake3_en):** This bit, when set to 1, enables the PCIE_WAKE3_STS to cause an SCI
7	0b RW	**PCI Express Wake2 Enable (PCIE_WAKE2_EN) (pcie_wake2_en):** This bit, when set to 1, enables the PCIE_WAKE2_STS to cause an SCI
6	0b RW	**PCI Express Wake1 Enable (PCIE_WAKE1_EN) (pcie_wake1_en):** This bit, when set to 1, enables the PCIE_WAKE1_STS to cause an SCI
5:4	0b RO	**reserved (reserved1):** Reserved.

Bit Range	Default & Access	Description
3	0b RW	**PCI Express Wake0 Enable (PCIE_WAKE0_EN) (pcie_wake0_en):** This bit, when set to 1, enables the PCIE_WAKE0_STS to to cause an SCI
2	0b RW	**Software GPE Enable (SWGPE_EN) (swgpe_en):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0b RW	**Hot Plug Enable (HOT_PLUG_EN) (hot_plug_en):** Enables the PMC to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events.
0	0b RO	**reserved:** Reserved.

30.7.6 SMI_EN - SMI Control and Enable (SMI_EN)—Offset 30h

Access Method

Type: I/O Register
(Size: 32 bits)

SMI_EN: [ACPI_BASE_ADDRESS] + 30h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000002h

Bits	Field	Default
31:19	reserved	0 0 0 0 0 0 0 0 0 0 0 0 0
18	usb_is_smi_en	0
17	usb_smi_en	0
16:15	reserved1	0 0
14	periodic_en	0
13	tco_en	0
12:8	reserved2	0 0 0 0 0
7	bios_rls	0
6	swsmi_tmr_en	0
5	apmc_en	0
4	smi_on_slp_en	0
3	reserved4	0
2	bios_en	0
1	eos	1
0	gbl_smi_en	0

Bit Range	Default & Access	Description
31:19	0b RO	**reserved:** Reserved.
18	0b RW	**Intel USB 2 Enable (USB_IS_SMI_EN): (usb_is_smi_en):** Enables Intel-Specific USB2 SMI logic to cause SMI#.
17	0b RW	**USB SMI Enable (USB_SMI_EN): (usb_smi_en):** Enables SMI from USB
16:15	0b RO	**reserved1:** Reserved.
14	0b RW	**Periodic Enable (PERIODIC_EN) (periodic_en):** Setting this bit will cause the PMC to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register.
13	0b RW	**TCO Enable (TCO_EN): (tco_en):** when set Enables the TCO logic to generate SMI#. when cleared disables TCO logic generating an SMI#. NOTE: This bit can not be written once the TCO_LOCK bit is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's
12:8	0b RO	**reserved2:** Reserved.

Bit Range	Default & Access	Description
7	0b RW	**BIOS_RLS (BIOS_RLS): (bios_rls):** Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. This bit always reads a zero. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.
6	0b RW	**Software SMI Timer Enable (SWSMI_TMR_EN): (swsmi_tmr_en):** Software sets this bit to a 1 to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0.
5	0b RW	**APMC_EN (apmc_en):** APMC Enable - If set, this enables writes to the APM register to cause an SMI#
4	0b RW	**SMI On Sleep Enable (SMI_ON_SLP_EN): (smi_on_slp_en):** If this bit is set, the PMC will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the PMC will not put the system to a sleep state. This allows the SMI# handler work around chip-level bugs. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit.
3	0b RO	**reserved4:** Reserved.
2	0b RW	**BIOS Enable (BIOS_EN): (bios_en):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	1b RW	**End of SMI (EOS): (eos):** SMI handler sets this bit when it finishes handling the SMI. Setting this bit will force the PMC internal SMI request to zero for 1 clock.Thus if the internal SMI request is still asserted due to new SMI trigger a new rising edge will happen, setting the interrupt to the PMC controller.
0	0b RW	**Global SMI Enable (GBL_SMI_EN): (gbl_smi_en):** When set, this bit enables the generation of SMIs in the system upon any enabled SMI event. This bit is reset by a PMU_PLTRST_B reset event. If this bit is not set, no SMI# will be generated. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed.

30.7.7 SMI_STS - SMI Status Register (SMI_STS)—Offset 34h

Access Method

Type: I/O Register
(Size: 32 bits)

SMI_STS: [ACPI_BASE_ADDRESS] + 34h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved		gunit_smi_sts	punit_smi_sts	reserved1	spi_smi_sts	reserved2				reserved5	pci_exp_smi_sts	reserved8	usb_is_sts	usb_sts	smbus_smi_sts	ilb_smi_sts	periodic_sts	tco_sts	reserved3			gpe0_sts	pm1_sts_reg	reserved4	swsmi_tmr_sts	apm_sts	smi_on_slp_en_sts	reserved6	bios_sts	reserved7	

Bit Range	Default & Access	Description
31:30	0b RO	**reserved:** Reserved.
29	0b RW	**GUNIT SMI Status (GUNIT_SMI_STS): (gunit_smi_sts):** This bit will be set if Graphics unit is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'
28	0b RW	**PUNIT SMI Status (PUNIT_SMI_STS): (punit_smi_sts):** This bit will be set if Power Management is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'
27	0b RO	**reserved (reserved1):** Reserved.
26	0b RO	**SPI_SMI Status (SPI_SMI_STS): (spi_smi_sts):** This bit will be set when the SPI logic is requesting an SMI#
25:22	0b RO	**reserved (reserved2):** Reserved.
21	0b RW	**reserved (reserved5):** This bit is reserved for future use
20	0b RO	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS): (pci_exp_smi_sts):** 1- PCI Express SMI event occurred. This could be due to a PCI Express PME event.
19	0b RO	**reserved (reserved8):** Reserved.
18	0b RO	**Intel USB2 Status (USB_IS_STS): (usb_is_sts):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the Intel-Specific USB2 SMI Status Register ANDed with the corresponding enable bits. Additionally, the Port Disable Write Enable SMI is reported in this bit; the specific status bit for this event is contained in the USB Per-Port Registers Write Control Register in this I/O space. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated USB2 Host Controllers are represented with this bit.
17	0b RO	**USB Status (USB_STS): (usb_sts):** This bit will be set when the USB logic is requesting an SMI#
16	0b RO	**SMBUS_SMI Status (SMBUS_SMI_STS): (smbus_smi_sts):** This bit will be set when the SMBUS logic is requesting an SMI#
15	0b RO	**ILB_SMI Status (ILB_SMI_STS): (ilb_smi_sts):** This bit will be set when the ILB logic is requesting an SMI#
14	0b RW	**Periodic Status (PERIODIC_STS): (periodic_sts):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the PMC will generate an SMI#. This bit is cleared by writing a 1 to this bit position.
13	0b RW	**TCO Status (TCO_STS): (tco_sts):** Indicates SMI was caused by the TCO logic. This bit is cleared by writing a 1 to this bit position.
12:10	0b RO	**reserved (reserved3):** Reserved.
9	0b RO	**GPE0a Status (GPE0a_STS): (gpe0_sts):** There are several status/enable bit pairs in GPE0a_STS/EN that are capable of triggering SMI. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#.
8	0b RO	**PM1 Status Register (PM1_STS_REG): (pm1_sts_reg):** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1_STS_EN Status Reg. Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.
7	0b RO	**reserved (reserved4):** Reserved.

Bit Range	Default & Access	Description
6	0b RW	**Software SMI Timer Status (SWSMI_TMR_STS): (swsmi_tmr_sts):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit.
5	0b RW	**APM_STS (apm_sts):** APM Status - SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position.
4	0b RW	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS): (smi_on_slp_en_sts):** This bit will be set by the PMC when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position
3	0b RO	**reserved (reserved6):** Reserved.
2	0b RW	**BIOS Status (BIOS_STS): (bios_sts):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position.
1:0	0b RO	**reserved (reserved7):** Reserved.

30.7.8 ALT_GPIO_SMI - Alternate GPIO SMI Status and Enable Register. (ALT_GPIO_SMI)—Offset 38h

reset_type=Resume Well Reset#

Access Method

Type: I/O Register
(Size: 32 bits)

ALT_GPIO_SMI: [ACPI_BASE_ADDRESS] + 38h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31:24	23:16	15:8	7:0
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
core_gpio_smi_sts	sus_gpio_smi_sts	core_gpio_smi_en	sus_gpio_smi_en

Bit Range	Default & Access	Description
31:24	0b RW	**CORE GPIO SMI Status Setting (CORE_GPIO_SMI_STS): (core_gpio_smi_sts):** These bits report the status of the corresponding GPIO's. 1 = active, -0 = inactive. These bits are sticky. If the following conditions are true, then an SMI# will be generated: 1. The corresponding enable bit in this register is set 2. The corresponding GPIO must be routed in the GPIO_ROUT register to cause an SMI. 3. The corresponding GPIO must be implemented. Core GPIO pins are: SATA_GP0 (GPIO core 0) SATA_GP1 (GPIO core 1) SATA_LEDN (GPIO core 2) PCIE_CLKREQ0B (GPIO core 3) PCIE_CLKREQ1B (GPIO core 4) PCIE_CLKREQ2B (GPIO core 5) PCIE_CLKREQ3B (GPIO core 6) PCIE_CLKREQ4B (GPIO core 7) All bits are in the resume well. Default for these bits are dependent on the state of the GPIO pins.

Bit Range	Default & Access	Description
23:16	0b RW	**SUS GPIO SMI Status Setting (SUS_GPIO_SMI_STS): (sus_gpio_smi_sts):** These bits report the status of the corresponding GPIO's. 1 = active, -0 = inactive. These bits are sticky. If the following conditions are true, then an SMI# will be generated: 1. The corresponding enable bit in this register is set 2. The corresponding GPIO must be routed in the GPIO_ROUT register to cause an SMI. 3. The corresponding GPIO must be implemented. Sus GPIO pins are GPIO_SUS0-7. All bits are in the resume well. Default for these bits are dependent on the state of the GPIO pins.
15:8	0b RW	**CORE GPIO SMI Enable Setting (CORE_GPIO_SMI_EN): (core_gpio_smi_en):** These bits are used to enable the corresponding GPIO to cause an SMI#.
7:0	0b RW	**SUS GPIO SMI Enable Setting (SUS_GPIO_SMI_EN): (sus_gpio_smi_en):** These bits are used to enable the corresponding GPIO to cause an SMI#.

30.7.9 UPRWC - USB Per-Port Registers Write Control (UPRWC)—Offset 3Ch

Access Method

Type: I/O Register
(Size: 32 bits)

UPRWC: [ACPI_BASE_ADDRESS] + 3Ch

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:9	Bit 8	Bits 7:2	Bit 1	Bit 0
reserved	we_sts	reserved1	usb_per_port_we	we_smi_en

Bit Range	Default & Access	Description
31:9	0b RO	**reserved:** Reserved.
8	0b RW	**Write Enable Status (WE_STS) (we_sts):** This bit gets set by hardware when the Per-Port Registers Write Enable bit is written from 0 to 1. This bit is cleared by software writing a 1b to this bit location. The setting condition takes precedence over the clearing condition in the event that both occur at once. When this bit is 1b and bit 0 is 1b, the INTEL_USB2_STS bit is set in the SMI_STS register.
7:2	0b RO	**reserved (reserved1):** Reserved.
1	0b RW	**USB Per-Port Registers Write Enable (USB_PER_PORT_WE) (usb_per_port_we):** This bit controls whether writes are enabled to the USB Port Power Off and Port Disable Override registers
0	0b RW	**Write Enable SMI Enable (WE_SMI_EN) (we_smi_en):** This bit enables the generation of SMI when the Per-Port Registers Write Enable (bit 1) is written from 0 to 1. Once written to 1b, this bit can not be cleared by software.

30.7.10 GPE_CTRL - General Purpose Event Control (GPE_CTRL)—Offset 40h

Access Method

Type: I/O Register
(Size: 32 bits)

GPE_CTRL: [ACPI_BASE_ADDRESS] + 40h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reserved (31:18), swgpe_ctrl (17), reserved1 (16:4), RSVD0 (3:0)

Bit Range	Default & Access	Description
31:18	0b RO	**reserved:** Reserved.
17	0b RW	**Software GPE Control (SWGPE_CTRL) (swgpe_ctrl):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0a_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. In addition to being reset by RSMRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip
16:4	0b RO	**reserved1:** Reserved.
3:0	0b RO	**RSVD0:** Reserved

30.7.11 PM2A_CNT_BLK - PM2a Control Block (PM2A_CNT_BLK)—Offset 50h

Access Method

Type: I/O Register
(Size: 32 bits)

PM2A_CNT_BLK: [ACPI_BASE_ADDRESS] + 50h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reserved (31:1), arb_dis (0)

Bit Range	Default & Access	Description
31:1	0b RO	**reserved:** Reserved.
0	0b RW	**ARB_DIS (ARB_DIS) (arb_dis):** This bit is essentially just a scratchpad bit for legacy software compatibility.

30.7.12 TCO_RLD: TCO Reload Register (TCO_RLD)—Offset 60h

Access Method

Type: I/O Register
(Size: 32 bits)

TCO_RLD: [ACPI_BASE_ADDRESS] + 60h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reserved (31:11), RSVD0 (10), tco_val (9:0)

Bit Range	Default & Access	Description
31:11	0b RO	**reserved:** Reserved.
10	0b RO	**RSVD0:** Reserved
9:0	0b RO	**TCO Timer Value (TCO_TVAL) (tco_val):** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

30.7.13 TCO_STS: TCO Timer Status (TCO_STS)—Offset 64h

Access Method

Type: I/O Register
(Size: 32 bits)

TCO_STS: [ACPI_BASE_ADDRESS] + 64h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: reserved2 (31:17), second_to_sts (16), reserved1 (15:4), tco_timeout (3), reserved (2:0)

Bit Range	Default & Access	Description
31:18	0b RO	**reserved (reserved2):** Reserved.
17	0b RW	**Second Timeout Status(SECOND_TO_STS) (second_to_sts):** PMC sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the PMC will reboot the system after the second timeout. The reboot is done by asserting PMU_PLTRST_B. This bit is only cleared by writing a 1 to this bit or by a RSMRST_B.
16:4	0b RO	**reserved (reserved1):** Reserved.
3	0b RW	**TCO Timeout (TCO_TIMEOUT) (tco_timeout):** Bit set to 1 by PMC to indicate that the SMI was caused by TCO timer reaching 0.
2:0	0b RO	**reserved:** Reserved.

30.7.14 TCO1_CNT: TCO Timer Control (TCO1_CNT)—Offset 68h

Access Method

Type: I/O Register
(Size: 32 bits)

TCO1_CNT: [ACPI_BASE_ADDRESS] + 68h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:22	Bits 21:20	Bits 19:13	Bit 12	Bit 11	Bits 10:0
reserved	os_policy	reserved2	tco_lock	tco_tmr_halt	reserved1

Bit Range	Default & Access	Description
31:22	0b RO	**reserved:** Reserved.
21:20	0b RW	**OS_POLICY (os_policy):** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Dont load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved
19:13	0b RO	**reserved (reserved2):** Reserved.
12	0b RW	**TCO Lock (TCO_LOCK) (tco_lock):** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	0b RW	**TCO Timer Halt (TCO_TMR_HALT) (tco_tmr_halt):** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0 = The TCO timer is enabled to count. This is the default.

Bit Range	Default & Access	Description
10:0	0b RO	**reserved1:** Reserved.

30.7.15 TCO_TMR: TCO Timer Register (TCO_TMR)—Offset 70h

Access Method

Type: I/O Register
(Size: 32 bits)

TCO_TMR: [ACPI_BASE_ADDRESS] + 70h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00040000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved1						tco_trld_val										reserved															

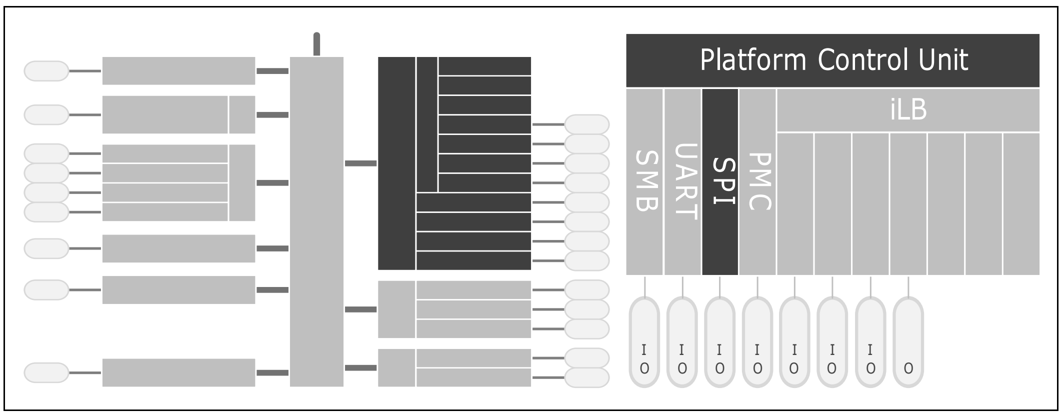
Bit Range	Default & Access	Description
31:26	0b RO	**reserved (reserved1):** Reserved.
25:16	004h RW	**TCO Timer reload value (TCO_TRLD_VAL) (tco_trld_val):** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 1 second, and thus allows timeouts ranging from 2 seconds to 1023 seconds. **Note:** The timer has an error of +/- 1 tick (1.0s). The TCO Timer will only count down in the S0 state.
15:0	0b RO	**reserved:** Reserved.

31 PCU – Serial Peripheral Interface (SPI)

The SoC implements a SPI controller as the interface for BIOS Flash storage. This SPI Flash device is also required to support firmware for the Trusted Execution Engine (required). The controller supports a maximum of two SPI Flash devices, using two chip select signals, with speeds of 20 MHz, 33 MHz or 50 MHz.

Note: The default interface speed is 20 MHz.

Note: SPI must operate in descriptor mode for correct operation of the SoC.



31.1 Signal Descriptions

Please see Chapter 2, “Physical Interfaces” for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal’s function

Table 298. SPI Signals

Signal Name	Direction Plat. Power	Description
PCU_SPI_CLK	O V1P8A	**SPI Clock:** When the bus is idle, the owner will drive the clock signal low.
PCU_SPI_CS[0]#	O V1P8A	**SPI Chip Select 0:** Used as the SPI bus request signal for the first SPI Flash device.
PCU_SPI_CS[1]#	O V1P8A	**SPI Chip Select 1:** Used as the SPI bus request signal for the second SPI Flash devices. *This signal is muxed and may be used by other functions.*
PCU_SPI_MISO	I V1P8A	**SPI Master IN Slave OUT:** Data input pin for the SoC.
PCU_SPI_MOSI	I/O V1P8A	**SPI Master OUT Slave IN:** Data output pin for the SoC. Operates as a second data input pin for the SoC when in Single Input, Dual Output Fast Read mode.

Note: All SPI signals are tri-stated with 20k ohm internal weak pull-up until PMC_CORE_PWROK is asserted.

31.2 Features

The SPI controller supports up to two SPI Flash devices using two separate chip select pins. Each SPI Flash device can be up to 16 MB. The SoC SPI interface supports 20 MHz, 33 MHz and 50 MHz SPI Flash devices. No other types of SPI devices are supported.

Communication on the SPI bus is done with a Master – Slave protocol. The Slave is connected to the SoC and is implemented as a tri-state bus.

Note: When GCS.BBS = 00b, LPC is selected as the location for BIOS. The SPI Flash may still contain data and firmware for other SoC functionality.

Note: When GCS.BBS =11b and a SPI device is detected by the SoC, LPC based BIOS Flash is disabled.

31.2.1 Operation Mode Feature Overview

The SPI controller has two operational modes, Non-Descriptor and Descriptor.

31.2.1.1 Non-Descriptor Mode

If no valid signature is read (either because there is no SPI Flash, or there is an SPI Flash with no valid descriptor), the Flash Controller will operate in a Non-Descriptor mode.

The following features are not supported in Non-Descriptor mode:

- Trusted Execution Engine
- Secure Boot
- Soft Straps
- Two SPI Flash device support
- Hardware sequencing access
- Descriptor-based security access restrictions

Note: When operating in Non-Descriptor mode, software sequencing must be used to access the Flash.

Note: When operating in Non-Descriptor Mode, and a SPI Flash is attached to the SoC, it is required that the Flash Valid Signature, at offset 10h of the Flash Descriptor, does not equal the expected valid value (0FF0A55Ah) or the SPI Controller will wrongly interpret that it has a valid signature and that a Flash Descriptor has been implemented.

31.2.2 Descriptor Mode

Descriptor Mode is required to enable many features of the SoC:

- Trusted Execution Engine
- Secure Boot
- PCI Express* root port configuration
- Supports for two SPI components using two separate chip select pins
- Hardware enforced security restricting master accesses to different regions
- Soft Strap region providing the ability to use Flash NVM to remove the need for pull-up/pull-down resistors for strapping SoC features
- Support for the SPI Fast Read instruction and frequencies greater than 20 MHz
- Support for Single Input, Dual Output Fast reads
- Use of standardized Flash instruction set

SPI Flash Regions

In Descriptor Mode the Flash is divided into five separate regions:

Table 299. SPI Flash Regions

Region	Content
0	Flash Descriptor
1	BIOS
2	Trusted Execution Engine
3	Reserved
4	Platform Data

Only two masters can access the 3 regions: The SoC CPU core running BIOS code and the Trusted Execution Engine. The only required region is Region 0, the Flash Descriptor. Region 0 must be located in the first sector of Device 0.

Flash Regions Sizes

SPI Flash space requirements differ by platform and configuration. Table 300 indicates the space needed in the Flash for each region.

Table 300. Region Size Versus Erase Granularity of Flash Components

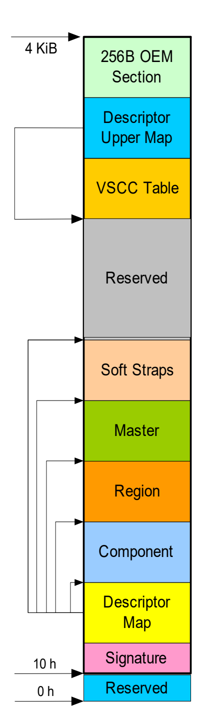
Region	Size with 4 KB Blocks	Size with 8 KB Blocks	Size with 64 KB Blocks
Descriptor	4 KB	8 KB	64 KB
BIOS	Varies by Platform	Varies by Platform	Varies by Platform
Trusted Execution Engine	Varies by Platform	Varies by Platform	Varies by Platform

31.2.3 Flash Descriptor

The maximum size of the Flash Descriptor is 4 KB. If the block/sector size of the SPI Flash device is greater than 4 KB, the Flash descriptor will only use the first 4 KB of the first block. The Flash descriptor requires its own block at the bottom of memory (00h). The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read only when the system containing the SoC leaves the manufacturing floor.

The Flash Descriptor is made up of eleven sections as indicated in below figure.

Figure 131. Flash Descriptor Sections



- The **Reserved** section at offset 0h is related to functionality not supported by the SoC.
- The **Signature** section selects Descriptor Mode as well as verifies if the Flash is programmed and functioning. The data at the bottom of the Flash (offset 10h) must be 0FF0A55Ah in order to be in Descriptor mode.
- The **Descriptor Map** section defines the logical structure of the Flash in addition to the number of components used.
- The **Component** section has information about the SPI Flash in the system including:
  - — Density of each component
  - — Illegal instructions (such as chip erase)
  - — Frequencies for read, fast read and write/erase instructions.
- The **Region** section points to the four other regions as well as the size of each region.
- The **Master** region contains the security settings for the Flash, granting read/write permissions for each region and identifying each master by a requestor ID.
- The **Soft Straps** section contains parameter bits that can be used to configure SoC features and/or behaviors.

- The **Reserved** section between the top of the **Soft Straps** section and the bottom of the **VSCC Table** is reserved for future SoC usages.
- The **VSCC Table** section holds the JEDEC ID and the VSCC (Vendor Specific Component Capabilities) information of the entire SPI Flash supported by the NVM image.
- The **Descriptor Upper Map** section determines the length and base address of the **VSCC Table** section.
- The **OEM Section** is 256 Bytes reserved at the top of the Flash Descriptor for use by an OEM.

31.2.3.1 Master Section

The Master section defines read and write access setting for each region of the SPI device, when the SPI controller is running in Descriptor mode. The master region recognize twos masters: SoC CPU core running BIOS code and the Trusted Execution Engine.

Note: Each master is only allowed to do direct reads of its primary regions. The Trusted Execution Engine is may also do a direct read of the BIOS region if it has been given read access to that region. See Section 31.2.4.1, “Direct Access” on page 4382 for further details on direct reads.

Table 301. Region Access Control

Master Read/Write Access		
Region	**BIOS**	**Trusted Execution Engine**
Descriptor	N/A	N/A
BIOS	CPU core and BIOS can always read from and write to BIOS Region	Read / Write
Trusted Execution Engine	Read / Write	Trusted Execution can always read from and write to Trusted Execution Engine Region
Platform Data	N/A	N/A

31.2.3.2 Invalid Flash Descriptor Handling

The SoC will respond to an invalid Flash Descriptor with the following:

- The SPI controller will operate in Non-Descriptor mode.
- If the BBS strap (see Section 31.2.2 for details) is set to 1, BIOS direct read access will be forwarded to the SPI Controller without any address translation.
- The HSFSTS.FDV register bits remains at 0b.

- All security checks are disabled and the entire Flash is open for reading and writing. No restriction on the 4k crossing.
- Trusted Execution Engine direct read accesses will not be handled, and the SPI controller will return all 1's.

Note: To ensure BIOS boot access even when the Flash Descriptor is invalid the BIOS region can be placed at the top of Flash Component 0. Placing the BIOS region in any other location will necessitate a full reprogramming of the Flash before boot is possible from that Flash.

31.2.3.3 Descriptor Security Override Strap

A strap is implemented on GPIO_S0_SC[065] to allow descriptor security to be overridden when the strap is sampled low.

If the strap is set (0b), it will have the following effect:

- The Master Region Read Access and Master Region Write Access permissions that were loaded from the Flash Descriptor Master Section will be overridden giving every master read and write permissions to the entire Flash component including areas outside the defined regions.
- BIOS Protected Range 4 (PR4), if enabled by soft strap, will be overridden so that all masters are able to write to the PR4. The PR4 base and limit addresses are fetched and received from soft strap.

31.2.4 Flash Access

There are two types of Flash accesses: Direct Access and Program Register Access.

31.2.4.1 Direct Access

- Direct writes are not allowed for any master.
- The SoC CPU core is only allowed to do a direct read of the BIOS region
- The Trusted Execution Engine is only allowed to do a direct read of the Trusted Execution Engine region. It may also do a direct read of the BIOS region if it has been given read access to that region.

Note: Trusted Execution Engine region direct reads are not supported when the SPI controller is operating in Non-Descriptor mode. The SPI controller returns all 1s if a direct read is attempted.

31.2.4.2 Security

- Calculated Flash Linear Address (FLA) must fall between primary region base/limit

Note: During non descriptor mode, the Flash Physical Address is used instead. Only the two BIOS ranges at the E0000h and F0000h segments just below 1MB are supported.

- Direct Read Cache contents are reset to 0's on a read from a different master

31.2.4.3 Program Register Access

- Reads, Writes and Erases are all supported.
- Program Register Access may use Hardware or Software Sequencing. See Section 31.3.1, "Hardware vs. Software Sequencing" on page 4389 for further information.
- Program Register Accesses are not allowed to cross a 4 KB boundary and can not issue a command that might extend across two components
- Software programs the FLA corresponding to the region desired
  - Software must read the devices Primary Region Base/Limit address to create a FLA.

Each master accesses the Flash through a set of memory mapped registers that are dedicated to each device.

There are two separate control and status registers that software can use when using register access to the Flash. The Hardware Sequencing control/status registers rely on hardware to issue appropriate Flash instructions and atomic sequences. The Software Sequencer puts control into the hands of the software for what instructions to issue and when.

The goal is to support all Flash components through hardware sequencing. Software sequencing is intended only for a back-up strategy.

Note: Software sequencing is required when operating in a non-descriptor mode.

31.2.4.4 Security

- Only primary region masters can access the registers
- Masters are only allowed to read or write those regions they have read/write permission
- Using the Flash region access permissions, one master can give another master read/write permissions to their area
- Using the five Protected Range registers, each master can add separate read/write protection above that granted in the Flash Descriptor for their own accesses
  - Example: BIOS may want to protect different regions of BIOS from being erased
  - Ranges can extend across region boundaries

31.2.5 Serial Flash Device Compatibility Requirements

A variety of serial Flash devices exist in the market. For a serial Flash device to be compatible with the SoC SPI bus, it must meet the minimum requirements detailed in the following sections.

31.2.5.1 BIOS SPI Flash Requirements

The SPI Flash device must meet the following minimum requirements when used explicitly for system BIOS storage.

- Erase size capability of at least one of the following: 64 Kbytes, 8 Kbytes, 4 Kbytes, or 256 bytes.
- Device must support multiple writes to a page without requiring a preceding erase cycle (Refer to Section 31.2.6.)
- Serial Flash device must ignore the upper address bits such that an address of FFFFFFh aliases to the top of the Flash memory.
- SPI Compatible Mode 0 support (clock phase is 0 and data is latched on the rising edge of the clock).
- If the device receives a command that is not supported or incomplete (less than 8 bits), the device must complete the cycle gracefully without any impact on the Flash content.
- An erase command (page, sector, block, chip, etc.) must set all bits inside the designated area (page, sector, block, chip, etc.) to 1 (Fh).
- Status Register bit 0 must be set to 1 when a write, erase or write to status register is in progress and cleared to 0 when a write or erase is NOT in progress.
- Devices requiring the Write Enable command must automatically clear the Write Enable Latch at the end of Data Program instructions.
- Byte write must be supported. The flexibility to perform a write between 1 byte to 64 bytes is recommended.
- Hardware Sequencing requirements are optional in BIOS only platforms.
- SPI Flash devices that do not meet hardware sequencing command set requirements may work in BIOS only platforms using software sequencing.
- If implementing two SPI flash devices, both devices must have the same erasable block/sector size. Additionally, the first device must be of a binary size.

31.2.5.2 Intel Trusted Execution Engine Firmware SPI Flash Requirements

Intel Trusted Execution Engine Firmware must meet all the requirements in Section 31.2.5.1 plus:

- Hardware sequencing
- The Flash device must have a uniform 4-KB erasable block throughout the entire device or have 64 KB blocks with the first block (lowest address) divided into 4-KB or 8-KB blocks.
- The write protection scheme must meet SPI Flash unlocking requirements for the Trusted Execution Engine

SPI Flash Unlocking Requirements for the Trusted Execution Engine

Flash devices must be globally unlocked (read, write and erase access on the Trusted Execution Engine region) from power on by writing 00h to the Flash's status register to disable write protection.

If the status register must be unprotected, it must use the enable write status register command 50h or write enable 06h.

Opcode 01h (write to status register) must then be used to write a single byte of 00h into the status register. This must unlock the entire device. If the SPI Flash's status register has non-volatile bits that must be written to, bits [5:2] of the Flash's status register must be all 0h to indicate that the Flash is unlocked.

If bits [5:2] return a non zero values, the Trusted Execution Engine firmware will send a write of 00h to the status register. This must keep the Flash part unlocked.

If there is no need to execute a write enable on the status register, then opcodes 06h and 50h must be ignored.

After global unlock, the BIOS has the ability to lock down small sections of the Flash as long as they do not involve the Trusted Execution Engine.

31.2.5.3 Hardware Sequencing Requirements

Below table contains a list of commands and the associated opcodes that a SPI-based serial Flash device must support in order to be compatible with hardware sequencing.

Table 302. Hardware Sequencing Commands and Opcode Requirements

Commands	Opcode	Notes
Write to Status Register	01h	Writes a byte to SPI Flash's status register. Enable Write to Status Register command must be run prior to this command.
Program Data	02h	Single byte or 64 byte write as determined by Flash part capabilities and software.
Read Data	03h	
Write Disable	04h	
Read Status	05h	Outputs contents of SPI Flash's status register
Write Enable	06h	
Fast Read	0Bh	
Enable Write to Status Register	50h	Enables a bit in the status register to allow an update to the status register
Erase	Programmabl e	Uses the value from LVSSC.LEO register or UVSSC.UEO register depending on the FLA and whether it is below or above the FPBA respectively

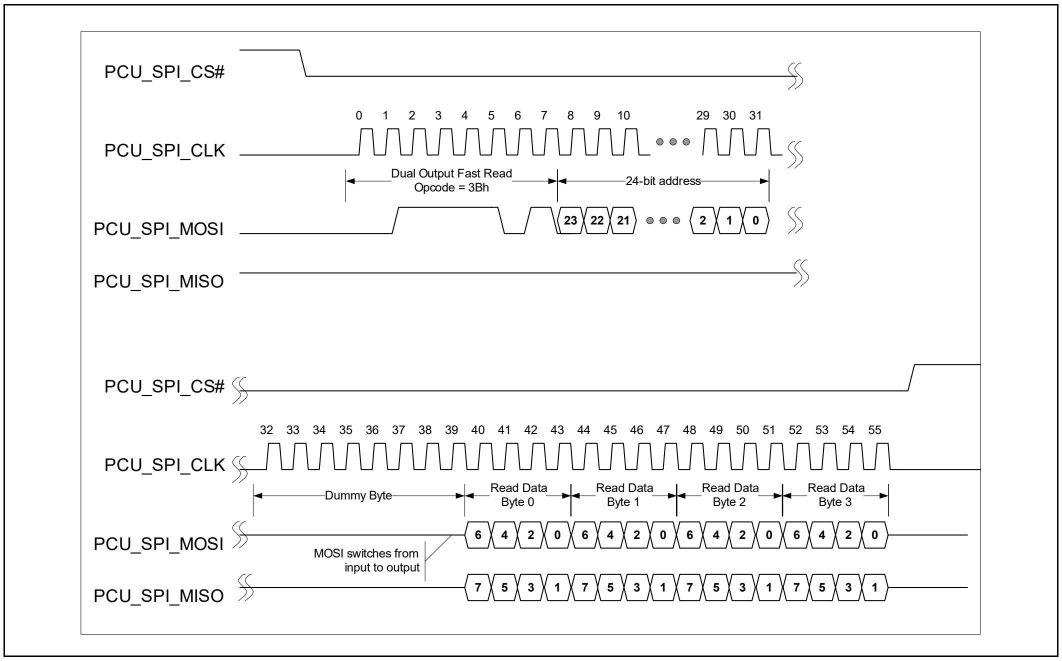
Single Input, Dual Output Fast Read

The SPI controller supports the functionality of a single input, dual output fast read: Opcode 3Bh. This instruction has the same timing (including a dummy byte) and the same frequencies as the Fast Read instruction, with the difference that the read data from the Flash is presented on both the MISO and MOSI pins. During a Dual Read instruction, the odd data bits are on the MISO pin and the even data bits are on the MOSI pin.

Note: When Dual Output Fast Read Support is enabled the Fast Read Support must be enabled as well.

Note: Micronix* SPI Flash uses a different opcode for dual fast read, and requires that during the address phase that the address bits are sent on both MOSI and MISO. The SoC does not support this implementation of the protocol.

Figure 132.Dual Output Fast Read Timing



JEDEC ID

Since each serial Flash device may have unique capabilities and commands, the JEDEC ID is the necessary mechanism for identifying the device so the uniqueness of the device can be comprehended by the controller (master). The JEDEC ID uses the opcode 9Fh and a specified implementation and usage model. This JEDEC Standard Manufacturer and Device ID read method is defined in Standard JESD21-C, PRN03-NV.

Error Correction and Detection

If the first 8 bits specify an opcode which is not supported the slave will not respond and wait for the next high to low transition on PCU_SPI_CS[1:0]#. The SPI controller should automatically discard 8 bit words that were not completely received upon de-assertion of the signal.

Any other error correction or detection mechanisms must be implemented in firmware and/or software.

31.2.6 Multiple Page Write Usage Model

The BIOS and Trusted Execution Engine firmware usage models require that the serial Flash device support multiple writes to a page (minimum of 512 writes) without requiring a preceding erase command. The BIOS commonly uses capabilities such as counters that are used for error logging and system boot progress logging. These counters are typically implemented by using byte-writes to 'increment' the bits within a page that have been designated as the counter. The Trusted Execution Engine firmware usage model requires the capability for multiple data updates within any given page. These data updates occur using byte-writes without executing a preceding erase to the given page. Both the BIOS and Trusted Execution Engine firmware multiple page write usage models apply to sequential and non-sequential data writes.

This usage model requirement is based on any given bit only being written once from a '1' to a '0'without requiring the preceding erase. An erase would be required to change bits back to the 1 state.

31.2.7 Soft Flash Protection

There are two types of Flash protection that are not defined in the Flash descriptor supported by the SPI controller:

1. Flash Range Read and Write Protection
2. Global Write Protection

31.2.7.1 Flash Range Read and Write Protection

The SPI controller provides a method for blocking reads and writes to specific ranges in the Flash when the Protected Ranges are enabled. This is achieved by checking the read or write cycle type and the address of the requested command against the base and limit fields of a Read or Write Protected range. Protected range registers are only applied to Programmed Register accesses and have no effect on Direct Reads.

Note: Once BIOS has locked down the Protected BIOS Range registers, this mechanism remains in place until the next system reset.

31.2.7.2 Global Write Protection

The SPI controller has a Write Protection Disable (BCR.WPD) configuration bit. When BCR.WPD=0b, BIOS is not able to perform any write or erase commands to the Flash. When BCR.WPD=1b, protection against BIOS erase and rewrite is disabled. When the lock enable (BCR.LE) bit is set, the BIOS can disable this protection only during System Management Mode (SMM) execution.

If BCR.LE=1b, the SPI controller confirms that only SMM code succeeds to set BCR.WPD=1b. In addition, if BCS.SMIWPEN=1b, the SPI controller should initiate an SMI when non SMM code tries to set BCR.WPD=1b.

31.2.8 SPI Flash Device Recommended Pinout

This table contains the recommended serial Flash device pin-out for an 8-pin device. Use of the recommended pin-out on an 8-pin device reduces complexities involved with designing the serial Flash device onto a motherboard and allows for support of a common footprint usage model (refer to Section 31.2.9.1).

Table 303. Recommended Pinout for 8-Pin Serial Flash Device

Pin #	Signal
1	Chips Select
2	Data Output
3	Write Protect
4	Ground
5	Data Input
6	Serial Clock
7	Hold / Reset
8	Supply Voltage

Although an 8-pin device is preferred over a 16-pin device due to footprint compatibility, Table 304 contains the recommended serial Flash device pin-out for a 16-pin SOIC.

31.2.9 Serial Flash Device Package

Table 304. Recommended Pinout for 16-Pin Serial Flash Device

Pin #	Signal	Pin #	Signal
1	Hold / Reset	9	Write Protect
2	Supply Voltage	10	Ground
3	No Connect	11	No Connect
4	No Connect	12	No Connect
5	No Connect	13	No Connect

Table 304. Recommended Pinout for 16-Pin Serial Flash Device

Pin #	Signal	Pin #	Signal
6	No Connect	14	No Connect
7	Chip Select	15	Serial Data In
8	Serial Data Out	16	Serial Clock

31.2.9.1 Common Footprint Usage Model

To minimize platform motherboard redesign and to enable platform Bill of Material (BOM) selectability, many OEMs design their motherboard with a single common footprint. This common footprint allows the population of a soldered down device or a socket that accepts a leadless device. This enables the board manufacturer to support, using selection of the appropriate BOM, either of these solutions on the same system without requiring any board redesign.

The common footprint usage model is desirable during system debug and by Flash content developers since the leadless device can be easily removed and reprogrammed without damage to device leads. When the board and Flash content is mature for high-volume production, both the socketed leadless solution and the soldered down leaded solution are available through BOM selection.

31.2.9.2 Serial Flash Device Package Recommendations

It is highly recommended that the common footprint usage model be supported. An example of how this can be accomplished is as follows:

- The recommended pinout for 8-pin serial Flash devices is used (refer to Table 303).
- The 8-pin device is supported in either an 8-contact VDFPN (6x5 mm MLP) package or an 8-contact WSON (5x6 mm) package. These packages can fit into a socket that is land pattern compatible with the wide body SO8 package.
- The 8-pin device is supported in the SO8 (150 mil) and in the wide-body SO8 (200 mil) packages.
- The 16-pin device is supported in the SO16 (300 mil) package.

31.3 Use

31.3.1 Hardware vs. Software Sequencing

Hardware and Software sequencing are the two methods the SoC uses to communicate with the Flash via programming registers for each of the three masters.

31.3.1.1 Hardware Sequencing

Hardware sequencing has a predefined list of opcodes, see Table 302 for more details, with only the erase opcode being programmable. This mode is only available if the descriptor is present and valid. Security Engine firmware must use HW sequencing, so

BIOS must properly set up the SoC to account for this. The Host VSCC registers and VSCC Table have to be correctly configured for BIOS and Security Engine have read/ write access to SPI.

31.3.1.2 Software Sequencing

All commands other than the standard (memory) reads must be programmed by the software in the Software Sequencing Control, Flash Address, Flash Data, and Opcode configuration registers. Software must issue either Read ID or Read JEDEC ID, or a combination of the two to determine what Flash component is attached. Based on the Read ID, software can determine the appropriate Opcode instructions sets to set in the program registers and at what SPI frequency to run the command.

Software must program the Flash Linear Address for all commands, even for those commands that don't require address such as the Read ID or Read Status. This is because the SPI controller uses the address to determine which chip select to use.

The opcode type and data byte count fields determine how many clocks to run before deasserting the chip enable. The Flash data is always shifted in for the number of bytes specified and the Flash Data out is always shifted out for the number of data bytes specified. Note that the hardware restricts the burst lengths that are allowed.

A status bit indicates when the cycle has completed on the SPI port allowing the host to know when read results can be checked and/or when to initiate a new command.

The controller also provides the “Atomic Cycle Sequence” for performing erases and writes to the SPI Flash. When this bit is 1 (and the Go bit is written to 1), a sequence of cycles is performed on the SPI interface without allowing other SPI device to arbitrate and interleave cycles to the Flash device. In this case, the specified cycle is preceded by the Prefix Command (8-bit programmable Opcode) and followed by repeated reads to the Status Register (Opcode 05h) until bit 0 indicates the cycle has completed. The hardware does not attempt to check that the programmed cycle is a write or erase.

If a Programmed Access is initiated (Cycle Go written to 1) while the SPI controller is already busy with a Direct Memory Read, then the SPI Host hardware will hold the new Programmed Access pending until the preceding SPI access completes.

Once the SPI controller has committed to running a programmed access, subsequent writes to the programmed cycle registers that occur before it has completed will not modify the original transaction and will result in the assertion of the FCERR bit. Software should never purposely behave in this way and rely on this behavior. However, the FCERR bit provides basic error-reporting in this situation. Writes to the following registers cause the FCERR bit assertion in this situation:

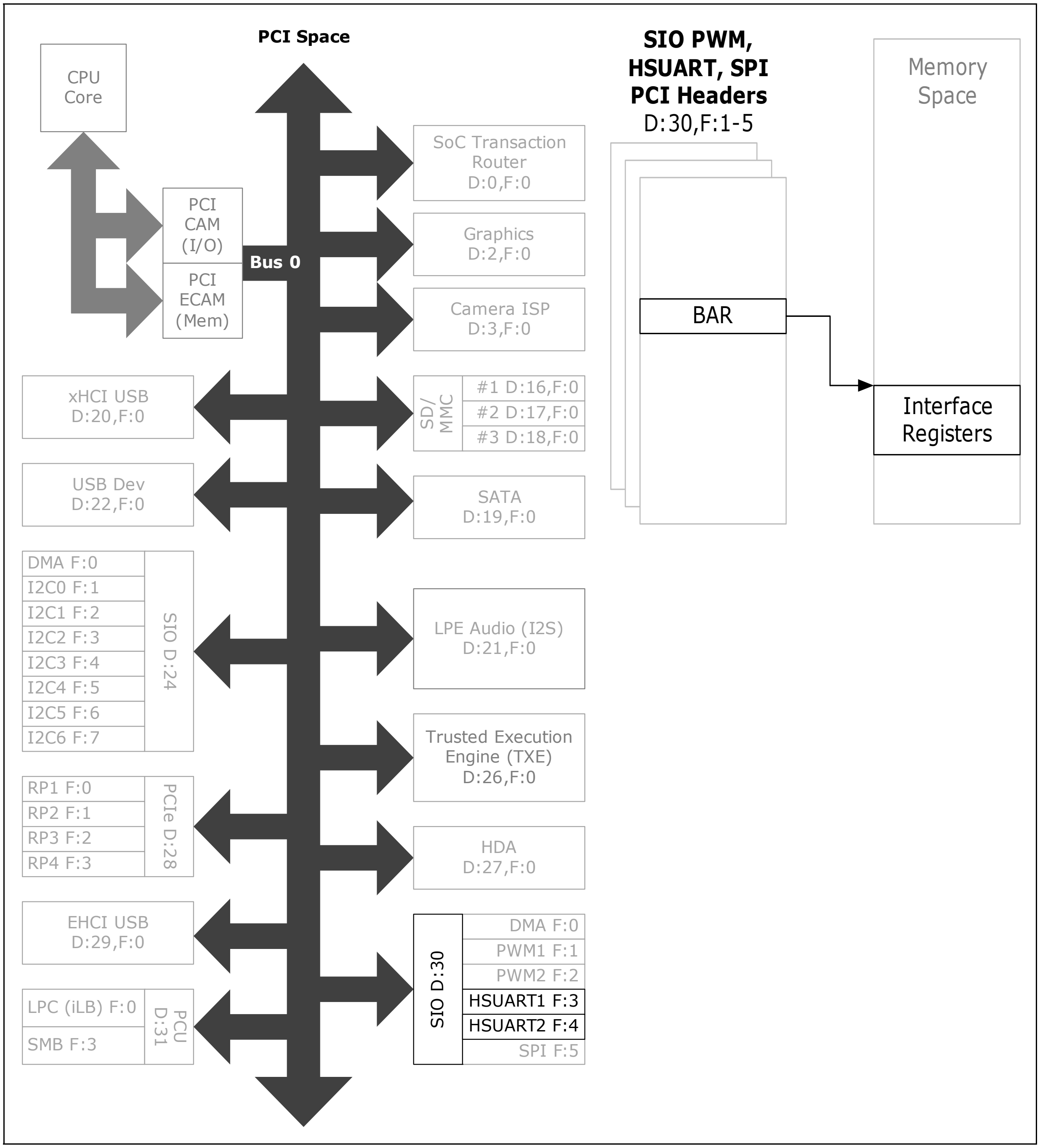
- Software Sequencing Control
- Software Sequencing Address
- SPI Data

With the exception of Illegal Opcodes, the SPI controller does not police which opcodes are valid to be used in SW Sequencing. For example, if SW programs a Dual Output Fast Read opcode, then the Dual Output Fast Read cycle will be issued, independent of whether the Dual Output Fast Read enable bit was set in the component descriptor section.

31.4 Register Map

Refer to Chapter 3, “Register Access Methods” and Chapter 4, “Mapping Address Spaces” for additional information.

Figure 133.SIO - HSUART Register Map



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31.5 PCU SPI for Firmware Memory Mapped I/O Registers

Table 305. Summary of PCU SPI for Firmware Memory Mapped I/O Registers—SPI_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"BFPREG (BIOS_Flash_Primary_Region_bios)—Offset 0h" on page 4394	00001FFFh
4h	2	"HSFSTS (Hardware_Sequencing_Flash_Status_bios)—Offset 4h" on page 4395	0000h
6h	2	"HSFCTL (Hardware_Sequencing_Flash_Control_bios)—Offset 6h" on page 4396	0000h
8h	4	"FADDR (Flash_Address_bios)—Offset 8h" on page 4397	00000000h
10h	4	"FDATA0 (Flash_Data_0_bios)—Offset 10h" on page 4397	00000000h
14h	4	"FDATA1 (Flash_Data_1_bios)—Offset 14h" on page 4398	00000000h
18h	4	"FDATA2 (Flash_Data_2_bios)—Offset 18h" on page 4398	00000000h
1Ch	4	"FDATA3 (Flash_Data_3_bios)—Offset 1Ch" on page 4399	00000000h
20h	4	"FDATA4 (Flash_Data_4_bios)—Offset 20h" on page 4399	00000000h
24h	4	"FDATA5 (Flash_Data_5_bios)—Offset 24h" on page 4400	00000000h
28h	4	"FDATA6 (Flash_Data_6_bios)—Offset 28h" on page 4400	00000000h
2Ch	4	"FDATA7 (Flash_Data_7_bios)—Offset 2Ch" on page 4401	00000000h
30h	4	"FDATA8 (Flash_Data_8_bios)—Offset 30h" on page 4401	00000000h
34h	4	"FDATA9 (Flash_Data_9_bios)—Offset 34h" on page 4402	00000000h
38h	4	"FDATA10 (Flash_Data_10_bios)—Offset 38h" on page 4402	00000000h
3Ch	4	"FDATA11 (Flash_Data_11_bios)—Offset 3Ch" on page 4403	00000000h
40h	4	"FDATA12 (Flash_Data_12_bios)—Offset 40h" on page 4403	00000000h
44h	4	"FDATA13 (Flash_Data_13_bios)—Offset 44h" on page 4404	00000000h
48h	4	"FDATA14 (Flash_Data_14_bios)—Offset 48h" on page 4404	00000000h
4Ch	4	"FDATA15 (Flash_Data_15_bios)—Offset 4Ch" on page 4405	00000000h
50h	4	"FRACC (Flash_Region_Access_Permissions_bios)—Offset 50h" on page 4405	00000202h
54h	4	"FREG0 (Flash_Region_0_bios)—Offset 54h" on page 4406	00001FFFh
58h	4	"FREG1 (Flash_Region_1_bios)—Offset 58h" on page 4407	00001FFFh
5Ch	4	"FREG2 (Flash_Region_2_bios)—Offset 5Ch" on page 4407	00001FFFh
60h	4	"FREG3 (Flash_Region_3_bios)—Offset 60h" on page 4408	00001FFFh
64h	4	"FREG4 (Flash_Region_4_bios)—Offset 64h" on page 4408	00001FFFh
74h	4	"PR0 (Protected_Range_0_bios)—Offset 74h" on page 4409	00000000h
78h	4	"PR1 (Protected_Range_1_bios)—Offset 78h" on page 4410	00000000h
7Ch	4	"PR2 (Protected_Range_2_bios)—Offset 7Ch" on page 4411	00000000h
80h	4	"PR3 (Protected_Range_3_bios)—Offset 80h" on page 4411	00000000h
84h	4	"PR4 (Protected_Range_4_bios)—Offset 84h" on page 4412	00000000h
90h	4	"SSFCTLSTS (Software_Sequencing_Flash_Control_Status_bios)—Offset 90h" on page 4413	F8000000h
94h	2	"PREOP (Prefix_Opcode_Configuration_bios)—Offset 94h" on page 4415	0000h
96h	2	"OPTYPE (Opcode_Type_Configuration_bios)—Offset 96h" on page 4415	0000h
98h	4	"OPMENU0 (Opcode_Menu_Configuration_0_bios)—Offset 98h" on page 4416	00000000h

Table 305. Summary of PCU SPI for Firmware Memory Mapped I/O Registers—SPI_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
9Ch	4	“OPMENU1 (Opcode_Menu_Configuration_1_bios)—Offset 9Ch” on page 4417	00000000h
A4h	4	“LOCK (Individual_Lock_Register)—Offset A4h” on page 4418	00000000h
B0h	4	“FDOC (Flash_Descriptor_Observability_Control_bios)—Offset B0h” on page 4419	00000000h
B4h	4	“FDOD (Flash_Descriptor_Observability_Data_bios)—Offset B4h” on page 4420	00000000h
C0h	4	“AFC (Additional_Flash_Control_bios)—Offset C0h” on page 4420	00000000h
C4h	4	“LVSCC (Lower_Vendor_Specific_Component_Capabilities_bios)—Offset C4h” on page 4421	00000000h
C8h	4	“UVSCC (Upper_Vendor_Specific_Component_Capabilities_bios)—Offset C8h” on page 4422	00000000h
D0h	4	“FPB (Flash_Partition_Boundary_bios)—Offset D0h” on page 4423	00000000h
F8h	4	“SCS (SMI_Control_Status_Register_bios)—Offset F8h” on page 4424	00000080h
FCh	4	“BCR (BIOS_Control_Register_bios)—Offset FCh” on page 4425	00000020h
100h	4	“TCGC (Trunk_Clock_Gating_Control_bios)—Offset 100h” on page 4426	00000510h

31.5.1 BFPREG (BIOS_Flash_Primary_Region_bios)—Offset 0h

BIOS flash primary region addresses

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

BIOS_Flash_Primary_Region_bios: [SPI_BASE_ADDRESS] + 0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
RSVD0			PRL													RSVD1			PRB												

Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**BIOS Flash Primary Region Limit (PRL):** This specifies address bits 24:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG1.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**BIOS Flash Primary Region Base (PRB):** This specifies address bits 24:12 for the Primary Region Base The value in this register iloaded from the contents in the Flash Descriptor.FLREG1.Region Base

31.5.2 HSFSTS (Hardware_Sequencing_Flash_Status_bios)—Offset 4h

Hardware sequencing flash status Note: If operating in Non-Descriptor mode, the Software Sequencing Flash Status register must be used.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Hardware_Sequencing_Flash_Status_bios: [SPI_BASE_ADDRESS] + 4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FLOCKDN	FDV	FDOPSS	RSVD0							SCIP	BERASE		AEL	FCERR	FDONE

Bit Range	Default & Access	Description
15	0b RW/L	**Flash Configuration Lock-Down (FLOCKDN):** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
14	0b RO	**Flash Descriptor Valid (FDV):** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1 , software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	0b RO	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register reflects the value the Flash Descriptor Override Pin-Strap. '1': No override '0': The Flash Descriptor Overide strap is set
12:6	0b RO	**RSVD0:** Reserved
5	0b RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	00b RO	**Block/Sector Erase Size (BERASE):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 : 256 Byte 01 : 4K Byte 10 : 8K Byte 11 : 64K Byte If the FLA (FPBA then this field reflects the value in the LVSCC.LBES register. If the FLA)= FPBA then this field reflects the value in the UVSCC.UBES register.
2	0b RW/1C	**Access Error Log (AEL):** Hardware sets this bit to a 1 when a direct read was made by BIOS that violated the security restrictions. Or , when a SB transaction to read/write one of the BIOS registers was accepted with bad SAI - see security table. This bit has no affect on indirect accesses. This bit is cleared by software writing a 1.
1	0b RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occures. Software must clear this bit before setting the FLASH Cycle GO bit in this register.

Bit Range	Default & Access	Description
0	0b RW/1C	**Flash Cycle Done (FDONE):** The SPI controller sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

31.5.3 HSFCTL (Hardware_Sequencing_Flash_Control_bios)—Offset 6h

Hardware sequencing flash control.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Hardware_Sequencing_Flash_Control_bios: [SPI_BASE_ADDRESS] + 6h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FSMIE	RSVD0	FDBC						RRWSP					FCYCLE		FGO

Bit Range	Default & Access	Description
15	0b RW	**Flash SPI SMI# Enable (FSMIE):** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
14	0b RO	**RSVD0:** Reserved
13:8	00h RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b reprenting 1 byte and 111111b representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	00h RW	**Reserved RW Scratch Pad (RRWSP):** Reserved: Scratch Pad bits that are R/W to be used during ECO
2:1	00b RW	**FLASH Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 Read (1 up to 64 bytes by setting FDBC) 01 Reserved 10 Write (1 up to 64 bytes by setting FDBC) 11 Block Erase Implementation Note: if reserved 2'b01 is programmed to this field, flash controller will handle it as if it is 00 (Read)
0	0b RW/SE	**Flash Cycle Go (FGO):** A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

31.5.4 FADDR (Flash_Address_bios)—Offset 8h

Flash address

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Address_bios: [SPI_BASE_ADDRESS] + 8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

RSVD0 (31:25)	FLA (24:0)

Bit Range	Default & Access	Description
31:25	0b RO	**RSVD0:** Reserved
24:0	00000000h RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus. When operating in Tekoa mode bit 24 is ignored and the FLA[lb]13:0[rb] is the FPA.

31.5.5 FDATA0 (Flash_Data_0_bios)—Offset 10h

Flash data #0

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Data_0_bios: [SPI_BASE_ADDRESS] + 10h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

FD0 (31:0)

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 0 (FD0):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- 8-23-22- 16-31 24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions, byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

31.5.6 FDATA1 (Flash_Data_1_bios)—Offset 14h

Flash data #1

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Data_1_bios: [SPI_BASE_ADDRESS] + 14h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD1

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 1 (FD1):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD0 has completely shifted in/out.

31.5.7 FDATA2 (Flash_Data_2_bios)—Offset 18h

Flash data #2

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Data_2_bios: [SPI_BASE_ADDRESS] + 18h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD2

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 2 (FD2):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD1 has completely shifted in/out.

31.5.8 FDATA3 (Flash_Data_3_bios)—Offset 1Ch

Flash data #3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_3_bios: [SPI_BASE_ADDRESS] + 1Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD3

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 3 (FD3):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD2 has completely shifted in/out.

31.5.9 FDATA4 (Flash_Data_4_bios)—Offset 20h

Flash data #4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_4_bios: [SPI_BASE_ADDRESS] + 20h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD4

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 4 (FD4):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD3 has completely shifted in/out.

31.5.10 FDATA5 (Flash_Data_5_bios)—Offset 24h

Flash data #5

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Data_5_bios: [SPI_BASE_ADDRESS] + 24h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD5

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 5 (FD5):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD4 has completely shifted in/out.

31.5.11 FDATA6 (Flash_Data_6_bios)—Offset 28h

Flash data #6

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Data_6_bios: [SPI_BASE_ADDRESS] + 28h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD6

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 6 (FD6):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD5 has completely shifted in/out.

31.5.12 FDATA7 (Flash_Data_7_bios)—Offset 2Ch

Flash data #7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_7_bios: [SPI_BASE_ADDRESS] + 2Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FD7																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 7 (FD7):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD6 has completely shifted in/out.

31.5.13 FDATA8 (Flash_Data_8_bios)—Offset 30h

Flash data #8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_8_bios: [SPI_BASE_ADDRESS] + 30h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FD8																															

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 8 (FD8):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD7 has completely shifted in/out.

31.5.14 FDATA9 (Flash_Data_9_bios)—Offset 34h

Flash data #9

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_9_bios: [SPI_BASE_ADDRESS] + 34h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD9

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 9 (FD9):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD8 has completely shifted in/out.

31.5.15 FDATA10 (Flash_Data_10_bios)—Offset 38h

Flash data #10

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_10_bios: [SPI_BASE_ADDRESS] + 38h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD10

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 10 (FD10):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD9 has completely shifted in/out.

31.5.16 FDATA11 (Flash_Data_11_bios)—Offset 3Ch

Flash data #11

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_11_bios: [SPI_BASE_ADDRESS] + 3Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD11

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 11 (FD11):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD10 has completely shifted in/out.

31.5.17 FDATA12 (Flash_Data_12_bios)—Offset 40h

Flash data #12

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_12_bios: [SPI_BASE_ADDRESS] + 40h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD12

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 12 (FD12):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD11 has completely shifted in/out.

31.5.18 FDATA13 (Flash_Data_13_bios)—Offset 44h

Flash data #13

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Data_13_bios: [SPI_BASE_ADDRESS] + 44h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
FD13							

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 13 (FD13):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD12 has completely shifted in/out.

31.5.19 FDATA14 (Flash_Data_14_bios)—Offset 48h

Flash data #14

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Data_14_bios: [SPI_BASE_ADDRESS] + 48h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
FD14							

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 14 (FD14):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD13 has completely shifted in/out.

31.5.20 FDATA15 (Flash_Data_15_bios)—Offset 4Ch

Flash data #15

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Data_15_bios: [SPI_BASE_ADDRESS] + 4Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FD15

Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 15 (FD15):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD14 has completely shifted in/out.

31.5.21 FRACC (Flash_Region_Access_Permissions_bios)—Offset 50h

Flash region access permissions

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_Access_Permissions_bios: [SPI_BASE_ADDRESS] + 50h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000202h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

BMWAG | BMRAG | BRWA | BRRA

Bit Range	Default & Access	Description
31:24	00h RW/L	**BIOS Master Write Access Grant (BMWAG):** Each bit [lb]31:24[rb] corresponds to Master[lb]7:0[rb]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]3[rb] is GBE. Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN or BMWAGLOCKDN bits.

Bit Range	Default & Access	Description
23:16	00h RW/L	**BIOS Master Read Access Grant (BMRAG):** Each bit [lb]23:16[rb] corresponds to Master[lb]7:0[rb]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/ BIOS, Master[lb]2[rb] is SEC, Master[lb]3[rb] is GBE. Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN or BMRAGLOCKDN bit.
15:8	02h RO	**BIOS Region Write Access (BRWA):** Each bit [lb]15:8[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the write access to its own Region 1 by default. Thus, the reset default of this field will be read as 8'h02 regardless of descriptor or non-descriptor mode.
7:0	02h RO	**BIOS Region Read Access (BRRA):** Each bit [lb]7:0[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the read access to its own Region 1 by default. Thus, the reset default of this field will be read as 8'h02 regardless of descriptor or non-descriptor mode.

31.5.22 FREG0 (Flash_Region_0_bios)—Offset 54h

Flash region 0 (flash descriptor)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_0_bios: [SPI_BASE_ADDRESS] + 54h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
RSVD0			RL													RSVD1			RB												

Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base

31.5.23 FREG1 (Flash_Region_1_bios)—Offset 58h

Flash region 1 (BIOS)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_1_bios: [SPI_BASE_ADDRESS] + 58h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
RSVD0			RL													RSVD1			RB												

Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base

31.5.24 FREG2 (Flash_Region_2_bios)—Offset 5Ch

Flash region 2 (SEC)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_2_bios: [SPI_BASE_ADDRESS] + 5Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
RSVD0			RL													RSVD1			RB												

Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit

Bit Range	Default & Access	Description
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base

31.5.25 FREG3 (Flash_Region_3_bios)—Offset 60h

Flash region 3 (GBE)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Region_3_bios: [SPI_BASE_ADDRESS] + 60h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
RSVD0			RL													RSVD1			RB												

Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

31.5.26 FREG4 (Flash_Region_4_bios)—Offset 64h

Flash region 4 (platform data)

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Region_4_bios: [SPI_BASE_ADDRESS] + 64h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
RSVD0			RL													RSVD1			RB												

Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base

31.5.27 PR0 (Protected_Range_0_bios)—Offset 74h

Protected range #0. This register can not be written when the FLOCKDN or PR0LOCKDN bits are set to 1.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Protected_Range_0_bios: [SPI_BASE_ADDRESS] + 74h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WPE	RSVD0		PRL													RPE	RSVD1		PRB												

Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.

Bit Range	Default & Access	Description
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

31.5.28 PR1 (Protected_Range_1_bios)—Offset 78h

Protected range #1. This register can not be written when the FLOCKDN or PR1LOCKDN bits are set to 1.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Protected_Range_1_bios: [SPI_BASE_ADDRESS] + 78h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WPE	RSVD0		PRL													RPE	RSVD1		PRB												

Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

31.5.29 PR2 (Protected_Range_2_bios)—Offset 7Ch

Protected range #2. This register can not be written when the FLOCKDN or PR2LOCKDN bits are set to 1.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Protected_Range_2_bios: [SPI_BASE_ADDRESS] + 7Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WPE	RSVD0		PRL													RPE	RSVD1		PRB												

Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

31.5.30 PR3 (Protected_Range_3_bios)—Offset 80h

Protected range #3. This register can not be written when the FLOCKDN or PR3LOCKDN bits are set to 1.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Protected_Range_3_bios: [SPI_BASE_ADDRESS] + 80h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31	30:29	28:16	15	14:13	12:0
0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0
WPE	RSVD0	PRL	RPE	RSVD1	PRB

Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

31.5.31 PR4 (Protected_Range_4_bios)—Offset 84h

Protected range #4. This register use for H/W range protection. All register values are coming from soft-straps, and the Write Protection Enable is controlled also by the Flash Security Override Pin Strap

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_4_bios: [SPI_BASE_ADDRESS] + 84h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31	30:29	28:16	15	14:13	12:0
0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0
WPE	RSVD0	PRL	RPE	RSVD1	PRB

Bit Range	Default & Access	Description
31	X RO	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. This field value should be an or between soft-strap and the ~Flash Security Override Pin Strap. Such, H/W range protection is active aonly if write protection is enabled by soft-strap and Flash Security Override Pin Strap is deasserted.
30:29	0b RO	**RSVD0:** Reserved
28:16	X RO	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. This field value should be taken from soft-straps.
15	0b RO	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. This field should be always 1'b0
14:13	0b RO	**RSVD1:** Reserved
12:0	X RO	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. This field value should be taken from soft-straps.

31.5.32 SSFCTLSTS (Software_Sequencing_Flash_Control_Status_bios)—Offset 90h

The software sequencing flash control and Status register is a combination of two registers the software sequencing flash status register (bits 7:0) and the software sequencing flash control register (bits 31:8). This register is intended to be used only as a back-up mode to the hardware sequencing control and status registers.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Software_Sequencing_Flash_Control_Status_bios:
[SPI_BASE_ADDRESS] + 90h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: F8000000h

Bits	Default	Field
31:27	1 1 1 1 1	RESERVED
26:24	0 0 0	SCF
23	0	SME
22	0	DC
21:16	0 0 0 0 0 0	DBC
15	0	RSVD0
14:12	0 0 0	COP
11	0	SPOP
10	0	ACS
9	0	SCGO
8	0	RSVD1
7	0	FRS
6	0	DOFRS
5	0	RSVD2
4	0	AEL
3	0	FCERR
2	0	CDS
1	0	RSVD3
0	0	SCIP

Bit Range	Default & Access	Description
31:27	11111b RO	**RESERVED:** reserved, should be with default 1

Bit Range	Default & Access	Description
26:24	000b RW/L	**SPI Cycle Frequency (SCF):** 000 : 20MHz 001 : 33MHz 010 : 66MHz (reserved - not supported on VLV) 011 : 25MHz (reserved - not supported on VLV) 100 : 50MHz (reserved - not supported on VLV-DC) All Others: Reserved This register sets frequency to use for all SPI Software Sequencing cycles (write, erase, fast read, read status, .etc) except for the Read cycle which always run at 20MHz. This register is locked when the SPI Configuration Lock-Down bit is set or when FREQLOCKDN bit is set.
23	0b RW	**SPI SMI# Enable (SME):** When set to 1, the SPI asserts an SMI# request whenever the Cycle Done Status bit is 1.
22	0b RW	**Data Cycle (DC):** When set to 1, there is data that corresponds to this transaction. When 0, no data is dleivered for this cycle, and the DBC and data fields themselves are don t cares.
21:16	000000b RW	**Data Byte Count (DBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer.
15	0b RO	**RSVD0:** Reserved
14:12	000b RW	**Cycle Opcode Pointer (COP):** This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
11	0b RW	**Sequence Prefix Opcode Pointer (SPOP):** This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the SPI controller supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
10	0b RW	**Atomic Cycle Sequence (ACS):** When set to 1 along with the SCGO assertion, the SPI controller will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of:) Atomic Sequence Prefix Command (8-bit opcode only)) Primary Command specified below by software (can include address and data)) Polling the Flash Status Register (opcode 8'h05) until bit 0 becomes 1'b0. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
9	0b RW/SE	**SPI Cycle Go (SCGO):** This bit always returns 1'b0 on reads. However, a write to this register with a 1'b1 in this bit starts the SPI cycle defined by the other bits of this register. The SPI Cycle in Progress (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1'b1. This saves an additional memory write.
8	0b RO	**RSVD1:** Reserved
7	0b RO/U	**Fast Read Supported (FRS):** This bit reflects the value of the Fast Read Support bit in the Flash Descriptor Component Section.
6	0b RO/U	**Dual Output Fast Read Supported (DOFRS):** This bit reflects the value of the Dual Output Fast Read Support bit in the Flash Descriptor Component Section.
5	0b RO	**RSVD2:** Reserved
4	0b RO	**Access Error Log (AEL):** This bit reflects the value of the Hardware Sequencing Status.AEL register.
3	0b RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1'b1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset.

Bit Range	Default & Access	Description
2	0b RW/1C	**Cycle Done Status (CDS):** The SPI controller sets this bit to 1'b1 when the SPI Cycle completes i.e., SCIP bit is 1'b0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	0b RO	**RSVD3:** Reserved
0	0b RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 1'b0.

31.5.33 PREOP (Prefix_Opcode_Configuration_bios)—Offset 94h

Prefix opcode configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when the PREOPLOCKDN bit is set.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Prefix_Opcode_Configuration_bios: [SPI_BASE_ADDRESS] + 94h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PO1								PO0							

Bit Range	Default & Access	Description
15:8	00h RW/L	**Prefix Opcode 1 (PO1):** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	00h RW/L	**Prefix Opcode 0 (PO0):** Prefix Opcode 0: Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

31.5.34 OPTYPE (Opcode_Type_Configuration_bios)—Offset 96h

Opcode type configuration. This register is not writable when the Flash Configuration Lock-Down bit is set or when the OPTYPELOCKDN bit is set. Entries in this register correspond to the entries in the Opcode Menu Configuration register. Note that the definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, Chip Erase and Auto-Address Increment Byte Program).

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

Opcode_Type_Configuration_bios: [SPI_BASE_ADDRESS] + 96h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OT7		OT6		OT5		OT4		OT3		OT2		OT1		OT0	

Bit Range	Default & Access	Description
15:14	00b RW/L	**Opcode Type 7 (OT7):** See the description for bits 1:0
13:12	00b RW/L	**Opcode Type 6 (OT6):** See the description for bits 1:0
11:10	00b RW/L	**Opcode Type 5 (OT5):** See the description for bits 1:0
9:8	00b RW/L	**Opcode Type 4 (OT4):** See the description for bits 1:0
7:6	00b RW/L	**Opcode Type 3 (OT3):** See the description for bits 1:0
5:4	00b RW/L	**Opcode Type 2 (OT2):** See the description for bits 1:0
3:2	00b RW/L	**Opcode Type 1 (OT1):** See the description for bits 1:0
1:0	00b RW/L	**Opcode Type 0 (OT0):** This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The hardware implementation also uses the read vs. write information for modifying the behavior of the SPI interface logic. The encoding of the two bits is: 00 = No Address associated with this Opcode and Read Cycle type 01 = No Address associated with this Opcode and Write Cycle type 10 = Address required, Read cycle type 11 = Address required, Write cycle type

31.5.35 OPMENU0 (Opcode_Menu_Configuration_0_bios)—Offset 98h

Opcode (0-3) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when OPMENULOCKDN bit is set. Four entries are available in this register and four are available in OPMENU1 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Opcode_Menu_Configuration_0_bios: [SPI_BASE_ADDRESS] + 98h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
AO3		AO2		AO1		AO0		

Bit Range	Default & Access	Description
31:24	00h RW/L	**Allowable Opcode 3 (AO3):** See the description for bits 7:0
23:16	00h RW/L	**Allowable Opcode 2 (AO2):** See the description for bits 7:0
15:8	00h RW/L	**Allowable Opcode 1 (AO1):** See the description for bits 7:0
7:0	00h RW/L	**Allowable Opcode 0 (AO0):** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

31.5.36 OPMENU1 (Opcode_Menu_Configuration_1_bios)—Offset 9Ch

Opcode (7-4) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when OPMENULOCKDN bit is set. Four entries are available in this register and four are available in OPMENU0 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Opcode_Menu_Configuration_1_bios: [SPI_BASE_ADDRESS] + 9Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
AO7		AO6		AO5		AO4		

Bit Range	Default & Access	Description
31:24	00h RW/L	**Allowable Opcode 7 (AO7):** See the description for bits 7:0 in OPMENU0
23:16	00h RW/L	**Allowable Opcode 6 (AO6):** See the description for bits 7:0 in OPMENU0
15:8	00h RW/L	**Allowable Opcode 5 (AO5):** See the description for bits 7:0 in OPMENU0
7:0	00h RW/L	**Allowable Opcode 4 (AO4):** See the description for bits 7:0 in OPMENU0

31.5.37 LOCK (Individual_Lock_Register)—Offset A4h

Used to individually lock each one of the registers formaly locked only by FLOCKDN bit. This register doesn't exclude FLOCKDN. It adds an individual option to lock each register in above to FLOCKDN.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Individual_Lock_Register: [SPI_BASE_ADDRESS] + A4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

Bits	31:10	9	8	7	6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0
Field	RESERVED	OPMENULOCKDN	OPTYPELOCKDN	PREOPLOCKDN	FREQLOCKDN	PR3LOCKDN	PR2LOCKDN	PR1LOCKDN	PR0LOCKDN	BMRAGLOCKDN	BMWAGLOCKDN

Bit Range	Default & Access	Description
31:10	000000000 000000000 0000b RO	**RESERVED:** reserved, should be with default 0
9	0b RW/L	**OPMENU Lock-Down (OPMENULOCKDN):** When set to 1, OPMENU0 and OPMENU1 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
8	0b RW/L	**OPTYPE Lock-Down (OPTYPELOCKDN):** When set to 1, OPTYPE register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
7	0b RW/L	**PREOP Lock-Down (PREOPLOCKDN):** When set to 1, PREOP register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
6	0b RW/L	**SCF Lock-Down (FREQLOCKDN):** When set to 1, SCF field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.

Bit Range	Default & Access	Description
5	0b RW/L	**PR3 Lock-Down (PR3LOCKDN):** When set to 1, PR3 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
4	0b RW/L	**PR2 Lock-Down (PR2LOCKDN):** When set to 1, PR2 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
3	0b RW/L	**PR1 Lock-Down (PR1LOCKDN):** When set to 1, PR1 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
2	0b RW/L	**PR0 Lock-Down (PR0LOCKDN):** When set to 1, PR0 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
1	0b RW/L	**BMRAG Lock-Down (BMRAGLOCKDN):** When set to 1, BMRAG field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
0	0b RW/L	**BMWAG Lock-Down (BMWAGLOCKDN):** When set to 1, BMWAG field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.

31.5.38 FDOC (Flash_Descriptor_Observability_Control_bios)—Offset B0h

Flash Descriptor Observability Control. This is a test mode only register that can be used to observe the contents of the Flash Descriptor that is stored internally in the SPI Controller.

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Descriptor_Observability_Control_bios:
[SPI_BASE_ADDRESS] + B0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0	FDSS	FDSI	RSVD1

Bit Range	Default & Access	Description
31:15	0b RO	**RSVD0:** Reserved
14:12	000b RW	**Flash Descriptor Section Select (FDSS):** Selects which section within the loaded Flash Descriptor to observe. 000 : Flash Signature and Descriptor Map 001 : Component 010 : Region 011 : Master 100 : Soft Straps 111 : Reserved
11:2	000h RW	**Flash Descriptor Section Index (FDSI):** Selects the DW offset within the Flash Descriptor Section to observe.
1:0	0b RO	**RSVD1:** Reserved

31.5.39 FDOD (Flash_Descriptor_Observability_Data_bios)—Offset B4h

Flash descriptor observability data

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Descriptor_Observability_Data_bios: [SPI_BASE_ADDRESS] + B4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:0: FDSD

Bit Range	Default & Access	Description
31:0	00000000h RO	**Flash Descriptor Section Data (FDSD):** Contains the DW of data to observe as selected in the Flash Descriptor Observability Control. at default the FDSS==3'b000 hence this register contans the data of Flash Signature and Descriptor Map.

31.5.40 AFC (Additional_Flash_Control_bios)—Offset C0h

Additional flash control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Additional_Flash_Control_bios: [SPI_BASE_ADDRESS] + C0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:8: RSVD0; bits 7:4: RRWSP; bit 3: SPFP; bit 2: FSDCGE; bit 1: FMDCGE; bit 0: FCDCGE

Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:4	0000b RW	**Reserved RW Scratch Pad (RRWSP):** Scratch Pad bits that are R/W to be used during ECO
3	0b RW	**Stop Prefetch on Flush Pending (SPFP):** When set to 1'b1, the in progress of a prefetch will be ended if subsequence access from the same master is detected to be a cache-miss and read cache will be flushed. When set to 1'b0, the prefetch will be allowed to complete prior to flushing.

Bit Range	Default & Access	Description
2	0b RW	**Flash IOSF PRI Dynamic Clock Gating Enable (FSDCGE):** When set to 1'b1, the SPI controller IOSF-PRI interface logic can be dynamically clock gated. This register is only clear on a reset.
1	0b RW	**Flash IOSF SB Dynamic Clock Gating Enable (FMDCGE):** When set to 1'b1, the SPI controller IOSF-SB interface logic can be dynamically clock gated. This register is only clear on a reset.
0	0b RW	**Flash Core Dynamic Clock Gating Enable (FCDCGE):** When set to 1'b1, the SPI controller core logic can be dynamically clock gated. This register is only clear on a reset.

31.5.41 LVSCC (Lower_Vendor_Specific_Component_Capabilities_bios)—Offset C4h

Lower vendor specific component capabilities

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Lower_Vendor_Specific_Component_Capabilities_bios:
[SPI_BASE_ADDRESS] + C4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

Bits	31:24	23	22:16	15:8	7:5	4	3	2	1:0
Default	0 0 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0	0	0	0	0 0
Field	RSVD0	VCL	RSVD1	LEO	RSVD	WEWS	LWSR	LWG	LBES

Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23	0b RW/L	**Vendor Component Lock (VCL):** '0': The lock bit is not set '1': The Vendor Component Lock bit is set. This register locks itself when set. If this register is not set and the Flash is operating in Flash Mode (as opposed to EEPROM mode), then software cannot use hardware sequencing. This requirement is not enforced by hardware, but is a requirement of the the power-on usage model.
22:16	0b RO	**RSVD1:** Reserved
15:8	00h RW/L	**Lower Erase Opcode (LEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.
7:5	000b RW/L	**Reserved RW/L Scratch Pad (RSVD):** Keep RW/L for future Flash Component Specific capabilities. This register is locked by the Vendor Component Lock (VCL) bit.
4	0b RW/L	**Write Enable on Write Status (WEWS):** '0' : No Write Enable command is required to write to the Write Status register '1' : Write Enable command is required to write to the Write Status register Must be set to 1'b1 for Intel's Blanshard Flash Component and for Atmel

Bit Range	Default & Access	Description
3	0b RW/L	**Lower Write Status Required (LWSR):** '0' : No requirement to to write to the Write Status Register prior to a write '1' : A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.
2	0b RW/L	**Lower Write Granularity (LWG):** '0' : 1 Byte '1' : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.
1:0	00b RW/L	**Lower Block/Sector Erase Size (LBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte This register is locked by the Vendor Component Lock (VCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers. This field is used for cycles targeting addresses below the Flash Partition Address.

31.5.42 UVSCC (Upper_Vendor_Specific_Component_Capabilities_bios)—Offset C8h

Upper vendor specific component capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Upper_Vendor_Specific_Component_Capabilities_bios: [SPI_BASE_ADDRESS] + C8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

Bits	31:16	15:8	7:5	4	3	2	1:0
Default	0000 0000 0000 0000	0000 0000	000	0	0	0	00
Field	RSVD0	UEO	RSVD	WEWS	UWSR	UWG	UBES

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RW/L	**Upper Erase Opcode (UEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
7:5	0h RW/L	**Reserved RW/L Scratch Pad (RSVD):** Keep RW/L for future Flash Component Specific capabilities. This register is locked by the Vendor Component Lock (VCL) bit.
4	0b RW/L	**Write Enable on Write Status (WEWS):** '0' : No Write Enable command is required to write to the Write Status register '1' : Write Enable command is required to write to the Write Status register Must be set to 1'b1 for Intel's Blanshard Flash Component and for Atmel

Bit Range	Default & Access	Description
3	0b RW/L	**Upper Write Status Required (UWSR):** '0': No requirement to to write to the Write Status Register prior to a write '1': A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
2	0b RW/L	**Upper Write Granularity (UWG):** '0' : 1 Byte '1' : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
1:0	00b RW/L	**Upper Block/Sector Erase Size (UBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte Note: If supporting more than one Flash component, all flash components must have identical Block/ Sector erase sizes. This register is locked by the Vendor Component Lock (VCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GBE program registers. This field is used for cycles targeting addresses above the Flash Partition Address.

31.5.43 FPB (Flash_Partition_Boundary_bios)—Offset D0h

Flash partition boundary

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Flash_Partition_Boundary_bios: [SPI_BASE_ADDRESS] + D0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD0 (31:13)	FPBA (12:0)

Bit Range	Default & Access	Description
31:13	0b RO	**RSVD0:** Reserved
12:0	0000h RO/U	**Flash Partition Boundary Address (FPBA):** This register reflects the value of the Flash Descriptor Component FPBA field

31.5.44 SCS (SMI_Control_Status_Register_bios)—Offset F8h

SMI Control and Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SMI_Control_Status_Register_bios: [SPI_BASE_ADDRESS] + F8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
RSVD0																								SMIWPEN	SMIWPST	RSVD1					

Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	1b RW	**SMI WPD Enable (SMIWPEN):** When this bit is set to a 1'b1, it enables the SPI controller to generate SMI upon not SMM code is trying to set WPD from a 1'b0 to a 1'b1 while LE is set.
6	0b RW/1C	**SMI WPD Status (SMIWPST):** Set when SMI is generated upon trying to set WPD from a 1'b0 to a 1'b1 by not SMM code (while LE and SMIWPEN are set). Write a 1'b1 to this bit should clear it and clear the SMI (send DEASSERT_SMI)
5:0	0b RO	**RSVD1:** Reserved

31.5.45 BCR (BIOS_Control_Register_bios)—Offset FCh

BIOS control register. This register formerly was in the 0:31:0 config space

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BIOS_Control_Register_bios: [SPI_BASE_ADDRESS] + FCh

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000020h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
RSVD0																										EISS	RSVD1	SRC		LE	WPD

Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	1b RW/L	**Enable InSMM_STS (EISS):** When this bit is set, the BIOS region is writable only to SMM code. Today BIOS Flash is writable if WPD is a '1'. If this bit [lb]5[rb] is set, then WPD must be a 1'b1 and iosfep_xxx_hprot[lb]1[rb] signal be 1'b1 also. If this bit [lb]5[rb] is clear, then BIOS is writable based only on WPD = 1'b1 and the iosfep_xxx_hprot[lb]1[rb] signal is a don't care.
4	0b RO	**RSVD1:** Reserved
3:2	00b RW	**SPI Read Configuration (SRC):** This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3 - Prefetch Enable, Bit 2 - Cache Disable. Settings are summarized below: '00' : No prefetching, but caching enabled. Direct Memory reads load the read buffer cache with 'valid' data, allowing repeated reads to the same range to complete quickly. '01' : No prefetching and no caching. One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. '10' : Prefetching and Caching enabled. This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) '11' : Illegal. Caching must be enabled when Prefetching is enabled. This eliminates the need for a complex prefetch-flushing mechanism. Note that if BIOS direct read caching is disabled while data has already been cached internally, subsequent BIOS direct reads will continue to return data from the cache until the cache is invalidated.
1	0b RW/L	**Lock Enable (LE):** When set, WPD bit could be set from a 1'b0 to a 1'b1 only by SMM code. When cleared, setting the WP bit is allowed in all modes and SMI is not generated. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [lb]5[rb] of this register is locked down.
0	0b RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles. When cleared, only read cycles are permitted to the flash. When LE bit is set this bit could be written from a 1'b0 to a 1'b1 only by SMM code. When not SMM code tries to writes this bit from a 1'b0 to a 1'b1, bit remain in its 1'b0 value. An Async-SMI is generated (Send ASSERT_SMI) if SMIWPEN is set. This ensures that only SMM code can update BIOS.

31.5.46 TCGC (Trunk_Clock_Gating_Control_bios)—Offset 100h

Trunk_Clock_Gating_Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Trunk_Clock_Gating_Control_bios: [SPI_BASE_ADDRESS] + 100h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000510h

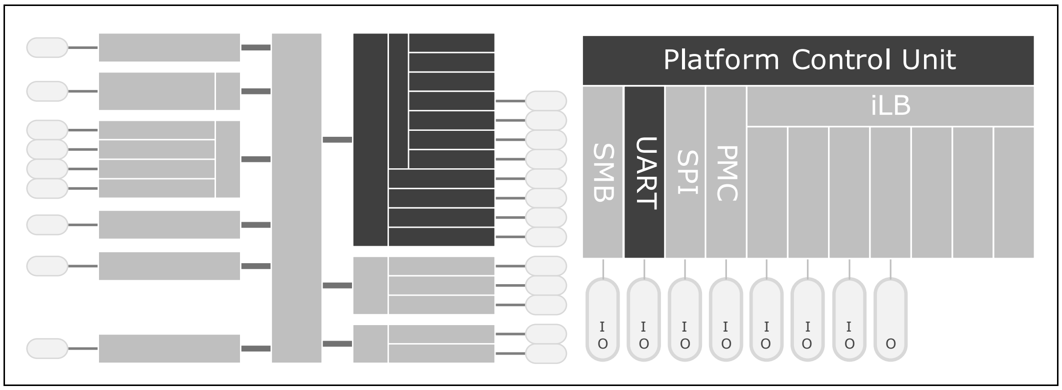
31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0
RSVD0																				RSVD	FCGDIS	SBCGCDEF	SBCGEN	SBCGCNT							

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RO	**Reserved (RSVD):** Reserved.
10	1b RW	**FCGDIS:** Functional clock gating disable, chicken bit for the func_clk_gating FSM
9	0b RW	**SBCGCDEF:** SideBanb Control Gating Clock Defeature .Clock gate defeature bit which allows the ISM to transition to idle, but prevents the final clock masking from occurring. The value of this bit goes to the 'cgctrl_clkgatedef' port of the SideBand EndPoint
8	1b RW	**SBCGEN:** SideBanb Control Gating Clock Enable. Clock gate enable which prevents ISM from leaving ACTIVE. Also prevents the clocks from being gated. The value of this bit goes to the 'cgctrl_clkgaten' port of the SideBand EndPoint
7:0	10h RW	**SBCGCNT:** SideBanb Control Gating Clock Counter. Idle count limit for ISM which is used to determine the block is idle.Recommended value 8'd16 . The value of those bits goes to the 'cgctrl_idlecnt' ports of the SideBand EndPoint

32 PCU – Universal Asynchronous Receiver/Transmitter (UART)

This section describes the Universal Asynchronous Receiver/Transmitter (UART) serial port integrated into the PCU. The UART may be controlled through programmed IO.

Note: Only a minimal ball-count, comprising receive & transmit signals, UART port is implemented. Further, a maximum baud rate of only 115,200 bps is supported. For this reason, it is recommended that the UART port be used for debug purposes only.



32.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 306. UART Signals

Signal Name	Direction Plat. Power	Description
PCU_UART_RXD	I V1P8S	**COM1 Receive:** Serial data input from device pin to the receive port. *This signal is muxed and may be used by other functions.*
PCU_UART_TXD	O V1P8S	**COM1 Transmit:** Serial data output from transmit port to the device pin. *This signal is muxed and may be used by other functions.*

32.2 Features

The serial port consists of a UART which supports a subset of the functions of the 16550 industry standard.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the processor. The processor may read the complete status of the UART at any time during the functional operation. Available status information includes the type and condition of the transfer operations being performed by the UART and any error conditions.

The serial port may operate in either FIFO or non-FIFO mode. In FIFO mode, a 16-byte transmit FIFO holds data from the processor to be transmitted on the serial link and a 16-byte Receive FIFO buffers data from the serial link until read by the processor.

The UART includes a programmable baud rate generator which is capable of generating a baud rate of between 50 bps and 115,200 bps from a fixed baud clock input of 1.8432 MHz. The baud rate is calculated as follows:

Baud Rate Calculation:

$$\text{BaudRate} = \frac{1.8432 \times 10^6}{16 \times \text{Divisor}}$$

The divisor is defined by the Divisor Latch LSB and Divisor Latch MSB registers. Some common values are shown in Table 307.

Table 307. Baud Rate Examples

Desired Baud Rate	Divisor	Divisor Latch LSB Register	Divisor Latch MSB Register
115,200	1	1h	0h
57,600	2	2h	0h
38,400	3	3h	0h
19,200	6	6h	0h
9,600	12	Ch	0h
4,800	24	18h	0h
2,400	48	30h	0h
1,200	96	60h	0h
300	384	80h	1h
50	2,304	0h	9h

The UART has interrupt support and those interrupts may be programmed to the user's requirements, minimizing the computing required to handle the communications link. Each UART may operate in a polled or an interrupt driven environment as configured by software.

32.2.1 FIFO Operation

32.2.1.1 FIFO Interrupt Mode Operation

Receiver Interrupt

When the Receive FIFO and receiver interrupts are enabled (FIFO Control Register, bit 0 = 1b and Interrupt Enable Register (IIR), bit 0 = 1b), receiver interrupts occur as follows:

- The receive data available interrupt is invoked when the FIFO has reached its programmed trigger level. The interrupt is cleared when the FIFO drops below the programmed trigger level.
- The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, the bits are cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR = C6h), as before, has the highest priority. The receiver data available interrupt (IIR = C4h) is lower. The line status interrupt occurs only when the character at the top of the FIFO has errors.
- The COM1_LSR.DR bit is set to 1b as soon as a character is transferred from the shift register to the Receive FIFO. This bit is reset to 0b when the FIFO is empty.

Character Time Out Interrupt

When the receiver FIFO and receiver time out interrupt are enabled, a character time out interrupt occurs when all of the following conditions exist:

- At least one character is in the FIFO.
- The last received character was longer than four continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- The most recent processor read of the FIFO was longer than four continuous character times ago.
- The receiver FIFO trigger level is greater than one.

The maximum time between a received character and a timeout interrupt is 160 ms at 300 baud with a 12-bit receive character (i.e., 1 start, 8 data, 1 parity, and 2 stop bits).

When a time out interrupt occurs, it is cleared and the timer is reset when the processor reads one character from the receiver FIFO. If a time out interrupt has not occurred, the time out timer is reset after a new character is received or after the processor reads the receiver FIFO.

Transmit Interrupt

When the transmitter FIFO and transmitter interrupt are enabled (FIFO Control Register, bit 0 = 1b and Interrupt Enable Register, bit 0 = 1b), transmit interrupts occur as follows:

The Transmit Data Request interrupt occurs when the transmit FIFO is half empty or more than half empty. The interrupt is cleared as soon as the Transmit Holding Register is written (1 to 16 characters may be written to the transmit FIFO while servicing the interrupt) or the Interrupt Identification Register is read.

32.2.1.2 FIFO Polled Mode Operation

With the FIFOs enabled (FIFO Control register, bit 0 = 1b), setting Interrupt Enable register (IER), bits 3:0 = 000b puts the serial port in the FIFO polled mode of operation. Since the receiver and the transmitter are controlled separately, either one or both may be in the polled mode of operation. In this mode, software checks receiver and transmitter status through the Line Status Register (LSR). As stated in the register description:

- LSR[0] is set as long as there is one byte in the receiver FIFO.
- LSR[1] through LSR[4] specify which error(s) has occurred for the character at the top of the FIFO. Character error status is handled the same way as interrupt mode. The Interrupt Identification Register is not affected since IER[2] = 0b.
- LSR[5] indicates when the transmitter FIFO needs data.
- LSR[6] indicates that both the transmitter FIFO and shift register are empty.
- LSR[7] indicates whether there are any errors in the receiver FIFO.

32.3 Use

32.3.1 Base I/O Address

32.3.1.1 COM1

The base I/O address for the COM1 UART is fixed to 3F8h.

32.3.2 Legacy Interrupt

32.3.2.1 COM1

The legacy interrupt assigned to the COM1 UART is fixed to IRQ4.

32.4 UART Enable/Disable

The COM1 UART may be enabled or disabled using the UART_CONT.COM1EN register bit. By default, the UART is disabled.

Note: It is recommended that the UART be disabled during normal platform operation since it is a PIO device and, as such, can prevent residency in lower power states by the processor.

32.5 IO Mapped Registers

There are 12 registers associated with the UART. These registers share eight address locations in the IO address space. Table 308 shows the registers and their addresses as offsets of a base address. Note that the state of the COM1_LCR.DLAB register bit, which is the most significant bit (MSB) of the Serial Line Control register, affects the selection of certain of the UART registers. The COM1_LCR.DLAB register bit must be set high by the system software to access the Baud Rate Generator Divisor Latches.

Table 308. Register Access List

Register Address (Offset to Base IO Address)	COM1_LCR.DLAB Value	Register Access Type	Register Accessed
0h	0b	RO	Receiver Buffer[1]
0h	0b	WO	Transmitter Holding[1]
0h	1b	RW	Divisor Latch LSB (Lowest Significant Bit)[1]
1h	0b	RW	Interrupt Enable[2]
1h	1b	RW	Divisor Latch MSB (Most Significant Bit)[2]
2h	xb	RO	Interrupt Identification[3]
2h	xb	WO	FIFO Control[3]
3h	xb	RW	Line Control
4h	xb	RW	Modem Control[4]
5h	xb	RO	Line Status
6h	xb	RO	Modem Status[4]
7h	xb	RW	Scratchpad

Notes:
1. These registers are consolidated in the Receiver Buffer / Transmitter Holding Register (COM1_RX_TX_BUFFER)
2. These registers are consolidated in the Interrupt Enable Register (COM1_IER)
3. These registers are consolidated in the Interrupt Identification / FIFO Control Register (COM1_IIR)
4. These registers are implemented but unused since the UART signals related to modem interaction are not implemented.

§

32.6 PCU iLB UART IO Registers

Table 309. Summary of PCU iLB UART I/O Registers—

Offset	Size	Register ID—Description	Default Value
3F8h	1	"Receiver Buffer / Transmitter Holding Register (COM1_Rx_Tx_Buffer)—Offset 3F8h" on page 4432	00h
3F9h	1	"Interrupt Enable Register (COM1_IER)—Offset 3F9h" on page 4433	00h
3FAh	1	"Interrupt Identification / FIFO Control Register (COM1_IIR)—Offset 3FAh" on page 4434	01h
3FBh	1	"Line Control Register (COM1_LCR)—Offset 3FBh" on page 4435	00h
3FCh	1	"Modem Control Register (COM1_MCR)—Offset 3FCh" on page 4436	00h
3FDh	1	"Line Status Register (COM1_LSR)—Offset 3FDh" on page 4437	60h
3FEh	1	"Modem Status Register (COM1_MSR)—Offset 3FEh" on page 4438	00h
3FFh	1	"Scratchpad Register (COM1_SCR)—Offset 3FFh" on page 4440	00h

32.6.1 Receiver Buffer / Transmitter Holding Register (COM1_Rx_Tx_Buffer)—Offset 3F8h

This register is a combination of three registers: the receiver buffer register (RBR) that is a read-only register when DLAB=0, the transmitter holding register (THR) that is a write-only register when DLAB=0 and the divisor latch LSB (DLL) register when DLAB=1.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_Rx_Tx_Buffer: 3F8h

Default: 00h

7 4 0

0 0 0 0 0 0 0 0

RBR_THR_DLL

Bit Range	Default & Access	Description
7:0	00h RW	**Receiver buffer / transmitter holding (RBR_THR_DLL): When reading from this register and DLAB=1'b0**, it contains the byte received if no FIFO is used, or the oldest unread byte with FIFO's. If FIFO buffering is used, each new read action of the register will return the next byte, until no more bytes are present. Bit 0 in the LSR line status register can be used to check if all received bytes have been read. This bit wil change to zero if no more bytes are present. **When writing to this register and DLAB=1'b0**, it is used to buffer outgoing characters. If no FIFO buffering is used, only one character can be stored. Otherwise the amount of characters depends on the type of UART. Bit 5 in the LSR, line status register can be used to check if new information must be written to this register. The value 1'b1 indicates that the register is empty. If FIFO buffering is used, more than one character can be written to the transmitter holding register when the bit signals an empty state. There is no indication of the amount of bytes currently present in the transmitter FIFO. This register is not used to transfer the data directly. The byte is first transferred to a shift register where the information is broken in single bits which are sent one by one. **If DLAB=1'b1**, this register is used as DLL (Divisor Latch LSB). For generating its timing information, each UART uses an oscillator generating a frequency of about 1.8432 MHz. This frequency is divided by 16 to generate the time base for communucation. Because of this division, the maximum allowed communication speed is 115200 bps. Modern UARTS like the 16550 are capable of handling higher input frequencies up to 24 MHz which makes it possible to communicate with a maximum speed of 1.5 Mbps. On PC's higher frequencies than the 1.8432 MHz are rarely seen because this would be software incompatible with the original XT configuration. This 115200 bps communication speed is not suitable for all applications. To change the communication speed, the frequency can be further decreased by dividing it by a programmable value. For very slow communications, this value can go beyond 255. Therefore, the divisor is stored in two seperate bytes, the divisor latch registers DLL and DLM which contain the least, and most significant byte. For error free communication, it is necessary that both the transmitting and receiving UART use the same time base. Default values have been defined which are commonly used. The table shows the most common values with the appropriate settings of the divisor latch bytes. Note that these values only hold for a PC compatible system where a clock frequency of 1.8432 MHz is used. Speed(bps) Divisor DLL DLM 50 2,304 0x00 0x09 300 384 0x80 0x01 1,200 96 0x60 0x00 2,400 48 0x30 0x00 4,800 24 0x18 0x00 9,600 12 0x0C 0x00 19,200 6 0x06 0x00 38,400 3 0x03 0x00 57,600 2 0x02 0x00 115,200 1 0x01 0x00

32.6.2 Interrupt Enable Register (COM1_IER)—Offset 3F9h

This register is a combination of two registers: the interrupt enable register (IER) when DLAB=0 and the divisor latch MSB (DLM) register when DLAB=1.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_IER: 3F9h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0

IER_DLM

Bit Range	Default & Access	Description
7:0	00h RW	**Interrupt Enable (IER_DLM): If DLAB=1'b0**, This field is used as interrupt enable register. The smartest way to perform serial communications on a PC is using interrupt driven routines. In that configuration, it is not necessary to poll the registers of the UART periodically for state changes. The UART will signal each change by generating a processor interrupt. A software routine must be present to handle the interrupt and to check what state change was responsible for it. Interrupts are not generated, unless the UART is told to do so. This is done by setting bits in the IER, interrupt enable register. A bit value 1 indicates, that an interrupt may take place. Bit Description 0 ERBFI - Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1 ETBEI - Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 2 ELSI - Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 3 EDSSI - Enable Modem Status Interrupt. This is used to enable/ disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 4 Reserved and read as zero 5 Reserved and read as zero 6 Reserved and read as zero 7 PTIME - Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. **If DLAB=1'b1**, this register is used as DLM (Divisor Latch MSB). See DLL field description in the Rx_Tx_Buffer register.

32.6.3 Interrupt Identification / FIFO Control Register (COM1_IIR)—Offset 3FAh

This register is a combination of two registers: the interrupt identification register (IIR) that is a read-only register and the FIFO control register (FCR) that is a write-only register. If FIFOs are not implemented, the FIFO control register does not exist and writing to this register address has no effect.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_IIR: 3FAh

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
FERT		TET		IIR			

Bit Range	Default & Access	Description
7:6	00b RO	**FIFOs Enabled / RCVR Trigger (FERT): Read** from this field is used to indicate whether the FIFOs are enabled or disabled. '00' - disabled '11' - enabled **Write** to this field is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. The following trigger levels are supported: '00' - 1 character in the FIFO '01' - FIFO 1/4 full '10' - FIFO 1/2 full '11' - FIFO 2 less than full
5:4	00b RO	**TX Empty Trigger (TET): Read** from this field is reserved and should return zero **Write** to this field is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: '00' - FIFO empty '01' - 2 characters in the FIFO '10' - FIFO 1/4 full '11' - FIFO 1/2 full

Bit Range	Default & Access	Description
3:0	0001b RO	**Interrupt ID (IIR): Read** from this field indicates the highest priority pending interrupt which can be one of the following types: '0000' - modem status '0001' - no interrupt pending '0010' - THR empty '0100' - received data available '0110' - receiver line status '0111' - busy detect '1100' - character timeout **Write** to this field is split to four bits: Bit Description 3 DMA Mode, determines the DMA signalling mode used: '0'- mode 0, '1' - mode 1 2 XMIT FIFO Reset, resets the control portion of the transmit FIFO and treats the FIFO as empty. 1 RCVR FIFO Reset, resets the control portion of the receive FIFO and treats the FIFO as empty. 0 FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

32.6.4 Line Control Register (COM1_LCR)—Offset 3FBh

The LCR, line control register is used at initialisation to set the communication parameters. Parity and number of data bits can be changed for example. The register also controls the accessibility of the DLL and DLM registers. These registers are mapped to the same I/O port as the RBR, THR and IER registers. Because they are only accessed at initialisation when no communication occurs this register swapping has no influence on performance.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_LCR: 3FBh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
DLAB	BC	SP	EPS	PEN	STOP	DLS	

Bit Range	Default & Access	Description
7	0b RW	**Divisor Latch Access Bit (DLAB):** This field is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. '0' - RBR, THR and IER accessible '1' - DLL and DLM accessible See Rx_Tx_Buffer and IER registers description for more details.
6	0b RW	**Break Control (BC):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0b RO	**Stick Parity (SP):** Reserved and read as zero
4	0b RW	**Even Parity Select (EPS):** This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	0b RW	**Parity Enable (PEN):** This is used to enable and disable parity generation and detection in transmitted and received serial character respectively. '0' - parity disabled '1' - parity enabled

Bit Range	Default & Access	Description
2	0b RW	**Number ofStop bits (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. '0' - 1 stop bit '1' - 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	00b RW	**Data Length Select (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: '00' - 5 bits '01' - 6 bits '10' - 7 bits '11' - 8 bits

32.6.5 Modem Control Register (COM1_MCR)—Offset 3FCh

The MCR, modem control register is used to perform handshaking actions with the attached device. In the original UART series including the 16550, setting and resetting of the control signals must be done by software. The new 16750 is capable of handling flow control automatically, thereby reducing the load on the processor.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_MCR: 3FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0	SIRE	AFCE	LB	OUT2	OUT1	RTS	DTR

Bit Range	Default & Access	Description
7	0b RO	**RSVD0:** Reserved
6	0b RW	**SIR Mode Enable (SIRE):** Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in 'IrDA 1.0 SIR Protocol' on Synopsys UART specification. '0' - IrDA SIR Mode disabled '1' - IrDA SIR Mode enabled
5	0b RW	**Auto Flow Control Enable (AFCE):** Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in 'Auto Flow Control' on Synopsys UART specification. '0' - Auto Flow Control Mode disabled '1' - Auto Flow Control Mode enabled
4	0b RW	**LoopBack (LB):** This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0b RW	**Auxiliary output 2 (OUT2):** This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: '0' - out2_n de-asserted (logic 1) '1' - out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.

Bit Range	Default & Access	Description
2	0b RW	**Auxiliary output 1 (OUT1):** This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: '0' - out1_n de-asserted (logic 1) '1' - out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0b RW	**Request to Send (RTS):** This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Note that PCU-UART does not implement the Request to Send (rts_n) output.
0	0b RW	**Data Terminal Ready (DTR):** This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: '0' - dtr_n de-asserted (logic 1) '1' - dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Note that PCU-UART does not implement the Data Terminal Ready (dtr_n) output.

32.6.6 Line Status Register (COM1_LSR)—Offset 3FDh

The LSR, line status register shows the current state of communication. Errors are reflected in this register. The state of the receive and transmit buffers is also available.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_LSR: 3FDh

Default: 60h

7			4				0
0	1	1	0	0	0	0	0
RFE	TEMT	THRE	BI	FE	PE	OE	DR

Bit Range	Default & Access	Description
7	0b RO	**Receiver FIFO Error (RFE):** This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. '0' - no error in RX FIFO '1' - error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1b RO	**Transmitter Empty (TEMT):** If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.

Bit Range	Default & Access	Description
5	1b RO	**Transmit Holding Register Empty (THRE):** If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0b RO	**Break Interrupt (BI):** This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	0b RO	**Framing Error (FE):** This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). '0' - no framing error '1' - framing error Reading the LSR clears the FE bit.
2	0b RO	**Parity Error (PE):** This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). '0' - no parity error '1' - parity error Reading the LSR clears the PE bit.
1	0b RO	**Overrun Error (OE):** This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. '0' - no overrun error '1' - overrun error Reading the LSR clears the OE bit.
0	0b RO	**Data Ready (DR):** This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. '0' - no data ready '1' - data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

32.6.7 Modem Status Register (COM1_MSR)—Offset 3FEh

The MSR, modem status register contains information about the four incomming modem control lines on the device. The information is split in two nibbles. The four most siginificant bits contain information about the current state of the inputs where the least significant bits are used to indicate state changes. The four LSB's are reset, each time the register is read. Whenever bits 0, 1, 2 or 3 are set to logic one, to indicate a change on the modem control inputs, a modem status interrupt is generated if enabled through the IER, regardless of when the change occurred. Since the delta bits (bits 0, 1, 3) can get set after a reset if their respective modem signals are active (see individual bits for details), a read of the MSR after reset can be performed to prevent unwanted interrupts.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_MSR: 3FEh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Bit Range	Default & Access	Description
7	0b RO	**Data Carrier Detect (DCD):** This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. '0' - dcd_n input is de-asserted (logic 1) '1' - dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Note that PCU-UART does not implement the Data Carrier Detect (dcd_n) input.
6	0b RO	**Ring Indicator (RI):** This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. '0' - ri_n input is de-asserted (logic 1) '1' - ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Note that PCU-UART does not implement the Ring Indicator (ri_n) input.
5	0b RO	**Data Set Ready (DSR):** This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. '0' - dsr_n input is de-asserted (logic 1) '1' - dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Note that PCU-UART does not implement the Data Set Ready (dsr_n) input.
4	0b RO	**Clear to Send (CTS):** This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. '0' - cts_n input is de-asserted (logic 1) '1' - cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Note that PCU-UART does not implement the Clear to Send (cts_n) input.
3	0b RO	**Delta Data Carrier Detect (DDCD):** This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. '0' - no change on dcd_n since last read of MSR '1' - change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Note that PCU-UART does not implement the Data Carrier Detect (dcd_n) input.
2	0b RO	**Trailing Edge of Ring Indicator (TERI):** This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. '0' - no change on ri_n since last read of MSR '1' - change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Note that PCU-UART does not implement the Ring Indicator (ri_n) input.

Bit Range	Default & Access	Description
1	0b RO	**Delta Data Set Ready (DDSR):** This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. '0' - no change on dsr_n since last read of MSR '1' - change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Note that PCU-UART does not implement the Data Set Ready (dsr_n) input.
0	0b RO	**Delta Clear to Send (DCTS):** This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. '0' - no change on cts_n since last read of MSR '1' - change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Note that PCU-UART does not implement the Clear to Send (cts_n) input.

32.6.8 Scratchpad Register (COM1_SCR)—Offset 3FFh

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_SCR: 3FFh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
SC							

Bit Range	Default & Access	Description
7:0	00h RW	**Scratchpad (SC):** This register is for programmers to use as a temporary storage space.

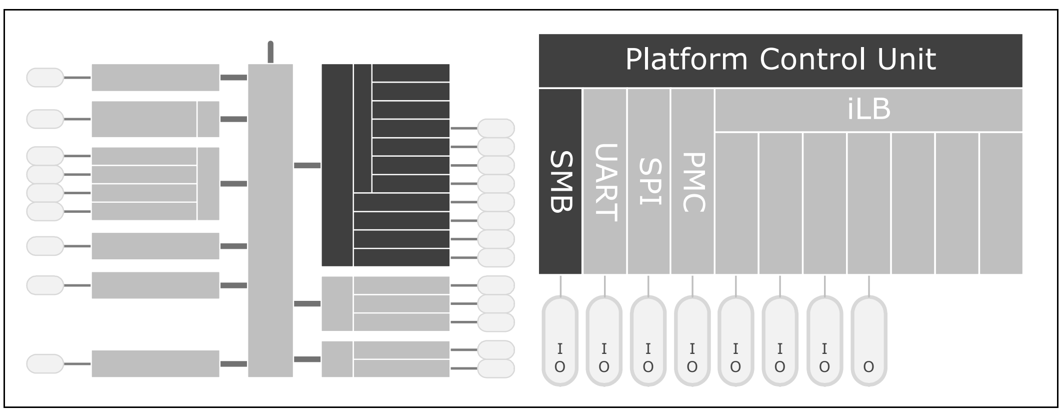
33 PCU – System Management Bus (SMBus)

The SoC provides a System Management Bus (SMBus) 2.0 host controller. The host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). The SoC is also capable of operating in a mode in which it can communicate with I^{2}C compatible devices.

The SoC can perform SMBus messages with packet error checking (PEC) enabled or disabled. The actual PEC calculation and checking can be performed in either hardware or software.

The SMBus Address Resolution Protocol (ARP) is supported by using the existing host controller commands through software, except for the Host Notify command (which is actually a received message).

The programming model of the host controller is combined into two portions: a PCI configuration portion, and a system I/O mapped portion. All static configuration, such as the I/O base address, is done using the PCI configuration space. Real-time programming of the Host interface is done in system I/O space.



33.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 310. SMBus Signal Names

Signal Name	Direction Plat. Power	Description
PCU_SMB_ALERT#	I/OD V1P8S	**SMBus Alert:** This signal is used to generate internal SMI#. *This signal is muxed and may be used by other functions.*
PCU_SMB_CLK	I/OD V1P8S	**SMBus Clock:** External pull-up resistor is required. *This signal is muxed and may be used by other functions.*
PCU_SMB_DATA	I/OD V1P8S	**SMBus Data:** External pull-up resistor is required. *This signal is muxed and may be used by other functions.*

33.2 Features

33.2.1 Host Controller

The SMBus host controller is used to send commands to other SMBus slave devices. Software sets up the host controller with an address, command, and, for writes, data and optional PEC; and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it generates an SMI# or interrupt, if enabled.

The host controller supports 8 command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification, Version 2.0*): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write and Block Write–Block Read Process Call. Additionally, it supports 1 command protocol for I^2C devices: I^2C Read.

The SMBus host controller requires that the various data and command fields be setup for the type of command to be sent. When software sets the START bit, the SMBus Host controller performs the requested transaction, and interrupts the processor (or generates an SMI#) when the transaction is completed. Once a START command has been issued, the values of the "active registers" (Host Control (SMB_Mem_HCTL), Host Command (SMB_Mem_HCMD), Transmit Slave Address (SMB_Mem_TSA), Data 0 (SMB_Mem_HD0), Data 1 (SMB_Mem_HD1)) should not be changed or read until the interrupt status message (SMB_Mem_HSTS.INTR) has been set (indicating the completion of the command). Any register values needed for computation purposes should be saved prior to issuing of a new command, as the SMBus host controller updates all registers while completing the new command.

33.2.1.1 Command Protocols

In all of the following commands, the Host Status (SMB_Mem_HSTS) register is used to determine the progress of the command. While the command is in operation, the SMB_Mem_HSTS.HBSY bit is set. If the command completes successfully, the SMB_Mem_HSTS.INTR bit will be set. If the device does not respond with an acknowledge, and the transaction times out, the SMB_Mem_HSTS.DEVERR bit is set. If software sets the SMB_Mem_HCTL.KILL bit while the command is running, the transaction will stop and the SMB_Mem_HSTS.FAILED bit will be set.

Quick Command

When programmed for a Quick Command, the Transmit Slave Address (SMB_Mem_TSA) register is sent. The PEC byte is never appended to the Quick Protocol. Software should force the SMB_Config_HCTL.PECEN bit to 0b when performing the Quick Command. Software must force the SMB_Config_HCFG.I2C_EN bit to 0b when running this command. See section 5.5.1 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Send Byte / Receive Byte

For the Send Byte command, the Transmit Slave Address (SMB_Mem_TSA) and Host Command (SMB_Mem_HCMD) registers are sent. For the Receive Byte command, the Transmit Slave Address (SMB_Mem_TSA) register is sent. The data received is stored in the Data 0 (SMB_Mem_HD0) register. Software must force the SMB_Config_HCFG.I2C_EN bit to 0b when running this command.

The Receive Byte is similar to a Send Byte, the only difference is the direction of data transfer. See sections 5.5.2 and 5.5.3 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Write Byte/Word

The first byte of a Write Byte/Word access is the command code. The next 1 or 2 bytes are the data to be written. When programmed for a Write Byte/Word command, the Transmit Slave Address (SMB_Mem_TSA), Host Command (SMB_Mem_HCMD), and Data 0 (SMB_Mem_HD0) registers are sent. In addition, the Data 1 (SMB_Mem_HD1) register is sent on a Write Word command. Software must force the SMB_Config_HCFG.I2C_EN bit to 0 when running this command. See section 5.5.4 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Read Byte/Word

Reading data is slightly more complicated than writing data. First the SoC must write a command to the slave device. Then it must follow that command with a repeated start condition to denote a read from that device's address. The slave then returns 1 or 2 bytes of data. Software must force the SMB_Config_HCFG.I2C_EN bit to 0b when running this command.

When programmed for the read byte/word command, the Transmit Slave Address (SMB_Mem_TSA) and Host Command (SMB_Mem_HCMD) registers are sent. Data is received into the Data 0 (SMB_Mem_HD0) on the read byte, and the Data 0

(SMB_Mem_HD0) and Data 1 (SMB_Mem_HD1) registers on the read word. See section 5.5.5 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Process Call

The process call is so named because a command sends data and waits for the slave to return a value dependent on that data. The protocol is simply a Write Word followed by a Read Word, but without a second command or stop condition.

When programmed for the Process Call command, the SoC transmits the Transmit Slave Address (SMB_Mem_TSA), Host Command (SMB_Mem_HCMD), Data 0 (SMB_Mem_HD0) and Data 1 (SMB_Mem_HD1) registers. Data received from the device is stored in the Data 0 (SMB_Mem_HD0) and Data 1 (SMB_Mem_HD1) registers. The Process Call command with SMB_Config_HCFG.I2C_EN set and the SMB_Config_HCTL.PECEN bit set produces undefined results. Software must force either SMB_Config_HCFG.I2C_EN or SMB_Config_HCTL.PECEN & SMB_Mem_AUXC.AAC to 0b when running this command. See section 5.5.6 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Note: For process call command, the value written into SMB_Mem_TSA.RW needs to be 0b.

Note: If the SMB_Config_HCFG.I2C_EN bit is set, the protocol sequence changes slightly: the Command Code (Bits 18:11 in the bit sequence) are not sent - as a result, the slave will not acknowledge (Bit 19 in the sequence).

Block Read/Write

The SoC contains a 32-byte buffer for read and write data which can be enabled by setting SMB_Mem_AUXC.E32B, as opposed to a single byte of buffering. This 32-byte buffer is filled with write data before transmission, and filled with read data on reception. In the SoC, the interrupt is generated only after a transmission or reception of 32 bytes, or when the entire byte count has been transmitted/received.

Note: When operating in I^2C mode (SMB_Config_HCFG.I2C_EN bit is set), the SoC will never use the 32-byte buffer for any block commands.

The byte count field is transmitted but ignored by the SoC as software will end the transfer after all bytes it cares about have been sent or received.

For a Block Write, software must either force the SMB_Config_HCFG.I2C_EN bit or both the SMB_Config_HCTL.PECEN and SMB_Mem_AUXC.AAC bits to 0b when running this command.

The block write begins with a slave address and a write condition. After the command code the SoC issues a byte count describing how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

When programmed for a block write command, the Transmit Slave Address (SMB_Mem_TSA), Host Command (SMB_Mem_HCMD) and Data 0 (SMB_Mem_HD0) registers are sent. Data is then sent from the Host Block Data (SMB_Mem_HBD) register; the total data sent being the value stored in the Data 0 (SMB_Mem_HD0) register. On block read commands, the first byte received is stored in the Data 0 (SMB_Mem_HD0) register, and the remaining bytes are stored in the Host Block Data (SMB_Mem_HBD) register. See section 5.5.7 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Note: For Block Write, if the SMB_Config_HCFG.I2C_EN bit is set, the format of the command changes slightly. The SoC will still send the number of bytes (on writes) or receive the number of bytes (on reads) indicated in the Data 0 (SMB_Mem_HD0) register. However, it will not send the contents of the Data 0 (SMB_Mem_HD0) register as part of the message. Also, the Block Write protocol sequence changes slightly: the Byte Count (bits 27:20 in the bit sequence) are not sent - as a result, the slave will not acknowledge (bit 28 in the sequence).

Block Write–Block Read Process Call

The block write-block read process call is a two-part message. The call begins with a slave address and a write condition. After the command code the host issues a write byte count (M) that describes how many more bytes will be written in the first part of the message. If a master has 6 bytes to send, the byte count field will have the value 6 (0000 0110b), followed by the 6 bytes of data. The write byte count (M) cannot be 0.

The second part of the message is a block of read data beginning with a repeated start condition followed by the slave address and a Read bit. The next byte is the read byte count (N), which may differ from the write byte count (M). The read byte count (N) cannot be 0.

The combined data payload must not exceed 32 bytes. The byte length restrictions of this process call are summarized as follows:

- $M \geq 1$ byte
- $N \geq 1$ byte
- $M + N \leq 32$ bytes

The read byte count does not include the PEC byte. The PEC is computed on the total message beginning with the first slave address and using the normal PEC computational rules. It is highly recommended that a PEC byte be used with the Block Write-Block Read Process Call. Software must do a read to the Host Command (SMB_Mem_HCMD) register to reset the 32 byte buffer pointer prior to reading the Host Block Data (SMB_Mem_HBD) register.

Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

Note: The SMB_Mem_AUXC.E32B bit in the Auxiliary Control register must be set when using this protocol.

See section 5.5.8 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

I²C Read

This command allows the SoC to perform block reads to certain I²C devices, such as serial EEPROMs. The SMBus Block Read supports the 7-bit addressing mode only.

However, this does not allow access to devices using the I²C "Combined Format" that has data bytes after the address. Typically these data bytes correspond to an offset (address) within the serial memory chips.

Note: This command is supported independent of the setting of the SMB_Config_HCFG.I2C_EN bit. The I²C Read command with the SMB_Config_HCTL.PECEN bit set produces undefined results. Software must force both the SMB_Config_HCTL.PECEN and SMB_Mem_AUXC.AAC bit to 0b when running this command.

For I²C Read command, the value written into SMB_Mem_TSA.RW needs to be 1b. The format that is used for the command is shown in below table.

Table 311. I²C Block Read

Bit	Description
1	Start
8:2	Slave Address – 7 bits
9	Write
10	Acknowledge from slave
18:11	Send Data 1 (SMB_Mem_HD1) register
19	Acknowledge from slave
20	Repeated Start
27:21	Slave Address – 7 bits
28	Read
29	Acknowledge from slave
37:30	Data byte 1 from slave – 8 bits
38	Acknowledge
46:39	Data byte 2 from slave – 8 bits
47	Acknowledge
–	Data bytes from slave / Acknowledge
–	Data byte N from slave – 8 bits
–	NOT Acknowledge
–	Stop

The SoC will continue reading data from the peripheral until the NAK is received.

33.2.2 Bus Arbitration

Several masters may attempt to get on the bus at the same time by driving the PCU_SMB_DATA line low to signal a start condition. The SoC continuously monitors the PCU_SMB_DATA line. When the SoC is attempting to drive the bus to a 1 by letting go of the PCU_SMB_DATA line, and it samples PCU_SMB_DATA low, then some other master is driving the bus and the SoC will stop transferring data.

If the SoC sees that it has lost arbitration, the condition is called a collision. The SoC will set SMB_Mem_HSTS.BERR, and if enabled, generate an interrupt or SMI#. The processor is responsible for restarting the transaction.

The SoC, as a SMBus master, drives the clock. When the SoC is sending address or command or data bytes on writes, it drives data relative to the clock it is also driving. It will not start toggling the clock until the start or stop condition meets proper setup and hold time. The SoC will also ensure minimum time between SMBus transactions as a master.

33.2.3 Bus Timing

33.2.3.1 Clock Stretching

Some devices may not be able to handle their clock toggling at the rate that the SoC as an SMBus master would like. They have the capability of stretching the low time of the clock. When the SoC attempts to release the clock (allowing the clock to go high), the clock will remain low for an extended period of time.

The SoC monitors the SMBus clock line after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. Similarly, the low period of the clock can be stretched by an SMBus master if it is not ready to send or receive data.

33.2.3.2 Bus Time Out (SoC as SMBus Master)

If there is an error in the transaction, such that an SMBus device does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction will time out. The SoC will discard the cycle and set the SMB_Mem_HSTS.DEVERR bit. The time out minimum is 25 ms (800 RTC clocks). The time-out counter inside the SoC will start after the last bit of data is transferred by the SoC and it is waiting for a response.

The 25-ms time-out counter will not count under the following conditions:

1. The SMB_Mem_HSTS.BYTE_DONE_STS bit is set

2. The TCO_STS.SECOND_TO_STS bit is not set (this indicates that the system has not locked up).

33.2.4 Interrupts / SMI#

The SoC SMBus controller uses INTB as its virtual interrupt wire. However, the system can alternatively be set up to generate SMI# instead of an interrupt, by setting the SMB_Config_HCFG.SMI_EN bit.

Below tables specify how the various enable bits in the SMBus function control the generation of the interrupt and Host SMI internal signals. The rows in the tables are additive, which means that if more than one row is true for a particular scenario then the Results for all of the activated rows will occur.

Table 312. Enable for PCU_SMB_ALERT#

Event	SMB_Mem_ HCTL.INTREN	SMB_Config_ HCFG.SMI_EN	SMB_Mem_ SCMD.SMBAL TDIS	Result
PCU_SMB_ALERT# asserted low (always reported in SMB_Mem_ HSTS.SMBALERT)	X	1	0	Slave SMI# generated (SMBUS_SMI_S TS)
	1	0	0	Interrupt generated

Table 313. Enables for SMBus Host Events

Event	SMB_Mem_ HCTL.INTREN	SMB_Config_ HCFG.SMI_EN	Event
Any combination of SMB_Mem_HSTS. FAILED, SMB_Mem_HSTS. BERR, SMB_Mem_HSTS. DEVERR, SMB_Mem_HSTS. INTR asserted	0	X	None
	1	0	Interrupt generated
	1	1	Host SMI# generated

Table 314. Enables for the Host Notify Command

SMB_Mem_ SCMD.HNINTREN	SMB_Config_ HCFG.SMI_EN	SMB_Mem_ SCMD.HNWAKEEN	Result
0	X	0	None
1	0	X	Interrupt generated
1	1	X	Slave SMI# generated (SMBUS_SMI_STS)

33.2.5 PCU_SMB_ALERT#

PCU_SMB_ALERT# is multiplexed with GPIO_S0_SC[53]. When enabled and the signal is asserted, the SoC can generate an interrupt or an SMI#.

Note: Using this signal as a wake event from is not supported.

33.2.6 SMBus CRC Generation and Checking

If the SMB_Mem_AUXC.AAC is set, the SoC automatically calculates and drives CRC at the end of the transmitted packet for write cycles, and will check the CRC for read cycles. It will not transmit the contents of the Packet Error Check Data Register (SMB_Mem_PEC) PEC register for CRC. The SMB_Mem_HCTL.PECEN bit must not be set if this bit is set, or unspecified behavior will result.

If the read cycle results in a CRC error, the SMB_Mem_HSTS.DEVERR bit and the SMB_Mem_AUXS.CRCE bit will be set.

33.2.7 SMBus Slave Interface

The SoC does not implement a complete SMBus slave interface. Only the Host Notify Command is implemented to maintain specification compatibility.

33.2.7.1 Format of Host Notify Command

The SoC tracks and responds to the standard Host Notify command as specified in the System Management Bus (SMBus) Specification, Version 2.0. The host address for this command is fixed to 0001000b. If the SoC already has data for a previously-received host notify command which has not been serviced yet by the host software (as indicated by the SMB_Mem_SSTS.HNST bit), then it will NACK following the host address byte of the protocol. This allows the host to communicate non-acceptance to the master and retain the host notify address and data values for the previous cycle until host software completely services the interrupt.

Note: Host software must always clear the SMB_Mem_SSTS.HNST bit after completing any necessary reads of the address and data registers.

Below table shows the Host Notify format.

Table 315. Host Notify Format (Sheet 1 of 2)

Bit	Description	Driven By	Comment
1	Start	External Master	
8:2	SMB Host Address – 7 bits	External Master	Always 0001_000
9	Write	External Master	Always 0
10	ACK (or NACK)	SoC	SoC NACKs if SMB_Mem_SSTS.HNST is 1
17:11	Device Address – 7 bits	External Master	Indicates the address of the master; loaded into the Notify Device Address Register (SMB_Mem_NDA)
18	Unused – Always 0	External Master	7-bit-only address; this bit is inserted to complete the byte
19	ACK	SoC	

Table 315. Host Notify Format (Sheet 2 of 2)

Bit	Description	Driven By	Comment
27:20	Data Byte Low – 8 bits	External Master	Loaded into the Notify Data Low Byte Register (SMB_Mem_NDLB)
28	ACK	SoC	
36:29	Data Byte High – 8 bits	External Master	Loaded into the Notify Data High Byte Register (SMB_Mem_NDHB)
37	ACK	SoC	
38	Stop	External Master	

33.3 Use

33.3.1 Function Disable

The SMBus interface may be disable by setting FUNC_DIS_2.SMB_DIS to 1b.

33.3.2 SPD Write Disable

DRAM memory modules contain a 256-byte EEPROM, called SPD, accessible via SMBus used to store configuration information such as timing, physical size and more. A malicious user with administrative privileges can change and permanently lock invalid settings which could then lead to a permanent denial of service attack or a memory aliasing attack.

Write access to the SPI should be disabled by setting SMB_Config_HCFG.SPD_WD to 1b.

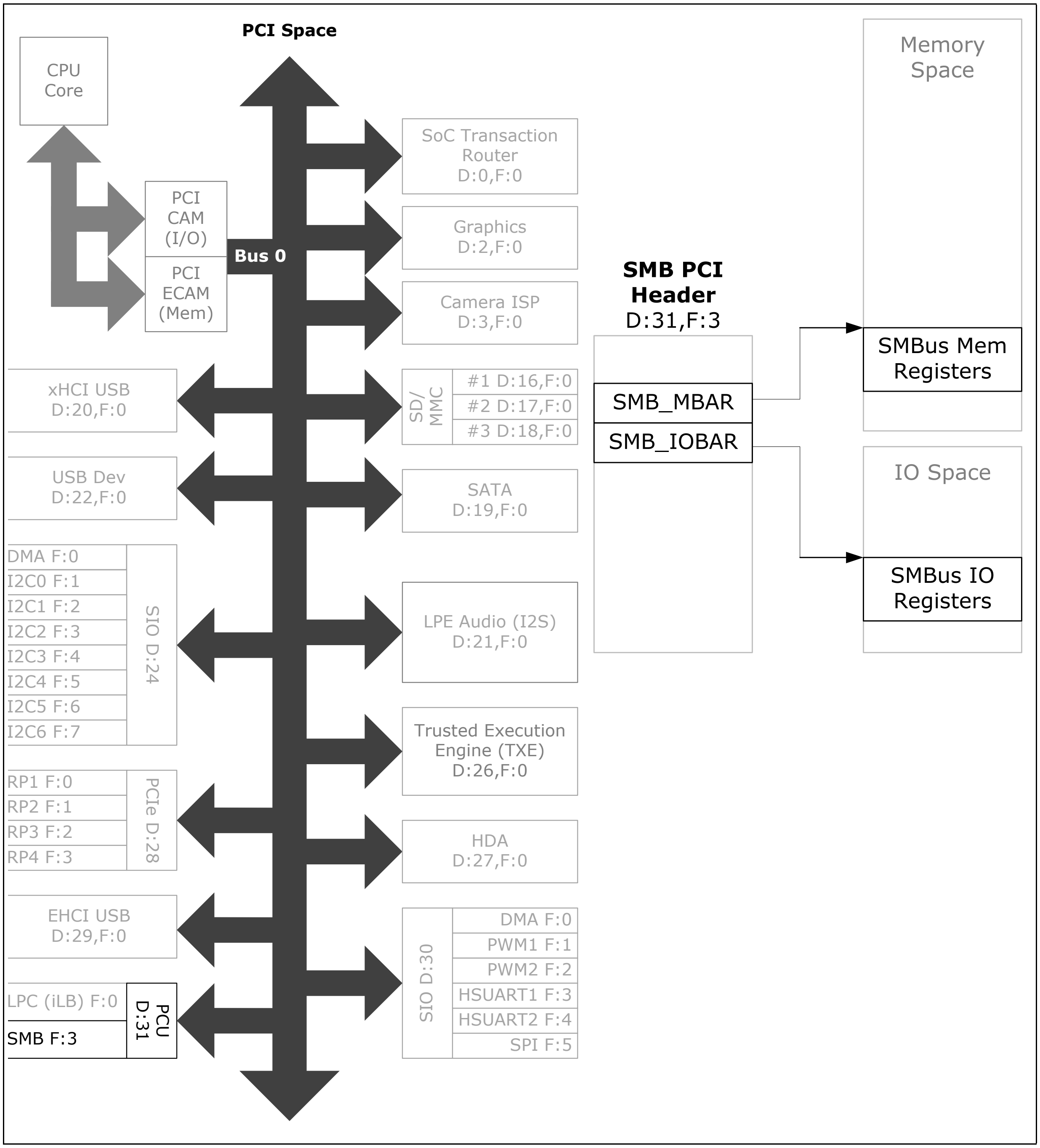
33.4 References

- System Management Bus (SMBus) Specification Version 2.0: http://www.smbus.org/specs/

33.5 Register Map

Refer to Chapter 3, “Register Access Methods” and Chapter 4, “Mapping Address Spaces” for additional information.

Figure 134.PCU - SMBus Register Map



33.6 PCU SMBUS PCI Configuration Registers

Table 316. Summary of PCU SMBUS PCI Configuration Registers—0/31/3

Offset	Size	Register ID—Description	Default Value
0h	2	“D31_F3_Vendor ID (SMB_Config_VID)—Offset 0h” on page 4452	8086h
2h	2	“D31_F3_Device ID (SMB_Config_DID)—Offset 2h” on page 4453	0F12h
4h	2	“D31_F3_Command (SMB_Config_CMD)—Offset 4h” on page 4453	0000h
6h	2	“D31_F3_Device_Status (SMB_Config_STAT)—Offset 6h” on page 4454	0290h
8h	1	“D31_F3_Revision ID (SMB_Config_REV)—Offset 8h” on page 4455	00h
9h	1	“D31_F3_Programming Interface (SMB_Config_PRGIF)—Offset 9h” on page 4455	00h
Ah	1	“D31_F3_Sub Class Code (SMB_config_SCC)—Offset Ah” on page 4456	05h
Bh	1	“D31_F3_Base Class Code (SMB_Config_BCC)—Offset Bh” on page 4456	0Ch
10h	4	“D31_F3_SMBus Memory Base Address (SMB_Config_MBARL)—Offset 10h” on page 4456	00000000h
14h	4	“D31_F3_SMBus Memory Base Address (SMB_Config_MBARH)—Offset 14h” on page 4457	00000000h
20h	4	“D31_F3_SMB Base Addr (SMB_Config_IOBAR)—Offset 20h” on page 4457	00000001h
2Ch	2	“D31_F3_SVID (SMB_Config_SVID)—Offset 2Ch” on page 4458	0000h
2Eh	2	“D31_F3_SID (SMB_Config_SID)—Offset 2Eh” on page 4458	0000h
34h	1	“D31_F3_CAP_POINTER (SMB_Config_CAP_POINTER)—Offset 34h” on page 4459	50h
3Ch	1	“D31_F3_Interrupt Line (SMB_Config_INTLN)—Offset 3Ch” on page 4459	00h
3Dh	1	“D31_F3_Interrupt Pin (SMB_Config_INTPN)—Offset 3Dh” on page 4460	02h
40h	1	“D31_F3_Host Configuration (SMB_Config_HCFG)—Offset 40h” on page 4460	00h
50h	2	“D31_F3_PID (SMB_Config_CAP_ID)—Offset 50h” on page 4461	0001h
52h	2	“D31_F3_PC (SMB_Config_PMC)—Offset 52h” on page 4461	0003h
54h	2	“D31_F3_PMCSR (SMB_Config_PMCSR)—Offset 54h” on page 4462	0008h
56h	1	“D31_F3_PMCSR_BSE (SMB_Config_PMCSR_BSE)—Offset 56h” on page 4463	00h
57h	1	“D31_F3_DATA (SMB_Config_DATA)—Offset 57h” on page 4464	00h
F0h	4	“IOSF Error Control (SMB_Config_ERR)—Offset F0h” on page 4464	00000000h
F8h	4	“D31_F3_Manufacturer's ID (SMB_Config_MANID)—Offset F8h” on page 4465	00000000h

33.6.1 D31_F3_Vendor ID (SMB_Config_VID)—Offset 0h

Vendor ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_VID: [B:0, D:31, F:3] + 0h

Default: 8086h

15			12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
VID															

Bit Range	Default & Access	Description
15:0	8086h RO	**VID:** Vendor ID

33.6.2 D31_F3_Device ID (SMB_Config_DID)—Offset 2h

Indicates the SMBus controller device number. The upper 9-bits of this register are coming from centralize DevID unit indicating this SOC. The lower 7 bits are indicating SMBus controller while the 2 most lower bits are controlled by the SMBus DID fuses.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_DID: [B:0, D:31, F:3] + 2h

Default: 0F12h

15			12				8				4				0
0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0
DID1															

Bit Range	Default & Access	Description
15:0	000011110 0010010b RO	**DID (DID1):** Device ID-SOC, value from the SETIDVALUE message

33.6.3 D31_F3_Command (SMB_Config_CMD)—Offset 4h

CMD register enables/disables memory/io space access and interrupt

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_CMD: [B:0, D:31, F:3] + 4h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSV					INTD	FBE	SERR	WCC	PER	VGAPS	PMWE	SCE	BME	MSE	IOSE

Bit Range	Default & Access	Description
15:11	00000b RO	**Reserved (RSV):** Reserved
10	0b RW	**INTD:** Interrupt disable - 1 Disable SMBus to assert its interrupt
9	0b RO	**FBE:** FBE - reserved as '0'
8	0b RO	**SERR:** SERR enable - reserved as '0'

Bit Range	Default & Access	Description
7	0b RO	**Wait Cycle Ctrl (WCC):** Wait cycle control - reserved as '0'
6	0b RO	**Parity error response (PER):** Parity error - reserved as '0'
5	0b RO	**VGA palette snnop (VGAPS):** VGA palette snoop - reserved as '0'
4	0b RO	**PMWE:** Postable Memory Write Enable - reserved as '0'
3	0b RO	**SCE:** Special Cycle Enable - reserved as '0'
2	0b RO	**BME:** Bus Master Enable - reserved as '0'
1	0b RW	**MSE:** Memory space enable - 1 enables access to the SM Bus memory space registers as defined by the Base Address Registes
0	0b RW	**IOSE:** I/O space enable - 1 enables access to the SM Bus I/O space registers as defined by the Base Address Register

33.6.4 D31_F3_Device_Status (SMB_Config_STAT)—Offset 6h

Configuration status register

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_STAT: [B:0, D:31, F:3] + 6h

Default: 0290h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		DPED	FB2B	UDF	FREQ66	CLI	INTS	RSV		

Bit Range	Default & Access	Description
15	0b RO	**DPE:** Detect Parity Error - reserved as '0'
14	0b RO	**SSE:** Signaled System Error - reserved as '0'
13	0b RO	**RMA:** Received Master Abort - reserved as '0'
12	0b RO	**RTA:** Received Target Abort - reserved as '0'
11	0b RO	**STA:** Signaled Target Abort - reserved as '0'
10:9	01b RO	**DEVT:** Devsel Timing Status reserved as 2'b01
8	0b RO	**DPED:** Data Parity Error Detected - reserved as '0'

Bit Range	Default & Access	Description
7	1b RO	**Fast Back To Back (FB2B):** Fast Back To Back Capable - reserved as '1'
6	0b RO	**UDF:** User Defined Features - reserved as '0'
5	0b RO	**66 MHz Capable (FREQ66):** 66 MHz Capable - reserved as '0'
4	1b RO	**Capabilities List Indicator (CLI):** Capabilities List Indicator - set to '1'
3	0b RO	**INTS:** This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register
2:0	000b RO	**Reserved (RSV):** Reserved

33.6.5 D31_F3_Revision ID (SMB_Config_REV)—Offset 8h

The value reported in this register is coming from centralize unit by the SETIDVALUE message

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_REV: [B:0, D:31, F:3] + 8h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
REVID							

Bit Range	Default & Access	Description
7:0	00h RO	**Revision ID (REVID):** Revision ID

33.6.6 D31_F3_Programming Interface (SMB_Config_PRGIF)—Offset 9h

The value reported in this register is coming from centralize unit by the SETIDVALUE message

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_PRGIF: [B:0, D:31, F:3] + 9h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PRGIF							

Bit Range	Default & Access	Description
7:0	00h RO	**Programming Interface (PRGIF):** Programming Interface

33.6.7 D31_F3_Sub Class Code (SMB_config_SCC)—Offset Ah

A value of 05h indicates that this device is a SM Bus serial controller

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

SMB_config_SCC: [B:0, D:31, F:3] + Ah

Default: 05h

7			4				0
0	0	0	0	0	1	0	1
SCC							

Bit Range	Default & Access	Description
7:0	05h RO	**SCC:** Sub Class Code

33.6.8 D31_F3_Base Class Code (SMB_Config_BCC)—Offset Bh

A value of 0Ch indicates that this device is a serial controller

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

SMB_Config_BCC: [B:0, D:31, F:3] + Bh

Default: 0Ch

7			4				0
0	0	0	0	1	1	0	0
BCC							

Bit Range	Default & Access	Description
7:0	0Ch RO	**BCC:** Base Class Code

33.6.9 D31_F3_SMBus Memory Base Address (SMB_Config_MBARL)—Offset 10h

The memory bar

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

SMB_Config_MBARL: [B:0, D:31, F:3] + 10h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BAR | RSV1 | PREF | IOSI | MSI

Bit Range	Default & Access	Description
31:5	000000h RW	**BAR:** Base Address - Provides the 32 byte system memory base address
4	0b RO	**Reserved (RSV1):** Reserved
3	0b RO	**PREF:** Hardwired to 0. Indicated that SMBMBAR is not prefetchable
2:1	00b RO	**Type (IOSI):** This field is hardwired to 2'b00 indicating that this range can be mapped anywhere within 32-bit address space.
0	0b RO	**MSI:** Memory Space Indicator - This read-only bit always is 0, indicating that the SMB logic is Memory mapped

33.6.10 D31_F3_SMBus Memory Base Address (SMB_Config_MBARH)—Offset 14h

RESERVED

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_MBARH: [B:0, D:31, F:3] + 14h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BAR

Bit Range	Default & Access	Description
31:0	00000000h RO	**BAR:** RESERVED

33.6.11 D31_F3_SMB Base Addr (SMB_Config_IOBAR)—Offset 20h

The I/O memory bar

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_IOBAR: [B:0, D:31, F:3] + 20h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

RSV1 | BAR | RSV2 | IOSI

Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSV1):** Reserved
15:5	000000000 00b RW	**BAR:** Base Address - Provides the 32 byte system I/O base address
4:1	0000b RO	**Reserved (RSV2):** Reserved
0	1b RO	**I/O Space Indicator (IOSI):** IO Space Indicator - This read-only bit always is 1, indicating that the SMB logic is I/O mapped

33.6.12 D31_F3_SVID (SMB_Config_SVID)—Offset 2Ch

BIOS sets the value in this register to identify the Subsystem Vendor ID. The SMBus SVID register, in combination with the SMBus Subsystem ID register, enables the operating system to distinguish each subsystem from the others. **Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.**

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_SVID: [B:0, D:31, F:3] + 2Ch

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SVID															

Bit Range	Default & Access	Description
15:0	0000h RW/O	**SVID:** Subsystem Vendor ID

33.6.13 D31_F3_SID (SMB_Config_SID)—Offset 2Eh

BIOS can write to this register to identify the Subsystem ID. The SID register, in combination with the SVID, enable the operating system to distinguish each subsystem from other(s). **Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.**

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_SID: [B:0, D:31, F:3] + 2Eh

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SID															

Bit Range	Default & Access	Description
15:0	0000h RW/O	**SID:** Subsystem ID

33.6.14 D31_F3_CAP_POINTER (SMB_Config_CAP_POINTER)—Offset 34h

This optional register is used to point to a linked list of new capabilities implemented by this device. This register is only valid if the Capabilities List bit in the Status Register is set. If implemented, the bottom two bits are reserved and should be set to 00b. Software should mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities.

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

SMB_Config_CAP_POINTER: [B:0, D:31, F:3] + 34h

Default: 50h

7			4				0
0	1	0	1	0	0	0	0
CP							

Bit Range	Default & Access	Description
7:0	50h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

33.6.15 D31_F3_Interrupt Line (SMB_Config_INTLN)—Offset 3Ch

This data is not used

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

SMB_Config_INTLN: [B:0, D:31, F:3] + 3Ch

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
INTLN							

Bit Range	Default & Access	Description
7:0	00h RW	**INTLN:** Intrerrupt Line

33.6.16 D31_F3_Interrupt Pin (SMB_Config_INTPN)—Offset 3Dh

This register reflects the D31IP.SMIP in chipset configuration space

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_INTPN: [B:0, D:31, F:3] + 3Dh

Default: 02h

7			4				0
0	0	0	0	0	0	1	0
INTPN							

Bit Range	Default & Access	Description
7:0	02h RO	**INTPN:** The 4 msb bits are hardwired to 0, and the 4 lsb bitsare hardwired to 4'h2 indicates the INTB is used by the SMBus controller

33.6.17 D31_F3_Host Configuration (SMB_Config_HCFG)—Offset 40h

Host Configuration Register

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_HCFG: [B:0, D:31, F:3] + 40h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSV1			SPD_WD	SSRST	I2C_EN	SMI_EN	HST_EN

Bit Range	Default & Access	Description
7:5	000b RO	**Reserved (RSV1):** Reserved
4	0b RW/O	**SPD write disable (SPD_WD):** This bit is must be set to 1b1 to disable writes to SPD which are on Host SMB address ranges 0xA0 0xAE. The SMBus range is unwriteable until next platform reset HW Default is 1b0. Note: This bit is locked on 1b1 and will be reset on PLTRST# reset. This should be set by BIOS memory reference code to 1b1. SW can only program this bit when both HCTL[6] = 1b0 (START) and HSTS[0] = 1b0 (HBSY), else it may result in an undefined behavior.
3	0b RW	**SSRST:** Soft SMBus Reset - When this bit is 1, the SMbus state machine and logic is reset. The HW will reset this bit to 0 when reset operation is completed
2	0b RW	**I2C_EN:** When this bit is 1, the SMBus host is enabled to communicate with I2C devices. This will change the formatting of some commands. When this bit is 0, behavior is for SMBus
1	0b RW	**SMI_EN:** When this bit is set, any source of an SMB interrupt will instead be routed to generate an SMI

Bit Range	Default & Access	Description
0	0b RW	**HST_EN:** When set, the SMB Host Controller interface is enabled to execute commands. The SMB_Mem_HCTL.INTREN bit needs to be enabled in order for the SMB Host Controller to interrupt or SMI#. Additionally, the SMB Host Controller will not respond to any new requests until all interrupt requests have been cleared

33.6.18 D31_F3_PID (SMB_Config_CAP_ID)—Offset 50h

Power Management Capability ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_CAP_ID: [B:0, D:31, F:3] + 50h

Default: 0001h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Next_Item_Ptr								Cap_ID							

Bit Range	Default & Access	Description
15:8	00h RO	**Next Item Pointer (Next_Item_Ptr):** This field provides an offset into the functions PCI Configuration Space pointing to the location of next item in the functions capability list. If there are no additional items in the Capabilities List, this register is set to 00h.
7:0	01h RO	**Capability Identifier (Cap_ID):** This field, when 01h identifies the linked list item as being the PCI Power Management registers.

33.6.19 D31_F3_PC (SMB_Config_PMC)—Offset 52h

Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_PMC: [B:0, D:31, F:3] + 52h

Default: 0003h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
PMES					D2S	D1S	AC			DSI	RSV1	PMEC	VS		

Bit Range	Default & Access	Description
15:11	00000b RO	**PME_Support (PMES):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1 bit(13) X X1XXb - PME# can be asserted from D2 bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold

Bit Range	Default & Access	Description
10	0b RO	**D2_Support (D2S):** If this bit is a '1', this function supports the D2 Power Management State. Functions that do not support D2 must always return a value of '0' for this bit.
9	0b RO	**D1_Support (D1S):** If this bit is a '1', this function supports the D1 Power Management State. Functions that do not support D2 must always return a value of '0' for this bit.
8:6	000b RO	**Aux_Current (AC):** Auxiliary current - should be 3'b000
5	0b RO	**DSI:** Device specific initialization
4	0b RO	**Reserved (RSV1):** Reserved
3	0b RO	**PME Clock (PMEC):** PME Clock. Does not apply.
2:0	011b RO	**Version (VS):** A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.

33.6.20 D31_F3_PMCSR (SMB_Config_PMCSR)—Offset 54h

Power Management Control/Status Register

Access Method

Type: PCI Configuration Register
(Size: 16 bits)

SMB_Config_PMCSR: [B:0, D:31, F:3] + 54h

Default: 0008h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
PMES	DATA_SCALE		DATA_SEL				PMEE	RSV1				DSI	RSV2	PS	

Bit Range	Default & Access	Description
15	0b RO	**PME_Status (PMES):** SMBus does not initiate PME#. Hence this bit should be always '0'
14:13	00b RO	**Data_Scale (DATA_SCALE):** If the Data register has not been implemented, this field must return '00b' when the PMCSR is read.
12:9	0000b RO	**Data_Select (DATA_SEL):** If the Data register is not implemented, this field should be read only and return '0000b' when the PMCSR is read.
8	0b RO	**PME_En (PMEE):** Should be '0' since SMBus does not initiate PME#
7:4	0000b RO	**Reserved (RSV1):** Reserved

Bit Range	Default & Access	Description
3	1b RO	**No_Soft_Reset (DSI):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0b RO	**Reserved (RSV2):** Reserved
1:0	00b RW	**PowerState (PS):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

33.6.21 D31_F3_PMCSR_BSE (SMB_Config_PMCSR_BSE)—Offset 56h

PMCSR_BSE supports PCI bridge specific functionality and is required for all PCI-to-PCI bridges.

Access Method

Type: PCI Configuration Register
(Size: 8 bits)

SMB_Config_PMCSR_BSE: [B:0, D:31, F:3] + 56h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
BPCCE	B23	RSV1					

Bit Range	Default & Access	Description
7	0b RO	**BPCC_En (BPCCE):** Bus Power/Clock Control Enable - Does not apply
6	0b RO	**B2_B3 (B23):** B2/B3 support for D3hot - Does not apply
5:0	00h RO	**Reserved (RSV1):** Reserved

33.6.22 D31_F3_DATA (SMB_Config_DATA)—Offset 57h

PMCSR_BSE supports PCI bridge specific functionality and is required for all PCI-to-PCI bridges.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_DATA: [B:0, D:31, F:3] + 57h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
DT							

Bit Range	Default & Access	Description
7:0	00h RO	**Data (DT):** Data - Does not apply

33.6.23 IOSF Error Control (SMB_Config_ERR)—Offset F0h

IOSF Error Control- is set when an Unsupported Request Detected

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_ERR: [B:0, D:31, F:3] + F0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSV1																															URD

Bit Range	Default & Access	Description
31:1	0000h RO	**Reserved (RSV1):** Reserved
0	0b RW	**URD:** Unsupported Request Detected, SMBus could not receive unsupported request hence this bit is tied to 1b0

33.6.24 D31_F3_Manufacturer's ID (SMB_Config_MANID)—Offset F8h

Manufacturer's ID Register,The value reported in this register is coming from centralize unit by the SETIDVALUE message

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_MANID: [B:0, D:31, F:3] + F8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSV1				DOTID				SID								MID								PPID							

Bit Range	Default & Access	Description
31:28	00h RO	**Reserved (RSV1):** Reserved
27:24	0000b RO	**DOTID:** The value reported in this field is coming from centralize unit by the SETIDVALUE message
23:16	00h RO	**SID:** The value reported in this field is coming from centralize unit by the SETIDVALUE message
15:8	00h RO	**MID:** The value reported in this field is coming from centralize unit by the SETIDVALUE message
7:0	00h RO	**PPID:** The value reported in this field is coming from centralize unit by the SETIDVALUE message

33.7 PCU SMBUS Memory Mapped I/O Registers

Table 317. Summary of PCU SMBUS Memory Mapped I/O Registers—SMB_Config_MBARL

Offset	Size	Register ID—Description	Default Value
0h	1	"Host Status Register (SMB_Mem_HSTS)—Offset 0h" on page 4466	00h
2h	1	"Host Control Register (SMB_Mem_HCTL)—Offset 2h" on page 4467	00h
3h	1	"Host Command Register (SMB_Mem_HCMD)—Offset 3h" on page 4470	00h
4h	1	"Transmit Slave Address Register (SMB_Mem_TSA)—Offset 4h" on page 4470	00h
5h	1	"Data 0 Register (SMB_Mem_HD0)—Offset 5h" on page 4471	00h
6h	1	"Data 1 Register (SMB_Mem_HD1)—Offset 6h" on page 4471	00h
7h	1	"Host Block Data (SMB_Mem_HBD)—Offset 7h" on page 4471	00h
8h	1	"Packet Error Check Data Register (SMB_Mem_PEC)—Offset 8h" on page 4472	00h
Ch	1	"Auxiliary Status (SMB_Mem_AUXS)—Offset Ch" on page 4473	00h
Dh	1	"Auxiliary Control (SMB_Mem_AUXC)—Offset Dh" on page 4473	00h
Fh	1	"SMBUS_PIN_CTL Register (SMB_Mem_SMBC)—Offset Fh" on page 4474	07h
10h	1	"Slave Status Register (SMB_Mem_SSTS)—Offset 10h" on page 4474	00h
11h	1	"Slave Command Register (SMB_Mem_SCMD)—Offset 11h" on page 4475	00h
14h	1	"Notify Device Address Register (SMB_Mem_NDA)—Offset 14h" on page 4476	00h
16h	1	"Notify Data Low Byte Register (SMB_Mem_NDLB)—Offset 16h" on page 4476	00h
17h	1	"Notify Data High Byte Register (SMB_Mem_NDHB)—Offset 17h" on page 4477	00h

33.7.1 Host Status Register (SMB_Mem_HSTS)—Offset 0h

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_HSTS: [MBARL] + 0h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
BDS	IUS	SMB_ALERTB	FAILED	BERR	DEVERR	INTR	HBSY

Bit Range	Default & Access	Description
7	0b RW	**BDS:** BYTE_DONE_STS (BDS) - This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit has no meaning for block transfers when the 32-byte buffer is enabled.**Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the SMBus host will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.**
6	0b RW	**IUS:** In Use Status (IUS) - After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the SMBus host
5	0b RW	**SMB_ALERTB:** the SOC sets this bit to a '1' to indicates source of the interrupt or SMI# was the SMB_ALERTB signal. Software resets this bit by writing a 1 to this location.
4	0b RW	**FAILED:** Failed (FAIL) - When set, this indicates that the source of the interrupt or SMI was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0b RW	**BERR:** Bus Error (BERR) - When set, this indicates the source of the interrupt or SMI was a transaction collision.
2	0b RW	**DEVERR:** Device Error (DERR) - When set, this indicates that the source of the interrupt or SMI was due one of the following: Illegal Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error Write Protection Access Error (START bit will be cleared, Device Error will be set and Host Busy is never set because SMB Transaction never took place).
1	0b RW	**INTR:** Interrupt (INTR) - When set, this indicates that the source of the interrupt or SMI was the successful completion of its last command.
0	0b RW	**HBSY:** Host Busy (HBSY) - A '1' indicates that the SMBus host is running a command from the host interface. No SMB registers should be accessed while this bit is set. Exception: The BLOCK DATA REGISTER can be accessed when this bit is set ONLY when the SMB_CMD bits (in Host control register) are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

33.7.2 Host Control Register (SMB_Mem_HCTL)—Offset 2h

Host Control Register

Note: A read to this register will clear the pointer in the 32-byte buffer.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_HCTL: [MBARL] + 2h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PECEN	SATRT	LBYTE	SMBCMD			KILL	INTREN

Bit Range	Default & Access	Description
7	0b RW	**PECEN:** PEC_EN: When set to '1', this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to '0', the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.
6	0b WO	**START (SATRT):** START: This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a '1' to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the SMBus controller has finished the command.
5	0b RW	**LBYTE:** LAST_BYTE: Used for I2C Read commands as an indication that the next byte will be the last one to be received for that block. The algorithm and usage model for this bit will be as follows (assume a message of n bytes): A. When the software sees the BYTE_DONE_STS bit set (bit 7 in the SMBus Host Status Register) for each of bytes 1 through n-2 of the message, the software should then read the Block Data Byte Register to get the byte that was just received. B. After reading each of bytes 1 to n-2 of the message, the software will then clear the BYTE_DONE_STS bit. C. After receiving byte n-1 of the message, the software will then set the 'LAST BYTE' bit. The software will then clear the BYTE_DONE_STS bit. D. The Intel SOC will then receive the last byte of the message (byte n). However, the Intel SOC state machine will see the LAST BYTE bit set, and instead of sending an ACK after receiving the last byte, it will instead send a NAK. E. After receiving the last byte (byte n), the software will still clear the BYTE_DONE_STS bit. However, the LAST_BYTE bit will be irrelevant at that point. Note: This bit may be set when the TCO timer causes the SECOND_TO_STS bit to be set. See the TCO_STS.SECOND_TO_STS register, for more details on that bit. The SMBus device driver should clear the LAST_BYTE bit (if it is set) before starting any new command. Note: In addition to I2C Read Commands, the LAST_BYTE bit will also cause Block Read/Write cycles to stop prematurely (at the end of the next byte).

Bit Range	Default & Access	Description
4:2	000b RW	**SMBCMD:** SMB_CMD - As shown by the bit encoding below, indicates which command the SMBus host is to perform. If enabled, the SMBus host will generate an interrupt or SMI when the command has completed If the value is for a non-supported or reserved command, the SMBus host will set the device error (DEV_ERR) status bit and generate an interrupt when the START bit is set. The SMBus controller will perform no command, and will not operate until DEV_ERR is cleared.***3'b000 - Quick*** The slave address and read/write value (bit 0) are stored in the tx slave address register ***3'b001 - Byte*** This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 register will contain the read data. ***3'b010 - Byte Data*** This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data ***3'b011 - Word Data*** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. ***3'b100 - Process Call*** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. ***3'b101 - Block*** This command uses the transmit slave address, command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. ***3'b110 - I2C Read*** This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The Intel SOC will continue reading data until the NAK is received. ***3'b111 - Block Process*** This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. **Note: E32B bit in the Auxiliary Control Register must be set for this command to work.**
1	0b RW	**KILL:** KILL - When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI) selected by the SMB_Cfg_HCFG.SMI_EN field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally
0	0b RW	**INTREN:** Enable the generation of an interrupt or SMI upon the completion of the command. Enables also other interrupt sendings , like ALERT and HOST_NOTIFY

33.7.3 Host Command Register (SMB_Mem_HCMD)—Offset 3h

This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_HCMD: [MBARL] + 3h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HCMD							

Bit Range	Default & Access	Description
7:0	00h RW	**HCMD:** Command to be transmitted

33.7.4 Transmit Slave Address Register (SMB_Mem_TSA)—Offset 4h

This register is transmitted by the host controller in the slave address field of the SMB protocol. This is the address of the target

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_TSA: [MBARL] + 4h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
ADDR							RW

Bit Range	Default & Access	Description
7:1	0000000b RW	**ADDR:** 7-bit address of the targeted slave
0	0b RW	**RW:** Direction of the host transfer. 1 = read, 0 = write Note: Writes to TSA values of 0xA0 0xAE are blocked depending on the setting of the SPD write disable bit in HCFG D31_F3_HostConfiguration.

33.7.5 Data 0 Register (SMB_Mem_HD0)—Offset 5h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_HD0: [MBARL] + 5h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HD0							

Bit Range	Default & Access	Description
7:0	00h RW	**HD0:** DATA0/COUNT - This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

33.7.6 Data 1 Register (SMB_Mem_HD1)—Offset 6h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_HD1: [MBARL] + 6h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HD1							

Bit Range	Default & Access	Description
7:0	00h RW	**HD1:** DATA1 - This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

33.7.7 Host Block Data (SMB_Mem_HBD)—Offset 7h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_HBD: [MBARL] + 7h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HBD							

Bit Range	Default & Access	Description
7:0	00h RW	**HBD:** Block Data (BDTA) - This is either a register, or a pointer into a 32-byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the INTEL SOC. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E32B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E32B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the FIFO pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E32B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the FIFO pointed to by this register. If the byte count has been exhausted or the 32-byte FIFO has been filled, the controller will generate an SMI or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the FIFO to when the DONE_STS bit is cleared, the controller will insert wait-states on the interface.

33.7.8 Packet Error Check Data Register (SMB_Mem_PEC)—Offset 8h

This register contains the 8-bit CRC value that is used as the Packet Error Check on SMBus. For writes, this register is written by software prior to running the command. For reads, this register is read by software after the read command is completed on SMBus.

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_PEC: [MBARL] + 8h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PEC							

Bit Range	Default & Access	Description
7:0	00h RW	**PEC:** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the IUS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

33.7.9 Auxiliary Status (SMB_Mem_AUXS)—Offset Ch

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_AUXS: [MBARL] + Ch

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD							CRCE

Bit Range	Default & Access	Description
7:1	0000000b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**CRCE:** CRC Error (CRCE) - This bit is set if a received message contained a CRC error. When this bit is set, the DEVERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after SMBus controller has received the final data bit transmitted by external slave.

33.7.10 Auxiliary Control (SMB_Mem_AUXC)—Offset Dh

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_AUXC: [MBARL] + Dh

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSV1						E32B	AAC

Bit Range	Default & Access	Description
7:2	000000b RO	**Reserved (RSV1):** Reserved
1	0b RW	**E32B:** Enable 32-byte Buffer (E32B) - When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the controller generates an interrupt
0	0b RW/O	**AAC:** Automatically Append CRC (AAC) - When set, the SMBus controller will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

33.7.11 SMBUS_PIN_CTL Register (SMB_Mem_SMBC)—Offset Fh

Software bus accesses register

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_SMBC: [MBARL] + Fh

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 07h

7			4				0
0	0	0	0	0	1	1	1
RSV1					SMBCLKCTL	SMBDAT	SMBCLK

Bit Range	Default & Access	Description
7:3	00000b RO	**Reserved (RSV1):** Reserved
2	1b RW	**SMBCLKCTL:** This Read/Write bit has a default of 1. 0 = SMBus controller will drive the SMB_CLK pin low, independent of what the other SMB logic would otherwise indicate for the SMB_CLK pin. 1 = The SMB_CLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	1b RO	**SMBDAT:** This pin returns the value on the SMB_DATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	1b RO	**SMBCLK:** This pin returns the value on the SMB_CLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

33.7.12 Slave Status Register (SMB_Mem_SSTS)—Offset 10h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_SSTS: [MBARL] + 10h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSV1							HNST

Bit Range	Default & Access	Description
7:1	0000000b RO	**Reserved (RSV1):** Reserved
0	0b RW	**HNST:** HOST_NOTIFY_STS: The SMBus controller sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the SMBus controller will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the SMBus controller will NACK the first byte (host address) of any new 'Host Notify' commands on the SMBus. Writing a 0 to this bit has no effect.

33.7.13 Slave Command Register (SMB_Mem_SCMD)—Offset 11h

All bits in this register are implemented in a slow (64khz) clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_SCMD: [MBARL] + 11h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSV1					SMBALTDIS	HNWAKEEN	HNINTREN

Bit Range	Default & Access	Description
7:3	00000b RO	**Reserved (RSV1):** Reserved
2	0b RW	**SMBALTDIS:** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMB_ALERTB source. This bit is logically inverted and 'AND'ed with the SMB_ALERTB bit of HSTS register. The resulting signal is distributed to the SMI# and/or interrupt generation logic.
1	0b RW	**HNWAKEEN:** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event.
0	0b RW	**HNINTREN:** Software sets this bit to 1 to enable the generation of interrupt or SMI when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either INTRB or SMI is generated, depending on the value of the SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI) will be generated. The interrupt (or SMI) is logically generated by AND'ing the STS and INTREN bits.

33.7.14 Notify Device Address Register (SMB_Mem_NDA)—Offset 14h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_NDA: [MBARL] + 14h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
NDA							RSV1

Bit Range	Default & Access	Description
7:1	0000000b RO	**NDA:** DEVICE_ADDRESS - This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	0b RO	**Reserved (RSV1):** Reserved

33.7.15 Notify Data Low Byte Register (SMB_Mem_NDLB)—Offset 16h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_NDLB: [MBARL] + 16h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
NDLB							

Bit Range	Default & Access	Description
7:0	00h RO	**NDLB:** DATA_LOW_BYTE - This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

33.7.16 Notify Data High Byte Register (SMB_Mem_NDHB)—Offset 17h

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

SMB_Mem_NDHB: [MBARL] + 17h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
NDHB							

Bit Range	Default & Access	Description
7:0	00h RO	**NDHB:** DATA_HIGH_BYTE - This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

33.8 PCU SMBUS I/O Registers

Table 318. Summary of PCU SMBUS I/O Registers—SMB_Config_IOBAR

Offset	Size	Register ID—Description	Default Value
0h	1	"Host Status Register (SMB_Mem_HSTS_io)—Offset 0h" on page 4478	00h
2h	1	"Host Control Register (SMB_Mem_HCTL_io)—Offset 2h" on page 4479	00h
3h	1	"Host Command Register (SMB_Mem_HCMD_io)—Offset 3h" on page 4482	00h
4h	1	"Transmit Slave Address Register (SMB_Mem_TSA_io)—Offset 4h" on page 4482	00h
5h	1	"Data 0 Register (SMB_Mem_HD0_io)—Offset 5h" on page 4483	00h
6h	1	"Data 1 Register (SMB_Mem_HD1_io)—Offset 6h" on page 4483	00h
7h	1	"Host Block Data (SMB_Mem_HBD_io)—Offset 7h" on page 4483	00h
8h	1	"Packet Error Check Data Register (SMB_Mem_PEC_io)—Offset 8h" on page 4484	00h
Ch	1	"Auxiliary Status (SMB_Mem_AUXS_io)—Offset Ch" on page 4485	00h
Dh	1	"Auxiliary Control (SMB_Mem_AUXC_io)—Offset Dh" on page 4485	00h
Fh	1	"SMBUS_PIN_CTL Register (SMB_Mem_SMBC_io)—Offset Fh" on page 4486	07h
10h	1	"Slave Status Register (SMB_Mem_SSTS_io)—Offset 10h" on page 4486	00h
11h	1	"Slave Command Register (SMB_Mem_SCMD_io)—Offset 11h" on page 4487	00h
14h	1	"Notify Device Address Register (SMB_Mem_NDA_io)—Offset 14h" on page 4488	00h
16h	1	"Notify Data Low Byte Register (SMB_Mem_NDLB_io)—Offset 16h" on page 4488	00h
17h	1	"Notify Data High Byte Register (SMB_Mem_NDHB_io)—Offset 17h" on page 4489	00h

33.8.1 Host Status Register (SMB_Mem_HSTS_io)—Offset 0h

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HSTS_io: [IOBAR] + 0h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
BDS	IUS	SMB_ALERTB	FAILED	BERR	DEVERR	INTR	HBSY

Bit Range	Default & Access	Description
7	0b RW	**BDS:** BYTE_DONE_STS (BDS) - This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit has no meaning for block transfers when the 32-byte buffer is enabled.**Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the SMBus host will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.**
6	0b RW	**IUS:** In Use Status (IUS) - After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the SMBus host
5	0b RW	**SMB_ALERTB:** the SOC sets this bit to a '1' to indicates source of the interrupt or SMI# was the SMB_ALERTB signal. Software resets this bit by writing a 1 to this location.
4	0b RW	**FAILED:** Failed (FAIL) - When set, this indicates that the source of the interrupt or SMI was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0b RW	**BERR:** Bus Error (BERR) - When set, this indicates the source of the interrupt or SMI was a transaction collision.
2	0b RW	**DEVERR:** Device Error (DERR) - When set, this indicates that the source of the interrupt or SMI was due one of the following: Illegal Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error Write Protection Access Error (START bit will be cleared, Device Error will be set and Host Busy is never set because SMB Transaction never took place).
1	0b RW	**INTR:** Interrupt (INTR) - When set, this indicates that the source of the interrupt or SMI was the successful completion of its last command.
0	0b RW	**HBSY:** Host Busy (HBSY) - A '1' indicates that the SMBus host is running a command from the host interface. No SMB registers should be accessed while this bit is set. Exception: The BLOCK DATA REGISTER can be accessed when this bit is set ONLY when the SMB_CMD bits (in Host control register) are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

33.8.2 Host Control Register (SMB_Mem_HCTL_io)—Offset 2h

Host Control Register

Note: A read to this register will clear the pointer in the 32-byte buffer.

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HCTL_io: [IOBAR] + 2h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PECEN	SATRT	LBYTE	SMBCMD			KILL	INTREN

Bit Range	Default & Access	Description
7	0b RW	**PECEN:** PEC_EN: When set to '1', this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to '0', the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.
6	0b WO	**START (SATRT):** START: This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a '1' to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the SMBus controller has finished the command.
5	0b RW	**LBYTE:** LAST_BYTE: Used for I2C Read commands as an indication that the next byte will be the last one to be received for that block. The algorithm and usage model for this bit will be as follows (assume a message of n bytes): A. When the software sees the BYTE_DONE_STS bit set (bit 7 in the SMBus Host Status Register) for each of bytes 1 through n-2 of the message, the software should then read the Block Data Byte Register to get the byte that was just received. B. After reading each of bytes 1 to n-2 of the message, the software will then clear the BYTE_DONE_STS bit. C. After receiving byte n-1 of the message, the software will then set the 'LAST BYTE' bit. The software will then clear the BYTE_DONE_STS bit. D. The Intel PCH will then receive the last byte of the message (byte n). However, the Intel PCH state machine will see the LAST BYTE bit set, and instead of sending an ACK after receiving the last byte, it will instead send a NAK. E. After receiving the last byte (byte n), the software will still clear the BYTE_DONE_STS bit. However, the LAST_BYTE bit will be irrelevant at that point. Note: This bit may be set when the TCO timer causes the SECOND_TO_STS bit to be set. See the TCO2_STS Register in Volume 1, bit 1 for more details on that bit. The SMBus device driver should clear the LAST_BYTE bit (if it is set) before starting any new command. Note: In addition to I2C Read Commands, the LAST_BYTE bit will also cause Block Read/Write cycles to stop prematurely (at the end of the next byte).

Bit Range	Default & Access	Description
4:2	000b RW	**SMBCMD:** SMB_CMD - As shown by the bit encoding below, indicates which command the SMBus host is to perform. If enabled, the SMBus host will generate an interrupt or SMI when the command has completed If the value is for a non-supported or reserved command, the SMBus host will set the device error (DEV_ERR) status bit and generate an interrupt when the START bit is set. The SMBus controller will perform no command, and will not operate until DEV_ERR is cleared.***3'b000 - Quick*** The slave address and read/write value (bit 0) are stored in the tx slave address register ***3'b001 - Byte*** This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 register will contain the read data. ***3'b010 - Byte Data*** This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data ***3'b011 - Word Data*** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. ***3'b100 - Process Call*** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. ***3'b101 - Block*** This command uses the transmit slave address, command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. ***3'b110 - I2C Read*** This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The Intel PCH will continue reading data until the NAK is received. ***3'b111 - Block Process*** This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. **Note: E32B bit in the Auxiliary Control Register must be set for this command to work.**
1	0b RW	**KILL:** KILL - When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI) selected by the SMB_INTRSEL field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally
0	0b RW	**INTREN:** Enable the generation of an interrupt or SMI upon the completion of the command. Enables also other interrupt sendings , like ALERT and HOST_NOTIFY

33.8.3 Host Command Register (SMB_Mem_HCMD_io)—Offset 3h

This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HCMD_io: [IOBAR] + 3h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HCMD							

Bit Range	Default & Access	Description
7:0	00h RW	**HCMD:** Command to be transmitted

33.8.4 Transmit Slave Address Register (SMB_Mem_TSA_io)—Offset 4h

This register is transmitted by the host controller in the slave address field of the SMB protocol. This is the address of the target

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_TSA_io: [IOBAR] + 4h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
ADDR							RW

Bit Range	Default & Access	Description
7:1	0000000b RW	**ADDR:** 7-bit address of the targeted slave
0	0b RW	**RW:** Direction of the host transfer. 1 = read, 0 = write Note: Writes to TSA values of 0xA0 0xAE are blocked depending on the setting of the SPD write disable bit in HCFG D31_F3_HostConfiguration.

33.8.5 Data 0 Register (SMB_Mem_HD0_io)—Offset 5h

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HD0_io: [IOBAR] + 5h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HD0							

Bit Range	Default & Access	Description
7:0	00h RW	**HD0:** DATA0/COUNT - This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

33.8.6 Data 1 Register (SMB_Mem_HD1_io)—Offset 6h

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HD1_io: [IOBAR] + 6h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HD1							

Bit Range	Default & Access	Description
7:0	00h RW	**HD1:** DATA1 - This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

33.8.7 Host Block Data (SMB_Mem_HBD_io)—Offset 7h

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HBD_io: [IOBAR] + 7h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
HBD							

Bit Range	Default & Access	Description
7:0	00h RW	**HBD:** Block Data (BDTA) - This is either a register, or a pointer into a 32-byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the INTEL SOC. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E32B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E32B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the FIFO pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E32B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the FIFO pointed to by this register. If the byte count has been exhausted or the 32-byte FIFO has been filled, the controller will generate an SMI or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the FIFO to when the DONE_STS bit is cleared, the controller will insert wait-states on the interface.

33.8.8 Packet Error Check Data Register (SMB_Mem_PEC_io)—Offset 8h

This register contains the 8-bit CRC value that is used as the Packet Error Check on SMBus. For writes, this register is written by software prior to running the command. For reads, this register is read by software after the read command is completed on SMBus.

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_PEC_io: [IOBAR] + 8h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PEC							

Bit Range	Default & Access	Description
7:0	00h RW	**PEC:** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the IUS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

33.8.9 Auxiliary Status (SMB_Mem_AUXS_io)—Offset Ch

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_AUXS_io: [IOBAR] + Ch

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD							CRCE

Bit Range	Default & Access	Description
7:1	0000000b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**CRCE:** CRC Error (CRCE) - This bit is set if a received message contained a CRC error. When this bit is set, the DEVERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after SMBus controller has received the final data bit transmitted by external slave.

33.8.10 Auxiliary Control (SMB_Mem_AUXC_io)—Offset Dh

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_AUXC_io: [IOBAR] + Dh

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSV1						E32B	AAC

Bit Range	Default & Access	Description
7:2	000000b RO	**Reserved (RSV1):** Reserved
1	0b RW	**E32B:** Enable 32-byte Buffer (E32B) - When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the controller generates an interrupt
0	0b RW/O	**AAC:** Automatically Append CRC (AAC) - When set, the SMBus controller will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

33.8.11 SMBUS_PIN_CTL Register (SMB_Mem_SMBC_io)—Offset Fh

Software bus accesses register

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_SMBC_io: [IOBAR] + Fh

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 07h

7			4				0
0	0	0	0	0	1	1	1
RSV1					SMBCLKCTL	SMBDAT	SMBCLK

Bit Range	Default & Access	Description
7:3	00000b RO	**Reserved (RSV1):** Reserved
2	1b RW	**SMBCLKCTL:** This Read/Write bit has a default of 1. 0 = SMBus controller will drive the SMB_CLK pin low, independent of what the other SMB logic would otherwise indicate for the SMB_CLK pin. 1 = The SMB_CLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	1b RO	**SMBDAT:** This pin returns the value on the SMB_DATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	1b RO	**SMBCLK:** This pin returns the value on the SMB_CLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

33.8.12 Slave Status Register (SMB_Mem_SSTS_io)—Offset 10h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_SSTS_io: [IOBAR] + 10h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSV1							HNST

Bit Range	Default & Access	Description
7:1	0000000b RO	**Reserved (RSV1):** Reserved
0	0b RW	**HNST:** HOST_NOTIFY_STS: The SMBus controller sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the SMBus controller will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the SMBus controller will NACK the first byte (host address) of any new 'Host Notify' commands on the SMBus. Writing a 0 to this bit has no effect.

33.8.13 Slave Command Register (SMB_Mem_SCMD_io)—Offset 11h

All bits in this register are implemented in a slow (64khz) clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_SCMD_io: [IOBAR] + 11h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSV1					SMBALTDIS	HNWAKEEN	HNINTREN

Bit Range	Default & Access	Description
7:3	00000b RO	**Reserved (RSV1):** Reserved
2	0b RW	**SMBALTDIS:** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMB_ALERTB source. This bit is logically inverted and 'AND'ed with the SMB_ALERTB bit of HSTS register. The resulting signal is distributed to the SMI# and/or interrupt generation logic.
1	0b RW	**HNWAKEEN:** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event.
0	0b RW	**HNINTREN:** Software sets this bit to 1 to enable the generation of interrupt or SMI when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either INTRB or SMI is generated, depending on the value of the SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI) will be generated. The interrupt (or SMI) is logically generated by AND'ing the STS and INTREN bits.

33.8.14 Notify Device Address Register (SMB_Mem_NDA_io)—Offset 14h

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_NDA_io: [IOBAR] + 14h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
NDA							RSV1

Bit Range	Default & Access	Description
7:1	0000000b RO	**NDA:** DEVICE_ADDRESS - This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	0b RO	**Reserved (RSV1):** Reserved

33.8.15 Notify Data Low Byte Register (SMB_Mem_NDLB_io)—Offset 16h

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_NDLB_io: [IOBAR] + 16h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
NDLB							

Bit Range	Default & Access	Description
7:0	00h RO	**NDLB:** DATA_LOW_BYTE - This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

33.8.16 Notify Data High Byte Register (SMB_Mem_NDHB_io)—Offset 17h

Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_NDHB_io: [IOBAR] + 17h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
NDHB							

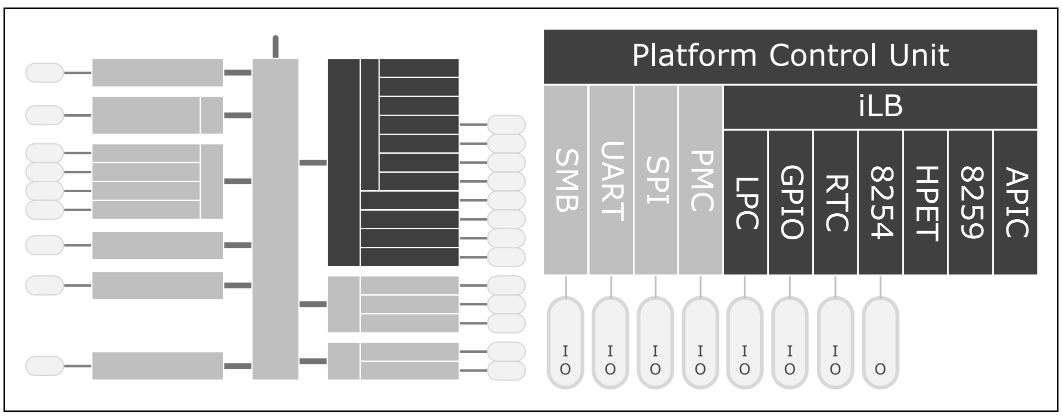
Bit Range	Default & Access	Description
7:0	00h RO	**NDHB:** DATA_HIGH_BYTE - This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

34 PCU – Intel® Legacy Block (iLB) Overview

The Intel Legacy Block (iLB) is a collection of disparate functional blocks that are critical for implementing the legacy PC platform features. These blocks include:

- PCU – iLB – Low Pin Count (LPC) Bridge
- PCU – iLB – Real Time Clock (RTC)
- PCU – iLB – 8254 Timers
- PCU – iLB – High Precision Event Timer (HPET)
- PCU – iLB – GPIO
- PCU – iLB – IO APIC
- PCU – iLB – 8259 Programmable Interrupt Controllers (PIC)

The iLB also implements a register range for configuration of some of those blocks along with support for Non-Maskable Interrupts (NMI).



34.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details as well as the subsequent sections.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 319. iLB Signals

Signal Name	Direction Plat. Power	Description
ILB_NMI	I V1P8S	Non-Maskable Interrupt: This is an NMI event indication into the SoC. *This signal is muxed and may be used by other functions.*

34.2 Features

34.2.1 Key Features

The key features of various blocks are as follows:

- Subtractive agent for the PCU
- LPC Interface
  — Supports Low Pin Count (LPC) 1.1 Specification
  — No support for DMA or bus mastering
  — Supports Trusted Platform Module (TPM) 1.2 and 2.0
  — Subtractive agent for the Intel Legacy Block
- General Purpose Input Output
  — Control interface for SoC GPIOs
  — I/O mapped registers
- 8259 Programmable Interrupt Controller
  — Legacy interrupt support
  — 15 total interrupts through two cascaded controllers
  — I/O and Memory mapped registers
- I/O Advanced Programmable Interrupt Controller
  — Legacy-free interrupt support
  — 87 total interrupts
  — Memory mapped registers
- 8254
  — Legacy timer support
  — Three timers with fixed uses: System Timer, Refresh Request Signal and Speaker Tone
  — I/O mapped registers
- HPET - High Performance Event Timers
  — Legacy-free timer support

  - Three timers and one counter
  - Memory mapped registers
- Real-Time Clock (RTC)
  - 242 byte RAM backed by battery (aka CMOS RAM)
  - Can generate wake/interrupt when time matches programmed value
  - I/O and indexed registers

34.2.2 Non-Maskable Interrupt

NMI support is enabled by setting the NMI Enable (NMI_EN) bit, at IO Port 70h, Bit 7, to 0b.

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in Table 320.

Table 320. NMI Sources

NMI Source	NMI Source Enabler/ Disabler	NMI Source Status	Alternate Configuration
SERR# goes active **NOTE:** A SERR# is only generated internally in the SoC)	NSC.SNE	NSC.SNS	All NMI sources may, alternatively, generate a SMI by setting GNMI.NMI2SMIEN=1b The SoC uses GNMI.NMI2SMIST for observing SMI status
IOCHK# goes active **NOTE:** A IOCHK# is only generated as a SERIRQ# frame	NSC.INE	NSC.INS	
ILB_NMI goes active **NOTE:** Active can be defined as being on the positive or negative edge of the signal using the GNMI.GNMIED register bit.	GNMI.GNMIED	GNMI.GNMIS	
Software sets the GNMI.NMIN register bit	GNMI.NMIN	GNMI.NMINS	

§

34.3 PCU iLB Interrupt Decode and Route

Table 321. Summary of PCU iLB Interrupt Decode and Route Memory Mapped I/O Registers—ILB_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	“ACTL—Offset 0h” on page 4494	00000003h
4h	4	“MC—Offset 4h” on page 4495	00000000h
8h	1	“PIRQA—Offset 8h” on page 4495	80h
9h	1	“PIRQB—Offset 9h” on page 4496	80h
Ah	1	“PIRQC—Offset Ah” on page 4497	80h
Bh	1	“PIRQD—Offset Bh” on page 4497	80h
Ch	1	“PIRQE—Offset Ch” on page 4498	80h
Dh	1	“PIRQF—Offset Dh” on page 4498	80h
Eh	1	“PIRQG—Offset Eh” on page 4499	80h
Fh	1	“PIRQH—Offset Fh” on page 4499	80h
10h	4	“SCNT—Offset 10h” on page 4500	00000000h
14h	4	“KMC—Offset 14h” on page 4501	00000000h
18h	4	“FS—Offset 18h” on page 4502	00112233h
1Ch	4	“BC—Offset 1Ch” on page 4502	00000100h
20h	2	“IR0—Offset 20h” on page 4503	0000h
22h	2	“IR1—Offset 22h” on page 4504	0000h
24h	2	“IR2—Offset 24h” on page 4504	0000h
26h	2	“IR3—Offset 26h” on page 4505	0000h
28h	2	“IR4—Offset 28h” on page 4505	0000h
2Ah	2	“IR5—Offset 2Ah” on page 4506	0000h
2Ch	2	“IR6—Offset 2Ch” on page 4506	0000h
2Eh	2	“IR7—Offset 2Eh” on page 4507	0000h
30h	2	“IR8—Offset 30h” on page 4508	0000h
32h	2	“IR9—Offset 32h” on page 4508	0000h
34h	2	“IR10—Offset 34h” on page 4509	0000h
36h	2	“IR11—Offset 36h” on page 4509	0000h
38h	2	“IR12—Offset 38h” on page 4510	0000h
3Ah	2	“IR13—Offset 3Ah” on page 4510	0000h
3Ch	2	“IR14—Offset 3Ch” on page 4511	0000h
3Eh	2	“IR15—Offset 3Eh” on page 4512	0000h
40h	2	“IR16—Offset 40h” on page 4512	0000h
42h	2	“IR17—Offset 42h” on page 4513	0000h
44h	2	“IR18—Offset 44h” on page 4513	0000h
46h	2	“IR19—Offset 46h” on page 4514	0000h
48h	2	“IR20—Offset 48h” on page 4514	0000h

Table 321. Summary of PCU iLB Interrupt Decode and Route Memory Mapped I/O Registers—ILB_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
4Ah	2	"IR21—Offset 4Ah" on page 4515	0000h
4Ch	2	"IR22—Offset 4Ch" on page 4516	0000h
4Eh	2	"IR23—Offset 4Eh" on page 4516	0000h
50h	2	"IR24—Offset 50h" on page 4517	0000h
52h	2	"IR25—Offset 52h" on page 4517	0000h
54h	2	"IR26—Offset 54h" on page 4518	0000h
56h	2	"IR27—Offset 56h" on page 4518	0000h
58h	2	"IR28—Offset 58h" on page 4519	0000h
5Ah	2	"IR29—Offset 5Ah" on page 4520	0000h
5Ch	2	"IR30—Offset 5Ch" on page 4520	0000h
5Eh	2	"IR31—Offset 5Eh" on page 4521	0000h
60h	4	"OIC—Offset 60h" on page 4522	00001100h
64h	4	"RC—Offset 64h" on page 4523	00000000h
6Ch	4	"BCS - BIOS Control Status (BCS)—Offset 6Ch" on page 4523	00000002h
70h	4	"LE—Offset 70h" on page 4524	00000003h
80h	4	"NMI (GNMI)—Offset 80h" on page 4524	00000004h
84h	4	"LPCC—Offset 84h" on page 4525	00000001h
88h	4	"IRQEN (IRQE)—Offset 88h" on page 4526	00000000h

34.3.1 ACTL—Offset 0h

ACPI Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ACTL: [ILB_BASE_ADDRESS] + 0h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000003h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
RSVD0																														SCIS	

Bit Range	Default & Access	Description
31:3	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
2:0	011b RW	**SCIS:** SCI IRQ Select (SCIS): Specifies on which IRQ SCI will rout to. If not using APIC, SCI must be routed to IRQ9-11 , and that interrupt is not sharable with SERIRQ, but is shareable with other interrupts. If using APIC, SCI can be mapped to IRQ20-23, and can be shared with other interrupts. When the interrupt is mapped to APIC interrupts 9, 10 or 11, APIC must be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, APIC must be programmed for active-low reception.

34.3.2 MC—Offset 4h

Miscellaneous Control

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

MC: [ILB_BASE_ADDRESS] + 4h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																												DRTC	D8259	D8254	AME

Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3	0b RW	**DRTC:** Disable RTC (DRTC): When set, decodes to the RTC will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.
2	0b RW	**D8259:** Disable 8259 (D8259): When set, decodes to the 8259 will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.
1	0b RW	**D8254:** Disable 8254 (D8254): When set, decodes to the 8254 will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.
0	0b RW	**AME:** Alt Access Mode is a mode that enables host reading some WO registers . 1. Read 8254 (legacy timers) indirect WO registers 2. Read 8259 (legacy interrupt controller) indirect WO registers 3. Read port 0x70 - port 0x70 includes the RTC memory address [6:0] and the NMI enable bit [7]

34.3.3 PIRQA—Offset 8h

PIRQA Routing Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

PIRQA: [ILB_BASE_ADDRESS] + 8h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

34.3.4 PIRQB—Offset 9h

PIRQB Routing Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

PIRQB: [ILB_BASE_ADDRESS] + 9h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

34.3.5 PIRQC—Offset Ah

PIRQC Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQC: [ILB_BASE_ADDRESS] + Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

34.3.6 PIRQD—Offset Bh

PIRQD Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQD: [ILB_BASE_ADDRESS] + Bh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

34.3.7 PIRQE—Offset Ch

PIRQE Routing Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

PIRQE: [ILB_BASE_ADDRESS] + Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

34.3.8 PIRQF—Offset Dh

PIRQF Routing Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

PIRQF: [ILB_BASE_ADDRESS] + Dh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

34.3.9 PIRQG—Offset Eh

PIRQG Routing Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

PIRQG: [ILB_BASE_ADDRESS] + Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

34.3.10 PIRQH—Offset Fh

PIRQH Routing Control

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

PIRQH: [ILB_BASE_ADDRESS] + Fh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

34.3.11 SCNT—Offset 10h

SCNT - Serial IRQ Control

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

SCNT: [ILB_BASE_ADDRESS] + 10h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																								MD	RSVD1						

Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0b RW	**MD:** Mode (MD): When set, the SERIRQ is in continuous mode. When cleared, SERIRQ is in quiet mode. This bit must be set to guarantee that the first action of SERIRQ is a start frame.
6:0	0b RO	**RSVD1:** Reserved

34.3.12 KMC—Offset 14h

USB Legacy Keyboard/Mouse Control

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

KMC: [ILB_BASE_ADDRESS] + 14h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h

Bits	31:12	11	10	9	8	7:4	3	2	1	0
Default	0000 0000 0000 0000 0000	0	0	0	0	0000	0	0	0	0
Field	RSVD0	TRAPBY64W	TRAPBY64R	TRAPBY60W	TRAPBY60R	RSVD1	R64WEN	R64REN	R60WEN	R60REN

Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW/1C	**TRAPBY64W:** TRAPBY64W - SMI Caused by Port 64 Write: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
10	0b RW/1C	**TRAPBY64R:** TRAPBY64R - SMI Caused by Port 64 Read: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0b RW/1C	**TRAPBY60W:** TRAPBY60W - SMI Caused by Port 60 Write: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
8	0b RW/1C	**TRAPBY60R:** TRAPBY60R - SMI Caused by Port 60 Read: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7:4	0b RO	**RSVD1:** Reserved
3	0b RW	**R64WEN:** R64WEN - SMI on Port 64 Writes Enable: When set, a 1 in bit 11 will cause an SMI event.
2	0b RW	**R64REN:** R64REN - SMI on Port 64 Reads Enable: When set, a 1 in bit 10 will cause an SMI event.
1	0b RW	**R60WEN:** R60WEN - SMI on Port 60 Writes Enable: When set, a 1 in bit 9 will cause an SMI event.
0	0b RW	**R60REN:** R60REN - SMI on Port 60 Reads Enable: When set, a 1 in bit 8 will cause an SMI event.

34.3.13 FS—Offset 18h

FS - FWH ID Select

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

FS: [ILB_BASE_ADDRESS] + 18h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00112233h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	0	1	1	0	0	1	1
IF8				IF0				IE8				IE0				ID8				ID0				IC8				IC0			

Bit Range	Default & Access	Description
31:28	0h RO	**IF8:** F8-FF IDSEL (IF8): IDSEL to use in FWH cycle for range enabled by BDE.EF8. The Address ranges are: FFF80000h - FFFFFFFFh, FFB80000h - FFBFFFFFh and 000E0000h - 000FFFFFh
27:24	0h RW	**IF0:** F0-F7 IDSEL (IF0): IDSEL to use in FWH cycle for range enabled by BDE.EF0. The Address ranges are: FFF00000h - FFF7FFFFh, FFB00000h - FFB7FFFFh
23:20	1h RW	**IE8:** E8-EF IDSEL (IE8): IDSEL to use in FWH cycle for range enabled by BDE.EE8. The Address ranges are: FFE80000h - FFEFFFFFh, FFA80000h - FFAFFFFFh
19:16	1h RW	**IE0:** E0-E7 IDSEL (IE0): IDSEL to use in FWH cycle for range enabled by BDE.EE0. The Address ranges are: FFE00000h - FFE7FFFFh, FFA00000h - FFA7FFFFh
15:12	2h RW	**ID8:** D8-DF IDSEL (ID8): IDSEL to use in FWH cycle for range enabled by BDE.ED8. The Address ranges are: FFD80000h - FFDFFFFFh, FF980000h - FF9FFFFFh
11:8	2h RW	**ID0:** D0-D7 IDSEL (ID0): IDSEL to use in FWH cycle for range enabled by BDE.ED0. The Address ranges are: FFD00000h - FFD7FFFFh, FF900000h - FF97FFFFh
7:4	3h RW	**IC8:** C8-CF IDSEL (IC8): IDSEL to use in FWH cycle for range enabled by BDE.EC8. The Address ranges are: FFC80000h - FFCFFFFFh, FF880000h - FF8FFFFFh
3:0	3h RW	**IC0:** C0-C7 IDSEL (IC0): IDSEL to use in FWH cycle for range enabled by BDE.EC0. The Address ranges are: FFC00000h - FFC7FFFFh, FF800000h - FF87FFFFh

34.3.14 BC—Offset 1Ch

BC - BIOS Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BC: [ILB_BASE_ADDRESS] + 1Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits 31:9	Bit 8	Bits 7:2	Bit 1	Bit 0
RSVD0	PFE	RSVD1	LE	WP

Bit Range	Default & Access	Description
31:9	0b RO	**RSVD0:** Reserved
8	1b RW	**PFE:** Prefetch Enable (PFE): When set, BIOS prefetching is enabled. An access to BIOS causes a 64-byte fetch of the line starting at that region. Subsequent accesses within that region result in data being returned from the prefetch buffer. The prefetch buffer is invalidated when this bit is cleared, or a BIOS access occurs to a different line than what is currently in the buffer.
7:2	0b RO	**RSVD1:** Reserved
1	0b RW	**LE:** Lock Enable (LE): When set, setting the WP bit will cause SMIs. When cleared, setting the WP bit will not cause SMIs. Once set, this bit can only be cleared by a PMU_PLTRST_B#.
0	0b RW	**WP:** Write Protect (WP): When set, access to BIOS is enabled for both read and write cycles. When cleared, only read cycles are permitted to BIOS. When written from a 0 to a 1 and LE is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

34.3.15 IR0—Offset 20h

IR0 - Interrupt Routing Device 0

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR0: [ILB_BASE_ADDRESS] + 20h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:12	Bits 11:8	Bits 7:4	Bits 3:0
IRD	IRC	IRB	IRA

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.16 IR1—Offset 22h

IR1 - Interrupt Routing Device 1

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR1: [ILB_BASE_ADDRESS] + 22h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.17 IR2—Offset 24h

IR2 - Interrupt Routing Device 2

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR2: [ILB_BASE_ADDRESS] + 24h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.18 IR3—Offset 26h

IR3 - Interrupt Routing Device 3

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR3: [ILB_BASE_ADDRESS] + 26h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.19 IR4—Offset 28h

IR4 - Interrupt Routing Device 4

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR4: [ILB_BASE_ADDRESS] + 28h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.20 IR5—Offset 2Ah

IR5 - Interrupt Routing Device 5

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR5: [ILB_BASE_ADDRESS] + 2Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.21 IR6—Offset 2Ch

IR6 - Interrupt Routing Device 6

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR6: [ILB_BASE_ADDRESS] + 2Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.22 IR7—Offset 2Eh

IR7 - Interrupt Routing Device 7

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR7: [ILB_BASE_ADDRESS] + 2Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.23 IR8—Offset 30h

IR8 - Interrupt Routing Device 8

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR8: [ILB_BASE_ADDRESS] + 30h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.24 IR9—Offset 32h

IR9 - Interrupt Routing Device 9

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR9: [ILB_BASE_ADDRESS] + 32h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.25 IR10—Offset 34h

IR10 - Interrupt Routing Device 10

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR10: [ILB_BASE_ADDRESS] + 34h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.26 IR11—Offset 36h

IR11 - Interrupt Routing Device 11

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR11: [ILB_BASE_ADDRESS] + 36h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.27 IR12—Offset 38h

IR12 - Interrupt Routing Device 12

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR12: [ILB_BASE_ADDRESS] + 38h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.28 IR13—Offset 3Ah

IR13 - Interrupt Routing Device 13

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR13: [ILB_BASE_ADDRESS] + 3Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.29 IR14—Offset 3Ch

IR14 - Interrupt Routing Device 14

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR14: [ILB_BASE_ADDRESS] + 3Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.30 IR15—Offset 3Eh

IR15 - Interrupt Routing Device 15

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR15: [ILB_BASE_ADDRESS] + 3Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.31 IR16—Offset 40h

IR16 - Interrupt Routing Device 16

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR16: [ILB_BASE_ADDRESS] + 40h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.32 IR17—Offset 42h

IR17 - Interrupt Routing Device 17

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR17: [ILB_BASE_ADDRESS] + 42h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.33 IR18—Offset 44h

IR18 - Interrupt Routing Device 18

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR18: [ILB_BASE_ADDRESS] + 44h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.34 IR19—Offset 46h

IR19 - Interrupt Routing Device 19

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR19: [ILB_BASE_ADDRESS] + 46h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.35 IR20—Offset 48h

IR20 - Interrupt Routing Device 20

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR20: [ILB_BASE_ADDRESS] + 48h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.36 IR21—Offset 4Ah

IR21 - Interrupt Routing Device 21

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR21: [ILB_BASE_ADDRESS] + 4Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.37 IR22—Offset 4Ch

IR22 - Interrupt Routing Device 22

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR22: [ILB_BASE_ADDRESS] + 4Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.38 IR23—Offset 4Eh

IR23 - Interrupt Routing Device 23

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR23: [ILB_BASE_ADDRESS] + 4Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.39 IR24—Offset 50h

IR24 - Interrupt Routing Device 24

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR24: [ILB_BASE_ADDRESS] + 50h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.40 IR25—Offset 52h

IR25 - Interrupt Routing Device 25

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR25: [ILB_BASE_ADDRESS] + 52h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.41 IR26—Offset 54h

IR26 - Interrupt Routing Device 26

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR26: [ILB_BASE_ADDRESS] + 54h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.42 IR27—Offset 56h

IR27 - Interrupt Routing Device 27

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR27: [ILB_BASE_ADDRESS] + 56h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.43 IR28—Offset 58h

IR28 - Interrupt Routing Device 28

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR28: [ILB_BASE_ADDRESS] + 58h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.44 IR29—Offset 5Ah

IR29 - Interrupt Routing Device 29

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR29: [ILB_BASE_ADDRESS] + 5Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.45 IR30—Offset 5Ch

IR30 - Interrupt Routing Device 30

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR30: [ILB_BASE_ADDRESS] + 5Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.46 IR31—Offset 5Eh

IR31 - Interrupt Routing Device 31

Access Method

Type: Memory Mapped I/O Register
(Size: 16 bits)

IR31: [ILB_BASE_ADDRESS] + 5Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

34.3.47 OIC—Offset 60h

Other Interrupt Control

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

OIC: [ILB_BASE_ADDRESS] + 60h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00001100h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
RSVD0																			SIRQEN	RSVD1			AEN	RSVD2							

Bit Range	Default & Access	Description
31:13	0b RO	**RSVD0:** Reserved
12	1b RW	**SIRQEN:** When set, enables the internal SIRQ . when cleared the internal sIRQ is disabled
11:9	0b RO	**RSVD1:** Reserved
8	1b RW	**AEN:** When set, enables the internal IOAPIC and its address decode, when cleared the internal IOxAPIC is disabled. software should read this register after modifying the APIC enable prior to acces to IOxAPIC addresss range.
7:0	0b RO	**RSVD2:** Reserved

34.3.48 RC—Offset 64h

RC - RTC Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RC: [ILB_BASE_ADDRESS] + 64h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																														UL	LL

Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	0b RW/L	**UL:** Upper 128 Byte Lock (UL): When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked. Writes will be dropped and reads will not return any guaranteed data.
0	0b RW/L	**LL:** Lower 128 Byte Lock (LL): When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked. Writes will be dropped and reads will not return any guaranteed data.

34.3.49 BCS - BIOS Control Status (BCS)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

BCS: [ILB_BASE_ADDRESS] + 6Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD0																														SMIWPEN	SMIWPST

Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	1b RW	**SMIWPEN:** SMI WP Enable (SMIWPEN): When this bit is set to a 1, it enables the LPC to generate SMI upon not SMM code is trying to set BC.WP from a 0 to a 1 while BC.LE is set.

Bit Range	Default & Access	Description
0	0b RW/1C	**SMIWPST:** SMI WP Status (SMIWPST): Set when SMI is generated upon trying to set BC.WP from a 0 to a 1 by not SMM code (while BC.LE and SMIWPEN are set). Write a 1 to this bit should clear it and clear the SMI (send DEASSERT_SMI)

34.3.50 LE—Offset 70h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LE: [ILB_BASE_ADDRESS] + 70h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000003h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
RSVD0																														IRQ12C	IRQ1C

Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	1b RW	**IRQ12_CAUSE (IRQ12C):** When software sets the bit to 1, IRQ12 will be high (asserted), When software set bit to 0,IRQ12 will be low (deasserted). default for this bit is 1
0	1b RW	**IRQ1_CAUSE (IRQ1C):** When software sets the bit to 1, IRQ11 will be high (asserted), When software set bit to 0,IRQ1 will be low (deasserted). default for this bit is 1

34.3.51 NMI (GNMI)—Offset 80h

NMI register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GNMI: [ILB_BASE_ADDRESS] + 80h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RSVD0																									NMI2SMIEN	NMI2SMIST	NMIN	NMINS	GNMIED	GNMIE	GNMIS

Bit Range	Default & Access	Description
31:7	0b RO	**RSVD0:** Reserved
6	0b RW	**NMI2SMIEN:** NMI to SMI Enable (NMI2SMIEN): When set, instead of NMI messgae SMI message will be sent.
5	0b RO	**NMI2SMIST:** NMI to SMI bit Status (NMI2SMIST)
4	0b RW/1C	**NMIN:** NMI NOW (NMIN): When set, NMI messgae will be sent. Writing 1'b1 to NMI_NOW inverts NMI_MOW and NMI_NOW_STS value
3	0b RO	**NMINS:** NMI_NOW_STS is a result of the NMI_NOW configuration bit. Writing 1'b1 to NMI_NOW inverts NMI_NOW_STS value. Resulting that the first time NMI_NOW is written sets the NMI_NOW_STS and initiates NMI. Next writing clears the NMI_NOW_STS and allows initiating NMI by the next writing to NMI_NOW
2	1b RW	**GNMIED:** GPIO NMI Edge Detction (GNMIED): When set, NMI messgae will be sent on NMI GPIO posedge. when cleared the NMI message will be sent on negedge
1	0b RW	**GNMIE:** GPIO NMI Enable (GNMIE): When set, NMI messgae will be sent when NMI GPIO occured. when cleared the message will not be sent
0	0b RW/1C	**GNMS (GNMIS):** GPIO NMI Status (GNMIS), when NMI is recieved from GPIO this bit is set. write '1' to this register to clear the status bit

34.3.52 LPCC—Offset 84h

LPC Control register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

LPCC: [ILB_BASE_ADDRESS] + 84h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000001h

Bits	31:9	8	7:4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0 0	0	0	0	1
Field	RSVD0	LPCCLK_SLC	RSVD1	LPCCLK_force_off	CLKRUN_EN	LPCCLK1EN	LPCCLK0EN

Bit Range	Default & Access	Description
31:9	0b RO	**RSVD0:** Reserved
8	0b RO	**LPCCLK_SLC:** iLPCCLK mux select (0 - ilpcclk0, 1 ilpcclk1)This bit get value from soft strap.
7:4	0b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Description
3	0b RW	**LPCCLK_force_off:** when asserted,oLPCCLK shut off similarly to CLKRUN protocol while ignoring iCLKRUN (LPC device reactions)
2	0b RW	**CLKRUN_EN:** LPC CLKRUN protocol enable (when not asserted, oLPCCLK toggles)
1	0b RO	**LPCCLK1EN:** Clock 1 Enable (EN): This bit get value from soft strap. When set, LPC clock 1 is enabled. When cleared, it is disabled.
0	1b RO	**LPCCLK0EN:** Clock 0 Enable (EN): When set, LPC clock 0 is enabled. When cleared, it is disabled.

34.3.53 IRQEN (IRQE)—Offset 88h

IRQ Enable Control

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

IRQE: [ILB_BASE_ADDRESS] + 88h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

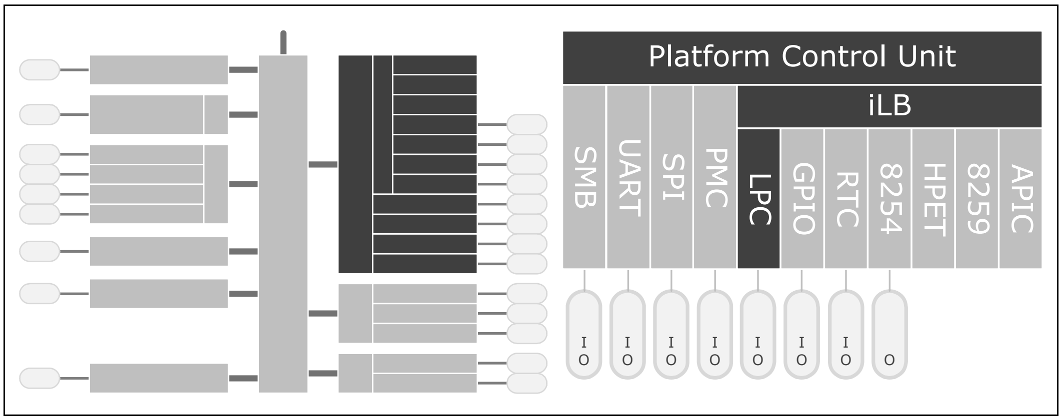
RSVD0 | UARTIRQEN | RSVD1

Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4	0b RO	**UARTIRQEN:** UART IRQ4 Enable
3:0	0b RO	**RSVD1:** Reserved

35 PCU – iLB – Low Pin Count (LPC) Bridge

The SoC implements an LPC Interface as described in the LPC 1.1 Specification. The Low Pin Count (LPC) bridge function of the SoC resides in PCI Device 31, Function 0.

Note: In addition to the LPC bridge interface function, D31:F0 contains other functional units including interrupt controllers, timers, power management, system management, GPIO, and RTC.



35.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction:** The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description:** A brief explanation of the signal's function

Note: If the VGA interfaces is used, VLPC must have a nominal voltage of 3.3V.

Table 322. LPC Signals

Signal Name	Direction Plat. Power	Description
ILB_LPC_AD[3:0]	I/O VLPC	**LPC Multiplexed Command, Address, Data:** Internal pull-ups are provided for these signals. *These signals are muxed and may be used by other functions.*
ILB_LPC_CLK[0]	O VLPC	**LPC Clock [0] Out:** 33 MHz PCI-like clock driven to LPC peripherals. *These signals are muxed and may be used by other functions.*
ILB_LPC_CLK[1]	O or I VLPC	**LPC Clock [1] Out:** 33 MHz PCI-like clock driven to LPC peripherals. Can be configured as an input to compensate for board routing delays through Soft Strap. *These signals are muxed and may be used by other functions.*
ILB_LPC_CLKRUN#	I/OD VLPC	**LPC Clock Run:** Input to determine the status of ILB_LPC_CLK and an open drain output used to request starting or speeding up ILB_LPC_CLK. This is a sustained tri-state signal used by the central resource to request permission to stop or slow ILB_LPC_CLK. The central resource is responsible for maintaining the signal in the asserted state when ILB_LPC_CLK is running and deasserts the signal to request permission to stop or slow ILB_LPC_CLK. An internal pull-up is provided for this signal. *This signal is muxed and may be used by other functions.*
ILB_LPC_FRAME#	O VLPC	**LPC Frame:** This signal indicates the start of an LPC cycle, or an abort. *This signal is muxed and may be used by other functions.*
ILB_LPC_SERIRQ	I/O V1P8S	**Serial Interrupt Request:** This signal implements the serial interrupt protocol. *This signal is muxed and may be used by other functions.*

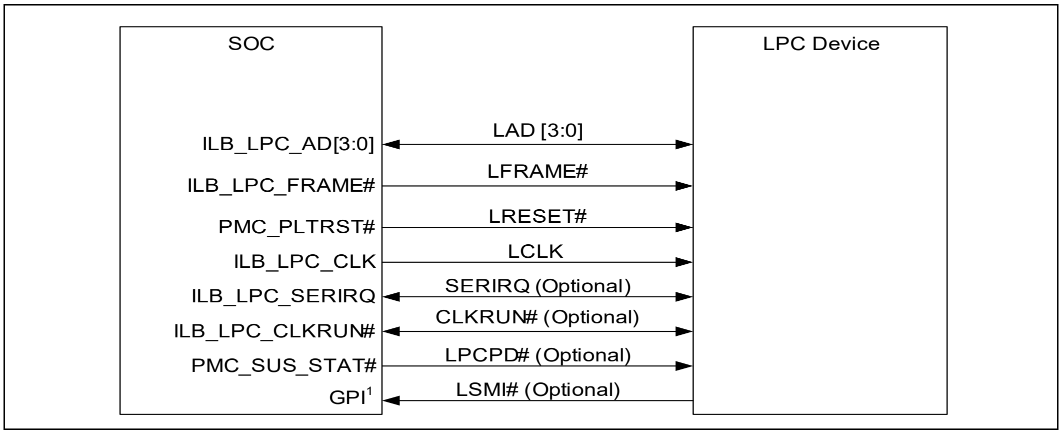
35.2 Features

The LPC interface to the SoC is shown in Figure 135. Note that the SoC implements all of the signals that are shown as optional, but peripherals are not required to do so.

Note: The LPC controller does not implement bus mastering cycles or DMA.

Note: The LPC controller is the subtractive agent of the Intel Legacy Block. All transactions not claimed elsewhere are sent to the LPC controller.

Figure 135.LPC Interface Diagram



NOTES:

1. The General Purpose Input (GPI) must use a SMI capable GPIO: GPIO_S0_SC[7:0].

35.2.1 Memory Cycle Notes

For cycles below 16M, the LPC Controller will perform standard LPC memory cycles. For cycles targeting firmware (BIOS/EFI code only), firmware memory cycles are used. Only 8-bit transfers are performed. If a larger transfer appears, the LPC controller will break it into multiple 8-bit transfers until the request is satisfied.

If the cycle is not claimed by any peripheral (and subsequently aborted), the LPC Controller will return a value of all 1's to the CPU.

35.2.2 Trusted Platform Module (TPM) 1.2 Support

The LPC interface supports accessing Trusted Platform Module (TPM) 1.2 and 2.0 devices via the LPC TPM START encoding. Memory addresses within the range FED40000h to FED40FFFh will be accepted by the LPC Bridge and sent on LPC as TPM special cycles. No additional checking of the memory cycle is performed.

Note: This is different to the FED00000h to FED4BFFFh range implemented on some other Intel components since no Intel® Trusted Execution Technology (Intel® TXT) transactions are supported.

35.2.3 FWH Cycle Notes

If the LPC controller receives any SYNC returned from the device other than short (0101), long wait (0110), or ready (0000) when running a FWH cycle, indeterminate results may occur. A FWH device is not allowed to assert an Error SYNC.

BIOS/EFI boot from LPC is not supported when Secure Boot is enabled.

35.2.4 Other Notes

All cycles that are not decoded internally, and are not targeted for LPC (i.e. configuration cycles and IO cycles above 64kb) will be sent to LPC with ILB_LPC_FRAME# not asserted. Memory cycles above 16 MB that are not decoded internally, and are not targeted for LPC will be sent to LPC with ILB_LPC_FRAME# asserted.

35.2.5 POST Code Redirection

Writes to addresses 80h - 8Fh in IO register space will also be passed to the LPC bus.

Note: Reads of these addresses do not result in any LPC transactions.

35.2.6 Power Management

35.2.6.1 LPCPD# Protocol

Same timings as for PMC_SUS_STAT#. After driving PMC_SUS_STAT# active, the SoC drives ILB_LPC_FRAME# low, and tri-states (or drives low) ILB_LPC_AD[3:0].

Note: The Low Pin Count Interface Specification, Revision 1.1 defines the LPCPD# protocol where there is at least 30 µs from LPCPD# assertion to LRST# assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states which does not include asynchronous reset events. The SoC asserts both PMC_SUS_STAT# (connects to LPCPD#) and ILB_PLTRST# (connects to LRST#) at the same time during a global reset. This is not inconsistent with the LPC LPCPD# protocol.

35.2.6.2 Clock Run (CLKRUN)

When there are no pending LPC cycles, and SERIRQ is in quiet mode, the SoC can shut down the LPC clock. The SoC indicates that the LPC clock is going to shut down by de-asserting the ILB_LPC_CLKRUN# signal. LPC devices that require the clock to stay running should drive ILB_LPC_CLKRUN# low within 4 clocks of its de-assertion. If no device drives the signal low within 4 clocks, the LPC clock will stop. If a device asserts ILB_LPC_CLKRUN#, the SoC will start the LPC clock and assert ILB_LPC_CLKRUN#.

Note: The CLKRUN protocol is disabled by default. See Section 35.3.2.2, "Clock Run Enable" on page 4534 for further details.

35.2.7 Serialized IRQ (SERIRQ)

35.2.7.1 Overview

The interrupt controller supports a serial IRQ scheme. The signal used to transmit this information is shared between the interrupt controller and all peripherals that support serial interrupts. The signal line, ILB_LPC_SERIRQ, is synchronous to LPC clock, and follows the sustained tri-state protocol that is used by LPC signals. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S - Sample Phase:** Signal driven low
- **R - Recovery Phase:** Signal driven high
- **T - Turn-around Phase:** Signal released

The interrupt controller supports 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0- 1, 3-15), the four PCI interrupts, and the control signals SMI# and IOCHK#. Serial interrupt information is transferred using three types of frames:

- Start Frame: ILB_LPC_SERIRQ line driven low by the interrupt controller to indicate the start of IRQ transmission
- Data Frames: IRQ information transmitted by peripherals. The interrupt controller supports 21 data frames.
- Stop Frame: ILB_LPC_SERIRQ line driven low by the interrupt controller to indicate end of transmission and next mode of operation.

35.2.7.2 Start Frame

The serial IRQ protocol has two modes of operation which affect the start frame:

- Continuous Mode: The interrupt controller is solely responsible for generating the start frame
- Quiet Mode: Peripheral initiates the start frame, and the interrupt controller completes it.

These modes are entered via the length of the stop frame.

Continuous mode must be entered first, to start the first frame. This start frame width is 8 LPC clocks. This is a polling mode.

In Quiet mode, the ILB_LPC_SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives ILB_LPC_SERIRQ low. The interrupt controller senses the line low and drives it low for the remainder of the Start Frame. Since the first LPC clock of the start frame was driven by the peripheral, the interrupt controller drives ILB_LPC_SERIRQ low for 1 LPC clock less than in continuous mode. This mode of operation allows for lower power operation.

35.2.7.3 Data Frames

Once the Start frame has been initiated, the ILB_LPC_SERIRQ peripherals start counting frames based on the rising edge of ILB_LPC_SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- **Sample Phase:** During this phase, a device drives ILB_LPC_SERIRQ low if its corresponding interrupt signal is low. If its corresponding interrupt is high, then the ILB_LPC_SERIRQ devices tri-state ILB_LPC_SERIRQ. ILB_LPC_SERIRQ remains high due to pull-up resistors.
- **Recovery Phase:** During this phase, a device drives ILB_LPC_SERIRQ high if it was driven low during the Sample Phase. If it was not driven during the sample phase, it remains tri-stated in this phase.
- **Turn-around Phase:** The device tri-states ILB_LPC_SERIRQ.

35.2.7.4 Stop Frame

After the data frames, a Stop Frame will be driven by the interrupt controller. ILB_LPC_SERIRQ will be driven low for two or three LPC clocks. The number of clocks is determined by the SCNT.MD register bit. The number of clocks determines the next mode, as indicated in Table 323.

Table 323. SERIRQ, Stop Frame Width to Operation Mode Mapping

Stop Frame Width	Next Mode
Two LPC clocks	**Quiet Mode:** Any SERIRQ device initiates a Start Frame
Three LPC clocks	**Continuous Mode:** Only the interrupt controller initiates a Start Frame

35.2.7.5 Serial Interrupts Not Supported

There are four interrupts on the serial stream which are not supported by the interrupt controller. These interrupts are:

- IRQ0: Heartbeat interrupt generated off of the internal 8254 counter 0.
- IRQ8: RTC interrupt can only be generated internally.
- IRQ13: This interrupt (floating point error) is not supported.
- IRQ14: Interrupt can only be generated by the SATA controller in Legacy mode.

The interrupt controller will ignore the state of these interrupts in the stream.

35.2.7.6 Data Frame Format and Issues

Table below shows the format of the data frames. The decoded INT[A:D]# values are ANDed with the corresponding PCI-express input signals (PIRQ[A:D]#). This way, the interrupt can be shared.

The other interrupts decoded via SERIRQ are also ANDed with the corresponding internal interrupts. For example, if IRQ10 is set to be used as the SCI, then it is ANDed with the decoded value for IRQ10 from the SERIRQ stream.

Table 324. SERIRQ Interrupt Mapping

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. Can only be generated via the internal 8524
2	IRQ1	5	Before port 60h latch
3	SMI#	8	Causes SMI# if low. Sets SMI_STS.ILB_SMI_STS register bit.
4	IRQ3	11	
5	IRQ4	14	
6	IRQ5	17	
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can only be generated internally
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	Before port 60h latch
14	IRQ13	41	Ignored
15	IRQ14	44	Ignored
16	IRQ15	47	
17	IOCHCK#	50	Same as ISA IOCHCK# going active.
18	PCI INTA#	53	
19	PCI INTB#	56	
20	PCI INTC#	59	
21	PCI INTD#	62	

35.3 Use

35.3.1 LPC Clock Delay Compensation

In order to meet LPC interface AC timing requirements, a LPC clock loop back is required. The operation of this loop back can be configured in two ways:

1. On the SOC: In this configuration, ILB_LPC_CLK[0] is looped back on itself on the SOC pad.

    a. Benefit:

    ILB_LPC_CLK[0] and ILB_LPC_CLK[1] are both available for system clocking

b. Drawback:

Clock delay compensation is less effective at compensating for mainboard delay

c. Soft Strap & Register Requirements:

Soft Strap LPCCLK_SLC = 0b

Configuration is reflected by register bit LPCC.LPCCLK_SLC=0b

Soft Strap LPCCLK1_ENB = 0b (ILB_LPC_CLK[1] disabled) or 1b (ILB_LPC_CLK[1] enabled)

2. Configuration is reflected by register bit LPCC.LPCCLK1EN=0b (ILB_LPC_CLK[1] disabled) or 1b (ILB_LPC_CLK[1] enabled)
3. On the main board: In this configuration, ILB_LPC_CLK[0] is looped back to ILB_LPC_CLK[1] on the main board.

a. Benefit:

Clock delay compensation in more effective at compensating for main board delay

b. Drawback:

Only ILB_LPC_CLK[0] is available for system clocking. ILB_LPC_CLK[1] must be disabled.

c. Soft Strap & Register Requirements:

Soft Strap LPCCLK_SLC = 1b

Configuration is reflected by register bit LPCC.LPCCLK_SLC=1b

Soft Strap LPCCLK1_ENB = 0b (ILB_LPC_CLK[1] disabled)

Configuration is reflected by register bit LPCC.LPCCLK1EN=0b

35.3.2 LPC Power Management

35.3.2.1 Clock Enabling

The LPC clocks can be enabled or disabled by setting or clearing, respectively, the LPCC.LPCCLK[1:0]EN bits.

35.3.2.2 Clock Run Enable

The Clock Run protocol is disabled by default and should only be enabled once all LPC devices have been initialized. The Clock Run protocol is enabled by setting the LPCC.CLKRUN_EN register bit.

35.3.3 SERIRQ Disable

Serialized IRQ support may be disabled by setting the OIC.SIRQEN bit to 0b.

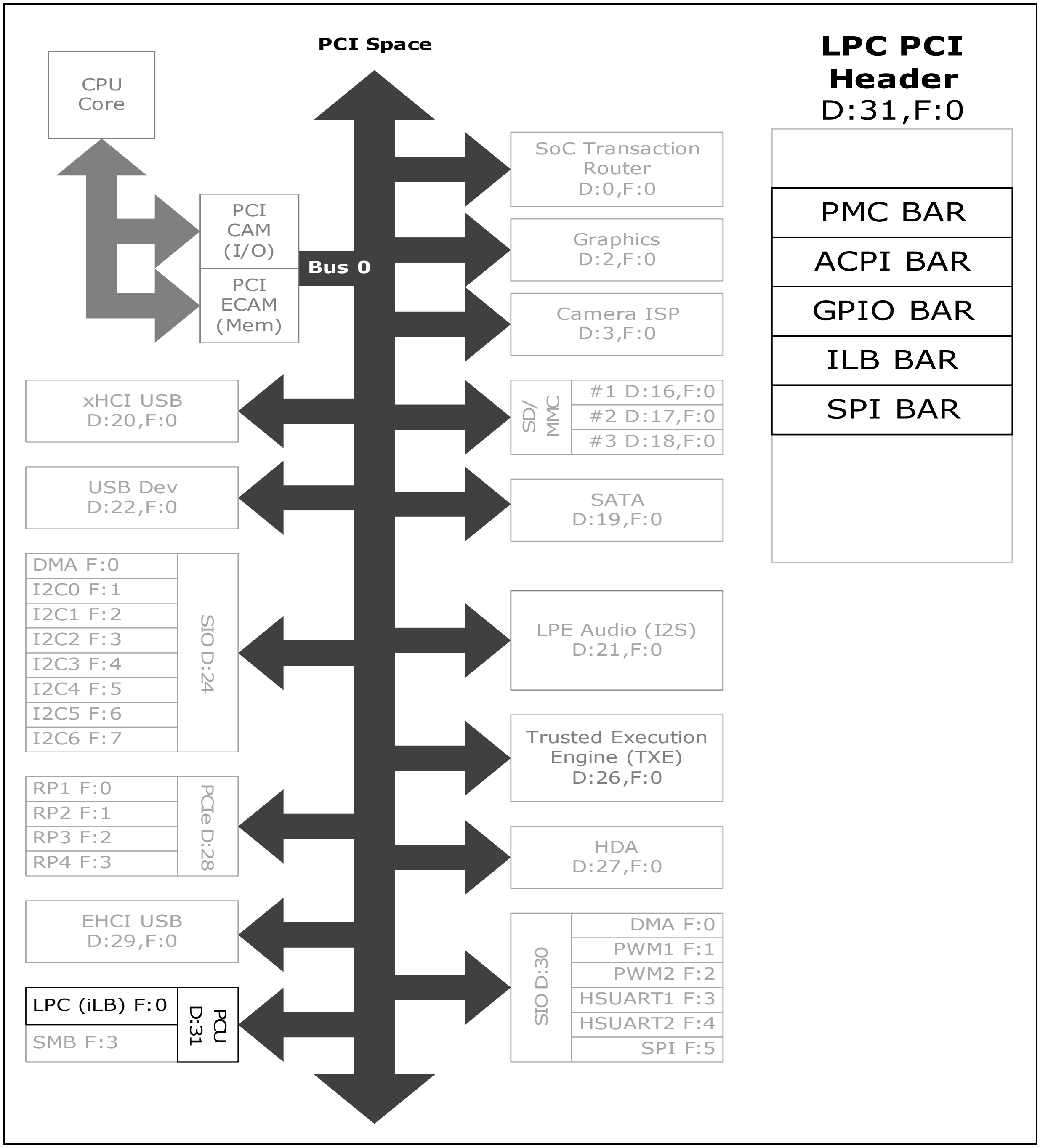
35.4 References

- Low Pin Count Interface Specification, Revision 1.1 (LPC): http://www.intel.com/design/chipsets/industry/lpc.htm
- Serialized IRQ Support for PCI Systems, Revision 6.0: http://www.smsc.com/media/Downloads_Public/papers/serirq60.doc
- Implementing Industry Standard Architecture (ISA) with Intel® Express Chipsets (318244): http://www.intel.com/assets/pdf/whitepaper/318244.pdf

35.5 Register Map

Refer to Chapter 3, “Register Access Methods” and Chapter 4, “Mapping Address Spaces” for additional information.

Figure 136.PCU - iLB - LPC Register Map



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35.6 PCU iLB Low Pin Count (LPC) Bridge PCI Configuration Registers

Table 325. Summary of PCU iLB Low Pin Count (LPC) Bridge PCI Configuration Registers—0/31/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Identifiers Register (PCIE_REG_Identifiers)—Offset 0h" on page 4538	00008086h
4h	2	"Command (PCIE_REG_COMMAND)—Offset 4h" on page 4538	0007h
6h	2	"Status (PCIE_REG_STATUS)—Offset 6h" on page 4539	0210h
8h	4	"Revision ID and Class Code (PCIE_REG_REVISION_ID_CLASS_CODE)—Offset 8h" on page 4540	06010000h
Dh	1	"Master Latency Timer (PCIE_REG_MASTER_LAT_TIMER)—Offset Dh" on page 4541	00h
Eh	1	"Header Type (PCIE_REG_HEADER_TYPE)—Offset Eh" on page 4541	80h
2Ch	4	"Subsystem ID and Vendor ID (PCIE_REG_SUBSYS_VENDOR_ID)—Offset 2Ch" on page 4542	00000000h
34h	4	"Capability List Pointer (PCIE_REG_CAP_POINTER)—Offset 34h" on page 4543	000000E0h
40h	4	"ABASE (ACPI_BASE_ADDRESS)—Offset 40h" on page 4543	00000001h
44h	4	"PBASE (PMC_BASE_ADDRESS)—Offset 44h" on page 4544	00000000h
48h	4	"GBASE (GPIO_BASE_ADDRESS)—Offset 48h" on page 4544	00000001h
4Ch	4	"IOBASE (IO_CONTROLLER_BASE_ADDRESS)—Offset 4Ch" on page 4545	00000000h
50h	4	"IBASE (ILB_BASE_ADDRESS)—Offset 50h" on page 4546	00000000h
54h	4	"SBASE (SPI_BASE_ADDRESS)—Offset 54h" on page 4547	00000000h
58h	4	"MPBASE (MPHY_BASE_ADDRESS)—Offset 58h" on page 4547	00000000h
5Ch	4	"PUBASE (PUNIT_BASE_ADDRESS)—Offset 5Ch" on page 4548	00000000h
80h	4	"UART Control (UART_CONT)—Offset 80h" on page 4549	00000000h
D8h	2	"BIOS Decode Enable (PCIE_REG_BIOS_DECODE_EN)—Offset D8h" on page 4549	FFCFh
E0h	2	"FDCAP (Feature_Detection_Capability_ID)—Offset E0h" on page 4551	0009h
E2h	1	"FDLEN (Feature_Detection_Capability_Length)—Offset E2h" on page 4551	0Ch
E3h	1	"FDVER (Feature_Detection_Version_Register)—Offset E3h" on page 4552	10h
E4h	4	"FVECTIDX (Feature_Vector_Index)—Offset E4h" on page 4552	00000000h
E8h	4	"FVECTD (Feature_Vector_Data)—Offset E8h" on page 4553	00000000h
F0h	4	"RCBA (RCRB_BASE_ADDRESS)—Offset F0h" on page 4553	00000000h
F8h	4	"Manufacturer ID (PCIE_REG_MANUFACTURER_ID) - Offset F8h" on page 4553	01xx0F1A

35.6.1 Identifiers Register (PCIE_REG_Identifiers)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_Identifiers: [B:0, D:31, F:0] + 0h

Default: 00008086h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
DID																VID															

Bit Range	Default & Access	Description
31:16	X RO	**Device Identification (DID):** This field identifies the particular device. This identifier is allocated by the vendor. This field is controlled by the LPC DID fuses Bits [31:23] are coming from the SETIDVALUE message Device ID[15:7] bits. Bits [22:21] are set constantly to 2'b00. Bits [20:16] are set constantly by pcu_did fuses.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 0 FFFFh is an invalid value for Vendor ID.

35.6.2 Command (PCIE_REG_COMMAND)—Offset 4h

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not be implemented depending on a device's functionality

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_COMMAND: [B:0, D:31, F:0] + 4h

Default: 0007h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
RSVD0					ID	FBE	SEE	WCC	PERE	VGA_PSE	MWIE	SCE	BME	MSE	IOSE

Bit Range	Default & Access	Description
15:11	0b RO	**RSVD0:** Reserved
10	0b RO	**Interrupt Disable (ID):** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. The LPC bridge has no interrupts to disable
9	0b RO	**Fast Back to Back Enable (FBE):** This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. A value of 0 means fast back-to-back transactions are only allowed to the same agent
8	0b RW	**SERR# Enable (SEE):** This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver.

Bit Range	Default & Access	Description
7	0b RO	**Wait Cycle Control (WCC):** Reserved as '0' per PCI-Express spec
6	0b RW	**Parity Error Response Enable (PERE):** This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error status bit (bit 15 in the Status register) when an error is detected, but does not assert PERR# and continues normal operation.
5	0b RO	**VGA Palette Snoop (VGA_PSE):** This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. When this bit is 1, palette snooping is enabled (i.e., the device does not respond to palette register writes and snoops the data). When the bit is 0, the device should treat palette write accesses like all other accesses. Reserved as '0' per PCI-Express spec
4	0b RO	**Memory Write and Invalidate Enable (MWIE):** This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, masters may generate the command. When it is 0, Memory Write must be used instead. Reserved as '0' per PCI-Express spec
3	0b RO	**Special Cycle Enable (SCE):** Controls a device's action on Special Cycle operations. A value of 0 causes the device to ignore all Special Cycle operations. A value of 1 allows the device to monitor Special Cycle operations. Reserved as '0' per PCI-Express spec
2	1b RO	**Bus Master Enable (BME):** Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. Bus master cannot be disabled on LPC
1	1b RO	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. Memory space cannot be disable on LPC
0	1b RO	**I/O Space Enable (IOSE):** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. I/O space cannot be disable on LPC

35.6.3 Status (PCIE_REG_STATUS)—Offset 6h

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A one bit is reset (if it is not read-only) whenever the register is written, and the write data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_STATUS: [B:0, D:31, F:0] + 6h

Default: 0210h

15			12				8				4				0
0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DTS		DPD	FBC	RSVD0	C66	CLIST	IS	RSVD1		

Bit Range	Default & Access	Description
15	0b RW	**Detected Parity Error (DPE):** This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).

Bit Range	Default & Access	Description
14	0b RW	**Signaled System Error (SSE):** This bit must be set whenever the device asserts SERR#. Set when the LPC bridge signals a system error to the internal SERR# logic.
13	0b RW	**Received Master Abort (RMA):** This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
12	0b RW	**Received Target Abort: (RTA):** This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
11	0b RW	**Signaled Target Abort (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target- Abort do not need to implement this bit.
10:9	01b RO	**DEVSEL# Timing Status (DTS):** These bits encode the timing of DEVSEL#. These are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits Indicate medium timing, although this has no meaning on the backbone
8	0b RW	**Data Parity Error Detected (DPD):** This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command register) is set.
7	0b RO	**Fast Back to Back Capable (FBC):** This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. This bit has no meaning on internal backbone.
6	0b RO	**RSVD0:** Reserved
5	0b RO	**66 MHz Capable (C66):** This optional read-only bit indicates whether or not this device is capable of running at 66 MHz. A value of zero indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. This bit has no meaning on internal backbone
4	1b RO	**Capabilities List (CLIST):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities. There is a capabilities list in the LPC bridge.
3	0b RO	**Interrupt Status (IS):** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. The LPC bridge does not generate interrupts
2:0	0b RO	**RSVD1:** Reserved

35.6.4 Revision ID and Class Code (PCIE_REG_REVISION_ID_CLASS_CODE)—Offset 8h

This register is a combination of two registers the Revision ID register and the Class Code register. The revision ID register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. The Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific registerlevel programming interface.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_REVISION_ID_CLASS_CODE: [B:0, D:31, F:0] + 8h

Default: 06010000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BCC								SCC								PI								RIS							

Bit Range	Default & Access	Description
31:24	06h RO	**Base Class Code (BCC):** This field is a base class code which broadly classifies the type of function the device performs. Indicates the device is a bridge device.
23:16	01h RO	**Sub-Class Code (SCC):** This field is a sub-class code which identifies more specifically the function of the device. Indicates the device a PCI to ISA bridge
15:8	00h RO	**Programming Interface (PI):** This field identifies a specific register-level programming interface if any) so that device independent software can interact with the device. The LPC bridge has no programming interface.
7:0	X RO	**Revision ID (RIS):** This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the Device ID. This field is controlled by the LPC RID fuses. Coming from the SETIDVALUE message Revision ID field

35.6.5 Master Latency Timer (PCIE_REG_MASTER_LAT_TIMER)—Offset Dh

This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. This register is implemented as read-only, the register must be initialized to 0.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PCIE_REG_MASTER_LAT_TIMER: [B:0, D:31, F:0] + Dh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MLC					RSVD0		

Bit Range	Default & Access	Description
7:3	00h RO	**Master Latency Count (MLC):** Reserved per PCIe spec.
2:0	0b RO	**RSVD0:** Reserved

35.6.6 Header Type (PCIE_REG_HEADER_TYPE)—Offset Eh

This byte identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and also whether or not the device contains multiple functions.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PCIE_REG_HEADER_TYPE: [B:0, D:31, F:0] + Eh

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
MFD	HTYPE						

Bit Range	Default & Access	Description
7	1b RO	**Multi-function Device (MFD):** This field is used to identify a multi-function device. If the bit is 0, then the device is single function. If the bit is 1, then the device has multiple functions.
6:0	00h RO	**Header Type (HTYPE):** This field identifies the layout of the second part of the predefined header. The encoding 00h specifies the standard layout.

35.6.7 Subsystem ID and Vendor ID (PCIE_REG_SUBSYS_VENDOR_ID)—Offset 2Ch

This register is used to uniquely identify the add-in card or subsystem where the PCI device resides. It provides a mechanism for add-in card vendors to distinguish their add- in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID). Implementation of this register is required for all PCI devices except those that have a base class 6 with sub class 0-4 (0, 1, 2, 3, 4), or a base class 8 with sub class 0-3 (0, 1, 2, 3). Subsystem Vendor IDs can be obtained from the PCI SIG and are used to identify the vendor of the add-in card or subsystem. Values for the Subsystem ID are vendor specific. Values in these registers must be loaded and valid prior to the system firmware or any system software accessing the PCI Configuration Space. How these values are loaded is not specified but could be done during the manufacturing process or loaded from external logic (e.g., strapping options, serial ROMs, etc.). These values must not be loaded using expansion ROM software because expansion ROM software is not guaranteed to be run during POST in all systems. Devices are responsible for guaranteeing the data is valid before allowing reads to these registers to complete. This can be done by responding to any accesses with Retry until the data is valid. If a device is designed to be used exclusively on the system board, the system vendor may use system specific software to initialize these registers after each power-on. This register can be written only once after PMU_PLTRST_B de-assertion.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_SUBSYS_VENDOR_ID: [B:0, D:31, F:0] + 2Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
SSID				SSVID				

Bit Range	Default & Access	Description
31:16	0000h RW	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value. This field could be written only once.
15:0	0000h RW	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value. This field could be written only once.

35.6.8 Capability List Pointer (PCIE_REG_CAP_POINTER)—Offset 34h

This optional register is used to point to a linked list of new capabilities implemented by this device. This register is only valid if the Capabilities List bit in the Status Register is set. If implemented, the bottom two bits are reserved and should be set to 00b. Software should mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_CAP_POINTER: [B:0, D:31, F:0] + 34h

Default: 000000E0h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0
RSVD0																								CP							

Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	E0h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

35.6.9 ABASE (ACPI_BASE_ADDRESS)—Offset 40h

ACPI is mapped into I/O space. It is used by the PMC. Base Address registers that map into I/O Space are always 32 bits wide with bit 0 hardwired to a 1. Bit 1 is used to enable IO range pointed by this base address. Bits 31:16 are reserved and must return 0 on reads and the other bits could be used to map the device into I/O Space.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS: [B:0, D:31, F:0] + 40h

Default: 00000001h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
RSVD0																BA									RSVD1					EN	MEMI

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Base Address (BA):** Provides the 128 bytes of I/O space for ACPI and TCO logic
6:2	0b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Description
1	0b RW	**Enable (EN):** When set, decode of the IO range pointed to by the ABASE is enabled.
0	1b RO	**Memory Space Indication (MEMI):** This read-only bit always is 1, indicating that this BAR is IO mapped

35.6.10 PBASE (PMC_BASE_ADDRESS)—Offset 44h

PMC registers are mapped into memory space. It is used by the PMC. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS: [B:0, D:31, F:0] + 44h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:9	Bits 8:4	Bit 3	Bit 2	Bit 1	Bit 0
BA	RSVD0	PREF	ADDRNG	EN	MEMI

Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the PMC logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the PBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

35.6.11 GBASE (GPIO_BASE_ADDRESS)—Offset 48h

GPIO registers are mapped into I/O space. It is used by the Proxy agent (to IO controllers). Base Address registers that map into I/O Space are always 32 bits wide with bit 0 hardwired to a 1. Bit 1 is used to enable IO range pointed by this base address. Bits 31:16 are reserved and must return 0 on reads and the other bits could be used to map the device into I/O Space.

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

GPIO_BASE_ADDRESS: [B:0, D:31, F:0] + 48h

Default: 00000001h

31–16	15–8	7–2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0	1
RSVD0	BA	RSVD1	EN	MEMI

Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RW	**Base Address (BA):** Provides the 256 bytes of I/O space for GPIO logic
7:2	0b RO	**RSVD1:** Reserved
1	0b RW	**Enable (EN):** When set, decode of the IO range pointed to by the GBASE is enabled.
0	1b RO	**Memory Space Indication (MEMI):** This read-only bit always is 1, indicating that this BAR is IO mapped

35.6.12 IOBASE (IO_CONTROLLER_BASE_ADDRESS)—Offset 4Ch

IO Controllers registers are mapped into memory space. It is used by the Proxy agent (to IO controllers). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

IO_CONTROLLER_BASE_ADDRESS: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31–14	13–4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0	0	0	0
BA	RSVD0	PREF	ADDRNG	EN	MEMI

Bit Range	Default & Access	Description
31:14	00000h RW	**Base Address (BA):** Provides 8K byte system memory base address for the IO controllers logic
13:4	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the IOBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

35.6.13 IBASE (ILB_BASE_ADDRESS)—Offset 50h

iLB registers are mapped into memory space. It is used by the iLB. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register
(Size: 32 bits)

ILB_BASE_ADDRESS: [B:0, D:31, F:0] + 50h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BA																							RSVD0					PREF	ADDRNG	EN	MEMI

Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the iLB logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the IBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

35.6.14 SBASE (SPI_BASE_ADDRESS)—Offset 54h

SPI registers are mapped into memory space. It is used by the SPI. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**SPI_BASE_ADDRESS:** [B:0, D:31, F:0] + 54h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BA																							RSVD0					PREF	ADDRNG	EN	MEMI

Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the SPI logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the SBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

35.6.15 MPBASE (MPHY_BASE_ADDRESS)—Offset 58h

M-phys registers are mapped into memory space. It is used by the Proxy agent (to M-phys). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)	**MPHY_BASE_ADDRESS:** [B:0, D:31, F:0] + 58h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BA	RSVD0	PREF	ADDRNG	EN	MEMI

Bit Range	Default & Access	Description
31:20	000h RW	**Base Address (BA):** Provides 1M byte system memory base address for the M phys logic
19:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the MPBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

35.6.16 PUBASE (PUNIT_BASE_ADDRESS)—Offset 5Ch

P-Unit registers are mapped into memory space. It is used by the Proxy agent (to P-Unit). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PUNIT_BASE_ADDRESS: [B:0, D:31, F:0] + 5Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

BA	RSVD0	PREF	ADDRNG	EN	MEMI

Bit Range	Default & Access	Description
31:11	00000h RW	**Base Address (BA):** Provides 2K byte system memory base address for the P-Unit registers
10:4	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the PUBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

35.6.17 UART Control (UART_CONT)—Offset 80h

Controls the internal PCU UART ports

Access Method

Type: PCI Configuration Register (Size: 32 bits)

UART_CONT: [B:0, D:31, F:0] + 80h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0																															COM1EN

Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0b RW	**COM1 Enable (COM1EN):** When set, enables the internal PCU COM1 UART port.

35.6.18 BIOS Decode Enable (PCIE_REG_BIOS_DECODE_EN)—Offset D8h

This register enables ranges in the BIOS for decoding purposes. Note that this register affects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. PCU EP simply decodes these ranges as memory accesses when enabled for the SPI/LPC flash interface.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_BIOS_DECODE_EN: [B:0, D:31, F:0] + D8h

Default: FFCFh

15			12				8				4				0
1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
EF8	EF0	EE8	EE0	ED8	ED0	EC8	EC0	LFE	LEE	RSVD0		E70	E60	E50	E40

Bit Range	Default & Access	Description
15	1b RW	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFF80000 - 0xFFFFFFFF - Feature space: 0xFFB80000 - 0xFFBFFFFF
14	1b RW	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFF00000 - 0xFFF7FFFF - Feature space: 0xFFB00000 - 0xFFB7FFFF
13	1b RW	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFE80000 - 0xFFEFFFFF - Feature space: 0xFFA80000 - 0xFFAFFFFF
12	1b RW	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFE00000 - 0xFFE7FFFF - Feature space: 0xFFA00000 - 0xFFA7FFFF
11	1b RW	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFD80000 - 0xFFDFFFFF - Feature space: 0XFF980000 - 0xFF9FFFFF
10	1b RW	**D0-D8 Enable (ED0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFD00000 - 0xFFD7FFFF - Feature space: 0XFF900000 - 0xFF97FFFF
9	1b RW	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFC80000h - 0xFFCFFFFF - Feature space: 0xFF880000h - 0xFF8FFFFF
8	1b RW	**C0-C8 Enable (EC0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFC00000 - 0xFFC7FFFF - Feature space: 0xFF800000 - 0xFF87FFFF
7	1b RW	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at 0xF0000 - 0xFFFFF
6	1b RW	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at 0xE0000 - 0xEFFFF
5:4	0b RO	**RSVD0:** Reserved
3	1b RW	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF700000 - 0xFF7FFFFF - Feature space: 0xFF300000 - 0xFF3FFFFF
2	1b RW	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF600000 - 0xFF6FFFFF - Feature Space: 0xFF200000 - 0xFF2FFFFF
1	1b RW	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF500000 - 0xFF5FFFFF - Feature space: 0xFF100000 - 0xFF1FFFFF
0	1b RW	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF400000 - 0xFF4FFFFF - Feature Space: 0xFF000000 - 0xFF0FFFFF

35.6.19 FDCAP (Feature_Detection_Capability_ID)—Offset E0h

Feature detection capability ID.

Access Method

Type: PCI Configuration Register (Size: 16 bits)	**Feature_Detection_Capability_ID:** [B:0, D:31, F:0] + E0h

Default: 0009h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
NEXT								CAPID							

Bit Range	Default & Access	Description
15:8	00h RO	**Next Item Pointer (NEXT):** Configuration offset of the next Capability Item. 0x00 indicates the last item in the Capability List.
7:0	09h RO	**Capability ID (CAPID):** Value of 0x09 indicates a Vendor Specific Capability

35.6.20 FDLEN (Feature_Detection_Capability_Length)—Offset E2h

Feature detection capability length.

Access Method

Type: PCI Configuration Register (Size: 8 bits)	**Feature_Detection_Capability_Length:** [B:0, D:31, F:0] + E2h

Default: 0Ch

7			4				0
0	0	0	0	1	1	0	0
CAPLEN							

Bit Range	Default & Access	Description
7:0	0Ch RO	**Capability Length (CAPLEN):** Indicates the length of this Vendor Specific capability, as required by PCI Spec

35.6.21 FDVER (Feature_Detection_Version_Register)—Offset E3h

Feature detection version register.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Feature_Detection_Version_Register: [B:0, D:31, F:0] + E3h

Default: 10h

7			4				0
0	0	0	1	0	0	0	0
VSCID				CAPVER			

Bit Range	Default & Access	Description
7:4	1h RO	**Vendor-Specific Capability ID (VSCID):** A value of 0x1 in this 4-bit field identifies this Capability as Feature Detection Type. This field allows software to differentiate the Feature Detection Capability from other Vendor-Specific capabilities.
3:0	0h RO	**Capability Version (CAPVER):** This field indicates the version of the Feature Detection capability

35.6.22 FVECTIDX (Feature_Vector_Index)—Offset E4h

Feature vector index - Reserved

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Feature_Vector_Index: [B:0, D:31, F:0] + E4h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																															

Bit Range	Default & Access	Description
31:0	00000000h RO	**RSVD:** RSVD

35.6.23 FVECTD (Feature_Vector_Data)—Offset E8h

Feature vector data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Feature_Vector_Data: [B:0, D:31, F:0] + E8h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA (bits 31:0)

Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** 32-bit data value that is taken from capability feature fuses

35.6.24 RCBA (RCRB_BASE_ADDRESS)—Offset F0h

Root Complex registers are mapped into memory space. It is used by the PCU EP and Proxy engine.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RCRB_BASE_ADDRESS: [B:0, D:31, F:0] + F0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BA (bits 31:10), RSVD0 (bits 9:1), EN (bit 0)

Bit Range	Default & Access	Description
31:10	000000h RW	**Base Address (BA):** Base Address for the root complex register block decode range. This address is aligned on a 1KB boundary.
9:1	0b RO	**RSVD0:** Reserved
0	0b RW	**Enable (EN):** When set, enables the range specified in BA to be claimed as the RCRB.

35.6.25 Manufacturer ID (PCIE_REG_MANUFACTURER_ID) - Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RCRB_BASE_ADDRESS: [B:0, D:31, F:0] + F8h

Default: 00000000h

31		28				24				20				16				12				8			4					0
0	0	0	0	0	0	1	x	x	x	x	x	x	x	x	0	0	0	0	1	1	1	1	0	0	0	1	1	0	1	0	0
RSVD							MSID								RSVD1																

Bit Range	Default & Access	Description
31:24	01h RO	**RSVD0:** Reserved
23:16	xxh RO	**Manufacturing Stepping ID (MSID):** This value of this filed depends on the stepping of the processor • B2:0Ah • B3:0Ch • D0:11h • D1:13h
15:0	0F1Ah RO	**RSVD1:** Reserved

35.7 PCU iLB LPC BIOS Control Memory Mapped I/O Registers

Table 326. Summary of PCU iLB LPC BIOS Control Memory Mapped I/O Registers—RCRB_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"GCS (RCRB_GENERAL_CONTROL)—Offset 0h" on page 4555	00000000h

35.7.1 GCS (RCRB_GENERAL_CONTROL)—Offset 0h

General Control and Status - contains BIOS configuration and status

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

RCRB_GENERAL_CONTROL: [RCRB_BASE_ADDRESS] + 0h

RCRB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

RCRB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + F0h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD0	BBSize		RSVD1																	BBS		RSVD2								TS	BILD

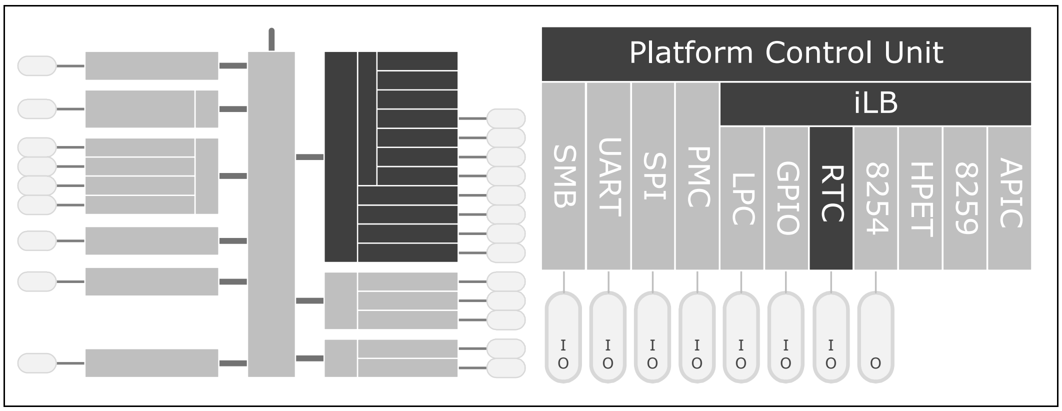
Bit Range	Default & Access	Description
31	0b RO	**RSVD0:** Reserved
30:29	X RO	**Boot Block Size (BBSize):** This field determines the size of the BIOS boot block. Default is controlled by 'Boot Block Size' soft strap. 00 : 64KB (Default) : Invert A16 if Top Swap is enabled 01 : 128KB : Invert A17 if Top Swap is enabled 10 : 256KB : Invert A18 if Top Swap is enabled 11 : Reserved This soft strap only applies when booting from SPI. Boot from LPC (FWH) only supports a 64KB boot block size (Invert A16) and this soft strap value is a don't care.
28:12	0b RO	**RSVD1:** Reserved
11:10	X RW	**Boot BIOS Straps (BBS):** This field determines the destination of accesses to the BIOS memory range. Default is controlled by 'Boot BIOS Straps' pin strap. 00 LPC 01 Reserved 10 Reserved 11 SPI The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) is not set.
9:2	0b RO	**RSVD2:** Reserved
1	X RW	**Top Swap (TS):** When set, PCU EP will invert either A16, A17, or A18 for cycles going to the BIOS space (but not the feature space) in the FWH. When cleared, PCU EP will not invert A16. If booting from LPC (FWH), then the Boot Blook size is 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, or A18 should be inverted if Top Swap is enabled. If Top-Swap pin-strap is active, then this bit cannot be cleared by software. This bit should be kept in RTC well and should be reset only by SRTCRST_b
0	0h RW	**BIOS Interface Lock-Down (BILD):** When set, prevents GCS.TS and GCS.BBS from being changed. This bit can only be written from 0 to 1 once.

36 PCU – iLB – Real Time Clock (RTC)

The SoC contains a Motorola MC146818B-compatible real-time clock with 242 bytes of battery-backed RAM. The real-time clock performs twos key functions—keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 kHz crystal and a 3.3 V battery.

The RTC supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC supports a date alarm that allows for scheduling a wake up event up to 30 days in advance.



36.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 327. RTC Signals

Signal Name	Direction Plat. Power	Description
ILB_RTC_X1	I VRTC	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, the signal can be driven with the desired clock rate.
ILB_RTC_X2	I VRTC	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, the signal should be left floating.
ILB_RTC_RST#	I VRTC	**RTC Reset:** An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. The RC time delay should be in the 18-25 ms range. Contact your Intel representative for details. When asserted, this signal resets all register bits in the RTC well except for GEN_PMCON1.RPS. **NOTE:** Unless registers are being cleared (only to be done in the G3 power state), the signal input must always be high when all other RTC power planes are on. **NOTE:** In the case where the RTC battery is dead or missing on the platform, the signal should be deasserted before the PMC_RSMRST# signal is deasserted.
ILB_RTC_TEST#	I VRTC	**RTC Battery Test:** An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. The RC time delay should be in the 18-25 ms range. Contact your Intel representative for details. If the battery is missing/weak, this signal appears low (asserted) at boot just after the suspend power rail (V3P3A) is up since it will not have time to meet Vih when V3P3A is high. The weak/missing battery condition is reported in the GEN_PMCON1.RPS (RTC Power Status) register. When asserted, BIOS may clear the RTC CMOS RAM. **NOTE:** Unless CMOS is being cleared (only to be done in the G3 power state) or the battery is low, the signal input must always be high when all other RTC power planes are on. **NOTE:** This signal may also be used for debug purposes, as part of a XDP port. Contact your Intel representative for details.
ILB_RTC_EXTPAD	I VRTC	**External capacitor connection**

36.2 Features

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 us to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted.

The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block have very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions. A host-initiated write takes precedence over a hardware update in the event of a collision.

36.2.1 Update Cycles

An update cycle occurs once a second, if the B.SET bit is not asserted and the divide chain is properly configured. During this procedure, the stored time and date are incremented, overflow checked, a matching alarm condition is checked, and the time and date are rewritten to the RAM locations. The update cycle starts at least 488 us after A.UIP is asserted, and the entire cycle does not take more than 1984 us to complete. The time and date RAM locations (00h to 09h) are disconnected from the external bus during this time.

36.3 Interrupts

The real-time clock interrupt is internally routed within the SoC both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the SoC, nor is it shared with any other interrupt. IRQ8# from the ILB_LPC_SERIRQ stream is ignored. However, the High Performance Event Timers can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

36.3.1 Lockable RAM Ranges

The RTC battery-backed RAM supports two 8-byte ranges that can be locked: the RC.UL and RC.LL register bits. When the locking bits are set, the corresponding range in the RAM is not readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (resultant value is undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to re-lock the RAM range.

36.3.2 Clearing Battery-Backed RTC CMOS RAM

Clearing CMOS RAM in an SoC-based platform can be done by using a jumper on ILB_RTC_TEST# or a GPI. Implementations should not attempt to clear CMOS by using a jumper to pull RTC_VCC low.

Note: The entire Extended Bank and bytes 0Eh-7Fh of the Standard Bank will be cleared.

36.3.2.1 Using ILB_RTC_TEST# to Clear the RTC CMOS RAM

A jumper on ILB_RTC_TEST# can be used to clear CMOS values. When ILB_RTC_TEST# is low, the GEN_PMCON1.RPS register bit will be set. BIOS can monitor the state of this bit, and manually clear the RTC CMOS array once the system is booted. The normal position will cause ILB_RTC_TEST# to be pulled up through a weak pull-up resistor. This ILB_RTC_TEST# jumper technique allows the jumper to be moved and then replaced—all while the system is powered off. Then, once booted, the GEN_PMCON1.RPS bit can be detected in the set state.

36.3.3 Using a GPI to Clear CMOS

A jumper on a GPI can also be used to clear CMOS values. BIOS should detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

Note: The GPI strap technique to clear CMOS requires multiple steps to implement. The system is booted with the jumper in new position, then powered back down. The jumper is replaced back to the normal position, then the system is rebooted again.

Warning: Do not implement a jumper on RTC_VCC to clear CMOS.

36.3.4 Clearing Battery Backed RTC Registers

Clearing Battery Backed RTC Registers in an SoC based platform can be done by using a jumper on ILB_RTC_RST#. Implementations should not attempt to clear the registers by using a jumper to pull RTC_VCC low. A jumper on ILB_RTC_RST# pulled to ground can be used to reset the state of those Battery Backed RTC Register configurations bit that reside in the RTC power well to their default state. Table 328 shows which bits are set to their default state when ILB_RTC_RST# is asserted low.

Table 328. Register Bits Reset by ILB_RTC_RST# Assertion (Sheet 1 of 2)

Register Bit	Bit(s)	Default State
RCRB_GENERAL_CONTROL.TS	1	xb
GEN_PMCON1.PME_B0_S5_DIS	15	0b
GEN_PMCON1.WOL_EN_OVRD	13	0b
GEN_PMCON1.DIS_SLP_X_STRCH_SUS_UP	12	0b
GEN_PMCON1.RTC Reserved	8	0b
GEN_PMCON1.SWSMI_RATESEL	7:6	00b
GEN_PMCON1.S4MAW	5:4	00b
GEN_PMCON1.S4ASE	3	0b
GEN_PMCON1.AG3E	0	0b
PM1_STS_EN.RTC_EN	26	0b
PM1_STS_EN.PWRBTNOR_STS	11	0b

Table 328. Register Bits Reset by ILB_RTC_RST# Assertion (Sheet 2 of 2)

Register Bit	Bit(s)	Default State
PM1_CNT.SLP_TYP	12:10	0b
GPE0a_EN.PME_B0_EN	13	0b
GPE0a_EN.BATLOW_EN	10	0b

36.4 References

Accessing the Real Time Clock Registers and the NMI Enable Bit: http://download.intel.com/design/intarch/PAPERS/321088.pdf

36.5 Register Map

36.6 IO Mapped Registers

The RTC internal registers and RAM is organized as two banks of 128 bytes each, called the standard and extended banks.

Note: It is not possible to disable the extended bank.

The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A - D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM. All data movement between the host CPU and the RTC is done through registers mapped to the standard I/O space.

Note: Registers reg_RTC_IR_type and reg_RTC_TR_type are used for data movement to and from the standard bank. Registers reg_RTC_RIR_type and reg_RTC_RTR_type are used for data movement to and from the extended bank. All of these registers have alias I/O locations, as indicated in Table 329.

Table 329. I/O Registers Alias Locations

Register	Original I/O Location	Alias I/O Location
reg_RTC_IR_type	70h	74h
reg_RTC_TR_type	71h	75h
reg_RTC_RIR_type	72h	76h
reg_RTC_RTR_type	73h	77h

36.7 Indexed Registers

The RTC contains indexed registers that are accessed via the reg_RTC_IR_type and reg_RTC_TR_type registers.

Table 330. RTC Indexed Registers

Start	End	Name
00h	00h	Seconds
01h	01h	Seconds Alarm
02h	02h	Minutes
03h	03h	Minutes Alarm
04h	04h	Hours
05h	05h	Hours Alarm
06h	06h	Day of Week
07h	07h	Day of Month
08h	08h	Month
09h	09h	Year
0Ah	0Ah	Register A
0Bh	0Bh	Register B
0Ch	0Ch	Register C
0Dh	0Dh	Register D
0Eh	7Fh	114 Bytes of User RAM

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36.8 PCU iLB Real Time Clock (RTC) I/O Registers

Table 331. Summary of PCU iLB Real Time Clock (RTC) I/O Registers—

Offset	Size	Register ID—Description	Default Value
70h	1	"IR (reg_RTC_IR_type)—Offset 70h" on page 4562	00h
71h	1	"TR (reg_RTC_TR_type)—Offset 71h" on page 4562	00h
72h	1	"RIR (reg_RTC_RIR_type)—Offset 72h" on page 4563	00h
73h	1	"RTR (reg_RTC_RTR_type)—Offset 73h" on page 4563	00h

36.8.1 IR (reg_RTC_IR_type)—Offset 70h

Indexed Registers

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_IR_type: 70h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IR							

Bit Range	Default & Access	Description
7:0	X RW	**IR:** Real-Time Clock (Standard RAM) Index Register Note: Writes to 72h, 74h, and 76h do not affect the NMI enable (bit 7 of 70h)

36.8.2 TR (reg_RTC_TR_type)—Offset 71h

Target Registers

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_TR_type: 71h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
TR							

Bit Range	Default & Access	Description
7:0	X RW	**TR:** Real-Time Clock (Standard RAM) Target Register

36.8.3 RIR (reg_RTC_RIR_type)—Offset 72h

Extended RAM Index Register

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_RIR_type: 72h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RIR							

Bit Range	Default & Access	Description
7:0	X RW	**RIR:** Extended RAM Index Register

36.8.4 RTR (reg_RTC_RTR_type)—Offset 73h

Extended RAM Target Register

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_RTR_type: 73h

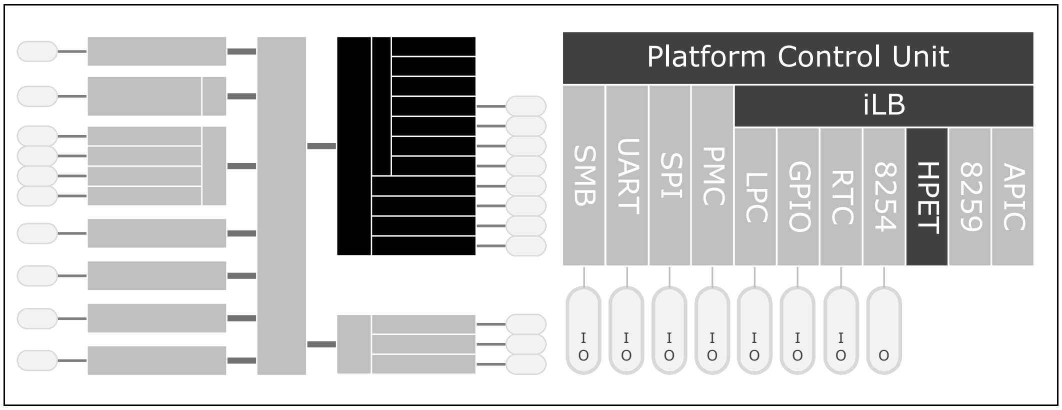
Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RTR							

Bit Range	Default & Access	Description
7:0	X RW	**RTR:** Extended RAM Target Register

37 PCU – iLB – 8254 Timers

The 8254 contains three counters which have fixed uses including system timer and speaker tone. The reference clock for the counters (1.19318 MHz) is generated from a 14.318 MHz clock divided by 12.



37.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane.
- **Description**: A brief explanation of the signal's function

Table 332. 8254 Signals

Signal Name	Direction Plat. Power	Description
ILB_8254_SPKR	O V1P8S	**Speaker:** The signal drives an external speaker driver device, which in turn drives the system speaker. Upon PMC_PLTRST#, its output state is 0. *This signal is muxed and may be used by other functions.*

37.2 Features

37.2.1 Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

37.2.2 Counter 1, Refresh Request Signal

This counter is programmed for Mode 2 operation and impacts the period of the NSC.RTS register bit. Programming the counter to anything other than Mode 2 results in undefined behavior.

37.2.3 Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to the NSC.SDE register bit.

37.3 Use

37.3.1 Timer Programming

The counter/timers are programmed in the following fashion:

1. Write a control word to select a counter.
2. Write an initial count for that counter.
3. Load the least and/or most significant bytes (as required by Control Word Bits 5, 4) of the 16-bit counter.
4. Repeat with other counters.

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- **Control Word Command.** Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- **Counter Latch Command.** Latches the current count so that it can be read by the system. The countdown process continues.
- **Read Back Command.** Reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 333 lists the six operating modes for the interval counters.

Table 333. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware re-triggerable one-shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, etc.
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.

37.3.2 Reading from the Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, counter Latch command, and the Read-Back command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

37.3.2.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through Port 40h (Counter 0), 41h (Counter 1), or 42h (Counter 2).

Note: Performing a direct read from the counter does not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of Counter 2, the count can be stopped by writing 0b to the NSC.TC2E register bit.

37.3.2.2 Counter Latch Command

The Counter Latch command, written to Port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter’s Count register as was programmed by the Control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read is the count at the time the first Counter Latch command was issued.

37.3.2.3 Read Back Command

The Read Back command, written to Port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back commands. If multiple count and/or status Read Back commands are issued to the same counters without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter returns the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two type counts, returns the latched count. Subsequent reads return unlatched count.

37.4 Register Map

37.5 IO Mapped Registers

The IO ports listed in Table 334 have multiple register functions depending on the current programmed state of the 8254. The port numbers referenced in the register descriptions following Table 334 is one possible combination but not the only one.

Table 334. Register Aliases

Port	Alias	Register Name	Default Value	Access
40h	50h	Counter 0 Interval Time Status Byte Format (C0TS)	0xxxxxxxb	RO
		Counter 0 Counter Access Port Register (C0AP)	Undefined	RW
41h	51h	Counter 1 Interval Time Status Byte Format (C1TS)	0xxxxxxxb	RO
		Counter 1 Counter Access Port Register (C1AP)	Undefined	RW
42h	52h	Counter 2 Interval Time Status Byte Format (C2TS)	0xxxxxxxb	RO
		Counter 2 Counter Access Port Register (C2AP)	Undefined	RW
43h	-	Timer Control Word Register (TCW)	Undefined	WO
		Read Back Command (RBC)	xxxxxxx0b	WO
		Counter Latch Command (CLC)	xxxx0000b	WO

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37.6 PCU iLB 8254 Timers IO Registers

Table 335. Summary of PCU iLB 8254 Timers I/O Registers—

Offset	Size	Register ID—Description	Default Value
40h	1	"C0TS—Offset 40h" on page 4569	00h
41h	1	"C1TS—Offset 41h" on page 4570	00h
42h	1	"C2TS—Offset 42h" on page 4570	00h
43h	1	"TCW—Offset 43h" on page 4571	00h
50h	1	"C0AP—Offset 50h" on page 4572	00h
51h	1	"C1AP—Offset 51h" on page 4572	00h
52h	1	"C2AP—Offset 52h" on page 4572	00h
61h	1	"NSC—Offset 61h" on page 4573	20h

37.6.1 C0TS—Offset 40h

Counter 0 Interval Time Status Byte Format.Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 0, the next read from this register returns the status byte.

Access Method

Type: I/O Register
(Size: 8 bits)

C0TS: 40h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CS	CR	RWS		MD			CT

Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

37.6.2 C1TS—Offset 41h

Counter 1 Interval Time Status Byte Format. Counter 1 Interval Time Status Byte Format. Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 1, the next read from this register returns the status byte.

Access Method

Type: I/O Register (Size: 8 bits)

C1TS: 41h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CS	CR	RWS		MD			CT

Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

37.6.3 C2TS—Offset 42h

Counter 2 Interval Time Status Byte Format. Counter 2 Interval Time Status Byte Format. Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 2, the next read from this register returns the status byte.

Access Method

Type: I/O Register (Size: 8 bits)

C2TS: 42h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CS	CR	RWS		MD			CT

Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

37.6.4 TCW—Offset 43h

Timer Control Word Register. This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Access Method

Type: I/O Register
(Size: 8 bits)

TCW: 43h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CS		RWS		CMS			BCS

Bit Range	Default & Access	Description
7:6	X WO	**CS:** Counter Select (CS): The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select 11 Read Back Command
5:4	X WO	**RWS:** Read/Write Select RWS): The counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X WO	**CMS:** Counter Mode Selection (CMS): Selects one of six modes of operation for the selected counter. 000 = Out signal on end of count (=0) 001 = Hardware retriggerable one-shot x10 = Rate generator (divide by n counter) x11 = Square wave output 100 = Software triggered strobe 101 = Hardware triggered strobe
0	X WO	**BCS:** Binary/BCD Countdown Select (BCS): 0 Binary countdown is used. The largest possible binary count is 216 1 Binary coded decimal (BCD) count is used. The largest possible BCD count is 104

37.6.5 C0AP—Offset 50h

Counter 0 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

C0AP: 50h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CP							

Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

37.6.6 C1AP—Offset 51h

Counter 1 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

C1AP: 51h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CP							

Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

37.6.7 C2AP—Offset 52h

Counter 2 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

C2AP: 52h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CP							

Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

37.6.8 NSC—Offset 61h

NMI Status and Control

Access Method

Type: I/O Register
(Size: 8 bits)

NSC: 61h

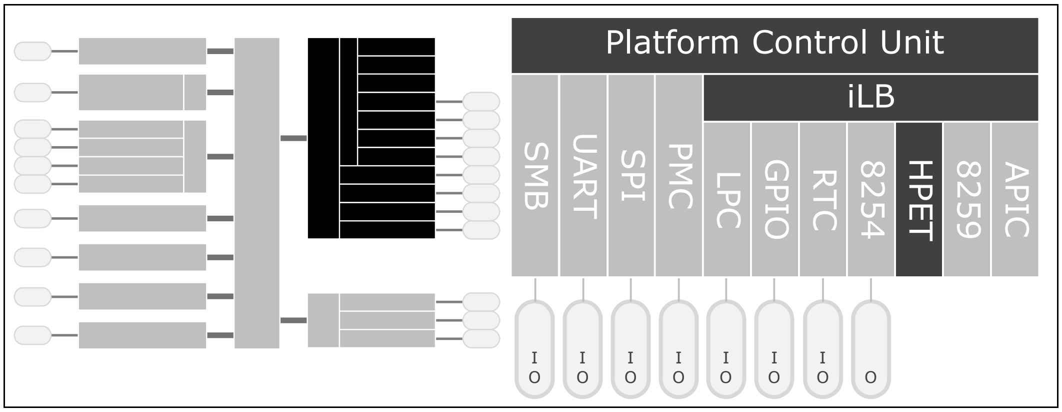
Default: 20h

7			4				0
0	0	1	0	0	0	0	0
SNS	INS	T2S	RTS	INE	SNE	SDE	TC2E

Bit Range	Default & Access	Description
7	0b RO	**SNS:** SERR# NMI Status (SNS): Set on errors from a PCIe port or internal functions that generate SERR#. SNE in this register must be cleared in order for this bit to be set. To reset the interrupt, set bit 2 to 1 and then set it to 0.
6	0b RO	**INS:** IOCHK NMI Status (INS): Set when SERIRQ asserts IOCHK# and INE in this register is cleared. To reset the interrupt, set bit 3 to 1 and then set it to 0.
5	1b RO	**RTS (T2S):** Timer Counter 2 Status (T2S): Reflects the current state of the 8254 counter 2 outputs. Counter 2 must be programmed for this bit to have a determinate value.
4	0b RO	**RTS:** Refresh Cycle Toggle Status (RTS): Reflects the current state of 8254 counter 1
3	X RW	**INE:** IOCHK NMI Enable (INE): When set, IOCHK# NMIs are disabled. When cleared, IOCHK# NMIs are enabled.
2	0b RW	**SNE:** SERR# NMI Enable (SNE): When set, SERR# NMIs are disabled. When cleared, SERR# NMIs are enabled.
1	0b RW	**SDE:** Speaker Data Enable (SDE): When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0b RW	**TC2E:** Timer Counter 2 Enable (TC2E): When cleared, counter 2 counting is disabled. When set, counting is enabled.

38 PCU – iLB – High Precision Event Timer (HPET)

This function provides a set of timers that to be used by the operating system for timing events. One timer block is implemented, containing one counter and three timers.



38.1 Features

38.1.1 Non-Periodic Mode - All Timers

This mode can be thought of as creating a one-shot. When a timer is set up for non-periodic mode, it generates an interrupt when the value in the main counter matches the value in the timer's comparator register. As timers 1 and 2 are 32-bit, they will generate another interrupt when the main counter wraps.

T0CV cannot be programmed reliably by a single 64-bit write in a 32-bit environment unless only the periodic rate is being changed. If T0CV needs to be re-initialized, the following algorithm is performed:

1. Set T0C.TVS
2. Set T0CV[31:0]
3. Set T0C.TVS
4. Set T0CV[63:32]

Every timer is required to support the non-periodic mode of operation.

38.1.2 Periodic Mode - Timer 0 only

When set up for periodic mode, when the main counter value matches the value in T0CV, an interrupt is generated (if enabled). Hardware then increases T0CV by the last value written to T0CV. During run-time, T0CV can be read to find out when the next periodic interrupt will be generated. Software is expected to remember the last value written to T0CV.

Example: if the value written to T0CV is 00000123h, then

- An interrupt will be generated when the main counter reaches 00000123h.
- T0CV will then be adjusted to 00000246h.
- Another interrupt will be generated when the main counter reaches 00000246h.
- T0CV will then be adjusted to 00000369h.

When the incremented value is greater than the maximum value possible for T0CV, the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h.

If software wants to change the periodic rate, it writes a new value to T0CV. When the timer's comparator matches, the new value is added to derive the next matching point. If software resets the main counter, the value in the comparator's value register must also be reset by setting T0C.TVS. To avoid race conditions, this should be done with the main counter halted. The following usage model is expected:

1. Software clears GCFG.EN to prevent any interrupts.
2. Software clears the main counter by writing a value of 00h to it.
3. Software sets T0C.TVS.
4. Software writes the new value in T0CV.
5. Software sets GCFG.EN to enable interrupts.

38.1.2.1 Interrupts

If each timer has a unique interrupt and the timer has been configured for edge-triggered mode, then there are no specific steps required. If configured to level-triggered mode, then its interrupt must be cleared by software by writing a '1' back to the bit position for the interrupt to be cleared.

Interrupts associated with the various timers have several interrupt mapping options. Software should mask GCFG.LRE when reprogramming HPET interrupt routing to avoid spurious interrupts.

38.1.2.2 Mapping Option #1: Legacy Option (GCFG.LRE set)

This forces the following mapping:

Table 336. 8254 Interrupt Mapping

Timer	8259 Mapping	APIC Mapping	Comment
0	IRQ0	IRQ2	The 8254 timer will not cause any interrupts
1	IRQ8	IRQ8	RTC will not cause any interrupts.
2	T2C.IR	T2C.IRC	

38.1.2.3 Mapping Option #2: Standard Option (GCFG.LRE cleared)

Each timer has its own routing control. The interrupts can be routed to various interrupts in the I/O APIC. T[2:0]C.IRC indicates which interrupts are valid options for routing. If a timer is set for edge-triggered mode, the timers should not be shared with any other interrupts.

38.2 References

IA-PC HPET (High Precision Event Timers) Specification, Revision 1.0a: http://www.intel.com/hardware design/hpetspec_1.pdf

38.3 Register Map

38.4 Memory Mapped Registers

The register space is memory mapped to a 1K block at address FED00000h. All registers are in the core well. Accesses that cross register boundaries result in undefined behavior.

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38.5 PCU iLB High Performance Event Timer (HPET) Memory Mapped IO Registers

Table 337. Summary of PCU iLB High Performance Event Timer (HPET) Memory Mapped I/O Registers—

Offset	Size	Register ID—Description	Default Value
FED00000h	8	"GCID (HPET_GCID)—Offset FED00000h" on page 4577	0429B17F8086A201h
FED00010h	8	"GCFG (HPET_GCFG)—Offset FED00010h" on page 4578	0000000000000000h
FED00020h	8	"GIS (HPET_GIS)—Offset FED00020h" on page 4578	0000000000000000h
FED000F0h	8	"MCV (HPET_MCV)—Offset FED000F0h" on page 4579	0000000000000000h
FED00100h	8	"T0C (HPET_T0C)—Offset FED00100h" on page 4579	00F0000000000030h
FED00108h	4	"T0CV_L (HPET_T0CV_L)—Offset FED00108h" on page 4580	FFFFFFFFh
FED0010Ch	4	"T0CV_U (HPET_T0CV_U)—Offset FED0010Ch" on page 4581	FFFFFFFFh
FED00120h	8	"T1C (HPET_T1C)—Offset FED00120h" on page 4581	00F0000000000000h
FED00128h	8	"T1CV (HPET_T1CV)—Offset FED00128h" on page 4582	00000000FFFFFFFFh
FED00140h	8	"T2C (HPET_T2C)—Offset FED00140h" on page 4583	00F0080000000000h
FED00148h	8	"T2CV (HPET_T2CV)—Offset FED00148h" on page 4584	00000000FFFFFFFFh

38.5.1 GCID (HPET_GCID)—Offset FED00000h

General Capabilities and ID

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

HPET_GCID: FED00000h

Default: 0429B17F8086A201h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4
0 0 0 0	0 1 0 0	0 0 1 0	1 0 0 1	1 0 1 1	0 0 0 1	0 1 1 1	1 1 1 1	1 0 0 0	0 0 0 0	1 0 0 0	0 1 1 0	1 0 1 0	0 0 1 0	0 0 0 0	0 0 0 1

Fields (bit 63 to bit 0): CTP, VID, LRC, RESERVED, CS, NT, RID

Bit Range	Default & Access	Description
63:32	0429B17Fh RO	**CTP:** Counter Tick Period (CTP): Indicates a period of 69.841279ns, (14.1318 MHz clock period)
31:16	8086h RO	**VID:** Vendor ID (VID): Value of 8086h indicates Intel.
15	1b RO	**LRC:** Legacy Rout Capable (LRC): Indicates support for Legacy Interrupt Rout.
14	0b RO	**RESERVED:** Reserved.
13	1b RO	**CS:** Counter Size (CS): This bit is set to indicate that the main counter is 64 bits wide.

Bit Range	Default & Access	Description
12:8	02h RO	**NT:** Number of Timers (NT): Indicates that 3 timers are supported.
7:0	01h RO	**RID:** Revision ID (RID): Indicates that revision 1.0 of the specification is implemented.

38.5.2 GCFG (HPET_GCFG)—Offset FED00010h

General Configuration

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

HPET_GCFG: FED00010h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

RESERVED | LRE | EN

Bit Range	Default & Access	Description
63:2	0b RO	**RESERVED:** Reserved.
1	0b RW	**LRE:** Legacy Rout Enable (LRE): When set, interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in 8259 and I/O APIC Timer 2 will be routed as per the routing in T2C When set, the T[1:0]C.IR will have no impact for timers 0 and 1.
0	0b RW	**EN:** Overall Enable (EN): When set, the timers can generate interrupts. When cleared, the main counter will halt and no interrupts will be caused by any timer. For level-triggered interrupts, if an interrupt is pending when this bit is cleared, the GIS.Tx will not be cleared.

38.5.3 GIS (HPET_GIS)—Offset FED00020h

General Interrupt Status

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

HPET_GIS: FED00020h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

RESERVED | T2 | T1 | T0

Bit Range	Default & Access	Description
63:3	0b RO	**RESERVED:** Reserved.
2	0b RW	**T2:** Timer 2 Status (T2): Same functionality as T0, for timer 2.
1	0b RW	**T1:** Timer 1 Status (T1): Same functionality as T0, for timer 1.
0	0b RW	**T0:** Timer 0 Status (T0): In edge triggered mode, this bit always reads as 0. In level triggered mode, this bit is set when an interrupt is active.

38.5.4 MCV (HPET_MCV)—Offset FED000F0h

Main Counter Value

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

HPET_MCV: FED000F0h

Default: 0000000000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	

Field: CV (63:0)

Bit Range	Default & Access	Description
63:0	0b RW	**CV:** Counter Value (CV): Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

38.5.5 T0C (HPET_T0C)—Offset FED00100h

Timer 0 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

HPET_T0C: FED00100h

Default: 00F0000000000030h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0000	0000	1111	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0011	0000	

Fields (MSB to LSB): CV, RESERVED, FID, FE, IR, T32M, RESERVED2, TVS, TS, PIC, TYP, IE, IT, RESERVED3

Bit Range	Default & Access	Description
63:32	00f00000h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23

Bit Range	Default & Access	Description
31:16	0h RO	**RESERVED:** Reserved.
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RW	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RW	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	1b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	1b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0b RW	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0b RO	**RESERVED (RESERVED3):** Reserved.

38.5.6 T0CV_L (HPET_T0CV_L)—Offset FED00108h

Lower Timer 0 Comperator Value

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

HPET_T0CV_L: FED00108h

Default: FFFFFFFFh

31			28				24				20				16				12				8				4				0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

T0CV_L

Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW	**T0CV_L:** Lower Timer 0 Comperator Value

38.5.7 T0CV_U (HPET_T0CV_U)—Offset FED0010Ch

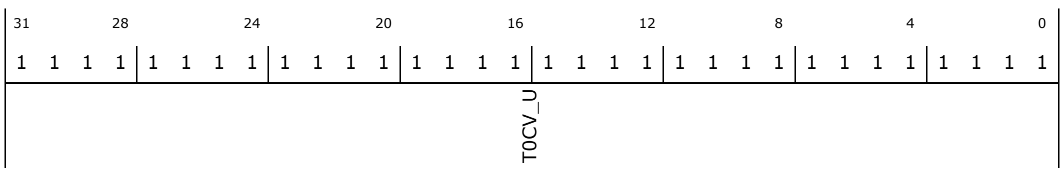
Upper Timer 0 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HPET_T0CV_U: FED0010Ch

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW	**T0CV_U:** Upper Timer 0 Comperator Value

38.5.8 T1C (HPET_T1C)—Offset FED00120h

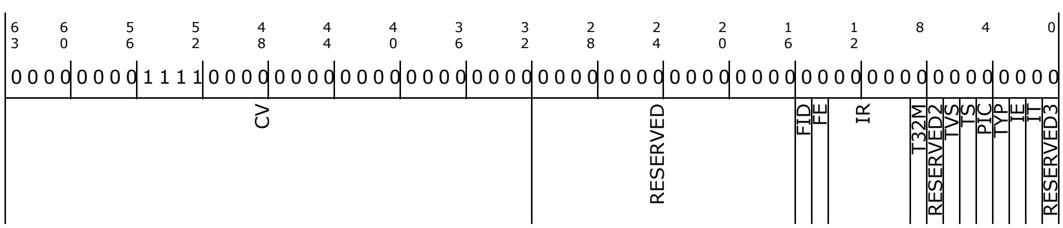
Timer 1 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T1C: FED00120h

Default: 00F0000000000000h



Bit Range	Default & Access	Description
63:32	00f00000h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0h RO	**RESERVED:** Reserved.
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported

Bit Range	Default & Access	Description
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RO	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RO	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0b RO	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0b RO	**RESERVED (RESERVED3):** Reserved.

38.5.9 T1CV (HPET_T1CV)—Offset FED00128h

Timer 1 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)	**HPET_T1CV:** FED00128h

Default: 00000000FFFFFFFFh

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	

63:32	31:0
RESERVED1	T1CV

Bit Range	Default & Access	Description
63:32	0b RO	**RESERVED (RESERVED1):** Reserved.
31:0	FFFFFFFFh RO	**T1CV:** Timer 1 Comperator Value

38.5.10 T2C (HPET_T2C)—Offset FED00140h

Timer 2 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register
(Size: 64 bits)

HPET_T2C: FED00140h

Default: 00F0080000000000h

63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Fields: CV | RESERVED | FID | FE | IR | T32M | RESERVED2 | TVS | TS | PIC | TYP | IE | IT | RESERVED3

Bit Range	Default & Access	Description
63:32	00f00800h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0h RO	**RESERVED:** Reserved.
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RO	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RO	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.

Bit Range	Default & Access	Description
3	0b RO	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0b RO	**RESERVED (RESERVED3):** Reserved.

38.5.11 T2CV (HPET_T2CV)—Offset FED00148h

Timer 2 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T2CV: FED00148h

Default: 00000000FFFFFFFFh

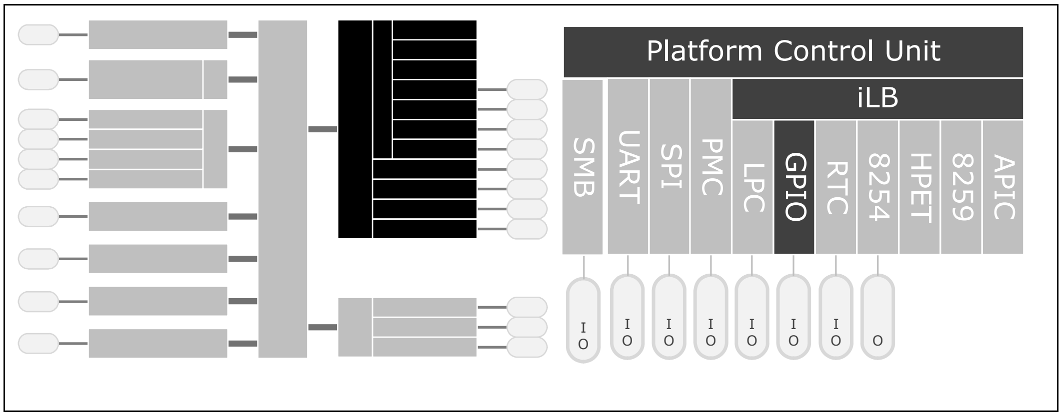
63	60	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	

RESERVED1 (bits 63:32) | T2CV (bits 31:0)

Bit Range	Default & Access	Description
63:32	0b RO	**RESERVED (RESERVED1):** Reserved.
31:0	FFFFFFFFh RO	**T2CV:** Timer 2 Comperator Value

39 PCU – iLB – GPIO

102 GPIOs are available for use during the S0 ACPI state, and 44 are available for use from S5 to S0 (SUS). Most of these GPIOs can be used as legacy GPIOs through IO registers.



39.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Platform Power**: The reference power plane
- **Description**: A brief explanation of the signal's function

Table 338. GPIO Signals

Signal Name	Direction Plat. Power	Description
GPIO_S0_SC[101:0]	I/O Varies	These GPIO pins are powered and active in S0 only. Many of these are multiplexed with other functions and may have different default pin names.
GPIO_S5[43:0]	I/O Varies	These GPIO pins are powered and active in S5-S0 (SUS). Many of these are multiplexed with other functions and may have different default pin names. Some are used as straps.

39.2 Features

GPIOs can generate general purpose events (GPEs) on rising and/or falling edges.

39.3 Legacy Use

Each GPIO has six registers that control how it is used, or report its status:

- Use Select
- I/O Select
- GPIO Level
- Trigger Positive Edge
- Trigger Negative Edge
- Trigger Status

The Use Select register selects a GPIO pin as a GPIO, or leaves it as its programmed function. This register must be set for all other registers to affect the GPIO.

The I/O Select register determines the direction of the GPIO.

The Trigger Positive Edge and Trigger Negative Edge registers enable general purpose events on a rising and falling edge respectively. This only applies to GPIOs set as input.

The Trigger Status register is used by software to determine if the GPIO triggered a GPE. This only applies to GPIOs set as input and with one or both of the Trigger modes enabled.

Additionally, there is one additional register for each S5 GPIO:

- Wake Enable

This register allows S5 GPIOs to trigger a wake event based on the Trigger registers' settings.

39.4 Memory Mapped Use

Each GPIO has two registers that control how it is used, or report its status:

- Pad Configuration (PCONF0)
- Pad Value (PAD_VAL)

Note: These registers are also implemented for the available Virtual GPIOs (vGPIOs).

The Pad Configuration register has the following functions:

- Configure the function of the pin as a GPIO or mulitplexed native functions
- Configure pull resistors
- Configure electrical behavior
- Configure edge detection
- Configure interrupt handling

Note: The PCONF0 register is valid irrespective of whether or not the pin is conifgured as a GPIO

The Pad Value register has the following functions:

- Reads the GPIO value, when configured as a GPI
- Writes the GPIO value, when configured as a GPO
- Enables/disables input and output capabilities

Note: The Pad Value register is only valid when the pin is configured as a GPIO in the Pad Configuration register.

Additionally, there are a number of general configuration registers that control groups of GPIOs or report their status. These include:

- IRQ Status (IRQ_TS)
- Direct IRQ Multiplexer (DIRECT_IRQ)

The IRQ Status register indicates if an IRQ associated with a GPIO has been triggered.

The Direct IRQ Multiplexer register allows for a selection of GPIOs to be assigned a dedicated APIC interrupt.

The GPIO South CORE and GPIO South SUS families have 16 dedicated IRQ outputs for each. Each of these 16 has a mux with an 8 bit select that can pick which of the input pads are mapped to that direct IRQ (the pad would still need to be programmed). Refer to the Intel Bios Writers Guide. This programming is done with the Direct IRQ 0 - 3 registers for SCORE and SSUS domains listed in the GPIO Family Register section.

The 16 GPSCORE direct IRQs are mapped to `IOAPIC_IRQ [66:51]`.

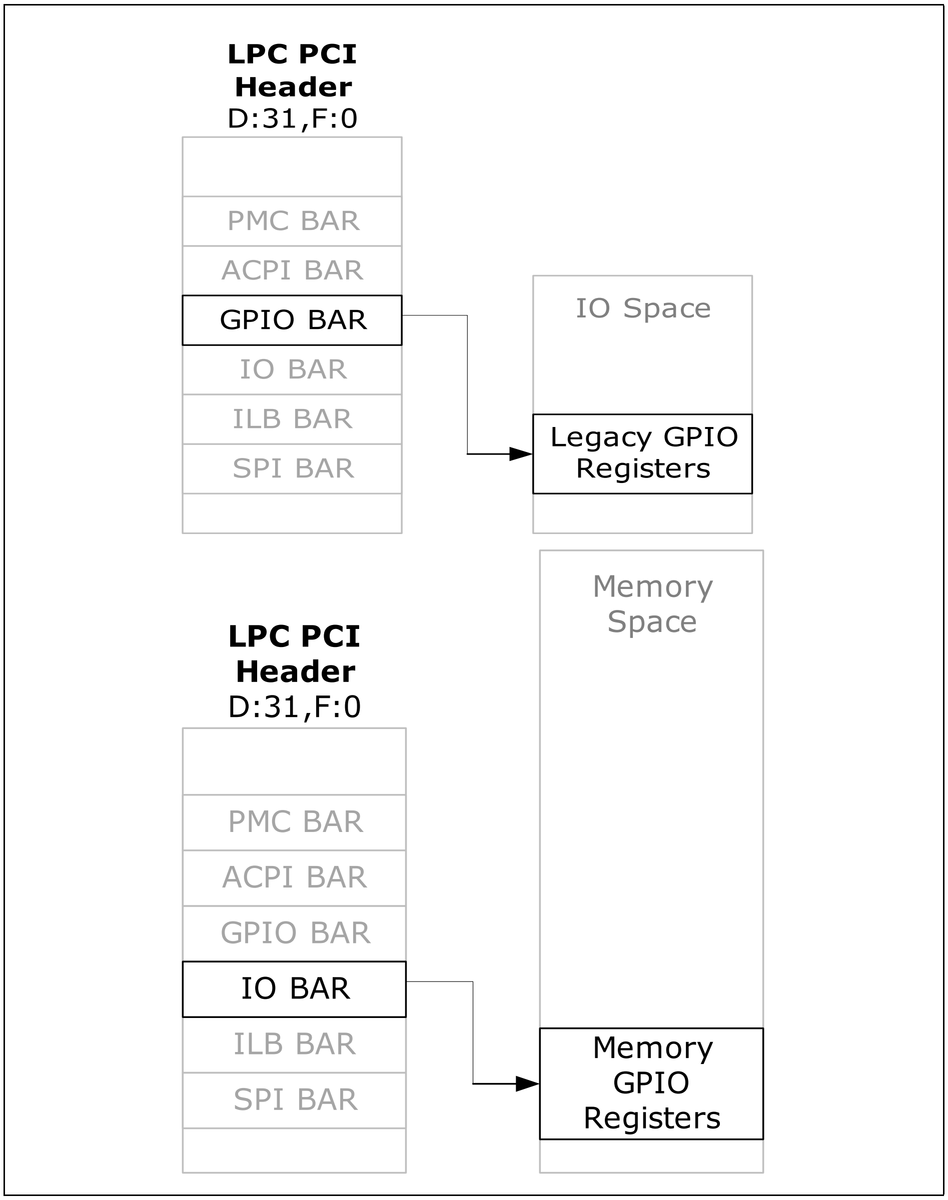
The 16 GPSSUS direct IRQs are mapped to `IOAPIC_IRQ [82:67]`.

For example:

1. Programming GPSCORE Direct IRQ 0 [dirq0] = 4 will map GPIO_S0_SC[004]/ pCIE_CLKREQ[1#] to IRQ51.
2. Programming GPSCORE Direct IRQ 0 [dirq1] = 8 will map GPIO_S0_SC[008]/ I2S0_CLK to IRQ52.

39.5 Register Map

Figure 137.SIO - I²C Register Map



39.6 GPIO Registers

Registers are broken into two groups: memory mapped and legacy IO registers. Memory mapped registers are used by BIOS and firmware to select the configurable function of the GPIO and setup analog states needed for that function's operation. They are named based on the pin/ball name. Legacy IO registers are the more traditional GPIO control/status type, and are used when the function selected is a traditional GPIO (direction, level, use registers). They are numbered based on the GPIO number.

Each group is further broken down into SCORE (internal partition naming) and SSUS. SCORE are for the GPIO's named GPIO_S0_SC[xxx], while SSUS are for the GPIO's named GPIO_S5[xx].

Note: All GPIO registers must be accessed as double words. Unpredictable results will occur otherwise.

Note: All memory mapped GPIO *_PAD_VAL's must set Ienenb = 0 in order to read the pad_val of the GPIO. This applies to RO GPIO's as well.

Note: vGPIO's are virtual GPIO's for use by software to generate interrupts. They are not tied to physical pins.

Note: When a GPIO is selected via the IO USE_SEL, Memory accesses are denied (pconf0, pconf1 and pad_val).

§

39.7 PCU iLB GPIO S0 IO Addressed Registers

Table 339. Summary of PCU iLB GPIO S0 IO Registers—GPIO_BASE_ADDRESS

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"South Core Use Select 1 (cfio_ioreg_SC_USE_SEL_31_0_)—Offset 0h" on page 4591	00000000h
4–7h	4	"South Core Io Select 1 (cfio_ioreg_SC_IO_SEL_31_0_)—Offset 4h" on page 4592	00000000h
8–Bh	4	"South Core Gpio Level 1 (cfio_ioreg_SC_GP_LVL_31_0_)—Offset 8h" on page 4593	00000000h
C–Fh	4	"South Core Trigger Positive Edge Enable 1 (cfio_ioreg_SC_TPE_31_0_)—Offset Ch" on page 4594	00000000h
10–13h	4	"South Core Trigger Negative Enable 1 (cfio_ioreg_SC_TNE_31_0_)—Offset 10h" on page 4595	00000000h
14–17h	4	"South Core Trigger Status 1 (cfio_ioreg_SC_TS_31_0_)—Offset 14h" on page 4596	00000000h
20–23h	4	"South Core Use Select 2 (cfio_ioreg_SC_USE_SEL_63_32_)—Offset 20h" on page 4597	00000000h
24–27h	4	"South Core Io Select 2 (cfio_ioreg_SC_IO_SEL_63_32_)—Offset 24h" on page 4598	00000000h
28–2Bh	4	"South Core Gpio Level 2 (cfio_ioreg_SC_GP_LVL_63_32_)—Offset 28h" on page 4599	00000000h
2C–2Fh	4	"South Core Trigger Positive Edge Enable 2 (cfio_ioreg_SC_TPE_63_32_)—Offset 2Ch" on page 4600	00000000h
30–33h	4	"South Core Trigger Negative Enable 2 (cfio_ioreg_SC_TNE_63_32_)—Offset 30h" on page 4601	00000000h
34–37h	4	"South Core Trigger Status 2 (cfio_ioreg_SC_TS_63_32_)—Offset 34h" on page 4602	00000000h
40–43h	4	"South Core Use Select 3 (cfio_ioreg_SC_USE_SEL_95_64_)—Offset 40h" on page 4603	00000000h
44–47h	4	"South Core Io Select 3 (cfio_ioreg_SC_IO_SEL_95_64_)—Offset 44h" on page 4604	00000000h
48–4Bh	4	"South Core Gpio Level 3 (cfio_ioreg_SC_GP_LVL_95_64_)—Offset 48h" on page 4605	00000000h
4C–4Fh	4	"South Core Trigger Positive Edge Enable 3 (cfio_ioreg_SC_TPE_95_64_)—Offset 4Ch" on page 4606	00000000h
50–53h	4	"South Core Trigger Negative Enable 3 (cfio_ioreg_SC_TNE_95_64_)—Offset 50h" on page 4607	00000000h
54–57h	4	"South Core Trigger Status 3 (cfio_ioreg_SC_TS_95_64_)—Offset 54h" on page 4608	00000000h
60–63h	4	"South Core Use Select 4 (cfio_ioreg_SC_USE_SEL_127_96_)—Offset 60h" on page 4609	00000000h
64–67h	4	"South Core Io Select 4 (cfio_ioreg_SC_IO_SEL_127_96_)—Offset 64h" on page 4610	00000000h
68–6Bh	4	"South Core Gpio Level 4 (cfio_ioreg_SC_GP_LVL_127_96_)—Offset 68h" on page 4610	00000000h

Table 339. Summary of PCU iLB GPIO S0 IO Registers—GPIO_BASE_ADDRESS

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6C–6Fh	4	"South Core Trigger Positive Edge Enable 4 (cfio_ioreg_SC_TPE_127_96_)—Offset 6Ch" on page 4611	00000000h
70–73h	4	"South Core Trigger Negative Enable 4 (cfio_ioreg_SC_TNE_127_96_)—Offset 70h" on page 4612	00000000h
74–77h	4	"South Core Trigger Status 4 (cfio_ioreg_SC_TS_127_96_)—Offset 74h" on page 4612	00000000h

39.7.1 South Core Use Select 1 (cfio_ioreg_SC_USE_SEL_31_0_)—Offset 0h

Access via PCU proxy, the register is setting the correspanding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 0h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

use_sel

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Use Select (use_sel):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

39.7.2 South Core Io Select 1 (cfio_ioreg_SC_IO_SEL_31_0_)—Offset 4h

Access via PCU proxy, define the Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 4h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

io_sel

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Io Select (io_sel):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

39.7.3 South Core Gpio Level 1 (cfio_ioreg_SC_GP_LVL_31_0_)—Offset 8h

Access via PCU proxy, the registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 8h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

gp_lvl

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000000000000000000000000000b RW	**Gpio Level (gp_lvl):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

39.7.4 South Core Trigger Positive Edge Enable 1 (cfio_ioreg_SC_TPE_31_0_)—Offset Ch

Access via PCU proxy, it is trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

tpe

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000000000000000000000000000b RW	**Tpe (tpe):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

39.7.5 South Core Trigger Negative Enable 1 (cfio_ioreg_SC_TNE_31_0_)—Offset 10h

Trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 10h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

tne

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Tne (tne):** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

39.7.6 South Core Trigger Status 1 (cfio_ioreg_SC_TS_31_0_)—Offset 14h

Access via PCU proxy, when set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV and it cannot be tested by the host

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 14h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ts

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b WOC	**ts:** bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

39.7.7 South Core Use Select 2 (cfio_ioreg_SC_USE_SEL_63_32_)—Offset 20h

Access via PCU proxy, the register is setting the correspanding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[32], and bit 1 will set GPIO[33] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 20h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

use_sel

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Use Select (use_sel):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

39.7.8 South Core Io Select 2 (cfio_ioreg_SC_IO_SEL_63_32_)—Offset 24h

Access via PCU proxy, define the Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 24h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

io_sel

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Io Select (io_sel):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

39.7.9 South Core Gpio Level 2 (cfio_ioreg_SC_GP_LVL_63_32_)—Offset 28h

Access via PCU proxy, the registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 28h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

gp_lvl

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Gpio Level (gp_lvl):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

39.7.10 South Core Trigger Positive Edge Enable 2 (cfio_ioreg_SC_TPE_63_32_)—Offset 2Ch

Access via PCU proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 2Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

tpe

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Tpe (tpe):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

39.7.11 South Core Trigger Negative Enable 2 (cfio_ioreg_SC_TNE_63_32_)—Offset 30h

Access via PCU proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 30h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

tne

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Tne (tne):** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

39.7.12 South Core Trigger Status 2 (cfio_ioreg_SC_TS_63_32_)—Offset 34h

When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [GBASE] + 34h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ts

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b WOC	**ts:** bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

39.7.13 South Core Use Select 3 (cfio_ioreg_SC_USE_SEL_95_64_)—Offset 40h

Access via PCU proxy, the register is setting the correspanding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 40h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

use_sel

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Use Select (use_sel):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

39.7.14 South Core Io Select 3 (cfio_ioreg_SC_IO_SEL_95_64_)—Offset 44h

Access via PCU proxy, it defines Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 44h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

io_sel

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000000000000000000000000000b RW	**Io Select (io_sel):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

39.7.15 South Core Gpio Level 3 (cfio_ioreg_SC_GP_LVL_95_64_)—Offset 48h

This registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [GBASE] + 48h

GBASE Type: PCI Configuration Register (Size: 32 bits)

GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

gp_lvl

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Gpio Level (gp_lvl):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

39.7.16 South Core Trigger Positive Edge Enable 3 (cfio_ioreg_SC_TPE_95_64_)—Offset 4Ch

Access via PCU proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 4Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

tpe

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Tpe (tpe):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

39.7.17 South Core Trigger Negative Enable 3 (cfio_ioreg_SC_TNE_95_64_)—Offset 50h

Access via PCU proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 50h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

tne

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b RW	**Tne (tne):** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

39.7.18 South Core Trigger Status 3 (cfio_ioreg_SC_TS_95_64_)—Offset 54h

When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [GBASE] + 54h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ts

Bit Range	Default & Access	Field Name (ID): Description
31:0	000000000 000000000 000000000 00000b WOC	**ts:** bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

39.7.19 South Core Use Select 4 (cfio_ioreg_SC_USE_SEL_127_96_)—Offset 60h

Access via PCU proxy, the register is setting the correspanding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 60h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																										use_sel					

Bit Range	Default & Access	Field Name (ID): Description
31:6	000000000 000000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Use Select (use_sel):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

39.7.20 South Core Io Select 4 (cfio_ioreg_SC_IO_SEL_127_96_)—Offset 64h

Access via PCU proxy, it defines Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 64h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved (bits 31:6), io_sel (bits 5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	000000000 000000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Io Select (io_sel):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

39.7.21 South Core Gpio Level 4 (cfio_ioreg_SC_GP_LVL_127_96_)—Offset 68h

This registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 68h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved (31:6)	gp_lvl (5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	000000000 000000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Gpio Level (gp_lvl):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

39.7.22 South Core Trigger Positive Edge Enable 4 (cfio_ioreg_SC_TPE_127_96_)—Offset 6Ch

Access via PCU proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 6Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved (31:6)	tpe (5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	000000000 000000000 00000000b RO	**Reserved (reserved):** reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0b RW	**Tpe (tpe):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

39.7.23 South Core Trigger Negative Enable 4 (cfio_ioreg_SC_TNE_127_96_)—Offset 70h

Access via PCU proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 70h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

reserved (bits 31:6) | tne (bits 5:0)

Bit Range	Default & Access	Field Name (ID): Description
31:6	000000000 000000000 00000000b RO	**Reserved (reserved):** reserved
5:0	0b RW	**Tne (tne):** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

39.7.24 South Core Trigger Status 4 (cfio_ioreg_SC_TS_127_96_)—Offset 74h

When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE] + 74h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved																										ts					

Bit Range	Default & Access	Field Name (ID): Description
31:6	000000000000000000000000000b RO	**Reserved (reserved):** reserved
5:0	0b WOC	**ts:** bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

39.8 PCU iLB GPIO S0 Memory Addressed Registers

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	“Uart1 Rts B Pad Configuration (cfio_regs_pad_uart1_rts_b_PCONF0)—Offset 0h” on page 4627	2003CC80h
8–Bh	4	“Uart1 Rts B Pad Value (cfio_regs_pad_uart1_rts_b_PAD_VAL)—Offset 8h” on page 4629	00000002h
10–13h	4	“Uart1 Txd Pad Configuration (cfio_regs_pad_uart1_txd_PCONF0)—Offset 10h” on page 4630	2003CC80h
18–1Bh	4	“Uart1 Txd Pad Value (cfio_regs_pad_uart1_txd_PAD_VAL)—Offset 18h” on page 4632	00000002h
20–23h	4	“Uart1 Rxd Pad Configuration (cfio_regs_pad_uart1_rxd_PCONF0)—Offset 20h” on page 4633	2003CC80h
28–2Bh	4	“Uart1 Rxd Pad Value (cfio_regs_pad_uart1_rxd_PAD_VAL)—Offset 28h” on page 4636	00000002h
30–33h	4	“I2c Nfc Scl Pad Configuration (cfio_regs_pad_i2c_nfc_scl_PCONF0)—Offset 30h” on page 4636	2003CC80h
38–3Bh	4	“I2c Nfc Scl Pad Value (cfio_regs_pad_i2c_nfc_scl_PAD_VAL)—Offset 38h” on page 4639	00000002h
40–43h	4	“Uart1 Cts B Pad Configuration (cfio_regs_pad_uart1_cts_b_PCONF0)—Offset 40h” on page 4639	2003CC80h
48–4Bh	4	“Uart1 Cts B Pad Value (cfio_regs_pad_uart1_cts_b_PAD_VAL)—Offset 48h” on page 4642	00000002h
50–53h	4	“I2c Nfc Sda Pad Configuration (cfio_regs_pad_i2c_nfc_sda_PCONF0)—Offset 50h” on page 4643	2003CC80h
58–5Bh	4	“I2c Nfc Sda Pad Value (cfio_regs_pad_i2c_nfc_sda_PAD_VAL)—Offset 58h” on page 4645	00000002h
60–63h	4	“Uart2 Rxd Pad Configuration (cfio_regs_pad_uart2_rxd_PCONF0)—Offset 60h” on page 4646	2003CC80h
68–6Bh	4	“Uart2 Rxd Pad Value (cfio_regs_pad_uart2_rxd_PAD_VAL)—Offset 68h” on page 4648	00000002h
70–73h	4	“Uart2 Txd Pad Configuration (cfio_regs_pad_uart2_txd_PCONF0)—Offset 70h” on page 4649	2003CC80h
78–7Bh	4	“Uart2 Txd Pad Value (cfio_regs_pad_uart2_txd_PAD_VAL)—Offset 78h” on page 4652	00000002h
80–83h	4	“Uart2 Cts B Pad Configuration (cfio_regs_pad_uart2_cts_b_PCONF0)—Offset 80h” on page 4652	2003CC80h
88–8Bh	4	“Uart2 Cts B Pad Value (cfio_regs_pad_uart2_cts_b_PAD_VAL)—Offset 88h” on page 4655	00000002h
90–93h	4	“Uart2 Rts B Pad Configuration (cfio_regs_pad_uart2_rts_b_PCONF0)—Offset 90h” on page 4655	2003CC80h
98–9Bh	4	“Uart2 Rts B Pad Value (cfio_regs_pad_uart2_rts_b_PAD_VAL)—Offset 98h” on page 4658	00000002h
A0–A3h	4	“Pwm0 Pad Configuration (cfio_regs_pad_pwm0_PCONF0)—Offset A0h” on page 4659	2003CD00h
A8–ABh	4	“Pwm0 Pad Value (cfio_regs_pad_pwm0_PAD_VAL)—Offset A8h” on page 4661	00000002h
B0–B3h	4	“Pwm1 Pad Configuration (cfio_regs_pad_pwm1_PCONF0)—Offset B0h” on page 4662	2003CD00h
B8–BBh	4	“Pwm1 Pad Value (cfio_regs_pad_pwm1_PAD_VAL)—Offset B8h” on page 4664	00000002h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C0–C3h	4	"Gp Ssp 2 Fs Pad Configuration (cfio_regs_pad_gp_ssp_2_fs_PCONF0)—Offset C0h" on page 4665	2003CC80h
C8–CBh	4	"Gp Ssp 2 Fs Pad Value (cfio_regs_pad_gp_ssp_2_fs_PAD_VAL)—Offset C8h" on page 4667	00000002h
D0–D3h	4	"Gp Ssp 2 Clk Pad Configuration (cfio_regs_pad_gp_ssp_2_clk_PCONF0)—Offset D0h" on page 4668	2003CD00h
D8–DBh	4	"Gp Ssp 2 Clk Pad Value (cfio_regs_pad_gp_ssp_2_clk_PAD_VAL)—Offset D8h" on page 4671	00000002h
E0–E3h	4	"Gp Ssp 2 Txd Pad Configuration (cfio_regs_pad_gp_ssp_2_txd_PCONF0)—Offset E0h" on page 4671	2003CC80h
E8–EBh	4	"Gp Ssp 2 Txd Pad Value (cfio_regs_pad_gp_ssp_2_txd_PAD_VAL)—Offset E8h" on page 4674	00000002h
F0–F3h	4	"Gp Ssp 2 Rxd Pad Configuration (cfio_regs_pad_gp_ssp_2_rxd_PCONF0)—Offset F0h" on page 4674	2003CD00h
F8–FBh	4	"Gp Ssp 2 Rxd Pad Value (cfio_regs_pad_gp_ssp_2_rxd_PAD_VAL)—Offset F8h" on page 4677	00000002h
100–103h	4	"Spi1 Clk Pad Configuration (cfio_regs_pad_spi1_clk_PCONF0)—Offset 100h" on page 4678	2003CD00h
108–10Bh	4	"Spi1 Clk Pad Value (cfio_regs_pad_spi1_clk_PAD_VAL)—Offset 108h" on page 4680	00000002h
110–113h	4	"Spi1 Cs0 B Pad Configuration (cfio_regs_pad_spi1_cs0_b_PCONF0)—Offset 110h" on page 4681	2003CC80h
118–11Bh	4	"Spi1 Cs0 B Pad Value (cfio_regs_pad_spi1_cs0_b_PAD_VAL)—Offset 118h" on page 4683	00000002h
120–123h	4	"Spi1 Miso Pad Configuration (cfio_regs_pad_spi1_miso_PCONF0)—Offset 120h" on page 4684	2003CC80h
128–12Bh	4	"Spi1 Miso Pad Value (cfio_regs_pad_spi1_miso_PAD_VAL)—Offset 128h" on page 4687	00000002h
130–133h	4	"Spi1 Mosi Pad Configuration (cfio_regs_pad_spi1_mosi_PCONF0)—Offset 130h" on page 4687	2003CC80h
138–13Bh	4	"Spi1 Mosi Pad Value (cfio_regs_pad_spi1_mosi_PAD_VAL)—Offset 138h" on page 4690	00000002h
140–143h	4	"I2c5 Scl Pad Configuration (cfio_regs_pad_i2c5_scl_PCONF0)—Offset 140h" on page 4690	2003CC80h
148–14Bh	4	"I2c5 Scl Pad Value (cfio_regs_pad_i2c5_scl_PAD_VAL)—Offset 148h" on page 4693	00000002h
150–153h	4	"I2c5 Sda Pad Configuration (cfio_regs_pad_i2c5_sda_PCONF0)—Offset 150h" on page 4694	2003CC80h
158–15Bh	4	"I2c5 Sda Pad Value (cfio_regs_pad_i2c5_sda_PAD_VAL)—Offset 158h" on page 4696	00000002h
160–163h	4	"I2c6 Scl Pad Configuration (cfio_regs_pad_i2c6_scl_PCONF0)—Offset 160h" on page 4697	2003CC80h
168–16Bh	4	"I2c6 Scl Pad Value (cfio_regs_pad_i2c6_scl_PAD_VAL)—Offset 168h" on page 4699	00000002h
170–173h	4	"I2c4 Scl Pad Configuration (cfio_regs_pad_i2c4_scl_PCONF0)—Offset 170h" on page 4700	2003CC80h
178–17Bh	4	"I2c4 Scl Pad Value (cfio_regs_pad_i2c4_scl_PAD_VAL)—Offset 178h" on page 4703	00000002h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
180–183h	4	"I2c6 Sda Pad Configuration (cfio_regs_pad_i2c6_sda_PCONF0)—Offset 180h" on page 4703	2003CC80h
188–18Bh	4	"I2c6 Sda Pad Value (cfio_regs_pad_i2c6_sda_PAD_VAL)—Offset 188h" on page 4706	00000002h
190–193h	4	"I2c3 Sda Pad Configuration (cfio_regs_pad_i2c3_sda_PCONF0)—Offset 190h" on page 4706	2003CC80h
198–19Bh	4	"I2c3 Sda Pad Value (cfio_regs_pad_i2c3_sda_PAD_VAL)—Offset 198h" on page 4709	00000002h
1A0–1A3h	4	"I2c4 Sda Pad Configuration (cfio_regs_pad_i2c4_sda_PCONF0)—Offset 1A0h" on page 4710	2003CC80h
1A8–1ABh	4	"I2c4 Sda Pad Value (cfio_regs_pad_i2c4_sda_PAD_VAL)—Offset 1A8h" on page 4712	00000002h
1B0–1B3h	4	"I2c2 Scl Pad Configuration (cfio_regs_pad_i2c2_scl_PCONF0)—Offset 1B0h" on page 4713	2003CC80h
1B8–1BBh	4	"I2c2 Scl Pad Value (cfio_regs_pad_i2c2_scl_PAD_VAL)—Offset 1B8h" on page 4715	00000002h
1C0–1C3h	4	"I2c3 Scl Pad Configuration (cfio_regs_pad_i2c3_scl_PCONF0)—Offset 1C0h" on page 4716	2003CC80h
1C8–1CBh	4	"I2c3 Scl Pad Value (cfio_regs_pad_i2c3_scl_PAD_VAL)—Offset 1C8h" on page 4719	00000002h
1D0–1D3h	4	"I2c2 Sda Pad Configuration (cfio_regs_pad_i2c2_sda_PCONF0)—Offset 1D0h" on page 4719	2003CC80h
1D8–1DBh	4	"I2c2 Sda Pad Value (cfio_regs_pad_i2c2_sda_PAD_VAL)—Offset 1D8h" on page 4722	00000002h
1E0–1E3h	4	"I2c1 Scl Pad Configuration (cfio_regs_pad_i2c1_scl_PCONF0)—Offset 1E0h" on page 4722	2003CC80h
1E8–1EBh	4	"I2c1 Scl Pad Value (cfio_regs_pad_i2c1_scl_PAD_VAL)—Offset 1E8h" on page 4725	00000002h
1F0–1F3h	4	"I2c1 Sda Pad Configuration (cfio_regs_pad_i2c1_sda_PCONF0)—Offset 1F0h" on page 4726	2003CC80h
1F8–1FBh	4	"I2c1 Sda Pad Value (cfio_regs_pad_i2c1_sda_PAD_VAL)—Offset 1F8h" on page 4728	00000002h
200–203h	4	"I2c0 Scl Pad Configuration (cfio_regs_pad_i2c0_scl_PCONF0)—Offset 200h" on page 4729	2003CC80h
208–20Bh	4	"I2c0 Scl Pad Value (cfio_regs_pad_i2c0_scl_PAD_VAL)—Offset 208h" on page 4731	00000002h
210–213h	4	"I2c0 Sda Pad Configuration (cfio_regs_pad_i2c0_sda_PCONF0)—Offset 210h" on page 4732	2003CC80h
218–21Bh	4	"I2c0 Sda Pad Value (cfio_regs_pad_i2c0_sda_PAD_VAL)—Offset 218h" on page 4735	00000002h
220–223h	4	"Hda Rstb Pad Configuration (cfio_regs_pad_hda_rstb_PCONF0)—Offset 220h" on page 4735	2003ED00h
228–22Bh	4	"Hda Rstb Pad Value (cfio_regs_pad_hda_rstb_PAD_VAL)—Offset 228h" on page 4738	00000002h
230–233h	4	"Hda Sdi1 Pad Configuration (cfio_regs_pad_hda_sdi1_PCONF0)—Offset 230h" on page 4738	2003ED00h
238–23Bh	4	"Hda Sdi1 Pad Value (cfio_regs_pad_hda_sdi1_PAD_VAL)—Offset 238h" on page 4741	00000002h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
240–243h	4	"Hda Clk Pad Configuration (cfio_regs_pad_hda_clk_PCONF0)—Offset 240h" on page 4742	2003ED00h
248–24Bh	4	"Hda Clk Pad Value (cfio_regs_pad_hda_clk_PAD_VAL)—Offset 248h" on page 4744	00000002h
250–253h	4	"Hda Sync Pad Configuration (cfio_regs_pad_hda_sync_PCONF0)—Offset 250h" on page 4745	2003ED00h
258–25Bh	4	"Hda Sync Pad Value (cfio_regs_pad_hda_sync_PAD_VAL)—Offset 258h" on page 4747	00000002h
260–263h	4	"Hda Sdo Pad Configuration (cfio_regs_pad_hda_sdo_PCONF0)—Offset 260h" on page 4748	2003ED00h
268–26Bh	4	"Hda Sdo Pad Value (cfio_regs_pad_hda_sdo_PAD_VAL)—Offset 268h" on page 4751	00000002h
270–273h	4	"Hda Sdi0 Pad Configuration (cfio_regs_pad_hda_sdi0_PCONF0)—Offset 270h" on page 4751	2003ED00h
278–27Bh	4	"Hda Sdi0 Pad Value (cfio_regs_pad_hda_sdi0_PAD_VAL)—Offset 278h" on page 4754	00000002h
280–283h	4	"Hda Dockrstb Pad Configuration (cfio_regs_pad_hda_dockrstb_PCONF0)—Offset 280h" on page 4754	2003ED00h
288–28Bh	4	"Hda Dockrstb Pad Value (cfio_regs_pad_hda_dockrstb_PAD_VAL)—Offset 288h" on page 4757	00000002h
290–293h	4	"Sdmmc3 D1 Pad Configuration (cfio_regs_pad_sdmmc3_d1_PCONF0)—Offset 290h" on page 4758	20038C80h
298–29Bh	4	"Sdmmc3 D1 Pad Value (cfio_regs_pad_sdmmc3_d1_PAD_VAL)—Offset 298h" on page 4760	00000002h
2A0–2A3h	4	"Sdmmc3 D3 Pad Configuration (cfio_regs_pad_sdmmc3_d3_PCONF0)—Offset 2A0h" on page 4761	20038C80h
2A8–2ABh	4	"Sdmmc3 D3 Pad Value (cfio_regs_pad_sdmmc3_d3_PAD_VAL)—Offset 2A8h" on page 4763	00000002h
2B0–2B3h	4	"Sdmmc3 Clk Pad Configuration (cfio_regs_pad_sdmmc3_clk_PCONF0)—Offset 2B0h" on page 4763	20038D00h
2B4–2B7h	4	"Sdmmc3 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc3_clk_PCONF1)—Offset 2B4h" on page 4765	00008000h
2B8–2BBh	4	"Sdmmc3 Clk Pad Value (cfio_regs_pad_sdmmc3_clk_PAD_VAL)—Offset 2B8h" on page 4766	00000002h
2C0–2C3h	4	"Sdmmc3 Cmd Pad Configuration (cfio_regs_pad_sdmmc3_cmd_PCONF0)—Offset 2C0h" on page 4767	20038C80h
2C8–2CBh	4	"Sdmmc3 Cmd Pad Value (cfio_regs_pad_sdmmc3_cmd_PAD_VAL)—Offset 2C8h" on page 4769	00000002h
2D0–2D3h	4	"Sdmmc3 D2 Pad Configuration (cfio_regs_pad_sdmmc3_d2_PCONF0)—Offset 2D0h" on page 4770	20038C80h
2D8–2DBh	4	"Sdmmc3 D2 Pad Value (cfio_regs_pad_sdmmc3_d2_PAD_VAL)—Offset 2D8h" on page 4772	00000002h
2E0–2E3h	4	"Sdmmc3 D0 Pad Configuration (cfio_regs_pad_sdmmc3_d0_PCONF0)—Offset 2E0h" on page 4772	20038C80h
2E8–2EBh	4	"Sdmmc3 D0 Pad Value (cfio_regs_pad_sdmmc3_d0_PAD_VAL)—Offset 2E8h" on page 4774	00000002h
2F0–2F3h	4	"Sdmmc2 D1 Pad Configuration (cfio_regs_pad_sdmmc2_d1_PCONF0)—Offset 2F0h" on page 4775	2003EC80h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2F8–2FBh	4	"Sdmmc2 D1 Pad Value (cfio_regs_pad_sdmmc2_d1_PAD_VAL)—Offset 2F8h" on page 4778	00000002h
300–303h	4	"Sdmmc2 Cmd Pad Configuration (cfio_regs_pad_sdmmc2_cmd_PCONF0)—Offset 300h" on page 4778	2003EC80h
308–30Bh	4	"Sdmmc2 Cmd Pad Value (cfio_regs_pad_sdmmc2_cmd_PAD_VAL)—Offset 308h" on page 4781	00000002h
310–313h	4	"Sdmmc2 D3 Cd B Pad Configuration (cfio_regs_pad_sdmmc2_d3_cd_b_PCONF0)—Offset 310h" on page 4781	2003EC80h
318–31Bh	4	"Sdmmc2 D3 Cd B Pad Value (cfio_regs_pad_sdmmc2_d3_cd_b_PAD_VAL)—Offset 318h" on page 4784	00000002h
320–323h	4	"Sdmmc2 Clk Pad Configuration (cfio_regs_pad_sdmmc2_clk_PCONF0)—Offset 320h" on page 4785	2003ED00h
324–327h	4	"Sdmmc2 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc2_clk_PCONF1)—Offset 324h" on page 4787	00008000h
328–32Bh	4	"Sdmmc2 Clk Pad Value (cfio_regs_pad_sdmmc2_clk_PAD_VAL)—Offset 328h" on page 4788	00000002h
330–333h	4	"Mmc1 Reset B Pad Configuration (cfio_regs_pad_mmc1_reset_b_PCONF0)—Offset 330h" on page 4788	2003ED00h
338–33Bh	4	"Mmc1 Reset B Pad Value (cfio_regs_pad_mmc1_reset_b_PAD_VAL)—Offset 338h" on page 4791	00000002h
340–343h	4	"Sdmmc2 D2 Pad Configuration (cfio_regs_pad_sdmmc2_d2_PCONF0)—Offset 340h" on page 4791	2003EC80h
348–34Bh	4	"Sdmmc2 D2 Pad Value (cfio_regs_pad_sdmmc2_d2_PAD_VAL)—Offset 348h" on page 4794	00000002h
350–353h	4	"Sdmmc2 D0 Pad Configuration (cfio_regs_pad_sdmmc2_d0_PCONF0)—Offset 350h" on page 4795	2003EC80h
358–35Bh	4	"Sdmmc2 D0 Pad Value (cfio_regs_pad_sdmmc2_d0_PAD_VAL)—Offset 358h" on page 4797	00000002h
360–363h	4	"Sdmmc1 D3 Cd B Pad Configuration (cfio_regs_pad_sdmmc1_d3_cd_b_PCONF0)—Offset 360h" on page 4798	2003EC80h
368–36Bh	4	"Sdmmc1 D3 Cd B Pad Value (cfio_regs_pad_sdmmc1_d3_cd_b_PAD_VAL)—Offset 368h" on page 4800	00000002h
370–373h	4	"Mmc1 D6 Pad Configuration (cfio_regs_pad_mmc1_d6_PCONF0)—Offset 370h" on page 4801	2003EC80h
378–37Bh	4	"Mmc1 D6 Pad Value (cfio_regs_pad_mmc1_d6_PAD_VAL)—Offset 378h" on page 4804	00000002h
380–383h	4	"Mmc1 D4 Sd We Pad Configuration (cfio_regs_pad_mmc1_d4_sd_we_PCONF0)—Offset 380h" on page 4804	2003EC80h
388–38Bh	4	"Mmc1 D4 Sd We Pad Value (cfio_regs_pad_mmc1_d4_sd_we_PAD_VAL)—Offset 388h" on page 4807	00000002h
390–393h	4	"Sdmmc1 Cmd Pad Configuration (cfio_regs_pad_sdmmc1_cmd_PCONF0)—Offset 390h" on page 4807	2003EC80h
398–39Bh	4	"Sdmmc1 Cmd Pad Value (cfio_regs_pad_sdmmc1_cmd_PAD_VAL)—Offset 398h" on page 4810	00000002h
3A0–3A3h	4	"Sdmmc3 Cd B Pad Configuration (cfio_regs_pad_sdmmc3_cd_b_PCONF0)—Offset 3A0h" on page 4811	2003CC80h
3A8–3ABh	4	"Sdmmc3 Cd B Pad Value (cfio_regs_pad_sdmmc3_cd_b_PAD_VAL)—Offset 3A8h" on page 4813	00000002h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3B0–3B3h	4	"Sdmmc1 D2 Pad Configuration (cfio_regs_pad_sdmmc1_d2_PCONF0)—Offset 3B0h" on page 4814	2003EC80h
3B8–3BBh	4	"Sdmmc1 D2 Pad Value (cfio_regs_pad_sdmmc1_d2_PAD_VAL)—Offset 3B8h" on page 4816	00000002h
3C0–3C3h	4	"Mmc1 D5 Pad Configuration (cfio_regs_pad_mmc1_d5_PCONF0)—Offset 3C0h" on page 4817	2003EC80h
3C8–3CBh	4	"Mmc1 D5 Pad Value (cfio_regs_pad_mmc1_d5_PAD_VAL)—Offset 3C8h" on page 4820	00000002h
3D0–3D3h	4	"Sdmmc1 D0 Pad Configuration (cfio_regs_pad_sdmmc1_d0_PCONF0)—Offset 3D0h" on page 4820	2003EC80h
3D8–3DBh	4	"Sdmmc1 D0 Pad Value (cfio_regs_pad_sdmmc1_d0_PAD_VAL)—Offset 3D8h" on page 4823	00000002h
3E0–3E3h	4	"Sdmmc1 Clk Pad Configuration (cfio_regs_pad_sdmmc1_clk_PCONF0)—Offset 3E0h" on page 4823	2003ED00h
3E4–3E7h	4	"Sdmmc1 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc1_clk_PCONF1)—Offset 3E4h" on page 4826	00008000h
3E8–3EBh	4	"Sdmmc1 Clk Pad Value (cfio_regs_pad_sdmmc1_clk_PAD_VAL)—Offset 3E8h" on page 4826	00000002h
3F0–3F3h	4	"Mmc1 D7 Pad Configuration (cfio_regs_pad_mmc1_d7_PCONF0)—Offset 3F0h" on page 4827	2003EC80h
3F8–3FBh	4	"Mmc1 D7 Pad Value (cfio_regs_pad_mmc1_d7_PAD_VAL)—Offset 3F8h" on page 4830	00000002h
400–403h	4	"Sdmmc1 D1 Pad Configuration (cfio_regs_pad_sdmmc1_d1_PCONF0)—Offset 400h" on page 4830	2003EC80h
408–40Bh	4	"Sdmmc1 D1 Pad Value (cfio_regs_pad_sdmmc1_d1_PAD_VAL)—Offset 408h" on page 4833	00000002h
410–413h	4	"Lpc Clkout1 Pad Configuration (cfio_regs_pad_lpc_clkout1_PCONF0)—Offset 410h" on page 4834	20038D00h
418–41Bh	4	"Lpc Clkout1 Pad Value (cfio_regs_pad_lpc_clkout1_PAD_VAL)—Offset 418h" on page 4836	00000002h
420–423h	4	"Lpc Ad3 Pad Configuration (cfio_regs_pad_lpc_ad3_PCONF0)—Offset 420h" on page 4836	20038C80h
428–42Bh	4	"Lpc Ad3 Pad Value (cfio_regs_pad_lpc_ad3_PAD_VAL)—Offset 428h" on page 4838	00000002h
430–433h	4	"Lpc Ad2 Pad Configuration (cfio_regs_pad_lpc_ad2_PCONF0)—Offset 430h" on page 4839	20038C80h
438–43Bh	4	"Lpc Ad2 Pad Value (cfio_regs_pad_lpc_ad2_PAD_VAL)—Offset 438h" on page 4841	00000002h
440–443h	4	"Lpc Ad1 Pad Configuration (cfio_regs_pad_lpc_ad1_PCONF0)—Offset 440h" on page 4842	20038C80h
448–44Bh	4	"Lpc Ad1 Pad Value (cfio_regs_pad_lpc_ad1_PAD_VAL)—Offset 448h" on page 4844	00000002h
450–453h	4	"Lpc Frameb Pad Configuration (cfio_regs_pad_lpc_frameb_PCONF0)—Offset 450h" on page 4845	20038C80h
458–45Bh	4	"Lpc Frameb Pad Value (cfio_regs_pad_lpc_frameb_PAD_VAL)—Offset 458h" on page 4847	00000002h
460–463h	4	"Lpc Ad0 Pad Configuration (cfio_regs_pad_lpc_ad0_PCONF0)—Offset 460h" on page 4848	20038C80h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
468–46Bh	4	"Lpc Ad0 Pad Value (cfio_regs_pad_lpc_ad0_PAD_VAL)—Offset 468h" on page 4850	00000002h
470–473h	4	"Lpc Clkout0 Pad Configuration (cfio_regs_pad_lpc_clkout0_PCONF0)—Offset 470h" on page 4850	20038D00h
478–47Bh	4	"Lpc Clkout0 Pad Value (cfio_regs_pad_lpc_clkout0_PAD_VAL)—Offset 478h" on page 4852	00000002h
480–483h	4	"Lpc Clkrunb Pad Configuration (cfio_regs_pad_lpc_clkrunb_PCONF0)—Offset 480h" on page 4853	20038C80h
488–48Bh	4	"Lpc Clkrunb Pad Value (cfio_regs_pad_lpc_clkrunb_PAD_VAL)—Offset 488h" on page 4855	00000002h
490–493h	4	"Hv Crt Ddc Clk Pad Configuration (cfio_regs_pad_hv_crt_ddc_clk_PCONF0)—Offset 490h" on page 4856	2003C800h
498–49Bh	4	"Hv Crt Ddc Clk Pad Value (cfio_regs_pad_hv_crt_ddc_clk_PAD_VAL)—Offset 498h" on page 4858	00000002h
4A0–4A3h	4	"Hv Crt Vsync Pad Configuration (cfio_regs_pad_hv_crt_vsync_PCONF0)—Offset 4A0h" on page 4859	20038800h
4A8–4ABh	4	"Hv Crt Vsync Pad Value (cfio_regs_pad_hv_crt_vsync_PAD_VAL)—Offset 4A8h" on page 4861	00000002h
4B0–4B3h	4	"Hv Crt Hsync Pad Configuration (cfio_regs_pad_hv_crt_hsync_PCONF0)—Offset 4B0h" on page 4862	20038800h
4B8–4BBh	4	"Hv Crt Hsync Pad Value (cfio_regs_pad_hv_crt_hsync_PAD_VAL)—Offset 4B8h" on page 4864	00000002h
4C0–4C3h	4	"Hv Crt Ddc Data Pad Configuration (cfio_regs_pad_hv_crt_ddc_data_PCONF0)—Offset 4C0h" on page 4865	2003C800h
4C8–4CBh	4	"Hv Crt Ddc Data Pad Value (cfio_regs_pad_hv_crt_ddc_data_PAD_VAL)—Offset 4C8h" on page 4867	00000002h
4D0–4D3h	4	"Mhsi Acdata Pad Configuration (cfio_regs_pad_mhsi_acdata_PCONF0)—Offset 4D0h" on page 4868	2003CD00h
4D8–4DBh	4	"Mhsi Acdata Pad Value (cfio_regs_pad_mhsi_acdata_PAD_VAL)—Offset 4D8h" on page 4871	00000002h
4E0–4E3h	4	"Mhsi Acwake Pad Configuration (cfio_regs_pad_mhsi_acwake_PCONF0)—Offset 4E0h" on page 4871	2003CD00h
4E8–4EBh	4	"Mhsi Acwake Pad Value (cfio_regs_pad_mhsi_acwake_PAD_VAL)—Offset 4E8h" on page 4874	00000002h
4F0–4F3h	4	"Mhsi Acflag Pad Configuration (cfio_regs_pad_mhsi_acflag_PCONF0)—Offset 4F0h" on page 4875	2003CC80h
4F8–4FBh	4	"Mhsi Acflag Pad Value (cfio_regs_pad_mhsi_acflag_PAD_VAL)—Offset 4F8h" on page 4877	00000002h
500–503h	4	"Mhsi Caflag Pad Configuration (cfio_regs_pad_mhsi_caflag_PCONF0)—Offset 500h" on page 4878	2003CD00h
504–507h	4	"Mhsi Caflag Delay Line Multiplexer (cfio_regs_pad_mhsi_caflag_PCONF1)—Offset 504h" on page 4880	00008000h
508–50Bh	4	"Mhsi Caflag Pad Value (cfio_regs_pad_mhsi_caflag_PAD_VAL)—Offset 508h" on page 4881	00000002h
510–513h	4	"Mhsi Cadata Pad Configuration (cfio_regs_pad_mhsi_cadata_PCONF0)—Offset 510h" on page 4882	2003CD00h
514–517h	4	"Mhsi Cadata Delay Line Multiplexer (cfio_regs_pad_mhsi_cadata_PCONF1)—Offset 514h" on page 4884	00008000h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
518–51Bh	4	"Mhsi Cadata Pad Value (cfio_regs_pad_mhsi_cadata_PAD_VAL)—Offset 518h" on page 4885	00000002h
520–523h	4	"Mhsi Caready Pad Configuration (cfio_regs_pad_mhsi_caready_PCONF0)—Offset 520h" on page 4885	2003CC80h
528–52Bh	4	"Mhsi Caready Pad Value (cfio_regs_pad_mhsi_caready_PAD_VAL)—Offset 528h" on page 4888	00000002h
530–533h	4	"Mhsi Acready Pad Configuration (cfio_regs_pad_mhsi_acready_PCONF0)—Offset 530h" on page 4888	2003CD00h
538–53Bh	4	"Mhsi Acready Pad Value (cfio_regs_pad_mhsi_acready_PAD_VAL)—Offset 538h" on page 4891	00000002h
540–543h	4	"Hda Dockenb Pad Configuration (cfio_regs_pad_hda_dockenb_PCONF0)—Offset 540h" on page 4892	2003CD00h
548–54Bh	4	"Hda Dockenb Pad Value (cfio_regs_pad_hda_dockenb_PAD_VAL)—Offset 548h" on page 4894	00000002h
550–553h	4	"Sata Gp0 Pad Configuration (cfio_regs_pad_sata_gp0_PCONF0)—Offset 550h" on page 4895	2003CD00h
558–55Bh	4	"Sata Gp0 Pad Value (cfio_regs_pad_sata_gp0_PAD_VAL)—Offset 558h" on page 4897	00000002h
560–563h	4	"Ilb Serirq Pad Configuration (cfio_regs_pad_ilb_serirq_PCONF0)—Offset 560h" on page 4898	2003CC80h
568–56Bh	4	"Ilb Serirq Pad Value (cfio_regs_pad_ilb_serirq_PAD_VAL)—Offset 568h" on page 4901	00000002h
570–573h	4	"Plt Clk1 Pad Configuration (cfio_regs_pad_plt_clk1_PCONF0)—Offset 570h" on page 4901	2003CD00h
578–57Bh	4	"Plt Clk1 Pad Value (cfio_regs_pad_plt_clk1_PAD_VAL)—Offset 578h" on page 4904	00000002h
580–583h	4	"Smb Clk Pad Configuration (cfio_regs_pad_smb_clk_PCONF0)—Offset 580h" on page 4904	2003CC80h
588–58Bh	4	"Smb Clk Pad Value (cfio_regs_pad_smb_clk_PAD_VAL)—Offset 588h" on page 4907	00000002h
590–593h	4	"Sata Gp1 Pad Configuration (cfio_regs_pad_sata_gp1_PCONF0)—Offset 590h" on page 4908	2003CD00h
598–59Bh	4	"Sata Gp1 Pad Value (cfio_regs_pad_sata_gp1_PAD_VAL)—Offset 598h" on page 4910	00000002h
5A0–5A3h	4	"Smb Data Pad Configuration (cfio_regs_pad_smb_data_PCONF0)—Offset 5A0h" on page 4911	2003CC80h
5A8–5ABh	4	"Smb Data Pad Value (cfio_regs_pad_smb_data_PAD_VAL)—Offset 5A8h" on page 4913	00000002h
5B0–5B3h	4	"Plt Clk2 Pad Configuration (cfio_regs_pad_plt_clk2_PCONF0)—Offset 5B0h" on page 4914	2003CD00h
5B8–5BBh	4	"Plt Clk2 Pad Value (cfio_regs_pad_plt_clk2_PAD_VAL)—Offset 5B8h" on page 4917	00000002h
5C0–5C3h	4	"Smb Alertb Pad Configuration (cfio_regs_pad_smb_alertb_PCONF0)—Offset 5C0h" on page 4917	2003CC80h
5C8–5CBh	4	"Smb Alertb Pad Value (cfio_regs_pad_smb_alertb_PAD_VAL)—Offset 5C8h" on page 4920	00000002h
5D0–5D3h	4	"Sata Ledn Pad Configuration (cfio_regs_pad_sata_ledn_PCONF0)—Offset 5D0h" on page 4920	2003CC80h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5D8–5DBh	4	"Sata Ledn Pad Value (cfio_regs_pad_sata_ledn_PAD_VAL)—Offset 5D8h" on page 4923	00000002h
5E0–5E3h	4	"Pmu Resetbutton B Pad Configuration (cfio_regs_pad_pmu_resetbutton_b_PCONF0)—Offset 5E0h" on page 4924	2003CC80h
5E8–5EBh	4	"Pmu Resetbutton B Pad Value (cfio_regs_pad_pmu_resetbutton_b_PAD_VAL)—Offset 5E8h" on page 4926	00000006h
5EC–5EFh	4	"Pmu Resetbutton B Pad Test (cfio_regs_pad_pmu_resetbutton_b_PAD_DFT)—Offset 5ECh" on page 4927	00000400h
5F0–5F3h	4	"Sdmmc3 1p8 En Pad Configuration (cfio_regs_pad_sdmmc3_1p8_en_PCONF0)—Offset 5F0h" on page 4928	2003CD00h
5F8–5FBh	4	"Sdmmc3 1p8 En Pad Value (cfio_regs_pad_sdmmc3_1p8_en_PAD_VAL)—Offset 5F8h" on page 4930	00000002h
600–603h	4	"Pcie Clkreq0b Pad Configuration (cfio_regs_pad_pcie_clkreq0b_PCONF0)—Offset 600h" on page 4931	2003CC80h
608–60Bh	4	"Pcie Clkreq0b Pad Value (cfio_regs_pad_pcie_clkreq0b_PAD_VAL)—Offset 608h" on page 4934	00000002h
610–613h	4	"Plt Clk4 Pad Configuration (cfio_regs_pad_plt_clk4_PCONF0)—Offset 610h" on page 4934	2003CD00h
618–61Bh	4	"Plt Clk4 Pad Value (cfio_regs_pad_plt_clk4_PAD_VAL)—Offset 618h" on page 4937	00000002h
620–623h	4	"Pcie Clkreq3b Pad Configuration (cfio_regs_pad_pcie_clkreq3b_PCONF0)—Offset 620h" on page 4937	2003CC80h
628–62Bh	4	"Pcie Clkreq3b Pad Value (cfio_regs_pad_pcie_clkreq3b_PAD_VAL)—Offset 628h" on page 4940	00000002h
630–633h	4	"Pcie Clkreq1b Pad Configuration (cfio_regs_pad_pcie_clkreq1b_PCONF0)—Offset 630h" on page 4941	2003CC80h
638–63Bh	4	"Pcie Clkreq1b Pad Value (cfio_regs_pad_pcie_clkreq1b_PAD_VAL)—Offset 638h" on page 4943	00000002h
640–643h	4	"Plt Clk5 Pad Configuration (cfio_regs_pad_plt_clk5_PCONF0)—Offset 640h" on page 4944	2003CD00h
648–64Bh	4	"Plt Clk5 Pad Value (cfio_regs_pad_plt_clk5_PAD_VAL)—Offset 648h" on page 4946	00000002h
650–653h	4	"Pcie Clkreq4b Pad Configuration (cfio_regs_pad_pcie_clkreq4b_PCONF0)—Offset 650h" on page 4947	2003CC80h
658–65Bh	4	"Pcie Clkreq4b Pad Value (cfio_regs_pad_pcie_clkreq4b_PAD_VAL)—Offset 658h" on page 4950	00000002h
660–663h	4	"Pcie Clkreq2b Pad Configuration (cfio_regs_pad_pcie_clkreq2b_PCONF0)—Offset 660h" on page 4950	2003CC80h
668–66Bh	4	"Pcie Clkreq2b Pad Value (cfio_regs_pad_pcie_clkreq2b_PAD_VAL)—Offset 668h" on page 4953	00000002h
670–673h	4	"Spkr Pad Configuration (cfio_regs_pad_spkr_PCONF0)—Offset 670h" on page 4953	2003CC80h
678–67Bh	4	"Spkr Pad Value (cfio_regs_pad_spkr_PAD_VAL)—Offset 678h" on page 4956	00000002h
680–683h	4	"Plt Clk3 Pad Configuration (cfio_regs_pad_plt_clk3_PCONF0)—Offset 680h" on page 4957	2003CD00h
688–68Bh	4	"Plt Clk3 Pad Value (cfio_regs_pad_plt_clk3_PAD_VAL)—Offset 688h" on page 4959	00000002h
690–693h	4	"Sdmmc3 Pwr En B Pad Configuration (cfio_regs_pad_sdmmc3_pwr_en_b_PCONF0)—Offset 690h" on page 4960	2003CC80h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
698–69Bh	4	"Sdmmc3 Pwr En B Pad Value (cfio_regs_pad_sdmmc3_pwr_en_b_PAD_VAL)—Offset 698h" on page 4962	00000002h
6A0–6A3h	4	"Plt Clk0 Pad Configuration (cfio_regs_pad_plt_clk0_PCONF0)—Offset 6A0h" on page 4963	2003CD00h
6A8–6ABh	4	"Plt Clk0 Pad Value (cfio_regs_pad_plt_clk0_PAD_VAL)—Offset 6A8h" on page 4966	00000002h
6B0–6B3h	4	"Vgpio 0 Pad Configuration (cfio_regs_pad_vgpio_0_PCONF0)—Offset 6B0h" on page 4966	20038800h
6B8–6BBh	4	"Vgpio 0 Pad Value (cfio_regs_pad_vgpio_0_PAD_VAL)—Offset 6B8h" on page 4968	00000004h
6C0–6C3h	4	"Vgpio 1 Pad Configuration (cfio_regs_pad_vgpio_1_PCONF0)—Offset 6C0h" on page 4969	20038800h
6C8–6CBh	4	"Vgpio 1 Pad Value (cfio_regs_pad_vgpio_1_PAD_VAL)—Offset 6C8h" on page 4971	00000004h
6D0–6D3h	4	"Vgpio 2 Pad Configuration (cfio_regs_pad_vgpio_2_PCONF0)—Offset 6D0h" on page 4972	20038800h
6D8–6DBh	4	"Vgpio 2 Pad Value (cfio_regs_pad_vgpio_2_PAD_VAL)—Offset 6D8h" on page 4974	00000004h
6E0–6E3h	4	"Vgpio 3 Pad Configuration (cfio_regs_pad_vgpio_3_PCONF0)—Offset 6E0h" on page 4975	20038800h
6E8–6EBh	4	"Vgpio 3 Pad Value (cfio_regs_pad_vgpio_3_PAD_VAL)—Offset 6E8h" on page 4977	00000004h
6F0–6F3h	4	"Vgpio 4 Pad Configuration (cfio_regs_pad_vgpio_4_PCONF0)—Offset 6F0h" on page 4978	20038800h
6F8–6FBh	4	"Vgpio 4 Pad Value (cfio_regs_pad_vgpio_4_PAD_VAL)—Offset 6F8h" on page 4980	00000006h
700–703h	4	"Vgpio 5 Pad Configuration (cfio_regs_pad_vgpio_5_PCONF0)—Offset 700h" on page 4980	20038800h
708–70Bh	4	"Vgpio 5 Pad Value (cfio_regs_pad_vgpio_5_PAD_VAL)—Offset 708h" on page 4982	00000004h
710–713h	4	"Vgpio 6 Pad Configuration (cfio_regs_pad_vgpio_6_PCONF0)—Offset 710h" on page 4983	20038800h
718–71Bh	4	"Vgpio 6 Pad Value (cfio_regs_pad_vgpio_6_PAD_VAL)—Offset 718h" on page 4985	00000004h
720–723h	4	"Vgpio 7 Pad Configuration (cfio_regs_pad_vgpio_7_PCONF0)—Offset 720h" on page 4986	20038800h
728–72Bh	4	"Vgpio 7 Pad Value (cfio_regs_pad_vgpio_7_PAD_VAL)—Offset 728h" on page 4988	00000004h
730–733h	4	"Vgpio 8 Pad Configuration (cfio_regs_pad_vgpio_8_PCONF0)—Offset 730h" on page 4989	20038800h
738–73Bh	4	"Vgpio 8 Pad Value (cfio_regs_pad_vgpio_8_PAD_VAL)—Offset 738h" on page 4991	00000004h
740–743h	4	"Vgpio 9 Pad Configuration (cfio_regs_pad_vgpio_9_PCONF0)—Offset 740h" on page 4992	20038800h
748–74Bh	4	"Vgpio 9 Pad Value (cfio_regs_pad_vgpio_9_PAD_VAL)—Offset 748h" on page 4994	00000004h
750–753h	4	"Vgpio 10 Pad Configuration (cfio_regs_pad_vgpio_10_PCONF0)—Offset 750h" on page 4994	20038800h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
758–75Bh	4	"Vgpio 10 Pad Value (cfio_regs_pad_vgpio_10_PAD_VAL)—Offset 758h" on page 4996	00000004h
760–763h	4	"Vgpio 11 Pad Configuration (cfio_regs_pad_vgpio_11_PCONF0)—Offset 760h" on page 4997	20038800h
768–76Bh	4	"Vgpio 11 Pad Value (cfio_regs_pad_vgpio_11_PAD_VAL)—Offset 768h" on page 4999	00000004h
770–773h	4	"Vgpio 12 Pad Configuration (cfio_regs_pad_vgpio_12_PCONF0)—Offset 770h" on page 5000	20038800h
778–77Bh	4	"Vgpio 12 Pad Value (cfio_regs_pad_vgpio_12_PAD_VAL)—Offset 778h" on page 5002	00000004h
780–783h	4	"Vgpio 13 Pad Configuration (cfio_regs_pad_vgpio_13_PCONF0)—Offset 780h" on page 5003	20038800h
788–78Bh	4	"Vgpio 13 Pad Value (cfio_regs_pad_vgpio_13_PAD_VAL)—Offset 788h" on page 5005	00000004h
790–793h	4	"Vgpio 14 Pad Configuration (cfio_regs_pad_vgpio_14_PCONF0)—Offset 790h" on page 5006	20038800h
798–79Bh	4	"Vgpio 14 Pad Value (cfio_regs_pad_vgpio_14_PAD_VAL)—Offset 798h" on page 5008	00000004h
7A0–7A3h	4	"Vgpio 15 Pad Configuration (cfio_regs_pad_vgpio_15_PCONF0)—Offset 7A0h" on page 5008	20038800h
7A8–7ABh	4	"Vgpio 15 Pad Value (cfio_regs_pad_vgpio_15_PAD_VAL)—Offset 7A8h" on page 5010	00000004h
7B0–7B3h	4	"Vgpio 16 Pad Configuration (cfio_regs_pad_vgpio_16_PCONF0)—Offset 7B0h" on page 5011	20038800h
7B8–7BBh	4	"Vgpio 16 Pad Value (cfio_regs_pad_vgpio_16_PAD_VAL)—Offset 7B8h" on page 5013	00000004h
7C0–7C3h	4	"Vgpio 17 Pad Configuration (cfio_regs_pad_vgpio_17_PCONF0)—Offset 7C0h" on page 5014	20038800h
7C8–7CBh	4	"Vgpio 17 Pad Value (cfio_regs_pad_vgpio_17_PAD_VAL)—Offset 7C8h" on page 5016	00000004h
7D0–7D3h	4	"Vgpio 18 Pad Configuration (cfio_regs_pad_vgpio_18_PCONF0)—Offset 7D0h" on page 5017	20038800h
7D8–7DBh	4	"Vgpio 18 Pad Value (cfio_regs_pad_vgpio_18_PAD_VAL)—Offset 7D8h" on page 5019	00000004h
7E0–7E3h	4	"Vgpio 19 Pad Configuration (cfio_regs_pad_vgpio_19_PCONF0)—Offset 7E0h" on page 5020	20038800h
7E8–7EBh	4	"Vgpio 19 Pad Value (cfio_regs_pad_vgpio_19_PAD_VAL)—Offset 7E8h" on page 5022	00000004h
7F0–7F3h	4	"Vgpio 20 Pad Configuration (cfio_regs_pad_vgpio_20_PCONF0)—Offset 7F0h" on page 5022	20038800h
7F8–7FBh	4	"Vgpio 20 Pad Value (cfio_regs_pad_vgpio_20_PAD_VAL)—Offset 7F8h" on page 5024	00000004h
800–803h	4	"TS0 SCORE Interrupt Status 0 (cfio_regs_REG_TS0_SCORE_IRQ_TS_0)—Offset 800h" on page 5025	00000000h
804–807h	4	"TS1 SCORE Interrupt Status 1 (cfio_regs_REG_TS1_SCORE_IRQ_TS_1)—Offset 804h" on page 5026	00000000h
808–80Bh	4	"TS2 SCORE Interrupt Status 2 (cfio_regs_REG_TS2_SCORE_IRQ_TS_2)—Offset 808h" on page 5027	00000000h

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80C–80Fh	4	"TS3 SCORE Interrupt Status 3 (cfio_regs_REG_TS3_SCORE_IRQ_TS_3)—Offset 80Ch" on page 5028	00000000h
810–813h	4	"C71p1cfiomvscoreaza Compensation Configuration (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_CFG)—Offset 810h" on page 5029	00078080h
81C–81Fh	4	"C71p1cfiomvscoreaza Compensation DFX Override (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_DFX)—Offset 81Ch" on page 5030	01000080h
820–823h	4	"C71p1cfiomvrscoresdio1 Compensation Configuration (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_CFG)—Offset 820h" on page 5031	00078080h
82C–82Fh	4	"C71p1cfiomvrscoresdio1 Compensation DFX Override (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_DFX)—Offset 82Ch" on page 5032	01000080h
830–833h	4	"C71p1cfiohvrscorepsdio3 Compensation Configuration (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_CFG)—Offset 830h" on page 5032	00078080h
83C–83Fh	4	"C71p1cfiohvrscorepsdio3 Compensation DFX Override (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_DFX)—Offset 83Ch" on page 5033	01000080h
840–843h	4	"C71p1cfiohvrscoreplpc Compensation Configuration (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_CFG)—Offset 840h" on page 5034	00078080h
84C–84Fh	4	"C71p1cfiohvrscoreplpc Compensation DFX Override (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_DFX)—Offset 84Ch" on page 5035	01000080h
850–853h	4	"Aza1 Strength Group (cfio_regs_aza1_STRENGTH)—Offset 850h" on page 5036	BABECAFEh
854–857h	4	"Clkreq Strength Group (cfio_regs_clkreq_STRENGTH)—Offset 854h" on page 5036	0003000Fh
858–85Bh	4	"Crt I2c Clk Strength Group (cfio_regs_crt_i2c_clk_STRENGTH)—Offset 858h" on page 5037	00020002h
85C–85Fh	4	"Crt I2c Data Strength Group (cfio_regs_crt_i2c_data_STRENGTH)—Offset 85Ch" on page 5037	00020002h
860–863h	4	"Hsi Strength Group (cfio_regs_hsi_STRENGTH)—Offset 860h" on page 5038	0003000Fh
864–867h	4	"I2c Strength Group (cfio_regs_i2c_STRENGTH)—Offset 864h" on page 5038	0003000Fh
868–86Bh	4	"Lpc Strength Group (cfio_regs_lpc_STRENGTH)—Offset 868h" on page 5038	BABECAFEh
86C–86Fh	4	"Mmc3 Strength Group (cfio_regs_mmc3_STRENGTH)—Offset 86Ch" on page 5039	BABECAFEh
870–873h	4	"Mvt Mmc3 Strength Group (cfio_regs_mvt_mmc3_STRENGTH)—Offset 870h" on page 5039	0003000Fh
874–877h	4	"Mvt Rcomp Strength Group (cfio_regs_mvt_rcomp_STRENGTH)—Offset 874h" on page 5040	BABECAFEh
878–87Bh	4	"Nfc Strength Group (cfio_regs_nfc_STRENGTH)—Offset 878h" on page 5040	0003000Fh
87C–87Fh	4	"Pltclk Strength Group (cfio_regs_pltclk_STRENGTH)—Offset 87Ch" on page 5041	0003000Fh
880–883h	4	"Pwm Strength Group (cfio_regs_pwm_STRENGTH)—Offset 880h" on page 5041	0003000Fh
884–887h	4	"Sata Strength Group (cfio_regs_sata_STRENGTH)—Offset 884h" on page 5042	0003000Fh
888–88Bh	4	"Smb Strength Group (cfio_regs_smb_STRENGTH)—Offset 888h" on page 5042	0003000Fh

Table 340. Summary of iLB GPIO S0 Memory Mapped I/O Registers—IOBASE (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
88C–88Fh	4	"Spi Strength Group (cfio_regs_spi_STRENGTH)—Offset 88Ch" on page 5043	0003000Fh
890–893h	4	"Spkr Strength Group (cfio_regs_spkr_STRENGTH)—Offset 890h" on page 5043	0003000Fh
894–897h	4	"Ssp Strength Group (cfio_regs_ssp_STRENGTH)—Offset 894h" on page 5043	0003000Fh
898–89Bh	4	"Uart1 Strength Group (cfio_regs_uart1_STRENGTH)—Offset 898h" on page 5044	0003000Fh
950–953h	4	"WR PATH SCORE Master Delay Line Write Address (cfio_regs_DLL_WR_PATH_SCORE_MDL_WRITE_PATH_C_F_ADDR)—Offset 950h" on page 5044	00080000h
954–957h	4	"WR PATH1 MUX SCORE Delay Line Write Multiplexer 1 (cfio_regs_DLL_WR_PATH1_MUX_SCORE_DLL_WRITE_PATH1_MUX)—Offset 954h" on page 5045	00000000h
958–95Bh	4	"WR PATH2 MUX SCORE Delay Line Write Multiplexer 2 (cfio_regs_DLL_WR_PATH2_MUX_SCORE_DLL_WRITE_PATH2_MUX)—Offset 958h" on page 5046	00000000h
95C–95Fh	4	"WR PATH3 MUX SCORE Delay Line Write Multiplexer 3 (cfio_regs_DLL_WR_PATH3_MUX_SCORE_DLL_WRITE_PATH3_MUX)—Offset 95Ch" on page 5046	00000000h
970–973h	4	"CTRL SCORE Master Delay Line Fsm Control (cfio_regs_DLL_CTRL_SCORE_MDL_FSM_CTRL)—Offset 970h" on page 5047	00000000h
980–983h	4	"DIRECT IRQ0 SCORE Direct Interrupt Multiplexer 0 (cfio_regs_REG_DIRECT_IRQ0_SCORE_DIRECT_IRQ_0)—Offset 980h" on page 5048	00000000h
984–987h	4	"DIRECT IRQ1 SCORE Direct Interrupt Multiplexer 1 (cfio_regs_REG_DIRECT_IRQ1_SCORE_DIRECT_IRQ_1)—Offset 984h" on page 5049	00000000h
988–98Bh	4	"DIRECT IRQ2 SCORE Direct Interrupt Multiplexer 2 (cfio_regs_REG_DIRECT_IRQ2_SCORE_DIRECT_IRQ_2)—Offset 988h" on page 5050	00000000h
98C–98Fh	4	"DIRECT IRQ3 SCORE Direct Interrupt Multiplexer 3 (cfio_regs_REG_DIRECT_IRQ3_SCORE_DIRECT_IRQ_3)—Offset 98Ch" on page 5050	00000000h
9A4–9A7h	4	"E Emmc 4.5 max high speed mux (cfio_regs_SCORE_EMMC_45_HSMAX)—Offset 9A4h" on page 5051	00000000h
9A8–9ABh	4	"E Emmc 4.5 sdr50 speed mux (cfio_regs_SCORE_EMMC_45_SDR50)—Offset 9A8h" on page 5052	00000000h
9AC–9AFh	4	"E Emmc 4.5 ddr50 speed mux (cfio_regs_SCORE_EMMC_45_DDR50)—Offset 9ACh" on page 5053	00000000h
9B0–9B3h	4	"E Emmc 4.5 max high speed mux (cfio_regs_SCORE_EMMC_45_HSMAX)—Offset 9A4h" on page 5051	00000000h
9B4–9B7h	4	"E Emmc 4.5 norm speed mux (cfio_regs_SCORE_EMMC_45_NORM)—Offset 9B4h" on page 5054	00000000h
9C0–9C3h	4	"E Special configuration bits (cfio_regs_SCORE_SPECIAL_BITS)—Offset 9C0h" on page 5055	00000000h
9D0–9D3h	4	"E Debounce Control (cfio_regs_SCORE_DEBOUNCE_CTRL)—Offset 9D0h" on page 5056	00000000h
9F4–9F7h	4	"E eMMC 4.5 TAP select register (cfio_regs_SCORE_TAP_SEL_REG)—Offset 9F4h" on page 5056	00000000h

39.8.1 Uart1 Rts B Pad Configuration (cfio_regs_pad_uart1_rts_b_PCONF0)—Offset 0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_72 function 1 is UART1_RTS_B

39.8.2 Uart1 Rts B Pad Value (cfio_regs_pad_uart1_rts_b_PAD_VAL)—Offset 8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.3 Uart1 Txd Pad Configuration (cfio_regs_pad_uart1_txd_PCONF0)—Offset 10h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 10h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_71 function 1 is UART1_TXD function 2 is MHSI_ACREADY

39.8.4 Uart1 Txd Pad Value (cfio_regs_pad_uart1_txd_PAD_VAL)—Offset 18h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 18h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.5 Uart1 Rxd Pad Configuration (cfio_regs_pad_uart1_rxd_PCONF0)—Offset 20h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 20h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_70 function 1 is UART1_RXD function 2 is MHSI_CAREADY

39.8.6 Uart1 Rxd Pad Value (cfio_regs_pad_uart1_rxd_PAD_VAL)—Offset 28h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 28h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.7 I2c Nfc Scl Pad Configuration (cfio_regs_pad_i2c_nfc_scl_PCONF0)—Offset 30h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 30h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is I2C_NFC_SCL function 1 is GPIOC_93

39.8.8 I2c Nfc Scl Pad Value (cfio_regs_pad_i2c_nfc_scl_PAD_VAL)—Offset 38h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 38h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	28	24	20	16	12	8	4	0
0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0

RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.9 Uart1 Cts B Pad Configuration (cfio_regs_pad_uart1_cts_b_PCONF0)—Offset 40h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 40h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_73 function 1 is UART1_CTS_B

39.8.10 Uart1 Cts B Pad Value (cfio_regs_pad_uart1_cts_b_PAD_VAL)—Offset 48h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 48h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.11 I2c Nfc Sda Pad Configuration (cfio_regs_pad_i2c_nfc_sda_PCONF0)—Offset 50h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 50h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is I2C_NFC_SDA function 1 is GPIOC_92

39.8.12 I2c Nfc Sda Pad Value (cfio_regs_pad_i2c_nfc_sda_PAD_VAL)—Offset 58h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 58h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.13 Uart2 Rxd Pad Configuration (cfio_regs_pad_uart2_rxd_PCONF0)—Offset 60h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 60h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Value	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_74 function 1 is UART2_RXD

39.8.14 Uart2 Rxd Pad Value (cfio_regs_pad_uart2_rxd_PAD_VAL)—Offset 68h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 68h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.15 Uart2 Txd Pad Configuration (cfio_regs_pad_uart2_txd_PCONF0)—Offset 70h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 70h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_75 function 1 is UART2_TXD

39.8.16 Uart2 Txd Pad Value (cfio_regs_pad_uart2_txd_PAD_VAL)—Offset 78h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 78h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.17 Uart2 Cts B Pad Configuration (cfio_regs_pad_uart2_cts_b_PCONF0)—Offset 80h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 80h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_77 function 1 is UART2_CTS_B

39.8.18 Uart2 Cts B Pad Value (cfio_regs_pad_uart2_cts_b_PAD_VAL)—Offset 88h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 88h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.19 Uart2 Rts B Pad Configuration (cfio_regs_pad_uart2_rts_b_PCONF0)—Offset 90h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 90h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_76 function 1 is UART2_RTS_B

39.8.20 Uart2 Rts B Pad Value (cfio_regs_pad_uart2_rts_b_PAD_VAL)—Offset 98h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 98h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	

RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.21 Pwm0 Pad Configuration (cfio_regs_pad_pwm0_PCONF0)—Offset A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	1 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_94 function 1 is PWM0

39.8.22 Pwm0 Pad Value (cfio_regs_pad_pwm0_PAD_VAL)—Offset A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.23 Pwm1 Pad Configuration (cfio_regs_pad_pwm1_PCONF0)—Offset B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_95 function 1 is PWM1

39.8.24 Pwm1 Pad Value (cfio_regs_pad_pwm1_PAD_VAL)—Offset B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.25 Gp Ssp 2 Fs Pad Configuration (cfio_regs_pad_gp_ssp_2_fs_PCONF0)—Offset C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_63 function 1 is GP_SSP_2_FS For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10 function 2 is MHSI_CAWAKE For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

39.8.26 Gp Ssp 2 Fs Pad Value (cfio_regs_pad_gp_ssp_2_fs_PAD_VAL)—Offset C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.27 Gp Ssp 2 Clk Pad Configuration (cfio_regs_pad_gp_ssp_2_clk_PCONF0)—Offset D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_62 function 1 is GP_SSP_2_CLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is SATA_DEVSLP1 function 3 is EDM_CFIO

39.8.28 Gp Ssp 2 Clk Pad Value (cfio_regs_pad_gp_ssp_2_clk_PAD_VAL)—Offset D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0

Fields: RSVD (31:22), RSVD (21:3), iinenb (2), ioutenb (1), pad_val (0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.29 Gp Ssp 2 Txd Pad Configuration (cfio_regs_pad_gp_ssp_2_txd_PCONF0)—Offset E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_65 function 1 is GP_SSP_2_TXD For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

39.8.30 Gp Ssp 2 Txd Pad Value (cfio_regs_pad_gp_ssp_2_txd_PAD_VAL)—Offset E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.31 Gp Ssp 2 Rxd Pad Configuration (cfio_regs_pad_gp_ssp_2_rxd_PCONF0)—Offset F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_64 function 1 is GP_SSP_2_RXD

39.8.32 Gp Ssp 2 Rxd Pad Value (cfio_regs_pad_gp_ssp_2_rxd_PAD_VAL)—Offset F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:0 = 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

Fields: RSVD (31:22), RSVD (21:3), iinenb (2), ioutenb (1), pad_val (0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.33 Spi1 Clk Pad Configuration (cfio_regs_pad_spi1_clk_PCONF0)—Offset 100h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 100h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_69 function 1 is SPI1_CLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01

39.8.34 Spi1 Clk Pad Value (cfio_regs_pad_spi1_clk_PAD_VAL)—Offset 108h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 108h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.35 Spi1 Cs0 B Pad Configuration (cfio_regs_pad_spi1_cs0_b_PCONF0)—Offset 110h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 110h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_66 function 1 is SPI1_CS0_B For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

39.8.36 Spi1 Cs0 B Pad Value (cfio_regs_pad_spi1_cs0_b_PAD_VAL)—Offset 118h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 118h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.37 Spi1 Miso Pad Configuration (cfio_regs_pad_spi1_miso_PCONF0)—Offset 120h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 120h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_67 function 1 is SPI1_MISO

39.8.38 Spi1 Miso Pad Value (cfio_regs_pad_spi1_miso_PAD_VAL)—Offset 128h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 128h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.39 Spi1 Mosi Pad Configuration (cfio_regs_pad_spi1_mosi_PCONF0)—Offset 130h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 130h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_68 function 1 is SPI1_MOSI

39.8.40 Spi1 Mosi Pad Value (cfio_regs_pad_spi1_mosi_PAD_VAL)—Offset 138h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 138h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.41 I2c5 Scl Pad Configuration (cfio_regs_pad_i2c5_scl_PCONF0)—Offset 140h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 140h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_89 function 1 is I2C5_SCL

39.8.42 I2c5 Scl Pad Value (cfio_regs_pad_i2c5_scl_PAD_VAL)—Offset 148h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 148h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.43 I2c5 Sda Pad Configuration (cfio_regs_pad_i2c5_sda_PCONF0)—Offset 150h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 150h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_88 function 1 is I2C5_SDA

39.8.44 I2c5 Sda Pad Value (cfio_regs_pad_i2c5_sda_PAD_VAL)—Offset 158h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 158h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RSVD (31:22)	RSVD (21:3)	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.45 I2c6 Scl Pad Configuration (cfio_regs_pad_i2c6_scl_PCONF0)—Offset 160h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 160h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_91 function 1 is I2C6_SCL function 2 is SDMMC3_WP

39.8.46 I2c6 Scl Pad Value (cfio_regs_pad_i2c6_scl_PAD_VAL)—Offset 168h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 168h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.47 I2c4 Scl Pad Configuration (cfio_regs_pad_i2c4_scl_PCONF0)—Offset 170h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 170h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_87 function 1 is I2C4_SCL

39.8.48 I2c4 Scl Pad Value (cfio_regs_pad_i2c4_scl_PAD_VAL)—Offset 178h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 178h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.49 I2c6 Sda Pad Configuration (cfio_regs_pad_i2c6_sda_PCONF0)—Offset 180h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 180h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

31			28				24			20				16			12			8		4		0
0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_90 function 1 is I2C6_SDA function 2 is NMI For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

39.8.50 I2c6 Sda Pad Value (cfio_regs_pad_i2c6_sda_PAD_VAL)—Offset 188h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 188h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.51 I2c3 Sda Pad Configuration (cfio_regs_pad_i2c3_sda_PCONF0)—Offset 190h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 190h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_84 function 1 is I2C3_SDA function 2 is Unused

39.8.52 I2c3 Sda Pad Value (cfio_regs_pad_i2c3_sda_PAD_VAL)—Offset 198h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 198h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.53 I2c4 Sda Pad Configuration (cfio_regs_pad_i2c4_sda_PCONF0)—Offset 1A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 1A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_86 function 1 is I2C4_SDA function 2 is Unused

39.8.54 I2c4 Sda Pad Value (cfio_regs_pad_i2c4_sda_PAD_VAL)—Offset 1A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.55 I2c2 Scl Pad Configuration (cfio_regs_pad_i2c2_scl_PCONF0)—Offset 1B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_83 function 1 is I2C2_SCL function 2 is Unused

39.8.56 I2c2 Scl Pad Value (cfio_regs_pad_i2c2_scl_PAD_VAL)—Offset 1B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.57 I2c3 Scl Pad Configuration (cfio_regs_pad_i2c3_scl_PCONF0)—Offset 1C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_85 function 1 is I2C3_SCL function 2 is Unused

39.8.58 I2c3 Scl Pad Value (cfio_regs_pad_i2c3_scl_PAD_VAL)—Offset 1C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.59 I2c2 Sda Pad Configuration (cfio_regs_pad_i2c2_sda_PCONF0)—Offset 1D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_82 function 1 is I2C2_SDA function 2 is Unused

39.8.60 I2c2 Sda Pad Value (cfio_regs_pad_i2c2_sda_PAD_VAL)—Offset 1D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	

31:22	21:3	2	1	0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.61 I2c1 Scl Pad Configuration (cfio_regs_pad_i2c1_scl_PCONF0)—Offset 1E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_81 function 1 is I2C1_SCL function 2 is CCU_PLL_LOCKEN

39.8.62 I2c1 Scl Pad Value (cfio_regs_pad_i2c1_scl_PAD_VAL)—Offset 1E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31:22	Bits 21:3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.63 I2c1 Sda Pad Configuration (cfio_regs_pad_i2c1_sda_PCONF0)—Offset 1F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 1F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_80 function 1 is I2C1_SDA function 2 is Unused

39.8.64 I2c1 Sda Pad Value (cfio_regs_pad_i2c1_sda_PAD_VAL)—Offset 1F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 1F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.65 I2c0 Scl Pad Configuration (cfio_regs_pad_i2c0_scl_PCONF0)—Offset 200h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 200h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_79 function 1 is I2C0_SCL function 2 is Unused

39.8.66 I2c0 Scl Pad Value (cfio_regs_pad_i2c0_scl_PAD_VAL)—Offset 208h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 208h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.67 I2c0 Sda Pad Configuration (cfio_regs_pad_i2c0_sda_PCONF0)—Offset 210h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 210h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Value	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_78 function 1 is I2C0_SDA function 2 is Unused

39.8.68 I2c0 Sda Pad Value (cfio_regs_pad_i2c0_sda_PAD_VAL)—Offset 218h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 218h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.69 Hda Rstb Pad Configuration (cfio_regs_pad_hda_rstb_PCONF0)—Offset 220h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 220h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_8 function 1 is GP_SSP_0_I2S_CLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_RSTB

39.8.70 Hda Rstb Pad Value (cfio_regs_pad_hda_rstb_PAD_VAL)—Offset 228h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 228h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

31:22	21:3	2	1	0
0000000000	0000000000000000000	0	1	0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.71 Hda Sdi1 Pad Configuration (cfio_regs_pad_hda_sdi1_PCONF0)—Offset 230h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 230h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_13 function 1 is GP_SSP_1_I2S_FS For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_SDI1

39.8.72 Hda Sdi1 Pad Value (cfio_regs_pad_hda_sdi1_PAD_VAL)—Offset 238h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 238h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31:22	Bits 21:3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.73 Hda Clk Pad Configuration (cfio_regs_pad_hda_clk_PCONF0)—Offset 240h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [IOBASE] + 240h
	IOBASE Type: PCI Configuration Register (Size: 32 bits) **IOBASE Reference:** [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

Bit(s)	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 1	0	1	1 0	1 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_10 function 1 is GP_SSP_0_I2S_TXD For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_CLK

39.8.74 Hda Clk Pad Value (cfio_regs_pad_hda_clk_PAD_VAL)—Offset 248h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 248h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.75 Hda Sync Pad Configuration (cfio_regs_pad_hda_sync_PCONF0)—Offset 250h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 250h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_9 function 1 is GP_SSP_0_I2S_FS For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_SYNC For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01

39.8.76 Hda Sync Pad Value (cfio_regs_pad_hda_sync_PAD_VAL)—Offset 258h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 258h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.77 Hda Sdo Pad Configuration (cfio_regs_pad_hda_sdo_PCONF0)—Offset 260h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 260h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_11 function 1 is GP_SSP_0_I2S_RXD function 2 is HDA_SDO For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01

39.8.78 Hda Sdo Pad Value (cfio_regs_pad_hda_sdo_PAD_VAL)—Offset 268h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 268h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.79 Hda Sdi0 Pad Configuration (cfio_regs_pad_hda_sdi0_PCONF0)—Offset 270h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 270h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 1	0	1	1 0	1 0	0 0	0	0	0 0 0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_12 function 1 is GP_SSP_1_I2S_CLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_SDI0

39.8.80 Hda Sdi0 Pad Value (cfio_regs_pad_hda_sdi0_PAD_VAL)—Offset 278h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 278h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.81 Hda Dockrstb Pad Configuration (cfio_regs_pad_hda_dockrstb_PCONF0)—Offset 280h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 280h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_14 function 1 is GP_SSP_1_I2S_TXD For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 2 is HDA_DOCKRSTB

39.8.82 Hda Dockrstb Pad Value (cfio_regs_pad_hda_dockrstb_PAD_VAL)—Offset 288h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 288h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.83 Sdmmc3 D1 Pad Configuration (cfio_regs_pad_sdmmc3_d1_PCONF0)—Offset 290h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 290h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	0 0	0	1	1 0	0 1	0 0	0	0	0 0 0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	RSVD	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_35 function 1 is SDMMC3_D1

39.8.84 Sdmmc3 D1 Pad Value (cfio_regs_pad_sdmmc3_d1_PAD_VAL)—Offset 298h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 298h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Fields: RSVD (31:22), RSVD (21:3), iinenb (2), ioutenb (1), pad_val (0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.85 Sdmmc3 D3 Pad Configuration (cfio_regs_pad_sdmmc3_d3_PCONF0)—Offset 2A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 2A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	RSVD		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_37 function 1 is SDMMC3_D3

39.8.86 Sdmmc3 D3 Pad Value (cfio_regs_pad_sdmmc3_d3_PAD_VAL)—Offset 2A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 2A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.87 Sdmmc3 Clk Pad Configuration (cfio_regs_pad_sdmmc3_clk_PCONF0)—Offset 2B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 2B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038D00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_33 function 1 is SDMMC3_CLK

39.8.88 Sdmmc3 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc3_clk_PCONF1)—Offset 2B4h

DLL Multiplexer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 2B4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	RSVD																dll_cf_od	dll_ddr_mux					dll_hgh_mux					dll_std_mux				

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15	1b RW	**Dll Cf Od (dll_cf_od):** 0 - Enable Master DLL tuning, 1 - Disable Master DLL tuning.
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Set the used number of dll cells to use for ddr speed for read path DLL. Recommended value is 3.5ns (5'b01101).
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Set the used number of dll cells to use for high speed for read path DLL. Recommended value is 3.5ns (5'b01101).
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Set the used number of dll cells to use for standard speed for read path DLL. Recommended value is 3.5ns (5'b01101).

39.8.89 Sdmmc3 Clk Pad Value (cfio_regs_pad_sdmmc3_clk_PAD_VAL)—Offset 2B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 2B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Field	RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required

Bit Range	Default & Access	Field Name (ID): Description
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.90 Sdmmc3 Cmd Pad Configuration (cfio_regs_pad_sdmmc3_cmd_PCONF0)—Offset 2C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 2C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_39 function 1 is SDMMC3_CMD

39.8.91 Sdmmc3 Cmd Pad Value (cfio_regs_pad_sdmmc3_cmd_PAD_VAL)—Offset 2C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 2C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD											RSVD																		iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.92 Sdmmc3 D2 Pad Configuration (cfio_regs_pad_sdmmc3_d2_PCONF0)—Offset 2D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 2D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Value	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	0 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	RSVD	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_36 function 1 is SDMMC3_D2

39.8.93 Sdmmc3 D2 Pad Value (cfio_regs_pad_sdmmc3_d2_PAD_VAL)—Offset 2D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 2D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.94 Sdmmc3 D0 Pad Configuration (cfio_regs_pad_sdmmc3_d0_PCONF0)—Offset 2E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 2E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	RSVD		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_34 function 1 is SDMMC3_D0

39.8.95 Sdmmc3 D0 Pad Value (cfio_regs_pad_sdmmc3_d0_PAD_VAL)—Offset 2E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 2E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Field
31:22	RSVD
21:3	RSVD
2	iinenb
1	ioutenb
0	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.96 Sdmmc2 D1 Pad Configuration (cfio_regs_pad_sdmmc2_d1_PCONF0)—Offset 2F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 2F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0

Bits	Field
31	RSVD
30	RSVD
29	disable_second_mask
28	RSVD
27	direct_irq_en
26	gd_tne
25	gd_tpe
24	gd_level
23	RSVD
22:21	RSVD
20	debounce
19	filter_en
18	filter_slow
17	slow_clkgate
16	fast_clkgate
15	RSVD
14:13	ihysctl
12	RSVD
11	bypass_flop
10:9	pull_str
8:7	pull_assign
6:5	RSVD
4	RSVD
3	RSVD
2:0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_29 function 1 is SDMMC2_D1

39.8.97 Sdmmc2 D1 Pad Value (cfio_regs_pad_sdmmc2_d1_PAD_VAL)—Offset 2F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 2F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.98 Sdmmc2 Cmd Pad Configuration (cfio_regs_pad_sdmmc2_cmd_PCONF0)—Offset 300h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 300h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bit	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 1	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_32 function 1 is SDMMC2_CMD

39.8.99 Sdmmc2 Cmd Pad Value (cfio_regs_pad_sdmmc2_cmd_PAD_VAL)—Offset 308h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 308h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RSVD (31:22)	RSVD (21:3)	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.100 Sdmmc2 D3 Cd B Pad Configuration (cfio_regs_pad_sdmmc2_d3_cd_b_PCONF0)—Offset 310h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 310h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 1	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_31 function 1 is SDMMC2_D3_CD_B

39.8.101 Sdmmc2 D3 Cd B Pad Value (cfio_regs_pad_sdmmc2_d3_cd_b_PAD_VAL)—Offset 318h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 318h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RSVD (31:22)	RSVD (21:3)	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.102 Sdmmc2 Clk Pad Configuration (cfio_regs_pad_sdmmc2_clk_PCONF0)—Offset 320h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 320h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_27 function 1 is SDMMC2_CLK

39.8.103 Sdmmc2 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc2_clk_PCONF1)—Offset 324h

DLL Multiplexer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 324h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																dll_cf_od	dll_ddr_mux					dll_hgh_mux					dll_std_mux				

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15	1b RW	**Dll Cf Od (dll_cf_od):** 0 - Enable Master DLL tuning, 1 - Disable Master DLL tuning.
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Set the used number of dll cells to use for ddr speed for read path DLL. Recommended value is 3.5ns (5'b01101).
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Set the used number of dll cells to use for high speed for read path DLL. Recommended value is 3.5ns (5'b01101).
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Set the used number of dll cells to use for standard speed for read path DLL. Recommended value is 3.5ns (5'b01101).

39.8.104 Sdmmc2 Clk Pad Value (cfio_regs_pad_sdmmc2_clk_PAD_VAL)—Offset 328h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 328h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.105 Mmc1 Reset B Pad Configuration (cfio_regs_pad_mmc1_reset_b_PCONF0)—Offset 330h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 330h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_26 function 1 is MMC1_RESET_B function 2 is SATA_DEVSLP0 function 3 is MMC_45_RESET_B

39.8.106 Mmc1 Reset B Pad Value (cfio_regs_pad_mmc1_reset_b_PAD_VAL)—Offset 338h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 338h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.107 Sdmmc2 D2 Pad Configuration (cfio_regs_pad_sdmmc2_d2_PCONF0)—Offset 340h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 340h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_30 function 1 is SDMMC2_D2

39.8.108 Sdmmc2 D2 Pad Value (cfio_regs_pad_sdmmc2_d2_PAD_VAL)—Offset 348h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 348h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD											RSVD																		iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.109 Sdmmc2 D0 Pad Configuration (cfio_regs_pad_sdmmc2_d0_PCONF0)—Offset 350h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 350h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_28 function 1 is SDMMC2_D0

39.8.110 Sdmmc2 D0 Pad Value (cfio_regs_pad_sdmmc2_d0_PAD_VAL)—Offset 358h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 358h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.111 Sdmmc1 D3 Cd B Pad Configuration (cfio_regs_pad_sdmmc1_d3_cd_b_PCONF0)—Offset 360h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 360h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_20 function 1 is SDMMC1_D3_CD_B function 2 is Unused function 3 is SDMMC_45_D3_CD_B

39.8.112 Sdmmc1 D3 Cd B Pad Value (cfio_regs_pad_sdmmc1_d3_cd_b_PAD_VAL)—Offset 368h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 368h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.113 Mmc1 D6 Pad Configuration (cfio_regs_pad_mmc1_d6_PCONF0)—Offset 370h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 370h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_23 function 1 is MMC1_D6 function 2 is Unused function 3 is MMC_45_D6

39.8.114 Mmc1 D6 Pad Value (cfio_regs_pad_mmc1_d6_PAD_VAL)—Offset 378h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 378h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.115 Mmc1 D4 Sd We Pad Configuration (cfio_regs_pad_mmc1_d4_sd_we_PCONF0)—Offset 380h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 380h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_21 function 1 is MMC1_D4_SD_WE function 2 is Unused function 3 is MMC_45_D4_SD_WE

39.8.116 Mmc1 D4 Sd We Pad Value (cfio_regs_pad_mmc1_d4_sd_we_PAD_VAL)—Offset 388h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 388h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.117 Sdmmc1 Cmd Pad Configuration (cfio_regs_pad_sdmmc1_cmd_PCONF0)—Offset 390h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 390h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_25 function 1 is SDMMC1_CMD function 2 is Unused function 3 is SDMMC_45_CMD

39.8.118 Sdmmc1 Cmd Pad Value (cfio_regs_pad_sdmmc1_cmd_PAD_VAL)—Offset 398h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 398h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31:22	Bits 21:3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.119 Sdmmc3 Cd B Pad Configuration (cfio_regs_pad_sdmmc3_cd_b_PCONF0)—Offset 3A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 3A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_38 function 1 is SDMMC3_CD_B

39.8.120 Sdmmc3 Cd B Pad Value (cfio_regs_pad_sdmmc3_cd_b_PAD_VAL)—Offset 3A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 3A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required

Bit Range	Default & Access	Field Name (ID): Description
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.121 Sdmmc1 D2 Pad Configuration (cfio_regs_pad_sdmmc1_d2_PCONF0)—Offset 3B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 3B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_19 function 1 is SDMMC1_D2 function 2 is Unused function 3 is SDMMC_45_D2

39.8.122 Sdmmc1 D2 Pad Value (cfio_regs_pad_sdmmc1_d2_PAD_VAL)—Offset 3B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 3B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.123 Mmc1 D5 Pad Configuration (cfio_regs_pad_mmc1_d5_PCONF0)—Offset 3C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 3C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_22 function 1 is MMC1_D5 function 2 is Unused function 3 is MMC_45_D5

39.8.124 Mmc1 D5 Pad Value (cfio_regs_pad_mmc1_d5_PAD_VAL)—Offset 3C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 3C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.125 Sdmmc1 D0 Pad Configuration (cfio_regs_pad_sdmmc1_d0_PCONF0)—Offset 3D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 3D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bit	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 1	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_17 function 1 is SDMMC1_D0 function 2 is Unused function 3 is SDMMC_45_D0

39.8.126 Sdmmc1 D0 Pad Value (cfio_regs_pad_sdmmc1_d0_PAD_VAL)—Offset 3D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 3D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.127 Sdmmc1 Clk Pad Configuration (cfio_regs_pad_sdmmc1_clk_PCONF0)—Offset 3E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 3E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003ED00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_16 function 1 is SDMMC1_CLK function 2 is Unused function 3 is SDMMC_45_CLK

39.8.128 Sdmmc1 Clk Delay Line Multiplexer (cfio_regs_pad_sdmmc1_clk_PCONF1)—Offset 3E4h

DLL Multiplexer

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 3E4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																dll_cf_od	dll_ddr_mux					dll_hgh_mux					dll_std_mux				

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15	1b RW	**Dll Cf Od (dll_cf_od):** 0 - Enable Master DLL tuning, 1 - Disable Master DLL tuning.
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Set the used number of dll cells to use for ddr speed for read path DLL. Recommended value is 3.5ns (5'b01101).
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Set the used number of dll cells to use for high speed for read path DLL. Recommended value is 3.5ns (5'b01101).
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Set the used number of dll cells to use for standard speed for read path DLL. Recommended value is 3.5ns (5'b01101).

39.8.129 Sdmmc1 Clk Pad Value (cfio_regs_pad_sdmmc1_clk_PAD_VAL)—Offset 3E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 3E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.130 Mmc1 D7 Pad Configuration (cfio_regs_pad_mmc1_d7_PCONF0)—Offset 3F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 3F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_24 function 1 is MMC1_D7 function 2 is Unused function 3 is MMC_45_D7

39.8.131 Mmc1 D7 Pad Value (cfio_regs_pad_mmc1_d7_PAD_VAL)—Offset 3F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 3F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.132 Sdmmc1 D1 Pad Configuration (cfio_regs_pad_sdmmc1_d1_PCONF0)—Offset 400h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 400h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_18 function 1 is SDMMC1_D1 function 2 is Unused function 3 is SDMMC_45_D1

39.8.133 Sdmmc1 D1 Pad Value (cfio_regs_pad_sdmmc1_d1_PAD_VAL)—Offset 408h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 408h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD											RSVD																		iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.134 Lpc Clkout1 Pad Configuration (cfio_regs_pad_lpc_clkout1_PCONF0)—Offset 410h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 410h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038D00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_48 function 1 is LPC_CLKOUT1

39.8.135 Lpc Clkout1 Pad Value (cfio_regs_pad_lpc_clkout1_PAD_VAL)—Offset 418h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 418h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	iinenb 0	ioutenb 1	pad_val 0

Fields: RSVD (bits 31:22), RSVD (bits 21:3), iinenb (bit 2), ioutenb (bit 1), pad_val (bit 0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.136 Lpc Ad3 Pad Configuration (cfio_regs_pad_lpc_ad3_PCONF0)—Offset 420h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 420h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	RSVD		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_45 function 1 is LPC_AD3

39.8.137 Lpc Ad3 Pad Value (cfio_regs_pad_lpc_ad3_PAD_VAL)—Offset 428h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 428h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.138 Lpc Ad2 Pad Configuration (cfio_regs_pad_lpc_ad2_PCONF0)—Offset 430h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 430h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	0 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	RSVD	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_44 function 1 is LPC_AD2

39.8.139 Lpc Ad2 Pad Value (cfio_regs_pad_lpc_ad2_PAD_VAL)—Offset 438h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 438h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.140 Lpc Ad1 Pad Configuration (cfio_regs_pad_lpc_ad1_PCONF0)—Offset 440h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 440h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_43 function 1 is LPC_AD1

39.8.141 Lpc Ad1 Pad Value (cfio_regs_pad_lpc_ad1_PAD_VAL)—Offset 448h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 448h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD											RSVD																		iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required

Bit Range	Default & Access	Field Name (ID): Description
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.142 Lpc Frameb Pad Configuration (cfio_regs_pad_lpc_frameb_PCONF0)—Offset 450h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 450h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_46 function 1 is LPC_FRAMEB

39.8.143 Lpc Frameb Pad Value (cfio_regs_pad_lpc_frameb_PAD_VAL)—Offset 458h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 458h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.144 Lpc Ad0 Pad Configuration (cfio_regs_pad_lpc_ad0_PCONF0)—Offset 460h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 460h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_42 function 1 is LPC_AD0

39.8.145 Lpc Ad0 Pad Value (cfio_regs_pad_lpc_ad0_PAD_VAL)—Offset 468h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 468h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.146 Lpc Clkout0 Pad Configuration (cfio_regs_pad_lpc_clkout0_PCONF0)—Offset 470h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 470h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038D00h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_47 function 1 is LPC_CLKOUT0

39.8.147 Lpc Clkout0 Pad Value (cfio_regs_pad_lpc_clkout0_PAD_VAL)—Offset 478h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 478h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Field	RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.148 Lpc Clkrunb Pad Configuration (cfio_regs_pad_lpc_clkrunb_PCONF0)—Offset 480h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 480h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038C80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	RSVD		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_49 function 1 is LPC_CLKRUNB

39.8.149 Lpc Clkrunb Pad Value (cfio_regs_pad_lpc_clkrunb_PAD_VAL)—Offset 488h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 488h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.150 Hv Crt Ddc Clk Pad Configuration (cfio_regs_pad_hv_crt_ddc_clk_PCONF0)—Offset 490h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 490h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.94435 max vil(V) - 1.3965 min vih(V) - 0.94435 max vih(V) - 1.3965 01: min vil(V) - 0.90365 max vil(V) - 1.30405 min vih(V) - 1.09065 max vih(V) - 1.44045 10: min vil(V) - 0.90365 max vil(V) - 1.30405 min vih(V) - 1.20945 max vih(V) - 1.52185 11: min vil(V) - 0.8569 max vil(V) - 1.2243 min vih(V) - 1.2243 max vih(V) - 1.5455
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - reserved 01 - reserved 10 - 20K 11 - reserved
8:7	00b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is HV_CRT_DDC_CLK

39.8.151 Hv Crt Ddc Clk Pad Value (cfio_regs_pad_hv_crt_ddc_clk_PAD_VAL)—Offset 498h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 498h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.152 Hv Crt Vsync Pad Configuration (cfio_regs_pad_hv_crt_vsync_PCONF0)—Offset 4A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 4A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit	Value	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	RSVD
26	0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RW	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is HV_CRT_VSYNC

39.8.153 Hv Crt Vsync Pad Value (cfio_regs_pad_hv_crt_vsync_PAD_VAL)—Offset 4A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 4A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Field	Bits
RSVD	31:22
RSVD	21:3
iinenb	2
RSVD	1
pad_val	0

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.154 Hv Crt Hsync Pad Configuration (cfio_regs_pad_hv_crt_hsync_PCONF0)—Offset 4B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 4B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Field	Bits
RSVD	31
RSVD	30
disable_second_mask	29
RSVD	28
RSVD	27
RSVD	26
RSVD	25
RSVD	24
RSVD	23
RSVD	22:21
RSVD	20
RSVD	19
RSVD	18
RSVD	17
RSVD	16
RSVD	15
RSVD	14:13
RSVD	12
bypass_flop	11
RSVD	10:9
RSVD	8:7
RSVD	6:5
RSVD	4
RSVD	3
func_pin_mux	2:0

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RW	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is HV_CRT_HSYNC

39.8.155 Hv Crt Hsync Pad Value (cfio_regs_pad_hv_crt_hsync_PAD_VAL)—Offset 4B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 4B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD											RSVD																		iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.156 Hv Crt Ddc Data Pad Configuration (cfio_regs_pad_hv_crt_ddc_data_PCONF0)—Offset 4C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 4C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.94435 max vil(V) - 1.3965 min vih(V) - 0.94435 max vih(V) - 1.3965 01: min vil(V) - 0.90365 max vil(V) - 1.30405 min vih(V) - 1.09065 max vih(V) - 1.44045 10: min vil(V) - 0.90365 max vil(V) - 1.30405 min vih(V) - 1.20945 max vih(V) - 1.52185 11: min vil(V) - 0.8569 max vil(V) - 1.2243 min vih(V) - 1.2243 max vih(V) - 1.5455
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - reserved 01 - reserved 10 - 20K 11 - reserved
8:7	00b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is HV_CRT_DDC_DATA

39.8.157 Hv Crt Ddc Data Pad Value (cfio_regs_pad_hv_crt_ddc_data_PAD_VAL)—Offset 4C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 4C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.158 Mhsi Acdata Pad Configuration (cfio_regs_pad_mhsi_acdata_PCONF0)—Offset 4D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 4D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_55 function 1 is MHSI_ACDATA

39.8.159 Mhsi Acdata Pad Value (cfio_regs_pad_mhsi_acdata_PAD_VAL)—Offset 4D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 4D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.160 Mhsi Acwake Pad Configuration (cfio_regs_pad_mhsi_acwake_PCONF0)—Offset 4E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 4E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_58 function 1 is MHSI_ACWAKE

39.8.161 Mhsi Acwake Pad Value (cfio_regs_pad_mhsi_acwake_PAD_VAL)—Offset 4E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 4E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.162 Mhsi Acflag Pad Configuration (cfio_regs_pad_mhsi_acflag_PCONF0)—Offset 4F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 4F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_56 function 1 is MHSI_ACFLAG

39.8.163 Mhsi Acflag Pad Value (cfio_regs_pad_mhsi_acflag_PAD_VAL)—Offset 4F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 4F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0

Bits	31:22	21:3	2	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.164 Mhsi Caflag Pad Configuration (cfio_regs_pad_mhsi_caflag_PCONF0)—Offset 500h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 500h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_60 function 1 is MHSI_CAFLAG

39.8.165 Mhsi Caflag Delay Line Multiplexer (cfio_regs_pad_mhsi_caflag_PCONF1)—Offset 504h

DLL Multiplexer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 504h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																dll_cf_od	dll_ddr_mux				dll_hgh_mux					dll_std_mux					

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	1b RW	**Dll Cf Od (dll_cf_od):** 0 - Enable Master DLL tuning, 1 - Disable Master DLL tuning.
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Set the used number of dll cells to use for ddr speed for read path DLL. Recommended value is 3.5ns (5'b01101).
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Set the used number of dll cells to use for high speed for read path DLL. Recommended value is 3.5ns (5'b01101).
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Set the used number of dll cells to use for standard speed for read path DLL. Recommended value is 3.5ns (5'b01101).

39.8.166 Mhsi Caflag Pad Value (cfio_regs_pad_mhsi_caflag_PAD_VAL)—Offset 508h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 508h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.167 Mhsi Cadata Pad Configuration (cfio_regs_pad_mhsi_cadata_PCONF0)—Offset 510h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 510h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default bits	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_59 function 1 is MHSI_CADATA function 2 is DLL_FBCLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01 function 3 is DLL_REFCLK For this function, software should make sure it changes the default pull from down to up. pull assign field, bits [8:7] should be set to 2'b01

39.8.168 Mhsi Cadata Delay Line Multiplexer (cfio_regs_pad_mhsi_cadata_PCONF1)—Offset 514h

DLL Multiplexer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 514h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00008000h

31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

31:16	15	14:10	9:5	4:0
RSVD	dll_cf_od	dll_ddr_mux	dll_hgh_mux	dll_std_mux

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO	**Reserved (RSVD):** Reserved.
15	1b RW	**Dll Cf Od (dll_cf_od):** 0 - Enable Master DLL tuning, 1 - Disable Master DLL tuning.
14:10	00000b RW	**Dll Ddr Mux (dll_ddr_mux):** Set the used number of dll cells to use for ddr speed for read path DLL. Recommended value is 3.5ns (5'b01101).
9:5	00000b RW	**Dll Hgh Mux (dll_hgh_mux):** Set the used number of dll cells to use for high speed for read path DLL. Recommended value is 3.5ns (5'b01101).
4:0	00000b RW	**Dll Std Mux (dll_std_mux):** Set the used number of dll cells to use for standard speed for read path DLL. Recommended value is 3.5ns (5'b01101).

39.8.169 Mhsi Cadata Pad Value (cfio_regs_pad_mhsi_cadata_PAD_VAL)—Offset 518h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 518h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.170 Mhsi Caready Pad Configuration (cfio_regs_pad_mhsi_caready_PCONF0)—Offset 520h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 520h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_61 function 1 is UART3_RXD

39.8.171 Mhsi Caready Pad Value (cfio_regs_pad_mhsi_caready_PAD_VAL)—Offset 528h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 528h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.172 Mhsi Acready Pad Configuration (cfio_regs_pad_mhsi_acready_PCONF0)—Offset 530h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 530h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit(s)	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	1 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_57 function 1 is UART3_TXD

39.8.173 Mhsi Acready Pad Value (cfio_regs_pad_mhsi_acready_PAD_VAL)—Offset 538h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 538h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.174 Hda Dockenb Pad Configuration (cfio_regs_pad_hda_dockenb_PCONF0)—Offset 540h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 540h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_15 function 1 is GP_SSP_1_I2S_RXD function 2 is HDA_DOCKENB

39.8.175 Hda Dockenb Pad Value (cfio_regs_pad_hda_dockenb_PAD_VAL)—Offset 548h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 548h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 0

RSVD | RSVD | iinenb | ioutenb | pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.176 Sata Gp0 Pad Configuration (cfio_regs_pad_sata_gp0_PCONF0)—Offset 550h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 550h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_0 function 1 is SATA_GP0

39.8.177 Sata Gp0 Pad Value (cfio_regs_pad_sata_gp0_PAD_VAL)—Offset 558h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 558h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.178 Ilb Serirq Pad Configuration (cfio_regs_pad_ilb_serirq_PCONF0)—Offset 560h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 560h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_50 function 1 is ILB_SERIRQ

39.8.179 Ilb Serirq Pad Value (cfio_regs_pad_ilb_serirq_PAD_VAL)—Offset 568h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 568h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.180 Plt Clk1 Pad Configuration (cfio_regs_pad_plt_clk1_PCONF0)—Offset 570h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 570h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_97 function 1 is PLT_CLK1

39.8.181 Plt Clk1 Pad Value (cfio_regs_pad_plt_clk1_PAD_VAL)—Offset 578h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 578h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.182 Smb Clk Pad Configuration (cfio_regs_pad_smb_clk_PCONF0)—Offset 580h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 580h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_52 function 1 is SMB_CLK

39.8.183 Smb Clk Pad Value (cfio_regs_pad_smb_clk_PAD_VAL)—Offset 588h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 588h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.184 Sata Gp1 Pad Configuration (cfio_regs_pad_sata_gp1_PCONF0)—Offset 590h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 590h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_1 function 1 is SATA_GP1 function 2 is SATA_DEVSLP0

39.8.185 Sata Gp1 Pad Value (cfio_regs_pad_sata_gp1_PAD_VAL)—Offset 598h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 598h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.186 Smb Data Pad Configuration (cfio_regs_pad_smb_data_PCONF0)—Offset 5A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 5A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_51 function 1 is SMB_DATA

39.8.187 Smb Data Pad Value (cfio_regs_pad_smb_data_PAD_VAL)—Offset 5A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 5A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.188 Plt Clk2 Pad Configuration (cfio_regs_pad_plt_clk2_PCONF0)—Offset 5B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 5B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_98 function 1 is PLT_CLK2

39.8.189 Plt Clk2 Pad Value (cfio_regs_pad_plt_clk2_PAD_VAL)—Offset 5B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 5B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.190 Smb Alertb Pad Configuration (cfio_regs_pad_smb_alertb_PCONF0)—Offset 5C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 5C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_53 function 1 is SMB_ALERTB

39.8.191 Smb Alertb Pad Value (cfio_regs_pad_smb_alertb_PAD_VAL)—Offset 5C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 5C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0

Bits	31:22	21:3	2	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.192 Sata Ledn Pad Configuration (cfio_regs_pad_sata_ledn_PCONF0)—Offset 5D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 5D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_2 function 1 is SATA_LEDN

39.8.193 Sata Ledn Pad Value (cfio_regs_pad_sata_ledn_PAD_VAL)—Offset 5D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 5D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.194 Pmu Resetbutton B Pad Configuration (cfio_regs_pad_pmu_resetbutton_b_PCONF0)—Offset 5E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 5E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_RESETBUTTON_B

39.8.195 Pmu Resetbutton B Pad Value (cfio_regs_pad_pmu_resetbutton_b_PAD_VAL)—Offset 5E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 5E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 0

Bits	31:22	21:3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.196 Pmu Resetbutton B Pad Test (cfio_regs_pad_pmu_resetbutton_b_PAD_DFT)—Offset 5ECh

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 5ECh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

Bits	31:11	10	9:6	5	4	3	2	1	0
Value	0000 0000 0000 0000 0000 0	1	0000	0	0	0	0	0	0
Field	RSVD	bscan_bypass	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.8.197 Sdmmc3 1p8 En Pad Configuration (cfio_regs_pad_sdmmc3_1p8_en_PCONF0)—Offset 5F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 5F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_40 function 1 is SDMMC3_1P8_EN

39.8.198 Sdmmc3 1p8 En Pad Value (cfio_regs_pad_sdmmc3_1p8_en_PAD_VAL)—Offset 5F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 5F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.199 Pcie Clkreq0b Pad Configuration (cfio_regs_pad_pcie_clkreq0b_PCONF0)—Offset 600h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 600h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_3 function 1 is PCIE_CLKREQ0B

39.8.200 Pcie Clkreq0b Pad Value (cfio_regs_pad_pcie_clkreq0b_PAD_VAL)—Offset 608h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 608h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.201 Plt Clk4 Pad Configuration (cfio_regs_pad_plt_clk4_PCONF0)—Offset 610h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 610h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_100 function 1 is PLT_CLK4

39.8.202 Plt Clk4 Pad Value (cfio_regs_pad_plt_clk4_PAD_VAL)—Offset 618h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 618h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.203 Pcie Clkreq3b Pad Configuration (cfio_regs_pad_pcie_clkreq3b_PCONF0)—Offset 620h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 620h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_6 function 1 is PCIE_CLKREQ3B

39.8.204 Pcie Clkreq3b Pad Value (cfio_regs_pad_pcie_clkreq3b_PAD_VAL)—Offset 628h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 628h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
				RSVD															RSVD										iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.205 Pcie Clkreq1b Pad Configuration (cfio_regs_pad_pcie_clkreq1b_PCONF0)—Offset 630h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 630h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_4 function 1 is PCIE_CLKREQ1B

39.8.206 Pcie Clkreq1b Pad Value (cfio_regs_pad_pcie_clkreq1b_PAD_VAL)—Offset 638h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 638h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.207 Plt Clk5 Pad Configuration (cfio_regs_pad_plt_clk5_PCONF0)—Offset 640h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 640h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_101 function 1 is PLT_CLK5

39.8.208 Plt Clk5 Pad Value (cfio_regs_pad_plt_clk5_PAD_VAL)—Offset 648h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 648h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Field	RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.209 Pcie Clkreq4b Pad Configuration (cfio_regs_pad_pcie_clkreq4b_PCONF0)—Offset 650h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 650h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_7 function 1 is PCIE_CLKREQ4B function 2 is SDMMC3_WP

39.8.210 Pcie Clkreq4b Pad Value (cfio_regs_pad_pcie_clkreq4b_PAD_VAL)—Offset 658h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 658h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.211 Pcie Clkreq2b Pad Configuration (cfio_regs_pad_pcie_clkreq2b_PCONF0)—Offset 660h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 660h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit(s)	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_5 function 1 is PCIE_CLKREQ2B

39.8.212 Pcie Clkreq2b Pad Value (cfio_regs_pad_pcie_clkreq2b_PAD_VAL)—Offset 668h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 668h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.213 Spkr Pad Configuration (cfio_regs_pad_spkr_PCONF0)—Offset 670h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 670h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.

Bit Range	Default & Access	Field Name (ID): Description
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_54 function 1 is SPKR function 2 is DLL_REFCLK For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10 function 3 is DLL_UPDN

39.8.214 Spkr Pad Value (cfio_regs_pad_spkr_PAD_VAL)—Offset 678h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 678h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31–22	21–3	2	1	0
0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.215 Plt Clk3 Pad Configuration (cfio_regs_pad_plt_clk3_PCONF0)—Offset 680h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [IOBASE] + 680h
	IOBASE Type: PCI Configuration Register (Size: 32 bits) **IOBASE Reference:** [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		debounce	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_99 function 1 is PLT_CLK3

39.8.216 Plt Clk3 Pad Value (cfio_regs_pad_plt_clk3_PAD_VAL)—Offset 688h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 688h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

31:22	21:3	2	1	0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.217 Sdmmc3 Pwr En B Pad Configuration (cfio_regs_pad_sdmmc3_pwr_en_b_PCONF0)—Offset 690h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 690h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_41 function 1 is SDMMC3_PWR_EN_B

39.8.218 Sdmmc3 Pwr En B Pad Value (cfio_regs_pad_sdmmc3_pwr_en_b_PAD_VAL)—Offset 698h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 698h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.219 Plt Clk0 Pad Configuration (cfio_regs_pad_plt_clk0_PCONF0)—Offset 6A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	debounce
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RW	**Debounce (debounce):** Enabling the debouncer for this pad. Debounce time will be according to the community setting at the debounce control register
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOC_96 function 1 is PLT_CLK0

39.8.220 Plt Clk0 Pad Value (cfio_regs_pad_plt_clk0_PAD_VAL)—Offset 6A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 6A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.221 Vgpio 0 Pad Configuration (cfio_regs_pad_vgpio_0_PCONF0)—Offset 6B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 6B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	0 0	0	1	0 0	0 0	0 0	0	0	0 0 0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	bypass_flop	RSVD	RSVD	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.222 Vgpio 0 Pad Value (cfio_regs_pad_vgpio_0_PAD_VAL)—Offset 6B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RSVD										RSVD																			RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.223 Vgpio 1 Pad Configuration (cfio_regs_pad_vgpio_1_PCONF0)—Offset 6C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.224 Vgpio 1 Pad Value (cfio_regs_pad_vgpio_1_PAD_VAL)—Offset 6C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

RSVD	RSVD	RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.225 Vgpio 2 Pad Configuration (cfio_regs_pad_vgpio_2_PCONF0)—Offset 6D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Field
31	RSVD
30	RSVD
29	disable_second_mask
28	RSVD
27	direct_irq_en
26	gd_tne
25	gd_tpe
24	gd_level
23	RSVD
22:21	RSVD
20	RSVD
19	RSVD
18	RSVD
17	RSVD
16	RSVD
15	RSVD
14:13	RSVD
12	RSVD
11	bypass_flop
10:9	RSVD
8:7	RSVD
6:5	RSVD
4	RSVD
3	RSVD
2:0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.226 Vgpio 2 Pad Value (cfio_regs_pad_vgpio_2_PAD_VAL)—Offset 6D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3	2	1	0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	1	0	0

Bits	31:22	21:3	2	1	0
Field	RSVD	RSVD	RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.227 Vgpio 3 Pad Configuration (cfio_regs_pad_vgpio_3_PCONF0)—Offset 6E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.228 Vgpio 3 Pad Value (cfio_regs_pad_vgpio_3_PAD_VAL)—Offset 6E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RSVD										RSVD																			RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.229 Vgpio 4 Pad Configuration (cfio_regs_pad_vgpio_4_PCONF0)—Offset 6F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 6F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.230 Vgpio 4 Pad Value (cfio_regs_pad_vgpio_4_PAD_VAL)—Offset 6F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 6F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD										RSVD																			RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.231 Vgpio 5 Pad Configuration (cfio_regs_pad_vgpio_5_PCONF0)—Offset 700h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 700h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	0 0	0	1	0 0	0 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	bypass_flop	RSVD	RSVD	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.232 Vgpio 5 Pad Value (cfio_regs_pad_vgpio_5_PAD_VAL)—Offset 708h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 708h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Fields: RSVD | RSVD | RSVD | ioutenb | pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.233 Vgpio 6 Pad Configuration (cfio_regs_pad_vgpio_6_PCONF0)—Offset 710h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 710h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD | RSVD | disable_second_mask | RSVD | direct_irq_en | gd_tne | gd_tpe | gd_level | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | bypass_flop | RSVD | RSVD | RSVD | RSVD | RSVD | func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.234 Vgpio 6 Pad Value (cfio_regs_pad_vgpio_6_PAD_VAL)—Offset 718h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 718h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 31:22	Bits 21:3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.235 Vgpio 7 Pad Configuration (cfio_regs_pad_vgpio_7_PCONF0)—Offset 720h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 720h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.236 Vgpio 7 Pad Value (cfio_regs_pad_vgpio_7_PAD_VAL)—Offset 728h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 728h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RSVD										RSVD																			RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.237 Vgpio 8 Pad Configuration (cfio_regs_pad_vgpio_8_PCONF0)—Offset 730h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 730h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.238 Vgpio 8 Pad Value (cfio_regs_pad_vgpio_8_PAD_VAL)—Offset 738h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 738h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

RSVD (31:22), RSVD (21:3), RSVD (2), ioutenb (1), pad_val (0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.239 Vgpio 9 Pad Configuration (cfio_regs_pad_vgpio_9_PCONF0)—Offset 740h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 740h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.240 Vgpio 9 Pad Value (cfio_regs_pad_vgpio_9_PAD_VAL)—Offset 748h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 748h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

RSVD (31:22)	RSVD (21:3)	RSVD (2)	ioutenb (1)	pad_val (0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.241 Vgpio 10 Pad Configuration (cfio_regs_pad_vgpio_10_PCONF0)—Offset 750h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 750h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	0 0	0	1	0 0	0 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	bypass_flop	RSVD	RSVD	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.242 Vgpio 10 Pad Value (cfio_regs_pad_vgpio_10_PAD_VAL)—Offset 758h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 758h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Fields: RSVD | RSVD | RSVD | ioutenb | pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.243 Vgpio 11 Pad Configuration (cfio_regs_pad_vgpio_11_PCONF0)—Offset 760h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 760h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD | RSVD | disable_second_mask | RSVD | direct_irq_en | gd_tne | gd_tpe | gd_level | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | bypass_flop | RSVD | RSVD | RSVD | RSVD | RSVD | func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.244 Vgpio 11 Pad Value (cfio_regs_pad_vgpio_11_PAD_VAL)—Offset 768h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 768h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

Bits	31:22	21:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0
Field	RSVD	RSVD	RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.245 Vgpio 12 Pad Configuration (cfio_regs_pad_vgpio_12_PCONF0)—Offset 770h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 770h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.246 Vgpio 12 Pad Value (cfio_regs_pad_vgpio_12_PAD_VAL)—Offset 778h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 778h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RSVD										RSVD																			RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.247 Vgpio 13 Pad Configuration (cfio_regs_pad_vgpio_13_PCONF0)—Offset 780h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 780h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.248 Vgpio 13 Pad Value (cfio_regs_pad_vgpio_13_PAD_VAL)—Offset 788h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 788h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RSVD										RSVD																			RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.249 Vgpio 14 Pad Configuration (cfio_regs_pad_vgpio_14_PCONF0)—Offset 790h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 790h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.250 Vgpio 14 Pad Value (cfio_regs_pad_vgpio_14_PAD_VAL)—Offset 798h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 798h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

RSVD (31:22)	RSVD (21:3)	RSVD (2)	ioutenb (1)	pad_val (0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.251 Vgpio 15 Pad Configuration (cfio_regs_pad_vgpio_15_PCONF0)—Offset 7A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7A0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.252 Vgpio 15 Pad Value (cfio_regs_pad_vgpio_15_PAD_VAL)—Offset 7A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

RSVD	RSVD	RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.253 Vgpio 16 Pad Configuration (cfio_regs_pad_vgpio_16_PCONF0)—Offset 7B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 7B0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	bypass_flop	RSVD	RSVD	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.254 Vgpio 16 Pad Value (cfio_regs_pad_vgpio_16_PAD_VAL)—Offset 7B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 7B8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 1 0 0

RSVD | RSVD | RSVD | ioutenb | pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.255 Vgpio 17 Pad Configuration (cfio_regs_pad_vgpio_17_PCONF0)—Offset 7C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 7C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.256 Vgpio 17 Pad Value (cfio_regs_pad_vgpio_17_PAD_VAL)—Offset 7C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7C8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

RSVD	RSVD	RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.257 Vgpio 18 Pad Configuration (cfio_regs_pad_vgpio_18_PCONF0)—Offset 7D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	0 0	RSVD
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.258 Vgpio 18 Pad Value (cfio_regs_pad_vgpio_18_PAD_VAL)—Offset 7D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7D8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

Bits	31:22	21:3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0	0
Field	RSVD	RSVD	RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.259 Vgpio 19 Pad Configuration (cfio_regs_pad_vgpio_19_PCONF0)—Offset 7E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7E0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.260 Vgpio 19 Pad Value (cfio_regs_pad_vgpio_19_PAD_VAL)—Offset 7E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7E8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RSVD										RSVD																			RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.261 Vgpio 20 Pad Configuration (cfio_regs_pad_vgpio_20_PCONF0)—Offset 7F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7F0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 20038800h

Bit	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	0 0	0	1	0 0	0 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	bypass_flop	RSVD	RSVD	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	00b RO	**Reserved (RSVD):** Reserved.
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function.

39.8.262 Vgpio 20 Pad Value (cfio_regs_pad_vgpio_20_PAD_VAL)—Offset 7F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 7F8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000004h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
RSVD										RSVD																			RSVD	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	0b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.8.263 TS0 SCORE Interrupt Status 0 (cfio_regs_REG_TS0_SCORE_IRQ_TS_0)—Offset 800h

IRQ TS 0 status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 800h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
status																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RWOC	**Status (status):** Trigger IRQ Status: Write one to clear. This status is reflecting IRQ in MMIO access mode only Bellow is the given list of gpio number and pads, the irq status refers to bit 31 - SDMMC2_D3_CD_B bit 30 - SDMMC2_D2 bit 29 - SDMMC2_D1 bit 28 - SDMMC2_D0 bit 27 - SDMMC2_CLK bit 26 - MMC1_RESET_B bit 25 - SDMMC1_CMD bit 24 - MMC1_D7 bit 23 - MMC1_D6 bit 22 - MMC1_D5 bit 21 - MMC1_D4_SD_WE bit 20 - SDMMC1_D3_CD_B bit 19 - SDMMC1_D2 bit 18 - SDMMC1_D1 bit 17 - SDMMC1_D0 bit 16 - SDMMC1_CLK bit 15 - HDA_DOCKENB bit 14 - HDA_DOCKRSTB bit 13 - HDA_SDI1 bit 12 - HDA_SDI0 bit 11 - HDA_SDO bit 10 - HDA_CLK bit 9 - HDA_SYNC bit 8 - HDA_RSTB bit 7 - PCIE_CLKREQ4B bit 6 - PCIE_CLKREQ3B bit 5 - PCIE_CLKREQ2B bit 4 - PCIE_CLKREQ1B bit 3 - PCIE_CLKREQ0B bit 2 - SATA_LEDN bit 1 - SATA_GP1 bit 0 - SATA_GP0

39.8.264 TS1 SCORE Interrupt Status 1 (cfio_regs_REG_TS1_SCORE_IRQ_TS_1)—Offset 804h

IRQ TS 1 status register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 804h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

status

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RWOC	**Status (status):** Trigger IRQ Status: Write one to clear. This status is reflecting IRQ in MMIO access mode only Bellow is the given list of gpio number and pads, the irq status refers to bit 31 - GP_SSP_2_FS bit 30 - GP_SSP_2_CLK bit 29 - MHSI_CAREADY bit 28 - MHSI_CAFLAG bit 27 - MHSI_CADATA bit 26 - MHSI_ACWAKE bit 25 - MHSI_ACREADY bit 24 - MHSI_ACFLAG bit 23 - MHSI_ACDATA bit 22 - SPKR bit 21 - SMB_ALERTB bit 20 - SMB_CLK bit 19 - SMB_DATA bit 18 - ILB_SERIRQ bit 17 - LPC_CLKRUNB bit 16 - LPC_CLKOUT1 bit 15 - LPC_CLKOUT0 bit 14 - LPC_FRAMEB bit 13 - LPC_AD3 bit 12 - LPC_AD2 bit 11 - LPC_AD1 bit 10 - LPC_AD0 bit 9 - SDMMC3_PWR_EN_B bit 8 - SDMMC3_1P8_EN bit 7 - SDMMC3_CMD bit 6 - SDMMC3_CD_B bit 5 - SDMMC3_D3 bit 4 - SDMMC3_D2 bit 3 - SDMMC3_D1 bit 2 - SDMMC3_D0 bit 1 - SDMMC3_CLK bit 0 - SDMMC2_CMD

39.8.265 TS2 SCORE Interrupt Status 2 (cfio_regs_REG_TS2_SCORE_IRQ_TS_2)—Offset 808h

IRQ TS 2 status register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 808h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

status

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RWOC	**Status (status):** Trigger IRQ Status: Write one to clear. This status is reflecting IRQ in MMIO access mode only Bellow is the given list of gpio number and pads, the irq status refers to bit 31 - PWM1 bit 30 - PWM0 bit 29 - I2C_NFC_SCL bit 28 - I2C_NFC_SDA bit 27 - I2C6_SCL bit 26 - I2C6_SDA bit 25 - I2C5_SCL bit 24 - I2C5_SDA bit 23 - I2C4_SCL bit 22 - I2C4_SDA bit 21 - I2C3_SCL bit 20 - I2C3_SDA bit 19 - I2C2_SCL bit 18 - I2C2_SDA bit 17 - I2C1_SCL bit 16 - I2C1_SDA bit 15 - I2C0_SCL bit 14 - I2C0_SDA bit 13 - UART2_CTS_B bit 12 - UART2_RTS_B bit 11 - UART2_TXD bit 10 - UART2_RXD bit 9 - UART1_CTS_B bit 8 - UART1_RTS_B bit 7 - UART1_TXD bit 6 - UART1_RXD bit 5 - SPI1_CLK bit 4 - SPI1_MOSI bit 3 - SPI1_MISO bit 2 - SPI1_CS0_B bit 1 - GP_SSP_2_TXD bit 0 - GP_SSP_2_RXD

39.8.266 TS3 SCORE Interrupt Status 3 (cfio_regs_REG_TS3_SCORE_IRQ_TS_3)—Offset 80Ch

IRQ TS 3 status register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 80Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

status

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RWOC	**Status (status):** Trigger IRQ Status: Write one to clear. This status is reflecting IRQ in MMIO access mode only Bellow is the given list of gpio number and pads, the irq status refers to bit 5 - PLT_CLK5 bit 4 - PLT_CLK4 bit 3 - PLT_CLK3 bit 2 - PLT_CLK2 bit 1 - PLT_CLK1 bit 0 - PLT_CLK0

39.8.267 C71p1cfiomvscoreaza Compensation Configuration (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_CFG)—Offset 810h

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 810h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

31:19	18	17:16	15	14:11	10	9	8:7	6:3	2	1	0
RSVD	irclk_en	ircintclkperiod	ircen	RSVD	RSVD	RSVD	ircstpcal	RSVD	RSVD	RSVD	ircdfx_select

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RO	**Reserved (RSVD):** Reserved.
18	1b RW	**Irclk En (irclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved as 0x3
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RO	**Reserved (RSVD):** Reserved.
10	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9	0b RO	**Reserved (RSVD):** Reserved.
8:7	01b RW	**Ircstpcal (ircstpcal):** Reseved as 0x1
6:3	0000b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

39.8.268 C71p1cfiomvscoreaza Compensation DFX Override (cfio_regs_fam_c71p1cfiomvscoreaza_FAM_RCOMP_DFX)—Offset 81Ch

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 81Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
ircdfx_pstr																ircdfx_nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** Override strength compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** Override strength compensation n-leg value Should be 50ohm typical corner.

39.8.269 C71p1cfiomvrscoresdio1 Compensation Configuration (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_CFG)—Offset 820h

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 820h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
RSVD													irclk_en	ircintclkperiod		ircen	RSVD				RSVD	RSVD	ircstpcal		RSVD				RSVD	RSVD	ircdfx_select

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RO	**Reserved (RSVD):** Reserved.
18	1b RW	**Irclk En (irclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved as 0x3
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RO	**Reserved (RSVD):** Reserved.
10	0b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.
8:7	01b RW	**Ircstpcal (ircstpcal):** Reseved as 0x1
6:3	0000b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

39.8.270 C71p1cfiomvrscoresdio1 Compensation DFX Override (cfio_regs_fam_c71p1cfiomvrscoresdio1_FAM_RCOMP_DFX)—Offset 82Ch

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 82Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
ircdfx_pstr																ircdfx_nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** Override strength compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** Override strength compensation n-leg value Should be 50ohm typical corner.

39.8.271 C71p1cfiohvrscorepsdio3 Compensation Configuration (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_CFG)—Offset 830h

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 830h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Field	RSVD													ircclk_en	ircintclkperiod		ircen	RSVD				RSVD	RSVD	ircstpcal		RSVD				RSVD	RSVD	ircdfx_select

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RO	**Reserved (RSVD):** Reserved.
18	1b RW	**Ircclk En (ircclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved as 0x3
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RO	**Reserved (RSVD):** Reserved.
10	0b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.
8:7	01b RW	**Ircstpcal (ircstpcal):** Reseved as 0x1
6:3	0000b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

39.8.272 C71p1cfiohvrscorepsdio3 Compensation DFX Override (cfio_regs_fam_c71p1cfiohvrscorepsdio3_FAM_RCOMP_DFX)—Offset 83Ch

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 83Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Fields: ircdfx_pstr (31:16), ircdfx_nstr (15:0)

Bit Range	Default & Access	Field Name (ID): Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** Override strength compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** Override strength compensation n-leg value Should be 50ohm typical corner.

39.8.273 C71p1cfiohvrscoreplpc Compensation Configuration (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_CFG)—Offset 840h

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 840h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Fields: RSVD (31:19), ircclk_en (18), ircintclkperiod (17:16), ircen (15), RSVD (14:11), RSVD (10), RSVD (9), ircstpcal (8:7), RSVD (6:3), RSVD (2), RSVD (1), ircdfx_select (0)

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RO	**Reserved (RSVD):** Reserved.
18	1b RW	**Ircclk En (ircclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved as 0x3

Bit Range	Default & Access	Field Name (ID): Description
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RO	**Reserved (RSVD):** Reserved.
10	0b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.
8:7	01b RW	**Ircstpcal (ircstpcal):** Reseved as 0x1
6:3	0000b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

39.8.274 C71p1cfiohvrscoreplpc Compensation DFX Override (cfio_regs_fam_c71p1cfiohvrscoreplpc_FAM_RCOMP_DFX)—Offset 84Ch

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 84Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
ircdfx_pstr	ircdfx_nstr

Bit Range	Default & Access	Field Name (ID): Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** Override strength compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** Override strength compensation n-leg value Should be 50ohm typical corner.

39.8.275 Aza1 Strength Group (cfio_regs_aza1_STRENGTH)—Offset 850h

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 850h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh

31			28				24				20				16				12				8				4				0
1	0	1	1	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	0
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.276 Clkreq Strength Group (cfio_regs_clkreq_STRENGTH)—Offset 854h

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 854h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used

Bit Range	Default & Access	Field Name (ID): Description
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.277 Crt I2c Clk Strength Group (cfio_regs_crt_i2c_clk_STRENGTH)—Offset 858h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 858h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00020002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0002h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	0002h RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.278 Crt I2c Data Strength Group (cfio_regs_crt_i2c_data_STRENGTH)—Offset 85Ch

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 85Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00020002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0002h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	0002h RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.279 Hsi Strength Group (cfio_regs_hsi_STRENGTH)—Offset 860h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 860h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.280 I2c Strength Group (cfio_regs_i2c_STRENGTH)—Offset 864h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 864h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.281 Lpc Strength Group (cfio_regs_lpc_STRENGTH)—Offset 868h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 868h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh

31			28				24				20				16				12				8				4				0
1	0	1	1	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	0
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.282 Mmc3 Strength Group (cfio_regs_mmc3_STRENGTH)—Offset 86Ch

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 86Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh

31			28				24				20				16				12				8				4				0
1	0	1	1	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	0
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.283 Mvt Mmc3 Strength Group (cfio_regs_mvt_mmc3_STRENGTH)—Offset 870h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 870h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.284 Mvt Rcomp Strength Group (cfio_regs_mvt_rcomp_STRENGTH)—Offset 874h

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 874h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh

31			28				24				20				16				12				8				4				0
1	0	1	1	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	0
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.285 Nfc Strength Group (cfio_regs_nfc_STRENGTH)—Offset 878h

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 878h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.286 Pltclk Strength Group (cfio_regs_pltclk_STRENGTH)—Offset 87Ch

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 87Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.287 Pwm Strength Group (cfio_regs_pwm_STRENGTH)—Offset 880h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 880h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used

Bit Range	Default & Access	Field Name (ID): Description
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.288 Sata Strength Group (cfio_regs_sata_STRENGTH)—Offset 884h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 884h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.289 Smb Strength Group (cfio_regs_smb_STRENGTH)—Offset 888h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 888h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.290 Spi Strength Group (cfio_regs_spi_STRENGTH)—Offset 88Ch

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 88Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.291 Spkr Strength Group (cfio_regs_spkr_STRENGTH)—Offset 890h

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 890h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.292 Ssp Strength Group (cfio_regs_ssp_STRENGTH)—Offset 894h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 894h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.293 Uart1 Strength Group (cfio_regs_uart1_STRENGTH)—Offset 898h

P and N strength register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 898h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.8.294 WR PATH SCORE Master Delay Line Write Address (cfio_regs_DLL_WR_PATH_SCORE_MDL_WRITE_PATH_C_F_ADDR)—Offset 950h

Master delay line write path values

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 950h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00080000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD												sel	RSVD				RSVD														

Bit Range	Default & Access	Field Name (ID): Description
31:20	000h RO	**Reserved (RSVD):** Reserved.
19	1b RW	**Sel (sel):** 0 - Enable Master DLL tuning 1 - Disable Master DLL tuning.
18:15	0000b RO	**Reserved (RSVD):** Reserved.
14:0	0h RO	**Reserved (RSVD):** Reserved.

39.8.295 WR PATH1 MUX SCORE Delay Line Write Multiplexer 1 (cfio_regs_DLL_WR_PATH1_MUX_SCORE_DLL_WRITE_PATH1_MUX)—Offset 954h

Master delay line write path mux values

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 954h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																	dll_mux_2					dll_mux_1					dll_mux_0				

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** SD-Card TX Slave DLL tap select for DDR Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** SDIO TX Slave DLL tap select for DDR Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** eMMC TX Slave DLL tap select for DDR Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).

39.8.296 WR PATH2 MUX SCORE Delay Line Write Multiplexer 2 (cfio_regs_DLL_WR_PATH2_MUX_SCORE_DLL_WRITE_PATH2_MUX)—Offset 958h

Master delay line write path mux values

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 958h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	

Bits 31:15	Bits 14:10	Bits 9:5	Bits 4:0
RSVD	dll_mux_2	dll_mux_1	dll_mux_0

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved (RSVD):** Reserved.
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** SD-Card TX Slave DLL tap select for HS Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** SDIO TX Slave DLL tap select for HS Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** eMMC TX Slave DLL tap select for HS Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).

39.8.297 WR PATH3 MUX SCORE Delay Line Write Multiplexer 3 (cfio_regs_DLL_WR_PATH3_MUX_SCORE_DLL_WRITE_PATH3_MUX)—Offset 95Ch

Master delay line write path mux values

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 95Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD | dll_mux_2 | dll_mux_1 | dll_mux_0

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved (RSVD):** Reserved.
14:10	0h RW	**Dll Mux 2 (dll_mux_2):** SD-Card TX Slave DLL tap select for FS Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).
9:5	0h RW	**Dll Mux 1 (dll_mux_1):** SDIO TX Slave DLL tap select for FS Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).
4:0	0h RW	**Dll Mux 0 (dll_mux_0):** eMMC TX Slave DLL tap select for FS Mode. Adjusts TX Clk to Data spacing in 250ps steps. Valid values are 0 to 10011 (0 to 19 for 0 to 5ns range). Recommended value is 3.5ns (5'b01101).

39.8.298 CTRL SCORE Master Delay Line Fsm Control (cfio_regs_DLL_CTRL_SCORE_MDL_FSM_CTRL)—Offset 970h

Master delay line fsm controller

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 970h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD | ctrl_val | delay_mux_val | swing

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved (RSVD):** Reserved.
12:9	0b RW	**Ctrl Val (ctrl_val):** fsm control value bit 3: Local Reset 2: Enable FSM 1: Reseved for debug 0: recalibrate
8:4	00000b RW	**Delay Mux Val (delay_mux_val):** fsm delay mux value to select how many delay cells master dll should use to lock on 5ns. If value is too low, DLL might not succeed to lock. Recomended value is 19 (highest posible), to allow smallest margin.
3:0	0000b RW	**Swing (swing):** number of swings untill the lock in the fsm (from the cfio register). Recomended value 3.

39.8.299 DIRECT IRQ0 SCORE Direct Interrupt Multiplexer 0 (cfio_regs_REG_DIRECT_IRQ0_SCORE_DIRECT_IRQ_0)—Offset 980h

Direct irq select register for irq 0 - 3.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 980h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	direct3							RSVD	direct2							RSVD	direct1							RSVD	direct0						

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30:24	0000000b RW	**Direct3 (direct3):** Selects the 3rd direct irq.
23	0b RO	**Reserved (RSVD):** Reserved.
22:16	0000000b RW	**Direct2 (direct2):**
15	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:8	0000000b RW	**Direct1 (direct1)**
7	0b RO	**Reserved (RSVD):** Reserved.
6:0	0000000b RW	**Direct0 (direct0)**

39.8.300 DIRECT IRQ1 SCORE Direct Interrupt Multiplexer 1 (cfio_regs_REG_DIRECT_IRQ1_SCORE_DIRECT_IRQ_1)—Offset 984h

Direct irq select register for irq 4 - 7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 984h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	30:24	23	22:16	15	14:8	7	6:0
0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0
RSVD	direct7	rsv6	direct6	rsv5	direct5	RSVD	direct4

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30:24	0000000b RW	**Direct7 (direct7):** Selects the 7th direct irq.
23	0b R0	**Rsv6 (rsv6):** reserved
22:16	0000000b RW	**Direct6 (direct6):** Selects the 6th direct irq.
15	0b R0	**Rsv5 (rsv5):** reserved
14:8	0000000b RW	**Direct5 (direct5):** Selects the 5th direct irq.
7	0b RO	**Reserved (RSVD):** Reserved.
6:0	0000000b RW	**Direct4 (direct4):** Selects the 4th direct irq.

39.8.301 DIRECT IRQ2 SCORE Direct Interrupt Multiplexer 2 (cfio_regs_REG_DIRECT_IRQ2_SCORE_DIRECT_IRQ_2)—Offset 988h

Direct irq select register for irq 8 - 11

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 988h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

Bits	31	30:24	23	22:16	15	14:8	7	6:0
Default	0	0000000	0	0000000	0	0000000	0	0000000
Field	RSVD	direct11	RSVD	direct10	RSVD	direct9	RSVD	direct8

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30:24	0000000b RW	**Direct11 (direct11):** Selects the 11th direct irq. S
23	0b RO	**Reserved (RSVD):** Reserved.
22:16	0000000b RW	**Direct10 (direct10):** Selects the 10th direct irq.
15	0b RO	**Reserved (RSVD):** Reserved.
14:8	0000000b RW	**Direct9 (direct9):** Selects the 9th direct irq.
7	0b RO	**Reserved (RSVD):** Reserved.
6:0	0000000b RW	**Direct8 (direct8):** Selects the 8th direct irq.

39.8.302 DIRECT IRQ3 SCORE Direct Interrupt Multiplexer 3 (cfio_regs_REG_DIRECT_IRQ3_SCORE_DIRECT_IRQ_3)—Offset 98Ch

Direct irq select register for irq 12 - 15

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 98Ch

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	30:24	23	22:16	15	14:8	7	6:0
0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0	0	0 0 0 0 0 0 0
RSVD	direct15	rsv14	direct14	RSVD	direct13	RSVD	direct12

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30:24	0000000b RW	**Direct15 (direct15):** Selects the 15th direct irq.
23	0b RO	**Rsv14 (rsv14):** reserved
22:16	0000000b RW	**Direct14 (direct14):** Selects the 14th direct irq. S
15	0b RO	**Reserved (RSVD):** Reserved.
14:8	0000000b RW	**Direct13 (direct13):** Selects the 13th direct irq.
7	0b RO	**Reserved (RSVD):** Reserved.
6:0	0000000b RW	**Direct12 (direct12):** Selects the 12th direct irq. S

39.8.303 E Emmc 4.5 max high speed mux (cfio_regs_SCORE_EMMC_45_HSMAX)—Offset 9A4h

Setting the DLL mux when highest speed is selected

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 9A4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD	tx_dat_dly_sel_sdr104	RSVD	rx_dly_sel_hs200

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.
20:16	0b RW	**Tx Dat Dly Sel Sdr104 (tx_dat_dly_sel_sdr104):** Set the tx delay for sdr104 for eMMC 4.5 clock. Recommended value is 1.5ns (5'b00101).
15:5	0h RO	**Reserved (RSVD):** Reserved.
4:0	0b RW	**Rx Dly Sel Hs200 (rx_dly_sel_hs200):** Set the rx delay for hs200 for eMMC 4.5 clock. Recommended value is 1.5ns (5'b00101).

39.8.304 E Emmc 4.5 sdr50 speed mux (cfio_regs_SCORE_EMMC_45_SDR50)—Offset 9A8h

Setting the DLL mux when sdr50 speed is selected

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 9A8h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD	tx_dat_dly_sel_sdr50	RSVD	rx_dly_sel_sdr50

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:16	0b RW	**Tx Dat Dly Sel Sdr50 (tx_dat_dly_sel_sdr50):** Set the tx delay for sdr50 for eMMC 4.5 clock. Recommended value is 3.5ns (5'b01101).
15:5	0h RO	**Reserved (RSVD):** Reserved.
4:0	0b RW	**Rx Dly Sel Sdr50 (rx_dly_sel_sdr50):** Set the rx delay for sdr50 for eMMC 4.5 clock. Recommended value is 3.5ns (5'b01101).

39.8.305 E Emmc 4.5 ddr50 speed mux (cfio_regs_SCORE_EMMC_45_DDR50)—Offset 9ACh

Setting the DLL mux when ddr50 speed is selected and 1.8v is used

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 9ACh

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

Bits	31:21	20:16	15:5	4:0
Value	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0
Field	RSVD	tx_dat_dly_sel_ddr50	RSVD	rx_dly_sel_ddr50

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.
20:16	0b RW	**Tx Dat Dly Sel Ddr50 (tx_dat_dly_sel_ddr50):** Set the tx delay for ddr50 for eMMC 4.5 clock. Recommended value is 3.5ns (5'b01101).
15:5	0h RO	**Reserved (RSVD):** Reserved.
4:0	0b RW	**Rx Dly Sel Ddr50 (rx_dly_sel_ddr50):** Set the rx delay for ddr50 for eMMC 4.5 clock. Recommended value is 3.5ns (5'b01101).

39.8.306 E Emmc 4.5 hs speed mux (cfio_regs_SCORE_EMMC_45_HS)—Offset 9B0h

Setting the DLL mux when 1. hs speed is selected or 2. ddr 50 and 1.8V Signaling Enable is set to 0. The SDMCC1 IO will still use 1.8V.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [IOBASE] + 9B0h
	IOBASE Type: PCI Configuration Register (Size: 32 bits) **IOBASE Reference:** [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (31:21), tx_dat_dly_sel_hs (20:16), RSVD (15:5), rx_dly_sel_hs (4:0)

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.
20:16	0b RW	**Tx Dat Dly Sel Hs (tx_dat_dly_sel_hs):** Set the tx delay for hs for eMMC 4.5 clock. Recommended value is 3.5ns (5'b01101).
15:5	0h RO	**Reserved (RSVD):** Reserved.
4:0	0b RW	**Rx Dly Sel Hs (rx_dly_sel_hs):** Set the rx delay for hs for eMMC 4.5 clock. Recommended value is 3.5ns (5'b01101).

39.8.307 E Emmc 4.5 norm speed mux (cfio_regs_SCORE_EMMC_45_NORM)—Offset 9B4h

Setting the DLL mux when norm speed is selected

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)	**Offset:** [IOBASE] + 9B4h
	IOBASE Type: PCI Configuration Register (Size: 32 bits) **IOBASE Reference:** [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (31:21), tx_dat_dly_sel_norm (20:16), RSVD (15:5), rx_dly_sel_norm (4:0)

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.
20:16	0b RW	**Tx Dat Dly Sel Norm (tx_dat_dly_sel_norm):** Set the tx delay for norm for eMMC 4.5 clock. Recommended value is 3.5ns (5'b01101).
15:5	0h RO	**Reserved (RSVD):** Reserved.
4:0	0b RW	**Rx Dly Sel Norm (rx_dly_sel_norm):** Set the rx delay for norm for eMMC 4.5 clock. Recommended value is 3.5ns (5'b01101).

39.8.308 E Special configuration bits (cfio_regs_SCORE_SPECIAL_BITS)—Offset 9C0h

The register is holding enable bits for last minutes features, like Mipi hsi active and SDcard input disable when power down

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 9C0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31 … 4	3	2	1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0
RSVD	sdio1_dummy_loopback_en	sdio2_dummy_loopback_en	sdcard_input_gate_en	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD):** Reserved.
3	0b RW	**Sdio1 Dummy Loopback En (sdio1_dummy_loopback_en):** Enable dummy pad loopback to avoid board reflection, for eMMC (4.4.1 and 4.5)
2	0b RW	**Sdio2 Dummy Loopback En (sdio2_dummy_loopback_en):** Enable dummy pad loopback to avoid board reflection, for sdio

Bit Range	Default & Access	Field Name (ID): Description
1	0b RW	**Sdcard Input Gate En (sdcard_input_gate_en):** Enable input disable when sd card power is down. Affect SD card input pads only SDMMC3_D0 SDMMC3_D1 SDMMC3_D2 SDMMC3_D3 SDMMC3_CMD
0	0b RO	**Reserved (RSVD):** Reserved.

39.8.309 E Debounce Control (cfio_regs_SCORE_DEBOUNCE_CTRL)—Offset 9D0h

The register is controlling the community debounce

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE] + 9D0h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31:3	Bits 2:0
reserved	debounce_pulse_cfg

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (reserved):** reserved
2:0	0h RW	**Debounce Pulse Cfg (debounce_pulse_cfg):** This will divide the rtc clock, for generating the pulse of the debounce. When all cleared, pulse will be always high. 3'b001 375us debounce 3'b010 750us debounce 3'b011 1.5ms debounce 3'b100 3ms debounce 3'b101 6ms debounce 3'b110 12ms debounce 3'b111 24ms debounce Recomended values are between 3 to 12 ms

39.8.310 E eMMC 4.5 TAP select register (cfio_regs_SCORE_TAP_SEL_REG)—Offset 9F4h

The register is controlling the community debounce

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE] + 9F4h

IOBASE Type: PCI Configuration Register (Size: 32 bits)
IOBASE Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSVD (bits 31:5), rxclk_tapsel (bits 4:0)

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved (RSVD):** Reserved.
4:0	0h RO	**Rxclk Tapsel (rxclk_tapsel):** This is the actual tap select value for the rx clock of eMMC 4.5

39.9 PCU iLB GPIO S5 IO Addressed Registers

Table 341. Summary of PCU iLB GPIO S5 IO Registers—GBASE + 80h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Sus Use Select 1 (cfio_ioreg_SUS_USE_SEL_31_0_)—Offset 0h" on page 5059	00000000h
4–7h	4	"Sus Io Select 1 (cfio_ioreg_SUS_IO_SEL_31_0_)—Offset 4h" on page 5060	00000000h
8–Bh	4	"Sus Gpio Level 1 (cfio_ioreg_SUS_GP_LVL_31_0_)—Offset 8h" on page 5061	00000000h
C–Fh	4	"Sus Trigger Positive Edge Enable 1 (cfio_ioreg_SUS_TPE_31_0_)—Offset Ch" on page 5062	00000000h
10–13h	4	"Sus Trigger Negative Edge Enable 1 (cfio_ioreg_SUS_TNE_31_0_)—Offset 10h" on page 5063	00000000h
14–17h	4	"Sus Trigger Status 1 (cfio_ioreg_SUS_TS_31_0_)—Offset 14h" on page 5063	00000000h
18–1Bh	4	"Sus Wake Enable 1 (cfio_ioreg_SUS_WAKE_EN_31_0_)—Offset 18h" on page 5065	00000000h
20–23h	4	"Sus Use Select 2 (cfio_ioreg_SUS_USE_SEL_43_32_)—Offset 20h" on page 5066	00000000h
24–27h	4	"Sus Io Select 2 (cfio_ioreg_SUS_IO_SEL_43_32_)—Offset 24h" on page 5066	00000000h
28–2Bh	4	"Sus Gpio Level 2 (cfio_ioreg_SUS_GP_LVL_43_32_)—Offset 28h" on page 5067	00000000h
2C–2Fh	4	"Sus Trigger Positive Edge Enable 2 (cfio_ioreg_SUS_TPE_43_32_)—Offset 2Ch" on page 5068	00000000h
30–33h	4	"Sus Trigger Negative Edge Enable 2 (cfio_ioreg_SUS_TNE_43_32_)—Offset 30h" on page 5069	00000000h
34–37h	4	"Sus Trigger Status (cfio_ioreg_SUS_TS_43_32_)—Offset 34h" on page 5070	00000000h
38–3Bh	4	"Sus Wake Enable 2 (cfio_ioreg_SUS_WAKE_EN_43_32_)—Offset 38h" on page 5071	00000000h

39.9.1 Sus Use Select 1 (cfio_ioreg_SUS_USE_SEL_31_0_)—Offset 0h

Access via PCU Proxy, the register is setting the correspanding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 0h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

use_sel

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Use Select (use_sel):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

39.9.2 Sus Io Select 1 (cfio_ioreg_SUS_IO_SEL_31_0_)—Offset 4h

Access via PCU Proxy, it defines Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 4h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

io_sel

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Io Select (io_sel):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

39.9.3 Sus Gpio Level 1 (cfio_ioreg_SUS_GP_LVL_31_0_)—Offset 8h

Access via PCU Proxy, the registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 8h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

gp_lvl

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Gpio Level (gp_lvl):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

39.9.4 Sus Trigger Positive Edge Enable 1 (cfio_ioreg_SUS_TPE_31_0_)—Offset Ch

Access via PCU Proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [GBASE + 80h] + Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

tpe

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Tpe (tpe):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

39.9.5 Sus Trigger Negative Edge Enable 1 (cfio_ioreg_SUS_TNE_31_0_)—Offset 10h

Access via PCU Proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [GBASE + 80h] + 10h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
tne																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Tne (tne):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

39.9.6 Sus Trigger Status 1 (cfio_ioreg_SUS_TS_31_0_)—Offset 14h

Access via PCU Proxy, When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV and it cannot be tested by the host

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 14h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ts

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WOC	**Ts (ts):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

39.9.7 Sus Wake Enable 1 (cfio_ioreg_SUS_WAKE_EN_31_0_)—Offset 18h

Access via PCU Proxy, Wake Enable: When set to a 1 and TS(n) is set, wake event should be initiated. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 18h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

wake_en

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Wake Enable (wake_en):** bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

39.9.8 Sus Use Select 2 (cfio_ioreg_SUS_USE_SEL_43_32_)—Offset 20h

Access via PCU Proxy, the register is setting the correspanding GPIO to be selected and to be changed to IO access instead of the default Memory access. Bit 0 will set GPIO[0], and bit 1 will set GPIO[1] and so on. The default of IO GPIO pad is input so pull must be activated in the pad pconf0 register.

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [GBASE + 80h] + 20h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved2																				use_sel											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Use Select (use_sel):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

39.9.9 Sus Io Select 2 (cfio_ioreg_SUS_IO_SEL_43_32_)—Offset 24h

Access via PCU Proxy, it defines Input Output Select: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output - Only the 8 lsb are used in VLV. Default values will be read as 0 if IO is not used

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [GBASE + 80h] + 24h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved2																				io_sel											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Io Select (io_sel):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

39.9.10 Sus Gpio Level 2 (cfio_ioreg_SUS_GP_LVL_43_32_)—Offset 28h

This registers are implemented as dual read/write with dedicated storage for write. Write value will be stored in the write register, while read is coming from the pad directly. If GPIO(n) is programmed to be an output (via the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL(n) write register value will drive a high or low value on the output pin. 1 = high, 0 = low. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 28h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved2																				gp_lvl											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (reserved2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11:0	0h RW	**Gpio Level (gp_lvl):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

39.9.11 Sus Trigger Positive Edge Enable 2 (cfio_ioreg_SUS_TPE_43_32_)—Offset 2Ch

Access via PCU Proxy, the register trigger Positive Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 0 to 1 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 0 to 1 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 2Ch

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved2																				tpe											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Tpe (tpe):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

39.9.12 Sus Trigger Negative Edge Enable 2 (cfio_ioreg_SUS_TNE_43_32_)—Offset 30h

Access via PCU Proxy, the register trigger Negative Edge Enable: When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL register) will case an GPE or SMI when a 1 to 0 transition occurs. When set to 0, the GPIO signal is not enabled to trigger an GPE or SMI on a 1 to 0 transition. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 30h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved2																				tne											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Tne (tne):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

39.9.13 Sus Trigger Status (cfio_ioreg_SUS_TS_43_32_)—Offset 34h

Access via PCU Proxy, When set to a 1, the corresponding GPIO (if enabled in the GPIO_USE_SEL register) if enabled as input via IO_SEL(n), triggered an GPE or SMI. This will be set if a 0 to 1 transition occurred and TPE(n) was set, or a 1 to 0 transition occurred and TNE(n) was set. If both TPE(n) and TNE(n) are set, then this bit will be set on both a 0 to 1 and a 1 to 0 transition. This bit will not be set if the GPIO is configured as an output. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 34h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved2																				ts											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h WOC	**Ts (ts):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

39.9.14 Sus Wake Enable 2 (cfio_ioreg_SUS_WAKE_EN_43_32_)—Offset 38h

Access via PCU Proxy, When set to a 1 and TS(n) is set, wake event should be initiated. - Only the 8 lsb are used in VLV

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [GBASE + 80h] + 38h

GBASE Type: PCI Configuration Register (Size: 32 bits)
GBASE Reference: [B:0, D:31, F:0] + 48h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reserved2																				wake_en											

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (reserved2):** Reserved.
11:0	0h RW	**Wake Enable (wake_en):** bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

39.10 PCU iLB GPIO S5 Memory Address Map

Table 342. Summary of iLB GPIO S5 Memory Mapped I/O Registers—IOBASE + 0x2000

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Usb Oc1 B Pad Configuration (cfio_regs_pad_usb_oc1_b_PCONF0)—Offset 0h" on page 5078	2003CC80h
8–Bh	4	"Usb Oc1 B Pad Value (cfio_regs_pad_usb_oc1_b_PAD_VAL)—Offset 8h" on page 5080	00000002h
10–13h	4	"Pmu Wake B Pad Configuration (cfio_regs_pad_pmu_wake_b_PCONF0)—Offset 10h" on page 5081	2003CC80h
18–1Bh	4	"Pmu Wake B Pad Value (cfio_regs_pad_pmu_wake_b_PAD_VAL)—Offset 18h" on page 5084	00000002h
1C–1Fh	4	"Pmu Wake B Pad Test (cfio_regs_pad_pmu_wake_b_PAD_DFT)—Offset 1Ch" on page 5084	00000400h
20–23h	4	"Spi Cs1 B Pad Configuration (cfio_regs_pad_spi_cs1_b_PCONF0)—Offset 20h" on page 5085	2003EC80h
28–2Bh	4	"Spi Cs1 B Pad Value (cfio_regs_pad_spi_cs1_b_PAD_VAL)—Offset 28h" on page 5088	00000002h
30–33h	4	"Spi Cs0 B Pad Configuration (cfio_regs_pad_spi_cs0_b_PCONF0)—Offset 30h" on page 5089	2003E800h
38–3Bh	4	"Spi Cs0 B Pad Value (cfio_regs_pad_spi_cs0_b_PAD_VAL)—Offset 38h" on page 5091	00000002h
40–43h	4	"Spi Clk Pad Configuration (cfio_regs_pad_spi_clk_PCONF0)—Offset 40h" on page 5092	2003E800h
48–4Bh	4	"Spi Clk Pad Value (cfio_regs_pad_spi_clk_PAD_VAL)—Offset 48h" on page 5094	00000002h
50–53h	4	"Spi Mosi Pad Configuration (cfio_regs_pad_spi_mosi_PCONF0)—Offset 50h" on page 5095	2003EC80h
58–5Bh	4	"Spi Mosi Pad Value (cfio_regs_pad_spi_mosi_PAD_VAL)—Offset 58h" on page 5098	00000002h
60–63h	4	"Spi Miso Pad Configuration (cfio_regs_pad_spi_miso_PCONF0)—Offset 60h" on page 5098	2003EC80h
68–6Bh	4	"Spi Miso Pad Value (cfio_regs_pad_spi_miso_PAD_VAL)—Offset 68h" on page 5101	00000006h
70–73h	4	"Suspwrdnack Pad Configuration (cfio_regs_pad_suspwrdnack_PCONF0)—Offset 70h" on page 5102	2003CD00h
78–7Bh	4	"Suspwrdnack Pad Value (cfio_regs_pad_suspwrdnack_PAD_VAL)—Offset 78h" on page 5104	00000002h
7C–7Fh	4	"Suspwrdnack Pad Test (cfio_regs_pad_suspwrdnack_PAD_DFT)—Offset 7Ch" on page 5105	00000400h
80–83h	4	"Pmu Pwrbtn B Pad Configuration (cfio_regs_pad_pmu_pwrbtn_b_PCONF0)—Offset 80h" on page 5106	2003CC80h
88–8Bh	4	"Pmu Pwrbtn B Pad Value (cfio_regs_pad_pmu_pwrbtn_b_PAD_VAL)—Offset 88h" on page 5108	00000002h
90–93h	4	"Pmu Batlow B Pad Configuration (cfio_regs_pad_pmu_batlow_b_PCONF0)—Offset 90h" on page 5109	2003CC80h
98–9Bh	4	"Pmu Batlow B Pad Value (cfio_regs_pad_pmu_batlow_b_PAD_VAL)—Offset 98h" on page 5112	00000006h
9C–9Fh	4	"Pmu Batlow B Pad Test (cfio_regs_pad_pmu_batlow_b_PAD_DFT)—Offset 9Ch" on page 5112	00000400h

Table 342. Summary of iLB GPIO S5 Memory Mapped I/O Registers—IOBASE + 0x2000

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A0–A3h	4	"Pmu Wake Lan B Pad Configuration (cfio_regs_pad_pmu_wake_lan_b_PCONF0)—Offset A0h" on page 5113	2003CC80h
A8–ABh	4	"Pmu Wake Lan B Pad Value (cfio_regs_pad_pmu_wake_lan_b_PAD_VAL)—Offset A8h" on page 5116	00000002h
AC–AFh	4	"Pmu Wake Lan B Pad Test (cfio_regs_pad_pmu_wake_lan_b_PAD_DFT)—Offset ACh" on page 5116	00000400h
B0–B3h	4	"Pmu Susclk Pad Configuration (cfio_regs_pad_pmu_susclk_PCONF0)—Offset B0h" on page 5118	2003CD00h
B8–BBh	4	"Pmu Susclk Pad Value (cfio_regs_pad_pmu_susclk_PAD_VAL)—Offset B8h" on page 5120	00000002h
BC–BFh	4	"Pmu Susclk Pad Test (cfio_regs_pad_pmu_susclk_PAD_DFT)—Offset BCh" on page 5121	00000400h
C0–C3h	4	"Usb Oc0 B Pad Configuration (cfio_regs_pad_usb_oc0_b_PCONF0)—Offset C0h" on page 5122	2003CC80h
C8–CBh	4	"Usb Oc0 B Pad Value (cfio_regs_pad_usb_oc0_b_PAD_VAL)—Offset C8h" on page 5124	00000002h
D0–D3h	4	"Pmu Slp S3 B Pad Configuration (cfio_regs_pad_pmu_slp_s3_b_PCONF0)—Offset D0h" on page 5125	2003C800h
D8–DBh	4	"Pmu Slp S3 B Pad Value (cfio_regs_pad_pmu_slp_s3_b_PAD_VAL)—Offset D8h" on page 5128	00000002h
DC–DFh	4	"Pmu Slp S3 B Pad Test (cfio_regs_pad_pmu_slp_s3_b_PAD_DFT)—Offset DCh" on page 5128	00000400h
E0–E3h	4	"Pmu Ac Present Pad Configuration (cfio_regs_pad_pmu_ac_present_PCONF0)—Offset E0h" on page 5129	2003CD00h
E8–EBh	4	"Pmu Ac Present Pad Value (cfio_regs_pad_pmu_ac_present_PAD_VAL)—Offset E8h" on page 5132	00000006h
EC–EFh	4	"Pmu Ac Present Pad Test (cfio_regs_pad_pmu_ac_present_PAD_DFT)—Offset ECh" on page 5133	00000400h
F0–F3h	4	"Pmu Slp S4 B Pad Configuration (cfio_regs_pad_pmu_slp_s4_b_PCONF0)—Offset F0h" on page 5134	2003C800h
F8–FBh	4	"Pmu Slp S4 B Pad Value (cfio_regs_pad_pmu_slp_s4_b_PAD_VAL)—Offset F8h" on page 5136	00000002h
FC–FFh	4	"Pmu Slp S4 B Pad Test (cfio_regs_pad_pmu_slp_s4_b_PAD_DFT)—Offset FCh" on page 5137	00000400h
100–103h	4	"Pmu Pltrst B Pad Configuration (cfio_regs_pad_pmu_pltrst_b_PCONF0)—Offset 100h" on page 5138	2003C800h
108–10Bh	4	"Pmu Pltrst B Pad Value (cfio_regs_pad_pmu_pltrst_b_PAD_VAL)—Offset 108h" on page 5140	00000002h
10C–10Fh	4	"Pmu Pltrst B Pad Test (cfio_regs_pad_pmu_pltrst_b_PAD_DFT)—Offset 10Ch" on page 5141	00000400h
110–113h	4	"Pmu Slp Lan B Pad Configuration (cfio_regs_pad_pmu_slp_lan_b_PCONF0)—Offset 110h" on page 5142	2003CC80h
118–11Bh	4	"Pmu Slp Lan B Pad Value (cfio_regs_pad_pmu_slp_lan_b_PAD_VAL)—Offset 118h" on page 5145	00000002h
11C–11Fh	4	"Pmu Slp Lan B Pad Test (cfio_regs_pad_pmu_slp_lan_b_PAD_DFT)—Offset 11Ch" on page 5145	00000400h
120–123h	4	"Sec Gpio Sus10 Pad Configuration (cfio_regs_pad_sec_gpio_sus10_PCONF0)—Offset 120h" on page 5146	2003CC80h

Table 342. Summary of iLB GPIO S5 Memory Mapped I/O Registers—IOBASE + 0x2000

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
128–12Bh	4	"Sec Gpio Sus10 Pad Value (cfio_regs_pad_sec_gpio_sus10_PAD_VAL)—Offset 128h" on page 5149	00000002h
130–133h	4	"Sus Stat B Pad Configuration (cfio_regs_pad_sus_stat_b_PCONF0)—Offset 130h" on page 5150	2003CD00h
138–13Bh	4	"Sus Stat B Pad Value (cfio_regs_pad_sus_stat_b_PAD_VAL)—Offset 138h" on page 5152	00000002h
13C–13Fh	4	"Sus Stat B Pad Test (cfio_regs_pad_sus_stat_b_PAD_DFT)—Offset 13Ch" on page 5153	00000400h
140–143h	4	"Pmu Slp S0ix B Pad Configuration (cfio_regs_pad_pmu_slp_s0ix_b_PCONF0)—Offset 140h" on page 5154	2003CD00h
148–14Bh	4	"Pmu Slp S0ix B Pad Value (cfio_regs_pad_pmu_slp_s0ix_b_PAD_VAL)—Offset 148h" on page 5156	00000002h
14C–14Fh	4	"Pmu Slp S0ix B Pad Test (cfio_regs_pad_pmu_slp_s0ix_b_PAD_DFT)—Offset 14Ch" on page 5157	00000400h
150–153h	4	"Gpio Dfx5 Pad Configuration (cfio_regs_pad_gpio_dfx5_PCONF0)—Offset 150h" on page 5158	2003CC80h
158–15Bh	4	"Gpio Dfx5 Pad Value (cfio_regs_pad_gpio_dfx5_PAD_VAL)—Offset 158h" on page 5161	00000002h
160–163h	4	"Gpio Dfx4 Pad Configuration (cfio_regs_pad_gpio_dfx4_PCONF0)—Offset 160h" on page 5161	2003CD00h
168–16Bh	4	"Gpio Dfx4 Pad Value (cfio_regs_pad_gpio_dfx4_PAD_VAL)—Offset 168h" on page 5164	00000002h
170–173h	4	"Gpio Dfx0 Pad Configuration (cfio_regs_pad_gpio_dfx0_PCONF0)—Offset 170h" on page 5165	2003CD00h
178–17Bh	4	"Gpio Dfx0 Pad Value (cfio_regs_pad_gpio_dfx0_PAD_VAL)—Offset 178h" on page 5167	00000002h
180–183h	4	"Gpio Dfx6 Pad Configuration (cfio_regs_pad_gpio_dfx6_PCONF0)—Offset 180h" on page 5168	2003CC80h
188–18Bh	4	"Gpio Dfx6 Pad Value (cfio_regs_pad_gpio_dfx6_PAD_VAL)—Offset 188h" on page 5170	00000002h
190–193h	4	"Gpio Dfx7 Pad Configuration (cfio_regs_pad_gpio_dfx7_PCONF0)—Offset 190h" on page 5171	2003CC80h
198–19Bh	4	"Gpio Dfx7 Pad Value (cfio_regs_pad_gpio_dfx7_PAD_VAL)—Offset 198h" on page 5174	00000002h
1A0–1A3h	4	"Gpio Dfx8 Pad Configuration (cfio_regs_pad_gpio_dfx8_PCONF0)—Offset 1A0h" on page 5174	2003CC80h
1A8–1ABh	4	"Gpio Dfx8 Pad Value (cfio_regs_pad_gpio_dfx8_PAD_VAL)—Offset 1A8h" on page 5177	00000002h
1B0–1B3h	4	"Gpio Dfx3 Pad Configuration (cfio_regs_pad_gpio_dfx3_PCONF0)—Offset 1B0h" on page 5178	2003CD00h
1B8–1BBh	4	"Gpio Dfx3 Pad Value (cfio_regs_pad_gpio_dfx3_PAD_VAL)—Offset 1B8h" on page 5180	00000002h
1C0–1C3h	4	"Gpio Dfx2 Pad Configuration (cfio_regs_pad_gpio_dfx2_PCONF0)—Offset 1C0h" on page 5181	2003CD00h
1C8–1CBh	4	"Gpio Dfx2 Pad Value (cfio_regs_pad_gpio_dfx2_PAD_VAL)—Offset 1C8h" on page 5183	00000002h
1D0–1D3h	4	"Gpio Sus0 Pad Configuration (cfio_regs_pad_gpio_sus0_PCONF0)—Offset 1D0h" on page 5184	2003CC80h

Table 342. Summary of iLB GPIO S5 Memory Mapped I/O Registers—IOBASE + 0x2000

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1D8–1DBh	4	"Gpio Sus0 Pad Value (cfio_regs_pad_gpio_sus0_PAD_VAL)—Offset 1D8h" on page 5187	00000002h
1E0–1E3h	4	"Gpio Sus2 Pad Configuration (cfio_regs_pad_gpio_sus2_PCONF0)—Offset 1E0h" on page 5187	2003CC80h
1E8–1EBh	4	"Gpio Sus2 Pad Value (cfio_regs_pad_gpio_sus2_PAD_VAL)—Offset 1E8h" on page 5190	00000002h
1F0–1F3h	4	"Gpio Sus3 Pad Configuration (cfio_regs_pad_gpio_sus3_PCONF0)—Offset 1F0h" on page 5191	2003CC80h
1F8–1FBh	4	"Gpio Sus3 Pad Value (cfio_regs_pad_gpio_sus3_PAD_VAL)—Offset 1F8h" on page 5193	00000002h
200–203h	4	"Gpio Sus4 Pad Configuration (cfio_regs_pad_gpio_sus4_PCONF0)—Offset 200h" on page 5194	2003CD00h
208–20Bh	4	"Gpio Sus4 Pad Value (cfio_regs_pad_gpio_sus4_PAD_VAL)—Offset 208h" on page 5196	00000002h
210–213h	4	"Gpio Sus1 Pad Configuration (cfio_regs_pad_gpio_sus1_PCONF0)—Offset 210h" on page 5197	2003CC80h
218–21Bh	4	"Gpio Sus1 Pad Value (cfio_regs_pad_gpio_sus1_PAD_VAL)—Offset 218h" on page 5200	00000002h
220–223h	4	"Gpio Sus5 Pad Configuration (cfio_regs_pad_gpio_sus5_PCONF0)—Offset 220h" on page 5201	2003CD00h
228–22Bh	4	"Gpio Sus5 Pad Value (cfio_regs_pad_gpio_sus5_PAD_VAL)—Offset 228h" on page 5203	00000002h
230–233h	4	"Gpio Sus7 Pad Configuration (cfio_regs_pad_gpio_sus7_PCONF0)—Offset 230h" on page 5204	2003CD00h
238–23Bh	4	"Gpio Sus7 Pad Value (cfio_regs_pad_gpio_sus7_PAD_VAL)—Offset 238h" on page 5206	00000002h
240–243h	4	"Gpio Sus6 Pad Configuration (cfio_regs_pad_gpio_sus6_PCONF0)—Offset 240h" on page 5207	2003CD00h
248–24Bh	4	"Gpio Sus6 Pad Value (cfio_regs_pad_gpio_sus6_PAD_VAL)—Offset 248h" on page 5210	00000002h
250–253h	4	"Sec Gpio Sus9 Pad Configuration (cfio_regs_pad_sec_gpio_sus9_PCONF0)—Offset 250h" on page 5210	2003CD00h
258–25Bh	4	"Sec Gpio Sus9 Pad Value (cfio_regs_pad_sec_gpio_sus9_PAD_VAL)—Offset 258h" on page 5213	00000002h
260–263h	4	"Sec Gpio Sus8 Pad Configuration (cfio_regs_pad_sec_gpio_sus8_PCONF0)—Offset 260h" on page 5214	2003CD00h
268–26Bh	4	"Sec Gpio Sus8 Pad Value (cfio_regs_pad_sec_gpio_sus8_PAD_VAL)—Offset 268h" on page 5216	00000002h
270–273h	4	"Gpio Dfx1 Pad Configuration (cfio_regs_pad_gpio_dfx1_PCONF0)—Offset 270h" on page 5217	2003CD00h
278–27Bh	4	"Gpio Dfx1 Pad Value (cfio_regs_pad_gpio_dfx1_PAD_VAL)—Offset 278h" on page 5219	00000002h
280–283h	4	"Usb Ulpi 0 Refclk Pad Configuration (cfio_regs_pad_usb_ulpi_0_refclk_PCONF0)—Offset 280h" on page 5220	2003CD00h
288–28Bh	4	"Usb Ulpi 0 Refclk Pad Value (cfio_regs_pad_usb_ulpi_0_refclk_PAD_VAL)—Offset 288h" on page 5223	00000002h
290–293h	4	"Tck Pad Configuration (cfio_regs_pad_tck_PCONF0)—Offset 290h" on page 5223	2003C900h
298–29Bh	4	"Tck Pad Value (cfio_regs_pad_tck_PAD_VAL)—Offset 298h" on page 5226	00000006h

Table 342. Summary of iLB GPIO S5 Memory Mapped I/O Registers—IOBASE + 0x2000

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2A0–2A3h	4	"Trst B Pad Configuration (cfio_regs_pad_trst_b_PCONF0)—Offset 2A0h" on page 5227	2003C880h
2A8–2ABh	4	"Trst B Pad Value (cfio_regs_pad_trst_b_PAD_VAL)—Offset 2A8h" on page 5229	00000006h
2B0–2B3h	4	"Tdi Pad Configuration (cfio_regs_pad_tdi_PCONF0)—Offset 2B0h" on page 5230	2003C880h
2B8–2BBh	4	"Tdi Pad Value (cfio_regs_pad_tdi_PAD_VAL)—Offset 2B8h" on page 5232	00000006h
2C0–2C3h	4	"Tms Pad Configuration (cfio_regs_pad_tms_PCONF0)—Offset 2C0h" on page 5233	2003C880h
2C8–2CBh	4	"Tms Pad Value (cfio_regs_pad_tms_PAD_VAL)—Offset 2C8h" on page 5236	00000006h
2D0–2D3h	4	"Cx Prdy B Pad Configuration (cfio_regs_pad_cx_prdy_b_PCONF0)—Offset 2D0h" on page 5237	2003C880h
2D8–2DBh	4	"Cx Prdy B Pad Value (cfio_regs_pad_cx_prdy_b_PAD_VAL)—Offset 2D8h" on page 5239	00000002h
2E0–2E3h	4	"Cx Preq B Pad Configuration (cfio_regs_pad_cx_preq_b_PCONF0)—Offset 2E0h" on page 5240	2003C880h
2E8–2EBh	4	"Cx Preq B Pad Value (cfio_regs_pad_cx_preq_b_PAD_VAL)—Offset 2E8h" on page 5243	00000006h
2F0–2F3h	4	"Tdo Pad Configuration (cfio_regs_pad_tdo_PCONF0)—Offset 2F0h" on page 5243	2003C800h
2F8–2FBh	4	"Tdo Pad Value (cfio_regs_pad_tdo_PAD_VAL)—Offset 2F8h" on page 5246	00000002h
300–303h	4	"Usb Ulpi 0 Data4 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data4_PCONF0)—Offset 300h" on page 5247	2003CD00h
308–30Bh	4	"Usb Ulpi 0 Data4 Pad Value (cfio_regs_pad_usb_ulpi_0_data4_PAD_VAL)—Offset 308h" on page 5249	00000002h
310–313h	4	"Usb Ulpi 0 Data2 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data2_PCONF0)—Offset 310h" on page 5250	2003CD00h
318–31Bh	4	"Usb Ulpi 0 Data2 Pad Value (cfio_regs_pad_usb_ulpi_0_data2_PAD_VAL)—Offset 318h" on page 5252	00000002h
320–323h	4	"Usb Ulpi 0 Data6 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data6_PCONF0)—Offset 320h" on page 5253	2003CD00h
328–32Bh	4	"Usb Ulpi 0 Data6 Pad Value (cfio_regs_pad_usb_ulpi_0_data6_PAD_VAL)—Offset 328h" on page 5256	00000002h
330–333h	4	"Usb Ulpi 0 Clk Pad Configuration (cfio_regs_pad_usb_ulpi_0_clk_PCONF0)—Offset 330h" on page 5256	2003CD00h
338–33Bh	4	"Usb Ulpi 0 Clk Pad Value (cfio_regs_pad_usb_ulpi_0_clk_PAD_VAL)—Offset 338h" on page 5259	00000002h
340–343h	4	"Usb Ulpi 0 Dir Pad Configuration (cfio_regs_pad_usb_ulpi_0_dir_PCONF0)—Offset 340h" on page 5260	2003CC80h
348–34Bh	4	"Usb Ulpi 0 Dir Pad Value (cfio_regs_pad_usb_ulpi_0_dir_PAD_VAL)—Offset 348h" on page 5262	00000002h
350–353h	4	"Usb Ulpi 0 Nxt Pad Configuration (cfio_regs_pad_usb_ulpi_0_nxt_PCONF0)—Offset 350h" on page 5263	2003CD00h
358–35Bh	4	"Usb Ulpi 0 Nxt Pad Value (cfio_regs_pad_usb_ulpi_0_nxt_PAD_VAL)—Offset 358h" on page 5265	00000002h
360–363h	4	"Usb Ulpi 0 Data1 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data1_PCONF0)—Offset 360h" on page 5266	2003CD00h
368–36Bh	4	"Usb Ulpi 0 Data1 Pad Value (cfio_regs_pad_usb_ulpi_0_data1_PAD_VAL)—Offset 368h" on page 5269	00000002h

Table 342. Summary of iLB GPIO S5 Memory Mapped I/O Registers—IOBASE + 0x2000

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
370–373h	4	"Usb Ulpi 0 Data3 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data3_PCONF0)—Offset 370h" on page 5269	2003CD00h
378–37Bh	4	"Usb Ulpi 0 Data3 Pad Value (cfio_regs_pad_usb_ulpi_0_data3_PAD_VAL)—Offset 378h" on page 5272	00000002h
380–383h	4	"Usb Ulpi 0 Data0 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data0_PCONF0)—Offset 380h" on page 5273	2003CD00h
388–38Bh	4	"Usb Ulpi 0 Data0 Pad Value (cfio_regs_pad_usb_ulpi_0_data0_PAD_VAL)—Offset 388h" on page 5275	00000002h
390–393h	4	"Usb Ulpi 0 Data5 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data5_PCONF0)—Offset 390h" on page 5276	2003CD00h
398–39Bh	4	"Usb Ulpi 0 Data5 Pad Value (cfio_regs_pad_usb_ulpi_0_data5_PAD_VAL)—Offset 398h" on page 5278	00000002h
3A0–3A3h	4	"Usb Ulpi 0 Data7 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data7_PCONF0)—Offset 3A0h" on page 5279	2003CD00h
3A8–3ABh	4	"Usb Ulpi 0 Data7 Pad Value (cfio_regs_pad_usb_ulpi_0_data7_PAD_VAL)—Offset 3A8h" on page 5282	00000002h
3B0–3B3h	4	"Usb Ulpi 0 Stp Pad Configuration (cfio_regs_pad_usb_ulpi_0_stp_PCONF0)—Offset 3B0h" on page 5282	2003CC80h
3B8–3BBh	4	"Usb Ulpi 0 Stp Pad Value (cfio_regs_pad_usb_ulpi_0_stp_PAD_VAL)—Offset 3B8h" on page 5285	00000002h
610–613h	4	"C71p1cfiomvnsusdfxgpio1 Compensation Configuration (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_CFG)—Offset 610h" on page 5286	00078080h
61C–61Fh	4	"C71p1cfiomvnsusdfxgpio1 Compensation DFX Override (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_DFX)—Offset 61Ch" on page 5287	01000080h
800–803h	4	"TS0 SSUS Interrupt Status 0 (cfio_regs_REG_TS0_SSUS_IRQ_TS_0)—Offset 800h" on page 5287	00000000h
804–807h	4	"TS1 SSUS Interrupt Status 1 (cfio_regs_REG_TS1_SSUS_IRQ_TS_1)—Offset 804h" on page 5288	00000000h
808–80Bh	4	"TS2 SSUS Interrupt Status 2 (cfio_regs_REG_TS2_SSUS_IRQ_TS_2)—Offset 808h" on page 5289	00000000h
80C–80Fh	4	"TS3 SSUS Interrupt Status 3 (cfio_regs_REG_TS3_SSUS_IRQ_TS_3)—Offset 80Ch" on page 5289	00000000h
850–853h	4	"Itp Strength Group (cfio_regs_itp_STRENGTH)—Offset 850h" on page 5290	0003000Fh
854–857h	4	"Sus Rcomp Strength Group (cfio_regs_sus_rcomp_STRENGTH)—Offset 854h" on page 5290	BABECAFEh
858–85Bh	4	"Sus Spi Strength Group (cfio_regs_sus_spi_STRENGTH)—Offset 858h" on page 5291	0003000Fh
85C–85Fh	4	"Ulpi Strength Group (cfio_regs_ulpi_STRENGTH)—Offset 85Ch" on page 5291	0003000Fh
980–983h	4	"DIRECT IRQ0 SSUS Direct Interrupt Multiplexer 0 (cfio_regs_REG_DIRECT_IRQ0_SSUS_DIRECT_IRQ_0)—Offset 980h" on page 5292	00000000h

Table 342. Summary of iLB GPIO S5 Memory Mapped I/O Registers—IOBASE + 0x2000

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
984–987h	4	"DIRECT IRQ1 SSUS Direct Interrupt Multiplexer 1 (cfio_regs_REG_DIRECT_IRQ1_SSUS_DIRECT_IRQ_1)—Offset 984h" on page 5293	00000000h
988–98Bh	4	"DIRECT IRQ2 SSUS Direct Interrupt Multiplexer 2 (cfio_regs_REG_DIRECT_IRQ2_SSUS_DIRECT_IRQ_2)—Offset 988h" on page 5294	00000000h
98C–98Fh	4	"DIRECT IRQ3 SSUS Direct Interrupt Multiplexer 3 (cfio_regs_REG_DIRECT_IRQ3_SSUS_DIRECT_IRQ_3)—Offset 98Ch" on page 5295	00000000h

39.10.1 Usb Oc1 B Pad Configuration (cfio_regs_pad_usb_oc1_b_PCONF0)—Offset 0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is USB_OC1_B function 1 is GPIOS_20

39.10.2 Usb Oc1 B Pad Value (cfio_regs_pad_usb_oc1_b_PAD_VAL)—Offset 8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD											RSVD																		iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.3 Pmu Wake B Pad Configuration (cfio_regs_pad_pmu_wake_b_PCONF0)—Offset 10h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 10h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_WAKE_B function 1 is GPIOS_15

39.10.4 Pmu Wake B Pad Value (cfio_regs_pad_pmu_wake_b_PAD_VAL)—Offset 18h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 18h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RSVD	RSVD	iinenb	ioutenb	pad_val
31:22	21:3	2	1	0

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.5 Pmu Wake B Pad Test (cfio_regs_pad_pmu_wake_b_PAD_DFT)—Offset 1Ch

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

Bits	31:11	10	9:6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0 0 0 0	0	0	0	0	0	0
Field	RSVD	bscan_bypass	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.6 Spi Cs1 B Pad Configuration (cfio_regs_pad_spi_cs1_b_PCONF0)—Offset 20h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 20h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SPI_CS1_B function 1 is GPIOS_21

39.10.7 Spi Cs1 B Pad Value (cfio_regs_pad_spi_cs1_b_PAD_VAL)—Offset 28h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 28h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.8 Spi Cs0 B Pad Configuration (cfio_regs_pad_spi_cs0_b_PCONF0)—Offset 30h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 30h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003E800h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 1	0	1	0 0	0 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl	RSVD	bypass_flop	RSVD	RSVD	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SPI_CS0_B

39.10.9 Spi Cs0 B Pad Value (cfio_regs_pad_spi_cs0_b_PAD_VAL)—Offset 38h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 38h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.10 Spi Clk Pad Configuration (cfio_regs_pad_spi_clk_PCONF0)—Offset 40h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 40h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003E800h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	RSVD
26	0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SPI_CLK

39.10.11 Spi Clk Pad Value (cfio_regs_pad_spi_clk_PAD_VAL)—Offset 48h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 48h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

31:22	21:3	2	1	0
RSVD	RSVD	iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.12 Spi Mosi Pad Configuration (cfio_regs_pad_spi_mosi_PCONF0)—Offset 50h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 50h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	RSVD
26	0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	1 1	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SPI_MOSI

39.10.13 Spi Mosi Pad Value (cfio_regs_pad_spi_mosi_PAD_VAL)—Offset 58h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 58h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31:22	Bits 21:3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.14 Spi Miso Pad Configuration (cfio_regs_pad_spi_miso_PCONF0)—Offset 60h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 60h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003EC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	11b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SPI_MISO

39.10.15 Spi Miso Pad Value (cfio_regs_pad_spi_miso_PAD_VAL)—Offset 68h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 68h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

Bits	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Value	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 0

Field	RSVD	RSVD	RSVD	RSVD	pad_val
Bits	31:22	21:3	2	1	0

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.16 Suspwrdnack Pad Configuration (cfio_regs_pad_suspwrdnack_PCONF0)—Offset 70h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 70h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SUSPWRDNACK function 1 is GPIOS_11

39.10.17 Suspwrdnack Pad Value (cfio_regs_pad_suspwrdnack_PAD_VAL)—Offset 78h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 78h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.18 Suspwrdnack Pad Test (cfio_regs_pad_suspwrdnack_PAD_DFT)—Offset 7Ch

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 7Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

Bits	31:11	10	9:6	5	4	3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0 0 0 0	0	0	0	0	0	0
Field	RSVD	bscan_bypass	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.19 Pmu Pwrbtn B Pad Configuration (cfio_regs_pad_pmu_pwrbtn_b_PCONF0)—Offset 80h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 80h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_PWRBTN_B function 1 is GPIOS_16

39.10.20 Pmu Pwrbtn B Pad Value (cfio_regs_pad_pmu_pwrbtn_b_PAD_VAL)—Offset 88h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 88h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31:22	Bits 21:3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.21 Pmu Batlow B Pad Configuration (cfio_regs_pad_pmu_batlow_b_PCONF0)—Offset 90h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 90h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	RSVD
26	0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_BATLOW_B

39.10.22 Pmu Batlow B Pad Value (cfio_regs_pad_pmu_batlow_b_PAD_VAL)—Offset 98h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 98h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Fields: RSVD (31:22), RSVD (21:3), RSVD (2), RSVD (1), pad_val (0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.23 Pmu Batlow B Pad Test (cfio_regs_pad_pmu_batlow_b_PAD_DFT)—Offset 9Ch

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 9Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

31 28 24 20 16 12 8 4 0

0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 1 0 0 | 0 0 0 0 | 0 0 0 0

RSVD | bscan_bypass | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.24 Pmu Wake Lan B Pad Configuration (cfio_regs_pad_pmu_wake_lan_b_PCONF0)—Offset A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + A0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_WAKE_LAN_B function 1 is GPIOS_17

39.10.25 Pmu Wake Lan B Pad Value (cfio_regs_pad_pmu_wake_lan_b_PAD_VAL)—Offset A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + A8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.26 Pmu Wake Lan B Pad Test (cfio_regs_pad_pmu_wake_lan_b_PAD_DFT)—Offset ACh

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + ACh

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
RSVD																					bscan_bypass	RSVD				RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.27 Pmu Susclk Pad Configuration (cfio_regs_pad_pmu_susclk_PCONF0)—Offset B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + B0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_SUSCLK function 1 is GPIOS_12

39.10.28 Pmu Susclk Pad Value (cfio_regs_pad_pmu_susclk_PAD_VAL)—Offset B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + B8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.29 Pmu Susclk Pad Test (cfio_regs_pad_pmu_susclk_PAD_DFT)—Offset BCh

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + BCh

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0

31:11	10	9:6	5	4	3	2	1	0
RSVD	bscan_bypass	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.30 Usb Oc0 B Pad Configuration (cfio_regs_pad_usb_oc0_b_PCONF0)—Offset C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + C0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is USB_OC0_B function 1 is GPIOS_19

39.10.31 Usb Oc0 B Pad Value (cfio_regs_pad_usb_oc0_b_PAD_VAL)—Offset C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + C8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.32 Pmu Slp S3 B Pad Configuration (cfio_regs_pad_pmu_slp_s3_b_PCONF0)—Offset D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + D0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	RSVD
26	0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_SLP_S3_B

39.10.33 Pmu Slp S3 B Pad Value (cfio_regs_pad_pmu_slp_s3_b_PAD_VAL)—Offset D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + D8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.34 Pmu Slp S3 B Pad Test (cfio_regs_pad_pmu_slp_s3_b_PAD_DFT)—Offset DCh

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + DCh

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
RSVD																					bscan_bypass	RSVD				RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.35 Pmu Ac Present Pad Configuration (cfio_regs_pad_pmu_ac_present_PCONF0)—Offset E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + E0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	1 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_AC_PRESENT

39.10.36 Pmu Ac Present Pad Value (cfio_regs_pad_pmu_ac_present_PAD_VAL)—Offset E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + E8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

31:22	21:3	2	1	0
RSVD	RSVD	RSVD	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.37 Pmu Ac Present Pad Test (cfio_regs_pad_pmu_ac_present_PAD_DFT)—Offset ECh

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + ECh

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Fields: RSVD (31:11) | bscan_bypass (10) | RSVD (9:6) | RSVD (5) | RSVD (4) | RSVD (3) | RSVD (2) | RSVD (1) | RSVD (0)

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.38 Pmu Slp S4 B Pad Configuration (cfio_regs_pad_pmu_slp_s4_b_PCONF0)—Offset F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + F0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_SLP_S4_B

39.10.39 Pmu Slp S4 B Pad Value (cfio_regs_pad_pmu_slp_s4_b_PAD_VAL)—Offset F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + F8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.40 Pmu Slp S4 B Pad Test (cfio_regs_pad_pmu_slp_s4_b_PAD_DFT)—Offset FCh

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + FCh

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits 31:11	Bit 10	Bits 9:6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSVD	bscan_bypass	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.41 Pmu Pltrst B Pad Configuration (cfio_regs_pad_pmu_pltrst_b_PCONF0)—Offset 100h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 100h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	RSVD
26	0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	0 0	RSVD
8:7	0 0	RSVD
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_PLTRST_B

39.10.42 Pmu Pltrst B Pad Value (cfio_regs_pad_pmu_pltrst_b_PAD_VAL)—Offset 108h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 108h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD											RSVD																		iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.43 Pmu Pltrst B Pad Test (cfio_regs_pad_pmu_pltrst_b_PAD_DFT)—Offset 10Ch

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 10Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

Bits	31:11	10	9:6	5	4	3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0 0 0 0	0	0	0	0	0	0
Field	RSVD	bscan_bypass	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.44 Pmu Slp Lan B Pad Configuration (cfio_regs_pad_pmu_slp_lan_b_PCONF0)—Offset 110h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 110h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_SLP_LAN_B function 1 is GPIOS_14 function 2 is ULPI_RESET_N

39.10.45 Pmu Slp Lan B Pad Value (cfio_regs_pad_pmu_slp_lan_b_PAD_VAL)—Offset 118h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 118h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.46 Pmu Slp Lan B Pad Test (cfio_regs_pad_pmu_slp_lan_b_PAD_DFT)—Offset 11Ch

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 11Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

Bits	31:11	10	9:6	5	4	3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0 0 0 0	0	0	0	0	0	0
Field	RSVD	bscan_bypass	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.47 Sec Gpio Sus10 Pad Configuration (cfio_regs_pad_sec_gpio_sus10_PCONF0)—Offset 120h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 120h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SEC_GPIO_SUS10 function 1 is Unused function 2 is USH_HBP[12] function 3 is MCSI_LPDEBUG[0] For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10 function 4 is DUN0_MISR_ECC_OUT_A function 5 is DUN1_MISR_ECC_OUT_A

39.10.48 Sec Gpio Sus10 Pad Value (cfio_regs_pad_sec_gpio_sus10_PAD_VAL)—Offset 128h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 128h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.49 Sus Stat B Pad Configuration (cfio_regs_pad_sus_stat_b_PCONF0)—Offset 130h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 130h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	1 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SUS_STAT_B function 1 is GPIOS_18

39.10.50 Sus Stat B Pad Value (cfio_regs_pad_sus_stat_b_PAD_VAL)—Offset 138h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 138h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.51 Sus Stat B Pad Test (cfio_regs_pad_sus_stat_b_PAD_DFT)—Offset 13Ch

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 13Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
RSVD																					bscan_bypass	RSVD				RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.52 Pmu Slp S0ix B Pad Configuration (cfio_regs_pad_pmu_slp_s0ix_b_PCONF0)—Offset 140h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 140h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is PMU_SLP_S0IX_B function 1 is GPIOS_13

39.10.53 Pmu Slp S0ix B Pad Value (cfio_regs_pad_pmu_slp_s0ix_b_PAD_VAL)—Offset 148h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 148h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.54 Pmu Slp S0ix B Pad Test (cfio_regs_pad_pmu_slp_s0ix_b_PAD_DFT)—Offset 14Ch

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 14Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000400h

Bits	31:11	10	9:6	5	4	3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0 0 0 0	0	0	0	0	0	0
Field	RSVD	bscan_bypass	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD):** Reserved.
10	1b RW	**Bscan Bypass (bscan_bypass):** Bypassing the bscan controll
9:6	0000b RO	**Reserved (RSVD):** Reserved.
5	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Reserved (RSVD):** Reserved.

39.10.55 Gpio Dfx5 Pad Configuration (cfio_regs_pad_gpio_dfx5_PCONF0)—Offset 150h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 150h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one

Bit Range	Default & Access	Field Name (ID): Description
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_27 function 1 is SUS_OBS_4 function 2 is USH_CRC_RESET function 3 is ICLKPH1 function 4 is GCLKPH function 5 is Cx_BPM0_TX

39.10.56 Gpio Dfx5 Pad Value (cfio_regs_pad_gpio_dfx5_PAD_VAL)—Offset 158h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 158h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.57 Gpio Dfx4 Pad Configuration (cfio_regs_pad_gpio_dfx4_PCONF0)—Offset 160h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 160h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	1 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_26 function 1 is SUS_OBS_3 function 2 is EXT_TRIG0 function 3 is ICLKPH0 function 4 is HCLKPH function 5 is Cx_BPM3_TX

39.10.58 Gpio Dfx4 Pad Value (cfio_regs_pad_gpio_dfx4_PAD_VAL)—Offset 168h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 168h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.59 Gpio Dfx0 Pad Configuration (cfio_regs_pad_gpio_dfx0_PCONF0)—Offset 170h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 170h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_22 function 1 is SUS_VALID function 2 is Unused function 3 is CCLKPH0[0] function 4 is HFPLLN function 5 is CRTDAC_CNT

39.10.60 Gpio Dfx0 Pad Value (cfio_regs_pad_gpio_dfx0_PAD_VAL)—Offset 178h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 178h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.61 Gpio Dfx6 Pad Configuration (cfio_regs_pad_gpio_dfx6_PCONF0)—Offset 180h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 180h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_28 function 1 is SUS_OBS_5 function 2 is IERR function 3 is DCLKPH[0] function 4 is ICLKPH0 function 5 is Cx_BPM1_TX

39.10.62 Gpio Dfx6 Pad Value (cfio_regs_pad_gpio_dfx6_PAD_VAL)—Offset 188h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 188h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:21	20:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.63 Gpio Dfx7 Pad Configuration (cfio_regs_pad_gpio_dfx7_PCONF0)—Offset 190h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 190h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_29 function 1 is SUS_OBS_6 function 2 is EXT_TRIG1 function 3 is HFPLLN function 4 is ICLKPH1 function 5 is Cx_BPM2_TX

39.10.64 Gpio Dfx7 Pad Value (cfio_regs_pad_gpio_dfx7_PAD_VAL)—Offset 198h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 198h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.65 Gpio Dfx8 Pad Configuration (cfio_regs_pad_gpio_dfx8_PCONF0)—Offset 1A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1A0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_30 function 1 is SUS_OBS_7 function 2 is SECTAP_TDO function 3 is CCK_ACLKPH function 4 is DCLKPH[1] function 5 is Cx_BPM3_TX

39.10.66 Gpio Dfx8 Pad Value (cfio_regs_pad_gpio_dfx8_PAD_VAL)—Offset 1A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1A8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.67 Gpio Dfx3 Pad Configuration (cfio_regs_pad_gpio_dfx3_PCONF0)—Offset 1B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1B0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_25 function 1 is SUS_OBS_2 function 2 is SECTAP_TDO function 3 is GCLKPH function 4 is CCLKPH1[1] function 5 is Cx_BPM2_TX

39.10.68 Gpio Dfx3 Pad Value (cfio_regs_pad_gpio_dfx3_PAD_VAL)—Offset 1B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1B8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.69 Gpio Dfx2 Pad Configuration (cfio_regs_pad_gpio_dfx2_PCONF0)—Offset 1C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1C0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_24 function 1 is SUS_OBS_1 function 2 is CRTSER_OUT function 3 is HCLKPH function 4 is CCLKPH0[1] function 5 is Cx_BPM1_TX

39.10.70 Gpio Dfx2 Pad Value (cfio_regs_pad_gpio_dfx2_PAD_VAL)—Offset 1C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1C8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Value	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.71 Gpio Sus0 Pad Configuration (cfio_regs_pad_gpio_sus0_PCONF0)—Offset 1D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1D0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIO_SUS0 function 1 is RO_BYPASS

39.10.72 Gpio Sus0 Pad Value (cfio_regs_pad_gpio_sus0_PAD_VAL)—Offset 1D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1D8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.73 Gpio Sus2 Pad Configuration (cfio_regs_pad_gpio_sus2_PCONF0)—Offset 1E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1E0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIO_SUS2 function 1 is SEC_TMS function 2 is USH_HBP[19] function 3 is SSA_MISR_DATA_OUT function 4 is DUN0_MISR_CMD_OUT_B function 5 is DUN1_MISR_CMD_OUT_B function 6 is PCI_WAKE2_B function 7 is DFX_VISA_OBS0

39.10.74 Gpio Sus2 Pad Value (cfio_regs_pad_gpio_sus2_PAD_VAL)—Offset 1E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1E8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

31:22	21:3	2	1	0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.75 Gpio Sus3 Pad Configuration (cfio_regs_pad_gpio_sus3_PCONF0)—Offset 1F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1F0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIO_SUS3 function 1 is SEC_TDI function 2 is USH_HBP[18] function 3 is SSA_MISR_S2CREQ function 4 is DUN0_MISR_ECC_OUT_B function 5 is DUN1_MISR_ECC_OUT_B function 6 is PCI_WAKE3_B function 7 is DFX_VISA_OBS1

39.10.76 Gpio Sus3 Pad Value (cfio_regs_pad_gpio_sus3_PAD_VAL)—Offset 1F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 1F8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required

Bit Range	Default & Access	Field Name (ID): Description
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.77 Gpio Sus4 Pad Configuration (cfio_regs_pad_gpio_sus4_PCONF0)—Offset 200h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 200h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIO_SUS4 function 1 is SEC_TDO function 2 is USH_HPB[17] function 3 is SSA_MISR_S2CDAT function 4 is Unused function 5 is Unused function 6 is Unused function 7 is DFX_VISA_OBS2

39.10.78 Gpio Sus4 Pad Value (cfio_regs_pad_gpio_sus4_PAD_VAL)—Offset 208h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 208h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	28	24	20	16	12	8	4	0
0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0

RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.79 Gpio Sus1 Pad Configuration (cfio_regs_pad_gpio_sus1_PCONF0)—Offset 210h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 210h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

31	28	24	20	16	12	8	4	0
0 0 1	0 0 0 0	0 0 0 0	0 0 1 1	1 1 0 0	1 1 0 0	1 0 0 0	0 0 0 0	0

RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIO_SUS1 function 1 is SEC_TCK For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10 function 2 is USH_CLK0 function 3 is SSA_MISR_CMD_OUT function 4 is DUN0_MISR_CMD_OUT_A function 5 is DUN1_MISR_CMD_OUT_A function 6 is PCI_WAKE1_B function 7 is DFX_VISA_VALID

39.10.80 Gpio Sus1 Pad Value (cfio_regs_pad_gpio_sus1_PAD_VAL)—Offset 218h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 218h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.81 Gpio Sus5 Pad Configuration (cfio_regs_pad_gpio_sus5_PCONF0)—Offset 220h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 220h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit(s)	Default value	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIO_SUS5 function 1 is PMU_SUSCLK1 function 2 is USH_HPB[16] function 3 is SSA_MISR_RPL_OUT function 4 is Unused function 5 is Unused function 6 is Unused function 7 is DFX_VISA_OBS3

39.10.82 Gpio Sus5 Pad Value (cfio_regs_pad_gpio_sus5_PAD_VAL)—Offset 228h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 228h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required

Bit Range	Default & Access	Field Name (ID): Description
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.83 Gpio Sus7 Pad Configuration (cfio_regs_pad_gpio_sus7_PCONF0)—Offset 230h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 230h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIO_SUS7 function 1 is PMU_SUSCLK3 function 2 is USH_HBP[20] function 3 is SSA_MISR_C2CDAT function 4 is Unused function 5 is Unused function 6 is Unused function 7 is DFX_VISA_OBS5

39.10.84 Gpio Sus7 Pad Value (cfio_regs_pad_gpio_sus7_PAD_VAL)—Offset 238h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 238h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.85 Gpio Sus6 Pad Configuration (cfio_regs_pad_gpio_sus6_PCONF0)—Offset 240h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 240h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIO_SUS6 function 1 is PMU_SUSCLK2 function 2 is USH_HBP[15] function 3 is SSA_MISR_C2CREQ function 4 is Unused function 5 is Unused function 6 is Unused function 7 is DFX_VISA_OBS4

39.10.86 Gpio Sus6 Pad Value (cfio_regs_pad_gpio_sus6_PAD_VAL)—Offset 248h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 248h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31 … 28	27 … 24	23 … 20	19 … 16	15 … 12	11 … 8	7 … 4	3 … 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0

Fields: RSVD (31:22), RSVD (21:3), iinenb (2), ioutenb (1), pad_val (0)

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.87 Sec Gpio Sus9 Pad Configuration (cfio_regs_pad_sec_gpio_sus9_PCONF0)—Offset 250h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 250h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SEC_GPIO_SUS9 function 1 is Unused function 2 is USH_HBP[13] function 3 is MCSI_LPDEBUG[1] function 4 is DUN0_MISR_DATA_OUT_B function 5 is DUN1_MISR_DATA_OUT_B function 6 is Unused function 7 is DFX_VISA_OBS7

39.10.88 Sec Gpio Sus9 Pad Value (cfio_regs_pad_sec_gpio_sus9_PAD_VAL)—Offset 258h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 258h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.89 Sec Gpio Sus8 Pad Configuration (cfio_regs_pad_sec_gpio_sus8_PCONF0)—Offset 260h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 260h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	1 0	0 0	0	0	0 0 0
RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is SEC_GPIO_SUS8 function 1 is Unused function 2 is USH_HBP[14] function 3 is MCSI_LPDEBUG[2] function 4 is DUN0_MISR_DATA_OUT_A function 5 is DUN1_MISR_DATA_OUT_A function 6 is Unused function 7 is DFX_VISA_OBS6

39.10.90 Sec Gpio Sus8 Pad Value (cfio_regs_pad_sec_gpio_sus8_PAD_VAL)—Offset 268h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 268h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31:22	Bits 21:3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required

Bit Range	Default & Access	Field Name (ID): Description
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.91 Gpio Dfx1 Pad Configuration (cfio_regs_pad_gpio_dfx1_PCONF0)—Offset 270h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 270h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Value	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad

Bit Range	Default & Access	Field Name (ID): Description
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switching to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter. **Note:** If changing from 0 to 1, it will change to slow clock. If changing from 1 to 0, it will change to fast clock.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924

Bit Range	Default & Access	Field Name (ID): Description
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_23 function 1 is SUS_OBS_0 function 2 is USH_CRC_DEBUG function 3 is CCLKPH1[0] function 4 is GCLKPH function 5 is Cx_BPM0_TX

39.10.92 Gpio Dfx1 Pad Value (cfio_regs_pad_gpio_dfx1_PAD_VAL)—Offset 278h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 278h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.93 Usb Ulpi 0 Refclk Pad Configuration (cfio_regs_pad_usb_ulpi_0_refclk_PCONF0)—Offset 280h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 280h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit(s)	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_43 function 1 is USB_ULPI_0_REFCLK function 2 is USH_HBP[11] function 3 is MCSI_LPDEBUG[3]

39.10.94 Usb Ulpi 0 Refclk Pad Value (cfio_regs_pad_usb_ulpi_0_refclk_PAD_VAL)—Offset 288h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 288h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.95 Tck Pad Configuration (cfio_regs_pad_tck_PCONF0)—Offset 290h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 290h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C900h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is TCK

39.10.96 Tck Pad Value (cfio_regs_pad_tck_PAD_VAL)—Offset 298h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 298h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD										RSVD																			RSVD	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.97 Trst B Pad Configuration (cfio_regs_pad_trst_b_PCONF0)—Offset 2A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2A0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Value	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	0 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is TRST_B

39.10.98 Trst B Pad Value (cfio_regs_pad_trst_b_PAD_VAL)—Offset 2A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2A8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD										RSVD																			RSVD	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.99 Tdi Pad Configuration (cfio_regs_pad_tdi_PCONF0)—Offset 2B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2B0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h

Bits	Value	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	RSVD
26	0	RSVD
25	0	RSVD
24	0	RSVD
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	RSVD
18	0	RSVD
17	1	RSVD
16	1	RSVD
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	0 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is TDI

39.10.100 Tdi Pad Value (cfio_regs_pad_tdi_PAD_VAL)—Offset 2B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2B8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD										RSVD																			RSVD	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.101 Tms Pad Configuration (cfio_regs_pad_tms_PCONF0)—Offset 2C0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2C0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	0 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is TMS

39.10.102 Tms Pad Value (cfio_regs_pad_tms_PAD_VAL)—Offset 2C8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2C8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD										RSVD																			RSVD	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.103 Cx Prdy B Pad Configuration (cfio_regs_pad_cx_prdy_b_PCONF0)—Offset 2D0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2D0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	0 0	0 1	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is CX_PRDY_B For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

39.10.104 Cx Prdy B Pad Value (cfio_regs_pad_cx_prdy_b_PAD_VAL)—Offset 2D8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2D8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0000000000	0000000000000000000	0	1	0
Field	RSVD	RSVD	iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.105 Cx Preq B Pad Configuration (cfio_regs_pad_cx_preq_b_PCONF0)—Offset 2E0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2E0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C880h

31			28				24				20				16				12				8				4				0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0
RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is CX_PREQ_B

39.10.106 Cx Preq B Pad Value (cfio_regs_pad_cx_preq_b_PAD_VAL)—Offset 2E8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2E8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000006h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD										RSVD																			RSVD	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	1b RO	**Reserved (RSVD):** Reserved.
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.107 Tdo Pad Configuration (cfio_regs_pad_tdo_PCONF0)—Offset 2F0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2F0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003C800h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ihysctl		RSVD	bypass_flop	RSVD		RSVD		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RO	**Reserved (RSVD):** Reserved.
26	0b RO	**Reserved (RSVD):** Reserved.
25	0b RO	**Reserved (RSVD):** Reserved.
24	0b RO	**Reserved (RSVD):** Reserved.
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RO	**Reserved (RSVD):** Reserved.
18	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	1b RO	**Slow Clkgate (slow_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
16	1b RO	**Fast Clkgate (fast_clkgate):** Reserved as 1 **Reserved (RSVD):** Reserved.
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	00b RO	**Reserved (RSVD):** Reserved.
8:7	00b RO	**Reserved (RSVD):** Reserved.
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is TDO

39.10.108 Tdo Pad Value (cfio_regs_pad_tdo_PAD_VAL)—Offset 2F8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 2F8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

31:22	21:3	2	1	0
RSVD	RSVD	iinenb	RSVD	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.109 Usb Ulpi 0 Data4 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data4_PCONF0)—Offset 300h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 300h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Value	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_36 function 1 is USB_ULPI_0_DATA4 function 2 is USH_HBP[6] function 3 is MCSI_LPDEBUG[10]

39.10.110 Usb Ulpi 0 Data4 Pad Value (cfio_regs_pad_usb_ulpi_0_data4_PAD_VAL)—Offset 308h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 308h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.111 Usb Ulpi 0 Data2 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data2_PCONF0)—Offset 310h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 310h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_34 function 1 is USB_ULPI_0_DATA2 function 2 is USH_HBP[8] function 3 is MCSI_LPDEBUG[12]

39.10.112 Usb Ulpi 0 Data2 Pad Value (cfio_regs_pad_usb_ulpi_0_data2_PAD_VAL)—Offset 318h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 318h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.113 Usb Ulpi 0 Data6 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data6_PCONF0)—Offset 320h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 320h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0

Bits	Field
31	RSVD
30	RSVD
29	disable_second_mask
28	RSVD
27	direct_irq_en
26	gd_tne
25	gd_tpe
24	gd_level
23	RSVD
22:21	RSVD
20	RSVD
19	filter_en
18	filter_slow
17	slow_clkgate
16	fast_clkgate
15	RSVD
14:13	ihysctl
12	RSVD
11	bypass_flop
10:9	pull_str
8:7	pull_assign
6:5	RSVD
4	RSVD
3	RSVD
2:0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_38 function 1 is USB_ULPI_0_DATA6 function 2 is USH_HBP[4] function 3 is MCSI_LPDEBUG[8]

39.10.114 Usb Ulpi 0 Data6 Pad Value (cfio_regs_pad_usb_ulpi_0_data6_PAD_VAL)—Offset 328h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 328h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.115 Usb Ulpi 0 Clk Pad Configuration (cfio_regs_pad_usb_ulpi_0_clk_PCONF0)—Offset 330h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 330h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_31 function 1 is USB_ULPI_0_CLK function 2 is USH_HBP_CLK1 function 3 is MCSI_LPDEBUG[15]

39.10.116 Usb Ulpi 0 Clk Pad Value (cfio_regs_pad_usb_ulpi_0_clk_PAD_VAL)—Offset 338h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 338h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.117 Usb Ulpi 0 Dir Pad Configuration (cfio_regs_pad_usb_ulpi_0_dir_PCONF0)—Offset 340h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 340h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_40 function 1 is USB_ULPI_0_DIR function 2 is USH_HBP[2] function 3 is MCSI_LPDEBUG[6] For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

39.10.118 Usb Ulpi 0 Dir Pad Value (cfio_regs_pad_usb_ulpi_0_dir_PAD_VAL)—Offset 348h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 348h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	

Bits 31:22	Bits 21:3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.119 Usb Ulpi 0 Nxt Pad Configuration (cfio_regs_pad_usb_ulpi_0_nxt_PCONF0)—Offset 350h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 350h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD		RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl		RSVD	bypass_flop	pull_str		pull_assign		RSVD		RSVD	RSVD	func_pin_mux		

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_41 function 1 is USB_ULPI_0_NXT function 2 is USH_HBP[1] function 3 is MCSI_LPDEBUG[5]

39.10.120 Usb Ulpi 0 Nxt Pad Value (cfio_regs_pad_usb_ulpi_0_nxt_PAD_VAL)—Offset 358h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 358h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.121 Usb Ulpi 0 Data1 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data1_PCONF0)—Offset 360h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 360h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_33 function 1 is USB_ULPI_0_DATA1 function 2 is USH_HBP[9] function 3 is MCSI_LPDEBUG[13]

39.10.122 Usb Ulpi 0 Data1 Pad Value (cfio_regs_pad_usb_ulpi_0_data1_PAD_VAL)—Offset 368h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 368h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RSVD | RSVD | iinenb | ioutenb | pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.123 Usb Ulpi 0 Data3 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data3_PCONF0)—Offset 370h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 370h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	31	30	29	28	27	26	25	24	23	22:21	20	19	18	17	16	15	14:13	12	11	10:9	8:7	6:5	4	3	2:0
Default	0	0	1	0	0	0	0	0	0	0 0	0	0	0	1	1	1	1 0	0	1	1 0	1 0	0 0	0	0	0 0 0
Field	RSVD	RSVD	disable_second_mask	RSVD	direct_irq_en	gd_tne	gd_tpe	gd_level	RSVD	RSVD	RSVD	filter_en	filter_slow	slow_clkgate	fast_clkgate	RSVD	ihysctl	RSVD	bypass_flop	pull_str	pull_assign	RSVD	RSVD	RSVD	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_35 function 1 is USB_ULPI_0_DATA3 function 2 is USH_HPB[7] function 3 is MCSI_LPDEBUG[11]

39.10.124 Usb Ulpi 0 Data3 Pad Value (cfio_regs_pad_usb_ulpi_0_data3_PAD_VAL)—Offset 378h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 378h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.125 Usb Ulpi 0 Data0 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data0_PCONF0)—Offset 380h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 380h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved

Bit Range	Default & Access	Field Name (ID): Description
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_32 function 1 is USB_ULPI_0_DATA0 function 2 is USH_HBP[10] function 3 is MCSI_LPDEBUG[14]

39.10.126 Usb Ulpi 0 Data0 Pad Value (cfio_regs_pad_usb_ulpi_0_data0_PAD_VAL)—Offset 388h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 388h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD										RSVD																			iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.

Bit Range	Default & Access	Field Name (ID): Description
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.127 Usb Ulpi 0 Data5 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data5_PCONF0)—Offset 390h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 390h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq

Bit Range	Default & Access	Field Name (ID): Description
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_37 function 1 is USB_ULPI_0_DATA5 function 2 is USH_HBP[5] function 3 is MCSI_LPDEBUG[9]

39.10.128 Usb Ulpi 0 Data5 Pad Value (cfio_regs_pad_usb_ulpi_0_data5_PAD_VAL)—Offset 398h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 398h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
RSVD											RSVD																		iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.129 Usb Ulpi 0 Data7 Pad Configuration (cfio_regs_pad_usb_ulpi_0_data7_PCONF0)—Offset 3A0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 3A0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CD00h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	1 0	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	10b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_39 function 1 is USB_ULPI_0_DATA7 function 2 is USH_HBP[3] function 3 is MCSI_LPDEBUG[7]

39.10.130 Usb Ulpi 0 Data7 Pad Value (cfio_regs_pad_usb_ulpi_0_data7_PAD_VAL)—Offset 3A8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 3A8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

31:22	21:3	2	1	0
RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.131 Usb Ulpi 0 Stp Pad Configuration (cfio_regs_pad_usb_ulpi_0_stp_PCONF0)—Offset 3B0h

PADs Memory space configuration register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 3B0h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 2003CC80h

Bits	Default	Field
31	0	RSVD
30	0	RSVD
29	1	disable_second_mask
28	0	RSVD
27	0	direct_irq_en
26	0	gd_tne
25	0	gd_tpe
24	0	gd_level
23	0	RSVD
22:21	0 0	RSVD
20	0	RSVD
19	0	filter_en
18	0	filter_slow
17	1	slow_clkgate
16	1	fast_clkgate
15	1	RSVD
14:13	1 0	ihysctl
12	0	RSVD
11	1	bypass_flop
10:9	1 0	pull_str
8:7	0 1	pull_assign
6:5	0 0	RSVD
4	0	RSVD
3	0	RSVD
2:0	0 0 0	func_pin_mux

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30	0b RO	**Reserved (RSVD):** Reserved.
29	1b RW	**Disable Second Mask (disable_second_mask):** Reserved as one
28	0b RO	**Reserved (RSVD):** Reserved.
27	0b RW	**Direct Irq En (direct_irq_en):** If this bit is set, interrupt will use direct wire and not shared. This bit should be cleared if io access mode is selected for this pad
26	0b RW	**Gd Tne (gd_tne):** Negative edge detect for general detect event. 0 - No falling edge detect. 1 - Detect falling edge. For level interrupt mode it will enable active low level irq
25	0b RW	**Gd Tpe (gd_tpe):** Positive edge detect for general detect event. 0 - No rising edge detect. 1 - Detect rising edge. For level interrupt mode it will enable active high level irq
24	0b RW	**Gd Level (gd_level):** When this bit is set a level irq will be choose and not edge irq
23	0b RO	**Reserved (RSVD):** Reserved.
22:21	0h RO	**Reserved (RSVD):** Reserved.
20	0b RO	**Reserved (RSVD):** Reserved.
19	0b RW	**Filter En (filter_en):** Enabling the glitch filter.
18	0b RW	**Filter Slow (filter_slow):** Switchg to slow mode glitch filter, using 32KHz clock with 62.5us glitch window filter.
17	1b RW	**Slow Clkgate (slow_clkgate):** Reserved as 1

Bit Range	Default & Access	Field Name (ID): Description
16	1b RW	**Fast Clkgate (fast_clkgate):** Reserved as 1
15	1b RO	**Reserved (RSVD):** Reserved.
14:13	10b RW	**Ihysctl (ihysctl):** Hysteresis control. 00: min vil(V) - 0.61254 max vih(V) - 1.19637 min vil(%) - 36.9 max vih(%) - 63.9 min hysteresis(V) - 0.25232 01: min vil(V) - 0.6391 max vih(V) - 1.19637 min vil(%) - 38.5 max vih(%) - 63.9 min hysteresis(V) - 0.21912 10: min vil(V) - 0.61254 max vih(V) - 1.16991 min vil(%) - 36.9 max vih(%) - 62.3 min hysteresis(V) - 0.22244 11: min vil(V) - 0.6391 max vih(V) - 1.16991 min vil(%) - 38.5 max vih(%) - 62.3 min hysteresis(V) - 0.18924
12	0b RO	**Reserved (RSVD):** Reserved.
11	1b RO	**Bypass Flop (bypass_flop):** Reserved as 1
10:9	10b RW	**Pull Str (pull_str):** Pull strength: 00 - 2K 01 - reserved 10 - 20K 11 - reserved
8:7	01b RW	**Pull Assign (pull_assign):** Pull assignment is only applicable when pad is in input mode. 00 - Non pull 01 - Pull up 10 - Pull down 11 - reserved
6:5	00b RO	**Reserved (RSVD):** Reserved.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	000b RW	**Func Pin Mux (func_pin_mux):** Func_Pin_Mux: Functional Pin Muxing Default function is always 0. These 3 bits are setting the memory function. function 0 is GPIOS_42 function 1 is USB_ULPI_0_STP function 2 is USH_HBP[0] function 3 is MCSI_LPDEBUG[4] For this function, software should make sure it changes the default pull from up to down. pull assign field, bits [8:7] should be set to 2'b10

39.10.132 Usb Ulpi 0 Stp Pad Value (cfio_regs_pad_usb_ulpi_0_stp_PAD_VAL)—Offset 3B8h

PADs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 3B8h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000002h

Bits	31:22	21:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	1	0
Field	RSVD	RSVD	iinenb	ioutenb	pad_val

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved.
21:3	0h RO	**Reserved (RSVD):** Reserved.
2	0b RW	**Iinenb (iinenb):** input disable. 0 - input enabled 1 - input disabled. This bit must be cleared if output readback is required
1	1b RW	**Ioutenb (ioutenb):** output disable. 0 - output enabled 1 - output disabled.
0	0b RW	**Pad Val (pad_val):** Use this bit to set the output value or to read the pin state in memory mapped GPIO mode. Memory mapped GPIO mode is enabled when this configurable pad is set to the GPIO function via its respective func_pn_mux field and only accessed via memory mapped registers. When used as a memory mapped GPIO output, clear both ioutenb and iinenb bits. Even when used as output, the iinenb bit must to cleared to allow this register to reflect the output state.

39.10.133 C71p1cfiomvnsusdfxgpio1 Compensation Configuration (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_CFG)—Offset 610h

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 610h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00078080h

Bits	31:19	18	17:16	15	14:11	10	9	8:7	6:3	2	1	0
Default	0 0 0 0 0 0 0 0 0 0 0 0 0	1	1 1	1	0 0 0 0	0	0	0 1	0 0 0 0	0	0	0
Field	RSVD	ircclk_en	ircintclkperiod	ircen	RSVD	RSVD	RSVD	ircstpcal	RSVD	RSVD	RSVD	ircdfx_select

Bit Range	Default & Access	Field Name (ID): Description
31:19	0000h RO	**Reserved (RSVD):** Reserved.
18	1b RW	**Ircclk En (ircclk_en):** This is enabling the rcomp clock. When rcomp clock is gated, rcomp reset is forced too, so when it is ungated again it will compensate
17:16	11b RW	**Ircintclkperiod (ircintclkperiod):** reserved as 0x3
15	1b RW	**Ircen (ircen):** Enable RCOMP state machine for periodic RCOMP mode. This has to be enabled throughout periodic mode .0 state machine disabled 1 state machine enabled (default)
14:11	0000b RO	**Reserved (RSVD):** Reserved.
10	0b RO	**Reserved (RSVD):** Reserved.
9	0b RO	**Reserved (RSVD):** Reserved.
8:7	01b RW	**Ircstpcal (ircstpcal):** Reseved as 0x1
6:3	0000b RO	**Reserved (RSVD):** Reserved.
2	0b RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**Ircdfx Select (ircdfx_select):** Bypass RCOMP calibration values and use DFX values instead. Setting this bit (1) would let ircdfx_pstr and ircdfx_nstr value loaded into all buffers.

39.10.134 C71p1cfiomvnsusdfxgpio1 Compensation DFX Override (cfio_regs_fam_c71p1cfiomvnsusdfxgpio1_FAM_RCOMP_DFX)—Offset 61Ch

FAMs Memory space Value register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 61Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 01000080h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits 31:16	Bits 15:0
ircdfx_pstr	ircdfx_nstr

Bit Range	Default & Access	Field Name (ID): Description
31:16	0100h RW	**Ircdfx Pstr (ircdfx_pstr):** Override strength compensation p-leg value. Should be 50ohm typical corner.
15:0	0080h RW	**Ircdfx Nstr (ircdfx_nstr):** Override strength compensation n-leg value Should be 50ohm typical corner.

39.10.135 TS0 SSUS Interrupt Status 0 (cfio_regs_REG_TS0_SSUS_IRQ_TS_0)—Offset 800h

IRQ TS 0 status register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 800h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
status																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RWOC	**Status (status):** Trigger IRQ Status: Write one to clear. This status is reflecting IRQ in MMIO access mode only Bellow is the given list of gpio number and pads, the irq status refers to bit 31 - USB_ULPI_0_CLK bit 30 - GPIO_DFX8 bit 29 - GPIO_DFX7 bit 28 - GPIO_DFX6 bit 27 - GPIO_DFX5 bit 26 - GPIO_DFX4 bit 25 - GPIO_DFX3 bit 24 - GPIO_DFX2 bit 23 - GPIO_DFX1 bit 22 - GPIO_DFX0 bit 21 - SPI_CS1_B bit 20 - USB_OC1_B bit 19 - USB_OC0_B bit 18 - SUS_STAT_B bit 17 - PMU_WAKE_LAN_B bit 16 - PMU_PWRBTN_B bit 15 - PMU_WAKE_B bit 14 - PMU_SLP_LAN_B bit 13 - PMU_SLP_S0IX_B bit 12 - PMU_SUSCLK bit 11 - SUSPWRDNACK bit 10 - SEC_GPIO_SUS10 bit 9 - SEC_GPIO_SUS9 bit 8 - SEC_GPIO_SUS8 bit 7 - GPIO_SUS7 bit 6 - GPIO_SUS6 bit 5 - GPIO_SUS5 bit 4 - GPIO_SUS4 bit 3 - GPIO_SUS3 bit 2 - GPIO_SUS2 bit 1 - GPIO_SUS1 bit 0 - GPIO_SUS0

39.10.136 TS1 SSUS Interrupt Status 1 (cfio_regs_REG_TS1_SSUS_IRQ_TS_1)—Offset 804h

IRQ TS 1 status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 804h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
status																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RWOC	**Status (status):** Trigger IRQ Status: Write one to clear. This status is reflecting IRQ in MMIO access mode only Bellow is the given list of gpio number and pads, the irq status refers to bit 11 - USB_ULPI_0_REFCLK bit 10 - USB_ULPI_0_STP bit 9 - USB_ULPI_0_NXT bit 8 - USB_ULPI_0_DIR bit 7 - USB_ULPI_0_DATA7 bit 6 - USB_ULPI_0_DATA6 bit 5 - USB_ULPI_0_DATA5 bit 4 - USB_ULPI_0_DATA4 bit 3 - USB_ULPI_0_DATA3 bit 2 - USB_ULPI_0_DATA2 bit 1 - USB_ULPI_0_DATA1 bit 0 - USB_ULPI_0_DATA0

39.10.137 TS2 SSUS Interrupt Status 2 (cfio_regs_REG_TS2_SSUS_IRQ_TS_2)—Offset 808h

IRQ TS 2 status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 808h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

status

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RWOC	**Status (status):** Trigger IRQ Status: Write one to clear. This status is reflecting IRQ in MMIO access mode only Bellow is the given list of gpio number and pads, the irq status refers to

39.10.138 TS3 SSUS Interrupt Status 3 (cfio_regs_REG_TS3_SSUS_IRQ_TS_3)—Offset 80Ch

IRQ TS 3 status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 80Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
status																															

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RWOC	**Status (status):** Trigger IRQ Status: Write one to clear. This status is reflecting IRQ in MMIO access mode only Bellow is the given list of gpio number and pads, the irq status refers to

39.10.139 Itp Strength Group (cfio_regs_itp_STRENGTH)—Offset 850h

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 850h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.10.140 Sus Rcomp Strength Group (cfio_regs_sus_rcomp_STRENGTH)—Offset 854h

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 854h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: BABECAFEh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	0
pstr																nstr															

Bit Range	Default & Access	Field Name (ID): Description
31:16	babeh RO	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	cafeh RO	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.10.141 Sus Spi Strength Group (cfio_regs_sus_spi_STRENGTH)—Offset 858h

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 858h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
							pstr																nstr								

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.10.142 Ulpi Strength Group (cfio_regs_ulpi_STRENGTH)—Offset 85Ch

P and N strength register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 85Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 0003000Fh

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
							pstr																nstr								

Bit Range	Default & Access	Field Name (ID): Description
31:16	0003h RW	**Pstr (pstr):** positive strength - for cfiohvio buffers, only the 2 lsb bits will be used
15:0	000Fh RW	**Nstr (nstr):** negetive strength - for cfiohvio buffers, only the 3 lsb bits will be used

39.10.143 DIRECT IRQ0 SSUS Direct Interrupt Multiplexer 0 (cfio_regs_REG_DIRECT_IRQ0_SSUS_DIRECT_IRQ_0)—Offset 980h

Direct irq select register for irq 0 - 3.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 980h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	direct3							RSVD	direct2							RSVD	direct1							RSVD	direct0						

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30:24	0000000b RW	**Direct3 (direct3):** Selects the 3rd direct irq.
23	0b RO	**Reserved (RSVD):** Reserved.
22:16	0000000b RW	**Direct2 (direct2):** Selects the 2nd direct irq.
15	0b RO	**Reserved (RSVD):** Reserved.
14:8	0000000b RW	**Direct1 (direct1):** Selects the 1st direct irq.
7	0b RO	**Reserved (RSVD):** Reserved.
6:0	0000000b RW	**Direct0 (direct0):** Selects the direct irq 0.

39.10.144 DIRECT IRQ1 SSUS Direct Interrupt Multiplexer 1 (cfio_regs_REG_DIRECT_IRQ1_SSUS_DIRECT_IRQ_1)—Offset 984h

Direct irq select register for irq 4 - 7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 984h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	direct7							rsv6	direct6							rsv5	direct5							RSVD	direct4						

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30:24	0000000b RW	**Direct7 (direct7):** Selects the 7th direct irq.
23	0b RO	**Rsv6 (rsv6):** reserved
22:16	0000000b RW	**Direct6 (direct6):** Selects the 6th direct irq.
15	0b RO	**Rsv5 (rsv5):** reserved
14:8	0000000b RW	**Direct5 (direct5):** Selects the 5th direct irq.
7	0b RO	**Reserved (RSVD):** Reserved.
6:0	0000000b RW	**Direct4 (direct4):** Selects the 4th direct irq.

39.10.145 DIRECT IRQ2 SSUS Direct Interrupt Multiplexer 2 (cfio_regs_REG_DIRECT_IRQ2_SSUS_DIRECT_IRQ_2)—Offset 988h

Direct irq select register for irq 8 - 11

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOBASE + 0x2000] + 988h

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)
IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	30:24	23	22:16	15	14:8	7	6:0
0	0000000	0	0000000	0	0000000	0	0000000
RSVD	direct11	RSVD	direct10	RSVD	direct9	RSVD	direct8

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30:24	0000000b RW	**Direct11 (direct11):** Selects the 11th direct irq.
23	0b RO	**Reserved (RSVD):** Reserved.
22:16	0000000b RW	**Direct10 (direct10):** Selects the 10th direct irq.
15	0b RO	**Reserved (RSVD):** Reserved.
14:8	0000000b RW	**Direct9 (direct9):** Selects the 9th direct irq.
7	0b RO	**Reserved (RSVD):** Reserved.
6:0	0000000b RW	**Direct8 (direct8):** Selects the 8th direct irq.

39.10.146 DIRECT IRQ3 SSUS Direct Interrupt Multiplexer 3 (cfio_regs_REG_DIRECT_IRQ3_SSUS_DIRECT_IRQ_3)—Offset 98Ch

Direct irq select register for irq 12 - 15

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

Offset: [IOBASE + 0x2000] + 98Ch

IOBASE + 0x2000 Type: PCI Configuration Register (Size: 32 bits)

IOBASE + 0x2000 Reference: [B:0, D:31, F:0] + 4Ch

Default: 00000000h

31	30:24	23	22:16	15	14:8	7	6:0
0	0000000	0	0000000	0	0000000	0	0000000
RSVD	direct15	rsv14	direct14	RSVD	direct13	RSVD	direct12

Bit Range	Default & Access	Field Name (ID): Description
31	0b RO	**Reserved (RSVD):** Reserved.
30:24	0000000b RW	**Direct15 (direct15):** Selects the 15th direct irq. S
23	0b RO	**Rsv14 (rsv14):** reserved
22:16	0000000b RW	**Direct14 (direct14):** Selects the 14th direct irq.
15	0b RO	**Reserved (RSVD):** Reserved.
14:8	0000000b RW	**Direct13 (direct13):** Selects the 13th direct irq.
7	0b RO	**Reserved (RSVD):** Reserved.
6:0	0000000b RW	**Direct12 (direct12):** Selects the 12th direct irq.

40 PCU – iLB – Interrupt Decoding and Routing

The interrupt decoder is responsible for receiving interrupt messages from other devices in the SoC and decoding them for consumption by the interrupt router, the PCU – iLB – 8259 Programmable Interrupt Controllers (PIC) and/or the PCU – iLB – IO APIC.

The interrupt router is responsible for mapping each incoming interrupt to the appropriate PIRQx, for consumption by the PCU – iLB – 8259 Programmable Interrupt Controllers (PIC) and/or PCU – iLB – IO APIC.

40.1 Features

40.1.1 Interrupt Decoder

The interrupt decoder receives interrupt messages from devices in the SoC. These interrupts can be split into two primary groups:

- For consumption by the interrupt router
- For consumption by the 8259 PIC

40.1.1.1 For Consumption by the Interrupt Router

When a PCI-mapped device in the SoC asserts or de-asserts an INT[A:D] interrupt, an interrupt message is sent to the decoder. This message is decoded to indicate to the interrupt router which specific interrupt is asserted or de-asserted and which device the INT[A:D] interrupt originated from.

40.1.1.2 For Consumption by the 8259 PIC

When a device in the SoC asserts or de-asserts a legacy interrupt (IRQ), an interrupt message is sent to the decoder. This message is decoded to indicate to the 8259 PIC, which specific interrupt (IRQ[3, 14 or 15]) was asserted or de-asserted.

40.1.2 Interrupt Router

The interrupt router aggregates the INT[A:D] interrupts for each PCI-mapped device in the SoC, received from the interrupt decoder, and the INT[A:D] interrupts direct from the Serialized IRQ controller. It then maps these aggregated interrupts to 8 PCI based interrupts: PIRQ[A:H]. This mapping is configured using the IR[31:0] registers.

PCI based interrupts PIRQ[A:H] are then available for consumption by either the 8259 PICs or the IO-APIC, depending on the configuration of the 8 PIRQx Routing Control Registers: PIRQA, PIQRB, PIRQC, PIRQD, PIRQE, PIRQF, PIRQG, PIRQH.

40.1.2.1 Routing PCI Based Interrupts to 8259 PIC

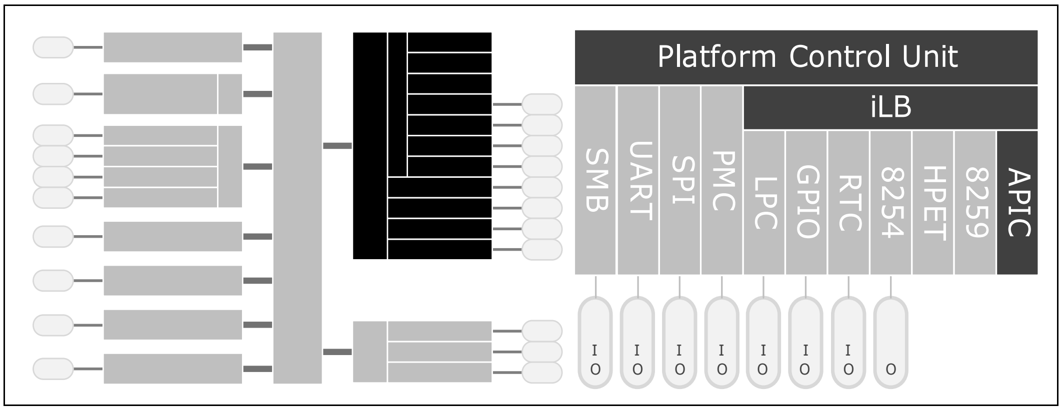
The interrupt router can be programmed to allow PIRQA-PIRQH to be routed internally to the 8259 as ISA compatible interrupts IRQ 3–7, 9–12 & 14–15. The assignment is programmable through the 8 PIRQx Routing Control Registers: PIRQA, PIQRB, PIRQC, PIRQD, PIRQE, PIRQF, PIRQG, PIRQH. One or more PIRQs can be routed to the same IRQ input. If ISA Compatible Interrupts are not required, the Route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive. When a PIRQx# is routed to specified IRQ line, software must change the IRQ's corresponding ELCR bit to level sensitive mode. The SoC internally inverts the PIRQx# line to send an active high level to the PIC. When a PCI interrupt is routed onto the PIC, the selected IRQ can no longer be used by an active high device (through SERIRQ). However, active low interrupts can share their interrupt with PCI interrupts.

§

41 PCU – iLB – IO APIC

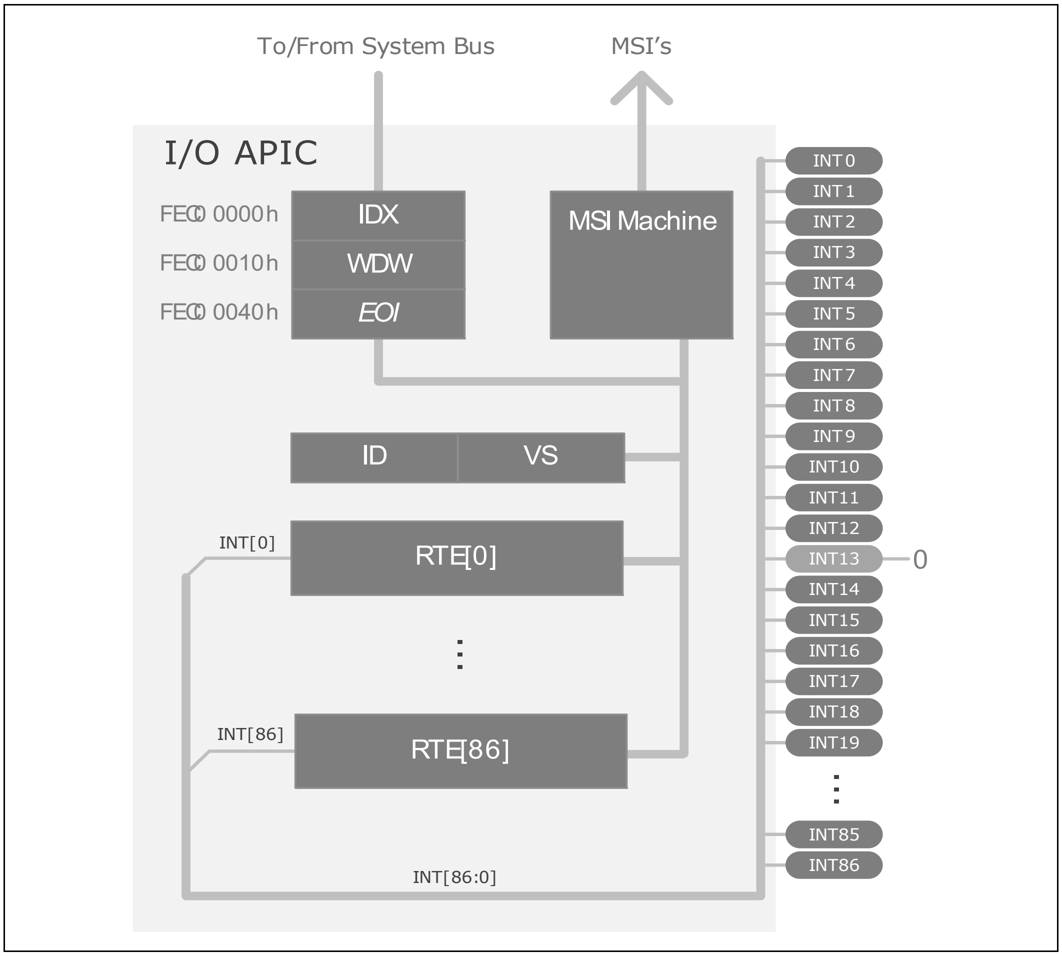
The IO Advanced Programmable Interrupt Controller (APIC) is used to support line interrupts more flexibly than the 8259 PIC. Line interrupts are routed to it from multiple sources, including legacy devices, via the interrupt decoder and serial IRQs, or they are routed to it from the interrupt router in the iLB. These line based interrupts are then used to generate interrupt messages targeting the local APIC in the processor.



41.1 Features

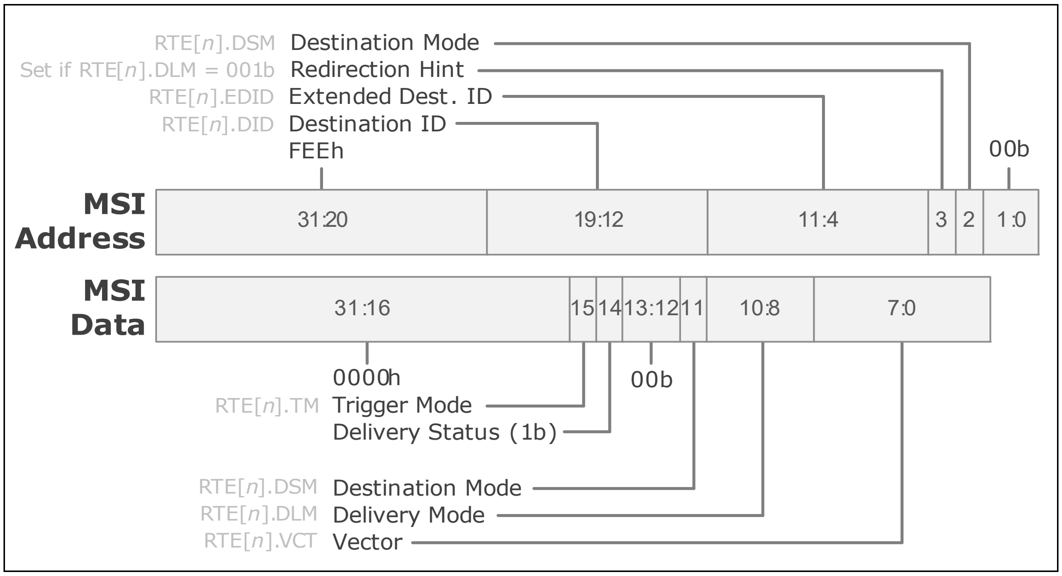
- 87 interrupt lines
  — IRQ0-86
- Edge or level trigger mode per interrupt
- Active low or high polarity per interrupt
- Works with local APIC in processor via MSIs
- MSIs can target specific processor core
- Established APIC programming model

Figure 138.Detailed Block Diagram



MSIs generated by the I/O APIC are sent as 32-bit memory writes to the Local APIC. The address and data of the write transaction are used as follows.

Figure 139.MSI Address and Data



Destination ID (DID) and Extended Destination ID (EDID) are used to target a specific processor core's local APIC.

41.2 Use

The I/O APIC contains indirectly accessed I/O APIC registers and normal memory mapped registers. There are three memory mapped registers:

- Index Register (IDX)
- Window Register (WDW)
- End Of Interrupt Register (EOI)

The Index register selects an indirect I/O APIC register (ID/VS/RTE[*n*]) to appear in the Window register.

The Window register is used to read or write the indirect register selected by the Index register.

The EOI register is written to by the Local APIC in the processor. The I/O APIC compares the lower eight bits written to the EOI register to the Vector set for each interrupt (RTE.VCT). All interrupts that match this vector will have their RTE.RIRR register cleared. All other EOI register bits are ignored.

41.3 Indirect I/O APIC Registers

These registers are selected with the IDX register, and read/written through the WDW register. Accessing these registers must be done as DW requests, otherwise unspecified behavior will result. Software should not attempt to write to reserved registers. Reserved registers may return non-zero values when read.

Note: There is one pair of redirection (RTE) registers per interrupt line. Each pair forms a 64-bit RTE register.

Note: Specified offsets should be placed in IDX, not added to IDX.

§

41.4 PCU iLB IO APIC Memory Mapped I/O Registers

Table 343. Summary of PCU iLB I/O APIC Memory Mapped I/O Registers—

Offset	Size	Register ID—Description	Default Value
FEC00000h	1	"IDX (IOAPIC_IDX)—Offset FEC00000h" on page 5302	00h
FEC00010h	4	"WDW (IOAPIC_WDW)—Offset FEC00010h" on page 5302	00000000h
FEC00040h	4	"EOI (IOAPIC_EOI)—Offset FEC00040h" on page 5303	00000000h

41.4.1 IDX (IOAPIC_IDX)—Offset FEC00000h

Index Register

Access Method

Type: Memory Mapped I/O Register
(Size: 8 bits)

IOAPIC_IDX: FEC00000h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0

11IDX

Bit Range	Default & Access	Description
7:0	0h RW	**IDX:** This 8-bit register selects which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired APIC internal register.

41.4.2 WDW (IOAPIC_WDW)—Offset FEC00010h

Window Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

IOAPIC_WDW: FEC00010h

Default: 00000000h

31			28				24				20				16				12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WDW

Bit Range	Default & Access	Description
31:0	0h RW	**WDW:** This 32-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities.

41.4.3 EOI (IOAPIC_EOI)—Offset FEC00040h

EOI Register

Access Method

Type: Memory Mapped I/O Register
(Size: 32 bits)

IOAPIC_EOI: FEC00040h

Default: 00000000h

31 28 24 20 16 12 8 4 0

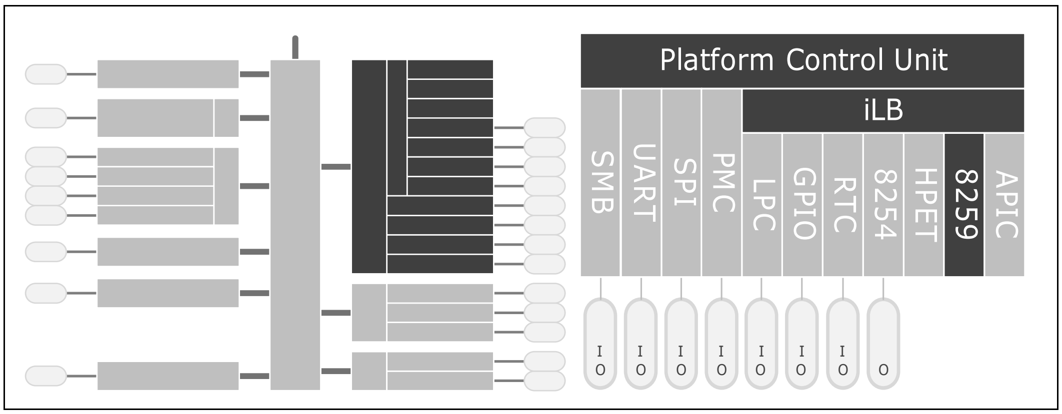
0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

RESERVED1 | EOI

Bit Range	Default & Access	Description
31:8	0b WO	**RESERVED (RESERVED1):** Reserved.
7:0	0h WO	**EOI:** When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared.

42 PCU – iLB – 8259 Programmable Interrupt Controllers (PIC)

The SoC provides an ISA-compatible programmable interrupt controller (PIC) that incorporates the functionality of two, cascaded 8259 interrupt controllers.



42.1 Features

In addition to providing support for ISA compatible interrupts, this interrupt controller can also support PCI based interrupts (PIRQs) by mapping the PCI interrupt onto a compatible ISA interrupt line. Each 8259 controller supports eight interrupts, numbered 0–7. Table 344 shows how the controllers are connected.

Note: The SoC does not implement any external PIRQ# signals. The PIRQs referred to in this chapter originate from the interrupt routing unit.

Table 344. Interrupt Controller Connections

8259	8259 Input	Connected Pin / Function
Master	0	Internal Timer / Counter 0 output or HPET #0; determined by GCFG.LRE register bit
	1	IRQ1 using SERIRQ, Keyboard Emulation
	2	Slave controller INTR output
	3	IRQ3 via SERIRQ or PIRQx
	4	IRQ4 SERIRQ, PIRQx or PCU UART
	5	IRQ5 via SERIRQ or PIRQx
	6	IRQ6 via SERIRQ or PIRQx
	7	IRQ7 via SERIRQ or PIRQx
Slave	0	Inverted IRQ8# from internal RTC or HPET
	1	IRQ9 via SERIRQ, SCI or PIRQx
	2	IRQ10 via SERIRQ, SCI or PIRQx
	3	IRQ11 via SERIRQ, SCI, HPET or PIRQx
	4	IRQ12 via SERIRQ, PIRQx or mouse emulation
	5	None
	6	PIRQx or IRQ14 from SATA controller
	7	IRQ15 via SERIRQ or PIRQx or IRQ15 from SATA controller

The SoC cascades the slave controller onto the master controller through master controller interrupt input 2. This means there are only 15 possible interrupts for the SoC PIC.

Interrupts can be programmed individually to be edge or level, except for IRQ0, IRQ2 and IRQ8#.

Note: Active-low interrupt sources (such as a PIRQ#) are inverted inside the SoC. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term "high" indicates "active," which means "low" on an originating PIRQ#.

42.1.1 Interrupt Handling

42.1.1.1 Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. Table 345 defines the IRR, ISR, and IMR.

Table 345. Interrupt Status Registers

Bit	Description
IRR	**Interrupt Request Register.** This bit is set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode.
ISR	**Interrupt Service Register.** This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
IMR	**Interrupt Mask Register.** This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.

42.1.1.2 Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle that is translated into a Interrupt Acknowledge Cycle to the SoC. The PIC translates this command into two internal INTA# pulses expected by the 8259 controllers. The PIC uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon the ICW2.IVBA bits, combined with the ICW2.IRL bits representing the interrupt within that controller.

Note: References to ICWx and OCWx registers are relevant to both the master and slave 8259 controllers.

Table 346. Content of Interrupt Vector Byte

Master, Slave Interrupt	Bits [7:3]	Bits [2:0]
IRQ7,15	ICW2.IVBA	111
IRQ6,14		110
IRQ5,13		101
IRQ4,12		100
IRQ3,11		011
IRQ2,10		010
IRQ1,9		001
IRQ0,8		000

42.1.1.3 Hardware/Software Interrupt Sequence

1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle.

4. Upon observing the special cycle, the SoC converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast by the master to the slave on a private, internal three bit wide bus. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC returns vector 7 from the master controller.
7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

42.1.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the SoC, this is a four byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the master controller, and A0h for the slave controller.

42.1.2.1 ICW1

A write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the PIC expects three more byte writes to 21h for the master controller, or A1h for the slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
2. The Interrupt Mask Register is cleared.
3. IRQ7 input is assigned priority 7.
4. The slave mode address is set to 7.
5. Special mask mode is cleared and Status Read is set to IRR.

42.1.2.2 ICW2

The second write in the sequence (ICW2) is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

42.1.2.3 ICW3

The third write in the sequence (ICW3) has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the SoC, IRQ2 is used. Therefore, MICW3.CCC is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the master controller broadcasts a code to the slave controller if the cascaded interrupt won arbitration on the master controller. The slave controller compares this identification code to the value stored in its ICW3, and if it matches, the slave controller assumes responsibility for broadcasting the interrupt vector.

42.1.2.4 ICW4

The final write in the sequence (ICW4) must be programmed for both controllers. At the very least, ICW4.MM must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

42.1.3 Operation Command Words (OCW)

These command words reprogram the Interrupt controller to operate in various interrupt modes.

- OCW1 masks and unmasks interrupt lines.
- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 sets up ISR/IRR reads, enables/disables the special mask mode (SMM), and enables/disables polled interrupt mode.

42.1.4 Modes of Operation

42.1.4.1 Fully Nested Mode

In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels generate another interrupt.

Interrupt priorities can be changed in the rotating priority mode.

42.1.4.2 Special Fully-Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully-nested mode is programmed to the master controller. This mode is similar to the fully-nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority interrupts within the slave are recognized by the master and initiate interrupts to the processor. In the normal-nested mode, a slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-Specific EOI command to the slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the master.

42.1.4.3 Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt has to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2.REOI; the Rotation on Non-Specific EOI Command (OCW2.REOI=101b) and the rotate in automatic EOI mode which is set by (OCW2.REOI=100b).

42.1.4.4 Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 is the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: OCW2.REOI=11xb, and OCW2.ILS is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (OCW2.REOI=111b) and OCW2.ILS=IRQ level to receive bottom priority.

42.1.4.5 Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting OCW3.PMC. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read contains a 1 in Bit 7 if there is an interrupt, and the binary code of the highest priority level in Bits 2:0.

42.1.4.6 Edge and Level Triggered Mode

In ISA systems this mode is programmed using ICW1.LTIM, which sets level or edge for the entire controller. In the SoC, this bit is disabled and a register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control Registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low-to-high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector is returned.

42.1.5 End of Interrupt (EOI) Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when the ICW4.AEOI bit is set to 1.

42.1.5.1 Normal End of Interrupt

In normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of operation of the PIC within the SoC, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI.

An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the master and slave controller.

42.1.5.2 Automatic End of Interrupt Mode

In this mode, the PIC automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can only be used in the master controller and not the slave controller.

Note: Both the master and slave PICs have an AEOI bit: MICW4.AEOI and SICW4.AEOI respectively. Only the MICW4.AEOI bit should be set by software. The SICW4.AEOI bit should not be set by software.

42.1.6 Masking Interrupts

42.1.6.1 Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller masks all requests for service from the slave controller.

42.1.6.2 Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The special mask mode enables all interrupts not masked by a bit set in the Mask register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern.

The special mask mode is set by OCW3.ESMM=1b & OCW3.SMM=1b, and cleared where OCW3.ESMM=1b & OCW3.SMM=0b.

42.2 IO Mapped Registers

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ0 - 7), and at A0h and A1h for the slave controller (IRQ8 - 13). These registers have multiple functions, depending upon the data written to them. Table 347 is a description of the different register possibilities for each address.

Note: The register descriptions after Table 347 represent one register possibility.

Table 347. I/O Registers Alias Locations

Registers	Original I/O Location	Alias I/O Locations
MICW1 MOCW2 MOCW3	20h	24h
		28h
		2Ch
		30h
		34h
		38h
		3Ch
MICW2 MICW3 MICW4 MOCW1	21h	25h
		29h
		2Dh
		31h
		35h
		39h
		3Dh
SICW1 SOCW2 SOCW3	A0h	A4h
		A8h
		ACh
		B0h
		B4h
		B8h
		BCh
SICW2 SICW3 SICW4 SOCW1	A1h	A5h
		A9h
		ADh
		B1h
		B5h
		B9h
		BDh
ELCR1	4D0h	N/A
ELCR2	4D1h	N/A

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42.3 PCU iLB 8259 Interrupt Controller (PIC) I/O Registers

Table 348. Summary of PCU iLB 8259 Interrupt Controller (PIC) I/O Registers—

Offset	Size	Register ID—Description	Default Value
20h	1	"MICW1—Offset 20h" on page 5313	00h
21h	1	"MICW2—Offset 21h" on page 5314	00h
24h	1	"MOCW2—Offset 24h" on page 5314	20h
25h	1	"MICW3—Offset 25h" on page 5315	00h
28h	1	"MOCW3—Offset 28h" on page 5315	22h
29h	1	"MICW4—Offset 29h" on page 5316	01h
2Dh	1	"MOCW1—Offset 2Dh" on page 5317	00h
A0h	1	"SICW1—Offset A0h" on page 5317	00h
A1h	1	"SICW2—Offset A1h" on page 5318	00h
A4h	1	"SOCW2—Offset A4h" on page 5319	20h
A5h	1	"SICW3—Offset A5h" on page 5319	00h
A8h	1	"SOCW3—Offset A8h" on page 5320	22h
A9h	1	"SICW4—Offset A9h" on page 5320	01h
ADh	1	"SOCW1—Offset ADh" on page 5321	00h
4D0h	1	"ELCR1—Offset 4D0h" on page 5321	00h
4D1h	1	"ELCR2—Offset 4D1h" on page 5322	00h

42.3.1 MICW1—Offset 20h

Master Initialization Command Word 1.A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs: * The Interrupt Mask register is cleared. * IRQ7 input is assigned priority 7. * The slave mode address is set to 7. * Special Mask Mode is cleared and Status Read is set to IRR. Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: I/O Register
(Size: 8 bits)

MICW1: 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MCS85			ICWOCWSEL	LTIM	ADI	SNGL	IC4

Bit Range	Default & Access	Description
7:5	X WO	**MCS85:** These bits are MCS-85 specific, and not needed. Should be programmed to 000

Bit Range	Default & Access	Description
4	X WO	**ICWOCWSEL:** ICW/OCW select: This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	X WO	**LTIM:** Edge/Level Bank Select (LTIM): Disabled. Replaced by ELCR1 and ELCR2.
2	X WO	**ADI:** ADI. Ignored for VLV. Should be programmed to 0.
1	X WO	**SNGL:** Single or Cascade (SNGL): Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	X WO	**IC4:** wICW4 Write Required (IC4): This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

42.3.2 MICW2—Offset 21h

Master ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: I/O Register
(Size: 8 bits)

MICW2: 21h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IVBA					IRL		

Bit Range	Default & Access	Description
7:3	X WO	**IVBA:** Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	X WO	**IRL:** Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

42.3.3 MOCW2—Offset 24h

Master Operational Control Word 2 (Interrupt Mask).Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: I/O Register
(Size: 8 bits)

MOCW2: 24h

Default: 20h

7			4				0
0	0	1	0	0	0	0	0
REOI			OCW2S		ILS		

Bit Range	Default & Access	Description
7:5	001b WO	**REOI:** Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 - Rotate in Auto EOI Mode (Clear) 001 - Non-specific EOI command 010 - No Operation 011 - *Specific EOI Command 100 - Rotate in Auto EOI Mode (Set) 101 - Rotate on Non-Specific EOI Command 110 - *Set Priority Command 111 - *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	X WO	**OCW2S:** OCW2 Select: When selecting OCW2, bits 4:3 = 00
2:0	X WO	**ILS:** Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Bits Interrupt Level Bits Interrupt Level 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

42.3.4 MICW3—Offset 25h

Master Initialization Command Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

MICW3: 25h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MBZ					CCC	MBZ1	

Bit Range	Default & Access	Description
7:3	X WO	**MBZ:** These bits must be programmed to zero.
2	X WO	**CCC:** Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.
1:0	X WO	**MBZ (MBZ1):** These bits must be programmed to zero.

42.3.5 MOCW3—Offset 28h

Master Operational Control Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

MOCW3: 28h

Default: 22h

7			4				0
0	0	1	0	0	0	1	0
RESERVED	SMM	ESMM	O3S		PMC	RRC	

Bit Range	Default & Access	Description
7	0b RO	**RESERVED:** Reserved. Must be 0.
6	0b WO	**SMM:** Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	1b WO	**ESMM:** Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a don't care.
4:3	X WO	**O3S:** OCW3 Select (O3S): When selecting OCW3, bits 4:3 = 01
2	X WO	**PMC:** Poll Mode Command (PMC): When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	10b WO	**RRC:** Register Read Command (RRC): These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

42.3.6 MICW4—Offset 29h

Master Initialization Command Word 4

Access Method

Type: I/O Register
(Size: 8 bits)

MICW4: 29h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
MBZ			SFNM	BUF	MSBM	AEOI	MM

Bit Range	Default & Access	Description
7:5	X WO	**MBZ:** These bits must be programmed to zero.
4	0b WO	**SFNM:** Special Fully Nested Mode (SFNM): Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.

Bit Range	Default & Access	Description
3	0b WO	**BUF:** Buffered Mode (BUF): Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0b WO	**MSBM:** Master/Slave in Buffered Mode (MSBM): Not used. Should always be programmed to 0.
1	0b WO	**AEOI:** Automatic End of Interrupt (AEOI): This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	1b WO	**MM:** Microprocessor Mode (MM): This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

42.3.7 MOCW1—Offset 2Dh

Master Operational Control Word 1 (Interrupt Mask)

Access Method

Type: I/O Register
(Size: 8 bits)

MOCW1: 2Dh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IRM							

Bit Range	Default & Access	Description
7:0	00h RW	**IRM:** Interrupt Request Mask (IRM): When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

42.3.8 SICW1—Offset A0h

Slave Initialization Command Word 1.A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs: * The Interrupt Mask register is cleared. * IRQ7 input is assigned priority 7. * The slave mode address is set to 7. * Special Mask Mode is cleared and Status Read is set to IRR. Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: I/O Register
(Size: 8 bits)

SICW1: A0h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MCS85			ICWOCWSEL	LTIM	ADI	SNGL	IC4

Bit Range	Default & Access	Description
7:5	X WO	**MCS85:** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	X WO	**ICWOCWSEL:** ICW/OCW select: This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	X WO	**LTIM:** Edge/Level Bank Select (LTIM): Disabled. Replaced by ELCR1 and ELCR2.
2	X WO	**ADI:** ADI. Ignored for VLV. Should be programmed to 0.
1	X WO	**SNGL:** Single or Cascade (SNGL): Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	X WO	**IC4:** wICW4 Write Required (IC4): This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

42.3.9 SICW2—Offset A1h

Slave ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: I/O Register
(Size: 8 bits)

SICW2: A1h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IVBA					IRL		

Bit Range	Default & Access	Description
7:3	X WO	**IVBA:** Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	X WO	**IRL:** Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

42.3.10 SOCW2—Offset A4h

Slave Operational Control Word 2 (Interrupt Mask).Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: I/O Register (Size: 8 bits) **SOCW2:** A4h

Default: 20h

7			4				0
0	0	1	0	0	0	0	0
REOI			OCW2S		ILS		

Bit Range	Default & Access	Description
7:5	001b WO	**REOI:** Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 - Rotate in Auto EOI Mode (Clear) 001 - Non-specific EOI command 010 - No Operation 011 - *Specific EOI Command 100 - Rotate in Auto EOI Mode (Set) 101 - Rotate on Non-Specific EOI Command 110 - *Set Priority Command 111 - *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	X WO	**OCW2S:** OCW2 Select: When selecting OCW2, bits 4:3 = 00
2:0	X WO	**ILS:** Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Bits Interrupt Level Bits Interrupt Level 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

42.3.11 SICW3—Offset A5h

Slave Initialization Command Word 3

Access Method

Type: I/O Register (Size: 8 bits) **SICW3:** A5h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MBZ					CCC	MBZ1	

Bit Range	Default & Access	Description
7:3	X WO	**MBZ:** These bits must be programmed to zero.
2	X WO	**CCC:** Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.

Bit Range	Default & Access	Description
1:0	X WO	**MBZ (MBZ1):** These bits must be programmed to zero.

42.3.12 SOCW3—Offset A8h

Slave Operational Control Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

SOCW3: A8h

Default: 22h

7			4				0
0	0	1	0	0	0	1	0
RESERVED	SMM	ESMM	O3S		PMC	RRC	

Bit Range	Default & Access	Description
7	0b RO	**RESERVED:** Reserved. Must be 0.
6	0b WO	**SMM:** Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	1b WO	**ESMM:** Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a don't care.
4:3	X WO	**O3S:** OCW3 Select (O3S): When selecting OCW3, bits 4:3 = 01
2	X WO	**PMC:** Poll Mode Command (PMC): When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	10b WO	**RRC:** Register Read Command (RRC): These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

42.3.13 SICW4—Offset A9h

Slave Initialization Command Word 4

Access Method

Type: I/O Register
(Size: 8 bits)

SICW4: A9h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
MBZ			SFNM	BUF	MSBM	AEOI	MM

Bit Range	Default & Access	Description
7:5	X WO	**MBZ:** These bits must be programmed to zero.
4	0b WO	**SFNM:** Special Fully Nested Mode (SFNM): Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0b WO	**BUF:** Buffered Mode (BUF): Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0b WO	**MSBM:** Master/Slave in Buffered Mode (MSBM): Not used. Should always be programmed to 0.
1	0b WO	**AEOI:** Automatic End of Interrupt (AEOI): This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	1b WO	**MM:** Microprocessor Mode (MM): This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

42.3.14 SOCW1—Offset ADh

Slave Operational Control Word 1 (Interrupt Mask)

Access Method

Type: I/O Register
(Size: 8 bits)

SOCW1: ADh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IRM							

Bit Range	Default & Access	Description
7:0	00h RW	**IRM:** Interrupt Request Mask (IRM): When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

42.3.15 ELCR1—Offset 4D0h

Master Edge/Level Control

Access Method

Type: I/O Register
(Size: 8 bits)

ELCR1: 4D0h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
ELC					RESERVED		

Bit Range	Default & Access	Description
7:3	X RW	**ELC:** Edge Level Control (ECL[7:3]): In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0b RO	**RESERVED:** Reserved.

42.3.16 ELCR2—Offset 4D1h

Slave Edge/Level Control

Access Method

Type: I/O Register
(Size: 8 bits)

ELCR2: 4D1h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
ELC1		RESERVED	ELC2				RESERVED1

Bit Range	Default & Access	Description
7:6	X RW	**ELC1:** Edge Level Control (ECL[15:14]): In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0b RO	**RESERVED:** Reserved.
4:1	X RW	**ELC2:** Edge Level Control (ECL[12:9]: In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0b RO	**RESERVED (RESERVED1):** Reserved.

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