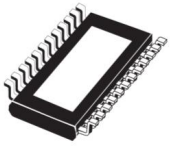
ALED1262ZT

Datasheet

Automotive-grade 12-channel LED driver with open detection, local dimming, bus driven and standalone operations



HTSSOP24 exposed pad

Features

- Designed for automotive applications
- 12 constant current output channels
- 19 V current generator rated voltage
- Output current: from 6 mA to 60 mA
- Current programmable by a single external resistor
- 7-bit PWM local brightness control
- Slow turn-on/off time, gradual output delay and dithered clock for EMI reduction
- Error detection for open LEDs
- Supply voltage: from 5.5 V to 38 V
- Thermal shutdown and overtemperature alert
- Standalone and bus-driven mode
- Custom configuration by OTP with Redundancy and ECC
- 400 kHz fast I²C interface with selectable extended Hamming encoding
- Wired-OR error flag connection

Applications

- Automotive rear lights
- Automotive interior lighting

Maturity status link
ALED1262ZT

Device summary	
Order code	ALED1262ZT
	ALED1262ZTTR
Package	HTSSOP24 exposed pad
Packing	62 parts per tube
	2500 parts per reel

Description

The ALED1262ZT is a monolithic 12 output LED driver designed for automotive exterior and interior lighting applications. The ALED1262ZT guarantees 19 V output driving capability allowing users to connect several LEDs in series. In the output stage, twelve regulated current sources provide from 6 mA to 60 mA constant current to drive LEDs. The current is programmed by a single external resistor. In the ALED1262ZT, LED open error detection is available.

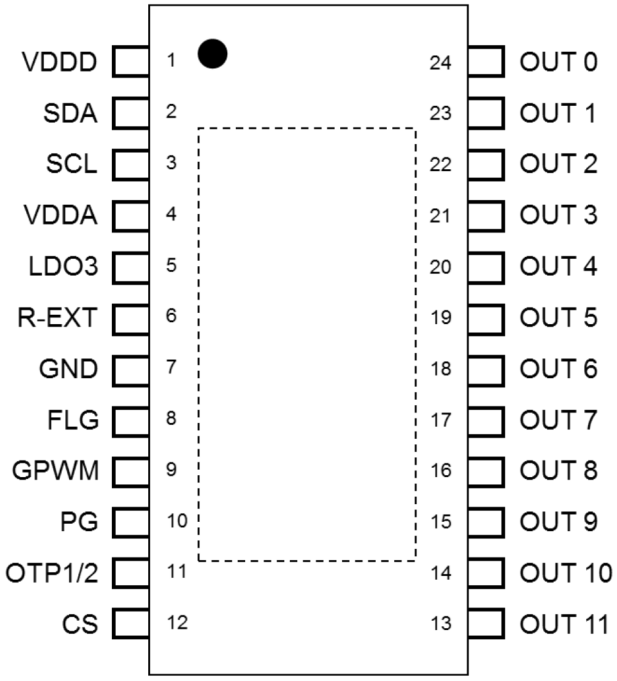
The brightness can be adjusted separately for each channel through a 7-bit grayscale control. A slow turn-on and turn-off time improves the system low noise generation performance. Moreover the gradual output delay reduces the inrush current. To further increase EMI performance, this device implements an internal clock dithering to have a spread spectrum noise reduction.

Thermal management is equipped with overtemperature data alert and the output thermal shutdown (170 °C). The I²C high clock frequency, up to 400 kHz, makes the device suitable for high data rate transmissions. The supply voltage range is between 5.5 V and 38 V avoiding any external pre-regulation or additional load dump protection on the power supply stage.

This device can operate in bus-driven mode (BDM) using I²C interface or in standalone mode (SAM) using internal custom configuration by OTP.

1 Pin description

Figure 1. **HTSSOP24 pinout**



AMG090320171202MT

Table 1. **Pin description**

HTSSOP24	Symbol	Name and function
1	VDDD	Digital supply terminal
2	SDA	I²C serial data input terminal
3	SCL	I²C clock input terminal
4	VDDA	Analog supply terminal and internal LDO input
5	LDO3	3.3 V internal LDO output
6	R-EXT	Terminal for external resistor for constant current programming
7	GND	Ground terminal
8	FLG	Fault flag: open-drain PMOS output for wired-OR connection
9	GPWM	Global PWM control. To be connected to LDO3 if it is not used
10	PG	Power Good pin. Connect to an external resistor divider to set a proper power supply voltage threshold for detection enabling
11	OTP1/2	Digital input for internal OTP register selection
12	CS	Chip-select and power supply (15 V) for OTP burning
13 to 24	OUT0 to OUT11	Output terminals (low-side current generators)
Exposed pad(1)	-	Additional device ground terminal to be connected to pin 7 (GND)

1. *The device exposed pad must be connected to GND, moreover it should be soldered directly to a PCB copper area to maximize thermal dissipation.*

2 Absolute maximum ratings

Stressing the device above the ratings listed on Table 2. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DDA}	Analog supply voltage	0 to 40	V
V_{DDD}	Digital supply voltage	0 to 7	
V_{PG}	Power Good pin	-0.3 to 20	
V_{GPWM}	Global PWM dimming		
$V_{OTP1/2}$	OTP register selection		
V_{OUT}	Output channel voltage		
CS	Chip select and OTP burning		
$V_{I/O}$	Digital I/O pin: SDA, SCL	-0.5 to V_{DDD}	
V_{LDO3}	LDO3 output voltage	0 to 4.6	
V_{FLG}	I/O flag: FLG	-0.3 to V_{DDD} (1)	
I_O	Output current	70	mA
ESD	Electrostatic discharge protection HBM (human body model)	±2.0	kV
	Electrostatic discharge protection CDM (charged device model)	±500	V
	Electrostatic discharge protection CDM (charged device model) for corner pins	±750	

1. *If V_{DDD} is not plugged AMR must be decreased to 3.3 V.*

3 Thermal characteristics

Table 3. Thermal characteristics

Symbol	Parameter		Value	Unit
T_{OPR}	Operative junction temperature range		-40 to +150	°C
T_{STG}	Storage ambient temperature range		-55 to +150	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	HTSSOP24(1)	37.5(2)	°C/W
$R_{thj\text{-}b}$	Thermal resistance junction-board		22.8 (2)	
$R_{thj\text{-}c}$	Thermal resistance junction-case		14.6 (2)	

1. *The exposed pad must be attached to a metal land electrically connected to ground. To get the thermal benefits it should be soldered directly to a PCB copper area.*
2. *Jedec test conditions on 2S2P board (4 layers).*

4 Electrical characteristics

Table 4. Electrical characteristics (V_{DDA} = 12 V, V_{DDD} = 5 V, Tj = -40 to 125 °C, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		5.5		38	V
V_{DDD}	Supply voltage		4.5		5.5	
V_{OUT}	Output voltage	OUT0 - OUT11			19	
V_{IH}	SDA, SCL digital thresholds	V_{DDD} plugged	0.7•V_{DDD}		V_{DDD}	
V_{IL}			-0.5		0.3•V_{DDD}	
V_{IH2}	FLG digital input threshold with V_{DDD} not active			1.70	1.90	
V_{IL2}			1.30	1.45		
V_{I2_Hys}	FLG hysteresis			0.25		
V_{IH3}	GPWM threshold	V_{DDA} plugged			2.00	
V_{IL3}			1.70			
V_{IH4}	OTP1/2 threshold				1.90	
V_{IL4}			1.30			
V_{IH5}	PG threshold			1.9	2.00	
V_{IL5}			1.70	1.8		
V_{I5_Hys}	PG hysteresis			0.1		
R_{CS}	CS pull-down			160		kΩ
I_{I_GPWM}	GPWM pin input current	V_{GPWM} = GND or 2 V	-1		+1	µA
$I_{I\_OTP1/2}$	OTP1/2 pin input current	$V_{OTP1/2}$ = GND or 2 V	-1		+1	
I_{I_PG}	PG pin input current	V_{PG} = GND or 2 V	-1		+1	
I_{OL_SDA}	SDA sink current	V_{DDD} = 4.5 V; V_{OL} = 0.4 V	3			mA
I_{OL_SCL}	SCL sink current	V_{DDD} = 4.5 V; V_{OL} = 0.4 V	3			
I_{Dleak}	SDA, SCL leakage current	V_I = GND or V_{DDD}	-10		+10	µA
I_{Oleak}	Output channel leakage current	V_{OUT} = 19 V, all outputs OFF			0.5	
I_{OH_FLG}	FLG source current	V_{DDD} plugged VOH = V_{DDD}-0.4V	3			mA
		V_{DDD} not plugged VOH = V_{LDO3}-0.4V				
V_{UVLO}	V_{DDA} UVLO threshold (falling)		1.7	1.85		V
V_{G_EN}	Global_EN V_{DDA} threshold (rising)	GPWM = LDO3		3.8	4.0	
	Global_EN V_{DDA} threshold (falling)		3.40	3.6		
H_{G_EN}	Global_EN hysteresis			0.2		
V_{ref}	R_{EXT} reference voltage			1.233		
V_{LDO}	LDO3 output voltage	External maximum load current: I_{load} = 200 µA	3.231	3.328	3.428	
I_{LDO}	LDO short-circuit output current	V_{DDA} = 5.5 V		110		mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Δ_{IOL1}	Output current precision channel to channel (all outputs ON) (1)	V_{OUT} = 0.65 V; R_{EXT} = 49.9 kΩ; Io ≈ 6 mA; T_j ≤ 90 °C; (outage)			±15	%
Δ_{IOL2}		V_{OUT} = 1.05 V; R_{EXT} = 24.9 kΩ; I_O ≈ 12 mA; (outage)			±10	
Δ_{IOL3}		V_{OUT} = 1.35 V; R_{EXT} = 4.99 kΩ; I_O ≈ 60 mA (outage)			±3	
Δ_{IOL2a}	Output current precision device to device (all outputs ON) (1)	V_{OUT} = 1.35 V; R_{EXT} = 4.99 KΩ; I_O ≈ 60 mA; (outage)			±6	
$\%/dV_{OUT}$	Output current vs output voltage regulation	V_{OUT} from 1.35 V to 3.35 V; R_{EXT} = 4.99 kΩ; I_O ≈ 60 mA		0.1		|%/V|
R_{EXT}	External current set-up resistance		4.99		49.9	kΩ
I_{DDD}	V_{DDD} supply current no dimming	R_{EXT} = 4.99 kΩ; No I²C data transfer OUT0 to 11 = ON (outage)		0.7	1.0	mA
$I_{DDA(OFF)}$	V_{DDA} supply current (OFF) GPWM = GND	R_{EXT} = 4.99 kΩ; OUT0 to 11 = OFF		0.3	0.6	
$I_{DDA(ON1)}$	V_{DDA} supply current (ON) no dimming	R_{EXT} = 24.9 kΩ; I_O ≈ 12 mA; OUT0 to 11 = ON (outage)		2	2.5	
$I_{DDA(ON2)}$	V_{DDA} supply current (ON) no dimming	R_{EXT} = 4.99 kΩ; I_O ≈ 60 mA OUT0 to 11 = ON (outage)		4	5.5	
$I_{DDA(REC)}$	VDDA supply current	R_{EXT} = 4.99 kΩ; SAM recovery condition			1.2	
T_{flg}	Thermal flag			140		°C
T_{flg-hy}	Thermal flag hysteresis			10		
T_{sd}	Thermal shutdown			170		
T_{sd-hy}	Thermal shutdown hysteresis			15		

1. *Tested with just one output loaded.*
2. *($(I_{On} – I_{Oavg1-12})/ I_{Oavg1-12}$) x 100*
3. $$\Delta\,(\%/V) = \frac{(I_{On}@V_{OUTn} = 3.35V) - (I_{On}@V_{OUTn} = 1.35V)}{(I_{On}@V_{OUTn} = 1.35V)} \cdot \frac{100}{3.35 - 1.35}$$

4.1 Switching characteristics

Table 5. Switching characteristics (V_{DDA} = 12 V, V_{DDD} = 5 V, Tj = 25 °C, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	I²C clock frequency		100		400	kHz
f_{PWM}	GPWM frequency				500	Hz
t_{PWM}	Output minimum t_{on} by GPWM	$GPWM_{HIGH}$ = 20 µs	5			µs
f_{PWM_local}	Local dimming frequency (1)		200	220	240	Hz
t_{PWM_local}	Local dimming minimum t_{on}			5		µs
$t_{(SP)}$	Pulse width of spikes that must be suppressed by the input filter				50	ns
$t_{(BUF)}$	Bus free time between a STOP and START condition		1.3			µs
$t_{pd(ACK)}$	SCL low to data out valid (acknowledge)				0.9	
t_{LOW}	SCL low time		1.3			
t_{HIGH}	SCL high time		0.6			
$t_{su(DAT)}$	SDA / SCL set-up time		100			ns
$t_{su(STA)}$	Set-up time for START condition		600			
$t_{su(STO)}$	Set-up time for STOP condition		600			
$t_{h(DAT)}$	Data input hold time				900	
$t_{h(STA)}$	START condition hold time		600			
t_r	Rise time both of SDA and SCL signals		20		300	
t_f	Fall time both of SDA and SCL signals		20		300	
t_{on}	Output current turn-on time	R_{EXT} = 4.99 kΩ I_O = 60 mA		1.7		µs
t_{off}	Output current turn-off time	V_{DROP} = 1.35 V RL = 50 Ω CL= 10 pF		1.4		
$t_{n\text{-}reg}$	Delay time from global_EN to output current regulation (V_{LED} is enough for regulation)	R_{EXT} = 4.99 kΩ I_O = 60 mA V_{DROP} = 1.35 V RL = 50 Ω CL = 10 pF			60	µs
$t_{n\text{-}err}$	Delay time from PG to output error detection				70	

1. *Using prescaler bit (Faulty_ch_1 register bit[7]) local dimming frequency value can be reduced by half (typ. = 110 Hz)*

Figure 2. I²C timing definition

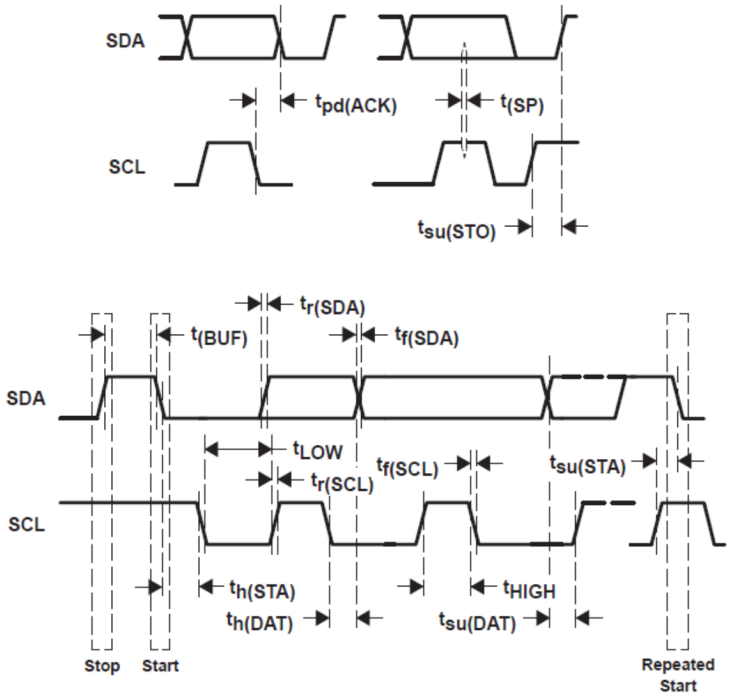
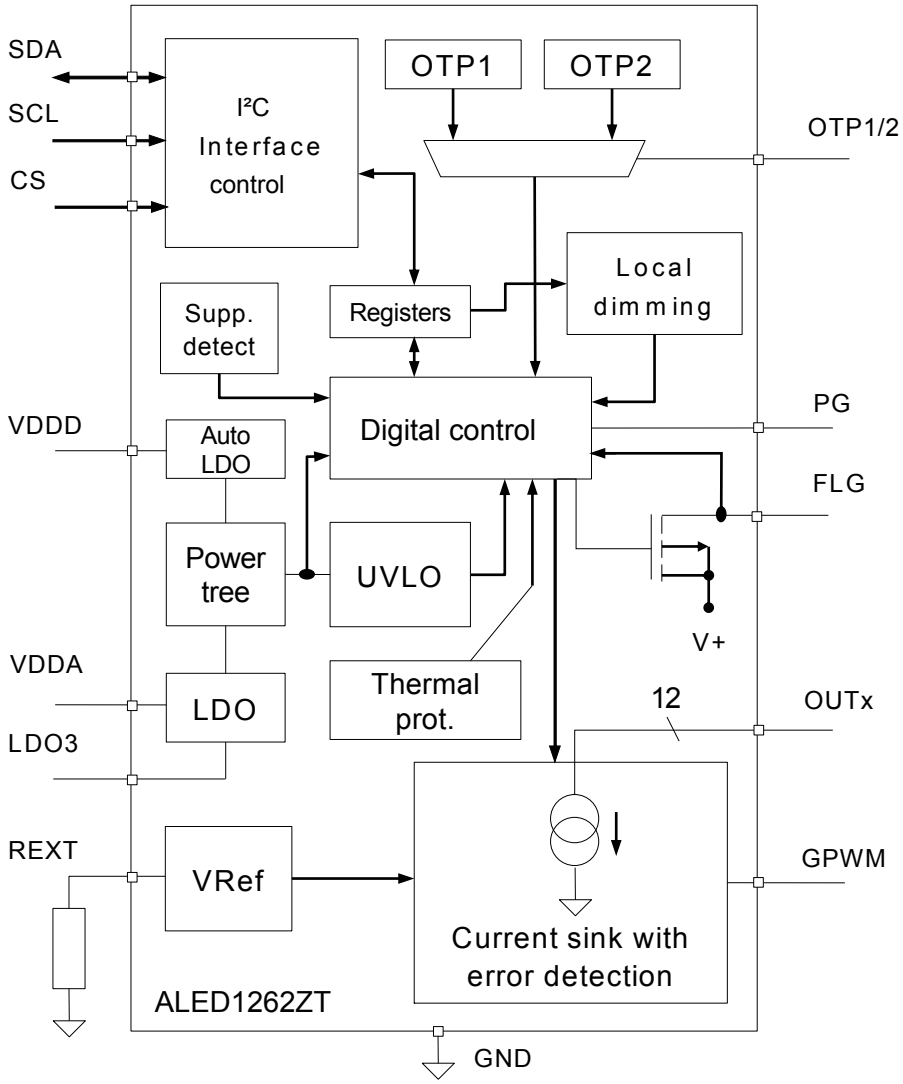


Figure 3. **Simplified internal block diagram**



5 Device pin functions

A detailed description about each pin function as follows:

SDA – I²C is the bidirectional data line, it must be pulled up with an external resistor connected to MCU power supply.

SCL – clock line, coming from MCU I²C bus, must be pulled up with an external resistor connected to MCU power supply.

CS – chip-select pin used exclusively to address each device during one time register programming (OTP). This procedure is carried out at the end of customer production line to set the device default configuration. CS pin has an internal pull-down resistor of about 160 kΩ. This pin is also used to supply 15 V during factory programming to set internal OTP registers.

Note: The CS pin cannot be connected to GND, neither directly nor through passive components. The only allowed polarization is floating or positive voltage (up to 15 V).

V_{DDD} – digital power supply coming from MCU section together with I²C bus. When V_{DDD} is below a threshold of about 2.9 V (typ. falling) or 3.0 V (typ. rising) the device goes automatically to SAM. Besides, providing the digital power supply V_{DDD} only (V_{DDA} not connected), the device I²C bus is active and internal registers can be programmed, the only restriction is related to V_{DDA} impedance to GND that must be higher than 4.7 kΩ. In case of a lower impedance, the device digital interface starts on the first V_{DDA} voltage rising edge. The allowed slew rate for this pin is below 0.17 V/µs (0 to 5 V; 30 µs ≤ t_{rise}).

Note: Fast V_{DDD} edges can cause internal regulator overvoltage spikes that may provoke electrical stresses in the device.

V_{DDA} – analog power supply coming from car body system. This is the main supply voltage for the driver and it can be dimmed to change LED brightness (100 or 200 Hz at 10% as minimum duty cycle, V_{DDA} = 0 to 12 V). Allowed slew rates for this pin are the following: from 0.4 to 1.2 V/µs (0 to 12 V; 10 µs ≤ $t_{rise/fall}$ ≤ 30 µs) in normal operation, from 6.8 to 8.4 V/ms for load dump conditions.

Note: If the I²C is programmed to only provide the digital power supply V_{DDD} (V_{DDA} not connected), a subsequent V_{DDA} plug or unplug with edges faster than those allowed ($t_{rise/fall}$ < 10 µs) may induce the internal register reset.

LDO3 – internal regulator output pin to be connected to an external capacitor (minimum value 1 µF). The output voltage is about 3.3 V ±3% and it is used as an external reference voltage and the device internal supply. The capacitor connected on this pin is also used as “tank capacitor” to maintain internal volatile register data during V_{DDA} pulsed dimming function (if required).

R_{EXT} – this resistor is used to program the regulated output current. The relationship between R_{EXT} value and the output current is given by the following equation:

$$I_{Ox} = \frac{V_{BG}}{R_{EXT}} \cdot K$$

The current gain factor "K" is about 240. The V_{BG} voltage is normally at 1.233 V used to get the reference current trough R-EXT pin; this current is mirrored by a precise circuit to generate the reference for the driver stage. On R-EXT pin, any filter capacitor can be connected.

GND – ground pin, it must be connected to a package exposed pad. Exposed pad should be soldered directly to the PCB to see the thermal benefits (see the device thermal management section).

GPWM – a variable duty cycle square wave on this pin allows all channels brightness to be fixed simultaneously (PWM global dimming). If this pin is not used, it must be connected to LDO3. GPWM control requires a square wave with a HIGH level longer than 20 µs caused by a 15 µs delay needed to power on all internal blocks before the channel activation. With 20 µs HIGH level, the real output activation is around 5 µs. The maximum allowed slew-rate on this pin is 1.9 V/µs.

OUTx – the ALED1262ZT has 12 current regulated low-side outputs. The output stage is a sinker, which is able to stand till 19 V, this is to use more than one LED series connected. The internal current generator turn-on and turn-off time has been slowed down to decrease as much as possible EMI noise.

FLG – this is the fault flag I/O pin used in wired-OR among those devices sharing the same application. In wired-OR connection, all FLG pins are connected together to a single pull-down resistor, this signal can also be read by an MCU to detect any fault condition. If the device receives an external error status, it reacts according to the internal configuration (see Section 13.1 BDM_conf_1 / Enable_CH_1 register, Section 13.2 BDM_conf_2 /

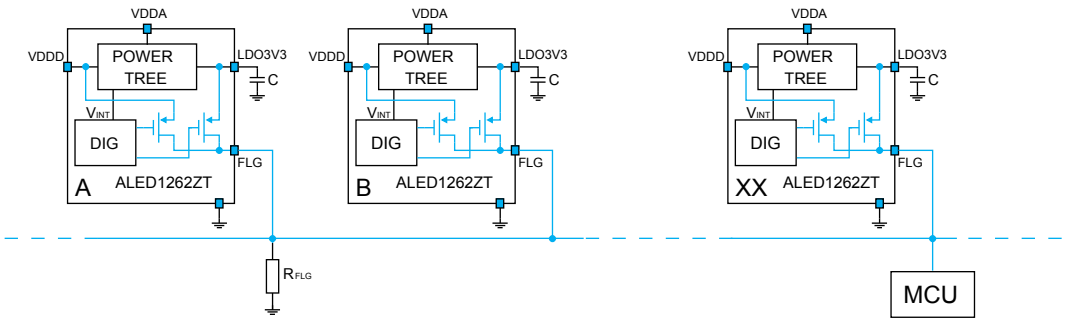
Enable_CH_2 register and Section 13.11 OTP/BA_n_SAM_setting register). This pin can be configured by setting internal registers and may combine error detection results and the overtemperature protection. The devices sharing the same FLG line must have the same supply domain. Different supply domains on the same FLG bus need to be managed externally according to the used voltage level (i.e., level shifter).

As soon as one device forces current on the external pull-down resistor (R_{FLG}) through the integrated high-sides, the digital information is generated. The internal high-side pull-up is connected to two different power lines to get the correct voltage level according to the external configuration:

- **V_{DDD} is plugged**: an internal high-side transistor is connected to the V_{DDD} (5 V). In this case the high level on FLG pin/bus is forced to V_{DDD} and it is compliant to fault information coming directly from the MCU as well.
- **V_{DDD} is not plugged**: a high-side transistor is connected to the internal regulated voltage 3V3 (LDO3). In this case there is not any external interrupt coming from MCU to be managed (5 V V_{DDD} is not available). The voltage level is among chips connected to the same power domain.

The power line selection for the FLG analog MUX is a matter of V_{DDD} comparator used to detect the V_{DDD} plug-in.

Figure 4. FLG pin connection



In case of dimming functions and FLG pin at high logic level due to one output in open condition (and/or thermal shutdown and/or R_{EXT} short), FLG behavior is different according to running dimming mode:

- Faulty channel, dimming by GPWM pin: FLG blinks according to GPWM external square wave and error detection conditions.
- Faulty channel, dimming by PWM register (BDM): FLG is constantly high according to the error detection conditions.

PG – this pin is the LED driver Power Good, it must be connected by a proper resistor divider to the main voltage coming from car body system (V_{DDA}) or to LED power supply. Starting from the internal threshold overcoming (above 1.95 V), the ALED1262ZT has a valid detection available in less than 70 µs. The maximum allowed slew-rate on this pin is 1.9 V/µs.

OTP1/2 – in standalone mode, it is possible to select two possible output configurations. Each configuration is stored in non-volatile cells (shadowed by SAM_conf_* registers). This pin can be also connected to a switched voltage coming from car body system (V_{DDA}3) by a resistor divider. When OTP1/2 is at logic level LOW, output configurations are related to SAM_conf_1 register. Conversely, when OTP1/2 is at logic level HIGH, output configurations are related to SAM_conf_2 register (see register description for more details). The maximum allowed slew-rate on this pin is 1.9 V/µs.

6 Driver dropout voltage

In order to correctly regulate the channel current, a minimum output voltage (V_{DROP}) across each current generator must be guaranteed.

Figure 5. Channel dropout voltage vs output current (Tj = 25 °C), Table 6. Minimum dropout voltage for certain current values (Tj = 25 °C; worst case simulated at target minus 3%) and Table 7. Minimum dropout voltage at 60 mA (worst case simulated at target minus 3%) show the minimum slightly less than the target value (output MOS transistor in triode region); these measurements have been recorded with just one output ON. When more than one output is active, the drop voltage increases. At 60 mA per channel, all channels ON, output voltage must be increased by about 110 mV (worst case at Tj = 125 °C). If the V_{DROP} is lower than the minimum recommended, the regulation of a current is lower than the expected one. However an excess of V_{DROP} increases the power dissipation.

Figure 5. Channel dropout voltage vs output current (Tj = 25 °C)

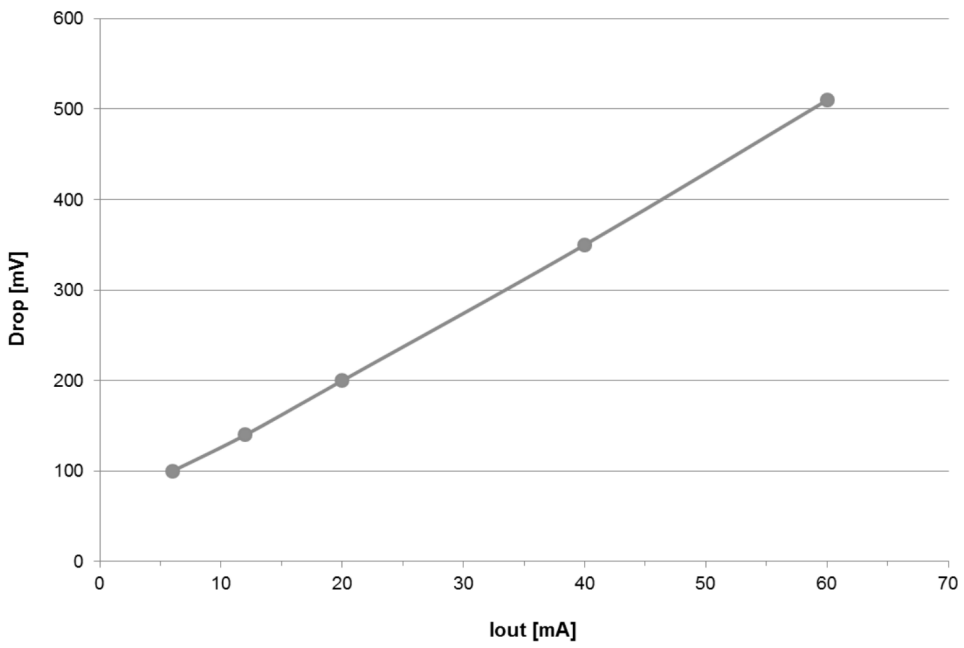


Table 6. Minimum dropout voltage for certain current values (Tj = 25 °C; worst case simulated at target minus 3%)

Target output current [mA]	V_{DROP} [mV]
6	100
12	140
20	200
40	350
60	510

Table 7. Minimum dropout voltage at 60 mA (worst case simulated at target minus 3%)

Tj [°C]	V_{DROP} [mV]
125	630
25	510
-40	440

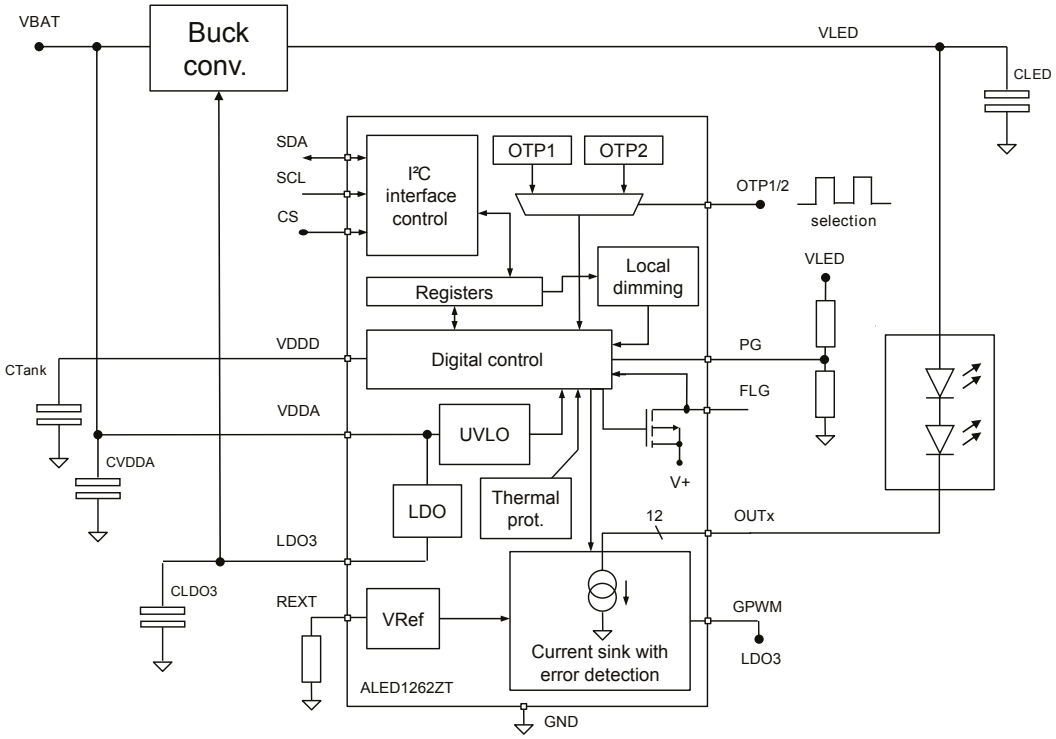
Table 8. Typical output current vs R_{EXT} value

Iout target value (mA)	R_{EXT} calculated value (Ω)	R_{EXT} - E96 1% nearest commercial value (Ω)
6	49360	49900
12	24680	24900
15	19744	19600
20	14808	14700
25	11846	11800
30	9872	9760
35	8462	8450
40	7404	7320
45	6581	6650
50	5923	5900
55	5385	5360
60	4936	4990

7 Device functional description

The ALED1262ZT has been designed to be very flexible so to meet application needs. In a very basic connection, the ALED1262ZT is supplied only by V_{DDA} pin (with a continuous voltage), and a resistor connected between R-EXT pin and GND (placed as near as possible to the device) programs the current sunk from outputs, GPWM is not used (to LDO3) and output channels connected to external LED cathodes.

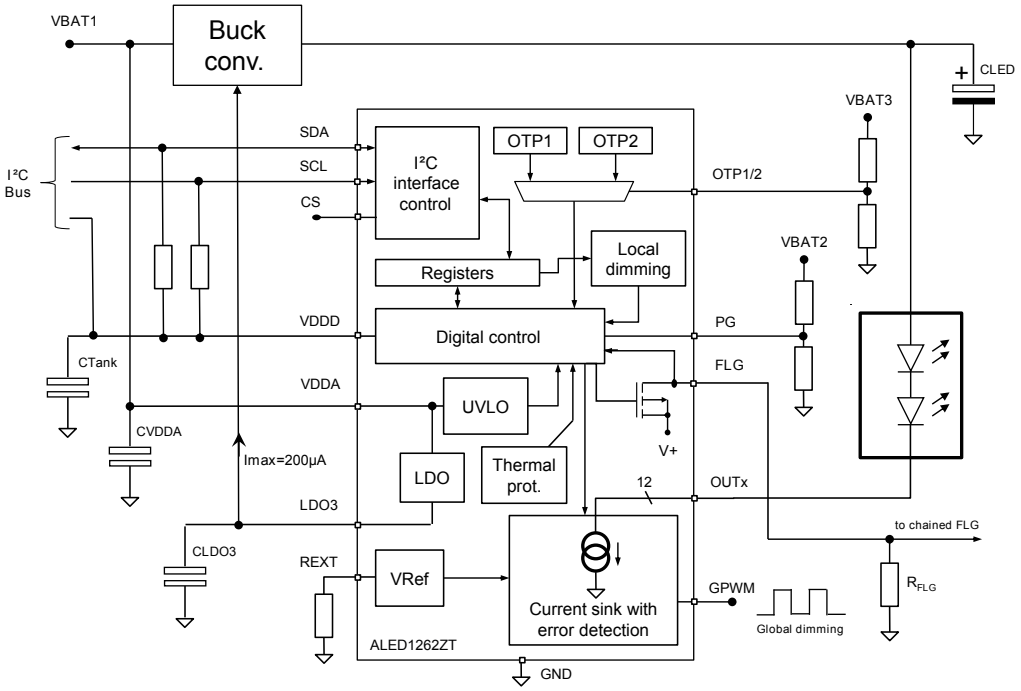
Figure 6. ALED1262ZT typical connection scheme



Furthermore, the Power Good pin (PG) can be connected to an external resistor divider. This divider supplied by V_{LED} provides the internal trigger signal when V_{LED} has a value enough for the device current regulation and consistent error detection. Fault flag pin (FLG) can be floating or connected to a pull-down resistor or in a wired-OR configuration to all FLG pins of additional devices sharing the same application. LDO3 is the internal regulator output supplied by V_{LED}, the output voltage is 3.3 V and it is used as the device internal block supply and, if necessary, as external reference voltage.

By changing the external circuit, more and more functions of the device can be used. The ALED1262ZT in a full feature configuration is connected using the I²C interface and OTP1/2 output configurations as fail-safe recovery in case of bus accidental disconnection (see the following diagram).

Figure 7. The ALED1262ZT full connection



Components typical selection	
CV_{DDD}	1µF
CV_{DDA}	1µF
C_{Tank}	1µF(*)
C_{LED}	2.2µF
R_{FLG}	2.2K

(*) Any de-rating included

On all applications where LEDs are dimmed using the main power line (VBAT1 on schematic) it's mandatory to rectify the V_{DDA} voltage to supply the device. In this condition GPWM pin must be connected, by a resistor divider, to the power line (on VBAT1 before rectifier diode) to allow channels to switch off during main power supply dimming falling edge. For right operations, resistor dividers must be calculated to have GPWM threshold lower than Power Good (PG) threshold. The placement of external capacitors and minimum capacitance values are always mandatory, in this particular case they are essential for the device steady setup (see "component typical selection" table).

As mentioned, the ALED1262ZT has been designed to work in two possible application architectures: standalone mode (SAM) and bus-driven mode (BDM). Some details about these two operation modes are the following:

SAM - In standalone mode configuration, the device is not connected to an MCU or a controller board so I²C bus leaves floating (SDA, SCL pins). In this condition, V_{DDD} is not supplied and an internal comparator senses this pin to set properly the device and to release the I²C bus.

In this mode, the device refers to four internal registers mimic the content of non-volatile memory: SAM_conf_1, SAM_conf_2, SAM_conf_1_2 and BA_n_SAM_setting. In the rest of the document we can refer to these registers as non-volatile registers, just for sake of simplicity. SAM_conf_x represent the output ON/OFF status in two possible configurations that can be selected on the application by OTP1/2 pin. Error detection system is adequate to the activated outputs.

According to BA_n_SAM_setting register, the device runs continuously an error detection indicating, if required, the error status to all other devices connected on the same board by fault flag chain. All these four registers can be preset during - one time programming phase - at the end of customer production line using the chip-select pin (CS – see OTP programming section).

BDM - In bus-driven mode configuration, the device is connected to an MCU or to a controller board, so I²C bus is active. V_{DDD} is also supplied in this condition and an internal comparator senses this voltage to switch

automatically to SAM in case of bus unintentional disconnection. In this mode, we refer to one non-volatile register and six volatile registers:

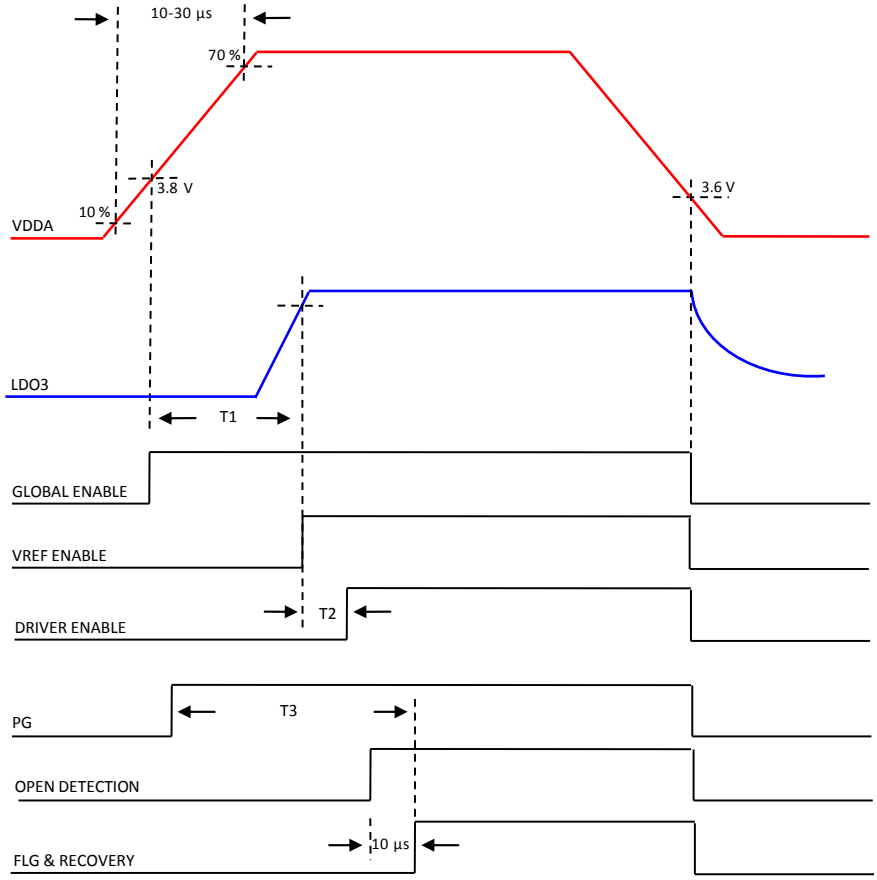
- Non-volatile – BA_n_SAM_setting register, it is programmed during one time programming phase, using chip-select pin (CS – see OTP programming section).
- Volatile – BDM_conf 1 and 2, BDM_status, Faulty_ch 1 and 2, PWM_gain registers.

BA_n_SAM_setting register sets the device I²C address on 31 possible selections (all zeros is valid only for fresh devices) and the communication protection mode; BDM_conf 1 and 2 set the output ON/OFF status; BDM_conf 1 also contains information about the error detection device behavior, diagnostic function and local dimming activation; BDM_status contains information about the diagnostic results, thermal protection and general driver status; Faulty_ch 1 and 2 contain indications about branches in which a fault is detected; PWM_gain represents the dimming value for each of 12 outputs (for more details see register description paragraph). Through bit BDM_Flag of the BDM_conf_1 register, we can force the device from SAM to BDM according to the following table:

Table 9. Operative status

V_{DDA}	V_{DDD}	BDM_FLAG	STATUS	Notes
OFF	OFF	X	OFF	The device is not supplied
OFF	ON	0	SAM	Analog part is OFF but the current regulation can be re-established quickly as soon as V_{DDA} is plugged and output configuration is related to SAM OTP registers, I²C registers are accessible
OFF	ON	1	BDM	Analog part is OFF but the current regulation can be re-established quickly as soon as V_{DDA} is plugged and output configuration is related to BDM registers, I²C registers are accessible
ON	OFF	0	SAM	Analog part is active and the output configuration is related to SAM_conf_* registers (OTP), I²C registers are supplied, I²C module is OFF
ON	OFF	1	SAM	BDM_FLAG is reset and the device comes back on the previous configuration (BDM_FLAG=0)
ON	ON	0	SAM	Analog part is active and output configuration is related to SAM_conf_* registers (OTP), I²C registers are supplied, I²C module is ON
ON	ON	1	BDM	Analog part is active and output configuration is related to BDM_conf_* registers (volatile), I²C registers are supplied, I²C module is ON

Figure 8. Power supply internal signal behavior



T1+T2 < 60 µs
T3 < 70 µs

AMG090320171208MT

8 Error detection

If Power Good threshold is asserted (PG pin voltage above 1.95 V), the ALED1262ZT runs continuously the output open detection. If the current flowing through the active channels is less than the half of the programmed one, the device reports an error that is managed according to BDM_conf register (see register description paragraph). Please note that all error flags: Rext_fault, Ext_fault, Led_fault, have a time delay mask (debounce), it means that a fault with duration lower than debounce time does not generate any type of interrupt. Time delay mask is about 10 µs on Rext_fault and LED_fault and 20 µs on Ext_fault signal. At the same time, if LED power-on time is less than 15 µs (delay mask + detection delay), no output detection can be available.

For the same reason, no output detection is available in case of dimmed channels with LED t_{on}-time less than 15 µs (below step 20 on non-linear dimming table). If recovery condition has been set on BDM_conf register and LED output channels are dimmed, in case of open condition detected, faulty channel duty cycle is brought to 100% till faulty retrieval. During recovery, the output current is typically regulated at 30 mA (value just as reference because channel is open condition). As soon as open channel is reconnected, the device sinks the recovery current for 10 µs, subsequently all active channels are switched OFF to have, 15 µs later, a new channel power-ON in normal regulation.

Furthermore, R-EXT pin is indirectly continuously monitored and any short-to-ground condition can be detected stopping output activities. In this case the parameter is indirectly the channel output current, above 65 to 95 mA (it depends on number of active channels and junction temperature) an internal comparator warns the R_{EXT} failure. In case of R_{EXT} short the outputs are in power-off. After 620 µs (typ.) channels are reactivated for 10 µs (typ.) to check again faulty condition. In other words, a physical short condition on R_{EXT} generates periodic pulsing on FLG pin at 630 µs period.

All error conditions are reported on BDM_status and Faulty_ch_1/2 registers (see register description paragraph) and on fault flag pin. A fault condition summarizing table is shown below:

Table 10. Type of fault and device behavior

Type of fault	FLG		Detection	
	Driven	Undriven	Outage	Recovery(1)
Open LED	Active	Not active	No action	All good channels OFF The device in low power mode Open channel in recovery
Fault flag input line	-		No action	All channels disabled
R_{EXT} short-to-GND	Active		Turn off all LED branches	
Thermal warning	No action		Communicated by bus message only	
Thermal shutdown	Active		Communicated by bus message + all channels OFF	
Message error on bus	No action		Communicated by bus message if Hamming ON only	

1. *If PG is not asserted, FLG and/or load diagnosis are ignored.*

9 Gradual output delay

An additional feature implemented on the ALED1262ZT is the gradual output delay. It consists of turning on gradually the current generators avoiding all channels to be turned on at the same time. In other words, enabling the device channels, the outputs can be turned ON with a staggered delay. The delay among each output is summarized on the following table, it is expressed in number of clock periods (typical internal clock frequency average value is 3.3 MHz ≡ 303 ns period):

Table 11. Gradual output delay

Channels	Added delay (number of CLK period)
ch0/ch1	1
ch1/ch2	1
ch2/ch3	1
ch3/ch4	1
ch4/ch5	2
ch5/ch6	7
ch6/ch7	1
ch7/ch8	1
ch8/ch9	1
ch9/ch10	1
ch10/ch11	1

Between first and last channel the cumulative delays are 18 internal clock periods. This feature also prevents large inrush current and reduces the bypass capacitor value on LED voltage rail. This function is activated in local dimming condition (BDM) only.

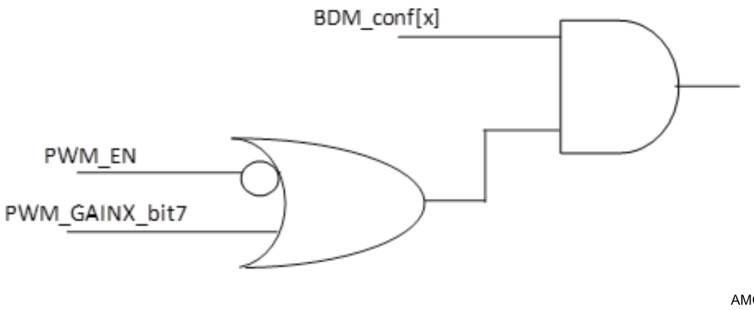
10 Thermal warning and protection

The device has a thermal control logic providing a digital flag status (warning) when the internal temperature exceeds 140 °C. If thermal alert is asserted, error data is uploaded into BDM_status register and this error notification is ready to stream through I²C bus. If temperature increases over 170 °C a thermal shutdown protects the device (all 12 channels OFF) and external fault flag (FLG) drives high.

11 Device local dimming function

The brightness of each channel can be adjusted through a 7-bit PWM grayscale brightness control according to local dimming register PWM_gain_x.

Figure 9. Device local dimming function logic

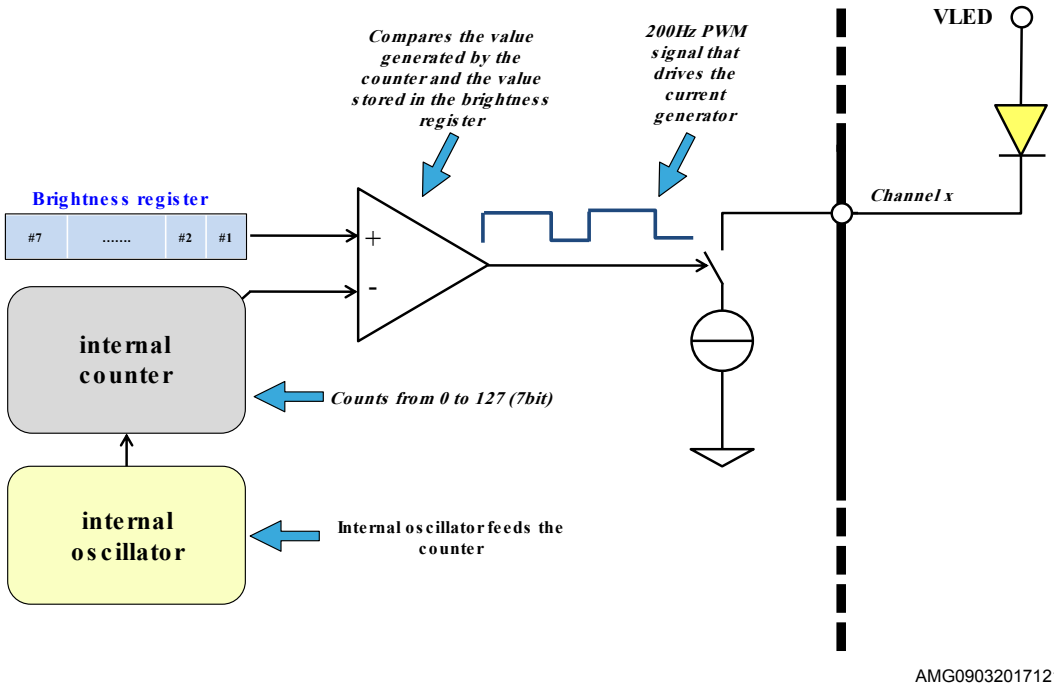


Brightness data are loaded through I²C bus, PWM signal for each channel is generated by comparing the content of the brightness register to a 7-bit counter. The counter's clock source is provided by 3.3 MHz internal oscillator. Brightness register default configuration is all "0" (0x00) this means minimum LED brightness.

Note: PWM_gain_x registers are made visible internally to the PWM generator, after an I²C transaction, when the internal 7-bit counter reaches the value 7Fh. Internal 7-bit counter stops when exiting PWM local dimming configuration (PWM_En and/or BDM_Flag set to '0'). When re-entering in PWM local dimming configuration 7-bit counter restarts from previous stopped value (unless HW reset), so first period of PWM waveform could be shorter.

The schematic below summarizes this functionality.

Figure 10. Channel dimming feature



The ALED1262ZT implements 128 non-linear dimming steps to adequate LED brightness change to human eye light perception, giving in this way the impression of brightness linear variation. The exponential law used to calculate the dimming steps is the following:

$$ton_i = PWM\_period \cdot \alpha^{(N-i)}$$

Where ton_i is the LED ON-time during step number "i", PWM_period = 5 ms or 10 ms (max. values), this means that minimum dimming frequency can be 200 Hz or 100 Hz according to Faulty_ch_1 register bit[7] (see register description), N = 127 (7-bit resolution), $0 \leq i \leq 127$, $\alpha \approx 0.9471$.

12 Local dimming non-linear step table

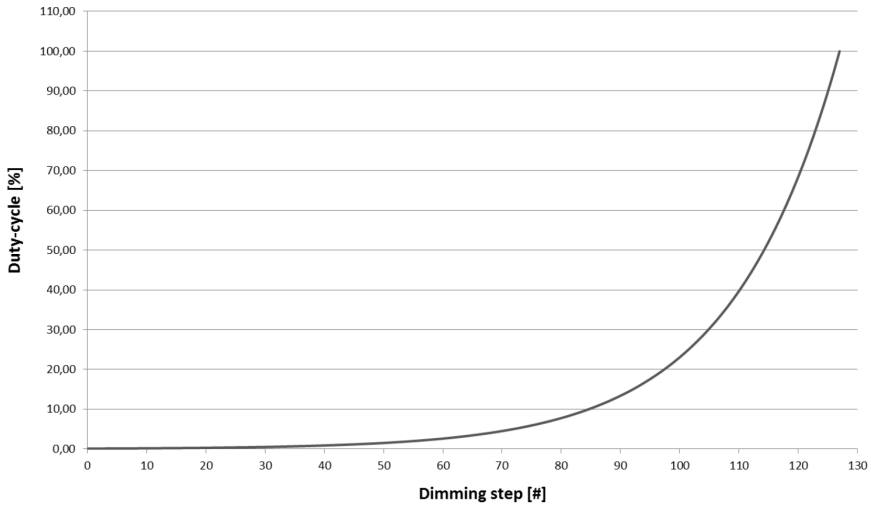
The following table is related to the ALED1262ZT 7-bit local dimming non-linear steps. LED brightness can be changed in 128 paces with duty cycle between 0.1% and 100% (t_{ON} and duty cycle real values can be slightly different respect to tabulated numbers. Values are referred to minimum high range frequency: f_{PWM} = 200 Hz).

Table 12. Local dimming step

Step number	t_{ON} (µs)	Duty cycle (%)	Step number	t_{ON} (µs)	Duty cycle (%)	Step number	t_{ON} (µs)	Duty cycle (%)
0	5.00	0.10	**43**	51.95	1.04	**86**	538.79	10.78
1	5.33	0.11	**44**	54.95	1.10	**87**	568.76	11.38
2	5.67	0.11	**45**	57.94	1.16	**88**	600.40	12.01
3	6.00	0.12	**46**	61.27	1.23	**89**	634.03	12.68
4	6.33	0.13	**47**	64.60	1.29	**90**	669.33	13.39
5	6.67	0.13	**48**	68.27	1.37	**91**	706.63	14.13
6	7.00	0.14	**49**	71.93	1.44	**92**	745.92	14.92
7	7.33	0.15	**50**	75.92	1.52	**93**	787.55	15.75
8	7.67	0.15	**51**	80.25	1.61	**94**	831.83	16.64
9	8.33	0.17	**52**	84.92	1.70	**95**	878.45	17.57
10	8.66	0.17	**53**	89.58	1.79	**96**	927.41	18.55
11	8.99	0.18	**54**	94.57	1.89	**97**	979.02	19.58
12	9.66	0.19	**55**	99.90	2.00	**98**	1033.63	20.67
13	10.32	0.21	**56**	105.23	2.10	**99**	1091.57	21.83
14	10.66	0.21	**57**	111.22	2.22	**100**	1152.51	23.05
15	11.32	0.23	**58**	117.55	2.35	**101**	1217.12	24.34
16	11.99	0.24	**59**	123.88	2.48	**102**	1285.05	25.70
17	12.65	0.25	**60**	130.87	2.62	**103**	1356.64	27.13
18	13.32	0.27	**61**	138.20	2.76	**104**	1432.23	28.64
19	13.99	0.28	**62**	145.85	2.92	**105**	1512.49	30.25
20	14.99	0.30	**63**	154.18	3.08	**106**	1597.07	31.94
21	15.65	0.31	**64**	162.84	3.26	**107**	1685.98	33.72
22	16.65	0.33	**65**	172.16	3.44	**108**	1780.22	35.60
23	17.65	0.35	**66**	181.82	3.64	**109**	1879.79	37.60
24	18.65	0.37	**67**	191.81	3.84	**110**	1984.68	39.69
25	19.65	0.39	**68**	202.46	4.05	**111**	2095.57	41.91
26	20.65	0.41	**69**	213.79	4.28	**112**	2212.79	44.26
27	21.65	0.43	**70**	225.77	4.52	**113**	2336.33	46.73
28	22.98	0.46	**71**	238.43	4.77	**114**	2466.53	49.33
29	24.31	0.49	**72**	251.75	5.03	**115**	2604.39	52.09
30	25.64	0.51	**73**	265.73	5.31	**116**	2749.91	55.00
31	26.97	0.54	**74**	280.72	5.61	**117**	2903.76	58.08
32	28.64	0.57	**75**	296.37	5.93	**118**	3065.60	61.31

Step number	t_{ON} (µs)	Duty cycle (%)	Step number	t_{ON} (µs)	Duty cycle (%)	Step number	t_{ON} (µs)	Duty cycle (%)
33	30.30	0.61	**76**	312.69	6.25	**119**	3237.09	64.74
34	31.97	0.64	**77**	330.34	6.61	**120**	3417.58	68.35
35	33.63	0.67	**78**	348.65	6.97	**121**	3608.72	72.17
36	35.63	0.71	**79**	367.97	7.36	**122**	3810.19	76.20
37	37.63	0.75	**80**	388.61	7.77	**123**	4022.97	80.46
38	39.63	0.79	**81**	410.26	8.21	**124**	4247.75	84.95
39	41.96	0.84	**82**	433.23	8.66	**125**	4484.84	89.70
40	44.29	0.89	**83**	457.21	9.14	**126**	4735.59	94.71
41	46.62	0.93	**84**	482.85	9.66	**127**	5000.00	100.00
42	49.28	0.99	**85**	510.16	10.20			

Figure 11. Local dimming duty cycle vs dimming steps



13 Register descriptions

Table 13. Embedded register list and direct address table

#	Register name (one byte content)	R/W	Functions	Reg. direct address (1)
BDM registers				
1	BDM_conf_1 (bus-driven mode config. 1)	R/W	BDM/SAM selection, FLG and detection behavior, PWM ON or OFF, channels 11 to 8 ON or OFF	0x00
2	BDM_conf_2 (bus-driven mode config. 2)	R/W	Channels 7 to 0 ON or OFF	0x01
3	BDM_status (bus-driven mode status)	R	Rext_fault, msg_err, global_en, diag_en, T_alert, T_fail, ext_fault, LED_fault	0x02
4	Faulty_ch_1 (faulty channels 1+PWM frequency)	R/W	PWM 110 or 220 Hz, faulty_ch 11 to 8	0x03
5	Faulty_ch_2 (faulty channels 2)	R	Faulty_ch 7 to 0	0x04
6 to 17	PWM_gain_x (channel PWM gain)	R/W	PWM chx ON or OFF, PWM chx gain (first byte is related to ch0)	0x05 to 0x10
18	LDD (LED driver device)	R	Versioning: driver ID and revision ID	-
SAM registers (OTP)				
1	SAM_conf_1_2 (standalone mode out config. 1/2)	R/W	OTP1/2=L channels 11 to 8 ON or OFF OTP1/2=H channels 11 to 8 ON or OFF	0x20
2	SAM_conf_2 (standalone mode out config. 2)	R/W	OTP1/2=L channels 7 to 0 ON or OFF	0x21
3	SAM_conf_2 (standalone mode out config. 2)	R/W	OTP1/2=H channels 7 to 0 ON or OFF	0x22
4	BA_n_SAM_setting (device bus ADDR and settings)	R/W	Hamming ON or OFF, FLG and detection behavior, I²C bus address	0x23

1. *Direct address can be used with 0x81 command (see the command table). Please note that register address must be maintained inside the allowed intervals: 0x00 ≤ direct ADDR ≤ 0x10 (BDM) and 0x20 ≤ direct ADDR ≤ 0x23 (SAM). Outside these intervals, all other addresses are forbidden.*
   - *Accessing read only registers (BDM_status and Faulty_ch_2) in write mode with direct address command could affect the register content.*
   - *Safer way to address registers is using the specific commands reported in Table 29. Command representation and description, they are fully controlled by internal state machine.*

13.1 BDM_conf_1 / Enable_CH_1 register

Reg. name: BDM_conf_1 / Enable_CH_1
Reg. default value: 0x00
Reg. direct address: 0x00
Command involved: 0x00/0x02
Reg. access mode: R/W

	7	6	5	4	3	2	1	0
W	BDM_Flag	D[1:0]		PWM_En	BDM_conf[11:8]			
R					Enable_CH[11:8]			

Table 14. BDM_conf_1 field descriptions

Field	Description		
BDM_Flag	Used to push the LED driver to BDM mode when VDDD is high(1) 0: SAM 1: BDM		
D[1:0]	Used to configure the LED open load circuit diagnosis response and associated FLG pin behavior (driven or undriven). Available responses are: **Recovery**: When set, and PG is asserted, the LED open load diagnosis is performed. When a fault is detected, the LED driver imposes a current on the faulty branch, switching OFF the others. When a fault is recovered, the LED driver returns to normal operation. If the FLG pin is triggered externally, the LED driver outputs are switched OFF and the low power mode is entered. If PG is not asserted, FLG and/or load diagnosis are ignored. **Outage**: When set, the LED open load diagnostic is performed by the LED driver and Faulty_ch_1/2 registers are updated accordingly. When a fault is detected no action is taken on the current regulation. If the FLG pin is triggered externally, no action is taken.		
	0	0	Detection is recovery – FLG undriven
	0	1	Detection is recovery – FLG driven
	1	0	Detection is outage – FLG undriven
	1	1	Detection is outage – FLG driven
	Note 1: in case of GPWM pulsing, the device in recovery mode and R_{EXT} fault occur, active channels could have a residual random low light emission. Note 2: in case of GPWM pulsing, the device in recovery mode and an open fault or an Ext_fault occurs, remaining active channels could have a flicker. Note 3: if the device is in detection recovery with switch-on channels and, at least an open faulty occurs, if detection mode changes from recovery to outage, the effect is the power-on for all channels at the recovery current (30 mA typ.) and not at the current set by R_{EXT}. To resume the normal operation it is enough to toggle the output activation (OFF/ON) or recover the open channels.		
PWM_En	It indicates if the PWM function is enabled or disabled: 0: PWM OFF 1: PWM ON		

Field	Description
BDM_conf[x]	Represents the programmed output status of the channel x when the LED driver operates in BDM. This register is written by I²C message: 0: channel ON 1: channel OFF
Enable_CH[x]	Represents the status of the channel_x according to the table at the end of this paragraph. This register is read by I²C message: 0: channel ON 1: channel OFF

1. *Each time the LED driver passes from BDM to SAM mode, this bit is reset.*

Note: BDM_conf_1 register will be updated only if also BDM_conf_2 is transmitted and acknowledged. This is valid for dedicated commands, such as ID_FW_BDM, as well as direct register access ID_DR_ACS.

13.2 BDM_conf_2 / Enable_CH_2 register

Reg.name: BDM_conf_2 / Enable_CH_2

Reg. default value: 0x00

Reg. direct address: 0x01

Command involved: 0x00/0x02

Reg. access mode: R/W

	7	6	5	4	3	2	1	0
W	BDM_conf[7:0]							
R	Enable_CH[7:0]							

Table 15. BDM_conf_2 field descriptions

Field	Description
BDM_conf[x]	Represents the output status of the channel x when the LED driver operates in BDM. This register is written by I²C message: 0: channel ON 1: channel OFF
Enable_CH[x]	Represents the status of the channel x according to the table at the end of this section. This register is read by I²C message: 0: channel ON 1: channel OFF

13.3 BDM_status register

Reg. name: BDM_status
Reg. default value: 0x00
Reg. direct address: 0x02
Command involved: 0x08/0x0A
Reg. access mode: R

7	6	5	4	3	2	1	0
Rext_fault	Msg_err	Global_en	Diag_en	T_alert	T_fail	Ext_fault	LED_fault

Table 16. BDM_status field descriptions

Field	Description	Notes
Rext_fault	0: no fault detected 1: short-circuit on Rext connection detected	Set on fault detection, latched if permanent after 10 µs. Reset by HW if no fault detected permanently for at least 10 µs or by GPWM off. Note1: if the device has GPWM pulsing, V_{DDD} applied and a Rext_fault occurs, active channels could randomly flicker. Note2: if the device is in BDM and a double fault occurs: Ext_fault (input from FLG pin) + Rext_fault, on BDM status register, priority is assigned to Rext_fault. Ext_fault is reported only after Rext_fault solution.
Msg_err	0: no error detected on I²C messages 1: error detected in the last message received from I²C	Set on fault detection, reset on register reading.
Global_en	It brings information about the internal Global_EN signal (it deactivates all outputs when supply is below required minimum value): 0: global_en low 1: global_en high	Set on global_en assertion. Reset by HW on global_en deassertion.
Diag_en	It indicates if the LED driver supply voltage is in the diagnostic voltage range (Power Good above threshold, see the PG pin function): 0: outside the diagnostic voltage range 1: inside the diagnostic voltage range	Set on rising PG threshold exceeded. Reset by HW on falling PG threshold exceeded.
T_alert	It indicates if the device junction temperature is over T_{flg}: 0: internal temperature under T_{flg} 1: internal temperature over T_{flg}	Set on temperature exceeding T_{flg}. Reset on register reading.
T_fail	It indicates if the device junction temperature is over T_{sd}: 0: internal temperature under T_{sd} 1: internal temperature over T_{sd}	Set on temperature exceeding T_{sd}. Reset on the register reading.

Field	Description	Notes
Ext_fault	When a fault is detected by a LED driver connected on the same FLG pin, this flag is set: 0: no external fault 1: external fault occurred	Set on fault detection, latched if permanent after 10 µs. Reset by HW if no fault detected permanently for at least 10 µs. Note: if the device is in BDM and a double fault occurs: Ext_fault (input from FLG pin) + Rext_fault, on BDM status register, priority is assigned to Rext_fault. Ext_fault is reported only after Rext_fault solution.
LED_fault	When a fault is detected this flag is set: 0: open detection ok 1: open detection fault	If diag_en =1 set on fault detection, latched if permanent after 10 µs. Reset by HW if no fault detected permanently for at least 10 µs. Fault information maintained on falling PG threshold exceeded.

13.4 Faulty_ch_1 register

Reg. name: Faulty_ch_1
Reg. default value: 0x00
Reg. direct address: 0x03
Command involved: 0x09/0x0A/0x03
Reg. access mode: R/W bit[7] / R bit[3…0]

	7	6	5	4	3	2	1	0
W	PWM_presc	Not used	Not used	Not used	Reserved			
R					Faulty_ch[11:8]			

Table 17. Faulty_ch_1 field descriptions

Field	Description	Notes
PWM_presc	Represents the enable bit for PWM prescaler to let it work at half dimming frequency: 0: PWM @ 220 Hz (typ.) 1: PWM @ 110 Hz (typ.)	
Faulty_ch[x]	This register can be written by the diagnostic block only and indicates in which channel a fault is detected: 0: no fault 1: fault on channel x	If diag_en = 1 set on fault detection, latched if permanent after 10 µs, reset on register reading (see BDM_status register)

13.5 Faulty_ch_2 register

Reg. name: Faulty_ch_2
Reg. default value: 0x00
Reg. direct address: 0x04
Command involved: 0x09/0x0A
Reg. access mode: R

7	6	5	4	3	2	1	0
Faulty_ch[7:0]							

Table 18. Faulty_ch_2 field descriptions

Field	Description	Notes
Faulty_ch[x]	This register can be written by the diagnostic block only and indicates in which channels a fault is detected: 0: no fault 1: fault on channel x	If diag_en = 1 set on fault detection, latched if permanent after 10 µs, reset on register reading (see BDM_status register)

13.6 PWM_gain_x register

Reg. name: PWM_gain_x (0 ≤ x ≤ 11)
Reg. default value: 0x00
Reg. direct address: 0x05 to 0x10 (0x05 refers to ch0 to 0x10 refers to ch11)
Command involved: 0x01/0x02
Reg. access mode: R/W

7	6	5	4	3	2	1	0
PWM_ch_on	PWM_gain_x[6:0]						

Table 19. PWM_gain_x field descriptions

Field	Description
PWM_ch_on [7]	This bit allows channel x activation or deactivation: 0: channel OFF 1: channel controlled by PWM_gain_x
PWM_gain_x [6:0]	Represents the 7 bit PWM gain on the channel x. This register is set by I²C message (see duty cycle step table). Default value is 0x00

Note: PWM_gain_x registers are programmed sequentially due to serial nature of I²C protocol, this might affect desired channel behavior whenever I²C transaction falls in the edge between two dimming cycles.

13.7 LDD register (LED driver device versioning)

Reg. name: LDD
Reg. default value: HW defined (current version: 0x07)
Command involved: 0x28
Reg. access mode: R

7	6	5	4	3	2	1	0
Device ID					Revision ID		

Table 20. LDD field descriptions

Field	Description
Device ID [7:3]	These bits identify the device type: 00000: ALED1262ZT
Revision ID [2:0]	111

13.8 OTP/SAM_conf_1_2 register

Reg. name: SAM_conf_1_2
Reg. default value: 0x00
Reg. direct address: 0x20
Command involved: 0x20/0x21/0x28
Reg. access mode: R/W

7	6	5	4	3	2	1	0
SAM_conf_2[11:8]				SAM_conf_1[11:8]			

Table 21. OTP / SAM_conf_1_2 field descriptions

Field	Description
SAM_conf_2[x]	Represents the output status of the channel x = [11:8] when the SAM_conf_2 is chosen by the external OTP1/2 pin high: 0: channel ON 1: channel OFF
SAM_conf_1[x]	Represents the output status of the channel x = [11:8] when the SAM_conf_1 is chosen by the external OTP1/2 pin low: 0: channel ON 1: channel OFF

13.9 OTP/SAM_conf_1 register

Reg. name: SAM_conf_1
Reg. default value: 0x00
Reg. direct address: 0x21
Command involved: 0x20/0x21/0x28
Reg. access mode: R/W

7	6	5	4	3	2	1	0
SAM_conf_1[7:0]							

Table 22. OTP / SAM_conf_1 field descriptions

Field	Description
SAM_conf_1[x]	Represents the output status of the channel x = [7:0] when the SAM_conf_1 is chosen by the external OTP1/2 pin low 0: channel ON 1: channel OFF

13.10 OTP/SAM_conf_2 register

Reg. name: SAM_conf_2
Reg. default value: 0x00
Reg. direct address: 0x22
Command involved: 0x20/0x21/0x28
Reg. access mode: R/W

7	6	5	4	3	2	1	0
SAM_conf_2[7:0]							

Table 23. SAM_conf_2 field description

Field	Description
SAM_conf_2[x]	Represents the output status of the channel x = [7:0] when the SAM_conf_2 is chosen by the external OTP1/2 pin high 0: channel ON 1: channel OFF

13.11 OTP/BA_n_SAM_setting register

Reg. name: BA_n_SAM_setting
Reg. default value: 0x00
Reg. direct address: 0x23
Command involved: 0x20/0x21/0x28
Reg. access mode: R/W

7	6	5	4	3	2	1	0
I²C_HA	D[1:0]		Bus_address[4:0]				

Table 24. OTP / BA_n_SAM_setting field descriptions

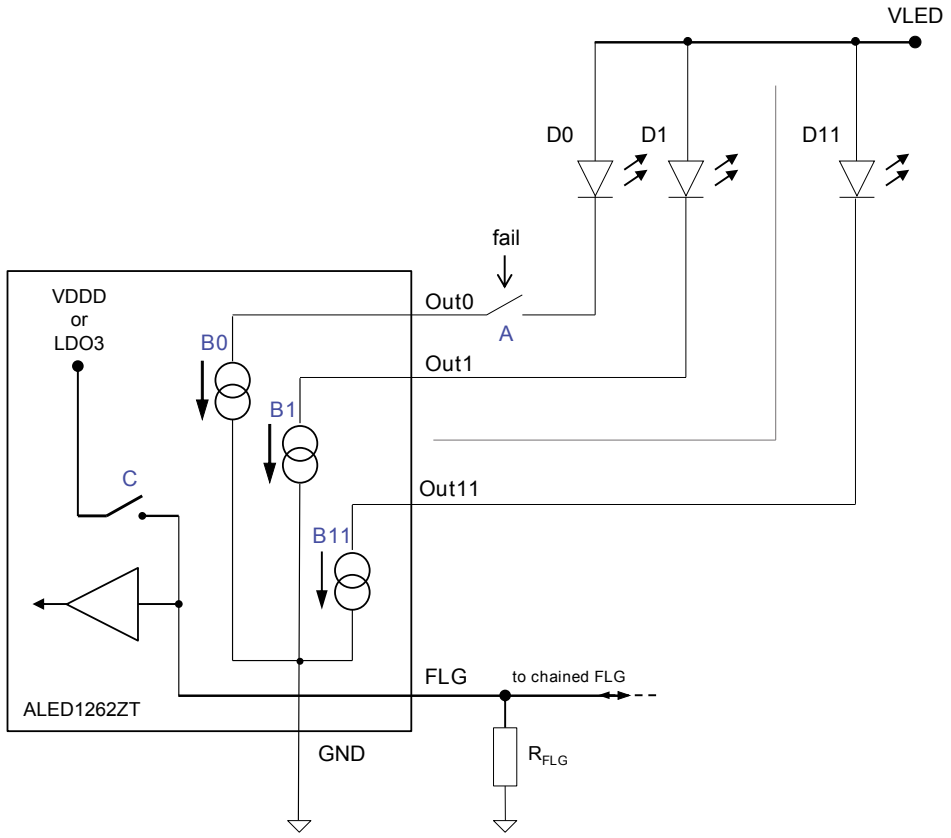
Field	Description		
I²C_HA	Bus-driven mode error protection/detection on communication: I²C Hamming encoding enable 0: parity check OFF 1: parity check ON		
D[1:0]	Used to configure the LED open load circuit diagnosis response and associated FLG pin behavior (driven or undriven). Available responses are: **Recovery**: when set, and PG is asserted, the LED open load diagnosis is performed. When a fault is detected, the LED driver imposes a current on the faulty branch, by switching OFF the others. When a fault is recovered, the LED driver returns to normal operation. If the FLG pin is triggered externally, the LED driver outputs are switched OFF and the low power mode is entered. If PG is not asserted, FLG and/or load diagnosis are ignored. **Outage**: when set, the LED open load diagnostic is performed by the LED driver. When a fault is detected no action is taken on the current regulation. If the FLG pin is triggered externally, no action is taken.		
	0	0	Detection is recovery – FLG undriven
	0	1	Detection is recovery – FLG driven
	1	0	Detection is outage – FLG undriven
	1	1	Detection is outage – FLG driven
	Note 1: in case of GPWM pulsing, the device in recovery mode and R_{EXT} fault occur, active channels could have a residual random low light emission. *Note 2*: in case of GPWM pulsing, the device in recovery mode and an open fault or an Ext_fault occur, remaining active channels could have a very light flicker.		
Bus_address[4:0]	A 7-bit wide address space theoretically allows 128 I²C addresses; however, some addresses are reserved for special purposes. Thus, only 112 addresses are available with the 7-bit address scheme imposed by the I²C bus standard. Nevertheless only 5 LSB can be defined in this register (the others are fixed at 01 so: 01xxxxx) allowing 32 possible slave addresses only.		

Table 25. Enable_CH[x] register content

Mode	Fault status	Notes	Enable_CH[x] register content
BDM	Any	BDM_Flag = 1 PWM_En = 0	Enable_CH[11:0] = BDM_conf[11:0] (1)
BDM / PWM	Any	BDM_Flag = 1 PWM_En = 1	Enable_CH[x] = {PWM_ch_on[x] **AND** BDM_conf[x]} **OR** (**NOT** PWM_ch_on[x](2)); with x=[0:11]
SAM	Any	BDM_Flag = 0 OTP1/2 pin = 0	Enable_CH[11:0] = SAM_conf_1[11:0] (1)
SAM	Any	BDM_Flag = 0 OTP1/2 pin = 1	Enable_CH[11:0] = SAM_conf_2[11:0]

1. *'0' if channel is ON; '1' if channel is OFF*
2. *'0' if channel is OFF; '1' if channel is controlled by PWM_gain_x*

Figure 12. LED open circuit diagnosis response table



Configuration	A	B0	From B1 to 11	C	Out0	From Out1 to 11
Recovery + int. FLG driven	Open: D0 failed	ON (Iout_recovery)	OFF	ON	tries to recover	OFF
Recovery + int. FLG undriven	Open: D0 failed	ON (Iout_recovery)	OFF	OFF	tries to recover	OFF
Outage + int. FLG driven	Open: D0 failed	ON (Iout_regulation)	ON	ON	tries to regulate	regulation
Outage + int. FLG undriven	Open: D0 failed	ON (Iout_regulation)	ON	OFF	tries to regulate	regulation
Recovery (+ external FLG sig. H)	Close: D0 OK	OFF	OFF	OFF	OFF	OFF
Outage (+ external FLG sig. H)	Close: D0 OK	ON (Iout_regulation)	ON	OFF	regulation	regulation

14 I²C bus operations

The ALED1262ZT can operate both in standalone mode and bus-driven mode. When an MCU is present on the application, it can drive communication following the I²C bus protocol (the bus is active 80 µs after V_{DDD} plug). Such a task is performed by an internal digital block, which implements a slave I²C communication peripheral as described in the reference documentation published by NXP (UM10204: I²C bus specification and user manual rev.6, 04 April 2014).

The ALED1262ZT operates as slave only, standard (up to 100 kHz) or fast (up to 400 kHz) mode. Clock stretching operation is performed by the ALED1262ZT when needed. During the bidirectional communication, to minimize EMI interferences, SDA and SCL low-side MOS are driven to slow falling edges according to the bus parasitic and/or connected capacity (typ. ≈ 100 ns; see the following charts).

Figure 13. Slave SDA falling time vs CBus Rup = 1.8 kΩ, V_{DDD} = 5 V

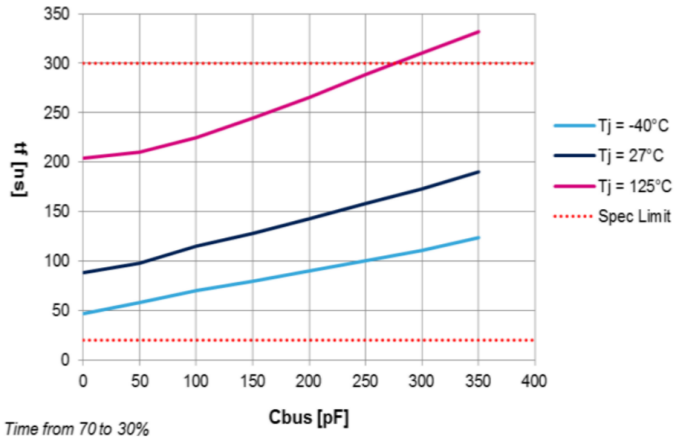
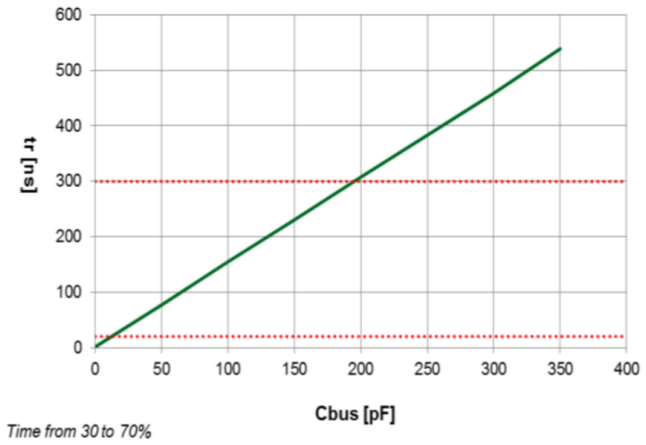


Figure 14. Slave SDA rising time vs CBus Rup = 1.8 kΩ, V_{DDD} = 5 V, -40 < T_J < 125 °C



14.1 I²C main concepts

I²C communication, performed on a two signal basis, is a synchronous half duplex protocol. Signals are conveniently named as SCL (synchronization signal from MASTER to SLAVE) and SDA (data signal which can be either MASTER to SLAVE, or SLAVE to MASTER).

The multi-MASTER application configuration, which is a MASTER specific property, is supported by the ALED1262ZT.

I²C communication is driven by specific events on the bus:

- START condition - it is a falling edge of SDA while SCL is HIGH level
- Slave addressing - it is the transmission (M→S) of the ID of the slave to be addressed (7-bit)
- Communication direction - it is one bit immediately following the slave ID: 0 for writing (M→S) or 1 for reading (S→M)
- Acknowledge - it is a LOW level on SDA line; driven by either SLAVE or MASTER depending on the communication moment
- Data bit - data are 8-bit per word driven either by MASTER or SLAVE depending on the communication moment
- STOP condition – it is a rising edge of SDA while SCL is HIGH level
- Restart condition - it is a new START condition which happens before a STOP condition: it normally implies a change in the direction of the communication

15 I²C addressing for the ALED1262ZT

Since having more than a single ALED1262ZT device is allowed in this application, a method to differentiate each of them has been put in place. Five OTPs (one time programmable) memory cells are dedicated to differentiate LSB bit of the ALED1262ZT address; this leads up to 31 devices valid addresses usable in the final application.

When OTP has not been programmed yet to address one specific SLAVE in the application board, an extra signal named CS is used (which is not part of I²C standard). CS pin is a chip select signal (active HIGH), it is internally pulled down by a resistor. Hence the recommended application scheme should connect all the ALED1262ZT devices CS pin to a corresponding output pin in the programmer.

When in the end factory line programming, the testing/set-up system has to leave floating CS pin on all the devices except the one meant to be programmed at that specific time, on this specific device, CS must be polarized at 15 V. For ‘fresh device’, the address is “0100000” (0x40 including the writing bit or 0x41 including the reading bit).

Once the programming of all devices is over, all CS pins must be left floating (fixed low by internal pull-down), the addressing, by MCU in application, is performed by each programmed address as a traditional I²C bus.

16 I²C selectable Hamming (8, 4) encoding

By bit-7 in BA_n_SAM_setting OTP byte, the user has the possibility to enable/disable the error detection on I²C bus communication.

Reg. name: BA_n_SAM_setting

7	6	5	4	3	2	1	0
I²C_HA	D[1:0]		Bus_address[4:0]				

Table 26. Excerpt from table "OTP / BA_n_SAM_setting field descriptions"

Field	Description
I²C_HA	Bus-driven mode error protection/detection on communication: I²C Hamming encoding enable 0: parity check OFF 1: parity check ON

Error detection occurs thanks to the extended Hamming code (8, 4), encoding info sent through the bus. The encoding packs 4-bit of useful information with 4-bit of parity checks. The benefit of the chosen encoding algorithm is the opportunity to detect up to 3-bit error along with each byte transfer. Encoding algorithm packs together payload bit and parity bit in the following structure:

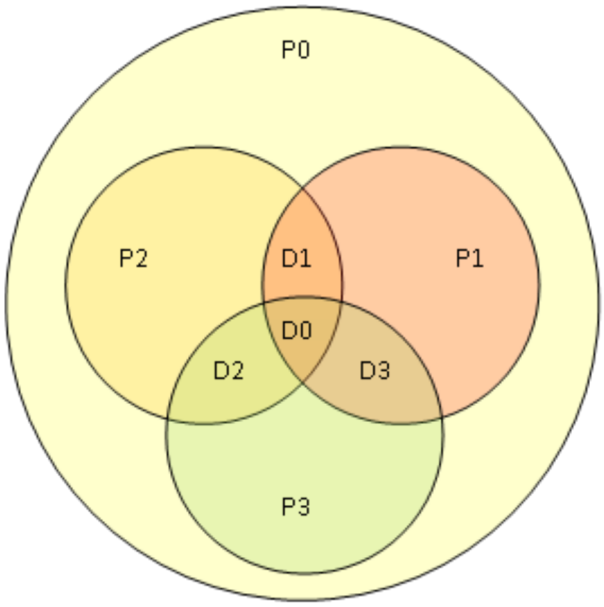
7	6	5	4	3	2	1	0
D3	D2	D1	P3	D0	P2	P1	P0

Where Dx represents data bit (useful information) and Px represents parity bit. Hereafter the encoding of parity bit vs data bit:

P3	D3 ⊕ D2 ⊕ D0
P2	D2 ⊕ D1 ⊕ D0
P1	D3 ⊕ D1 ⊕ D0
P0	D3 ⊕ D2 ⊕ D1 ⊕ P3 ⊕ D0 ⊕ P2 ⊕ P1

A graphical view of the encoding is shown below:

Figure 15. **Graphic view of encoding**



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The following table provides all available datawords and corresponding codewords:

Table 27. **Datawords and corresponding codewords**

	D3	D2	D1	D0		D3	D2	D1	P3	D0	P2	P1	P0
DW0	0	0	0	0	CW0	0	0	0	0	0	0	0	0
DW1	0	0	0	1	CW1	0	0	0	1	1	1	1	0
DW2	0	0	1	0	CW2	0	0	1	0	0	1	1	1
DW3	0	0	1	1	CW3	0	0	1	1	1	0	0	1
DW4	0	1	0	0	CW4	0	1	0	1	0	1	0	1
DW5	0	1	0	1	CW5	0	1	0	0	1	0	1	1
DW6	0	1	1	0	CW6	0	1	1	1	0	0	1	0
DW7	0	1	1	1	CW7	0	1	1	0	1	1	0	0
DW8	1	0	0	0	CW8	1	0	0	1	0	0	1	1
DW9	1	0	0	1	CW9	1	0	0	0	1	1	0	1
DW10	1	0	1	0	CW10	1	0	1	1	0	1	0	0
DW11	1	0	1	1	CW11	1	0	1	0	1	0	1	0
DW12	1	1	0	0	CW12	1	1	0	0	0	1	1	0
DW13	1	1	0	1	CW13	1	1	0	1	1	0	0	0
DW14	1	1	1	0	CW14	1	1	1	0	0	0	0	1
DW15	1	1	1	1	CW15	1	1	1	1	1	1	1	1

Figure 16. **Excerpt of communication scheme in application**

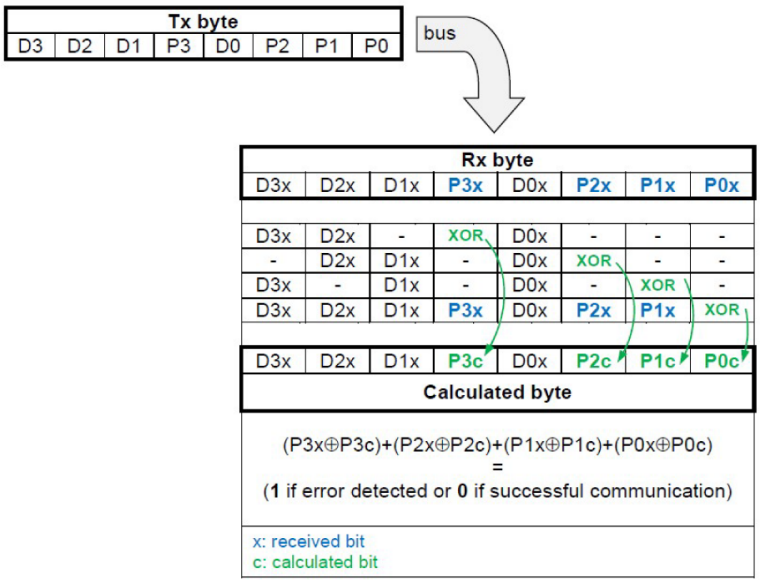


Table 28. **Not encoded nibbles and equivalent Hamming bytes**

HEX format	Nibble	Hamming (8, 4) encoding	Byte
0	0000	00	00000000
1	0001	1E	00011110
2	0010	27	00100111
3	0011	39	00111001
4	0100	55	01010101
5	0101	4B	01001011
6	0110	72	01110010
7	0111	6C	01101100
8	1000	93	10010011
9	1001	8D	10001101
A	1010	B4	10110100
B	1011	AA	10101010
C	1100	C6	11000110
D	1101	D8	11011000
E	1110	E1	11100001
F	1111	FF	11111111

17 Message structure

17.1 Available commands

A set of commands has been implemented to recall the functions made available by I²C communication.

A brief table with their representation and description is presented hereafter; these commands are found in the following pages where the structure of messages is presented.

Table 29. Command representation and description

Command ID mnemonic name	Hex format (8-bit)	Hamming (8,4) encoding	Affected registers	Description
ID_FW_BDM (functional write BDM)	0x00	0x00/0x00	BDM_conf[1|2]	Enables BDM_conf[1|2] registers write to LED driver. Both registers are effective after the second one has been received. If the second register is not transmitted or it is not acknowledged, then the first one is not updated.
ID_FW_PWM (functional write PWM)	0x01	0x00/0x1E	PWM_gain_[0...11]	Enables PWM_gain_[0...11] registers write to LED driver. Each register is effective just after acknowledgment. If LED driver does not acknowledge a byte, it is updated and the master has to stop data transfer to resume communication.
ID_FW_FULL (functional write BDM + PWM)	0x02	0x00/0x27	BDM_conf[1|2] + PWM_gain_[0...11]	Enables all BDM_conf[1|2] and PWM_gain_[0…11] registers write to LED driver.
ID_FW_FLT (functional write faulty)	0x03	0x00/0x39	FAULTY_ch1[7]	Enables FAULTY_ch1[7] bit register write (110/220 Hz prescaler)
ID_FR_STS (functional read status)	0x08	0x00/0x93	BDM_status	Enables BDM_status register read from LED driver.
ID_FR_FLT (functional read faulty)	0x09	0x00/0x8D	Faulty_ch[1|2]	Enables Faulty_ch[1|2] registers read from LED driver.
ID_FR_FULL (functional read channels enabled + status + faulty + PWM)	0x0A	0x00/0xB4	Enable_CH[1|2] + BDM_status + Faulty_ch[1|2] + PWM_gain_[0…11]	Enables all actual Enable_CH[1|2], BDM_status, Faulty_ch[1|2] and PWM_gain_[0...11] registers read from LED driver.
ID_FR_PWM (functional read PWM)	0x0B	0x00/0xAA	PWM_gain_[0…11]	Enables PWM_gain_[0…11] registers read from LED driver.
ID_EW_EMU (end-of-line write emulation)	0x20	0x27/0x00	SAM_conf_* + BA_n_SAM_setting	Enables all SAM_conf_* and BA_n_SAM_setting registers write to LED driver (OTP emulation).
ID_EW_BURN (end-of-line write burning)	0x21	0x27/0x1E	SAM_conf_* + BA_n_SAM_setting	Enables all SAM_conf_* and BA_n_SAM_setting registers are burnt on OTPs (OTP burn).
ID_ER_OTP (end-of-line read OTP)	0x28	0x27/0x93	LDD + SAM_conf_* + BA_n_SAM_setting	Enables the read back of: SAM_conf_* and BA_n_SAM_setting, registers as programmed by OTPs. It allows LDD byte (OTP read) to be read back.

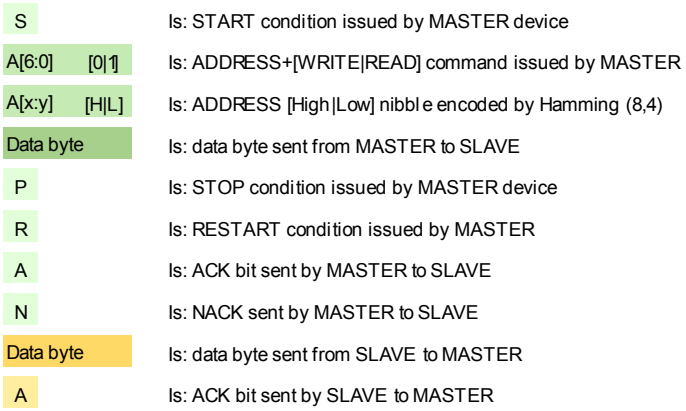
Command ID mnemonic name	Hex format (8-bit)	Hamming (8,4) encoding	Affected registers	Description
ID_DR_ACS (direct register access)	0x81	0x93/0x1E	All	Enables the direct access, for writing or reading, to all registers. See specific register address on the related table.

During reading and writing operations the basic master transmission is:

1. slave address + write bit (as per I²C protocol)
2. slave address repeating (slave replies ACK or NACK according to own I²C actual address)
3. command ID (according to the table above, a wrong command ID results in a slave NACK)
4. read or write sequence as described on the following sections (see write and read operations)

17.2 Pattern symbols

Figure 17. Pattern symbols



17.3 Write operations

In some cases, during the write operation, the whole setting information has to be split into different bytes, to avoid a partial device set-up change, related registers are updated only after full data receiving. In case of aborted communication, a stop signal restores the bus. Affected registers:

- Without parity detection
  - BDM_conf_1 + BDM_conf_2, registers updated at the end of the second byte
  - All remaining registers are updated at the end of the byte
- With parity detection
  - BDM_conf_1 + BDM_conf_2, registers updated at the end of the fourth byte (if correctly received)
  - All remaining registers are updated at the end of the second byte (if correctly received)

17.3.1 BDM configuration register write

Figure 18. Without parity detection (4 bytes)

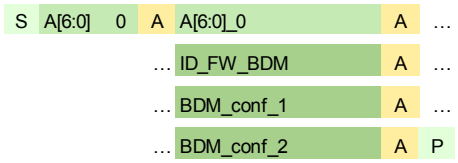
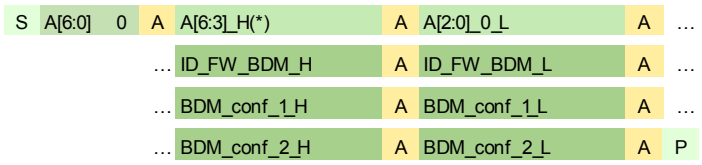


Figure 19. With parity detection (8 bytes)



Note: (*) e.g. BDM_conf_1_H = BDM_conf_1[7:4] w/ error detection; BDM_conf_1_L = BMD_conf_1[3:0] W/ error detection.

17.3.2 FAULTY_ch1[7] bit register write (prescaler)

Figure 20. Without parity detection (3 bytes)

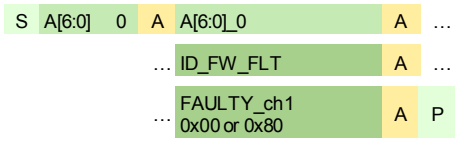
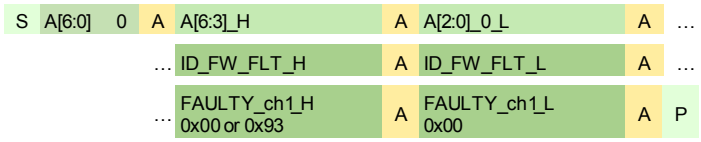


Figure 21. With parity detection (6 bytes)



17.3.3 PWM_gain_x register write

Figure 22. Without parity detection (14 bytes)

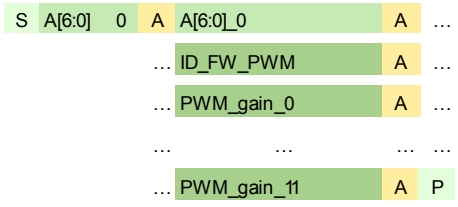
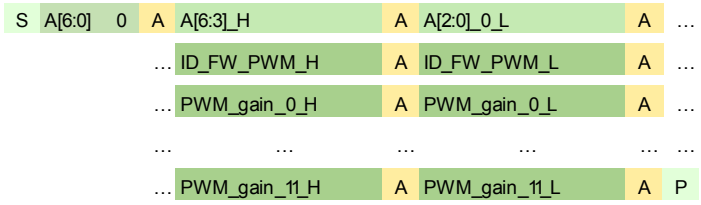


Figure 23. With parity detection (28 bytes)



17.3.4 BDM_conf and PWM_gain_x register write

Figure 24. Without parity detection (16 bytes)

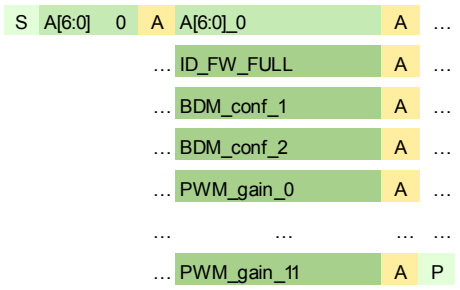
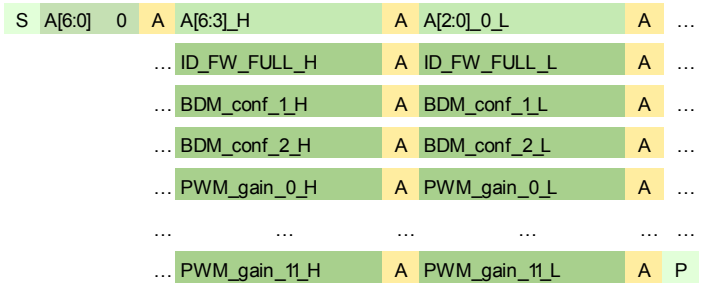


Figure 25. With parity detection (32 bytes)



Please note that, in terms of output duty cycle, each PWM_gain_x byte (or PWM_gain_x_H + PWM_gain_x_L bytes with parity detection) is updated at the end of each dimming count and the remaining channels PWM_gain_x byte transmission are disregarded. The same for PWM_ch_on [7] bit that switches each channel from controlled by PWM gain value to OFF (0: Channel OFF; 1: channel controlled by PWM_gain_x). Instead, BDM_conf[x] bit inside BDM_conf_1/2 registers updates instantly channel status (ON or OFF) ignoring PWM counter progression. Besides, PWM_En bit on BDM_conf_1 register updates instantly the channel status (dimming enabled or disabled) ignoring PWM counter progression.

In case of writing additional bytes beyond those expected by the specific command, extra data are ignored.

17.3.5 Direct write on registers

Figure 26. Without parity detection (16 bytes)

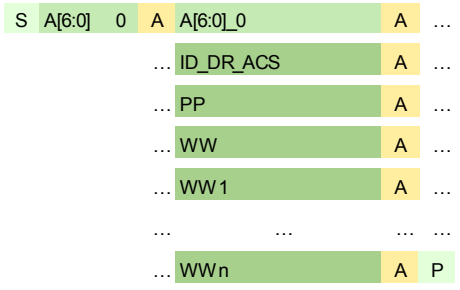
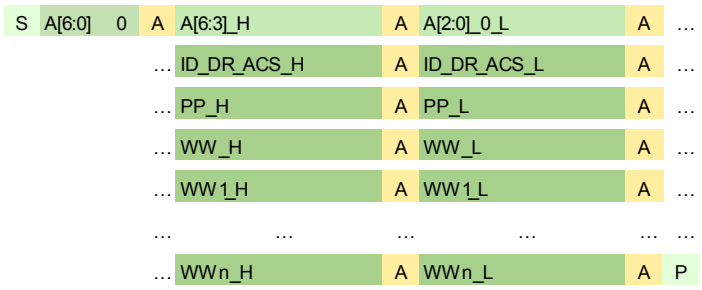


Figure 27. With parity detection (32 bytes)



Where: WW is the content to be written on register at position PP (direct address), WW1 to be written on register at position PP+1 and so on.

Note: Please note that PP+n position must be maintained inside allowed address intervals: 0x00 ≤ PP+n ≤ 0x10 (BDM) and 0x20 ≤ PP+n ≤ 0x23 (SAM). Outside these intervals all other addresses are forbidden.

See also the register address table.

17.4 Read operations

17.4.1 Status register

Figure 28. Without parity detection (4 bytes)

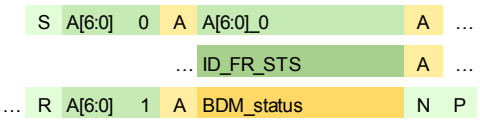
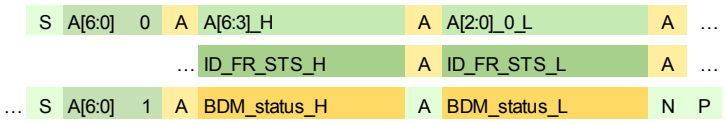


Figure 29. With parity detection (7 bytes)



17.4.2 Faulty_ch registers

Figure 30. Without parity detection (5 bytes)

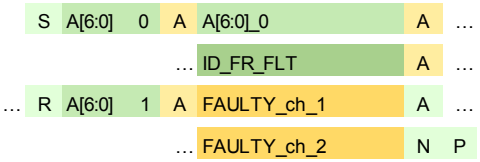
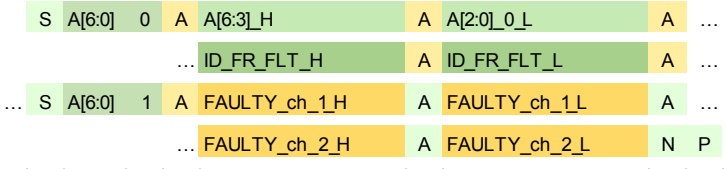


Figure 31. With parity detection (9 bytes)



17.4.3 PWM_gain_x registers

Figure 32. Without parity detection (15 bytes)

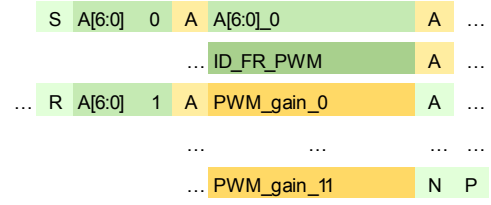
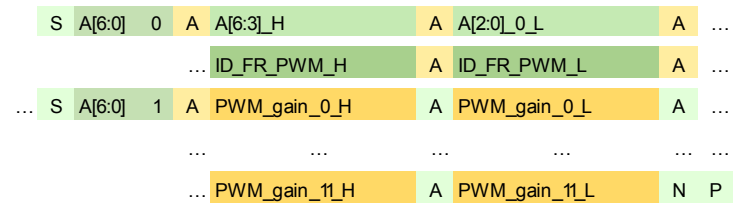


Figure 33. With parity detection (29 bytes)



17.4.4 BDM_conf, status, Faulty_ch, PWM_gain_x registers

Figure 34. Without parity detection (20 bytes)

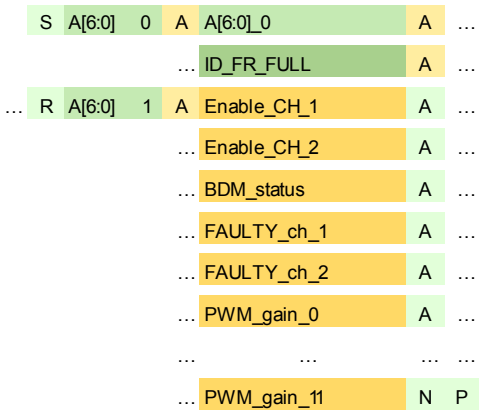
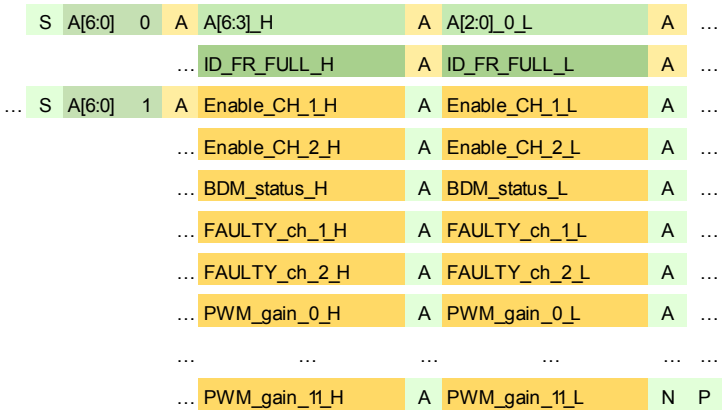


Figure 35. With parity detection (39 bytes)



In case of reading additional bytes beyond those provided by the specific command, the extra bit is zeroed.

17.4.5 Direct read from registers

Figure 36. Without parity detection

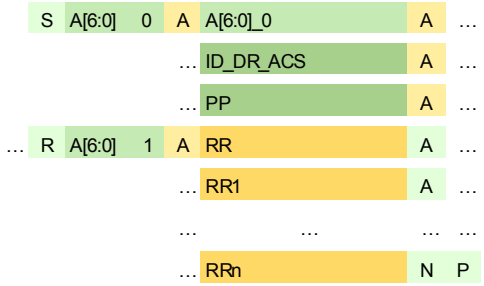
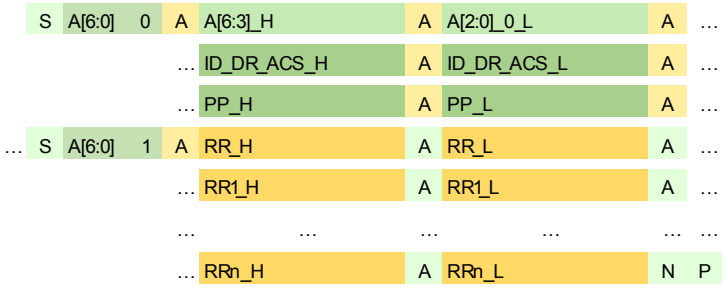


Figure 37. With parity detection



Where: RR is the content to be read from register at position PP (direct address), RR1 to be read from register at position PP+1 and so on. If PP+n position has not the corresponding register location, read data must be ignored. See also the register address table.

Please note that, if I²C communication starts with slave address plus reading bit (A[6:0]_1 as first byte is a word allowed by I²C standard but not allowed on the ALED1262ZT protocol), the related slave device reply data has to be ignored. Normal communication is resumed with a stop transition.

18 OTP operations

The ALED1262ZT can operate in standalone mode (SAM); the functionality in this working mode is configured by four registers: SAM_conf_1_2, SAM_conf_1, SAM_conf_2 and BA_n_SAM_setting. Refer to OTP register description for further information.

This configuration can be programmed during one time set phase at the end of the customer production line. The 32 bits of such configuration are stored, with Error-correcting code (ECC) and fully redundancy, into 80 OTP (one time programmable) cells.

Before the OTP zapping an ECC control word is generated based on the content of the four registers and all the resulting bits are stored in paired OTP cells. During the OTP load, happening at start up or after an HW reset, the paired cells are ORed, the resulting data is controlled by ECC word and copied into the four registers.

For non-volatile register programming and communication, we have to connect:

- V_{DDD} to 5 V
- SDA and SCL connected to 100 or 400 kHz I²C bus (W/O or W parity check according to OTP/ BA_n_SAM_setting [bit 7] programmed 0 or 1)
- CS used to address on application board device to be programmed (I²C address is not yet available because itself is to be programmed). CS pin must be supplied at 15 V with current capability I_{CS} > 100 mA.
- GND to power supply and I²C controller ground (general ground connection)

To program OTPs, the user needs to address the device; in case of ‘fresh device’, the address is “0100000” (0x40 including the writing bit or 0x41 including the reading bit); and drives HIGH to 15 V the CS pin. In this condition, the user can proceed with the OTP message to program the fuses. In case of several devices on same I²C bus, programming functions must be performed on a single device by time. This means that all others CS pin must be floating (it means LOW by internal pull-down resistor). After the device power supply and 15 V as CS polarization, OTP operation message must be sent by I²C bus master.

Three operations are available on OTP cells: EMULATE, BURN and READ.

EMULATE and READ are possible at any time without special care.

While BURN execution need a special attention because of ECC; the complete full procedure, based on a double zap, must be executed in a single run (meaning using same data configuration) since ECC is computed for the data actually present into non-volatile registers and once stored into OTP, cells cannot be modified any longer.

To invoke such operations, see related message structure and commands.

18.1 OTP emulate

To emulate OTPs, the user needs to address the device by using the actual device address (which may differ from default if the emulation/burning on BA_n_SAM_setting[4:0] bits has been performed sometimes in the past). Emulated bits are reset at their original status after an electrical HW reset that force an OTP load.

The OTP emulate command writes data inside shadow registers, such data will be transferred to the OTP cells only when the OTP Burn command will be issued. Anyway, ALED1262ZT will apply immediately the data written into shadow registers. This means that modifying in emulation the BA_n_SAM_setting[4:0] bits, the I²C address changes immediately and so the following commands have to use the new set address.

Figure 38. Emulate OTP bit without parity detection

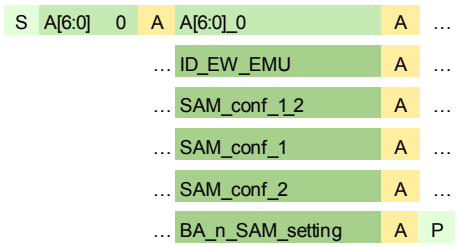
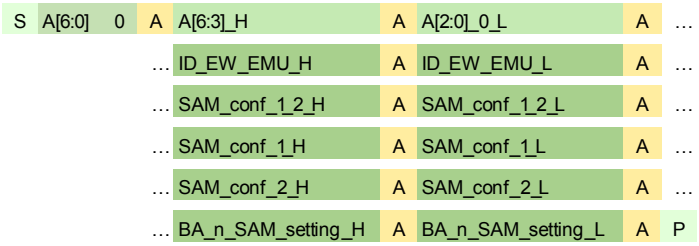


Figure 39. **Emulate OTP bit with parity detection**



18.2 OTP burn

To program OTPs, user needs to address the device by using the current device address (which may vary if the emulation/burning on BA_n_SAM_setting[4:0] bits has been performed sometime in the past) and driving accordingly the CS pin (CS is also the high voltage pin carrying the current used to zap OTPs). Before any burning command, OTP registers must be emulated as described in the previous section. OTP burn command writes permanently the emulated configuration on the device OTP banks.

In order to minimize the number of OTP cells which could had a not perfect burn it is requested to execute the OTP burn command twice without any change in the emulated configuration.

OTP burn has to be executed in a single run (meaning using same data configuration) since ECC is computed for the actual data present into non-volatile registers and once zapped into OTP cells can be confirmed but not modified.

When customer issues the command OTP burn, ALED1262ZT will compute the ECC word from the 32 bit of the four non-volatile registers; this ECC word allows the automatic correction of 1 bit error. Once all data will be ready ALED1262ZT generates sequentially the burning signals for zapping all the 80 OTP cells.

The OTP cells burning takes about 80 ms, this means that CS voltage has to be kept active for at least this time after the latest I²C 'acknowledge' sent by SLAVE.

During the burning process, ALED1262ZT puts on hold any running I²C communication using the clock stretching mechanism. This means that SCL pin is grounded for all the burning period in case the I²C communication is still active when Burn process starts. In same cases, with very fast I²C master, to force clock stretching it is necessary to add a "fake" byte before the Stop, if needed to know the real burning process duration.

Figure 40. **Burn OTP bit without parity detection**

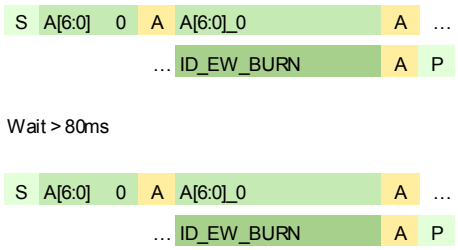
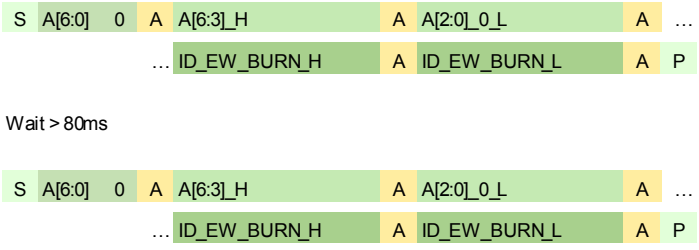


Figure 41. **Burn OTP bit with parity detection**



18.3 OTP read

After programming the device, user has to reset the device in order to force a data load and to be able to read back the OTP written values to validate their status. The address to be used to read back the data is: “01” + BA_n_SAM_setting [4:0] as LSB.

Figure 42. Read back OTP bit without parity detection

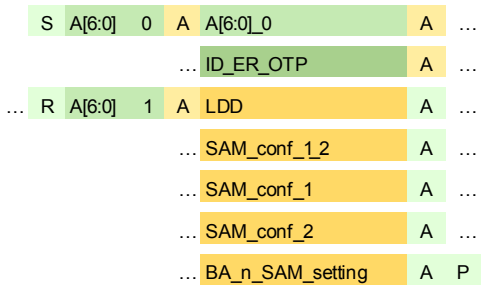
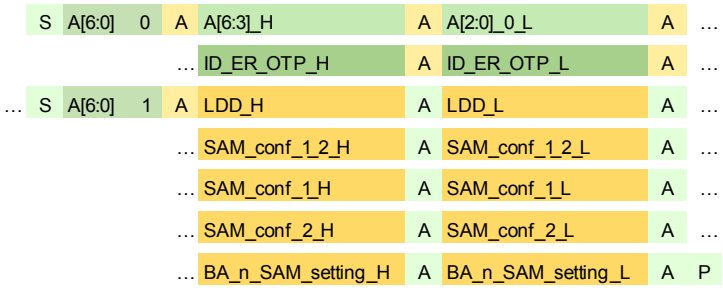


Figure 43. Read back OTP bit with parity detection



19 I²C communication examples

19.1 Communication without parity detection

19.1.1 OTP burning with double zap and read back

To emulate as example the address 0100001 the following sequence is needed:

- CS = 15 V
- VDDD = 5 V
- 0x40 0x40 0x20 0x00 0x00 0x00 0x01

Based on the new emulated address (0100001) the burning communication sequence is:

- 0x42 0x42 0x21
- wait > 80ms
- 0x42 0x42 0x21

Switch OFF the supply to be sure about the real burning before read back check using the following pattern:

- 0x42 0x42 0x28 R 0x43 **0x07 0x00 0x00 0x00 0x01**

(R means the restart condition; **in bold** the expected read back data, **0x07** is the current LDD value)
From now on, the device answers to 0x42 for writing and to 0x43 for reading operations; CS at 18 V for I²C communication is no more needed.

19.1.2 All LEDs with power-ON

To power on all the device output channels, in case of 0100001 I²C address, the following sequence is needed:

- CS = floating
- VDDD = 5 V
- VDDA = 12 V
- VLED according to number of LEDs in series per channel
- 0x42 0x42 0x00 0xA0 0x00

(0xA0 0x00 means: BDM_Flag = 1, detection = recovery, FLG = driven, PWM_En = OFF, channels from 11 to 0 = ON)

19.1.3 110 Hz dimming prescaler bit

For prescaler bit setting, 0100001 I²C address, the following sequence is needed:

- CS = floating
- VDDD = 5 V
- 0x42 0x42 0x03 0x80

(0x80 means: prescaler bit = 1)

19.1.4 All LEDs with PWM dimming at 50% (full configuration)

For PWM dimming setting, 0100001 I²C address, the following sequence is needed:

- CS = floating
- VDDD = 5 V
- VDDA = 12 V
- VLED according to number of LEDs per channel
- 0x42 0x42 0x02 0xB0 0x00 0xF2 0xF2 0xF2 0xF2 0xF2 0xF2 0xF2 0xF2 0xF2 0xF2 0xF2 0xF2

(0xB0 0x00 means: BDM_Flag=1, detection=recovery, FLG=driven, PWM_En=ON, channels from 11 to 0=ON; 0xF2 means dimming step #114)

19.1.5 Device status read back

For status read back, 0100001 I²C address, the following sequence is needed:

- CS = floating
- VDDD = 5 V
- 0x42 0x42 0x08 R 0x43 **0x??**

(R means the restart condition; **in bold** the read back data)

19.1.6 Device full status read back

For full status read back, 0100001 I²C address, the following sequence is needed:

- CS = floating
- VDDD = 5 V
- 0x42 0x42 0x0A R 0x43 **0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x?? 0x??**

(R means the restart condition; **in bold** the read back data)

To read the status up to faulty channels only it is matter to send a STOP condition after the fifth received byte, as shown in the following sequence:

- CS = floating
- VDDD = 5 V
- 0x42 0x42 0x0A R 0x43 **0x?? 0x?? 0x?? 0x?? 0x??** P

(R means the restart condition; P means the STOP condition; in bold the read back data).

19.1.7 LDD read back (device identifier)

For LDD read back, 0100001 I²C address, the following sequence is needed:

- CS = floating
- VDDD = 5 V
- 0x42 0x42 0x28 R 0x43 **0x07** P

(R means the restart condition; P means the STOP condition; **in bold** the read back data; **0x07** is current LDD value)

19.2 Communication with parity detection

19.2.1 All LEDs with power-ON

To power on all the device output channels, in case of **0100001** I²C address, the following sequence is needed:

- CS = floating
- VDDD = 5 V
- VDDA = 12 V
- VLED according to number of LEDs in series per channel

without parity detection pattern was:

- 0x42 0x42 0x00 0xA0 0x00

(0xA0 0x00 means: BDM_Flag=1, detection=recovery, FLG = driven, PWM_En = OFF, channels from 11 to 0 = ON)

With parity detection, we need to codify all words beyond the first address (0x42):

0x42, the repeated address, with Hamming encoding is 0x55 + 0x27 (see nibbles encoding table); byte 0x00 encoded is 0x00 + 0x00; byte 0xA0 encoded is 0xB4 + 0x00. So full pattern with Hamming (8, 4) is:

- 0x42 0x55 0x27 0x00 0x00 0xB4 0x00 0x00 0x00

This sequence powers on all the device output channels.

20 LED supply voltage

LED supply voltage (V_{LED}) must be chosen by taking into account several parameters:

- The voltage drop across each current generators (V_{DROP}) must be enough to guarantee the current regulation (see dedicated section in the datasheet)
- The maximum LED forward voltage ($V_{F,max}$)
- The maximum power that can be dissipated by the package under the application ambient conditions
- The accuracy of the supply voltage itself (V_{LED} can vary in a range and the minimum and maximum values must be considered)

Therefore the minimum LED supply voltage can be calculated as:

$$V_{LED,\ min} = V_{DROP,\ min} + V_{F,max}$$

The worst case for power dissipation is to consider all channels connected to LEDs at minimum V_F and maximum V_{LED}:

$$V_{DROP,max} = V_{LED,max} - V_{F,min}$$

The LED supply voltage should be higher than $V_{LED,min}$ (to consider any fluctuation of the involved parameters) but not too high in order to keep low the power dissipation:

$$P_D = V_{DDD} \cdot I_{DDD} + V_{DDA} \cdot I_{DDA} + \Sigma_{i=0}^{11} V_{DROP\_max\_i} \cdot I_{CHi}$$

where V_{DDA} and V_{DDD} are the device voltage supplies, I_{DDA} and I_{DDD} are the device supply currents, $V_{DROP\_max\_i}$ and I_{CHi} are respectively the maximum voltage drop across the current generator "i" and the channel "i" current. The simplified equation is the following:

$$P_D \cong \Sigma_{i=0}^{11} V_{DROP\_max\_i} \cdot I_{CHi}$$

The power dissipation should be kept below the maximum power dissipation, defined as:

$$P_{D,\ max} = \frac{(T_j - T_a)}{\theta_{ja}}$$

where T_j and T_a are respectively the maximum junction and ambient temperature, whereas θ_{ja} is the junction-to-ambient thermal resistance ($R_{thj\text{-}amb}$). Junction temperature should be maintained below 150 °C.

To summarize, the proper power supply choice must be a trade-off between the correct value assuring the desired LED current and the lowest power dissipation.

In multi-type LED applications, there can be a significant variability of the LED forward voltage (e.g. red LEDs have a lower forward voltage than white, green or blue LEDs).

In this case, the supply voltage must be chosen so to correctly switch on the LEDs with the highest forward voltage. At the same time, the excess of voltage in the lines with the lowest forward voltage LEDs drops on the current generators, increasing the power dissipation and the loss of efficiency.

To avoid these drawbacks, two different approaches are possible:

1. Adding a resistor in series to each low forward voltage LEDs. In this way, the voltage excess drops across the resistor instead of dropping across the current generators. This solution implies a significant reduction of the power dissipated by the chip (lower T_j). However the total power dissipation does not change and a remarkable part of the power is still wasted on the series resistor. This not only affects the efficiency, but also raises the cost of the system due to the need to dissipate the generated heat.
2. Another solution is to split the LED voltage rail: one for high forward voltage LEDs and one for low forward voltage LEDs, which can be derived from the former using a switching regulator. This solution is by far the most advantageous in terms of power dissipation. Voltage rails are tailored to the type of LEDs they drive and the wasted power is significantly reduced as well as the heat produced.

21 Higher current requests (outputs in parallel)

When the application requires driving high power LEDs, the current demand could be higher than the current provided by a single channel. In this case a higher current capability can be achieved by connecting together two or more channels (in accordance with the current value, it must be regulated). Normally no stability issues are shown using this output connection but, in any case, a bypass capacitor on driver power supplies (of about 1 µF on V_{DDA} and V_{DDD}) and in particular a bypass capacitor near LED anodes on VLED power supply rail (2.2 µF or higher) are strongly recommend.

22 PCB layout and external component guidelines

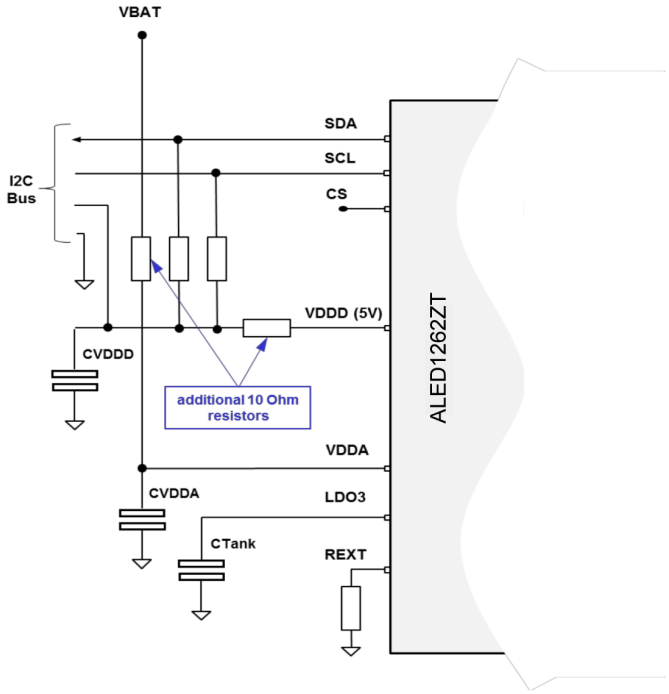
The aim of this paragraph is to provide some recommendations about the design of the application PCB designing. Routing general rules are always valid, however there are some other considerations tailored for this device family focused to reduce as much as possible EMI effects and maintain good signal integrity.

22.1 Signal integrity and EMI radiated/conducted immunity

- The external programming resistor between R-EXT and GND should be connected as close as possible to the device.
- The I²C bus should move unitarily on the board and should be shielded.
- Try to widen the spacing among signal lines as much as routing restrictions allow. Try not to bring traces closer than three times the dielectric height; the distance between the centers of two adjacent traces should be at least four times the trace width.
- Design the transmission line so that the conductor is as close to the ground plane as possible. This technique couples the transmission line tightly to the ground plane and help decouple it from adjacent signals.
- All I²C signals should proceed to the same board direction by a data bus.
- Regarding I²C bus, vias should be avoided, all strips should be traced on a single layer, if it is possible a ground plane has to be provided close to this layer. If it is an inner layer, insert the strips sandwiched between two GND surfaces. Reduce as much as possible the length of connections from the main bus to the device chain (derived traces ≡ stubs). Keep traces as straight as possible (corners should be rounded). Avoid crossing among SCL/SDA strips and power supply lines or fault flag connections (V_{DDA}, V_{DDD} and FLG).
- Filter capacitors (1 µF) must be connected as close as possible to the device on pins: V_{DDA}, V_{DDD} and LDO3. In parallel to each filter capacitor, it's suggested to add 10 nF compensation for EMC/EMI improvement. The same additional capacitor (10 nF X7R) must be connected in parallel on FLG pull-down resistor.

On V_{DDA} line, a serial resistor of about 10 Ω can be also added to constitute an RC low-pass filter to improve the external conducted disturbance immunity. As electromagnetic very noisy environment, to avoid resonant effects on internal digital supply, causing the device internal electrical stress, it's suggested to add a 10 Ω resistor between the external filter capacitor and V_{DDD} pin. The following figure shows the placement of the 10 Ω supplementary resistors.

Figure 44. **Additional filter connection**



22.2 Radiated emission reduction (EMI)

- To decrease the electromagnetic noise during LED power-on/off, the driver output lines should follow the shortest path "V_{LED} power-rail/LED/driver". Besides, as the system stability, a capacitor should be connected on the LED power supply rail (2.2 µF) as near as possible to LED anodes (the inductive LED power supply rail component should be compensated by the added capacitor, while regarding to a wider PCB, more distributed capacitors have to be placed). Another filter capacitor must be added to each driver power supply pins (V_{DDD} and V_{DDA}) and on linear regulator output (LDO3), see the previous section
- GND connection must be enlarged as much as possible
- I²C connection strips from controller to LED driver have to be as short as possible, and a ground plane should be provided close to bus lines and layer, see the previous section

22.3 Device thermal management

- For a better power dissipation (to decrease the device working temperature) it is necessary for the package exposed pad to be soldered to the board
- To guarantee a better thermal performance at least a 4-layer (e.g. 2S2P) PCB should be used
- The copper area below the package thermal pad should be enlarged as much as possible also outside the package perimeter using internal and copper side layers and/or extending the copper area using the no-pin package sides
- A reasonable number of vias must connect the copper area below the package to all available PCB layers (e.g. 3x4 or 3x5 via array). Smaller and closely spaced vias is the best solution. The best implementation is represented by copper filled vias
- On each inner layer a copper area must be provided for dissipation (the wider the better, at least 4 times or more the package dimensions). A good condition is to have at least a power layer as an entire copper area (e.g. GND layer)
- Traces for pin connection must be enlarged as much as layout constrains allow
- Several devices in power dissipation conditions on the same board must be adequately spaced

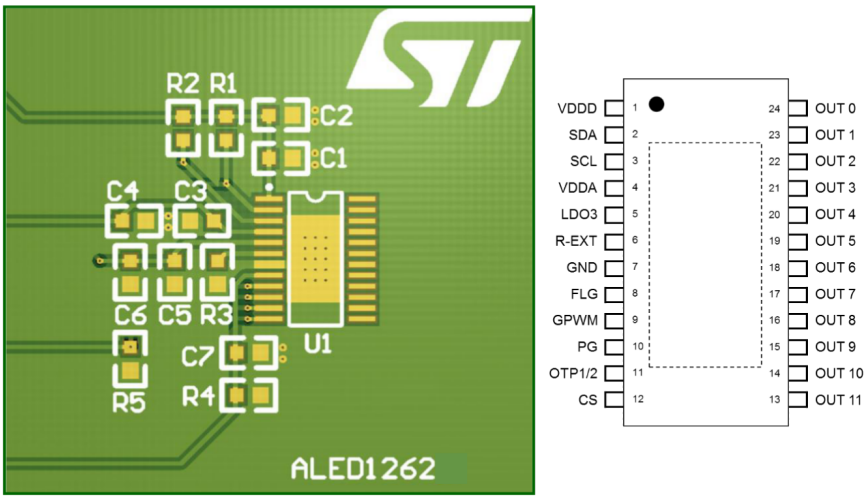
22.4 PCB layout example

On the image below a typical PCB layout is shown with main LED driver external components to be placed with higher priority (output channels to be connected). In this manner, the component position and strip routing length can be optimized. In this example, a two-layer PCB and 0603 component size are used:

- C1 and C2 are the V_{DDD} filter capacitors, very important for power supply noise reduction and internal regulator stability (C1 = 10 nF, C2 = 1 µF, X7R type)
- C3 and C4 are the V_{DDA} filter capacitors, very important for power supply noise reduction and internal regulator stability (C3=10 nF, C4=1 µF, X7R type)
- C5 and C6 are the LDO3 filter capacitors, very important for linear regulator stability (C5 = 10 nF, C6 = 1 µF, X7R type)
- C7 is the fault flag (FLG) filter capacitor, very useful for the device noise immunity (C7 = 10 nF, X7R type). R4 is the fault flag pull-down resistor
- R3 is the current programming resistor to be placed as close as possible to R-EXT pin and the device GND connection
- R2 and R1 are the I²C pull-up resistors
- R5 is the low-side resistor divider related to Power Good pin (PG)

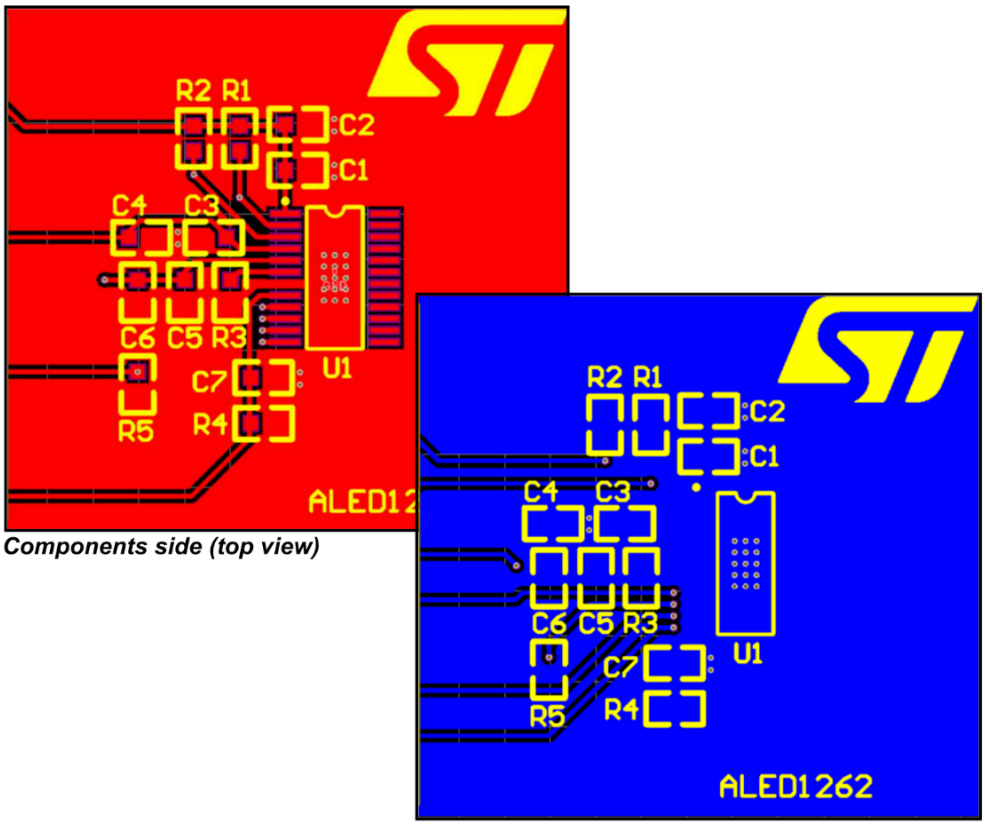
To be noticed vias near GND terminal for C1, C2, C3, C4 and C7 capacitors for a low ground impedance connection. I²C bus is mainly on a single layer, GND shielded and without crossing with the supply lines.

Figure 45. PCB routing example



As already mentioned, to improve external conducted disturbance immunity, a serial resistor can be added to analog power supply pin (V_{DDA}) before C3 and C4 to constitute a low-pass filter, and a serial resistor on digital power supply pin (V_{DDD}) after C1 and C2 to avoid internal resonant effects (EMI conducted immunity section). These resistors are not placed on the following PCB example.

Figure 46. **PCB routing example (components and copper side)**



Components side (top view)

Copper side (from components side)

23 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

23.1 HTSSOP24 exposed pad package information

Figure 47. HTSSOP24 exposed pad package outline

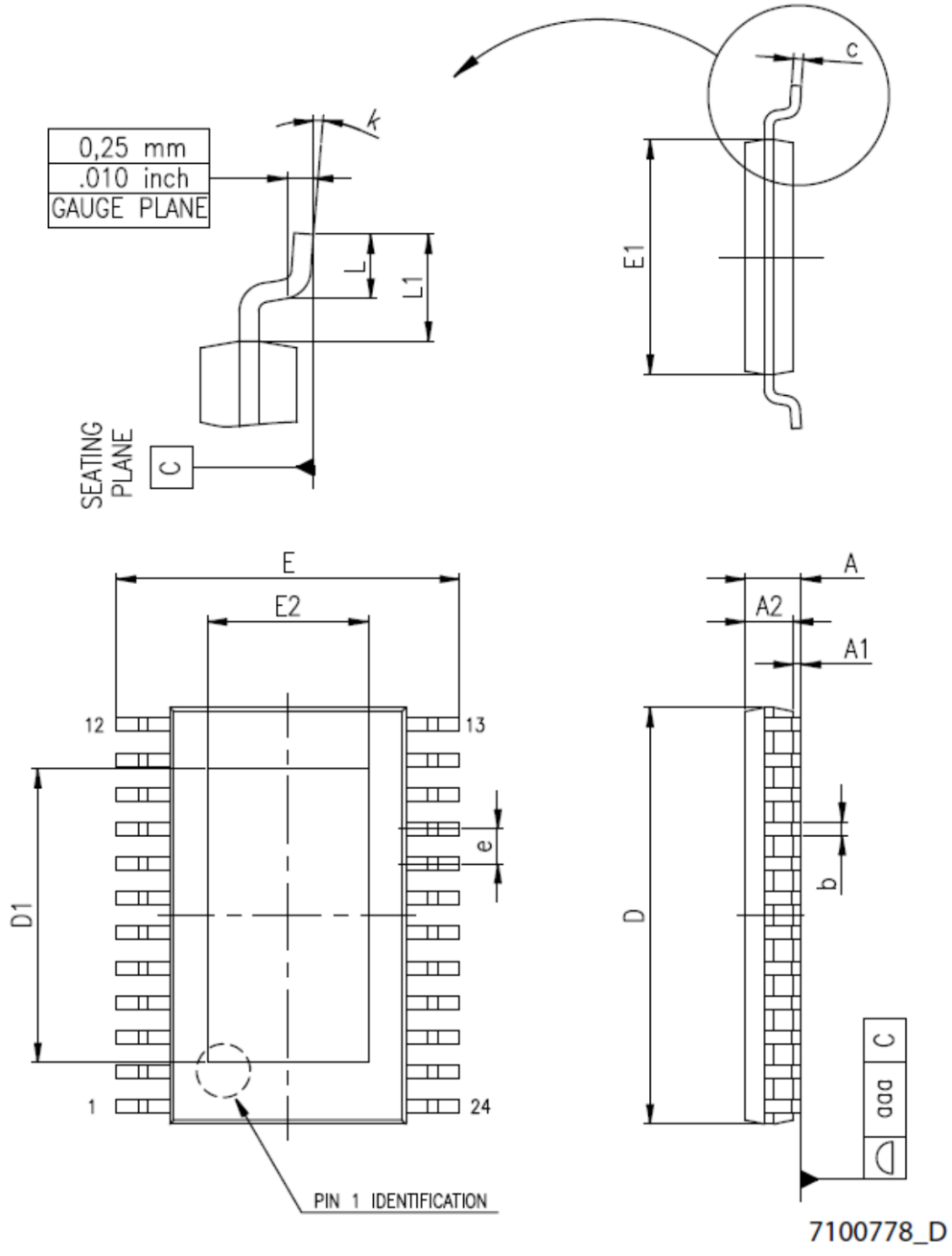
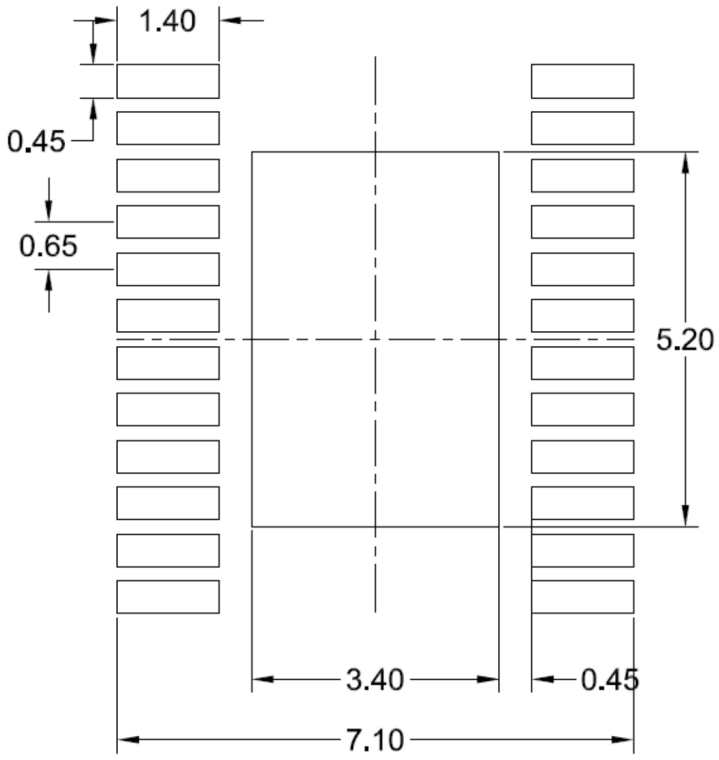


Table 30. **HTSSOP24 exposed pad mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	4.80	5.00	5.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00	3.20	3.40
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
K	0		8
aaa			0.10

Figure 48. **HTSSOP24 exposed pad recommended footprint**



Revision history

Table 31. **Document revision history**

Date	Revision	Changes
29-Jun-2018	1	First release
05-Nov-2018	2	Added: - Note in Figure 9. Device local dimming function logic - Note in Table 14. BDM_conf_1 field descriptions - Note in Table 19. PWM_gain_x field descriptions - Section 17.4.1 Enable_CH registers - Section 17.4.5 BDM_conf, status, Faulty_ch, PWM_gain_x registers Updated: - Footnote in Table 13. Embedded register list and direct address table - Table 25. Enable_CH[x] register content - Table 29. Command representation and description - Section 17.1 Available commands - Section 19.1.6 Device full status read back Minor text changes.
28-Jan-2019	3	Removed: ID_FR_BDM command in Table 29. Command representation and description and Section Enable_CH registers.
25-Feb-2019	4	Updated: Figure 4. FLG pin connection.

Contents

List of tables

List of figures