

TrenchP™
Power MOSFET

IXTY48P05T
IXTA48P05T
IXTP48P05T

$V_{DSS} = -50V$
 $I_{D25} = -48A$
 $R_{DS(on)} \leq 30m\Omega$

P-Channel Enhancement Mode
Avalanche Rated



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	- 50	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	- 50	V
V_{GSS}	Continuous	± 15	V
V_{GSM}	Transient	± 25	V
I_{D25}	$T_C = 25^\circ C$	- 48	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	-150	A
I_A	$T_C = 25^\circ C$	- 48	A
E_{AS}	$T_C = 25^\circ C$	300	mJ
P_D	$T_C = 25^\circ C$	150	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Torque (TO-220)	1.13 / 10	Nm/lb.in
Weight	TO-252	0.35	g
	TO-263	2.50	g
	TO-220	3.00	g

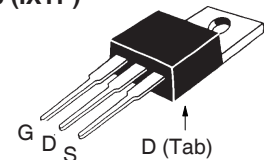
TO-252 (IXTY)



TO-263 (IXTA)



TO-220 (IXTP)



G = Gate D = Drain
S = Source Tab = Drain

Features

- International Standard Packages
- Avalanche Rated
- Extended FBSOA
- Fast Intrinsic Diode
- Low $R_{DS(ON)}$ and Q_g

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High-Side Switching
- Push Pull Amplifiers
- DC Choppers
- Automatic Test Equipment
- Current Regulators
- Battery Charger Applications

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = -250\mu A$	- 50		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	- 2.0		- 4.5 V
I_{GSS}	$V_{GS} = \pm 15V$, $V_{DS} = 0V$			± 50 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			- 10 μA
				- 250 μA
$R_{DS(on)}$	$V_{GS} = -10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			30 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = -10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	16	26	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = -25\text{V}$, $f = 1\text{MHz}$		3660	pF
C_{oss}			495	pF
C_{rss}			215	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = -10\text{V}$, $V_{DS} = -30\text{V}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 3\Omega$ (External)		20	ns
t_r			15	ns
$t_{d(off)}$			30	ns
t_f			13	ns
$Q_{g(on)}$	$V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		53	nC
Q_{gs}			16	nC
Q_{gd}			21	nC
R_{thJC}	TO-220			0.83 $^\circ\text{C/W}$
R_{thCS}			0.50	$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			-48 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			-192 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			-1.5 V
t_{rr}	$I_F = 0.5 \cdot I_{D25}$, $-di/dt = -100\text{A}/\mu\text{s}$ $V_R = -25\text{V}$, $V_{GS} = 0\text{V}$		30	ns
Q_{RM}			43.4	nC
I_{RM}			-2.8	A

Note 1: Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065B1	6,683,344	6,727,585	7,005,734B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123B1	6,534,343	6,710,405B2	6,759,692	7,063,975B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728B1	6,583,505	6,710,463	6,771,478B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

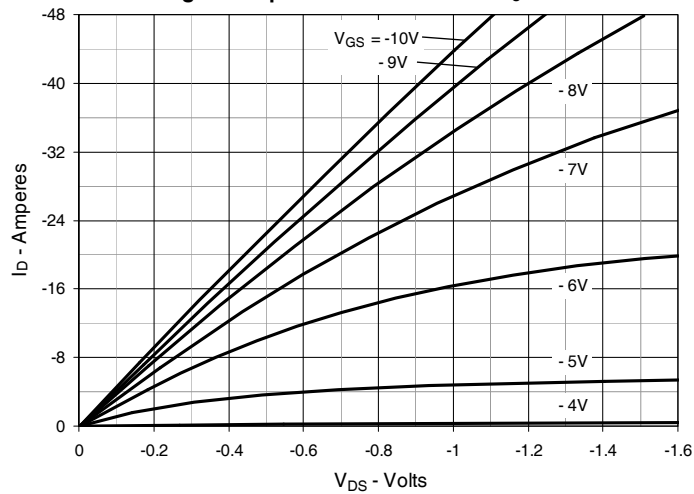


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

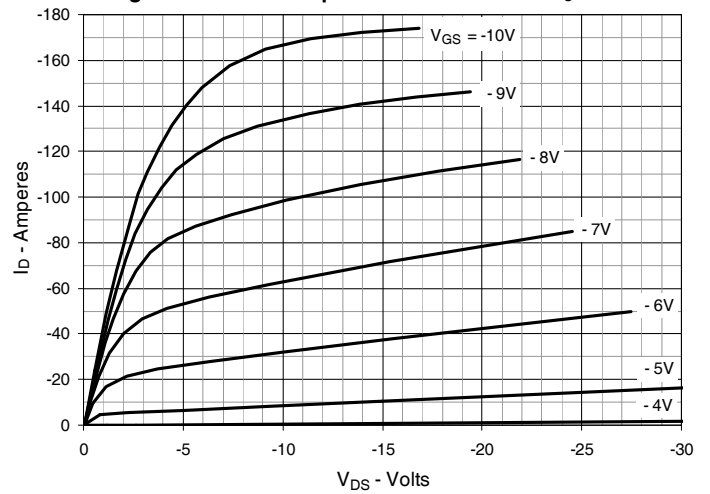


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

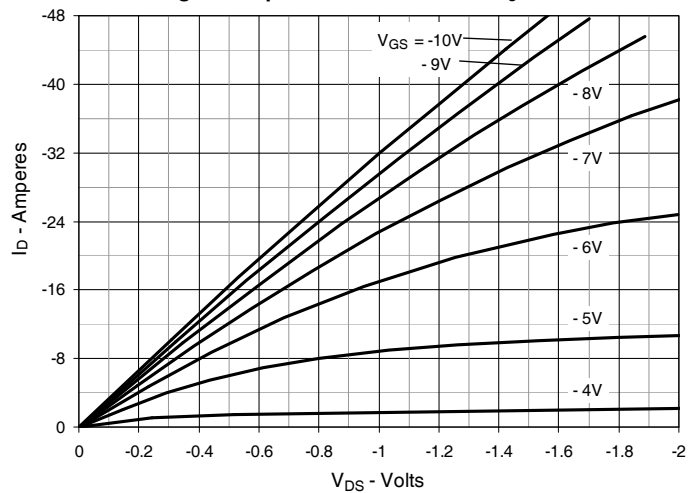


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = -24\text{A}$ Value vs. Junction Temperature

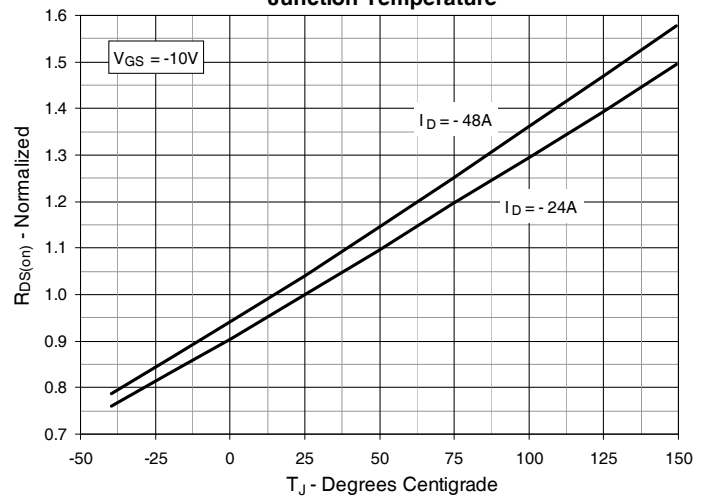


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = -24\text{A}$ Value vs. Drain Current

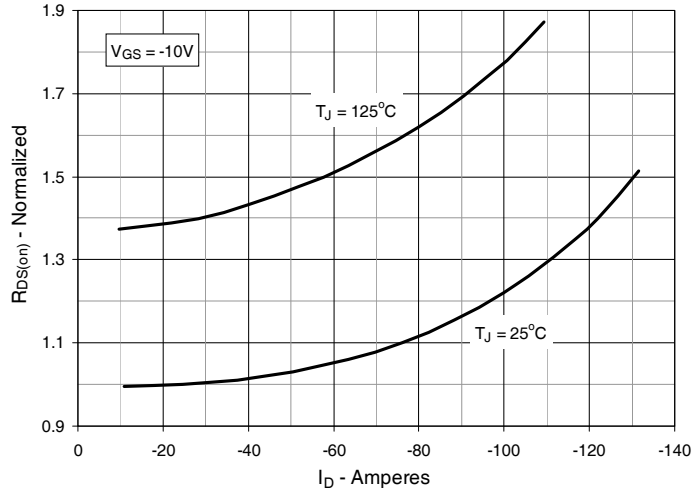


Fig. 6. Maximum Drain Current vs. Case Temperature

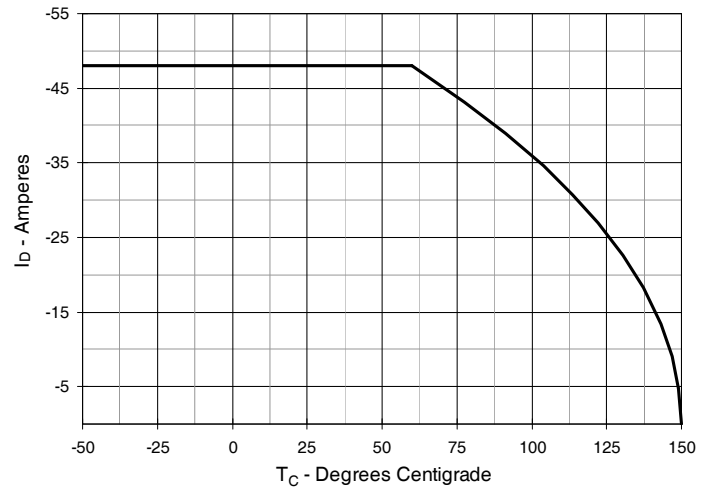


Fig. 7. Input Admittance

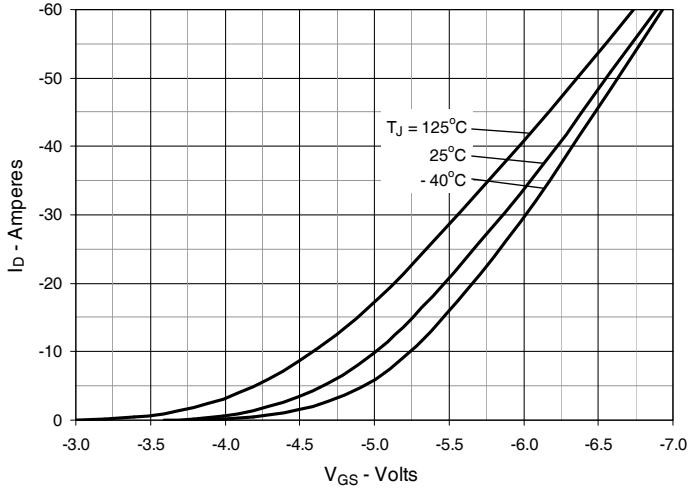


Fig. 8. Transconductance

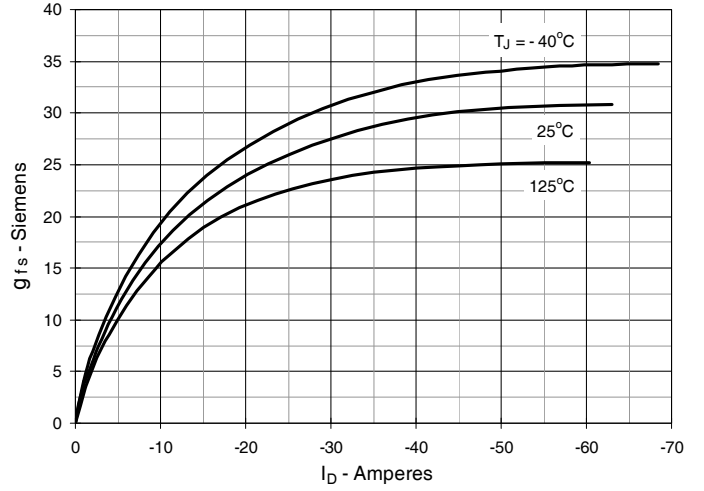


Fig. 9. Forward Voltage Drop of Intrinsic Diode

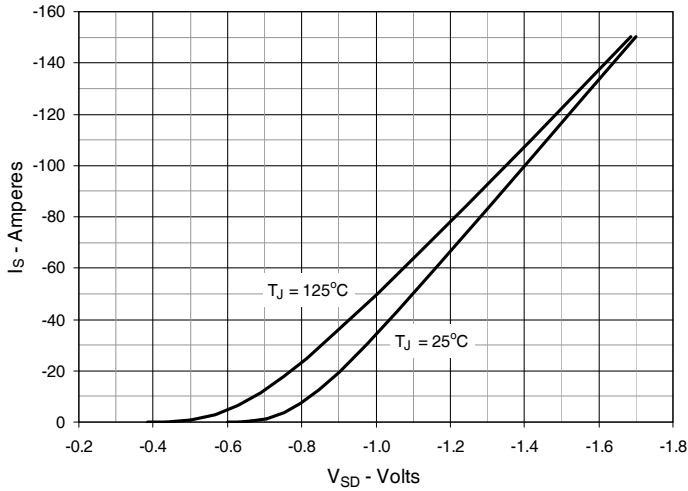


Fig. 10. Gate Charge

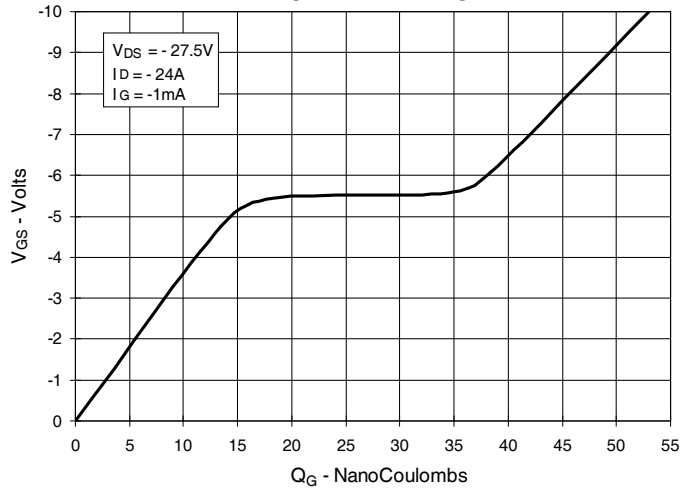


Fig. 11. Capacitance

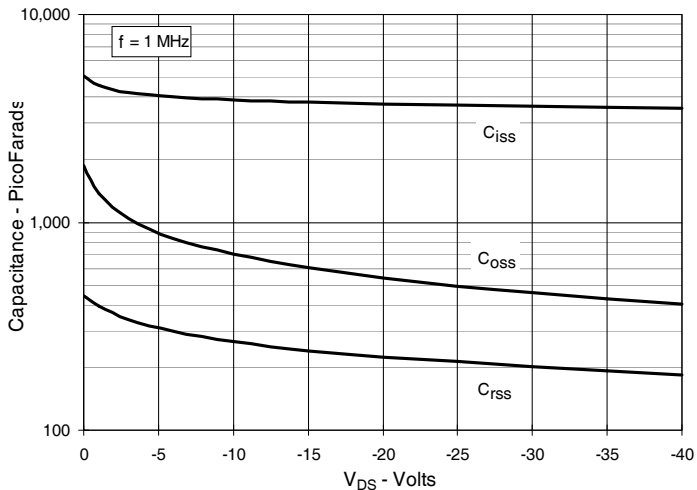


Fig. 12. Forward-Bias Safe Operating Area

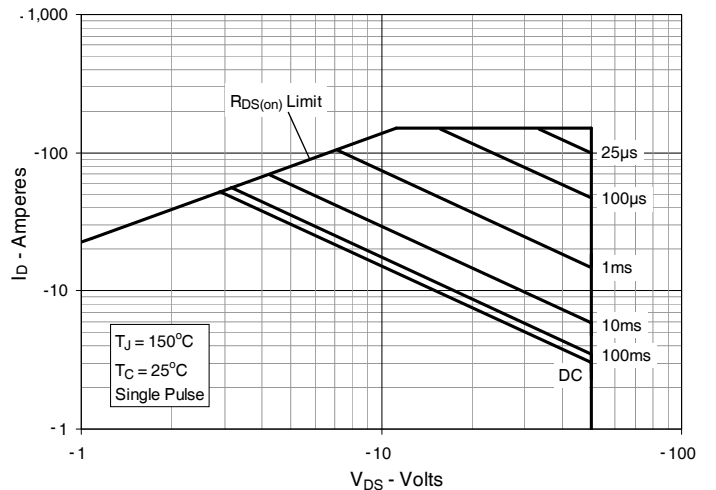


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

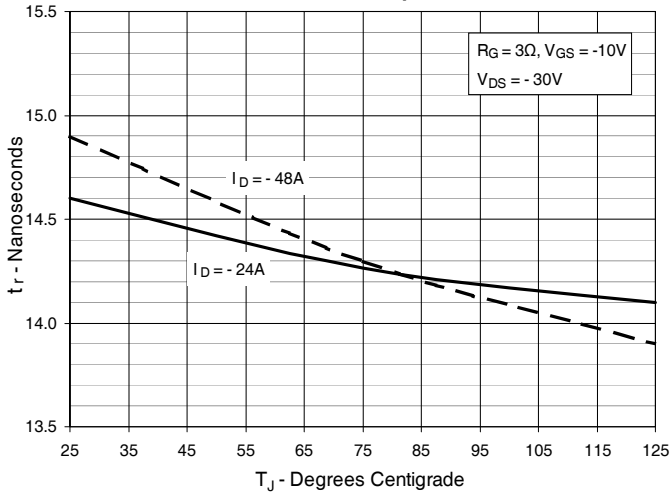


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

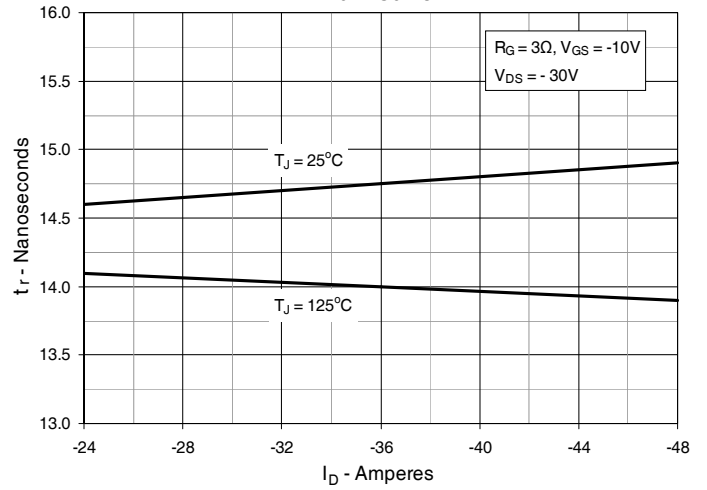


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

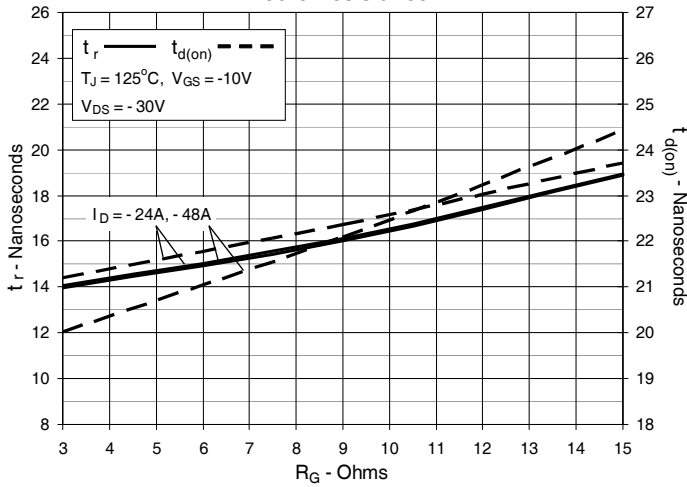


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

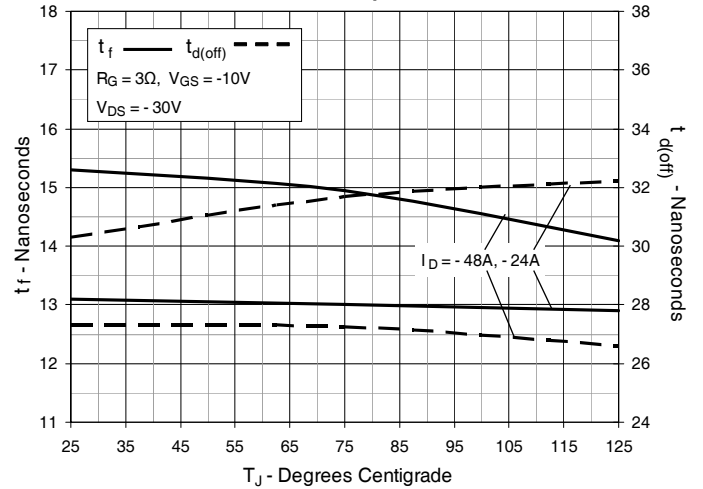


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

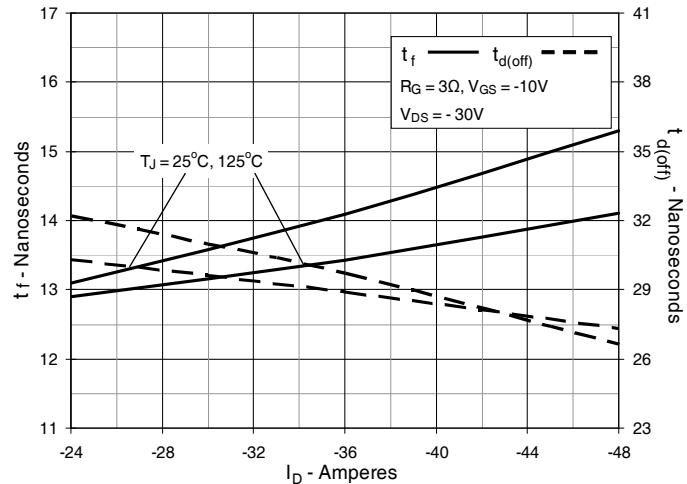


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

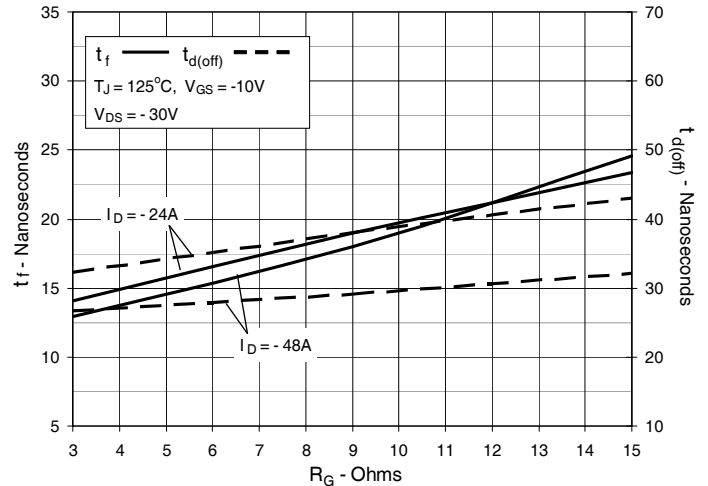
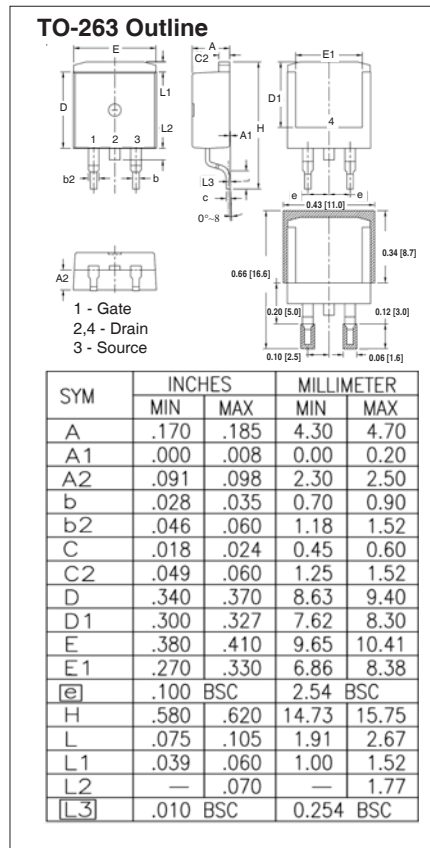
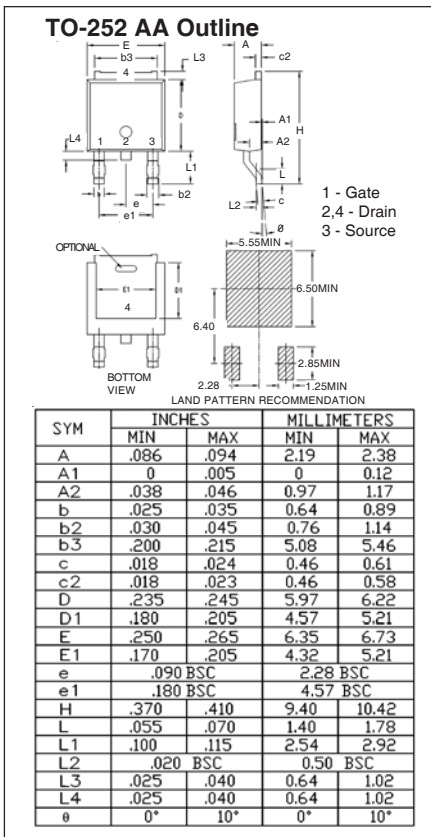
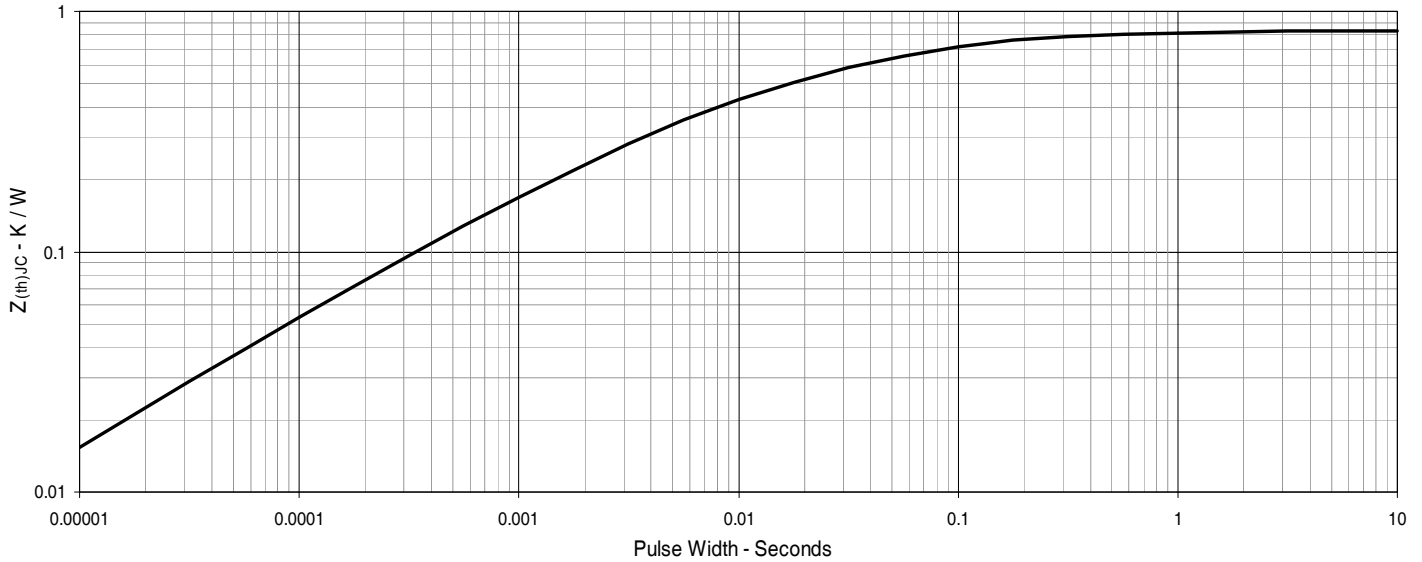


Fig. 19. Maximum Transient Thermal Impedance



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