

IFN410, IFN411, IFN412

N-Channel Matched Dual Silicon Junction Field-Effect Transistor

- Improved Replacements for the U410, U411, & U412
- Low Noise Differential Amplifier
- Differential Amplifier
- Wide-Band Amplifier

Absolute maximum ratings at $T_A = 25^\circ\text{C}$

Reverse Gate Source & Gate Drain Voltage	-40V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	375 mW
Power Derating	3.0 mW/ $^\circ\text{C}$
Operating Temperature Range	-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Storage Temperature Range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$

At 25 $^\circ\text{C}$ free air temperature Static Electrical Characteristics

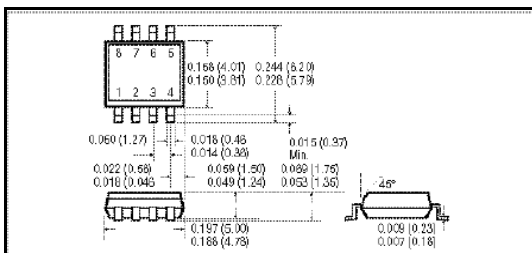
		410, 411, 412			Unit	Process NJ16	
		Min	Typ	Max		Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	-40			V	$I_G = -1\mu\text{A}, V_{DS} = 0\text{ V}$	
Gate Reverse Current	I_{GSS}			-0.2	nA	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	-0.5		-3.5	V	$V_{DS} = 20\text{ V}, I_D = 1\text{ nA}$	
Gate Source Voltage	V_{GS}	-0.2		-3	V	$V_{DS} = 20\text{ V}, I_D = 200\mu\text{A}$	
Drain Saturation Current (pulsed)	I_{DSS}	0.5		5	mA	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	
Gate Current	I_G			-200	pA	$V_{DS} = 10\text{ V}, I_D = 200\mu\text{A}$	

Dynamic Electrical Characteristics

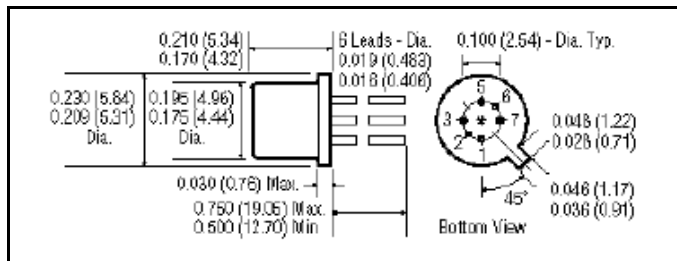
Common-Source Forward Transconductance	g_{fs}	1 0.6		4 1.2	mS	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 20\text{ V}, I_D = 200\mu\text{A}$	f = 1 kHz
Common-Source Output Conductance	g_{os}			20 5	μS	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 20\text{ V}, I_D = 200\mu\text{A}$	f = 1 kHz
Common-Source Input Capacitance	C_{iss}			4.5	pF	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	f = 1 MHz
Common-Source Reverse Transfer Capacitance	C_{rss}			1.2	pF	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\sim e_N$			50	nV/ $\sqrt{\text{Hz}}$	$V_{DS} = 20\text{ V}, I_D = 200\mu\text{A}$	f = 100 Hz

Matching Characteristics

		410	411	412	Units	Test Conditions
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	10	20	40	mV	$V_{DG} = 20\text{ V}, I_D = -200\mu\text{A}$
Differential Gate Source Voltage with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	10	25	80	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 20\text{ V}, I_D = 200\mu\text{A}$ 25 $^\circ\text{C}$ to 85 $^\circ\text{C}$
Common Mode Rejection Rate	CMRR (typ)	80	80	70	dB	$V_{DD} = 10\text{ V}$ to $V_{DD} = 20\text{ V}$ $I_D = 200\mu\text{A}$



SOIC-8 Package Pin Configuration
 SMPU410, SMPU411, SMPU412
 1-G1, 2-D1, 3-S1, 4-G2,
 5-G2, 6-D2, 7-S2, 8-G1



TO-71: Pin Configuration
 IFN410, IFN 411, IFN 412,

Pin Configuration
 1-S1, 2-D1, 3-G1,
 4-S2, 5-D2, 6-G2

Dimensions in Inches (mm)



715 N. Glenville Dr., Ste. 400
 Richardson, TX 75081
 (972) 238-9700 Fax (972) 238-5338
www.interfet.com