3.0 V to 5.5 V, ±12 kV IEC ESD Protected, 500 kbps/50 Mbps RS-485 Transceivers

Data Sheet **ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E**

FEATURES

- TIA/EIA RS-485 compliant over full supply range
- 3.0 V to 5.5 V operating voltage range on V_{CC}
- 1.62 V to 5.5 V V_{IO} logic supply option available
- ESD protection on the bus pins
  - IEC 61000-4-2 ±12 kV contact discharge
  - IEC 61000-4-2 ≥ ±12 kV air discharge
  - HBM: ≥ ±30 kV
- Full hot swap support (glitch free power-up/power-down)
- High speed 50 Mbps data rate (ADM3065E/ADM3066E/ ADM3067E/ADM3068E)
- Low speed 500 kbps data rate for long cables (ADM3061E/ ADM3062E/ADM3063E)
- Full receiver short-circuit, open circuit, and bus idle fail-safe
- Extended temperature range up to 125°C
- PROFIBUS compliant at V_{CC} ≥ 4.5 V
- Half duplex and full duplex models available
- Allows connection of up to 128 transceivers onto the bus
- Space-saving package options
  - 10-lead, 3 mm × 3 mm LFCSP
  - 8-lead and 10-lead, 3 mm × 3 mm MSOP
  - 8-lead and 14-lead, narrow body SOIC

APPLICATIONS

- Industrial fieldbuses
- Process control
- Building automation
- PROFIBUS networks
- Motor control servo drives and encoders

FUNCTIONAL BLOCK DIAGRAMS

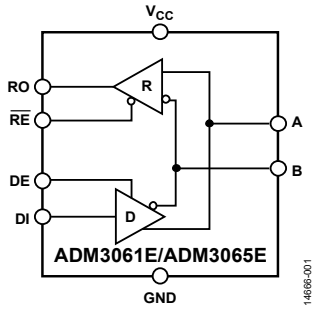

Figure 1. ADM3061E/ADM3065E Functional Block Diagram

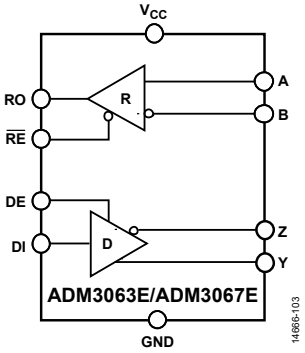

Figure 2. ADM3063E/ADM3067E Functional Block Diagram

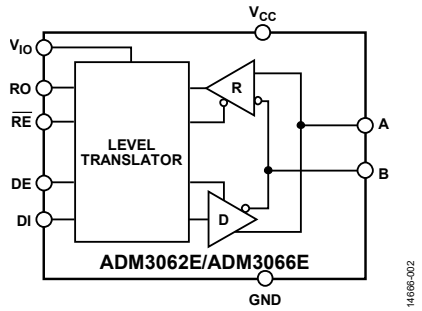

Figure 3. ADM3062E/ADM3066E Functional Block Diagram

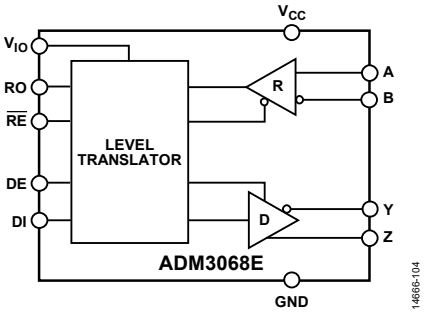

Figure 4. ADM3068E Functional Block Diagram

Rev. F

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6/2019—Rev. E to Rev. F

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3/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E are 3.0 V to 5.5 V, IEC electrostatic discharge (ESD) protected RS-485 transceivers, allowing the devices to withstand ±12 kV contact discharges on the transceiver bus pins without latch-up or damage. The ADM3062E/ADM3066E/ADM3068E feature a V_{IO} logic supply pin that allow a flexible digital interface capable of operating as low as 1.62 V.

The ADM3065E/ADM3066E/ADM3067E/ADM3068E are suitable for high speed, 50 Mbps, bidirectional data communication on multipoint bus transmission lines. The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E feature a 1/4 unit load input impedance that allows up to 128 transceivers on a bus. The ADM3061E/ADM3062E/ADM3063E models offer all of the same features as the ADM3065E/ADM3066E/ADM3067E/ADM3068E models at a low 500 kbps data rate that is suitable for operation over long cable runs.

The ADM3061E/ADM3062E/ADM3065E/ADM3066E are half-duplex RS-485 transceivers, fully compliant to the PROFIBUS® standard with increased 2.1 V bus differential voltage at $V_{CC} \geq$ 4.5 V. The ADM3063E/ADM3067E/ADM3068E are full duplex RS-485 transceiver options.

The RS-485 transceivers are available in a number of space-saving packages, such as the 10-lead, 3 mm × 3 mm lead frame chip-scale package (LFCSP), the 8-lead or 10-lead, 3 mm × 3 mm mini small outline package (MSOP), and the 8-lead or 14-lead, narrow body standard small outline packages (SOIC_N). Models with operating temperature ranges of −40°C to +125°C and −40°C to +85°C are available.

Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. If a significant temperature increase is detected in the internal driver circuitry during fault conditions, this feature forces the driver output into a high impedance state.

The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E guarantee a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled.

Table 1 presents an overview of the ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E data rate capability across temperature, power supply, and package options. Refer to the Ordering Guide for model numbering.

Table 1. Summary of the ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E Operating Conditions—Data Rate Capability Across Temperature, Power Supply, and Package

Maximum Data Rate[1]	Maximum V_{CC} (V)	Maximum Temperature	Package Description
50 Mbps	5.5	−40°C to +125°C	10-lead LFCSP
50 Mbps	5.5	−40°C to +105°C	8-lead SOIC_N, 8-lead MSOP, 10-lead MSOP, and 14-lead SOIC_N
50 Mbps	3.6	−40°C to +125°C	8-lead SOIC_N, 8-lead MSOP, 10-lead MSOP, and 14-lead SOIC_N
500 kbps	5.5	−40°C to +125°C	8-lead SOIC_N, 8-lead MSOP, 10-lead MSOP, 10-lead LFCSP, and 14-lead SOIC_N

[1] The ADM3065E/ADM3066E/ADM3067E/ADM3068E data input (DI) is transmitting 50 Mbps (or 500 kbps for the ADM3061E/ADM3062E/ADM3063E) clock data, and the ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E driver enable (DE) is enabled for 50% of the DI transmit time

SPECIFICATIONS

V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC} (ADM3062E/ADM3066E/ADM3068E), T_A = T_{MIN} (−40°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, V_{IO} = V_{CC} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
No Load Supply Current	I_{CC}		3.5	7.5	mA	DE = V_{IO}[1], $\overline{RE}$ = 0 V
			3.5	7.5	mA	DE = V_{IO}, $\overline{RE}$ = V_{IO}
			3	4.5	mA	DE = 0 V, $\overline{RE}$ = 0 V
ADM3065E/ADM3066E/ADM3067E/ ADM3068E Supply Current, Data Rate = 50 Mbps	I_{CC}		107	172	mA	Load resistance (R_L) = 54 Ω, DE = V_{IO}, $\overline{RE}$ = 0 V (V_{CC} ≥ 4.5 V)
			67	75	mA	R_L = 54 Ω, DE = V_{IO}, $\overline{RE}$ = 0 V (V_{CC} = 3.0 V)
ADM3061E/ADM3062E/ADM3063E Supply Current, Data Rate = 500 kbps	I_{CC}		100	165	mA	R_L = 54 Ω, DE = V_{IO}, $\overline{RE}$ = 0 V (V_{CC} ≥ 4.5 V)
			56	74	mA	R_L = 54 Ω, DE = V_{IO}, $\overline{RE}$ = 0 V (V_{CC} = 3.0 V)
Supply Current in Shutdown Mode	I_{SHDN}		210	450	µA	DE = 0 V, $\overline{RE}$ = V_{IO}
V_{IO} Shutdown Current[2]	I_{IOSHDN}		1	50	µA	DE = 0 V, $\overline{RE}$ = V_{IO}
DRIVER						
Differential Outputs						
Output Voltage, Loaded	$\lvert V_{OD2}\rvert$	2.0	2.5	V_{CC}	V	V_{CC} ≥ 3.0 V, R_L = 50 Ω, see Figure 38
	$\lvert V_{OD2}\rvert$	1.5	2.1	V_{CC}	V	V_{CC} ≥ 3.0 V, R_L = 27 Ω (RS-485), see Figure 38
	$\lvert V_{OD2}\rvert$	2.1	3.5	V_{CC}	V	V_{CC} ≥ 4.5 V, R_L = 50 Ω, see Figure 38
	$\lvert V_{OD2}\rvert$	2.1	3	V_{CC}	V	V_{CC} ≥ 4.5 V, R_L = 27 Ω (RS-485), see Figure 38
	$\lvert V_{OD3}\rvert$	1.5	2.1	V_{CC}	V	V_{CC} ≥ 3.0 V, −7 V ≤ common-mode voltage (V_{CM}) ≤ +12 V, see Figure 39
	$\lvert V_{OD3}\rvert$	2.1	3	V_{CC}	V	V_{CC} ≥ 4.5 V, −7 V ≤ V_{CM} ≤ +12 V, see Figure 39
Change in Differential Input Voltage for Complementary Output States	$\Delta\lvert V_{OD}\rvert$			0.2	V	R_L = 27 Ω or 50 Ω, see Figure 38
Common-Mode Output Voltage	V_{OC}		1.6	3.0	V	R_L = 27 Ω or 50 Ω, see Figure 38
Change in Common Mode Voltage for Complementary Output States	$\Delta\lvert V_{OC}\rvert$			0.2	V	R_L = 27 Ω or 50 Ω, see Figure 38
Output Short-Circuit Current	I_{OS}	−250		+250	mA	−7 V < output voltage (V_{OUT}) < +12 V
ADM3063E/ADM3067E Output Leakage (Y, Z)	I_O			+100	µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, input voltage (V_{IN}) = 12 V
		−100			µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = −7 V
Logic Inputs (DE, $\overline{RE}$, DI)						
Input Voltage						
Low	V_{IL}			0.33 × V_{IO}	V	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V
High	V_{IH}	0.67 × V_{IO}			V	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V
Input Current	I_I	−2		+2	µA	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−200	−125	−30	mV	−7 V < V_{CM} < +12 V
Input Voltage Hysteresis	V_{HYS}		30		mV	−7 V < V_{CM} < +12 V
Input Current (A, B)	I_I		0.1	0.25	mA	DE = 0 V, V_{CC} = powered/unpowered, V_{IN} = 12 V
		−0.20	−0.1		mA	DE = 0 V, V_{CC} = powered/unpowered, V_{IN} = −7 V
Line Input Resistance	R_{IN}	48	96		kΩ	−7 V ≤ V_{CM} ≤ +12 V
Logic Outputs						
Output Voltage						
Low	V_{OL}			0.4	V	V_{IO} = 3.6 V, output current (I_{OUT}) = 2 mA, V_{ID}[3] ≤ −0.2 V
				0.4	V	V_{IO} = 2.7 V, I_{OUT} = 1 mA, V_{ID} ≤ −0.2 V[2]
				0.2	V	V_{IO} = 1.95 V, I_{OUT} = +500 µA, V_{ID} ≤ −0.2 V[2]
High	V_{OH}	2.4			V	V_{IO} = 3.0 V, I_{OUT} = −2 mA, V_{ID} ≥ −0.03 V
		2.0			V	V_{IO} = 2.3 V, I_{OUT} = −1 mA, V_{ID} ≥ −0.03 V[2]
		V_{IO} − 0.2			V	V_{IO} = 1.65 V, I_{OUT} = −500 µA, V_{ID} ≥ −0.03 V[2]
Short-Circuit Current				85	mA	V_{OUT} = GND or V_{IO}
Three-State Output Leakage	I_{OZR}			±2	µA	RO pin = 0 V or V_{IO}

[1] V_{IO} = V_{CC} for ADM3061E/ADM3063E/ADM3065E/ADM3067E.
[2] ADM3062E/ADM3066E/ADM3068E only.
[3] V_{ID} is the receiver input differential voltage.

TIMING SPECIFICATIONS

ADM3061E/ADM3062E/ADM3063E

V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC} (ADM3062E), $T_A = T_{MIN}$ (−40°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, $V_{IO} = V_{CC}$ = 3.3 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate[1]		500			kbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		220	800	ns	R_{LDIFF} capacitor = 54 Ω, C_{L1} capacitor = C_{L2} capacitor = 100 pF, see Figure 5 and Figure 40
Skew	t_{DSKEW}		5	100	ns	R_{LDIFF} = 54 Ω, $C_{L1} = C_{L2}$ = 100 pF, see Figure 5 and Figure 40
Rise/Fall Times	t_{DR}, t_{DF}	120	300	800	ns	R_{LDIFF} = 54 Ω, $C_{L1} = C_{L2}$ = 100 pF, see Figure 5 and Figure 40
Enable to Output High	t_{DZH}		100	1000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Enable to Output Low	t_{DZL}		100	1000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Disable Time from Low	t_{DLZ}		350	2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Disable Time from High	t_{DHZ}		600	2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Enable Time from Shutdown to High	$t_{DZH(SHDN)}$[2]		550	2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Enable Time from Shutdown to Low	$t_{DZL(SHDN)}$[2]		550	2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
RECEIVER						
Maximum Data Rate		500			kbps	
Propagation Delay	t_{RPLH}, t_{RPHL}			200	ns	C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, V_{CM} = 1.5 V, see Figure 7 and Figure 42
Skew/Pulse Width Distortion	t_{RSKEW}			50	ns	C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, V_{CM} = 1.5 V, see Figure 7 and Figure 42
Enable to Output High	t_{RZH}		10	50	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, DE high, see Figure 8 and Figure 44
Enable to Output Low	t_{RZL}		10	50	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, DE high, see Figure 8 and Figure 44
Disable Time from Low	t_{RLZ}		10	50	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, see Figure 8 and Figure 44
Disable Time from High	t_{RHZ}		10	50	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, see Figure 8 and Figure 44
Enable from Shutdown to High	$t_{RZH(SHDN)}$[3]			2000	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, see Figure 8 and Figure 43
Enable from Shutdown to Low	$t_{RZL(SHDN)}$[3]			2000	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, see Figure 8 and Figure 43
TIME TO SHUTDOWN	t_{SHDN}[4]	40			ns	

[1] Maximum data rate assumes a ratio of t_{DR}:t_{BIT}:t_{DF} equal to 1:0.5:1.
[2] $t_{DZH(SHDN)}$ and $t_{DZL(SHDN)}$ refer to the time for the device to enable when DE changes from 0 V to V_{CC}. $\overline{RE} = V_{CC}$ for this condition.
[3] $t_{RZH(SHDN)}$ and $t_{RZL(SHDN)}$ refer to the time for the device to enable when $\overline{RE}$ changes from V_{CC} to 0 V. DE = 0 V for this condition.
[4] Minimum time required to put the device into shutdown: DE and $\overline{RE}$ must be disabled for more than 40 ns for the device to go into shutdown.

ADM3065E/ADM3066E/ADM3067E/ADM3068E

V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC} (ADM3066E/ADM3068E), T_A = T_{MIN} (−40°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, V_{IO} = V_{CC} = 3.3 V, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate[1]		50			Mbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		9	15	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 40
Skew	t_{DSKEW}		1	2	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 40
Rise/Fall Times	t_{DR}, t_{DF}		4	6.7	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 40
Enable to Output High	t_{DZH}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Enable to Output Low	t_{DZL}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Disable Time from Low	t_{DLZ}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Disable Time from High	t_{DHZ}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Enable Time from Shutdown to High	$t_{DZH(SHDN)}$[2]		550	2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
Enable Time from Shutdown to Low	$t_{DZL(SHDN)}$[2]		550	2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 6 and Figure 41
RECEIVER						
Maximum Data Rate		50			Mbps	
Propagation Delay	t_{RPLH}, t_{RPHL}		20	35	ns	C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, V_{CM} = 1.5 V, see Figure 7 and Figure 42
Skew/Pulse Width Distortion	t_{RSKEW}		1	3	ns	C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, V_{CM} = 1.5 V, see Figure 7 and Figure 42
Enable to Output High	t_{RZH}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, DE high, see Figure 8 and Figure 44
Enable to Output Low	t_{RZL}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, DE high, see Figure 8 and Figure 44
Disable Time from Low	t_{RLZ}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, see Figure 8 and Figure 44
Disable Time from High	t_{RHZ}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, see Figure 8 and Figure 44
Enable from Shutdown to High	$t_{RZH(SHDN)}$[3]		450	2000	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, see Figure 8 and Figure 43
Enable from Shutdown to Low	$t_{RZL(SHDN)}$[3]		450	2000	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\| \geq$ 1.5 V, see Figure 8 and Figure 43
TIME TO SHUTDOWN	t_{SHDN}[4]	40			ns	

[1] Maximum data rate assumes a ratio of t_{DR}:t_{BIT}:t_{DF} equal to 1:1:1.
[2] $t_{DZH(SHDN)}$ and $t_{DZL(SHDN)}$ refer to the time for the device to enable when $\overline{DE}$ changes from 0 V to V_{CC}. $\overline{RE}$ = V_{CC} for this condition.
[3] $t_{RZH(SHDN)}$ and $t_{RZL(SHDN)}$ refer to the time for the device to enable when $\overline{RE}$ changes from V_{CC} to 0 V. DE = 0 V for this condition.
[4] Minimum time required to put the device into shutdown: DE and $\overline{RE}$ must be disabled for more than 40 ns for the device to go into shutdown.

Timing Diagrams

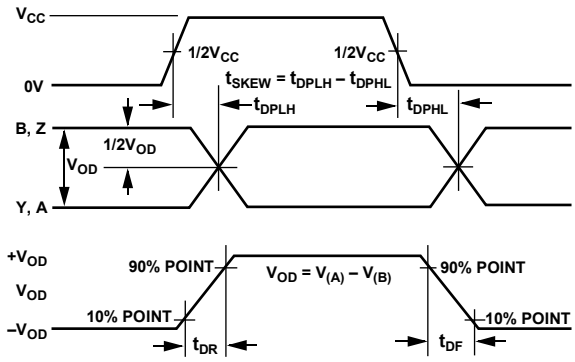


Figure 5. Driver Propagation Delay Rise and Fall Timing Diagram

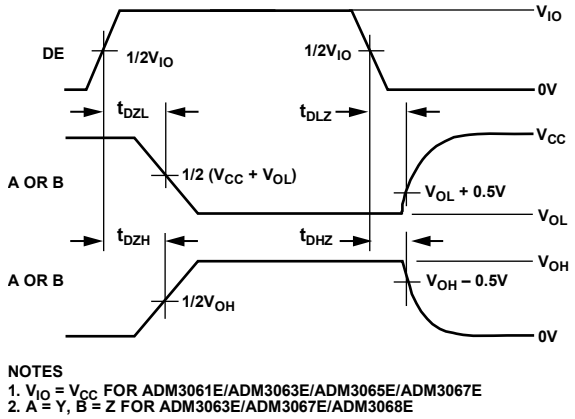


Figure 6. Driver Enable and Disable Timing Diagram

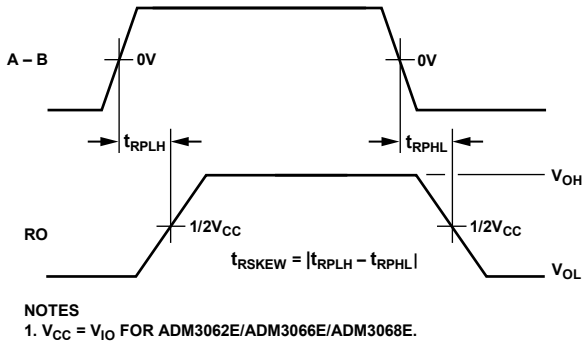


Figure 7. Receiver Propagation Delay Timing Diagram

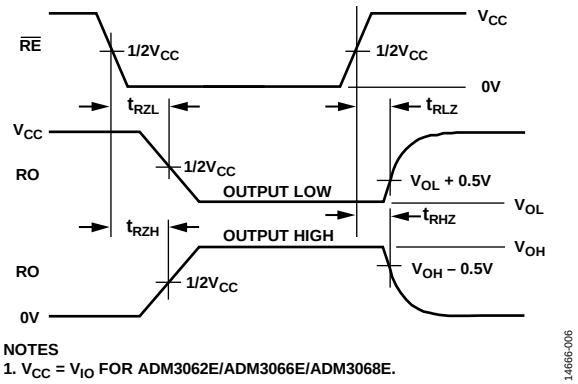


Figure 8. Receiver Enable and Disable Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{CC} to GND	6 V
V_{IO} to GND	−0.3 V to +6 V
Digital Input and Output Voltage (DE, $\overline{RE}$, DI, and RO)	−0.3 V to V_{IO}[1] + 0.3 V
Driver Output and Receiver Input Voltage	−9 V to +14 V
Operating Temperature Ranges	−40°C to +85°C
	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Continuous Total Power Dissipation	
8-Lead SOIC_N	0.225 W
8-Lead MSOP	0.151 W
10-Lead MSOP	0.151 W
10-Lead LFCSP	0.450 W
14-Lead SOIC_N	0.239 W
Maximum Junction Temperature (T_J)	150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD on the Bus Pins (A, B, Y, Z)	
IEC 61000-4-2 Contact Discharge	±12 kV
IEC 61000-4-2 Air Discharge	
10 Positive and 10 Negative Discharges	±12 kV
Three Positive or Three Negative Discharges	±15 kV
ESD Human Body Model (HBM)	
On the Bus Pins (A, B, Y, Z)	≥±30 kV
All Other Pins	±8 kV

[1] V_{IO} = V_{CC} on the ADM3061E/ADM3063E/ADM3065E/ADM3067E.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
R-8	110.88	58.63	°C/W
RM-8	165.69	49.61	°C/W
RM-10	165.69	49.61	°C/W
R-14	104.5	42.90	°C/W
CP-10-9	55.65	33.22	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

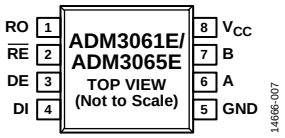


Figure 9. ADM3061E/ADM3065E 8-Lead Narrow Body SOIC_N Pin Configuration

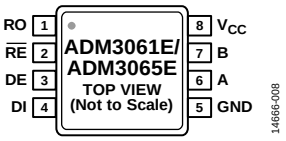


Figure 10. ADM3061E/ADM3065E 8-Lead MSOP Pin Configuration

Table 7. ADM3061E/ADM3065E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output Data. This output is high when (A − B) ≥ −30 mV and low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
2	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver and driving it high disables the receiver.
3	DE	Driver Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state.
4	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
5	GND	Ground.
6	A	Noninverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
7	B	Inverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
8	V_{CC}	3.0 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

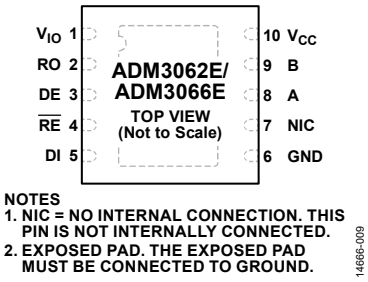


Figure 11. ADM3062E/ADM3066E 10-Lead LFCSP Pin Configuration

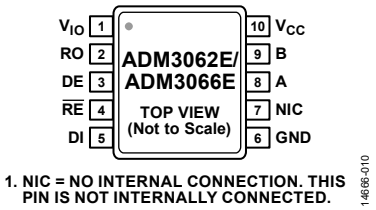


Figure 12. ADM3062E/ADM3066E 10-Lead MSOP Pin Configuration

Table 8. ADM3066E/ADM3062E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IO}	1.62 V to 5.5 V Logic Supply. Adding a 0.1 µF decoupling capacitor between the V_{IO} pin and the GND pin is recommended.
2	RO	Receiver Output Data. This output is high when (A − B) ≥ −30 mV and is low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
3	DE	Driver Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state.
4	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
5	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
6	GND	Ground.
7	NIC	No Internal Connection. This pin is not internally connected.
8	A	Noninverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
9	B	Inverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
10	V_{CC}	3.0 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.
	EPAD	Exposed Pad. The exposed pad must be connected to ground.

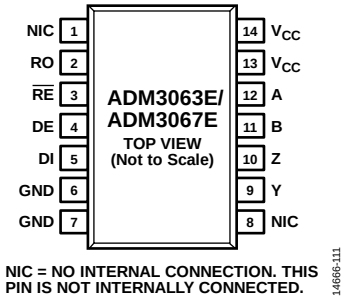


Figure 13. ADM3063E/ADM3067E 14-Lead SOIC Pin Configuration

Table 9. ADM3063E/ADM3067E Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	NIC	No Internal Connection. This pin is not internally connected.
2	RO	Receiver Output Data. This output is high when (A − B) ≥ −30 mV and is low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
3	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver and driving it high disables the receiver.
4	DE	Driver Enable. A high level on this pin enables the driver differential outputs, Y and Z. A low level places the driver output into a high impedance state.
5	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
6, 7	GND	Ground.
9	Y	Driver Noninverting Output. When the driver is disabled, or when V_{CC} is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
10	Z	Driver Inverting Output. When the driver is disabled, or when V_{CC} is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
11	B	Inverting Receiver Input.
12	A	Noninverting Receiver Input.
13, 14	V_{CC}	3.0 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

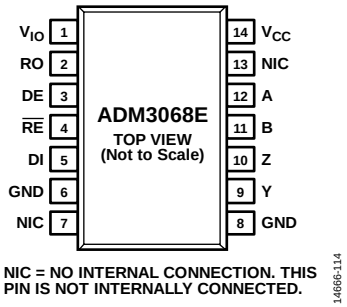


Figure 14. ADM3068E 14-Lead SOIC Pin Configuration

Table 10. ADM3068E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IO}	1.62 V to 5.5 V Logic Supply. Adding a 0.1 µF decoupling capacitor between the V_{IO} pin and the GND pin is recommended.
2	RO	Receiver Output Data. This output is high when (A − B) ≥ −30 mV and is low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
3	DE	Driver Enable. A high level on this pin enables the driver differential outputs, Y and Z. A low level places the driver output into a high impedance state.
4	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver and driving it high disables the receiver.
5	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
6, 8	GND	Ground.
7, 13	NIC	No Internal Connection. This pin is not internally connected.
9	Y	Driver Noninverting Output. When the driver is disabled, or when V_{CC} is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
10	Z	Driver Inverting Output. When the driver is disabled, or when V_{CC} is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
11	B	Inverting Receiver Input.
12	A	Noninverting Receiver Input.
14	V_{CC}	3.0 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

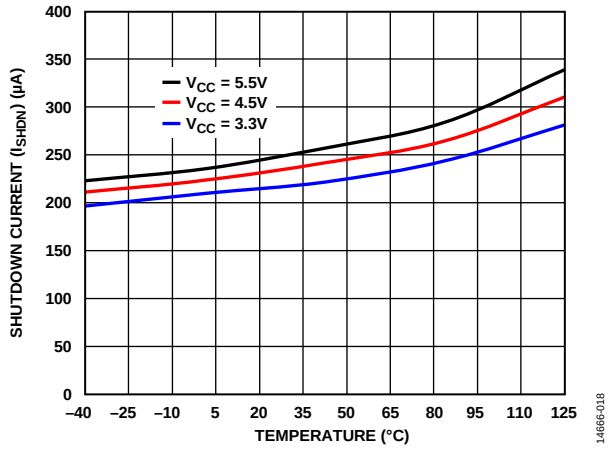


Figure 15. Shutdown Current (I_{SHDN}) vs. Temperature

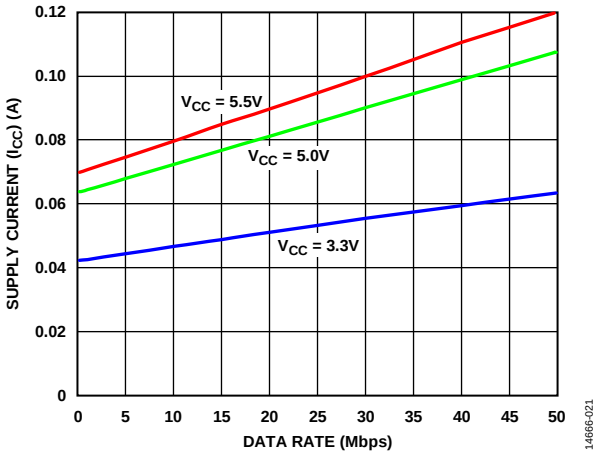


Figure 18. Supply Current (I_{CC}) vs. Data Rate with 54 Ω Load Resistance, 50 Mbps Models

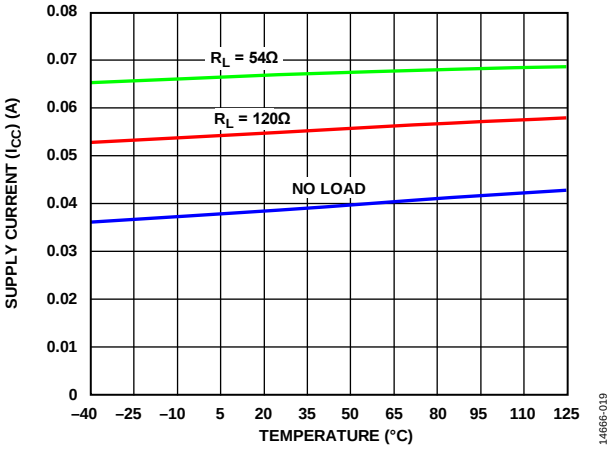


Figure 16. Supply Current (I_{CC}) vs. Temperature, Data Rate = 50 Mbps, 50 Mbps Models, V_{CC} = 3.3 V

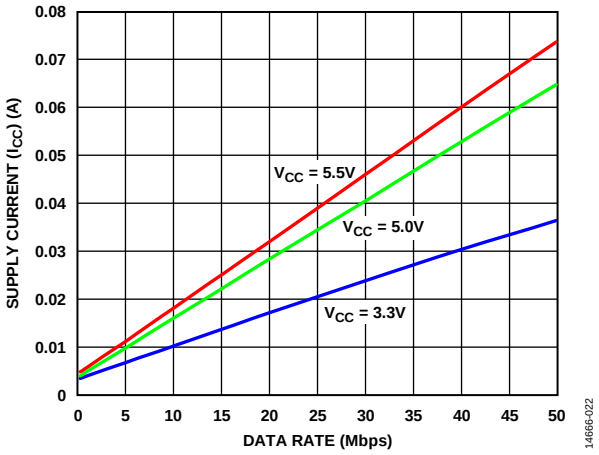


Figure 19. Supply Current (I_{CC}) vs. Data Rate with No Load Resistance, 50 Mbps Models

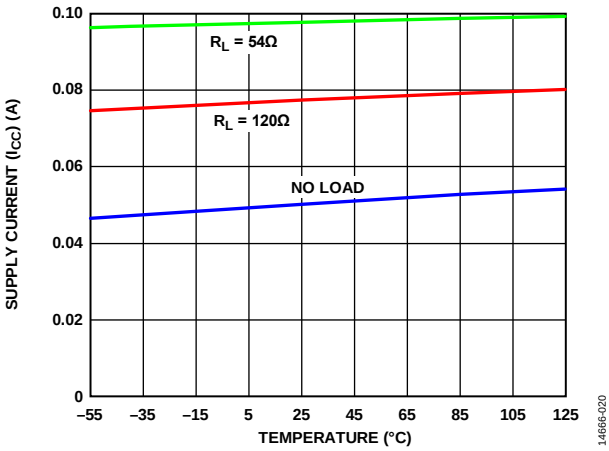


Figure 17. Supply Current (I_{CC}) vs. Temperature, Data Rate = 50 Mbps, 50 Mbps Models, V_{CC} = 5.0 V

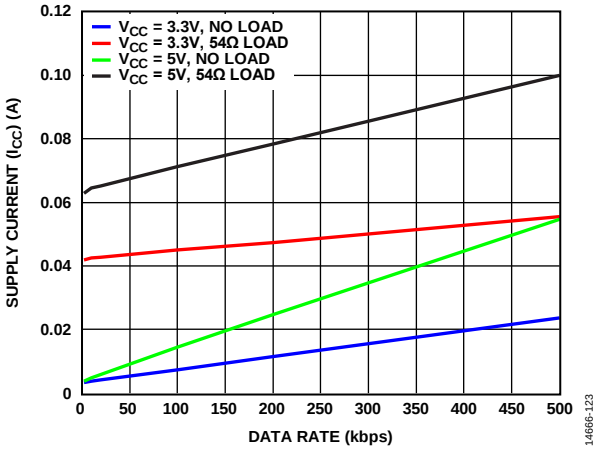


Figure 20. Supply Current (I_{CC}) vs. Data Rate with 54 Ω Load Resistance and No Load Resistance, 500 kbps Models

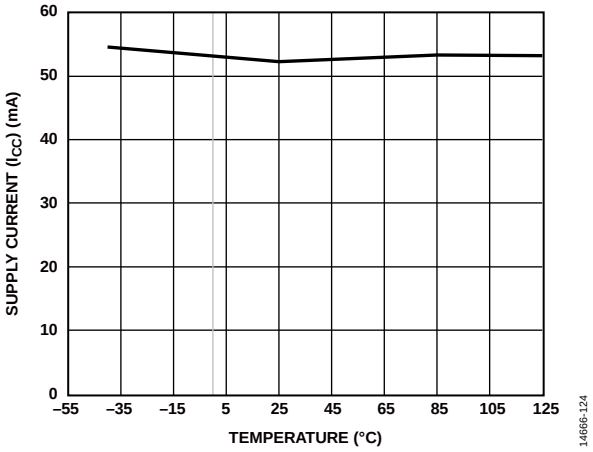


Figure 21. Supply Current (I_{CC}) vs. Temperature, Data Rate = 500 kbps, 500 kbps Models, V_{CC} = 3.0 V

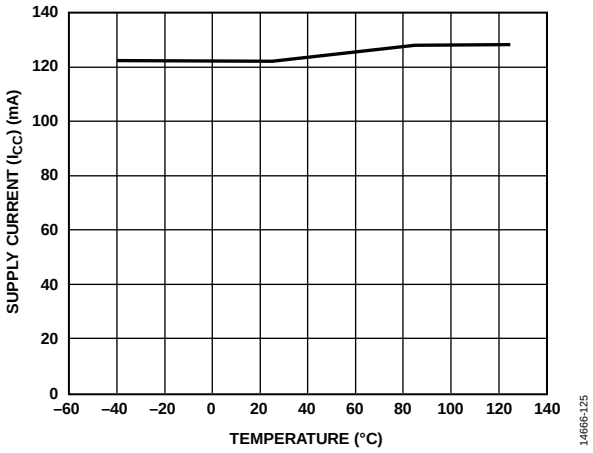


Figure 22. Supply Current (I_{CC}) vs. Temperature, Data Rate = 500 kbps, 500 kbps Models, V_{CC} = 5.5 V

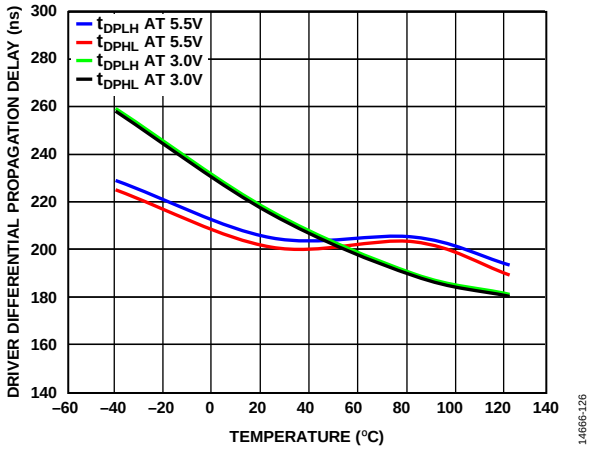


Figure 23. Driver Differential Propagation Delay vs. Temperature, 500 kbps Models

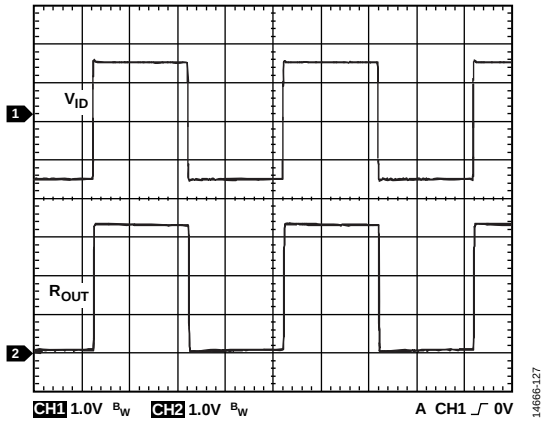


Figure 24. Receiver Propagation Delay (Oscilloscope Plot), Data Rate = 500 kbps, V_{ID} ≥ 1.5 V

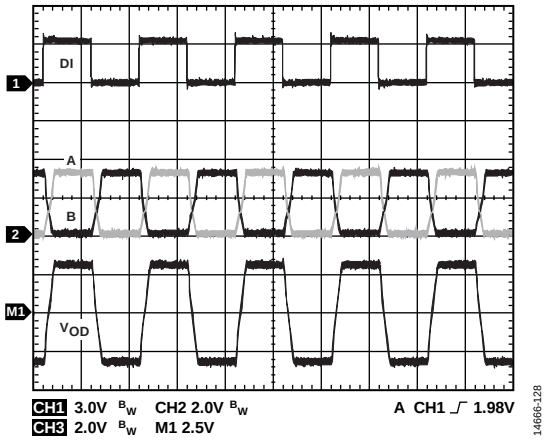


Figure 25. Driver Propagation Delay (Oscilloscope Plot), Data Rate = 500 kbps, 500 kbps Models

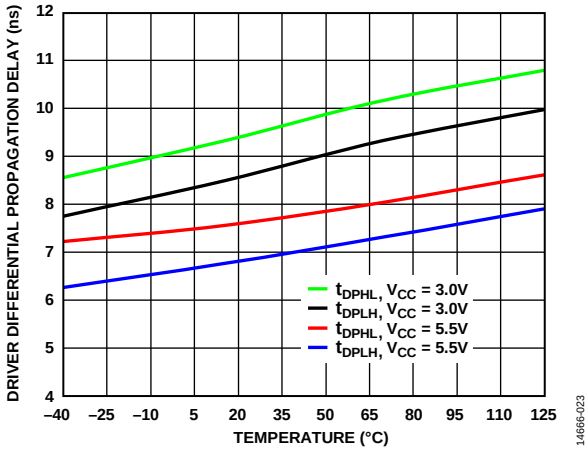


Figure 26. Driver Differential Propagation Delay vs. Temperature, 50 Mbps Models

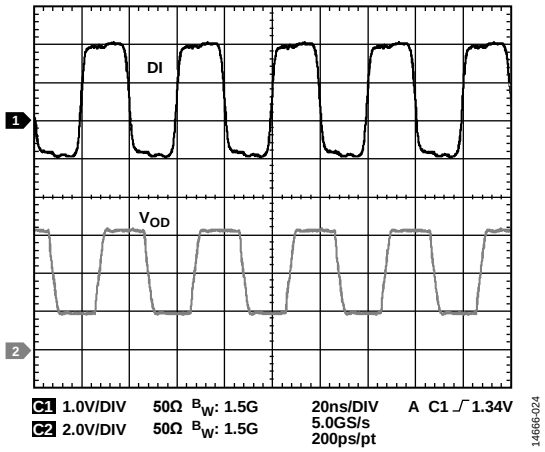


Figure 27. Driver Propagation Delay (Oscilloscope Plot), Data Rate = 50 Mbps, 50 Mbps models

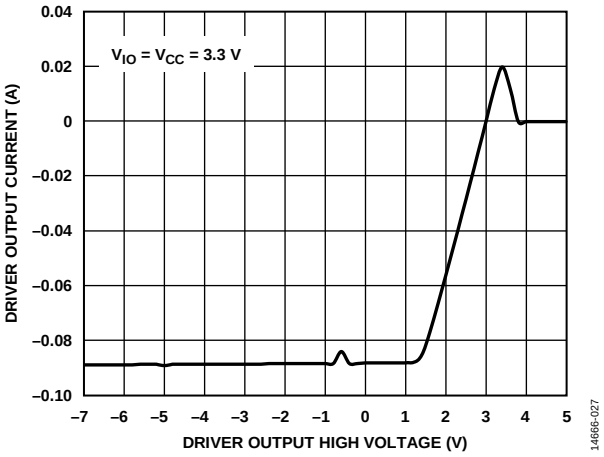


Figure 30. Driver Output Current vs. Driver Output High Voltage

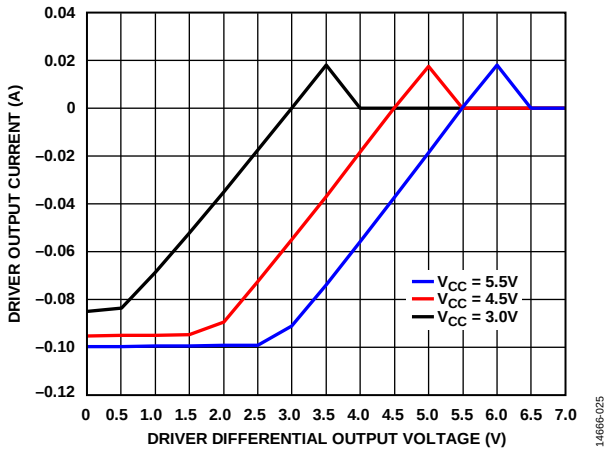


Figure 28. Driver Output Current vs. Driver Differential Output Voltage

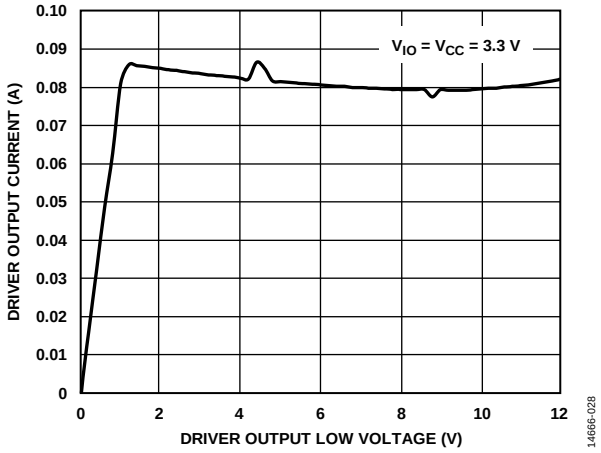


Figure 31. Driver Output Current vs. Driver Output Low Voltage

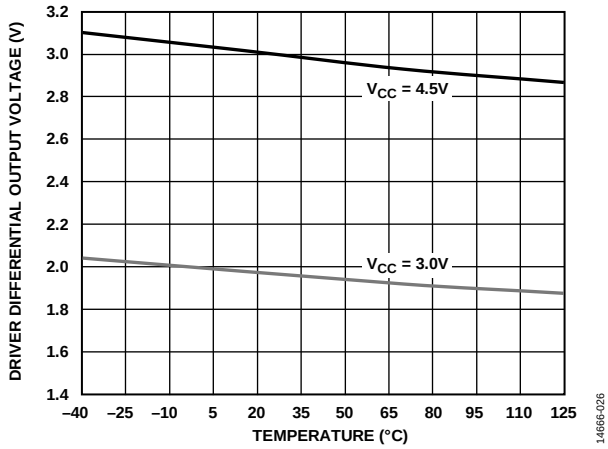


Figure 29. Driver Differential Output Voltage vs. Temperature

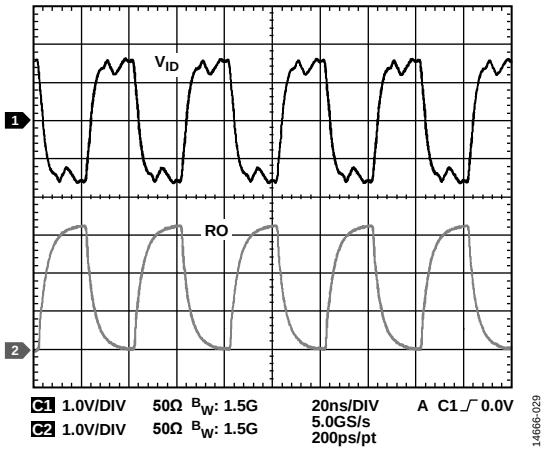


Figure 32. Receiver Propagation Delay at 50 Mbps, $|V_{ID}| \geq 1.5$ V

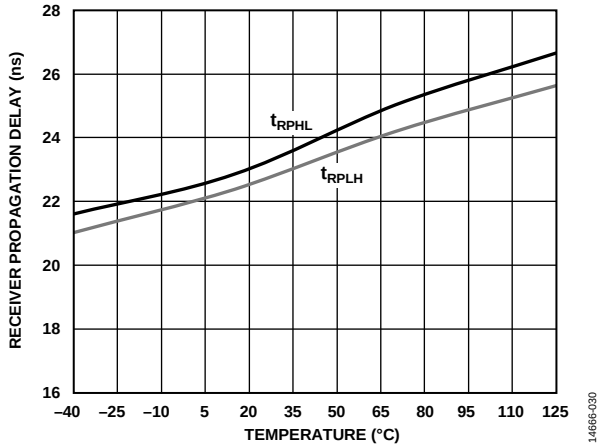


Figure 33. Receiver Propagation Delay vs. Temperature, 50 Mbps

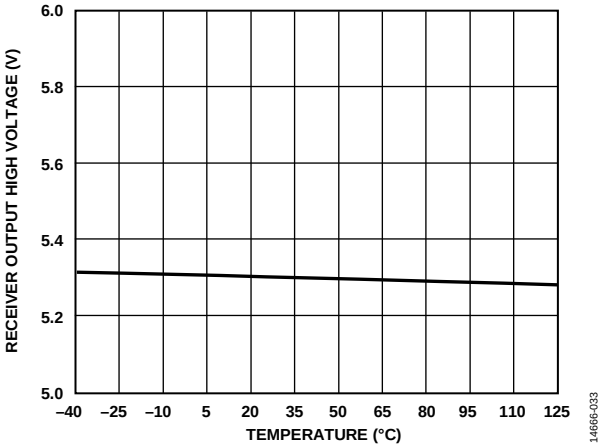


Figure 36. Receiver Output High Voltage vs. Temperature

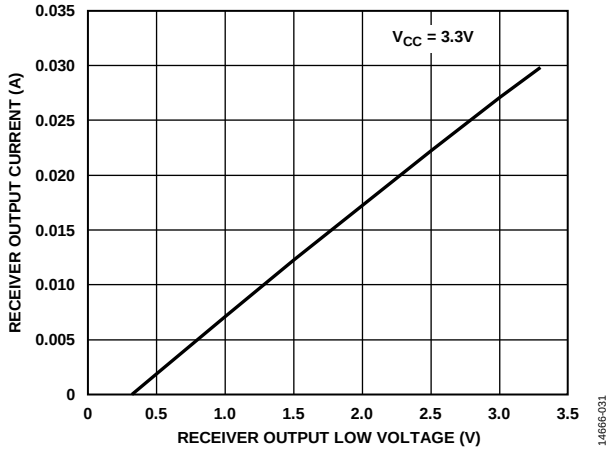


Figure 34. Receiver Output Current vs. Receiver Output Low Voltage (V_{CC} = 3.3 V)

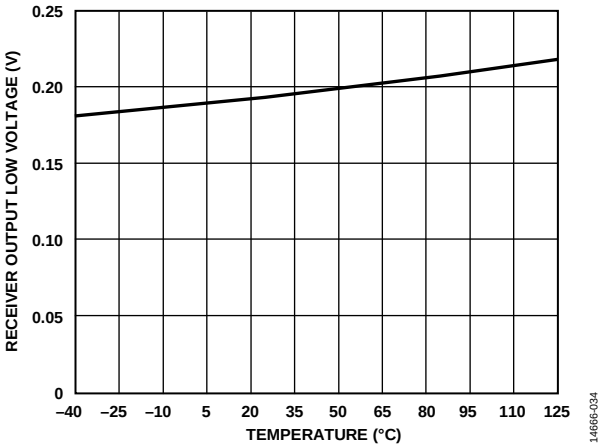


Figure 37. Receiver Output Low Voltage vs. Temperature

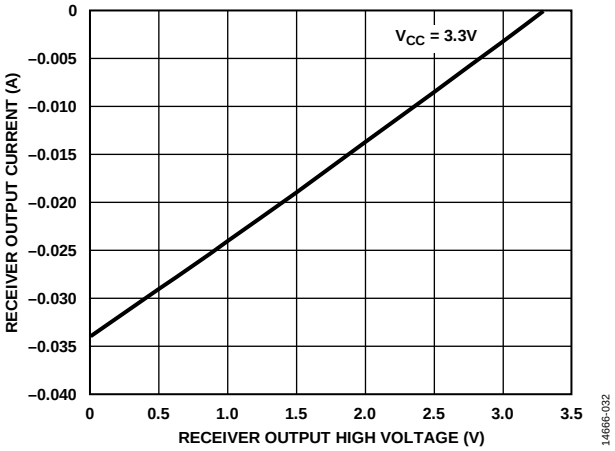


Figure 35. Receiver Output Current vs. Receiver Output High Voltage (V_{CC} = 3.3 V)

TEST CIRCUITS

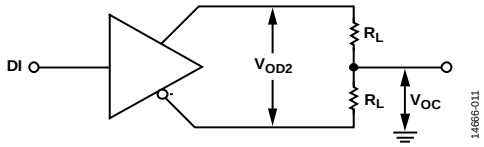


Figure 38. Driver Voltage Measurements

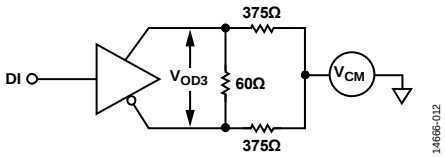


Figure 39. Driver Voltage Measurements over Common-Mode Range

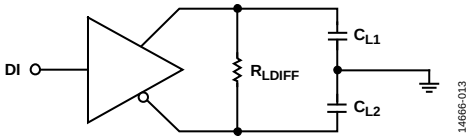


Figure 40. Driver Propagation Delay

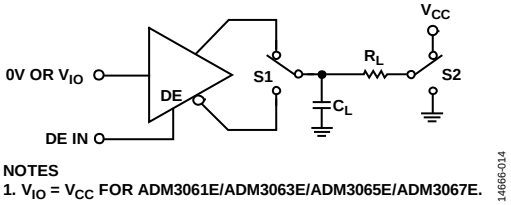


Figure 41. Driver Enable/Disable

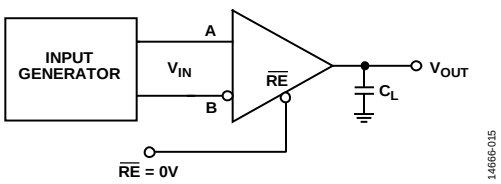


Figure 42. Receiver Propagation Delay/Skew

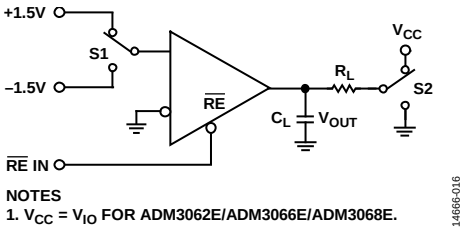


Figure 43. Receiver Enable/Disable from Shutdown

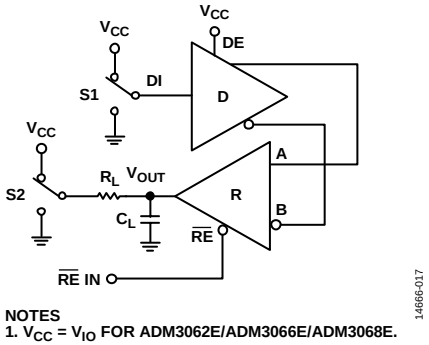


Figure 44. Receiver Enable/Disable

THEORY OF OPERATION

IEC ESD PROTECTED RS-485

The ADM3065E/ADM3066E/ADM3067E/ADM3068E are 3.0 V to 5.5 V, 50 Mbps RS-485 transceivers with IEC 61000-4-2 Level 4 ESD protection on the bus pins. The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E can withstand up to ±12 kV contact discharge on transceiver bus pins (A, B, Y, and Z) without latch-up or damage. The ADM3061E/ADM3062E/ADM3063E has the same robust IEC 61000-4-2 ESD protection as the ADM3065E/ADM3066E/ADM3067E/ADM3068E models and operate at a lower, 500 kbps data rate.

HIGH DRIVER DIFFERENTIAL OUTPUT VOLTAGE

The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E have characteristics that are optimized for use in PROFIBUS applications. When powered at $V_{CC} \geq 4.5$ V, the ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E driver output differential voltage meets or exceeds the PROFIBUS requirements of 2.1 V with a 54 Ω load.

IEC 61000-4-2 ESD PROTECTION

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused either by near contact or induced by an electric field. It has the characteristics of high current in a short time period. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 describes testing using two coupling methods: contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT. A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the EUT. This method is a more accurate representation of an actual ESD event but is not as repeatable. Therefore, contact discharge is the preferred test method.

During testing, the data port is subjected to at least 10 positive and 10 negative single discharges. Selection of the test voltage is dependent on the system end environment.

Figure 45 shows the 8 kV contact discharge current waveform as described in the IEC 61000-4-2 specification. Some of the key waveform parameters are rise times of less than 1 ns and pulse widths of approximately 60 ns.

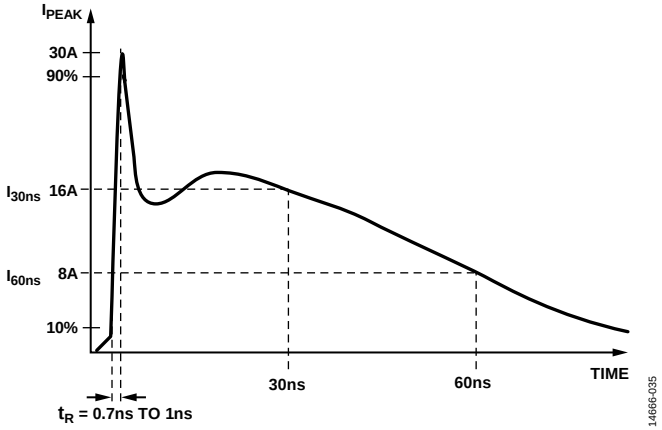


Figure 45. IEC 61000-4-2 ESD Waveform (8 kV)

Figure 46 shows the 8 kV contact discharge current waveform from the IEC 61000-4-2 standard compared to the HBM ESD 8 kV waveform. Figure 46 shows that the two standards specify a different waveform shape and peak current. The peak current associated with an IEC 61000-4-2 8 kV pulse is 30 A, whereas the corresponding peak current for HBM ESD is more than five times less, at 5.33 A. The other difference is the rise time of the initial voltage spike, with the IEC 61000-4-2 ESD waveform having a much faster rise time of 1 ns, compared to the 10 ns associated with the HBM ESD waveform. The amount of power associated with an IEC ESD waveform is much greater than that of an HBM ESD waveform. The HBM ESD standard requires the EUT to be subjected to three positive and three negative discharges, whereas the IEC ESD standard requires 10 positive and 10 negative discharge tests.

The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E with IEC 61000-4-2 ESD ratings is better suited for operation in harsh environments compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

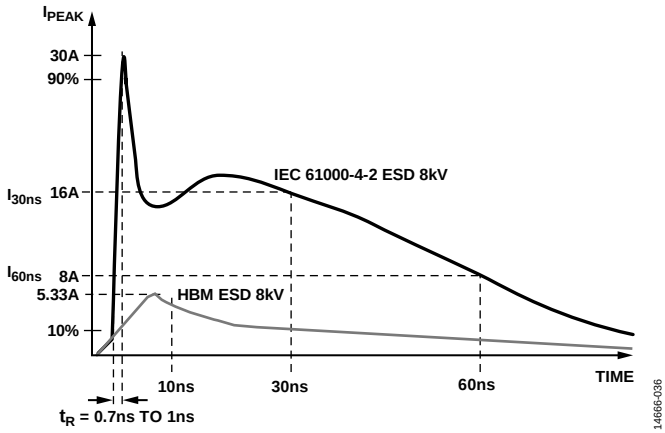


Figure 46. IEC 61000-4-2 ESD Waveform 8 kV Compared to HBM ESD Waveform 8 kV

TRUTH TABLES

Table 12 and Table 13 use the abbreviations shown in Table 11.

Table 11. Truth Table Abbreviations

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Any state
Z	High impedance (off)

Table 12. Transmitting Truth Table

Supply Status		Inputs			Outputs	
V_{IO}[1]	V_{CC}	$\overline{RE}$	DE	DI	A/Y	B/Z
On	On	X	H	H	H	L
On	On	X	H	L	L	H
On	On	X	L	X	Z	Z
Off	On	X	X	X	I	I
On	Off	X	X	X	Z	Z
Off	Off	X	X	X	Z	Z

[1] For the ADM3061E, ADM3063E, ADM3065E, and ADM3067E, the V_{IO} pin is not applicable.

Table 13. Receiving Truth Table

Supply Status		Inputs			Outputs
V_{IO}[1]	V_{CC}	A – B	$\overline{RE}$	DE	RO
On	On	>−0.03 V	L	X	H
On	On	<−0.2 V	L	X	L
On	On	−0.2 V ≤ A – B ≤ −0.03 V	L	X	I
On	On	Inputs open/shorted	L	X	H
On	On	X	H	X	Z
On	Off	X	L	X	I
On	Off	X	H	X	Z
Off	On	X	L	X	I
Off	Off	X	X	X	I

[1] For the ADM3061E, ADM3063E, ADM3065E, and ADM3067E, the V_{IO} pin is not applicable.

RECEIVER FAIL-SAFE

The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E guarantee a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled. This receiver output is achieved by setting the receiver input threshold between −30 mV and −200 mV. If the differential receiver input voltage (A − B) is greater than or equal to −30 mV, the RO pin is logic high.

If the (A − B) input is less than or equal to −200 mV, RO is logic low. In the case of a shorted, open circuit or terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0 V, resulting in a logic high with a 30 mV minimum noise margin.

HOT SWAP CAPABILITY

When a circuit board is inserted into a powered (or hot) backplane, differential disturbances to the data bus can lead to data errors. During this period, processor logic output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of the RS-485 transceivers to a defined logic level. Leakage currents up to ±10 µA from the high impedance state of the processor logic drivers can cause standard complementary metal-oxide semiconductor (CMOS) enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance can cause coupling of V_{CC} or GND to the enable inputs. Without the hot swap capability, these factors can improperly enable the driver or receiver of the transceiver. When V_{CC} or V_{IO} rises, an internal pull-down circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pull-down circuit becomes transparent, resetting the hot swap tolerable input.

128 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12 kΩ (one unit load), and the standard driver can drive up to 32 unit loads. The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E transceivers have a one fourth unit load receiver input impedance (48 kΩ), allowing up to 128 transceivers to be connected in parallel on one communication line. Any combination of these devices and other RS-485 transceivers with a total of 32 unit loads or fewer can be connected to the line.

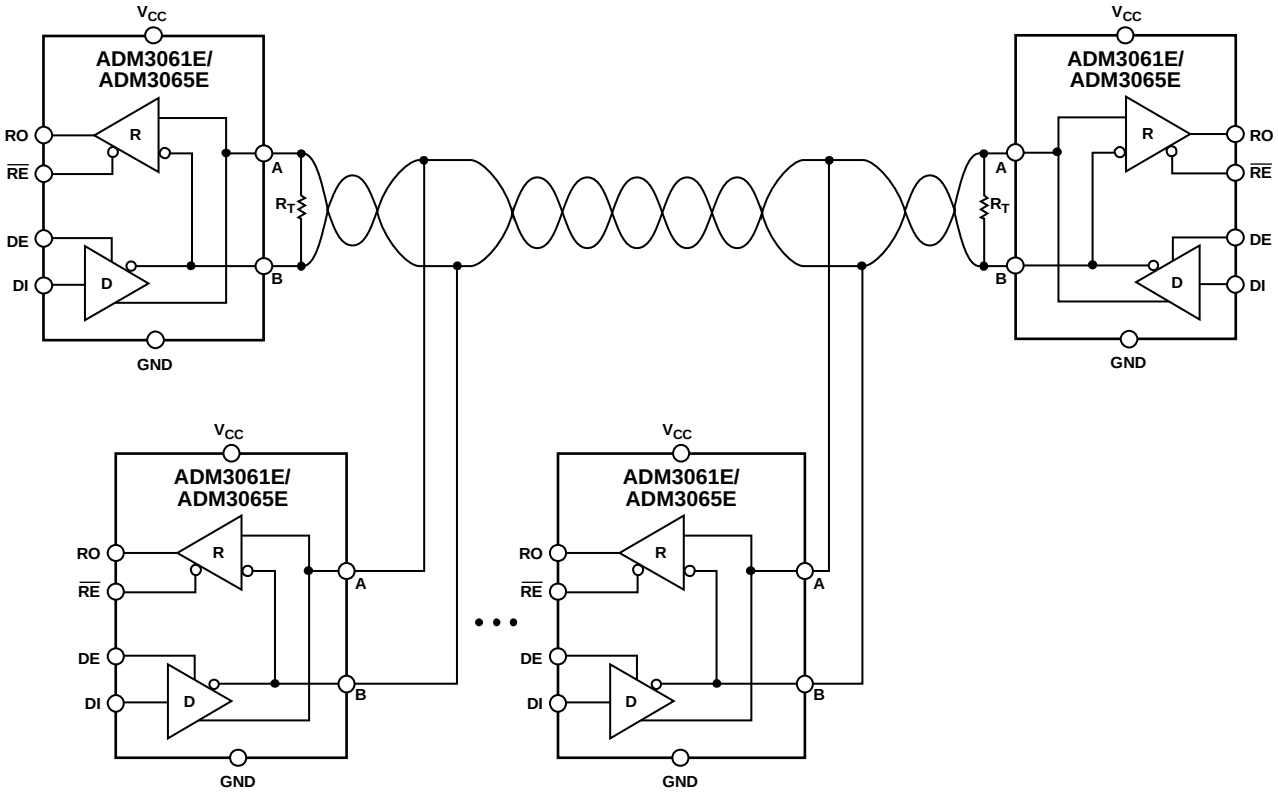
DRIVER OUTPUT PROTECTION

The ADM3061E/ADM3062E/ADM3063E/ADM3065E/ADM3066E/ADM3067E/ADM3068E feature two methods to prevent excessive output current and power dissipation caused by faults or by bus contention. Current-limit protection on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are reenabled at a temperature of 140°C.

APPLICATIONS INFORMATION

The ADM3061E/ADM3065E transceiver is designed for bidirectional data communications on multipoint bus transmission lines. Figure 47 shows a typical network applications circuit.

To minimize reflections, terminate the line at both ends with a termination resistor (the value of the termination resistor must be equal to the characteristic impedance of the cable used) and keep stub lengths off the main line as short as possible.



NOTES
1. THE MAXIMUM NUMBER OF NODES IS 128.
2. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 47. ADM3061E/ADM3065E Typical Half-Duplex RS-485 Communications Network

ISOLATED HIGH SPEED RS-485 NODE

Galvanic isolation, with reinforced insulation and 5 kV rms transient withstand voltage, can be added to the ADM3065E using Analog Devices, Inc., *i*Coupler® and *iso*Power® technology. The ADuM6401 provides the required quad channels of 5 kV rms signal isolation, operating at rates up to 25 Mbps, together with an integrated dc-to-dc converter. The ADuM6401 combines with the ADM3065E (shown in Figure 48) with the V_{ISO} pin configured for 3.3 V by connecting the V_{SEL} pin to GND_{ISO} and a 5 V supply connected to V_{DD1}. Operation at 3.3 V ensures the ADM3065E remains within the load capability of ADuM6401 even at 25 Mbps.

The dc-to-dc converter in the ADuM6401 *iso*Power device provides regulated, isolated power to the ADM3065E (and the ADuM241D). These *iso*Power devices use high frequency switching elements to transfer power through the transformers. Take care during PCB layout to meet emissions standards. See the AN-0971 Application Note for PCB layout recommendations.

Galvanic isolation of the ADM3065E at the full data rate, up to 50 Mbps, can be implemented using the ADuM241D quad-channel digital isolator and the ADuM6028 isolated dc-to-dc converter, as shown in Figure 49. The ADuM6028 is an 8-pin device that contains a 300 mW dc-to-dc converter optimized to meet emissions standards on a 2-layer PCB using two ferrite beads. The ADuM241D operates at a data rate up to 150 Mbps, and offers the precise timing required to fully support the ADM3065E at 50 Mbps.

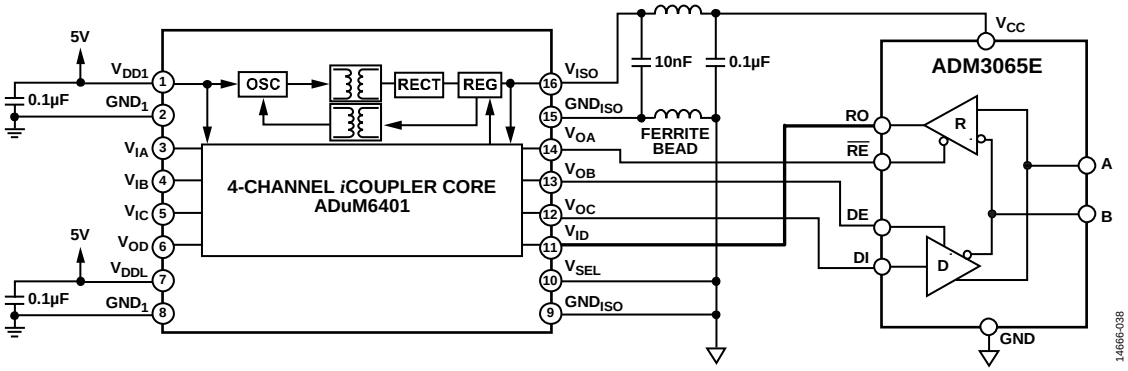


Figure 48. Signal and Power Isolated 25 Mbps RS-485 Solution (Simplified Diagram—All Connections Not Shown)

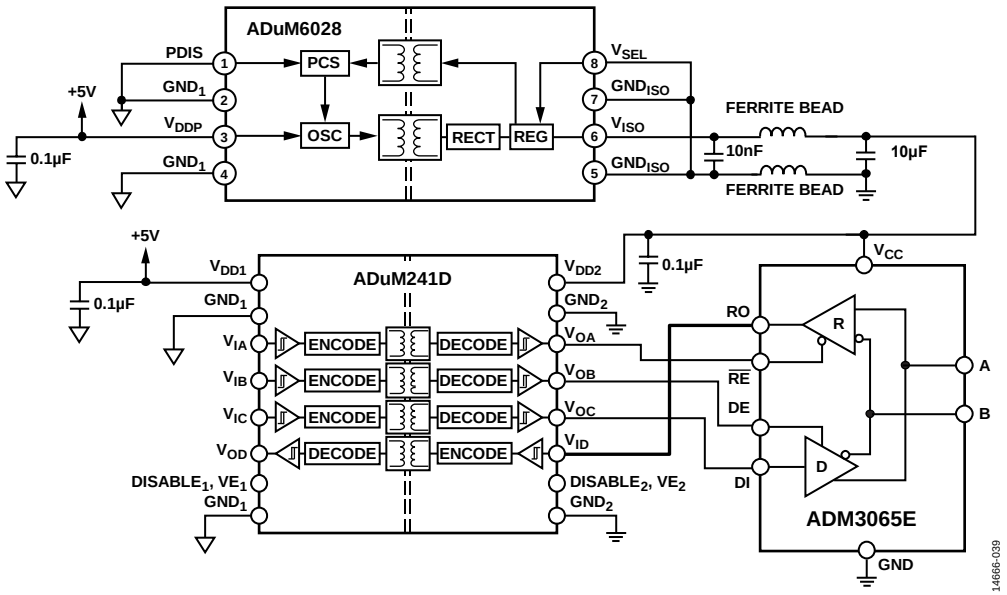
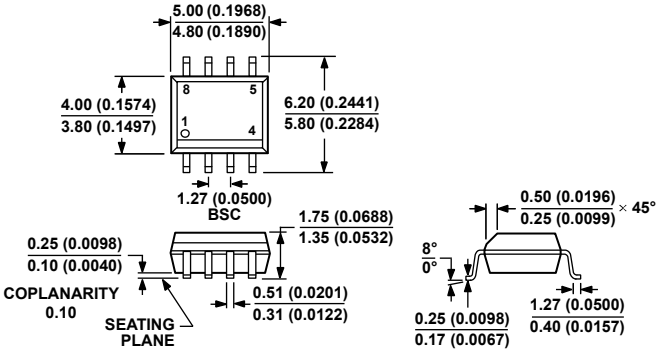


Figure 49. Signal and Power Isolated 50 Mbps RS-485 Solution (Simplified Diagram—All Connections Not Shown)

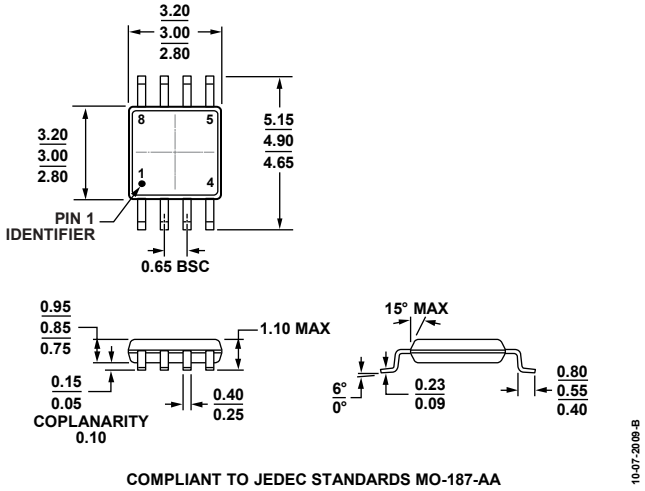
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 51. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

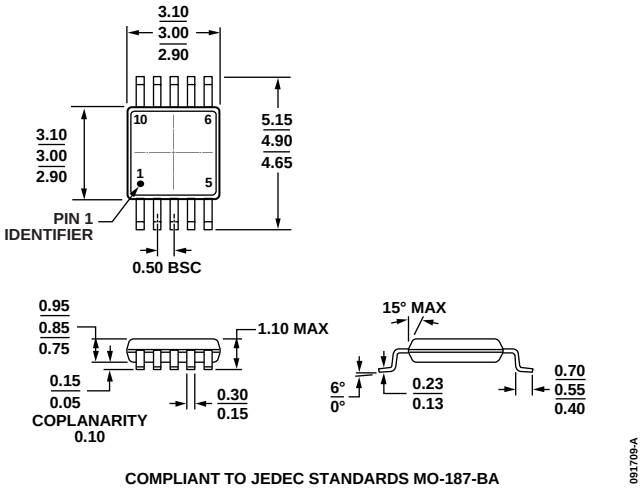


Figure 52. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

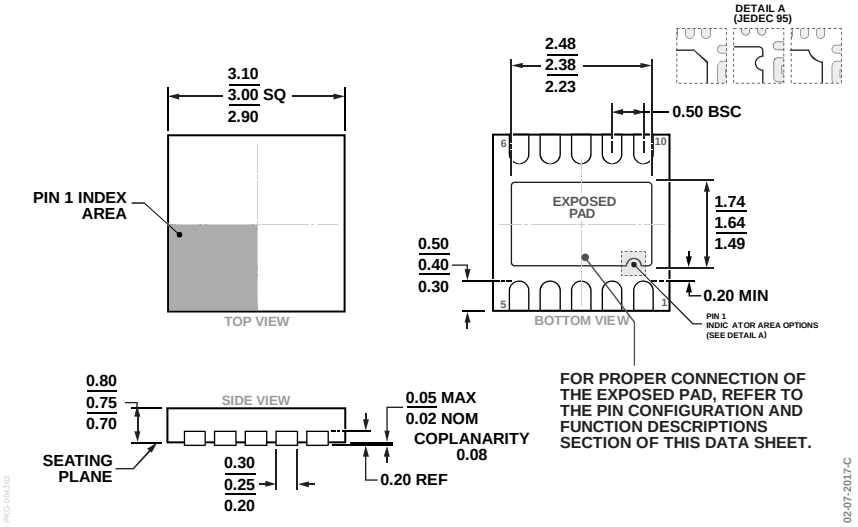


Figure 53. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-10-9)
Dimensions shown in millimeters

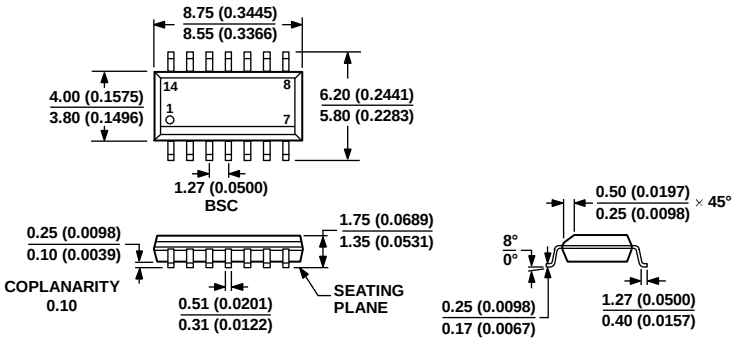


Figure 54. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADM3061EARZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3061EARZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3061EBRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3061EBRZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3061EARMZ	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	MBY
ADM3061EARMZ-R7	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	MBY
ADM3061EBRMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	MC0
ADM3061EBRMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	MC0
ADM3062EACPZ	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9	MCC
ADM3062EACPZ-R7	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9	MCC
ADM3062EBCPZ	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9	MCD
ADM3062EBCPZ-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9	MCD
ADM3062EARMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MC7
ADM3062EARMZ-R7	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MC7
ADM3062EBRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MC8
ADM3062EBRMZ-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MC8
ADM3063EARZ	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3063EARZ-R7	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3063EBRZ	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3063EBRZ-R7	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3065EARZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3065EARZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3065EBRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3065EBRZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3065EARMZ	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	MC1
ADM3065EARMZ-R7	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	MC1
ADM3065EBRMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	MC2
ADM3065EBRMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	MC2

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADM3066EACPZ	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9	MC9
ADM3066EACPZ-R7	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9	MC9
ADM3066EBCPZ	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9	MCA
ADM3066EBCPZ-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-9	MCA
ADM3066EARMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MC4
ADM3066EARMZ-R7	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MC4
ADM3066EBRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MC5
ADM3066EBRMZ-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MC5
ADM3067EARZ	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3067EARZ-R7	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3067EBRZ	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3067EBRZ-R7	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3068EARZ	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3068EARZ-R7	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3068EBRZ	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
ADM3068EBRZ-R7	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
EVAL-ADM3061EEBZ		8-Lead SOIC_N Evaluation Board		
EVAL-ADM3061EEB1Z		8-Lead MSOP Evaluation Board		
EVAL-ADM3062EEBZ		10-Lead MSOP Evaluation Board		
EVAL-ADM3062EEB1Z		10-Lead LFCSP Evaluation Board		
EVAL-ADM3063EEBZ		14-Lead SOIC_N Evaluation Board		
EVAL-ADM3065EEBZ		8-Lead SOIC_N Evaluation Board		
EVAL-ADM3065EEB1Z		8-Lead MSOP Evaluation Board		
EVAL-ADM3066EEBZ		10-Lead MSOP Evaluation Board		
EVAL-ADM3066EEB1Z		10-Lead LFCSP Evaluation Board		
EVAL-ADM3067EEBZ		14-Lead SOIC_N Evaluation Board		
EVAL-ADM3068EEBZ		14-Lead SOIC_N Evaluation Board		

[1] Z = RoHS Compliant Part.

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