Dual Output Synchronous Buck PWM Controller

Data Sheet

ADP1877

FEATURES

- Input voltage range: 2.75 V to 14.5 V
- Output voltage range: 0.6 V to 90% V_{IN}
- Maximum output current greater than 25 A per channel
- Programmable frequency: 200 kHz to 1.5 MHz
- Flex-Mode architecture with integrated drivers
- 180° phase shift minimizes input ripple current and required input capacitance
- ±0.85% output voltage accuracy −40°C to +85°C
- Integrated boost diodes
- Pulse skip high efficiency mode under light load
- Power good with internal pull-up resistor
- Overvoltage and overcurrent limit protection
- Thermal overload protection
- Input undervoltage lockout (UVLO)
- Externally adjustable soft start, slope compensation and current sense gain
- Independent precision enable inputs
- Synchronization input
- Suitable for any output capacitors
- Available in 32-lead 5 mm × 5 mm LFCSP

APPLICATIONS

- Set top boxes
- Printers
- Communication infrastructure
- Distributor power dc systems
- Industrial and instrumentation

GENERAL DESCRIPTION

The ADP1877 is a Flex-Mode™ (proprietary architecture of Analog Devices, Inc.), dual-channel, step-down switching controller with integrated drivers that drive N-channel synchronous power MOSFETs. The two PWM outputs are phase shifted 180°, which reduces the input RMS current, thus minimizing required input capacitance.

The boost diodes are built into the ADP1877, thus lowering the overall system cost and component count. The ADP1877 can be set to operate in pulse skip high efficiency mode under light load or in PWM continuous conduction mode.

The ADP1877 includes externally adjustable soft start, output overvoltage protection, externally adjustable current limit, power good, and a programmable oscillator frequency that ranges from 200 kHz to 1.5 MHz. The ADP1877 provides an output voltage accuracy of ±0.85% from −40°C to +85°C and ±1.5% from −40°C to 125°C in junction temperature. This part can be powered from a 2.75 V to 14.5 V supply, operates over the −40°C to +125°C junction temperature range, and is available in a 32-lead 5 mm × 5 mm LFCSP package.

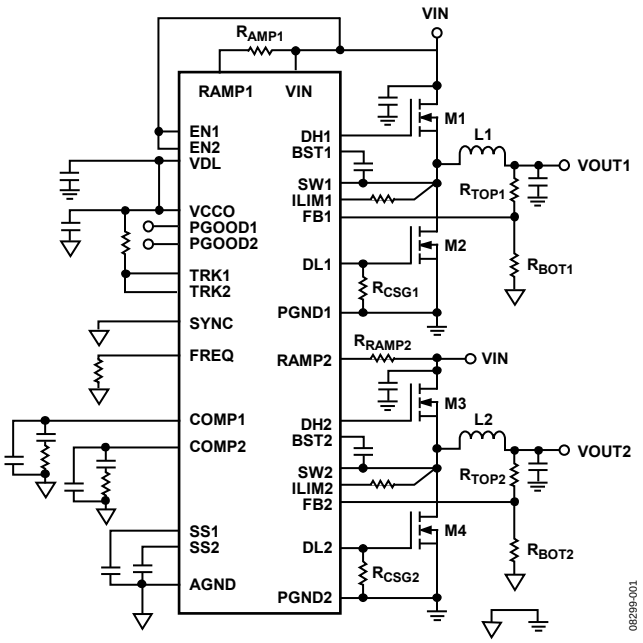

Figure 1. Typical Operation Circuit

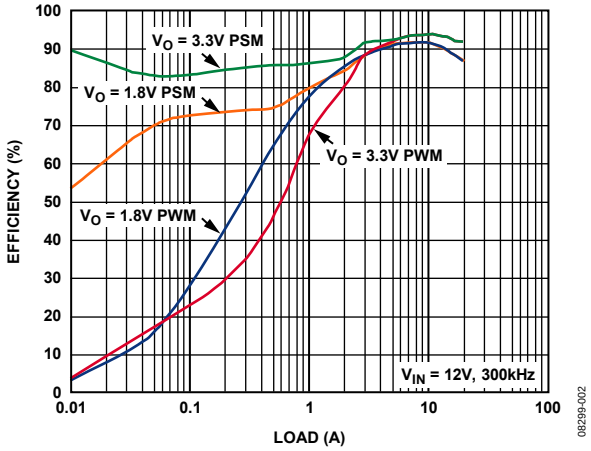

Figure 2. Efficiency Plot of Figure 42, 20 A Output

Rev. D

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SPECIFICATIONS

All limits at temperature extremes are guaranteed via correlation using standard statistical quality control. V_{IN} = 12 V. The specifications are valid for T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_A = 25°C.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Input Voltage	V_{IN}		2.75		14.5	V
Undervoltage Lockout Threshold	IN_{UVLO}	V_{IN} rising	2.45	2.6	2.75	V
		V_{IN} falling	2.4	2.5	2.6	
Undervoltage Lockout Hysteresis				0.1		V
Quiescent Current	I_{IN}	EN1 = EN2 = V_{IN} = 12 V, V_{FB} = V_{CCO} in PWM mode (no switching)		4.5	5.8	mA
Shutdown Current	I_{IN_SD}	EN1 = EN2 = GND, V_{IN} = 5.5 V or 14.5 V		100	200	µA
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB}		−100	+1	+100	nA
Transconductance	G_m	Sink or source 1 µA, T_A = 25 °C	440	550	660	µS
		Sink or source 1 µA	385	550	715	µS
TRK1, TRK2 Input Bias Current	I_{TRK}	0 V < $V_{TRK1/TRK2}$ < 1.5 V	−100	+1	+100	nA
CURRENT SENSE AMPLIFIER GAIN	A_{CS}	Gain resistor connected to DL, R_{CSG} = 47 kΩ ± 5%	2.4	3	3.6	V/V
		Gain resistor connected to DL, R_{CSG} = 22 kΩ ± 5%	5.2	6	6.9	V/V
		Default setting, R_{CSG} = open	10.5	12	13.5	V/V
		Gain resistor connected to DL, R_{CSG} = 100 kΩ ± 5%	20.5	24	26.5	V/V
OUTPUT CHARACTERICTISTICS						
Feedback Accuracy Voltage	V_{FB}	T_J = −40°C to +85°C, V_{FB} = 0.6 V	−0.85%	+0.6	+0.85%	V
		T_J = −40°C to +125°C, V_{FB} = 0.6 V	−1.5%	+0.6	+1.5%	V
Line Regulation of PWM	$\Delta V_{FB}/\Delta V_{IN}$			±0.015		%/V
Load Regulation of PWM	$\Delta V_{FB}/\Delta V_{COMP}$	V_{COMP} range 0.9 V to 2.2 V		±0.3		%
OSCILLATOR						
Frequency	f_{OSC}	R_{FREQ} = 340 kΩ to AGND	170	200	235	kHz
		R_{FREQ} = 78.7 kΩ to AGND	744	800	856	kHz
		R_{FREQ} = 39.2 kΩ to AGND	1275	1500	1725	kHz
		FREQ to AGND	235	300	345	kHz
		FREQ to VCCO	475	600	690	kHz
SYNC Input Frequency Range	f_{SYNC}	f_{SYNC} = 2 × f_{sw}; f_{SYNC} = f_{OSC}; the minimum sync frequency is 1 × the f_{OSC} set by the resistor	400		3000	kHz
SYNC Input Pulse Width	$t_{SYNCMIN}$		100			ns
SYNC Pin Capacitance to GND	C_{SYNC}			5		pF
LINEAR REGULATOR						
VCCO Output Voltage		T_A = 25°C, I_{VCCO} = 100 mA	4.8	5.0	5.18	V
		T_J = −40°C to +125°C	4.7	5.0	5.3	V
VCCO Load Regulation		I_{VCCO} = 0 mA to 100 mA,		35		mV
VCCO Line Regulation		V_{IN} = 5.5 V to 14.5 V, I_{VCCO} = 20 mA		10		mV
VCCO Current Limit[1]		VCCO drops to 4 V from 5 V		350		mA
VCCO Short-Circuit Current[1]		VCCO < 0.5 V		370	400	mA
VIN to VCCO Dropout Voltage[2]	$V_{DROPOUT}$	I_{VCCO} = 100 mA, V_{IN} ≤ 5 V		0.33		V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOGIC INPUTS						
EN1, EN2		EN1/EN2 rising	0.57	0.63	0.68	V
EN1, EN2 Hysteresis				0.03		V
EN1, EN2 Input Leakage Current	I_{EN}	V_{IN} = 2.75 V to 14.5 V		1	200	nA
SYNC Logic Input Low					1.3	V
SYNC Logic Input High			1.9			V
SYNC Input Leakage Current	I_{SYNC}	SYNC = 5 V, internal 1 MΩ pull-down		5	6.5	µA
GATE DRIVERS						
DH Rise Time		C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		16		ns
DH Fall Time		C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		14		ns
DL Rise Time		C_{DL} = 3 nF		16		ns
DL Fall Time		C_{DL} = 3 nF		14		ns
DH to DL Dead Time		External 3 nF is connected to DH and DL		25		ns
DH or DL Driver R_{ON}, Sourcing Current[1]	R_{ON_SOURC}	Sourcing 2 A with a 100 ns pulse		2		Ω
		Sourcing 1 A with a 100 ns pulse, V_{IN} = 3 V		2.3		Ω
DH or DL Driver R_{ON}, Tempco	TC_{RON}	V_{IN} = 3 V or 12 V		0.3		%/°C
DH or DL Driver R_{ON}, Sinking Current[1]	R_{ON_SINK}	Sinking 2 A with a 100 ns pulse		1.5		Ω
		Sinking 1 A with a 100 ns pulse, V_{IN} = 3 V		2		Ω
DH Maximum Duty Cycle		f_{OSC} = 300 kHz	90			%
DH Maximum Duty Cycle		f_{OSC} = 1500 kHz	50			%
Minimum DH On Time		f_{OSC} = 200 kHz to 1500 kHz			130	ns
Minimum DH Off Time		f_{OSC} = 200 kHz to 1500 kHz			330	ns
Minimum DL On Time		f_{OSC} = 200 kHz to 1500 kHz			280	ns
COMP VOLTAGE RANGE						
COMP Pulse Skip Threshold	$V_{COMP,THRES}$	In pulse skip mode		0.9		V
COMP Clamp High Voltage	$V_{COMP,HIGH}$		2.25			V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{TMSD}			155		°C
Thermal Shutdown Hysteresis				20		°C
OVERVOLTAGE AND POWER GOOD THRESHOLDS						
FB Overvoltage Threshold	V_{OV}	V_{FB} rising	0.67	0.7	0.73	V
FB Overvoltage Hysteresis				40		mV
FB Undervoltage Threshold	V_{UV}	V_{FB} rising	0.51	0.54	0.57	V
FB Undervoltage Hysteresis				30		mV
TRK INPUT VOLTAGE RANGE			0		5	V
FB TO TRK OFFSET VOLTAGE		TRK = 0.5 V to 0.6 V; offset = $V_{FB} - V_{TRK}$	−120	−70	−5	mV
SOFT START						
SS Output Current	I_{SS}	During start-up	4.6	6.5	8.4	µA
SS Pull-Down Resistor		During a fault condition		1		kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PGOOD						
PGOOD Pull-up Resistor	R_{PGOOD}	Internal pull-up resistor to VCCO		12.5		kΩ
PGOOD Delay				12		µs
Overvoltage or Undervoltage Minimum Duration		This is the minimum duration required to trip the PGOOD signal.		12		µs
ILIM1, ILIM2 Threshold Voltage[1]		Relative to PGND	−5	0	+5	mV
ILIM1, ILIM2 Output Current		ILIM = PGND	40	50	60	µA
Current Sense Blanking Period		After DL goes high, current limit is not sensed during this period.		100		ns
INTEGRATED RECTIFIER (BOOST DIODE) RESISTANCE		At 20 mA forward current		16		Ω
ZERO CURRENT CROSS OFFSET (SW TO PGND)[1]		In pulse skip mode only; f_{OSC} = 600 kHz	0	2	4	mV

[1] Guaranteed by design.
[2] Connect V_{IN} to VCCO when V_{IN} < 5.5 V. For applications with V_{IN} < 5.5 V and V_{IN} not connected to VCCO, keep in mind that VCCO = V_{IN} − VDROPOUT. VCCO must be ≥ 2.75 V for proper operation.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN1/EN2, RAMP1/RAMP2	15 V
FB1/FB2, COMP1/COMP2, SS1/SS2, TRK1/TRK2, FREQ, SYNC, VCCO, VDL, PGOOD1/PGOOD2	−0.3 V to +6 V
ILIM1/ILIM2	−0.3 V to +16 V
BST1/BST2, DH1/DH2, SW1/SW2 to PGND1/PGND2	−0.3 V to +22 V
DL1/DL2 to PGND1/PGND2	−0.3 V to VCCO + 0.3 V
BST1/BST2 to PGND1/PGND2, SW1/SW2 to PGND1/PGND2 20 ns Transients	+25 V
DL1/DL2, SW1/SW2, ILIM1/ILIM2 to PGND1/PGND2 20 ns Negative Transients	−8 V
PGND1/PGND2 to AGND	−0.3 V to +0.3 V
PGND1/PGND2 to AGND 20 ns Transients	−8 V to +4 V
θ_{JA}, =on a Multilayer PCB (Natural Convection)[1, 2]	32.6°C/W
Operating Ambient Temperature Range[3]	−40°C to +85°C
Operating Junction Temperature Range[3]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Soldering Lead Temperature	260°C

[1] Measured with exposed pad attached to PCB.
[2] Junction-to-ambient thermal resistance (θ_{JA}) of the package was calculated or simulated on a multilayer PCB.
[3] The device can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature, T_J, of the device is dependent on the ambient temperature, T_A, the power dissipation of the device, P_D, and the junction to ambient thermal resistance of the package, θ_{JA}. Maximum junction temperature is calculated from the ambient temperature and power dissipation using the formula $T_J = T_A + P_D \times \theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SIMPLIFIED BLOCK DIAGRAM

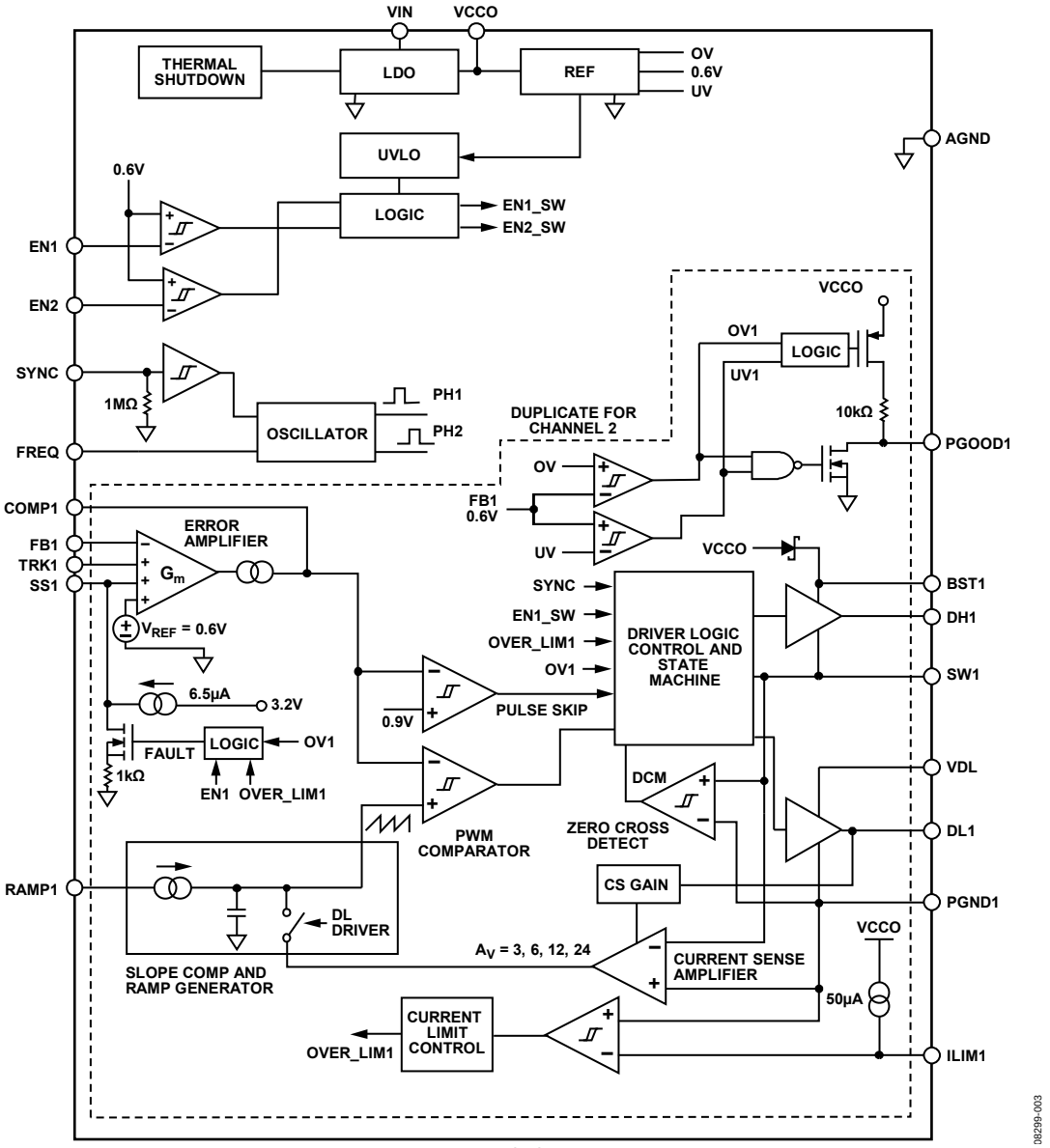


Figure 3. Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

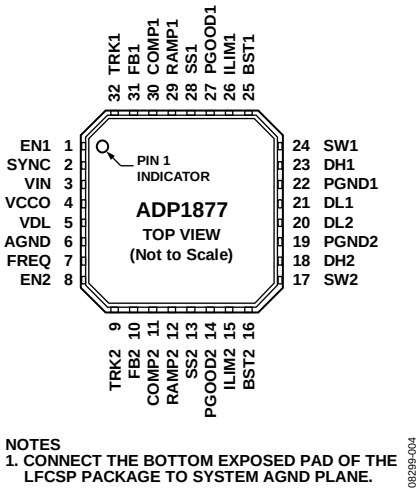


Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN1	Enable Input for Channel 1. Drive EN1 high to turn on the Channel 1 controller, and drive it low to turn off. Tie EN1 to VIN for automatic startup. For a precision UVLO, put an appropriately sized resistor divider from VIN to AGND, and tie the midpoint to this pin.
2	SYNC	Frequency Synchronization Input. Accepts an external signal between 1× and 2.3× of the internal oscillator frequency, f_{OSC}, set by the FREQ pin. The controller operates in forced PWM when a signal is detected at SYNC or when SYNC is high. The resulting switching frequency is ½ of the SYNC frequency. When SYNC is low or left floating, the controller operates in pulse skip mode.
3	VIN	Connect to Main Power Supply. Bypass with a 1 µF or larger ceramic capacitor connected as close to this pin as possible and PGND.
4	VCCO	Output of the Internal Low Dropout Regulator (LDO). The internal circuitry and gate drivers are powered from VCCO. Bypass VCCO to AGND with a 1 µF or larger ceramic capacitor. The VCCO output is always active, even during fault conditions and cannot be turned off even if EN1/EN2 is low. For operations at VIN below 5 V, VIN can be jumped to VCCO. Do not use the LDO to power other auxiliary system loads.
5	VDL	Power Supply for the Low-Side Driver. Bypass VDL to PGND with a 1 µF or greater ceramic capacitor. Connect VCCO to VDL.
6	AGND	Analog Ground.
7	FREQ	Sets the desired operating frequency between 200 kHz and 1.5 MHz with one resistor between FREQ and AGND. See Table 4 for more details. Connect FREQ to AGND for a preprogrammed 300 kHz or FREQ to VCCO for a 600 kHz operating frequency.
8	EN2	Enable Input for Channel 2. Drive EN2 high to turn on the Channel 2 controller, and drive it low to turn off. Tie EN2 to VIN for automatic startup. For a precision UVLO, put an appropriately sized resistor divider from VIN to AGND, and tie the midpoint to this pin.
9	TRK2	Tracking Input for Channel 2. If the tracking function is not used, it is recommended to connect TRK2 to VCCO through a resistor higher than 1 MΩ, or simply connect TRK2 between 0.7 V and 2 V to reduce the bias current going into the TRK2 pin.
10	FB2	Output Voltage Feedback for Channel 2. Connect to Channel 2 via a resistor divider.
11	COMP2	Compensation Node for Channel 2. Output of Channel 2 error amplifier. Connect a series resistor-capacitor network from COMP2 to AGND to compensate the regulation control loop.
12	RAMP2	Programmable Current Setting for Slope Compensation of Channel 2. Connect a resistor from RAMP2 to VIN. The voltage at RAMP2 is 0.2 V.
13	SS2	Soft Start Input for Channel 2. Connect a capacitor from SS2 to AGND to set the soft start period. This node is internally pulled up to 3.2 V through a 6.5 µA current source.

Pin No.	Mnemonic	Description
14	PGOOD2	Open-drain power-good indicator logic output with an internal 12 kΩ resistor connected between PGOOD2 and VCCO. PGOOD2 is pulled to ground when the Channel 2 output is outside the regulation window. An external pull-up resistor is not required.
15	ILIM2	Current Limit Sense Comparator Inverting Input for Channel 2. Connect a resistor between ILIM2 and SW2 to set the current limit offset. For accurate current limit sensing, connect ILIM2 to a current sense resistor at the source of the low-side MOSFET.
16	BST2	Boot Strapped Upper Rail of High Side Internal Driver for Channel 2. Connect a 0.1 µF to a 0.22 µF multilayer ceramic capacitor (MLCC) between BST2 and SW2. There is an internal boost rectifier connected between VCCO and BST2.
17	SW2	Switch Node for Channel 2. Connect to the source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET of Channel 2.
18	DH2	High-Side Switch Gate Driver Output for Channel 2. Capable of driving MOSFETs with total input capacitance up to 20 nF.
19	PGND2	Power Ground for Channel 2. Ground for internal Channel 2 driver. Differential current is sensed between SW2 and PGND2. It is not recommended to short PGND2 to PGND1 directly.
20	DL2	Low-Side Synchronous Rectifier Gate Driver Output for Channel 2. To set the gain of the current sense amplifier, connect a resistor between DL2 and PGND2. Capable of driving MOSFETs with a total input capacitance up to 20 nF.
21	DL1	Low-Side Synchronous Rectifier Gate Driver Output for Channel 1. To set the gain of the current sense amplifier, connect a resistor between DL1 and PGND1. Capable of driving MOSFETs with a total input capacitance up to 20 nF.
22	PGND1	Power Ground for Channel 1. Ground for internal Channel 1 driver. Differential current is sensed between SW1 and PGND1. It is not recommended to short PGND2 to PGND1 directly.
23	DH1	High-Side Switch Gate Driver Output for Channel 1. Capable of driving MOSFETs with a total input capacitance up to 20 nF.
24	SW1	Power Switch Node for Channel 1. Connect to the source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET of Channel 1.
25	BST1	Boot Strapped Upper Rail of High Side Internal Driver for Channel 1. Connect a 0.1 µF to a 0.22 µF multilayer ceramic capacitor (MLCC) between BST1 and SW1. There is an internal boost diode or rectifier connected between VCCO and BST1.
26	ILIM1	Current Limit Sense Comparator Inverting Input for Channel 1. Connect a resistor between ILIM1 and SW1 to set the current limit offset. For accurate current limit sensing, connect ILIM1 to a current sense resistor at the source of the low-side MOSFET.
27	PGOOD1	Power Good. Open drain power good indicator logic output with an internal 12 kΩ resistor connected between PGOOD1 and VCCO. PGOOD1 is pulled to ground when the Channel 1 output is outside the regulation window. An external pull-up resistor is not required.
28	SS1	Soft Start Input for Channel 1. Connect a capacitor from SS1 to AGND to set the soft start period. This node is internally pulled up to 3.2 V through a 6.5 µA current source.
29	RAMP1	Programmable Current Setting for Slope Compensation of Channel 1. Connect a resistor from RAMP1 to VIN. The voltage at RAMP1 is 0.2 V during operation. This pin is high impedance when the channel is disabled.
30	COMP1	Compensation Node for Channel 1. Output of Channel 1 error amplifier. Connect a series resistor-capacitor network from COMP1 to AGND to compensate the regulation control loop.
31	FB1	Output Voltage Feedback for Channel 1. Connect to Channel 1 via a resistor divider.
32	TRK1	Tracking Input for Channel 1. If the tracking function is not used, it is recommended to connect TRK1 to VCCO through a resistor higher than 1 MΩ, or simply connect TRK1 between 0.7 V and 2 V to reduce the bias current going into the TRK1 pin.
33	Bottom exposed pad	Connect the bottom exposed pad of the LFCSP package to the system AGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

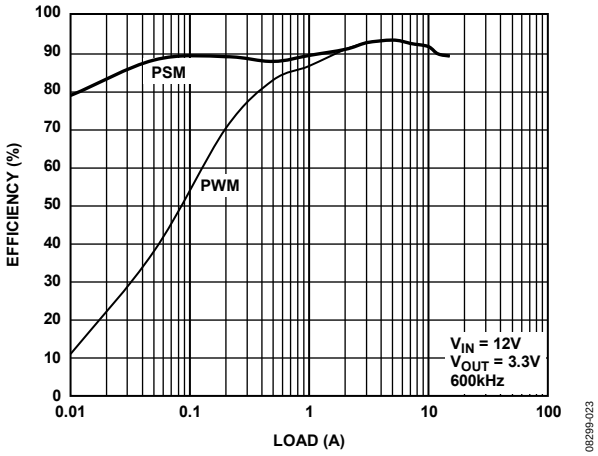


Figure 5. Efficiency Plot of Figure 41, 10 A Output

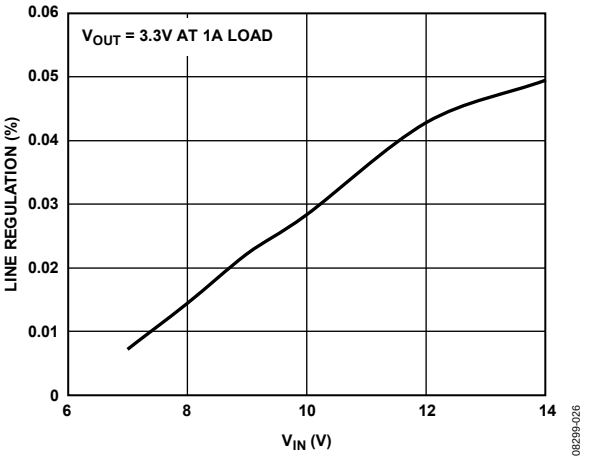


Figure 8. Line Regulation of Figure 42

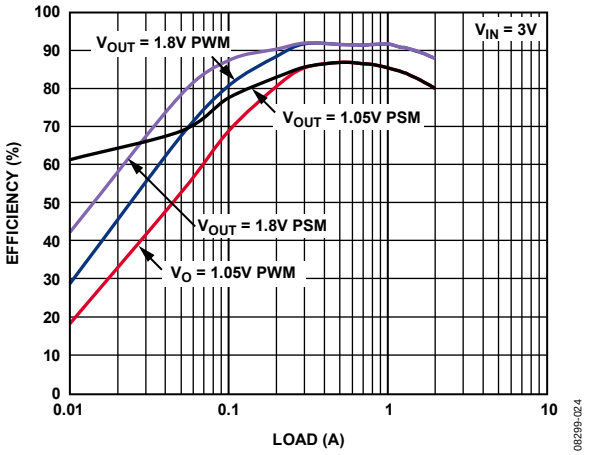


Figure 6. Efficiency Plot of Figure 44, 2 A Output

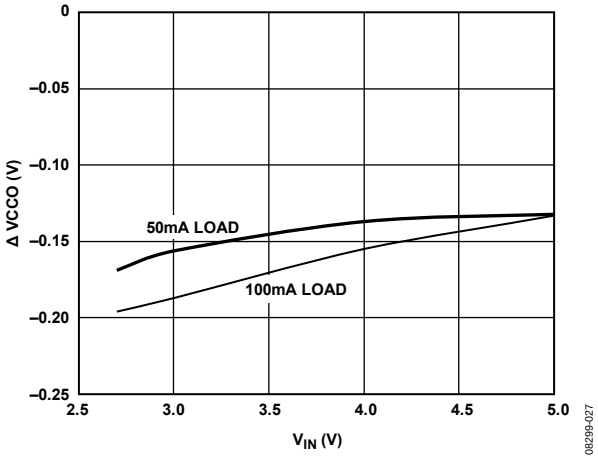


Figure 9. LDO Load Regulation

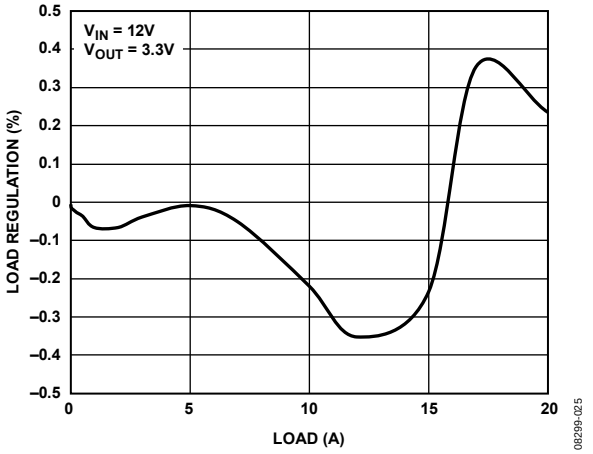


Figure 7. Load Regulation of Figure 42

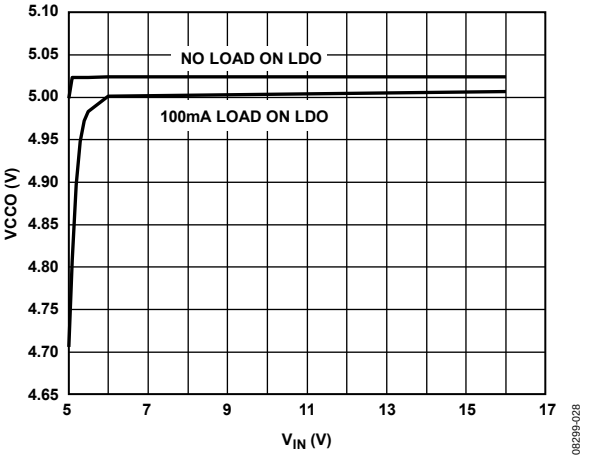


Figure 10. LDO Line Regulation

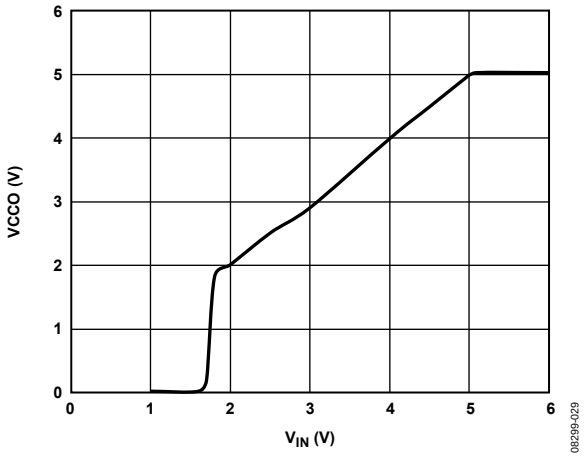


Figure 11. VCCO vs. V_{IN}

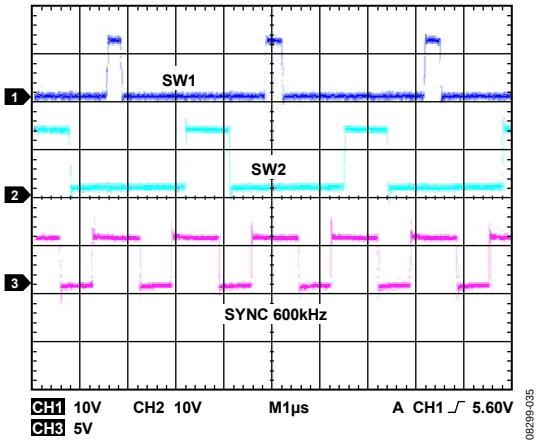


Figure 12. An Example of Synchronization, f_{SW} = 600 kHz

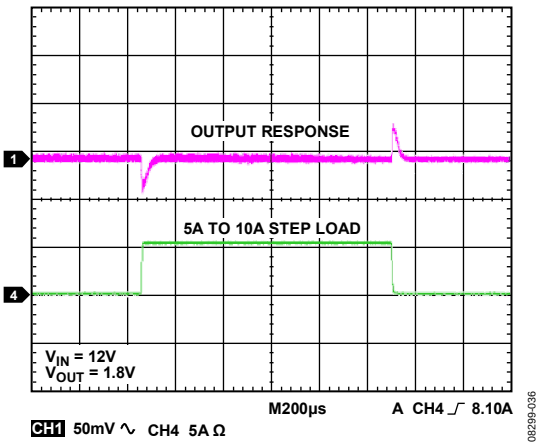


Figure 13. Step Load Transient of Figure 42, 5 A to 10 A

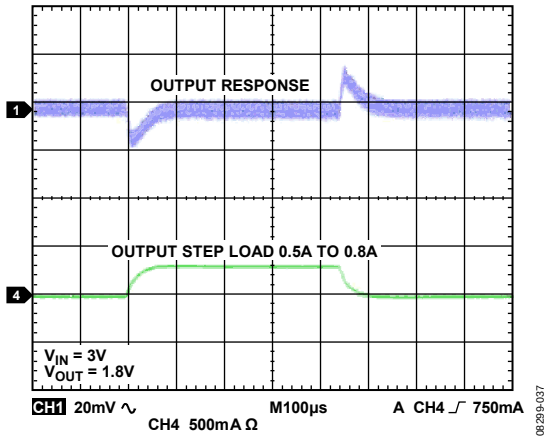


Figure 14. Step Load Transient of Figure 44

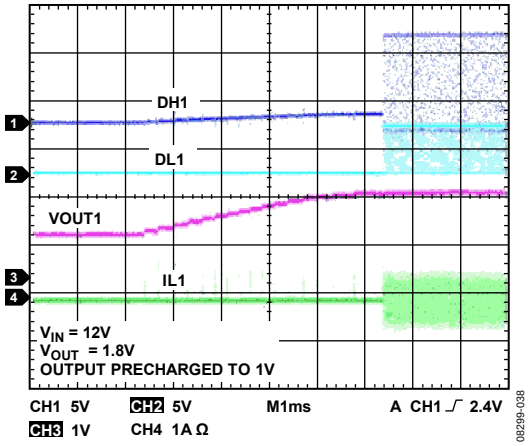


Figure 15. Soft Start into Precharged Output

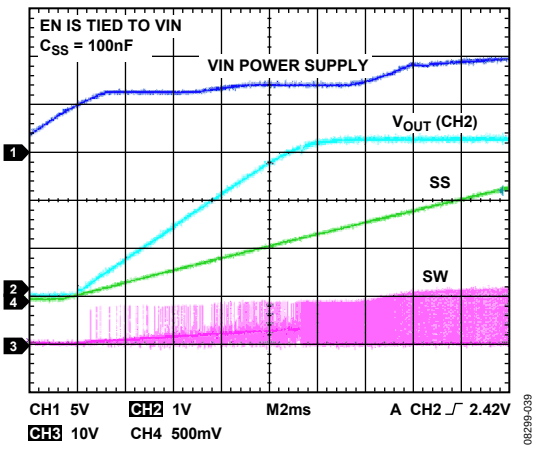


Figure 16. Power-On Sequence

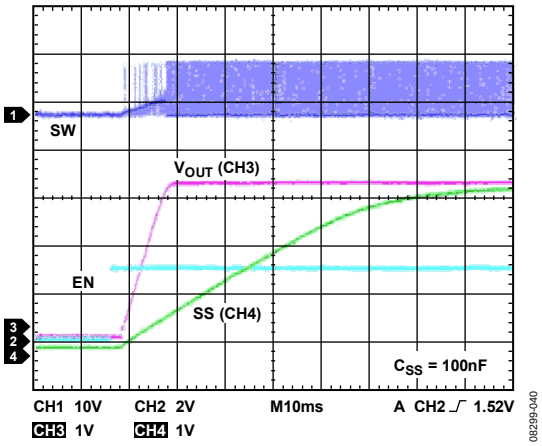


Figure 17. Enable Function

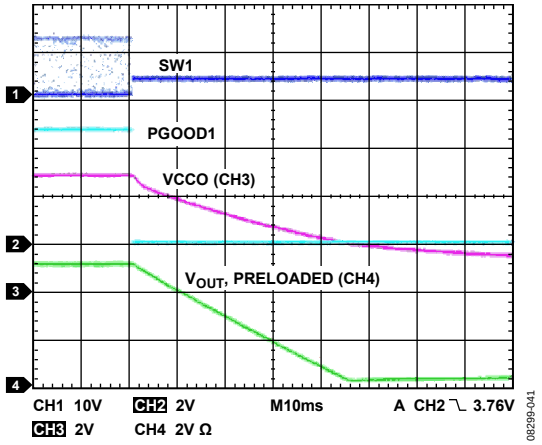


Figure 18. Thermal Shutdown Waveform

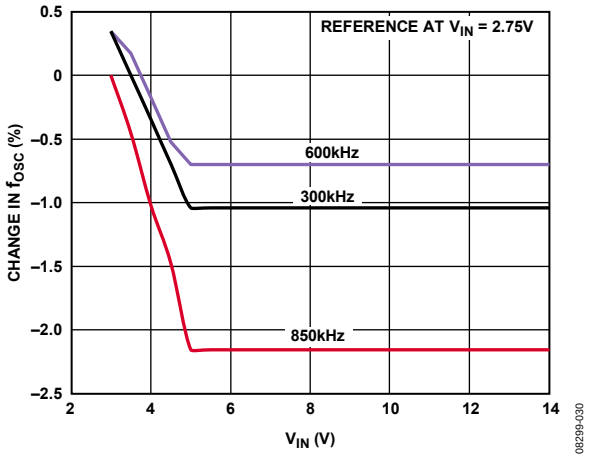


Figure 19. Change in f_{OSC} vs. V_{IN}

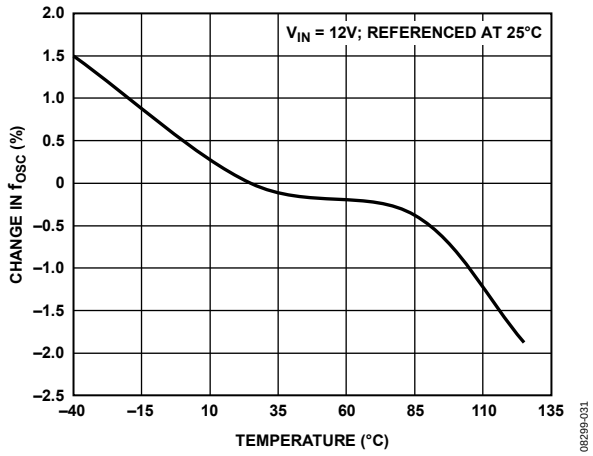


Figure 20. f_{OSC} vs. Temperature

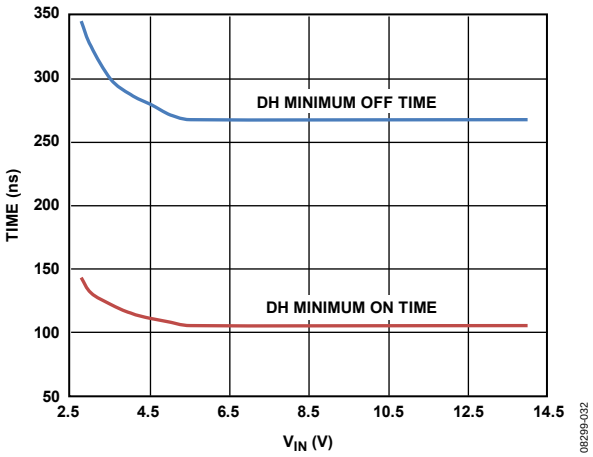


Figure 21. Typical DH Minimum On Time and Off Time

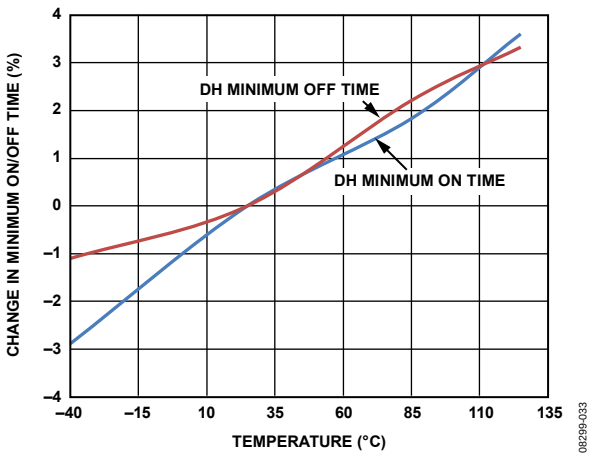


Figure 22. DH Minimum On Time and Off Time Overtemperature

THEORY OF OPERATION

The ADP1877 is a current mode (using ADI proprietary Flex-Mode architecture), dual-channel, step-down switching controller with integrated MOSFET drivers that drive N-channel synchronous power MOSFETs. The two outputs are phase shifted 180°. This reduces the input RMS current, thus minimizing required input capacitance.

The ADP1877 can be set to operate in pulse skip high efficiency mode under light load or in forced PWM. The integrated boost diodes in the ADP1877 reduce the overall system cost and component count. The ADP1877 includes programmable soft start, output overvoltage protection, programmable current limit, power good, and tracking function. The ADP1877 can be set to operate in any switching frequency between 200 kHz and 1.5 MHz with one external resistor.

CONTROL ARCHITECTURE

The ADP1877 is based on a fixed frequency current mode PWM control architecture. The inductor current is sensed by the voltage drop measured across the external low-side MOSFET R_{DSON} during the off period of the switching cycle (valley inductor current). The current sense signal is further processed by the current sense amplifier. The output of the current sense amplifier is held, and the emulated current ramp is multiplexed and fed into the PWM comparator as shown in Figure 23. The valley current information is captured at the end of the off period, and the emulated current ramp is applied at that point when the next on cycle begins. An error amplifier integrates the error between the feedback voltage and the generated the error voltage from the COMP pin (from error amp in Figure 23).

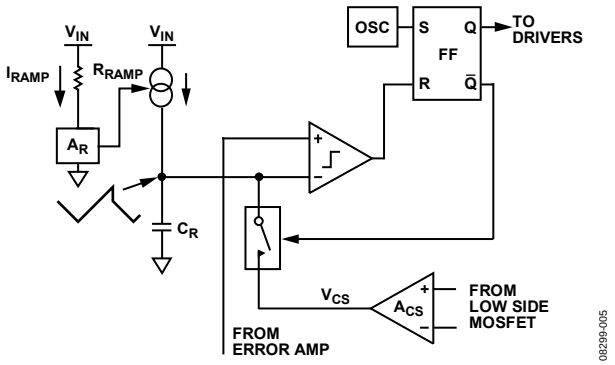


Figure 23. Simplified Control Architecture

As shown in Figure 23, the emulated current ramp is generated inside the IC but offers programmability through the RAMPx pin. Selecting an appropriate value resistor from V_{IN} to the RAMP pin programs a desired slope compensation value and, at the same time, provides a feed forward feature. The benefits realized by deploying this type of control scheme are that there is no need to worry about the turn-on current spike corrupting the current ramp. Also, the current signal is stable because the current signal is sampled at the end of the turn-off period, which gives time for the switch node ringing to settle. Other benefits of using current mode control scheme still apply, such as simplicity of loop compensation. Control logic enforces antishoot-through operation to limit cross conduction of the internal drivers and external MOSFETs.

OSCILLATOR FREQUENCY

The internal oscillator frequency, which ranges from 200 kHz to 1.5 MHz, is set by an external resistor, R_{FREQ}, at the FREQ pin. Some popular f_{OSC} values are shown in Table 4, and a graphical relationship is shown in Figure 24. For instance, a 78.7 kΩ resistor sets the oscillator frequency to 800 kHz. Furthermore, connecting FREQ to AGND or FREQ to VCCO sets the oscillator frequency to 300 kHz or 600 kHz, respectively. For other frequencies that are not listed in Table 4, the values of R_{FREQ} and f_{OSC} can be obtained from Figure 24, or use the following empirical formula to calculate these values:

$$R_{FREQ}(k\Omega) = 96568 \times f_{OSC}\ (kHz)^{-1.065}$$

Table 4. Setting the Oscillator Frequency

R_{FREQ}	f_{OSC} (Typical)
332 kΩ	200 kHz
78.7 kΩ	800 kHz
60.4 kΩ	1000 kHz
51 kΩ	1200 kHz
40.2 kΩ	1500 kHz
FREQ to AGND	300 kHz
FREQ to VCCO	600 kHz

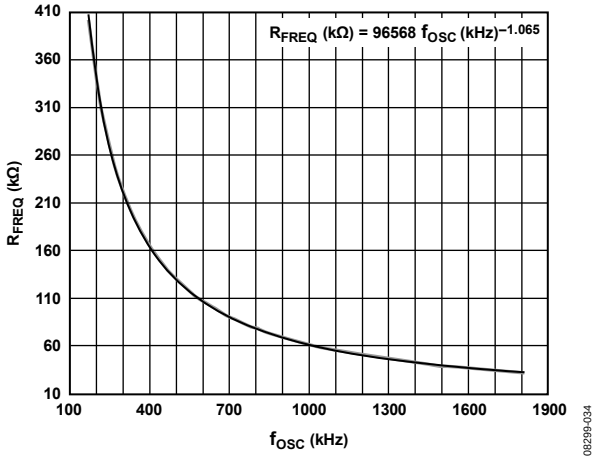


Figure 24. R_{FREQ} vs. f_{OSC}

MODE OF OPERATION

The SYNC pin is a multifunctional pin. PWM mode is enabled when SYNC is connected to VCCO or a high logic. With SYNC connected to ground or left floating, pulse skip mode is enabled. Switching SYNC from low to high or high to low on the fly causes the controller to transition from forced PWM to pulse skip mode or pulse skip mode to forced PWM, respectively, in two clock cycles.

Table 5. Mode of Operation Truth Table

SYNC Pin	Mode of Operation
Low	Pulse skip mode
High	Forced PWM
No Connect	Pulse skip mode
Clock Signal	Forced PWM

The ADP1877 has a built-in pulse skip sensing circuitry that allows the controller to skip PWM pulses, thus reducing the switching frequency at light loads and, therefore, maintaining high efficiency during a light load operation. The switching frequency is a fraction of the natural oscillator frequency and is automatically adjusted to regulate the output voltage. The resulting output ripple is larger than that of the fixed frequency forced PWM. Figure 25 shows that the ADP1877 operates in PSM under a light load of 10 mA. Pulse skip frequency under a certain light load is dependent on the inductor input and output voltages.

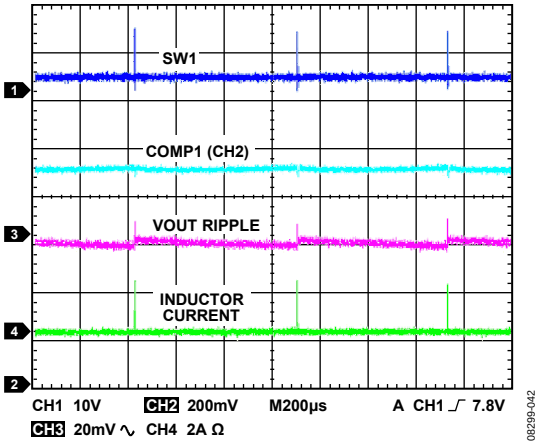


Figure 25. Example of Pulse Skip Mode Under a Light 5 mA Load

When the output load is greater than the pulse skip threshold current (when V_{COMP} reaches the threshold of 0.9 V), the ADP1877 exits the pulse skip mode operation and enters the fixed frequency discontinuous conduction mode (DCM), as shown in Figure 26. When the load increases further, the ADP1877 enters CCM.

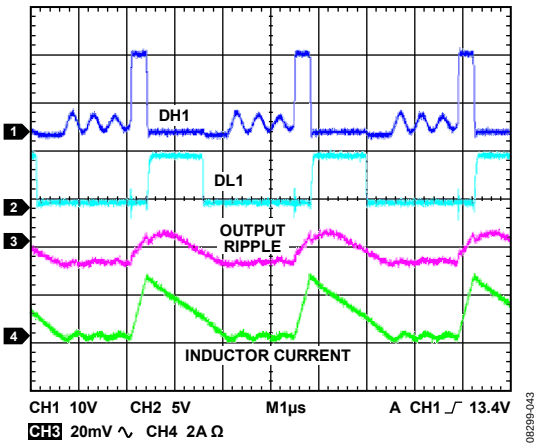


Figure 26. Example of Discontinuous Conduction Mode (DCM) Waveform

In forced PWM, the ADP1877 always operates in CCM at any load. The inductor current is always continuous (and even goes negative when there is no load); thus, efficiency is poor at light loads.

SYNCHRONIZATION

The switching frequency of the ADP1877 can be synchronized to an external clock by connecting SYNC to a clock signal, which should be between 1× and 2.3× of the internal oscillator frequency, f_{OSC}. The resulting switching frequency, f_{SW}, is ½ of the external SYNC frequency because the SYNC input is divided by 2, and the resulting phases are used to clock the two channels alternately. In synchronization, the ADP1877 operates in PWM, and f_{SW} equals ½ of f_{SYNC}.

When an external clock is detected at the first SYNC edge, the internal oscillator is reset, and the clock control shifts to SYNC. The SYNC edges then trigger subsequent clocking of the PWM outputs. The DH1/DH2 rising edges appear approximately 100 ns after the corresponding SYNC edge, and the frequency is locked to the external signal. Depending on the start-up conditions of Channel 1 and Channel 2, either Channel 1 or Channel 2 can be the first channel synchronized to the rising edge of the SYNC clock. If the external SYNC signal disappears during operation, the ADP1877 reverts to its internal oscillator. When the SYNC function is used, it is recommended to connect a pull-up resistor from SYNC to VCCO so that when the SYNC signal is lost, the ADP1877 continues to operate in PWM.

SOFT START

The soft start period is set by an external capacitor between SS1/SS2 and AGND. When EN1/EN2 is enabled, a current source of 6.5 µA starts charging the capacitor, and the regulation voltage is reached when the voltage at SS1/SS2 reaches 0.6 V. For more information, see the Applications Information section.

SYNCHRONOUS RECTIFIER AND DEAD TIME

The synchronous rectifier (low-side MOSFET) improves efficiency by replacing the Schottky diode that is normally used in an asynchronous buck regulator. In the ADP1877, the antishoot-through circuit monitors the SW and DL nodes and adjusts the low-side and high-side drivers to ensure break-before-make switching to prevent cross-conduction or shoot-through between the high-side and low-side MOSFETs. This break-before-make switching is known as the dead time, which is not fixed and depends on how fast the MOSFETs are turned on and off. In a typical application circuit that uses medium sized MOSFETs with input capacitance of approximately 3 nF, the typical dead time is approximately 30 ns. When small and fast MOSFETs are used, the dead time can be as low as 13 ns.

INPUT UNDERVOLTAGE LOCKOUT

When the bias input voltage, V_{IN}, is less than the undervoltage lockout (UVLO) threshold, the switch drivers stay inactive. When V_{IN} exceeds the UVLO threshold, the switchers start switching.

INTERNAL LINEAR REGULATOR

The internal linear regulator is low dropout (LDO), meaning it can regulate its output voltage, VCCO. VCCO powers up the internal control circuitry and provides power for the gate drivers. It is guaranteed to have more than 200 mA of output current capability, which is sufficient to handle the gate drive requirements of typical logic threshold MOSFETs driven at up to 1.5 MHz. VCCO is always active and cannot be shut down by the EN1/EN2 pins. Bypass VCCO to AGND with a 1 µF or greater capacitor.

Because the LDO supplies the gate drive current, the output of VCCO is subject to sharp transient currents as the drivers switch and the boost capacitors recharge during each switching cycle. The LDO has been optimized to handle these transients without overload faults. Due to the gate drive loading, using the VCCO output for other external auxiliary system load is not recommended.

The LDO includes a current limit well above the expected maximum gate drive load. This current limit also includes a short-circuit fold back to further limit the VCCO current in the event of a short-circuit fault.

The VDL pin provides power to the low-side driver. Connect VDL to VCCO. Bypass VDL to PGND with a 1 µF (minimum) ceramic capacitor, which must be placed close to the VDL pin.

For an input voltage less than 5.5 V, it is recommended to bypass the LDO by connecting VIN to VCCO, as shown in Figure 27, thus eliminating the dropout voltage. However, for example, if the input range is 4 V to 7 V, the LDO cannot be bypassed by shorting VIN to VCCO because the 7 V input has exceeded the maximum voltage rating of the VCCO pin. In this case, use the LDO to drive the internal drivers, but keep in mind that there is a dropout when V_{IN} is less than 5 V.

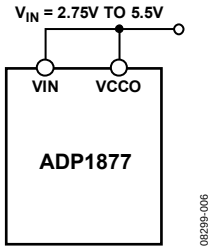


Figure 27. Configuration for V_{IN} < 5.5 V

OVERVOLTAGE PROTECTION

The ADP1877 has a built-in circuit for detecting output overvoltage at the FB node. When the FB voltage, V_{FB}, rises above the overvoltage threshold, the low-side NMOSFET is immediately turned on, and the high-side NMOSFET is turned off until the V_{FB} drops below the undervoltage threshold. This action is known as the crowbar overvoltage protection. If the overvoltage condition is not removed, the controller maintains the feedback voltage between the overvoltage and undervoltage thresholds, and the output is regulated to within approximately +16% and −10% of the regulation voltage. During an overvoltage event, the SS node discharges toward zero through an internal 1 kΩ pull-down resistor. When the voltage at FB drops below the undervoltage threshold, the soft start sequence restarts. The following graph shows the overvoltage protection scheme in action in PSM.

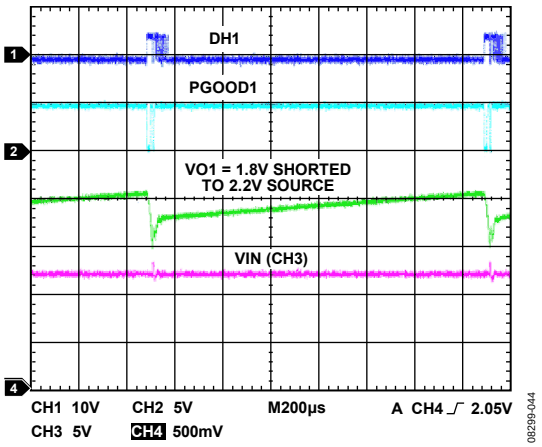


Figure 28. Overvoltage Protection in PSM

POWER GOOD

The PGOODx pin is an open-drain NMOS with an internal 12 kΩ pull-up resistor connected between PGOODx and VCCO. PGOODx is internally pulled up to VCCO during normal operation and is active low when tripped. When the feedback voltage, V_{FB}, rises above the overvoltage threshold or drops below the undervoltage threshold, the PGOODx output is pulled to ground after a delay of 12 µs. The overvoltage or undervoltage condition must exist for more than 12 µs for PGOODx to become active. The PGOODx output also becomes active if a thermal overload condition is detected.

SHORT-CIRCUIT AND CURRENT-LIMIT PROTECTION

When the output is shorted or the output current exceeds the current limit set by the R_{ILIM} resistor for eight consecutive cycles, the ADP1877 shuts off both the high-side and low-side drivers and restarts the soft start sequence every 10 ms, which is known as hiccup mode. The SS node discharges to zero through an internal 1 kΩ resistor during an overcurrent or short-circuit event. Figure 29 shows that the ADP1877 (a 20 A application circuit) is entering current limit hiccup mode when the output is shorted.

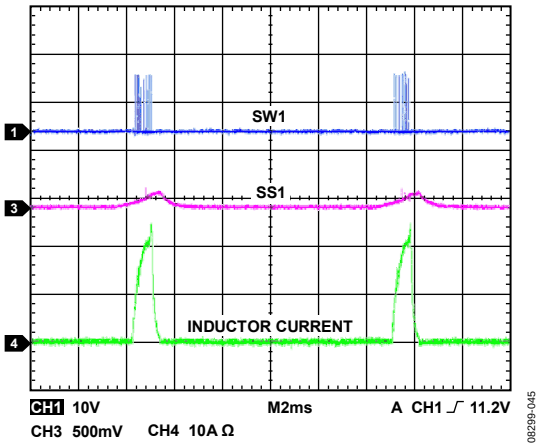


Figure 29. Current Limit Hiccup Mode, 20 A Circuit

SHUTDOWN CONTROL

The EN1 and EN2 pins are used to enable or disable Channel 1 and Channel 2, respectively, of the ADP1877. The precision enable threshold for EN1/EN2 is typically 0.63 V. When the EN1/EN2 voltage rises above 0.63 V, the ADP1877 is enabled and starts normal operation after the soft start period. When the voltage at EN1/EN2 drops below 0.57 V, the switchers and the internal circuits in the ADP1877 are turned off. Note that EN1/EN2 cannot shut down the LDO at VCCO, which is always active.

For the purpose of start-up power sequencing, the startup of the ADP1877 can be programmed by connecting an appropriate resistor divider from the master power supply to the EN1/EN2 pin, as shown in Figure 30. For instance, if the desired start-up voltage from the master power supply is 10 V, R1 and R2 can be set to 156 kΩ and 10 kΩ, respectively.

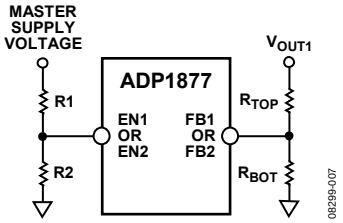


Figure 30. Optional Power-Up Sequencing Circuit

THERMAL OVERLOAD PROTECTION

The ADP1877 has an internal temperature sensor that senses the junction temperature of the chip. When the junction temperature of the ADP1877 reaches approximately 155°C, the ADP1877 goes into thermal shutdown, the converter is turned off, and SS discharges toward zero through an internal 1 kΩ resistor. At the same time, VCCO discharges to zero. When the junction temperature drops below 135°C, the ADP1877 resumes normal operation after the soft start sequence.

APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE

The output voltage is set using a resistive voltage divider from the output to FB. The voltage divider divides down the output voltage to the 0.6 V FB regulation voltage to set the regulation output voltage. The output voltage can be set to as low as 0.6 V and as high as 90% of the power input voltage.

The maximum input bias current into FB is 100 nA. For a 0.15% degradation in regulation voltage and with 100 nA bias current, the low-side resistor, R_{BOT}, must be less than 9 kΩ, which results in 67 µA of divider current. For R_{BOT}, use a 1 kΩ to 20 kΩ resistor. A larger value resistor can be used but results in a reduction in output voltage accuracy due to the input bias current at the FB pin, while lower values cause increased quiescent current consumption. Choose R_{TOP} to set the output voltage by using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right)$$

where:
R_{TOP} is the high-side voltage divider resistance.
R_{BOT} is the low-side voltage divider resistance.
V_{OUT} is the regulated output voltage.
V_{FB} is the feedback regulation threshold, 0.6 V.

The minimum output voltage is dependent on f_{SW} and minimum DH on time. The maximum output voltage is dependent on f_{SW}, the minimum DH off time, and the IR drop across the high-side N-channel MOSFET (NMOSFET) and the DCR of the inductor. For example, with an f_{SW} of 600 kHz (or 1.67 µs) and minimum on time of 130 ns, the minimum duty cycle is approximately 7.8% (130 ns/1.67 µs). If V_{IN} is 12 V and the duty cycle is 7.8%, then the lowest output is 0.94 V. As an example for the maximum output voltage, if V_{IN} is 5 V, f_{SW} is 600 kHz, and the minimum DH off time is 390 ns (330 ns DH off time plus approximately 60 ns total dead time), then the maximum duty cycle is 76%. Therefore, the maximum output is approximately 3.8 V. If the IR drop across the high-side NMOSFET and the DCR of the inductor is 0.5 V, then the absolute maximum output is 4.5 V (5 V − 0.5 V), independent of f_{SW} and duty cycle.

SOFT START

Program the soft start by connecting a capacitor from SSx to AGND. The soft start function limits the input inrush current and prevents the output overshoot.

On startup, a 6.5 µA current source charges the SSx capacitor. The soft start period is approximated by

$$t_{SS} = \frac{0.6\,V}{6.5\,\mu A} C_{SS}$$

The SSx pin reaches a final voltage equal to VCCO. If the output voltage is precharged prior to turn-on, the ADP1877 prevents reverse inductor current, which discharges the output capacitor. Once the voltage at SSx exceeds the regulation voltage (typically 0.6 V), the reverse current is reenabled to allow the output voltage regulation to be independent of load current.

When a controller is disabled, for instance, EN1/EN2 is pulled low or experiences an overcurrent limit condition, the soft start capacitor is discharged through an internal 1 kΩ pull-down resistor.

SETTING THE CURRENT LIMIT

The current limit comparator measures the voltage across the low-side MOSFET to determine the load current.

The current limit is set by an external current limit resistor, R_{ILIM}. The current sense pin, ILIMx, sources 50 µA to this external resistor. This creates an offset voltage of R_{ILIM} multiplied by 50 µA. When the drop across the low-side MOSFET, R_{DSON}, is equal to or greater than this offset voltage, the ADP1877 flags a current limit event.

Because the ILIMx current and the MOSFET, R_{DSON}, vary over process and temperature, the minimum current limit should be set to ensure that the system can handle the maximum desired load current. To do this, use the peak current in the inductor, which is the desired output current limit level plus ½ of the ripple current, the maximum R_{DSON} of the MOSFET at its highest expected temperature, and the minimum ILIM current.

$$R_{ILIM} = \frac{I_{LPK} \times R_{DSON\_MAX}}{40\ \mu A}$$

where:
I_{LPK} is the peak inductor current.

The buck converters usually run a fairly high current. PCB layout and component placement may affect the current limit setting. An iteration of the R_{ILIM} value may be required for a particular board layout and MOSFET selection. If alternative MOSFETs are substituted at some point in production, these resistor values may also need an iteration. Keep in mind that the temperature coefficient of the MOSFET, R_{DSON}, is typically 0.4%/°C.

ACCURATE CURRENT-LIMIT SENSING

R_{DSON} of the MOSFET can vary by more than 50% over the temperature range. Accurate current limit sensing can be achieved by adding a current sense resistor from the source of the low-side MOSFET to PGND. Make sure that the power rating of the current sense resistor is adequate for the application. Apply the above equation and calculate R_{ILIM} by replacing R_{DSON_MAX} with R_{SENSE}. The Figure 31 illustrates the implementation of this accurate current limit sensing.

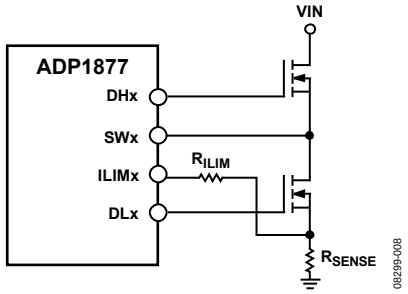


Figure 31. Accurate Current Limit Sensing

SETTING THE SLOPE COMPENSATION

In a current-mode control topology, slope compensation is needed to prevent subharmonic oscillations in the inductor current and to maintain a stable output. The external slope compensation is implemented by summing the amplified sense signal and a scaled voltage at the RAMPx pin. To implement the slope compensation, connect a resistor between RAMPx and the input voltage. The resistor, R_{RAMP}, is calculated by

$$R_{RAMP} = \frac{3.6 \times 10^{10} L}{A_{CS} \times R_{DSON\_MAX}}$$

where:
3.6×10^{10} is an internal parameter.
L is the inductance of the inductor.
R_{DSON_MAX} is the the low-side MOSFET maximum on resistance.
A_{CS} is the gain, either 3 V/V, 6 V/V, 12 V/V, or 24 V/V, of the current sense amplifier (see the Setting the Current Sense Gain section for more details).

Keep in mind that R_{DSON} is temperature dependent and can vary as much as 0.4%/°C. Choose R_{DSON} at the maximum operating temperature. The voltage at RAMPx is fixed at 0.2 V, and the current going into RAMPx should be in between 6 µA and 200 µA. Make sure that the following condition is satisfied:

$$6\,\mu A \le \frac{V_{IN} - 0.2V}{R_{RAMP}} \le 200\,\mu A$$

For instance, with an input voltage of 12 V, R_{RAMP} should not exceed 1.9 MΩ. If the calculated R_{RAMP} produces less than 6 µA, then select a R_{RAMP} value that produces between 6 µA and 20 µA. Figure 32 illustrates the connection of the slope compensation resistor R_{RAMP} and the current sense gain resistor R_{CSG}.

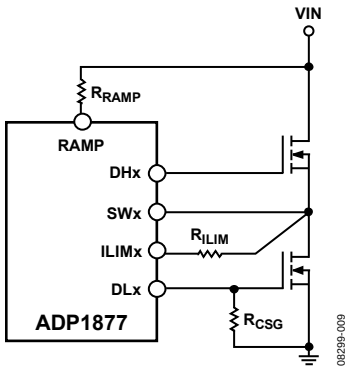


Figure 32. Slope Compensation and CS Gain Connection

SETTING THE CURRENT SENSE GAIN

The voltage drop across the external low-side MOSFET is sensed by a current sense amplifier by multiplying the peak inductor current and the R_{DSON} of the MOSFET. The result is then amplified by a gain factor of either 3 V/V, 6 V/V, 12 V/V, or 24 V/V, which is programmable by an external resistor, R_{CSG}, connected to the DL pin. This gain is sensed only during power-up and not during normal operation. The amplified voltage is summed with the slope compensation ramp voltage and fed into the PWM controller for a stable regulation voltage.

The voltage range of the internal node, V_{CS}, is between 0.4 V and 2.2 V. Select the current sense gain such that the internal minimum amplified voltage (V_{CSMIN}) is above 0.4 V and the maximum amplified voltage (V_{CSMAX}) is 2.1 V. Do not set V_{CSMAX} above 2.1 V to account for temperature and part-to-part variations. Note that V_{CSMIN} or V_{CSMAX} is not the same as V_{COMP}, which has a range of 0.75 V to 2.25 V. The following are equations for V_{CSMIN} and V_{CSMAX}:

$$V_{CSMIN} = 0.75\ V - \frac{1}{2} I_{LPP} \times R_{DSON\_MIN} \times A_{CS}$$

$$V_{CSMAX} = 0.75\ V + (I_{LOADMAX} - \frac{1}{2} I_{LPP}) \times R_{DSON\_MAX} \times A_{CS}$$

where:
V_{CSMIN} is the minimum amplified voltage of the internal current sense amplifier at zero output current.
V_{CSMAX} is the maximum amplified voltage of the internal current sense amplifier at maximum output current.
R_{DSON_MIN} is the the low-side MOSFET minimum on resistance. The zero-current level voltage of the current sense amplifier is 0.75 V.
I_{LPP} is the peak-to-peak ripple current in the inductor.
$I_{LOADMAX}$ is the maximum output DC load current.

Table 6 shows the appropriate current sense gain settings for a given R_{DSON} maximum load current and a 33% inductor current ripple. Because of the variation in R_{DSON} of the power MOSFETs (part-to-part variation and overtemperature) and the variation of the inductors, the users must verify that V_{COMP} does not exceed 2.2 V at the maximum output load current.

Table 6. CS Gain Setting Selection Table for Some Popular Configurations

I_{LPP} = 33% Load		ACS = 3		ACS = 6		ACS = 12		ACS = 24	
R_{DSON} (mΩ)	Load (A)	V_{CS} Min (V)	V_{CS} Max (V)	V_{CS} Min (V)	V_{CS} Max (V)	V_{CS} Min (V)	V_{CS} Max (V)	V_{CS} Min (V)	V_{CS} Max (V)
1.5	25	0.73	0.9	0.71	1.01	0.7	1.3	0.6	1.80
2	25	0.73	0.9	0.70	1.10	0.7	1.4		
2	20	0.73	0.9	0.71	1.03	0.7	1.3		
3	20	0.72	1.0	0.69	1.17	0.6	1.6		
5	15	0.71	1.0	0.68	1.27	0.6	1.8		
7	10	0.72	1.0	0.68	1.24	0.6	1.7		
10	10	0.70	1.1	0.65	1.45				
15	8	0.69	1.2	0.63	1.59				
18	8	0.68	1.3	0.61	1.76				
20	7	0.68	1.2	0.61	1.73				
25	5	0.69	1.2	0.63	1.62				
30	5	0.68	1.3	0.60	1.80				
40	5	0.65	1.4						
60	3	0.66	1.4						
80	2	0.67	1.3						
100	2	0.65	1.4						
120	2	0.63	1.6						

INPUT CAPACITOR SELECTION

The input current to a buck converter is a pulse waveform. It is zero when the high-side switch is off and approximately equal to the load current when it is on. The input capacitor carries the input ripple current, allowing the input power source to supply only the direct current. The input capacitor needs sufficient ripple current rating to handle the input ripple, as well as an ESR that is low enough to mitigate input voltage ripple. For the usual current ranges for these converters, it is good practice to use two parallel capacitors placed close to the drains of the high-side switch MOSFETs (one bulk capacitor of sufficiently high current rating and a 10 µF ceramic decoupling capacitor, typically).

Select an input bulk capacitor based on its ripple current rating. First, determine the duty cycle of the output.

$$D = \frac{V_{OUT}}{V_{IN}}$$

The input capacitor RMS ripple current is given by

$$I_{RMS} = I_O \sqrt{D(1-D)}$$

Where I_O is the output current, and D is the duty cycle.

The minimum input capacitance required for a particular load is

$$C_{IN,MIN} = \frac{I_O \times D(1-D)}{(V_{PP} - I_O \times DR_{ESR}) f_{SW}}$$

Where V_{PP} is the desired input ripple voltage, and R_{ESR} is the equivalent series resistance of the capacitor.

If an MLCC capacitor is used, the ESR is near 0, then the equation is simplified to

$$C_{IN,MIN} = I_O \times \frac{D(1-D)}{V_{PP} \times f_{SW}}$$

The capacitance of MLCC is voltage dependent. The actual capacitance of the selected capacitor must be derated accordingly. In addition, add more bulk capacitance, such as by using electrolytic or polymer capacitors, as necessary for large step load transients. Make sure the current ripple rating of the bulk capacitor exceeds the minimum input current ripple of a particular design.

INPUT FILTER

Normally the input pin, VIN, with a 0.1 µF or greater value bypass capacitor to AGND, is sufficient for filtering out any unwanted switching noise. However, depending on the PCB layout, some switching noises can be passed down to the ADP1877 internal circuitry; therefore, it is recommended to have a low pass filter at the VIN pin. Connecting a resistor, between 2 Ω and 5 Ω, in series with VIN and a 1 µF ceramic capacitor between VIN and AGND creates a low pass filter that effectively filters out any unwanted glitches caused by the switching regulator. Keep in mind that the input current could be larger than 100 mA when driving large MOSFETs. A 100 mA across a 5 Ω resistor creates a 0.5 V drop, which is the same voltage drop in VCCO. In this case, a lower resistor value is desirable.

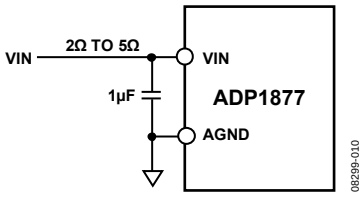


Figure 33. Input Filter Configuration

BOOST CAPACITOR SELECTION

To lower system component count and cost, the ADP1877 has a built-in rectifier (equivalent to the boost diode) between VCCO and BSTx. Choose a boost ceramic capacitor with values between 0.1 µF and 0.22 µF, which provides the current for the high-side driver during switching.

INDUCTOR SELECTION

The output LC filter smoothes the switched voltage at SWx. Choose an inductor value such that the inductor ripple current is approximately 1⁄3 of the maximum dc output load current. Using a larger value inductor results in a physical size larger than required, and using a smaller value results in increased losses in the inductor and/or MOSFET switches and larger voltage ripples at the output.

Choose the inductor value by the following equation:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}}$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
ΔI_L is the inductor ripple current, typically 1⁄3 of the maximum dc load current.

OUTPUT CAPACITOR SELECTION

Choose the output bulk capacitor to set the desired output voltage ripple. The impedance of the output capacitor at the switching frequency multiplied by the ripple current gives the output voltage ripple. The impedance is made up of the capacitive impedance plus the nonideal parasitic characteristics, the equivalent series resistance (ESR), and the equivalent series inductance (ESL). The output voltage ripple can be approximated with

$$\Delta V_{OUT} \cong \Delta I_L \left(R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}} + 4 f_{SW} \times L_{ESL} \right)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
R_{ESR} is the equivalent series resistance of the output capacitor (or the parallel combination of ESR of all output capacitors).
L_{ESL} is the equivalent series inductance of the output capacitor (or the parallel combination of ESL of all capacitors).

Solving C_{OUT} in the previous equation yields

$$C_{OUT} \cong \frac{\Delta I_L}{8 f_{SW}} \times \frac{1}{\Delta V_{OUT} - \Delta I_L R_{ESR} - 4 \Delta I_L f_{SW} \times L_{ESL}}$$

Usually, the impedance is dominated by ESR, such as in electrolytic or polymer capacitors, at the switching frequency, as stated in the maximum ESR rating on the capacitor data sheet; therefore, output ripple reduces to

$$\Delta V_{OUT} \cong \Delta I_L \times R_{ESR}$$

Electrolytic capacitors also have significant ESL, on the order of 5 nH to 20 nH, depending on type, size, and geometry. PCB traces contribute some ESR and ESL, as well. However, using the maximum ESR rating from the capacitor data sheet usually provides some margin such that measuring the ESL is not usually required.

In the case of output capacitors where the impedance of the ESR and ESL are small at the switching frequency, for instance, where the output cap is a bank of parallel MLCC capacitors, the capacitive impedance dominates and the output capacitance equation reduces to

$$C_{OUT} \cong \frac{\Delta I_L}{8 \Delta V_{OUT} \times f_{SW}}$$

Make sure that the ripple current rating of the output capacitors is greater than the maximum inductor ripple current.

During a load step transient on the output, for instance, when the load is suddenly increased, the output capacitor supplies the load until the control loop has a chance to ramp the inductor current. This initial output voltage deviation results in a voltage droop or undershoot. The output capacitance, assuming 0 ESR, required to satisfy the voltage droop requirement can be approximated by

$$C_{OUT} \cong \frac{\Delta I_{STEP}}{\Delta V_{DROOP} \times f_{SW}}$$

where:
ΔI_{STEP} is the step load.
ΔV_{DROOP} is the voltage droop at the output.

When a load is suddenly removed from the output, the energy stored in the inductor rushes into the capacitor, causing the output to overshoot. The output capacitance required to satisfy the output overshoot requirement can be approximated by

$$C_{OUT} \cong \frac{\Delta I_{STEP}{}^2 L}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}{}^2}$$

where:
$\Delta V_{OVERSHOOT}$ is the overshoot voltage during the step load.

Select the largest output capacitance given by any of the previous three equations.

MOSFET SELECTION

The choice of MOSFET directly affects the dc-to-dc converter performance. A MOSFET with low on resistance reduces I^2R losses, and low gate charge reduces transition losses. The MOSFET should have low thermal resistance to ensure that the power dissipated in the MOSFET does not result in excessive MOSFET die temperature.

The high-side MOSFET carries the load current during on time and usually carries most of the transition losses of the converter. Typically, the lower the on resistance of the MOSFET, the higher the gate charge and vice versa. Therefore, it is important to choose a high-side MOSFET that balances the two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C \cong (I_{LOAD})^2 \times R_{DSON}\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where:
R_{DSON} is the MOSFET on resistance.

The gate charging loss is approximated by the equation

$$P_G \cong V_{PV} \times Q_G \times f_{SW}$$

where
V_{PV} is the gate driver supply voltage.
Q_G is the MOSFET total gate charge.

Note that the gate charging power loss is not dissipated in the MOSFET but rather in the ADP1877 internal drivers. This power loss should be taken into consideration when calculating the overall power efficiency.

The high-side MOSFET transition loss is approximated by the equation

$$P_T \cong \frac{V_{IN} \times I_{LOAD} \times (t_R + t_F) \times f_{SW}}{2}$$

where:
P_T is the high-side MOSFET switching loss power.
t_R is the rise time in charging the high-side MOSFET.
t_F is the fall time in discharging the high-side MOSFET.

t_R and t_F can be estimated by

$$t_R \cong \frac{Q_{GSW}}{I_{DRIVER\_RISE}}$$

$$t_F \cong \frac{Q_{GSW}}{I_{DRIVER\_FALL}}$$

where:
Q_{GSW} is the gate charge of the MOSFET during switching and is given in the MOSFET data sheet.
I_{DRIVER_RISE} and I_{DRIVER_FALL} are the driver current put out by the ADP1877 internal gate drivers.

If Q_{GSW} is not given in the data sheet, it can be approximated by

$$Q_{GSW} \cong Q_{GD} + \frac{Q_{GS}}{2}$$

where:
Q_{GD} and Q_{GS} are the gate-to-drain and gate-to-source charges given in the MOSFET data sheet.

I_{DRIVER_RISE} and I_{DRIVER_FALL} can be estimated by

$$I_{DRIVER\_RISE} \cong \frac{V_{DD} - V_{SP}}{R_{ON\_SOURCE} + R_{GATE}}$$

$$I_{DRIVER\_FALL} \cong \frac{V_{SP}}{R_{ON\_SINK} + R_{GATE}}$$

where:
V_{DD} is the input supply voltage to the driver and is between 2.75 V and 5 V, depending on the input voltage.
V_{SP} is the switching point where the MOSFET fully conducts; this voltage can be estimated by inspecting the gate charge graph given in the MOSFET data sheet.
R_{ON_SOURCE} is the on resistance of the ADP1877 internal driver, given in Table 1, when charging the MOSFET.
R_{ON_SINK} is the on resistance of the ADP1877 internal driver, given in Table 1, when discharging the MOSFET.
R_{GATE} is the on gate resistance of MOSFET given in the MOSFET data sheet. If an external gate resistor is added, add this external resistance to R_{GATE}.

The total power dissipation of the high-side MOSFET is the sum of conduction and transition losses:

$$P_{HS} \cong P_C + P_T$$

The synchronous rectifier, or low-side MOSFET, carries the inductor current when the high-side MOSFET is off. The low-side MOSFET transition loss is small and can be neglected in the calculation. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time. Therefore, to achieve high efficiency, it is critical to optimize the low-side MOSFET for low on resistance. In cases where the power loss exceeds the MOSFET rating or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET conduction power loss is

$$P_{CLS} \cong (I_{LOAD})^2 \times R_{DSON}\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

There is also additional power loss during the time, known as dead time, between the turn-off of the high-side switch and the turn-on of the low-side switch, when the body diode of the low-side MOSFET conducts the output current. The power loss in the body diode is given by

$$P_{BODYDIODE} = V_F \times t_D \times f_{SW} \times I_O$$

where:
V_F is the forward voltage drop of the body diode, typically 0.7 V.
t_D is the dead time in the ADP1877, typically 30 ns when driving some medium-size MOSFETs with input capacitance of approximately 3 nF.

Then the power loss in the low-side MOSFET is

$$P_{LS} = P_{CLS} + P_{BODYDIODE}$$

Note that MOSFET, R_{DSON}, increases with increasing temperature with a typical temperature coefficient of 0.4%/°C. The MOSFET junction temperature rise over the ambient temperature is

$$T_J = T_A + \theta_{JA} \times P_D$$

where:
θ_{JA} is the thermal resistance of the MOSFET package.
T_A is the ambient temperature.
P_D is the total power dissipated in the MOSFET.

LOOP COMPENSATION

As with most current mode step-down controller, a transconductance error amplifier is used to stabilize the external voltage loop. Compensating the ADP1877 is fairly easy; an RC compensator is needed between COMP and AGND. Figure 34 shows the configuration of the compensation components: R_{COMP}, C_{COMP}, and CC2. Because C_{C2} is very small compared to C_{COMP}, to simplify calculation, C_{C2} is ignored for the stability compensation analysis.

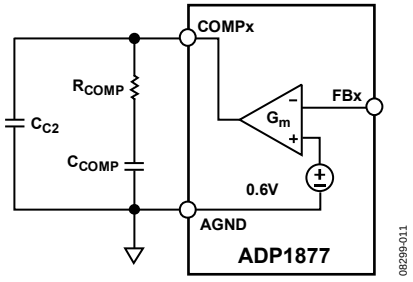


Figure 34. Compensation Components

The open loop gain transfer function at angular frequency, s, is given by

$$H(s) = G_m \times G_{CS} \times \frac{V_{REF}}{V_{OUT}} \times Z_{COMP}(s) \times Z_{FILTER}(s) \quad (1)$$

where:
G_m is the transconductance of the error amplifer, 500 µs.
G_{CS} is the tranconductance of the current sense amplifier.
Z_{COMP} is the impedance of the compensation network.
Z_{FILTER} is the impedance of the output filter.
V_{REF} = 0.6 V

G_{CS} with units of A/V is given by

$$G_{CS} = \frac{1}{A_{CS} \times R_{DSON\_MIN}} \quad (2)$$

where:
A_{CS} is the current sense gain of either 3 V/V, 6 V/V, 12 V/V, or 24 V/V set by the gain resistor between DL and PGND.
R_{DSON_MIN} is the the low-side MOSFET minimum on resistance.

Because the zero produced by the ESR of the output capacitor is not needed to stabilize the control loop, the ESR is ignored for analysis. Then Z_{FILTER} is given by

$$Z_{FILTER} = \frac{1}{sC_{OUT}} \quad (3)$$

Because C_{C2} is very small relative to C_{COMP}, Z_{COMP} can be written as

$$Z_{COMP} = R_{COMP} + \frac{1}{sC_{COMP}} = \frac{1 + sR_{COMP} \times C_{COMP}}{sC_{COMP}} \quad (4)$$

At the crossover frequency, the open loop transfer function is unity of 0 dB, H (f_{CROSS}) = 1. Combining Equation 1 and Equation 3, Z_{COMP} at the crossover frequency can be written as

$$Z_{COMP}(f_{CROSS}) = \left(\frac{2\pi \times f_{CROSS}}{G_m \times G_{CS}}\right)\left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (5)$$

The zero produced by R_{COMP} and C_{COMP} is

$$f_{ZERO} = \frac{1}{2\pi R_{COMP} \times C_{COMP}} \quad (6)$$

At the crossover frequency, Equation 4 can be shown as

$$Z_{COMP}(f_{CROSS}) = R_{COMP} \times \frac{f_{CROSS} + f_{ZERO}}{f_{CROSS}} \quad (7)$$

Combining Equation 5 and Equation 7 and solving for R_{COMP} gives

$$R_{COMP} = \frac{f_{CROSS}}{f_{CROSS} + f_{ZERO}} \times \left(\frac{2\pi \times f_{CROSS}}{G_m \times G_{CS}}\right) \times \left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (8)$$

Choose the crossover and zero frequencies as follows:

$$f_{CROSS} = \frac{f_{SW}}{13} \quad (9)$$

$$f_{ZERO} = \frac{f_{CROSS}}{5} = \frac{f_{SW}}{65} \quad (10)$$

Substituting Equation 2, Equation 9, and Equation 10 into Equation 8 yields

$$R_{COMP} = 0.83 \times A_{CS} \times R_{DSON} \left(\frac{2\pi \times f_{CROSS}}{G_m}\right) \times \left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (11)$$

where:
G_m is the transconductance of the error amplifer, 500 µs.
A_{CS} is the current sense gain of 3 V/V, 6 V/V, 12 V/V or 24 V/V.
R_{DSON} is on resistance of the low-side MOSFET.
V_{REF} = 0.6 V

And combining Equation 6 and Equation 10 yields

$$C_{COMP} = \frac{2}{\pi R_{COMP} \times f_{CROSS}} \quad (12)$$

And lastly set C_{C2} to

$$\frac{1}{20} \times C_{COMP} \le C_{C2} \le \frac{1}{10} \times C_{COMP} \quad (13)$$

SWITCHING NOISE AND OVERSHOOT REDUCTION

In any high speed step-down regulator, high frequency noise (generally in the range of 50 MHz to 100 MHz) and voltage overshoot are always present at the gate, the switch node (SW), and the drains of the external MOSFETs. The high frequency noise and overshoot are caused by the parasitic capacitance, C_{GD}, of the external MOSFET and the parasitic inductance of the gate trace and the packages of the MOSFETs. When the high current is switched, electromagnetic interference (EMI) is generated, which can affect the operation of the surrounding circuits. To reduce voltage ringing and noise, it is required to add an RC snubber between SW and PGND for applications with more than 10 A output current, as illustrated in Figure 35. Snubbers may also be needed in applications where the duty cycle in one of the channels is higher than or equal to 50%. In most applications, R_{SNUB} is typically 2 Ω to 4 Ω, and C_{SNUB} typically 1.2 nF to 3 nF.

R_{SNUB} can be estimated by

$$R_{SNUB} \cong 2\sqrt{\frac{L_{MOSFET}}{C_{OSS}}}$$

And C_{SNUB} can be estimated by

$$C_{SNUB} \cong C_{OSS}$$

where:

L_{MOSFET} is the total parasitic inductance of the high-side and low-side MOSFETs, typically 3 nH, and is package dependent.

C_{OSS} is the total output capacitance of the high-side and low-side MOSFETs given in the MOSFET data sheet.

The size of the RC snubber components need to be chosen correctly to handle the power dissipation. The power dissipated in R_{SNUB} is

$$P_{SNUB} = V_{IN}^{2} \times C_{SNUB} \times f_{SW}$$

In most applications, a component size 0805 for R_{SNUB} is sufficient. However, the use of an RC snubber reduces the overall efficiency, generally by an amount in the range of 0.1% to 0.5%. The RC snubber cannot reduce the voltage overshoot. A resistor, shown as R_{RISE} in Figure 35, at the BSTx pin helps to reduce overshoot and is generally between 2 Ω and 4 Ω. Adding a resistor in series, typically between 2 Ω and 4 Ω, with the gate driver also helps to reduce overshoot. If a gate resistor is added, then R_{RISE} is not needed.

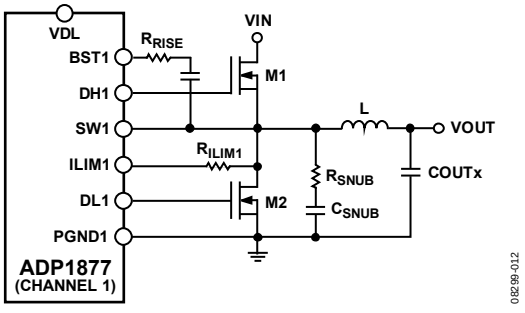


Figure 35. Application Circuit with a Snubber

VOLTAGE TRACKING

The ADP1877 includes a tracking feature that tracks a master voltage. This feature is especially important when the ADP1877 is powering separate power supply voltages on a single integrated circuit, such as the core and I/O voltages of a DSP or microcontroller. In these cases, improper sequencing can cause damage to the load.

In all tracking configurations, the output can be set as low as 0.6 V for a given operating condition. The soft start time setting of the master voltage should be longer than the soft start of the slave voltage. This forces the rise time of the master voltage to be imposed on the slave voltage. If the soft start setting of the slave voltage is longer, the slave comes up more slowly, and the tracking relationship is not seen at the output.

Two tracking configurations are possible with the ADP1877: coincident and ratiometric trackings. Full time DDR termination is not recommended when using these tracking features.

COINCIDENT TRACKING

The most common application is coincident tracking, used in core vs. I/O voltage sequencing and similar applications. Coincident tracking limits the slave output voltage to be the same as the master voltage until it reaches regulation. Connect the slave TRK input to a resistor divider from the master voltage that is the same as the divider used on the slave FB pin. This forces the slave voltage to be the same as the master voltage. For coincident tracking, use $R_{TRKT} = R_{TOP}$ and $R_{TRKB} = R_{BOT}$, as shown in Figure 37.

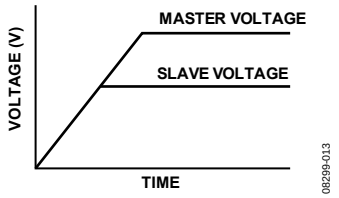


Figure 36. Coincident Tracking

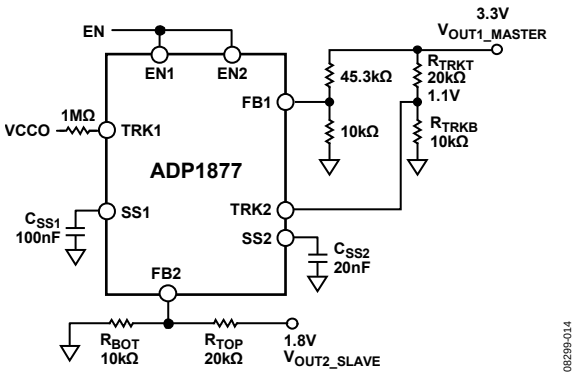


Figure 37. Example of a Coincident Tracking Circuit

The ratio of the slave output voltage to the master voltage is a function of the two dividers.

$$\frac{V_{OUT\_SLAVE}}{V_{OUT\_MASTER}} = \frac{\left(1+\frac{R_{TOP}}{R_{BOT}}\right)}{\left(1+\frac{R_{TRKT}}{R_{TRKB}}\right)}$$

As the master voltage rises, the slave voltage rises identically. Eventually, the slave voltage reaches its regulation voltage, where the internal reference takes over the regulation while the TRKx input continues to increase and thus removes itself from influencing the output voltage.

To ensure that the output voltage accuracy is not compromised by the TRKx pin being too close in voltage to the 0.6 V reference, make sure that the final value of the TRKx voltage of the slave channel is at least 0.7 V.

RATIOMETRIC TRACKING

Ratiometric tracking limits the output voltage to a fraction of the master voltage. For ratiometric tracking, the simplest configuration is to tie the TRK pin of the slave channel to the FBx pin of the master channel. However, because of the large internal offset between TRKx and FBx, this ratiometric tracking configuration is not recommended. A tracking configuration that requires the TRKx voltage of the slave channel below 0.6 V is not recommended because of the large internal TRKx to FBx offset voltage.

Another ratiometric tracking configuration is having the slave channel rise more quickly than the master channel, as shown in Figure 38 and Figure 39. The tracking circuits in Figure 37 and Figure 38 are virtually identical with the exception that RTRKB > RTRKT, as shown in Figure 38.

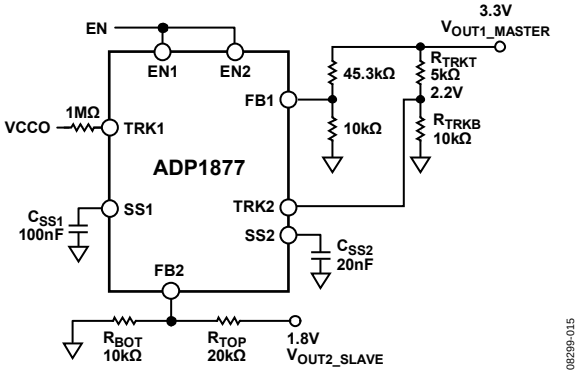


Figure 38. A Simple Ratiometric Tracking Circuit (Slave Channel Has a Faster Ramp Rate)

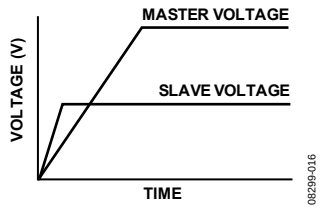


Figure 39. Ratiometric Tracking (Slave Channel Has a Faster Ramp Rate)

PCB LAYOUT GUIDELINE

In any switching converter, there are some circuit paths that carry high dI/dt, which can create spikes and noise. Some circuit paths are sensitive to noise, while other circuits carry high dc current and can produce significant IR voltage drops. The key to proper PCB layout of a switching converter is to identify these critical paths and arrange the components and the copper area accordingly. When designing PCB layouts, be sure to keep high current loops small. In addition, keep compensation and feedback components away from the switch nodes and their associated components.

The following is a list of recommended layout practices for the synchronous buck controller, arranged by decreasing order of importance.

MOSFETS, INPUT BULK CAPACITOR, AND BYPASS CAPACITOR

The current waveform in the top and bottom FETs is a pulse with very high dI/dt; therefore, the path to, through, and from each individual FET should be as short as possible, and the two paths should be commoned as much as possible. In designs that use a pair of D-Pak or a pair of SO-8 FETs on one side of the PCB, it is best to counter-rotate the two so that the switch node is on one side of the pair, and the high-side drain can be bypassed to the low side source with a suitable ceramic bypass capacitor, placed as close as possible to the FETs. This minimizes the inductance around this loop through the FETs and capacitor. The recommended bypass ceramic capacitor values range from 1 µF to 22 µF, depending upon the output current. This bypass capacitor is usually connected to a larger value bulk filter capacitor and should be grounded to the PGNDx plane.

HIGH CURRENT AND CURRENT SENSE PATHS

Part of the ADP1877 architecture is sensing the current across the low-side FET between the SWx and PGNDx pins. The switching GND currents of one channel creates noise and can be picked up by the other channel. It is essential to keep the SW1/SW2 and PGND1/PGND2 traces as short as possible and placed very close to the FETs to achieve accurate current sensing. The following schematic illustrates the proper connection technique for the SW1/SW2, PGND1/PGND2, and PGNDx plane. Note that PGND1 and PGND2 are only jointed at the PGND plane.

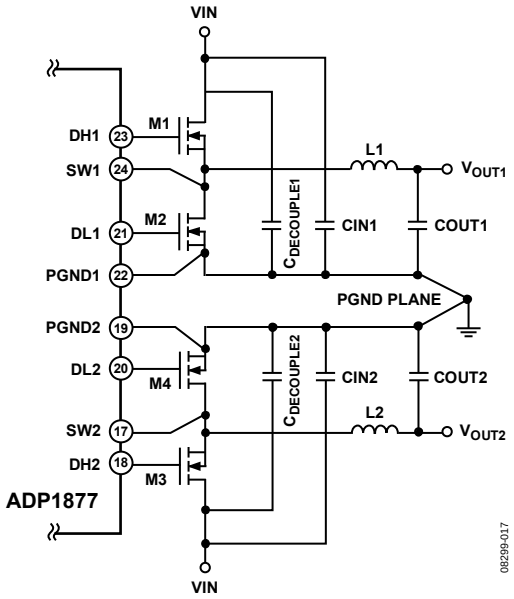


Figure 40. Grounding Technique for Two Channels

SIGNAL PATHS

The negative terminals of AGND, VIN bypass, compensation components, soft start capacitor, and the bottom end of the output feedback divider resistors should be tied to an almost isolated small AGND plane. These connections should attach from their respective pins to the AGND plane; these connections should be as short as possible. No high current or high dI/dt signals should be connected to this AGND plane. The AGND area should be connected through one wide trace to the negative terminal of the output filter capacitors.

PGND PLANE

The PGNDx pin handles a high dI/dt gate drive current returning from the source of the low side MOSFET. The voltage at this pin also establishes the 0 V reference for the overcurrent limit protection function and the ILIMx pin. A PGND plane should connect the PGNDx pin and the VDL bypass capacitor, 1 µF, through a wide and direct path to the source of the low side MOSFET. The placement of CIN is critical for controlling ground bounce. The negative terminal of CIN must be placed very close to the source of the low-side MOSFET.

FEEDBACK AND CURRENT-LIMIT SENSE PATHS

Avoid long traces or large copper areas at the FBx and ILIMx pins, which are low signal level inputs that are sensitive to capacitive and inductive noise pickup. It is best to position any series resistors and capacitors as close as possible to these pins. Avoid running these traces close and/or parallel to high dI/dt traces.

SWITCH NODE

The switch node is the noisiest place in the switcher circuit with large ac and dc voltages and currents. This node should be wide to keep resistive voltage drop down. To minimize the generation of capacitively coupled noise, the total area should be small. Place the FETs and inductor close together on a small copper plane to minimize series resistance and keep the copper area small.

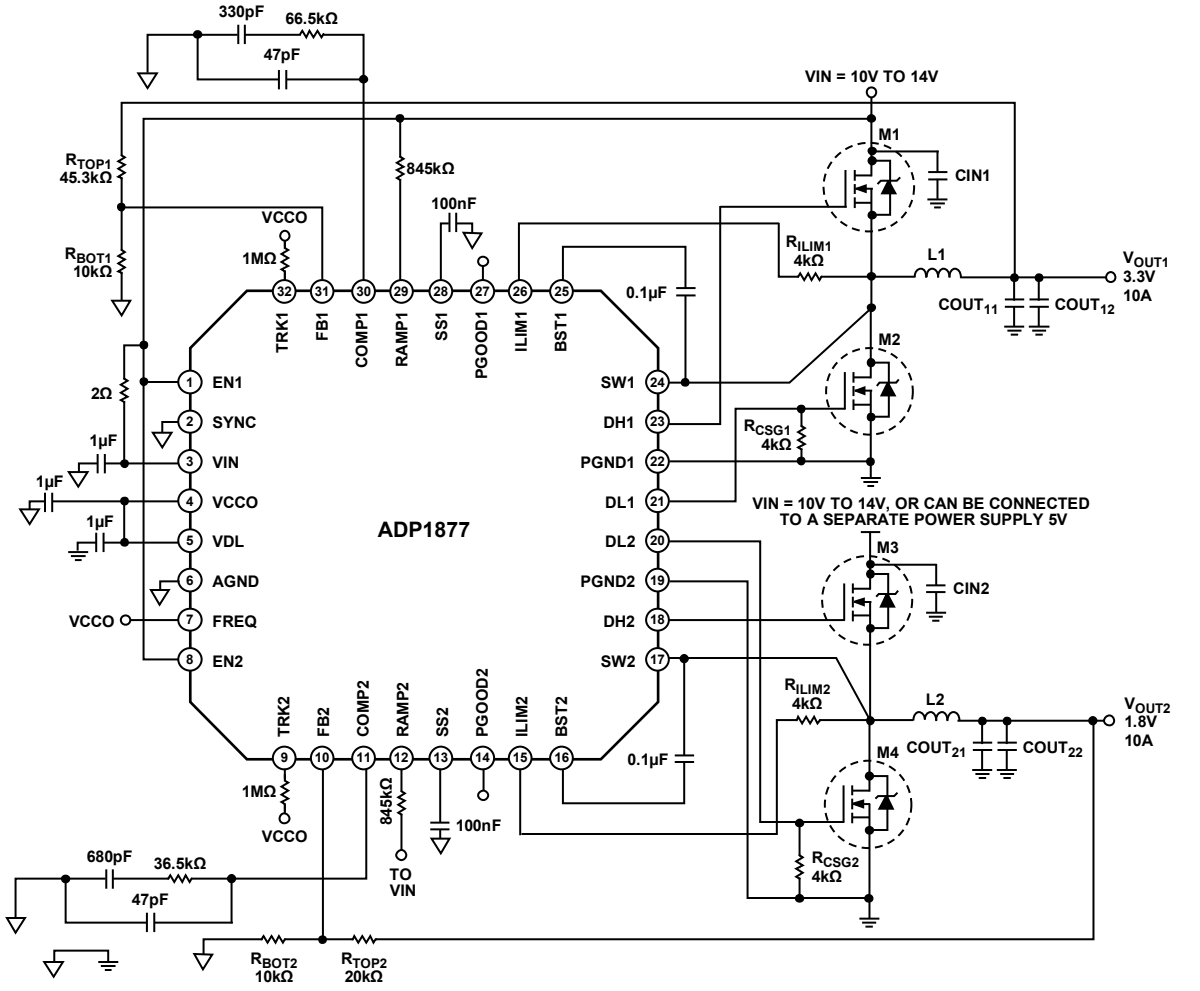
GATE DRIVER PATHS

Gate drive traces (DH and DL) handle high dI/dt and tend to produce noise and ringing. They should be as short and direct as possible. If possible, avoid using feedthrough vias in the gate drive traces. If vias are needed, it is best to use two relatively large ones in parallel to reduce the peak current density and the current in each via. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can be very helpful to reduce noise and ringing. It is occasionally helpful to place small value resistors, such as between 2 Ω and 4 Ω, on the DH and DL pins. These can be populated with 0 Ω resistors if resistance is not needed. Note that the added gate resistance increases the switching rise and fall times as well as switching power loss in the MOSFET.

OUTPUT CAPACITORS

The negative terminal of the output filter capacitors should be tied close to the source of the low side FET. Doing this helps to minimize voltage differences between AGND and PGNDx.

TYPICAL OPERATING CIRCUITS

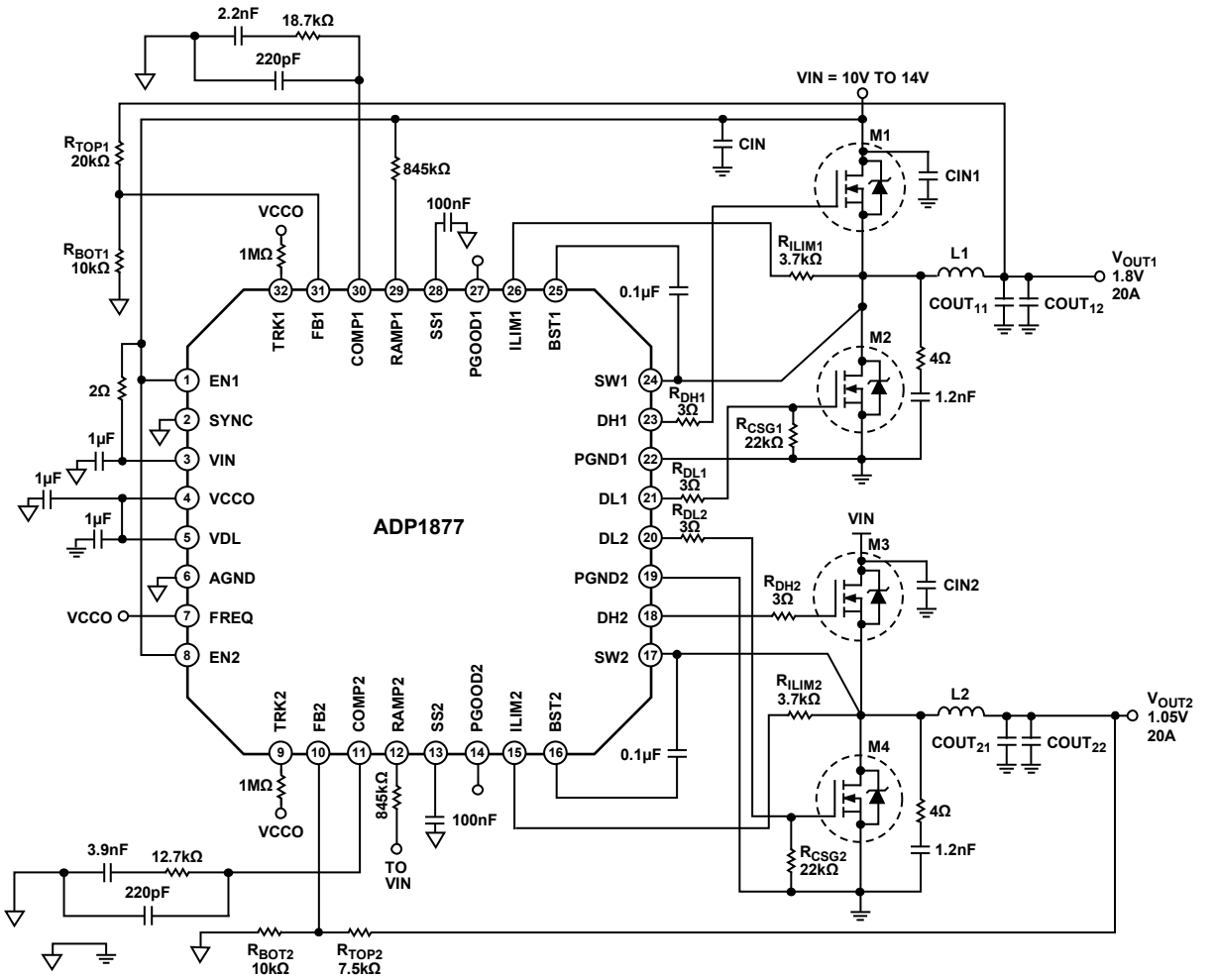


f_{SW} = 600kHz
L1, L2: 1.2µH, WURTH ELEKTRONIK, 744325120
M1, M2, M3, M4: IRLR7821

CIN1, CIN2: 10µF/X7R/25V/1210 × 2, GRM32DR71E106KA12, MURATA
$COUT_{11}$, $COUT_{21}$: 330µF/6.3V/POSCAP × 2, 6TPF330M9L, SANYO
$COUT_{12}$, $COUT_{22}$: 22µF/X5R/0805/6.3V, GRM21BR60J226ME39, MURATA

08299-019

Figure 41. Typical Medium Current Operating Circuit

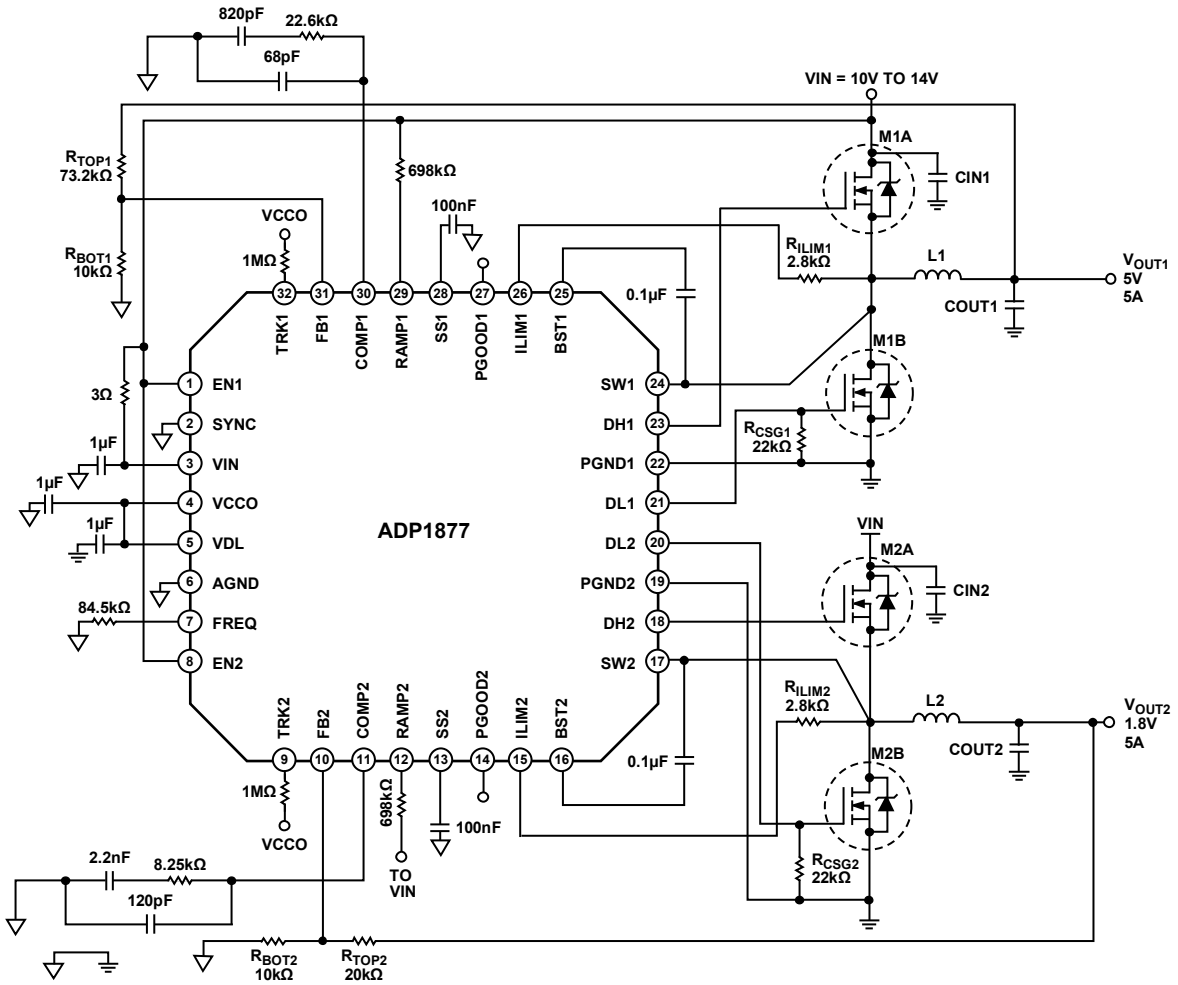


f_{SW} = 300kHz
CIN = 180µF/20V, 20SP180M, OSCON, SANYO
L1, L2: 1.3µH, WURTH ELEKTRONIK, 7443551130
M1, M3: BSC080N03LS
M2, M4: BSC030N03LS

CIN1, CIN2: 10µF/X7R/25V/1210 × 2, GRM32DR71E106KA12, MURATA
$COUT_{11}$, $COUT_{21}$: 680µF/2.5V/POSCAP × 2, 2R5TPD680M5, SANYO
$COUT_{12}$, $COUT_{22}$: 22µF/X5R/0805/6.3V × 3, GRM21BR60J226ME39, MURATA

08299-020

Figure 42. Typical 20 A Operating Circuit

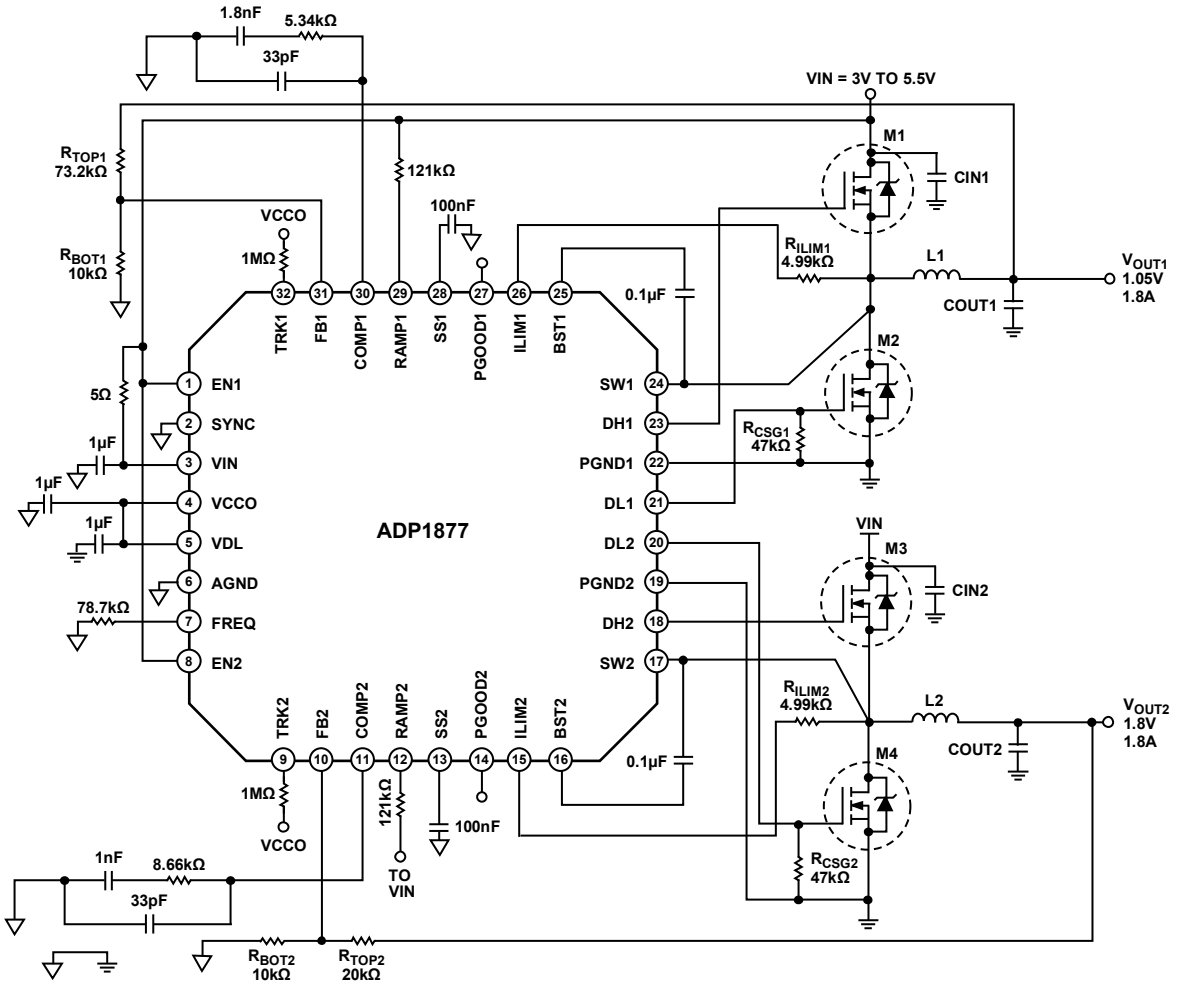


f_{SW} = 750kHz
L1: 2µH, 744310200, WURTH ELEKTRONIK
L2: 1.15µH, 744310115, WURTH ELEKTRONIK

CIN1, CIN2: 10µF/X5R/16V/1206 × 2, GRM31CR61C106KA88, MURATA
M1, M2: Si4944DY OR BSON03MD
COUT1: 22µF/X5R/1210/6.3V × 3, GRM32DR60J226KA01, MURATA
COUT2: 22µF/X5R/1210/6.3V × 3, GRM32DR60J226KA01, MURATA

08299-021

Figure 43. Typical Low Current Operating Circuit



f_{SW} = 800kHz
L1, L2: 1µH, D62LCB1R0M, TOKO

CIN1, CIN2: 4.7µF/X5R/16V/0805 × 2, GRM219R60J475KE19, MURATA
M1, M2, M3, M4: Si2302ADS, SOT23
COUT1, COUT2: 22µF/X5R/0805/6.3V, GRM21BR60J226ME39, MURATA

Figure 44. Typical Low Current Application with V_{IN} < 5.5 V

OUTLINE DIMENSIONS

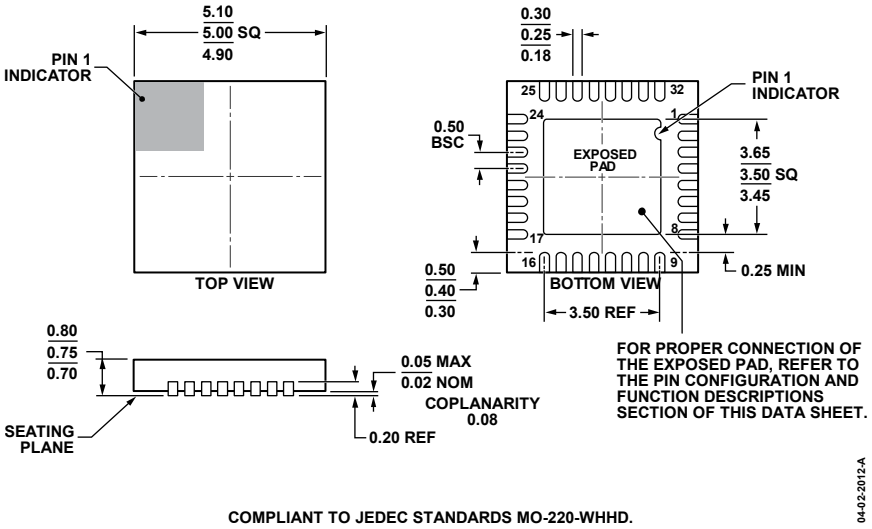


Figure 45. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1877ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
ADP1877HC-EVALZ		Evaluation Board with 13 A Output	

[1] Z = RoHS Compliant Part.

NOTES

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