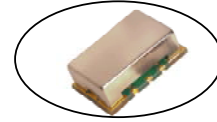


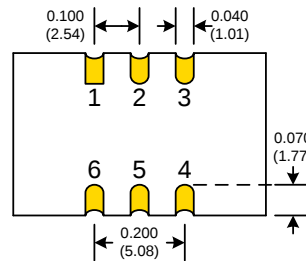
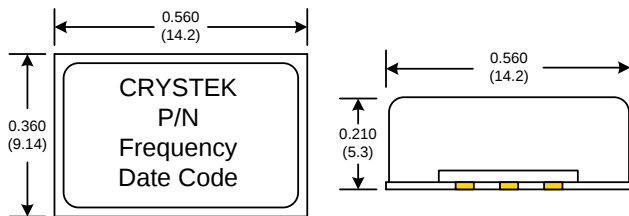
CVPD-920 Model

9X14 mm SMD, 3.3V, LVPECL

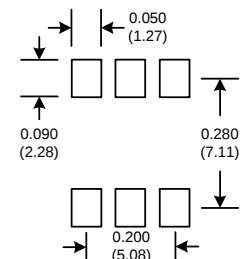
Frequency Range:	50MHz to 125MHz
Frequency Pulling:	±20ppm APR Min
Temperature Range:	0°C to 70°C
	(Option X)
	-40°C to 85°C
Storage:	-55°C to 120°C
Input Voltage:	3.3V ±0.3V
Control Voltage:	1.65V ±1.65V
Input Current:	88mA Max
Output:	Differential LVPECL
Symmetry:	45/55% Max @ 50% Vcc
Rise/Fall Time:	1ns Max @ 20% to 80% Vcc
Linearity:	±10% Max
Logic:	Terminated to Vcc-2V into 50 ohms
	"0" = Vcc-1.85V Min, Vcc-1.62V Max
	"1" = Vcc-1.02V Min, Vcc-0.81V Max
Disable Time:	200ns
Start-up Time:	1ms Typ., 2ms Max
Phase Jitter:	12KHz to 80MHz 0.5psec Typ., 1psec RMS Max
Phase Noise:	10Hz -65dBc/Hz Typical
	100Hz -98dBc/Hz Typical
	1KHz -125dBc/Hz Typical
	10KHz -140dBc/Hz Typical
	100KHz -145dBc/Hz Typical
Aging:	<3ppm 1st/yr, <1ppm every year thereafter



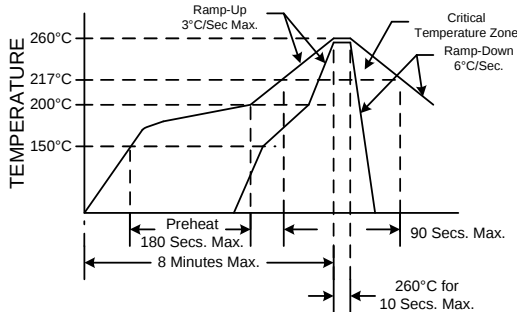
Designed to meet today's requirements for 3.3V Differential LVPECL applications. The CVPD-920 is produced using our cost saving FR5 PCB and UM-1 overtone crystal technology. This design offers considerable cost savings over other HFF VCXO products when broad frequency pulling is not required. Also available in 14 pin dip fully hermetic package.



SUGGESTED PAD LAYOUT



RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.

PIN	Function
1	Control Volt
2	E/D
3	GND
4	OUT
5	COU
6	Vcc

Crystek Part Number Guide

CVPD-920 X - 100.000

#1	#2	#3	#4
#1 Crystek 9x14 SMD PECL VCXO			
#2 Model 920			
#3 Temp. Range: Blank = 0/70°C, X=-40/85°C			
#4 Frequency in MHz: 3 or 6 decimal places			

Example:

CVPD-920X-25-100.000 = 3.3V, 45/55, -40/85°C, 25ppm, 100.000 MHz

Enable/Disable Function

Pin 2	Output Pin
Open	Active
"0" level Vcc-1.620V Max	Active
"1" level Vcc-1.025V Min	Disabled
Disabled State:	
Pin 4 will assume a fixed level of logic "0"	
Pin 5 will assume a fixed level of logic "1"	

Specifications subject to change without notice.

TD-030701 Rev. D