

# 74LVC07A-Q100

## Hex buffer with open-drain outputs

Rev. 2 — 14 December 2018

Product data sheet

## 1. General description

The 74LVC07A-Q100 provides six non-inverting buffers. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 5 V tolerant inputs and outputs (open-drain) for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF; R = 0 Ω)

## 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74LVC07AD-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm		SOT108-1
74LVC07APW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin small outline package; 14 leads; body width 4.4 mm		SOT402-1
74LVC07ABQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm		SOT762-1

## 4. Functional diagram

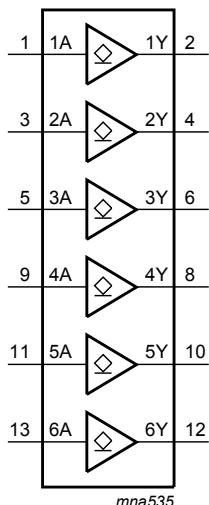


Fig. 1. Logic symbol

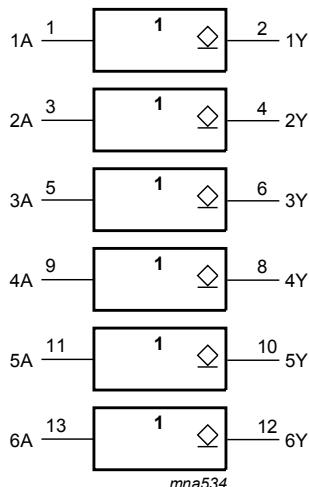


Fig. 2. IEC logic symbol

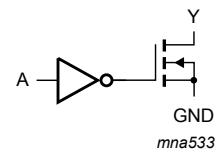


Fig. 3. Logic diagram for one gate

## 5. Pinning information

### 5.1. Pinning

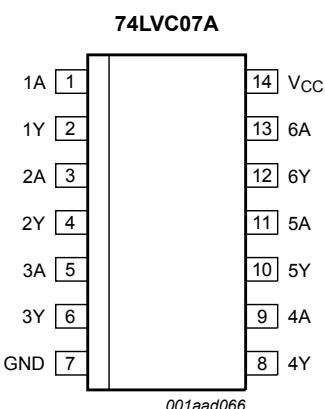
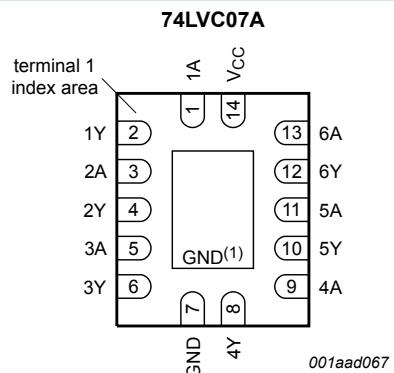


Fig. 4. Pin configuration for SO14 and TSSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig. 5. Pin configuration for DHVQFN14

## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
nA	nY
L	L
H	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA	
V <sub>I</sub>	input voltage		[1]	-0.5	+6.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA	
V <sub>O</sub>	output voltage	active mode	[2]	-0.5	+6.5	V
		high-impedance mode	[2]	-0.5	+6.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	50	mA	
I <sub>CC</sub>	supply current		-	100	mA	
I <sub>GND</sub>	ground current		-100	-	mA	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[3]	-	500	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C	

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C derates linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
		functional	1.2	-	-	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	active mode	0	-	5.5	V
		high-impedance mode	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2 \text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$	-	-	$0.7 \times V_{CC}$	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2 \text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	$0.30 \times V_{CC}$	-	$0.30 \times V_{CC}$	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = 100 \mu\text{A}$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.20	-	0.3	V
		$I_O = 4 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.6	V
		$I_O = 8 \text{ mA}$ ; $V_{CC} = 2.3 \text{ V}$	-	-	0.3	-	0.75	V
		$I_O = 12 \text{ mA}$ ; $V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
		$I_O = 32 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	-	-	0.55	-	0.8	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ ; $V_O = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	$\pm 0.1$	$\pm 10$	-	$\pm 20$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5 \text{ V}$ ; $V_{CC} = 0 \text{ V}$	-	$\pm 0.1$	$\pm 10$	-	$\pm 20$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	0.1	10	-	40	$\mu\text{A}$

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.7$ V to 5.5 V	-	5	500	-	5000	μA
$C_I$	input capacitance	$V_{CC} = 0$ V to 5.5 V; $V_I = GND$ to $V_{CC}$	-	5.0	-	-	-	pF

[1] All typical values are measured at  $V_{CC} = 3.3$  V (unless stated otherwise) and  $T_{amb} = 25$  °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Fig. 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{PLZ}$	OFF-state to LOW propagation delay	nA to nY; see <a href="#">Fig. 6</a>						
		$V_{CC} = 1.2$ V	-	8.0	-	-	-	ns
		$V_{CC} = 1.65$ V to 1.95 V	0.5	1.7	5.5	0.5	6.5	ns
		$V_{CC} = 2.3$ V to 2.7 V	0.5	1.2	2.8	0.5	3.5	ns
		$V_{CC} = 2.7$ V	0.5	1.8	3.3	0.5	4.5	ns
		$V_{CC} = 3.0$ V to 3.6 V	0.5	1.2	3.6	0.5	4.5	ns
		$V_{CC} = 4.5$ V to 5.5 V	0.5	1.6	2.6	0.5	3.5	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	nA to nY; see <a href="#">Fig. 6</a>						
		$V_{CC} = 1.2$ V	-	10	-	-	-	ns
		$V_{CC} = 1.65$ V to 1.95 V	0.5	3.0	5.5	0.5	6.5	ns
		$V_{CC} = 2.3$ V to 2.7 V	0.5	1.7	2.8	0.5	3.5	ns
		$V_{CC} = 2.7$ V	0.5	2.1	3.3	0.5	4.5	ns
		$V_{CC} = 3.0$ V to 3.6 V	0.5	2.5	3.6	0.5	4.5	ns
		$V_{CC} = 4.5$ V to 5.5 V	0.5	1.6	2.6	0.5	3.5	ns
$C_{PD}$	power dissipation capacitance	per buffer; $V_I = GND$ to $V_{CC}$ [2]						
		$V_{CC} = 1.65$ V to 1.95 V	-	6.5	-	-	-	pF
		$V_{CC} = 2.3$ V to 2.7 V	-	6.9	-	-	-	pF
		$V_{CC} = 3.0$ V to 3.6 V	-	7.2	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25$  °C and  $V_{CC} = 1.2$  V, 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

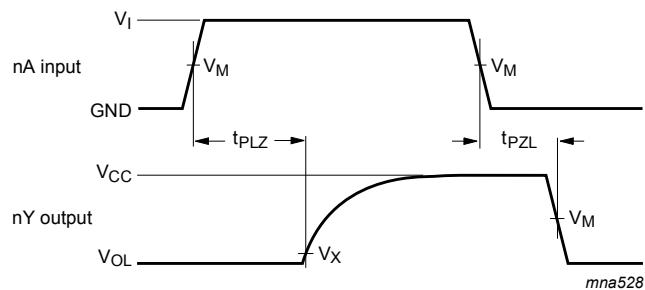
$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in Volts

N = number of inputs switching

$$\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of the outputs}$$

### 10.1. Waveforms and test circuit



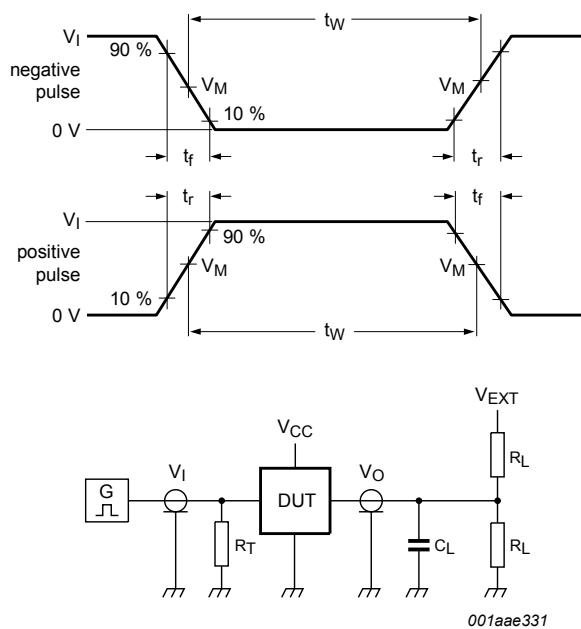
Measurements points are given in [Table 8](#).

Logic level:  $V_{OL}$  is a typical output voltage level that occurs with the output load.

**Fig. 6. The input (nA) to output (nY) propagation delays**

**Table 8. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_X$
< 2.7 V	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$
$\geq 2.7 \text{ V to } 3.6 \text{ V}$	1.5 V	$V_{OL} + 0.3 \text{ V}$
$\geq 4.5 \text{ V to } 5.5 \text{ V}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 7. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

## 11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

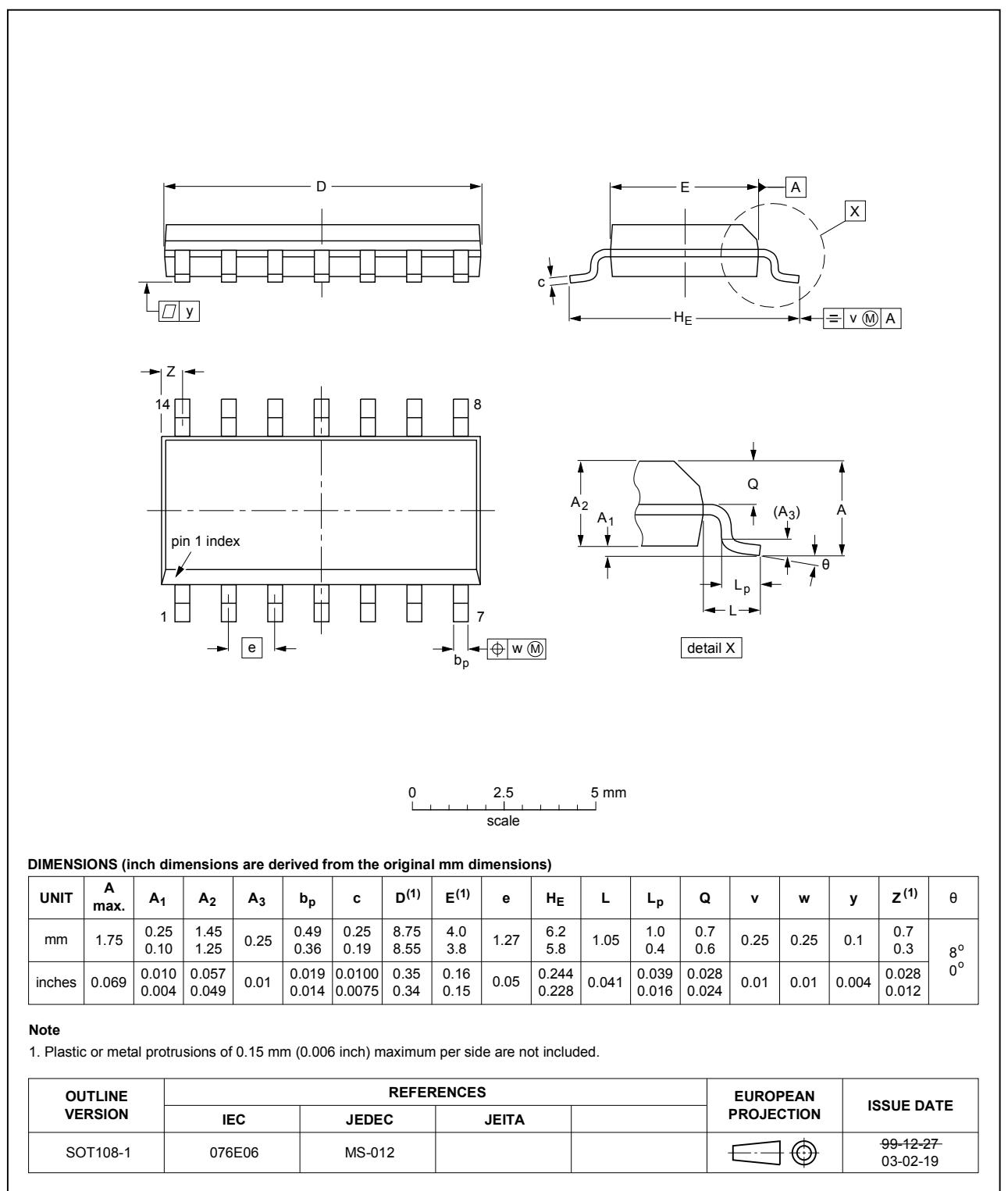
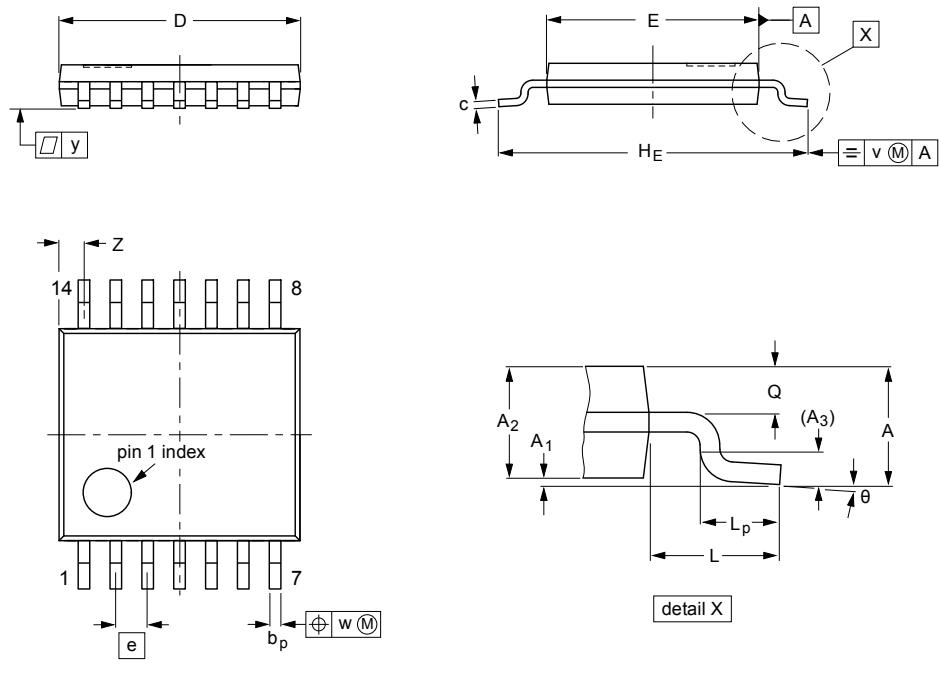


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



## DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1 0.05	0.15 0.80	0.95 0.25	0.25 0.19	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

## Notes

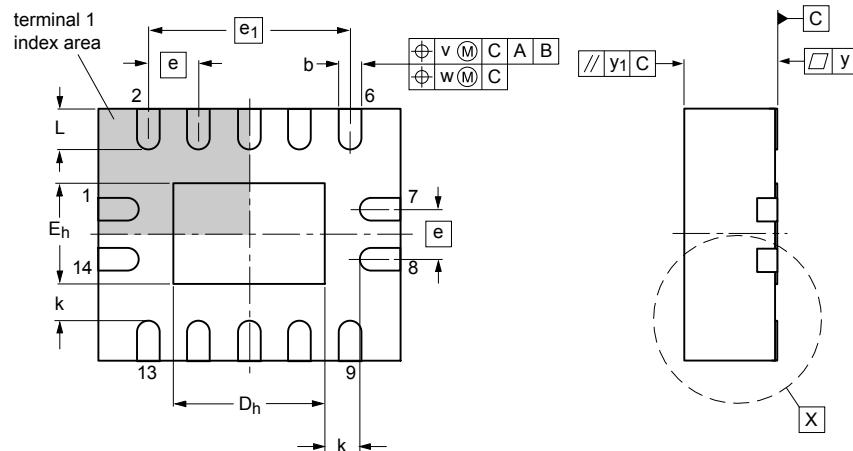
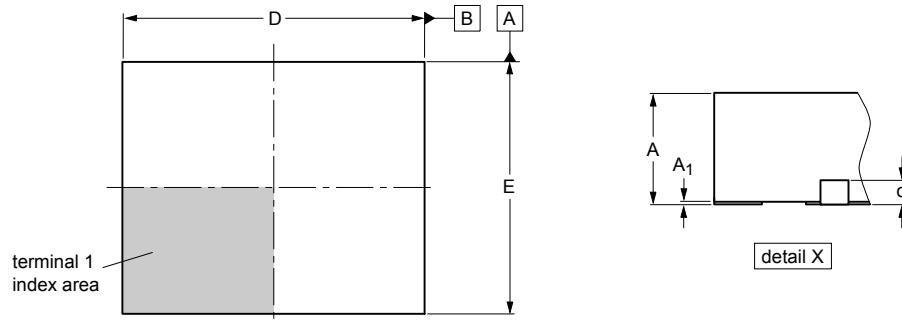
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				-99-12-27 03-02-18

Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



0 2 4 mm  
scale

Dimensions (mm are the original dimensions)

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	k	L	v	w	y	y <sub>1</sub>
mm	max	1	0.05	0.30	3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2	0.4	0.1	0.05	0.05	0.1
mm	min		0.00	0.18	2.9	1.35	2.4	0.85				0.2	0.3			

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1	MO-241					15-04-10 15-05-05

Fig. 10. Package outline SOT762-1 (DHVQFN14)

## 12. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

## 13. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC07A_Q100 v.2	20181214	Product data sheet	-	74LVC07A_Q100 v.1
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li><a href="#">Table 5</a>: Maximum output voltage (active mode) changed from <math>V_{CC}</math> to 5.5 V</li></ul>			
74LVC07A_Q100 v.1	20121001	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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