CBT3257A

Quad 1-of-2 multiplexer/demultiplexer

Rev. 6 — 20 June 2019 Product data sheet

1. General description

The CBT3257A is a quad 1-of-2 high-speed TTL-compatible multiplexer/demultiplexer. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

Output enable ($\overline{OE}$) and select-control (S) inputs select the appropriate nB1 and nB2 outputs for the nA input data.

The CBT3257A is characterized for operation from -40 °C to +85 °C.

2. Features and benefits

- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- Latch-up protection exceeds 100 mA per JEDEC standard JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
CBT3257AD	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3257ADB	-40 °C to +85 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
CBT3257ADS	-40 °C to +85 °C	SSOP16[1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
CBT3257APW	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
CBT3257ABQ	-40 °C to +85 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm	SOT763-1

[1] Also known as QSOP16.

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4. Functional diagram

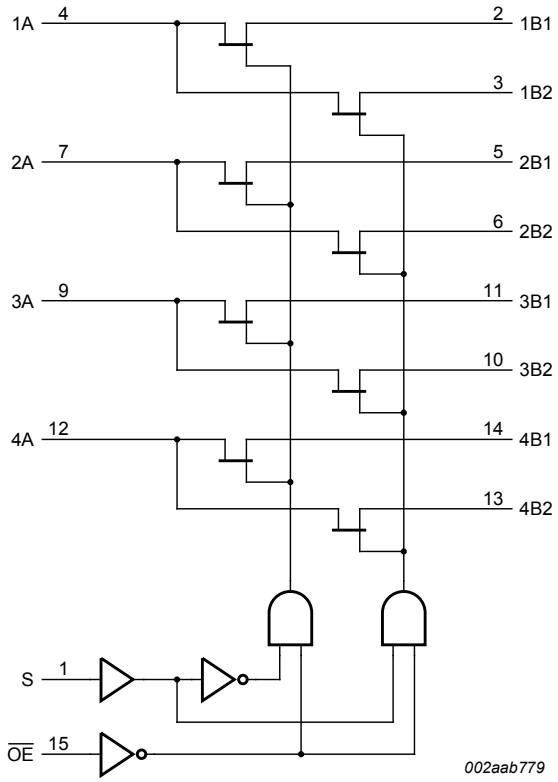


Fig. 1. Logic diagram

5. Pinning information

5.1. Pinning

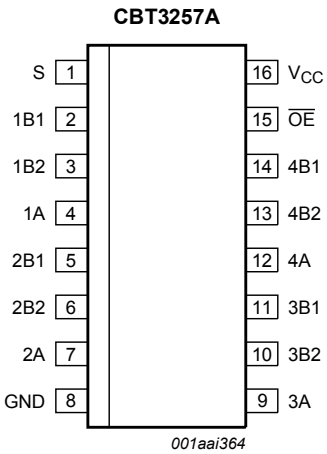


Fig. 2. Pin configuration SOT109-1 (SO16) and SOT519-1 (SSOP16)

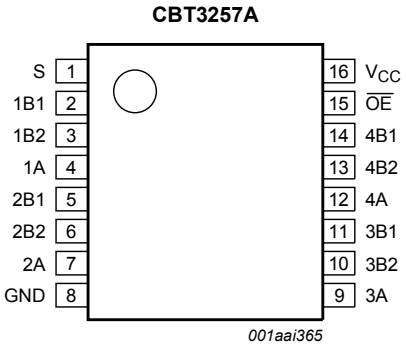
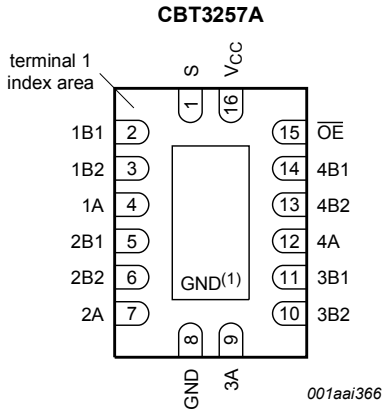


Fig. 3. Pin configuration SOT338-1 (SSOP16) and SOT403-1 (TSSOP16)



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 4. Pin configuration SOT763-1 (DHVQFN16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select control input
1B1, 2B1, 3B1, 4B1,	2, 5, 11, 14	B1 outputs/inputs
1B2, 2B2, 3B2, 4B2	3, 6, 10, 13	B2 outputs/inputs
1A, 2A, 3A, 4A	4, 7, 9, 12	A inputs/outputs
GND	8	ground (0 V)
$\overline{OE}$	15	output enable (active LOW)
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs		Switch
$\overline{OE}$	S	
L	L	nA to nB1
L	H	nA to nB2
H	X	switch off

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
I_{SW}	switch current	continuous current through each switch	-	128	mA

Symbol	Parameter	Conditions	Min	Max	Unit
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C			
		SO16, (T)SSOP16 and DHVQFN16 packages	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
T_{amb}	ambient temperature	operating in free-air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

T_{amb} = -40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = -18 mA	-	-	-1.2	V
V_{pass}	pass voltage	V_I = V_{CC} = 5.0 V; I_O = -100 µA	3.6	3.9	4.2	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	-	±1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	-	3	µA
ΔI_{CC}	additional supply current	per input; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND [2]	-	-	2.5	mA
C_I	input capacitance	control pins; V_I = 3 V or 0 V	-	3.3	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; V_O = 3 V or 0 V; $\overline{OE}$ = V_{CC}	-	9.9	-	pF
		B port; V_O = 3 V or 0 V; $\overline{OE}$ = V_{CC}	-	6.4	-	pF
R_{ON}	ON resistance	V_{CC} = 4.5 V [3]				
		V_I = 0 V; I_I = 64 mA	-	5	7	Ω
		V_I = 0 V; I_I = 30 mA	-	5	7	Ω
		V_I = 2.4 V; I_I = 15 mA	-	10	15	Ω

[1] All typical values are measured at V_{CC} = 5 V; T_{amb} = 25 °C.
[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
[3] Measured by the voltage drop between the nA and the nBn terminals at the indicated current through the switch. The lowest voltage of the two (nA or nBn) terminals determines the ON resistance.

10. Dynamic characteristics

Table 7. Dynamic characteristics

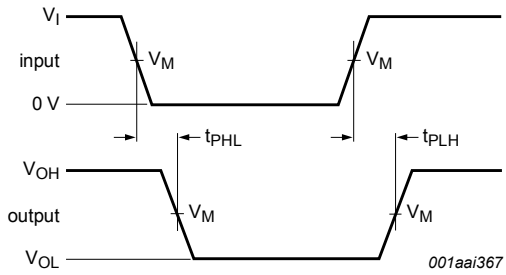
T_{amb} = -40 °C to +85 °C; V_{CC} = 4.5 V to 5.5 V; for test circuit see Fig. 7.

Symbol	Parameter	Conditions		Min	Max	Unit
t_{pd}	propagation delay	nA to nBn or nBn to nA; see Fig. 5	[1][2]	-	0.25	ns
		S to nA; see Fig. 5	[1][2]	1.4	5.0	ns
t_{en}	enable time	$\overline{OE}$ to nA or nBn; see Fig. 6	[2]	1.5	5.1	ns
		S to nBn; see Fig. 6	[2]	1.4	5.2	ns
t_{dis}	disable time	$\overline{OE}$ to nA or nBn; see Fig. 6	[2]	2.2	5.5	ns
		S to nBn; see Fig. 6	[2]	1.0	5.0	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t_{PLH} and t_{PHL} are the same as t_{pd}; t_{PZL} and t_{PZH} are the same as t_{en}; t_{PLZ} and t_{PHZ} are the same as t_{dis}.

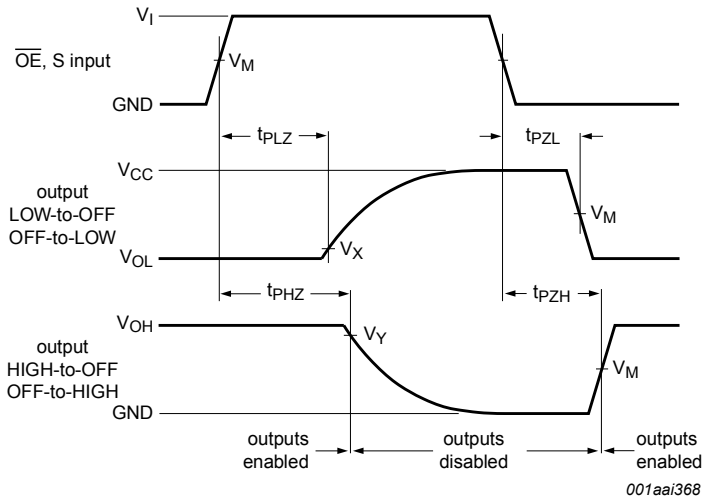
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. The input (nA; nBn) to output (nBn; nA) or input (S) to output (nA) propagation delay times



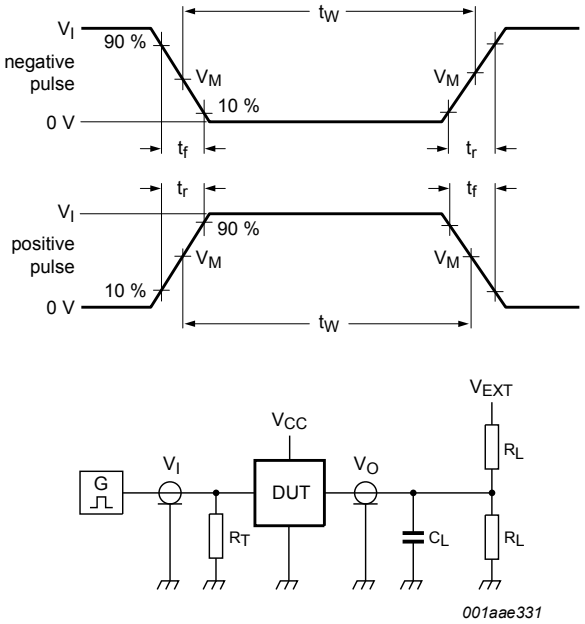
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
4.5 V to 5.5 V	GND to 3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

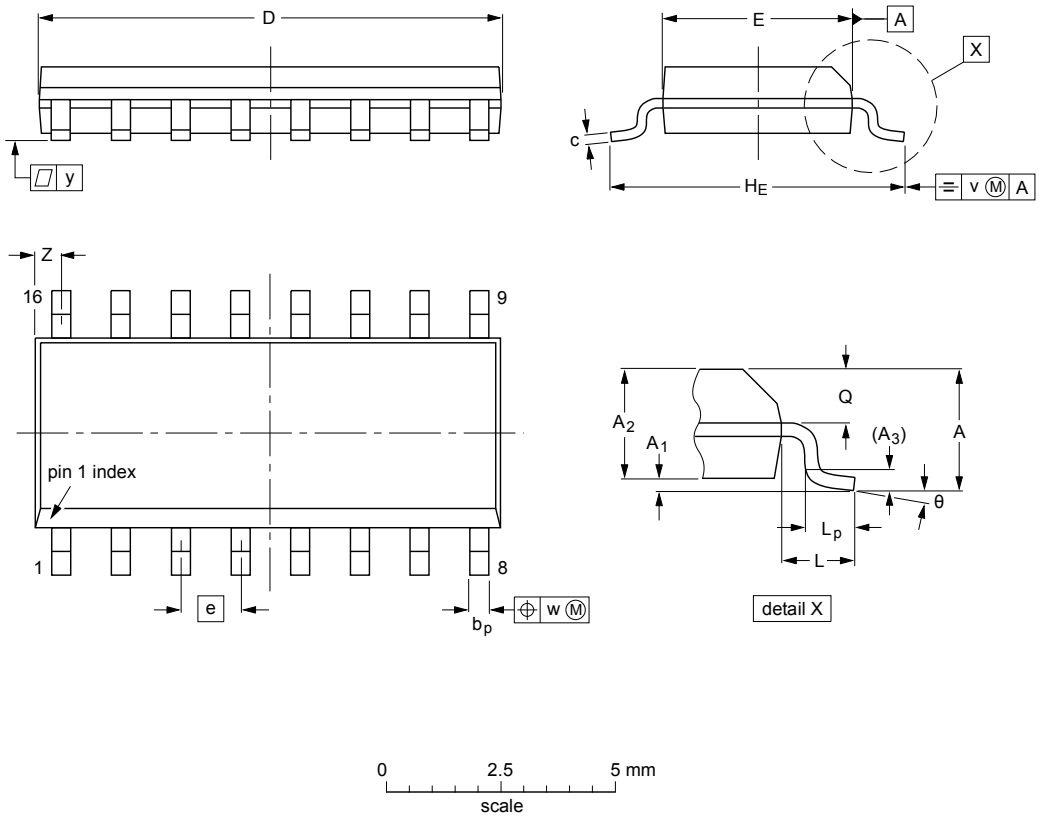
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
4.5 V to 5.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

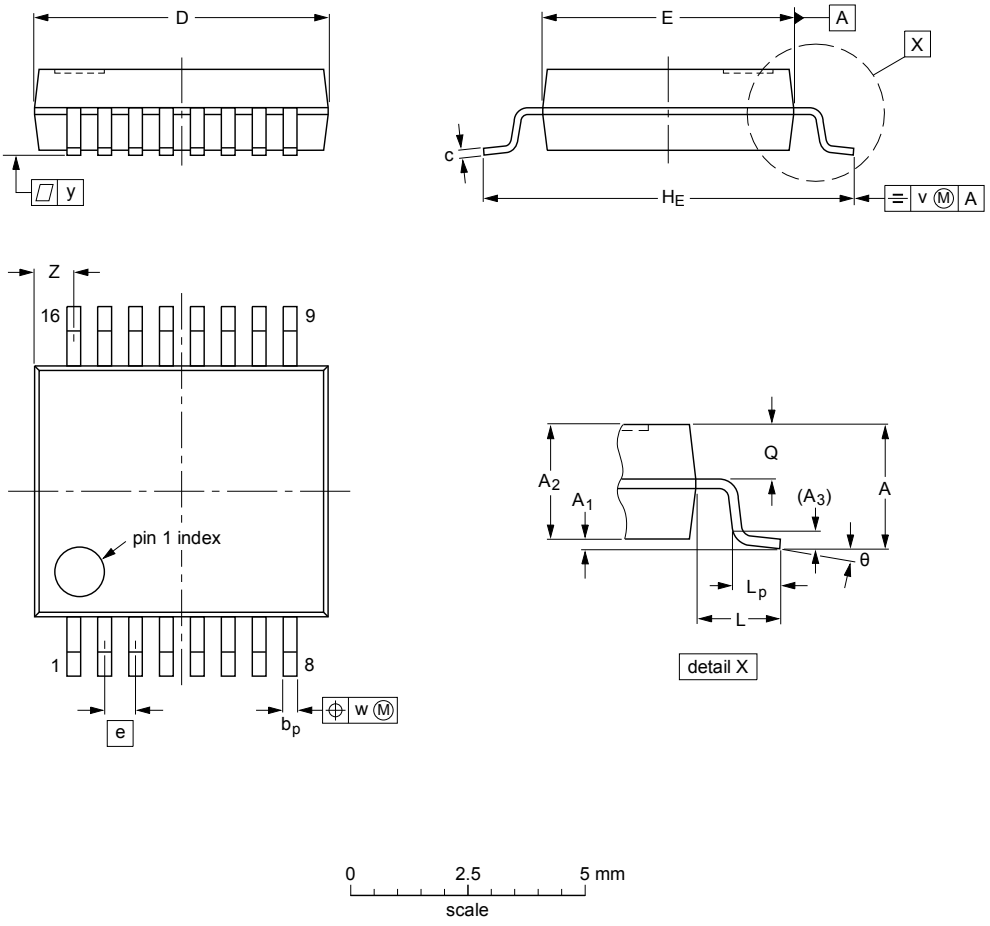
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

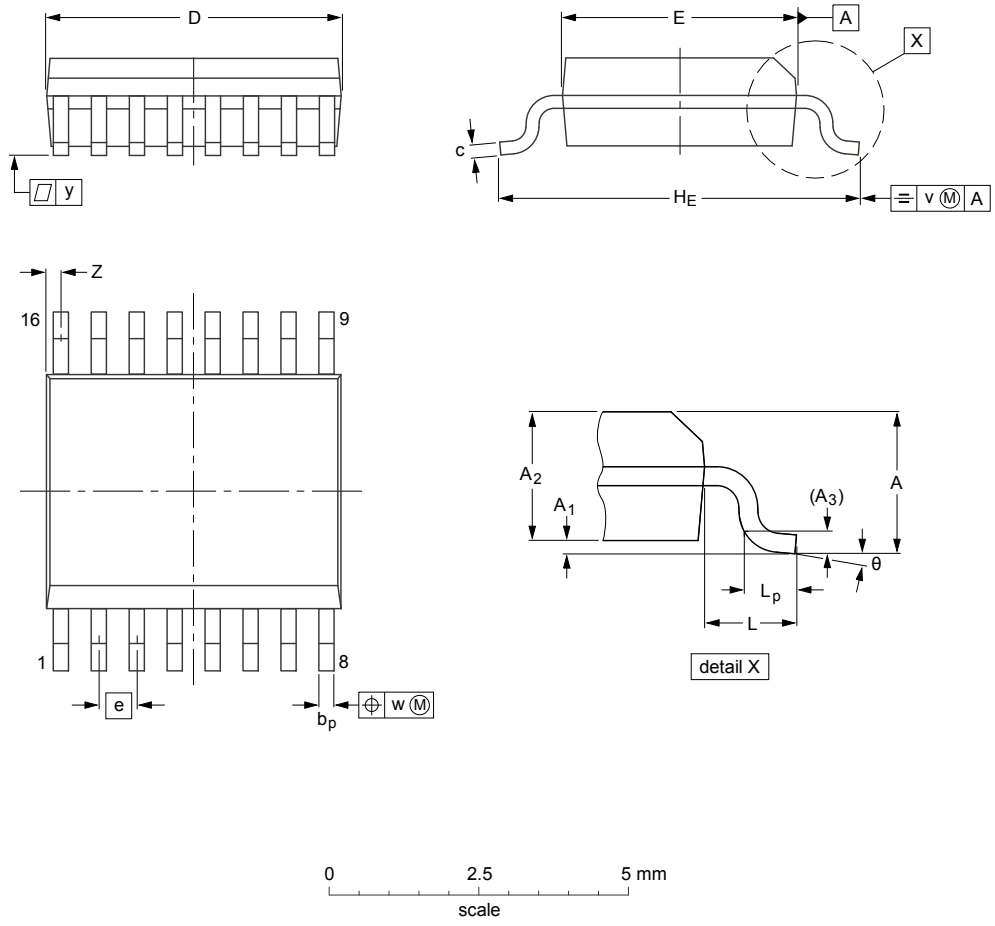
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 9. Package outline SOT338-1 (SSOP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT519-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	v	w	y	Z (1)	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8^o 0^o

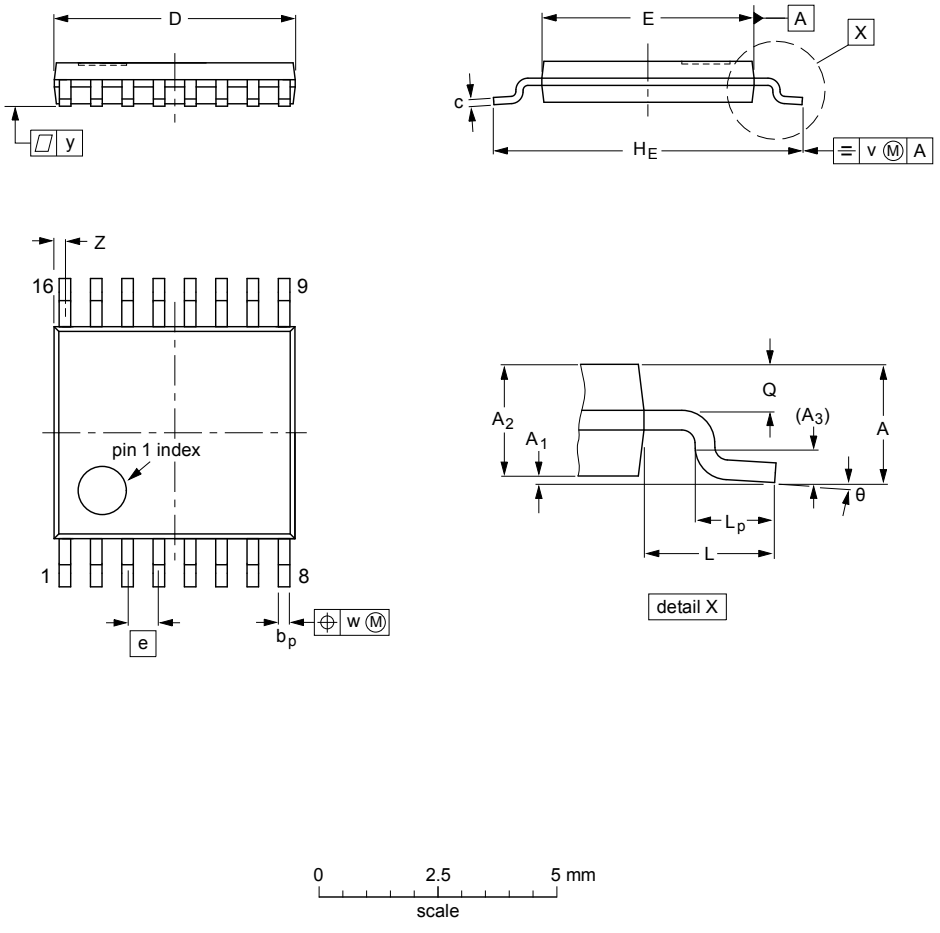
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT519-1						~~99-05-04~~ 03-02-18

Fig. 10. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

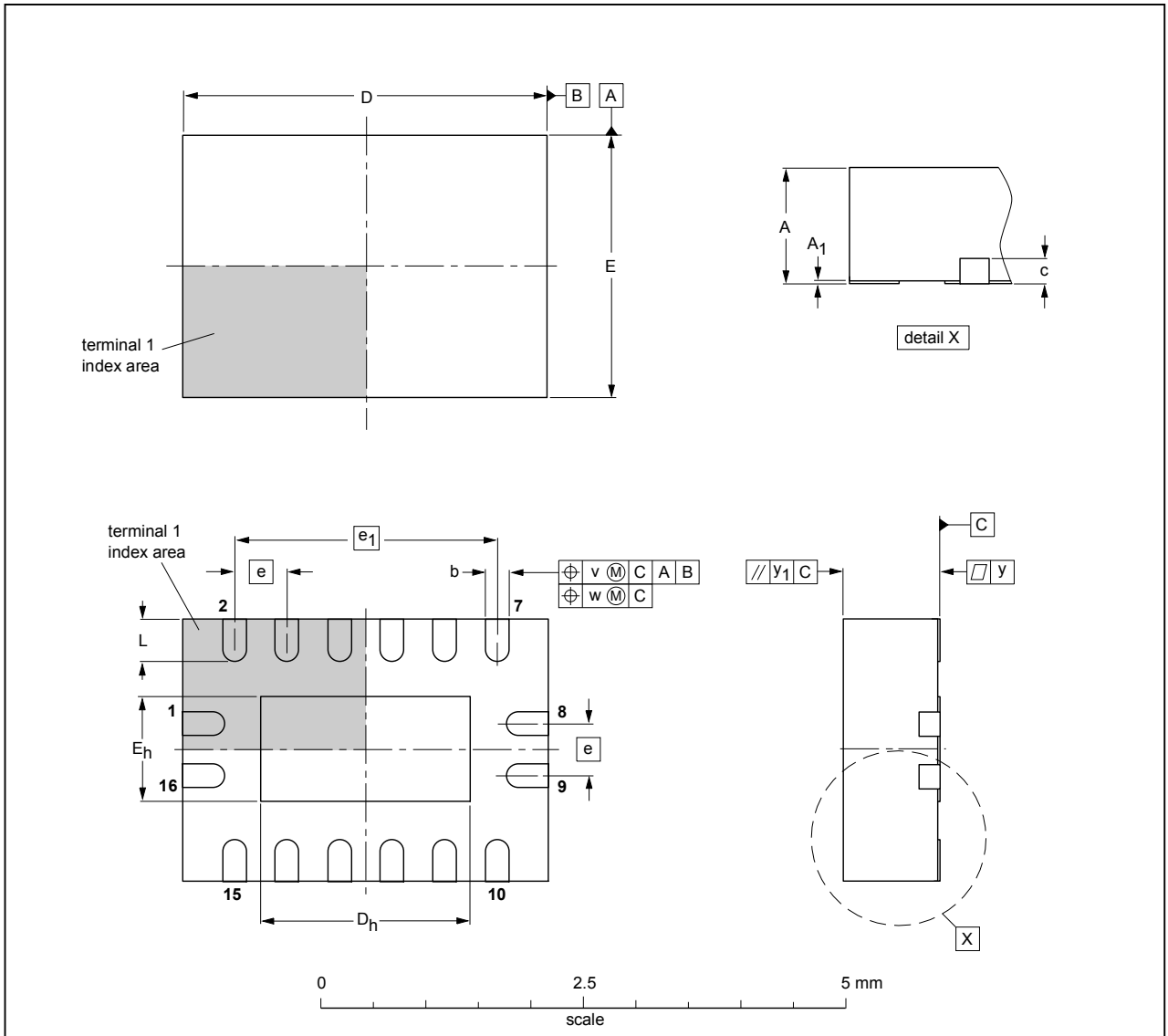
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 12. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3257A v.6	20190620	Product data sheet	-	CBT3257A v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
CBT3257A v.5	20130404	Product data sheet	-	CBT3257A v.4
Modifications:	Table 6: values for pass voltage modified.			
CBT3257A v.4	20090319	Product data sheet	-	CBT3257A v.3
CBT3257A v.3	20080704	Product data sheet	-	CBT3257A v.2
CBT3257A v.2	20070704	Product data sheet	-	CBT3257A v.1
CBT3257A v.1	20051027	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 20 June 2019