MP6924A

Fast Turn-Off, CCM/DCM Compatible, Dual LLC Synchronous Rectifier with Improved Noise Immunity

The Future of Analog IC Technology®

DESCRIPTION

The MP6924A is a dual, fast turn-off, intelligent rectifier for synchronous rectification in LLC resonant converters.

The IC drives two N-channel MOSFETs, regulates their forward voltage drop to V_{fwd} (about 29mV), and turns the MOSFETs off before the switching current goes negative.

The MP6924A has a light-load function to latch off the gate driver under light-load conditions, limiting the current to 175µA.

The MP6924A's fast turn-off enables both continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

The MP6924A requires a minimal number of readily available, standard, external components and is available in a SOIC-8 package.

FEATURES

- Works with Standard and Logic Level MOSFETs
- Compatible with Energy Star
- Fast Turn-Off Total Delay of 35ns
- Wide 4.2V ~ 35V V_{DD} Operating Range
- 175µA Low Quiescent Current in Light-Load Mode
- Supports CCM, CrCM, and DCM Operation
- Supports High-Side and Low-Side Rectification
- Available in a SOIC-8 Package

APPLICATIONS

- AC/DC Adapters
- PC Power Supplies
- LCD and LED TVs
- Isolated DC/DC Power Converters

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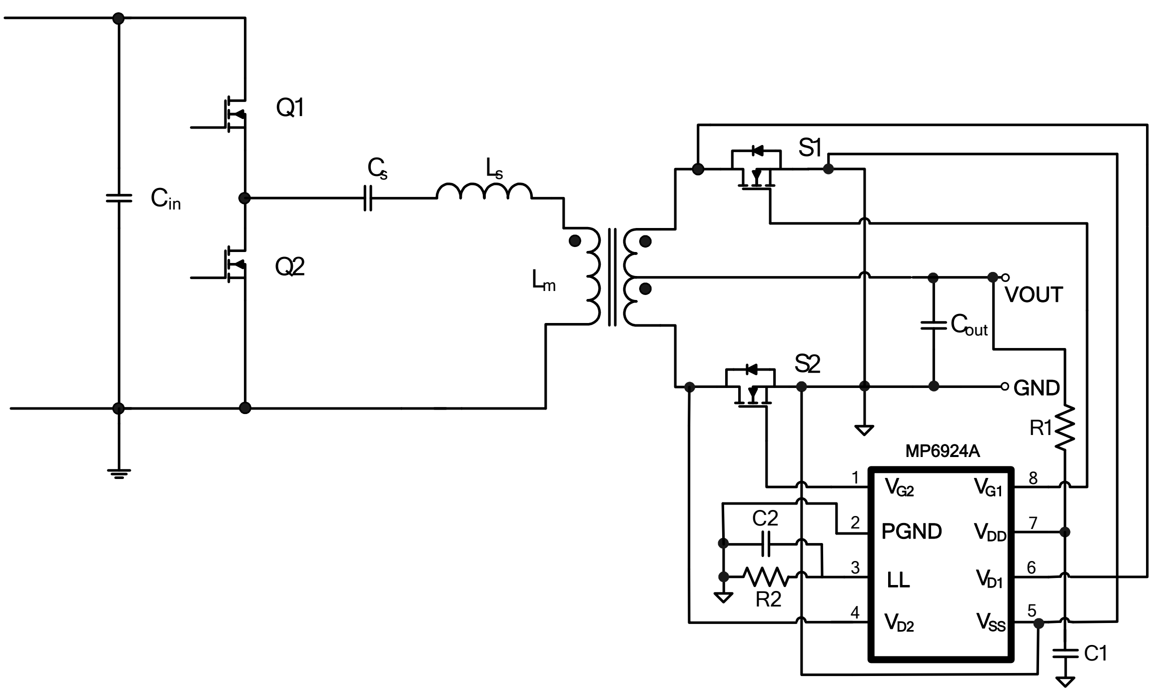
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marketing
MP6924AGS	SOIC-8	*See Below*

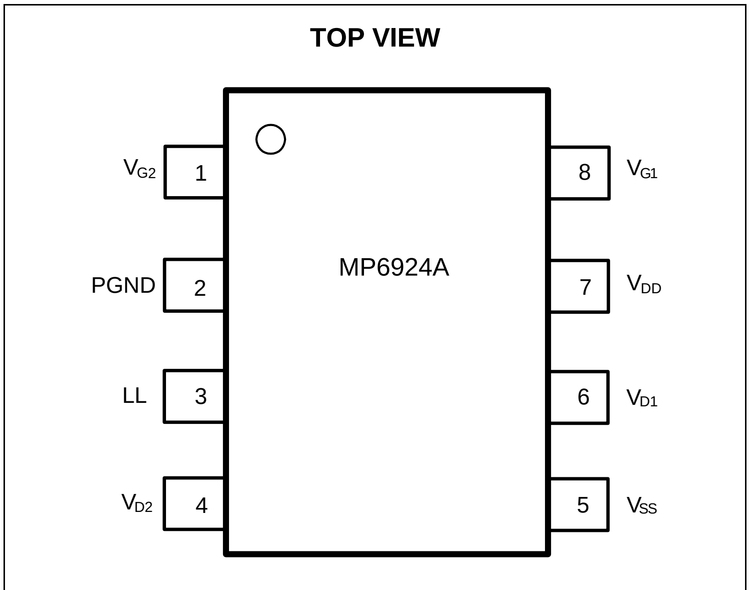
* For Tape & Reel, add suffix –Z (e.g. MP6924AGS–Z)

TOP MARKING

MP6924A
LLLLLLLL
MPSYWW

MP6924A: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



SOIC-8

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ABSOLUTE MAXIMUM RATINGS (1)

V_{DD} to V_{SS} .... -0.3V to +38V
PGND to V_{SS} .... -0.3V to +0.3V
V_G to V_{SS} .... -0.3V to +20V
V_D to V_{SS} .... -1V to +180V
LL to V_{SS} .... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2)
SOIC-8 .... 1.4W
Junction temperature .... 150°C
Lead temperature (solder) .... 260°C
Storage temperature .... -55°C to +150°C

Recommended Operation Conditions (3)

V_{DD} to V_{SS} .... 4.2V to 35V
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC-8	90	45	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, -40°C ≤ T_J ≤ +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{DD} voltage range			4.2		35	V
V_{DD} UVLO rising			3.7	3.95	4.2	V
V_{DD} UVLO hysteresis			0.13	0.185	0.24	V
Operating current	I_{CC}	C_{LOAD} = 4.7nF, F_{SW} = 100kHz		16	20	mA
Quiescent current	I_Q	V_{SS} - V_D = 0.5V		4.6	6	mA
Shutdown current		V_{DD} = 4V, LL = 0V		135	190	µA
		V_{DD} = 20V, LL = 0V		155	210	
Light-load mode current				175	225	µA
Thermal shutdown [5]				175		°C
Thermal shutdown hysteresis [5]				10		°C
Control Circuitry Section						
V_{SS} - V_D forward voltage	V_{fwd}		17	29	41	mV
Turn-off threshold (V_{SS} - V_D)				0		mV
Turn-on delay	t_{Don}	C_{LOAD} = 4.7nF, V_{GS} = 2V		190	300	ns
	t_{Don}	C_{LOAD} = 10nF, V_{GS} = 2V		270	410	ns
Input bias current on V_D		V_D = 180V			1	µA
Turn-on blanking time	t_{B_ON}	C_{LOAD} = 4.7nF	0.75	1.1	1.65	µs
Turn-off blanking time [5]	t_{B_OFF}	C_{LOAD} = 4.7nF		1750		ns
Light-load enter pulse width	T_{LL}	R_{LL} = 100kΩ	1.7	2.3	3	µs
Light-load turn-on pulse width hysteresis	T_{LL-H}	R_{LL} = 100kΩ		0.45		µs
Light-load enter delay	T_{LL-D}		45	78	121	µs
Gate disable threshold on LL	V_{LL_DIS}		0.1	0.2	0.3	V
Turn-on threshold (V_{DS})	V_{LL_DS}	V_{DD} = 12V	-330	-230	-130	mV
Gate Driver Section						
V_G (low)	V_{G_L}	I_{LOAD} = 1mA			0.1	V
V_G (high)	V_{G_H}	V_{DD} > 10V		11.5	13	V
		V_{DD} ≤ 10V		V_{DD}		
Turn-off propagation delay		V_D = V_{SS}		15		ns
Turn-off total delay	t_{Doff}	V_D = V_{SS}, C_{LOAD} = 4.7nF, R_{GATE} = 0Ω, V_{GS} = 2V		35	80	ns
	t_{Doff}	V_D = V_{SS}, C_{LOAD} = 10nF, R_{GATE} = 0Ω, V_{GS} = 2V		45	100	ns
Pull-down impedance				0.6	1.5	Ω

NOTE:

5) Guaranteed by characterization.

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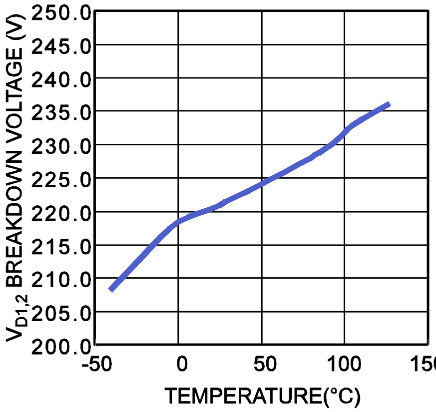
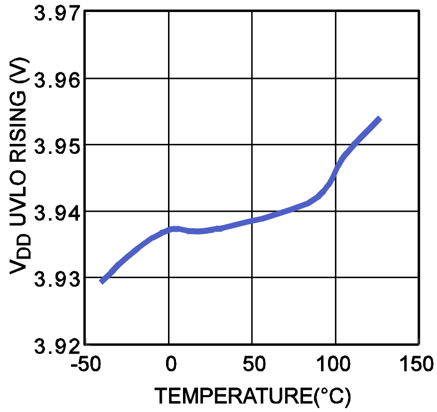
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, unless otherwise noted.

$V_{D1,2}$ Breakdown Voltage vs. Temperature

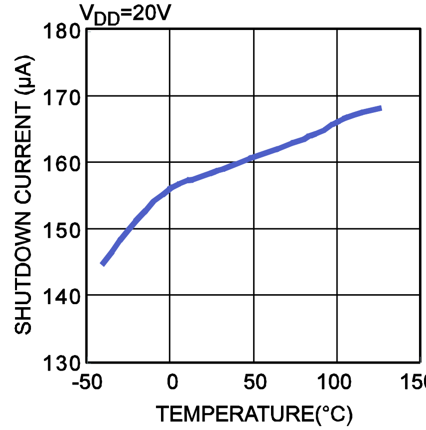


V_{DD} UVLO Rising vs. Temperature



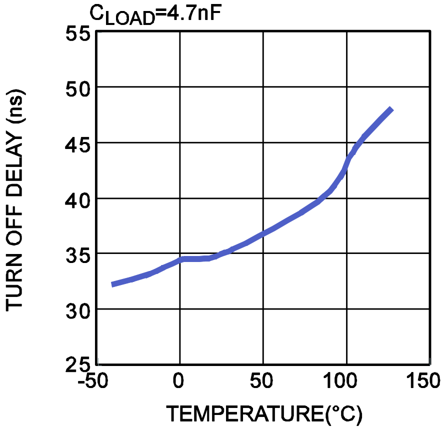
Shutdown Current vs. Temperature

V_{DD}=20V



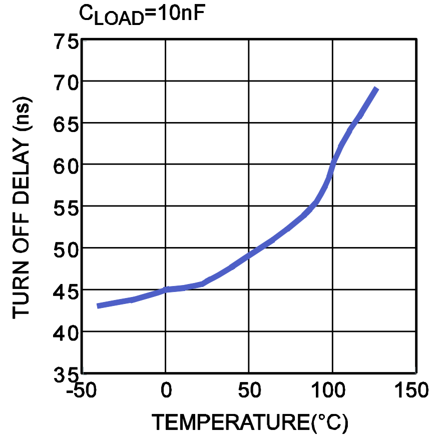
Turn-Off Delay vs. Temperature

C_{LOAD}=4.7nF



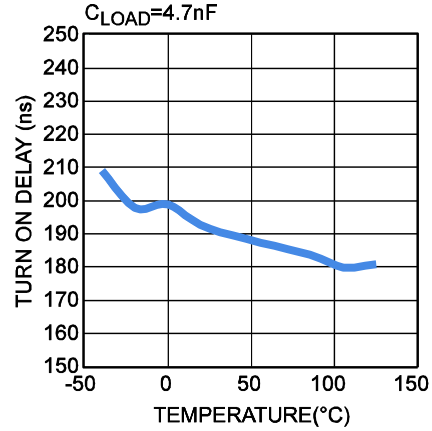
Turn-Off Delay vs. Temperature

C_{LOAD}=10nF



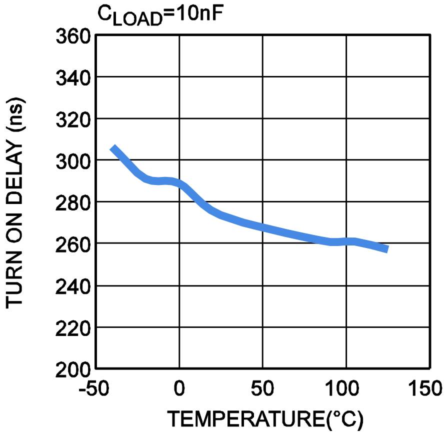
Turn-On Delay vs. Temperature

C_{LOAD}=4.7nF

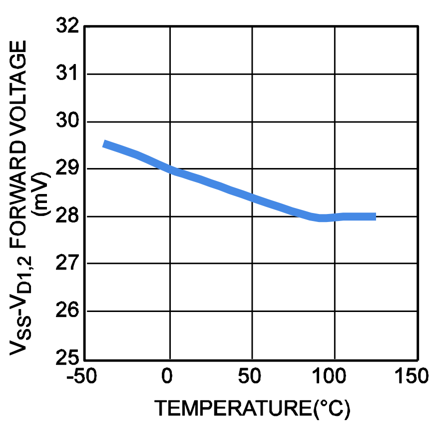


Turn-On Delay vs. Temperature

C_{LOAD}=10nF



V_{SS}-$V_{D1,2}$ Forward Voltage vs. Temperature



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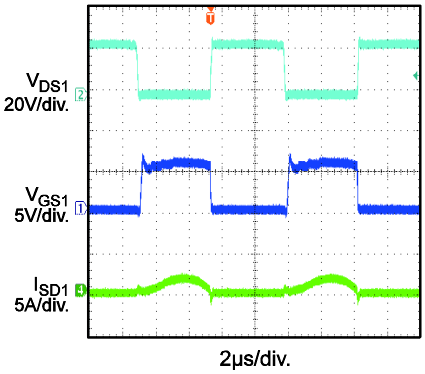
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 12V, unless otherwise noted.

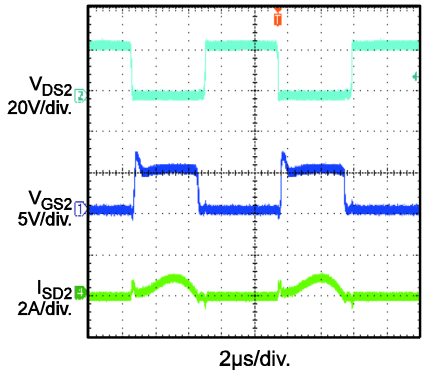
Operation in 90W LLC Converter

V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=0.75A



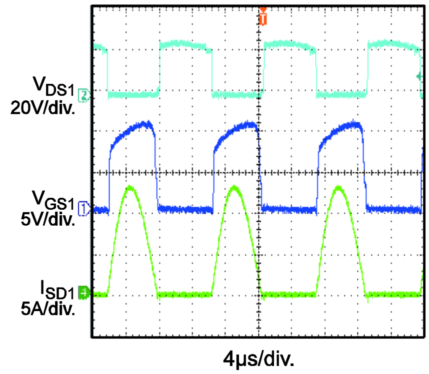
Operation in 90W LLC Converter

V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=0.75A



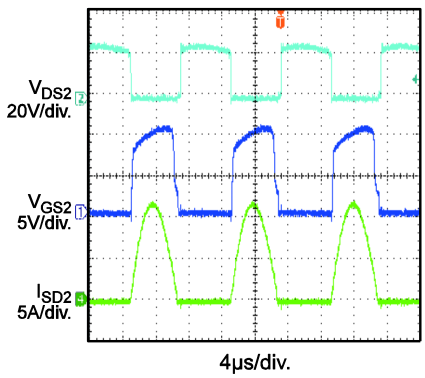
Operation in 90W LLC Converter

V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=7.5A



Operation in 90W LLC Converter

V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=7.5A



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PIN FUNCTIONS

Pin # (SOIC-8)	Name	Description
1	V_{G2}	**MOSFET 2 gate driver output.**
2	PGND	**Power ground.** PGND is the power switch return.
3	LL	**Light-load timing setting.** Connect a resistor to LL to set the light-load timing. Leave LL open to prevent the IC from entering light-load mode. Pull LL low to disable the gate driver.
4	V_{D2}	**MOSFET 2 drain voltage sense.**
5	V_{SS}	**Source pin used as reference for V_{D1} and V_{D2}.**
6	V_{D1}	**MOSFET 1 drain voltage sense.**
7	V_{DD}	**Supply voltage.**
8	V_{G1}	**MOSFET 1 gate driver output.**

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BLOCK DIAGRAM

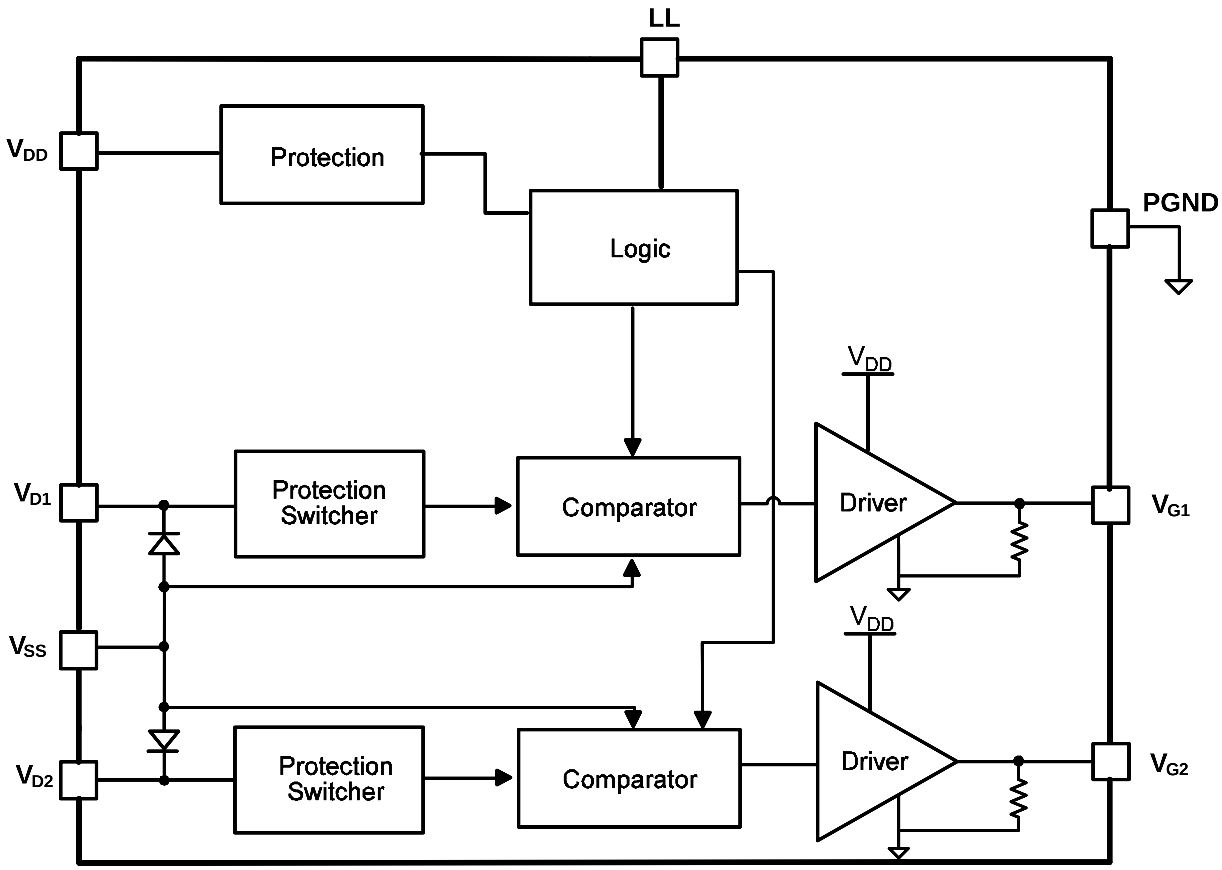

Figure 1: Functional Block Diagram

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OPERATION

The MP6924A operates in discontinuous conduction mode (DCM), continuous conduction mode (CCM), and critical conduction mode (CrCM). When the MP6924A operates in either DCM or CrCM, the control circuitry controls the gate in forward mode. The gate turns off when the MOSFET current is low. In CCM, the control circuitry turns off the gate during very fast transients.

VD Clamp

Because $V_{D1,2}$ can rise as high as 180V, a high-voltage JFET is used at the input. To prevent excessive currents when $V_{DS1,2}$ drops below -0.7V, a 1kΩ resistor is recommended between $V_{D1,2}$ and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

When V_{DD} is below the V_{DD} UVLO threshold, the MP6924A falls into sleep mode, and $V_{G1,2}$ remains at a low level.

Enable

If LL is pulled low, the MP6924A is in shutdown mode, which consumes 175µA of shutdown current. If LL is pulled high during the rectification cycle, the gate driver does not appear until the next rectification cycle begins (see Figure 2).

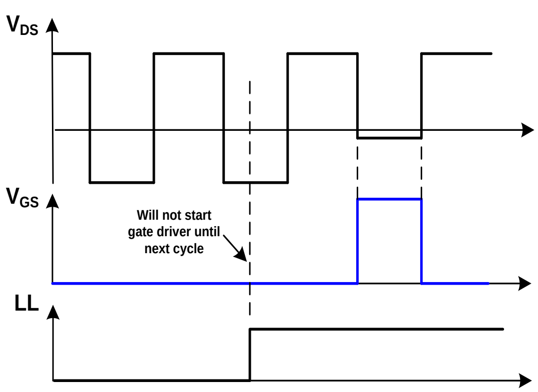

Figure 2: LL Control Scheme

Thermal Shutdown

If the junction temperature of the chip exceeds the thermal shutdown threshold, $V_{G1,2}$ is pulled low, and the MP6924A stops switching. The IC resumes normal function after the junction temperature drops 10°C.

Turn-On Phase

When the switch current flows through the body diode of the MOSFET, there is a negative voltage drop (V_D - V_{SS}) across the body diode. V_{DS} is much lower than the turn-on threshold of the control circuitry (V_{LL-DS}), which triggers a charge current to turn on the MOSFET (see Figure 3).

Turn-On Blanking

The control circuitry contains a blanking function that ensures that when the MOSFET turns on or off, it remains in that state for t_{B_ON} (~1.1µs), which determines the minimum on time. During the turn-on blanking period, the turn-off threshold is not blanked completely, but changes to about +100mV (instead of 0mV). This ensures that the part can always turn off, even during the turn-on blanking period, although it does so slower. Avoid setting the synchronous period below t_{B_ON} in CCM in the LLC converter to eliminate shoot-through.

Conduction Phase

When V_{DS} rises above the forward voltage drop ($-V_{fwd}$) according to the decrease of the switching current, the MP6924A pulls down the gate voltage level to make the on resistance of the synchronous MOSFET larger to ease the rise of V_{DS}.

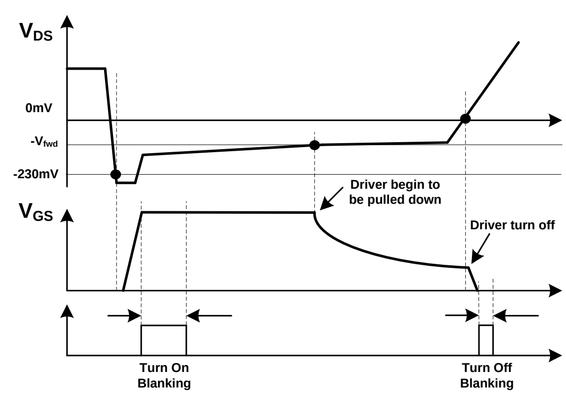

Figure 3: Turn-On/-Off Timing Diagram

The control scheme in Figure 3 shows V_{DS} adjusted to be around $-V_{fwd}$, even when the current through the MOSFET is fairly low. This function puts the driver voltage at a very low level when the synchronous MOSFET is turning off, which boosts the turn-off speed.

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Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold, the gate voltage is pulled to zero after a very short turn-off delay (see Figure 3).

Turn-Off Blanking

After the gate driver is pulled to zero by V_{DS} reaching the turn-off threshold, turn-off blanking is triggered to ensure that the gate driver is off for at least t_{B_ON} to prevent an erroneous trigger on V_{DS}.

Light-Load Latch-Off Function

The gate driver of the MP6924A is latched off to save driver loss in light-load condition and improve efficiency.

When the MOSFET's switching cycle conducting period falls below T_{LL}, the MP6924A enters light-load mode and latches off the MOSFET after a light-load enter delay (T_{LL-D}) (see Figure 4).

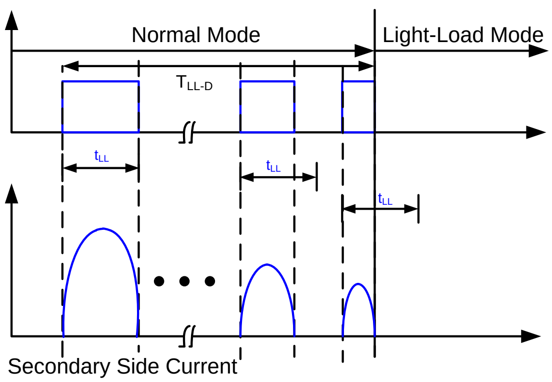

Figure 4: MP6924A Entering Light-Load Mode

During light-load mode, the MP6924A monitors the body diode conduction time. If this time exceeds T_{LL} + T_{LL-H}, the IC exits light-load mode and initiates the gate driver in the next new switching cycle (see Figure 5 and Figure 6).

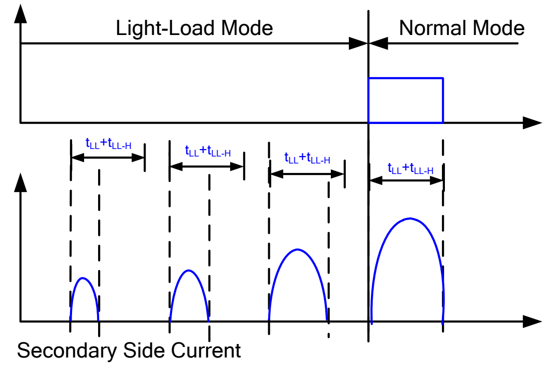

Figure 5: MP6924A Exiting Light-Load Mode

Light-load enter timing (T_{LL}) is programmable by connecting a resistor (R_{LL}) to LL. By monitoring the LL current (the LL voltage is kept at ~2V internally), T_{LL} can be calculated with Equation (1):

$$T_{LL} = R_{LL}(k\Omega) \cdot \frac{2.3us}{100k\Omega} \quad (1)$$

If the light-load mode of the MP6924A ends during the rectification cycle, the gate driver signal does not appear until the next rectification cycle begins (see Figure 6).

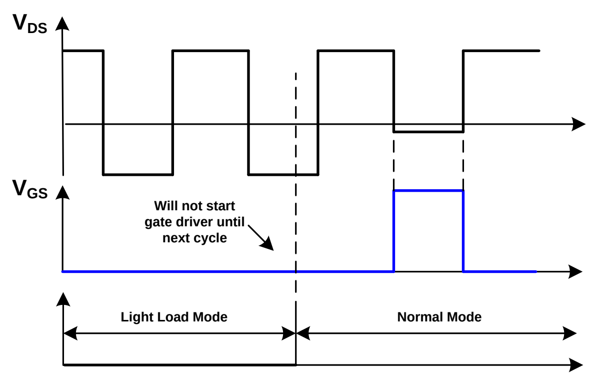

Figure 6: Gate Driver Starting after Exiting Light-Load Mode

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APPLICATION INFORMATION

Layout Considerations

Listed below are the main recommendations that should be taken into consideration when designing the PCB.

Sensing for V_D/V_S

1. Keep the sensing connections (V_{D1}/V_{SS}, V_{D2}/V_{SS}) as close to each of the MOSFETs (drain/source) as possible.
2. Keep the two channels' sensing loops separated from each other.
3. Make the sensing loop as small as possible (see Figure 7).

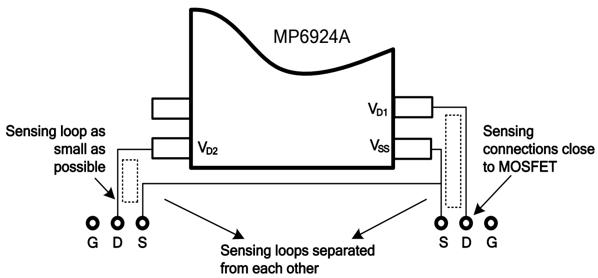

Figure 7: Sensing for V_D/V_S

Figure 8 shows a layout example of the MP6924A driving PowerPAK SO8 package MOSFETs with two, separate, small sensing loops.

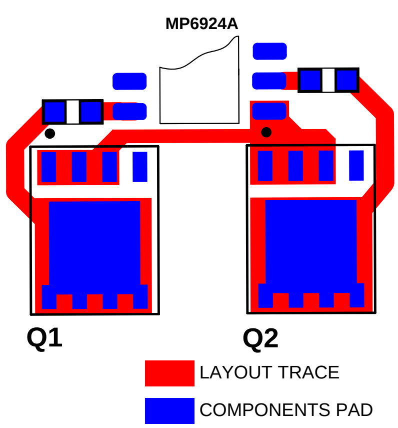

Figure 8: Layout Example for Sensing Loop and V_{DD} Decoupling

V_{DD} Decoupling Capacitor

1. Place a decoupling capacitor no smaller than 1µF from V_{DD} to PGND close to the IC for adequate filtering (see Figure 9).

System Power Loop

1. Keep the two channels' power loops separated from each other (see Figure 9).

   This minimizes the interaction between the two channels' power loops, which may affect the voltage sensing of the IC.

2. Make the power loop as small as possible to reduce parasitic inductance.

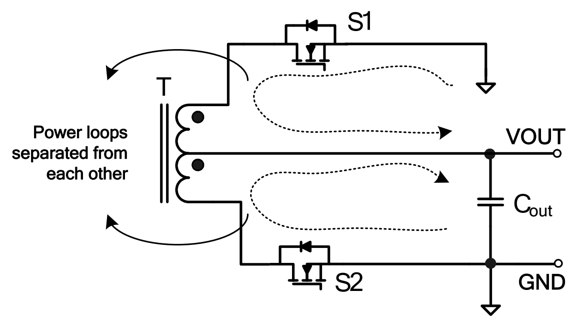

Figure 9: System Power Loop

Figure 10 shows a layout example of the power loop trace, which has a minimized loop length. The two channel power traces do not cross each other.

It is highly recommended to place the driver's sensing loop trace away from the power loop trace (see Figure 10). The sensing loop trace and power loop trace can be placed on different layers to keep them separate from each other.

Do not place the driver IC inside the power loop. This may affect MOSFET voltage sensing.

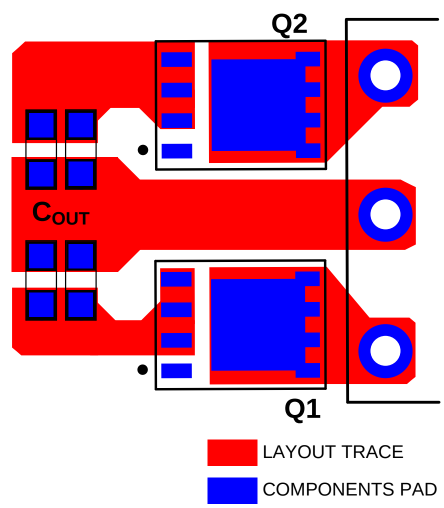

Figure 10: Layout Example for System Power Loop

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SR MOSFET Selection and Driver Ability

Power MOSFET selection is a trade-off between the $R_{DS(ON)}$ and Q_g. To achieve high efficiency, a MOSFET with a smaller $R_{DS(ON)}$ is recommended. A larger Q_g with a smaller $R_{DS(ON)}$ makes the turn-on/-off speed lower and the power loss larger. For the MP6924A, V_{DS} is adjusted at V_{fwd} during the driving period. A MOSFET with a small $R_{DS(ON)}$ is not recommended because the gate driver may be kept at a fairly low level with a small $R_{DS(ON)}$, even when the system load is high, which makes the advantage of the low $R_{DS(ON)}$ inconspicuous.

Figure 11 shows the typical waveform of the LLC on the secondary side. To achieve a fairly high usage of the MOSFET's $R_{DS(ON)}$, it is expected that the MOSFET driver voltage is kept at the maximum level until the last 25% of the SR conduction period. Calculate V_{DS} with Equation (2):

$$V_{DS} = -R_{ds(ON)} \cdot \frac{\sqrt{2}}{2} \cdot I_{peak} = -R_{ds(ON)} \cdot I_{OUT} = -V_{fwd} \quad (2)$$

Where V_{DS} is drain-source voltage of the MOSFET.

The MOSFET's $R_{DS(ON)}$ is recommended to be no lower than ~V_{fwd}/I_{OUT} (mΩ). For example, in a 10A application with V_{fwd} at 29mV, the $R_{DS(ON)}$ of the MOSFET is recommended to be no lower than 2.9mΩ.

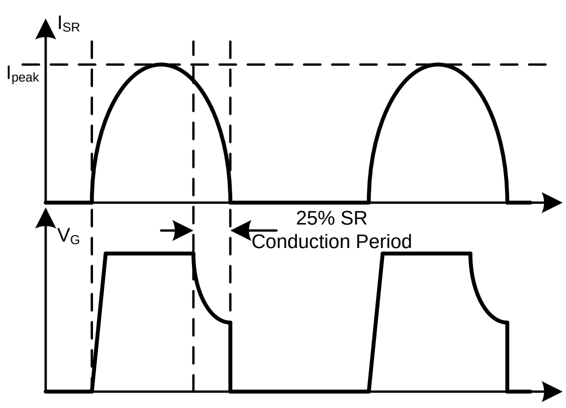

Figure 11: Synchronous Rectification Typical Waveform in LLC

Q_g of the MOSFET affects the turn-on and turn-off delay. Figure 12 shows the turn-on delay (t_{Don}) and the turn-off delay (t_{Doff}). t_{Don} indicates how long the body diode conducts before the MOSFET turns on, while t_{Doff} indicates how long the driver takes to turn off the MOSFET. With a higher turn-on delay, the body diode conduction duration of the MOSFET is longer, which brings down the total efficiency. However, with a higher turn-off delay, the shoot-through risk is higher in CCM operation.

Figure 12 and Figure 13 show the t_{Don} and t_{Doff} of the MP6924A according to different C_{load} values.

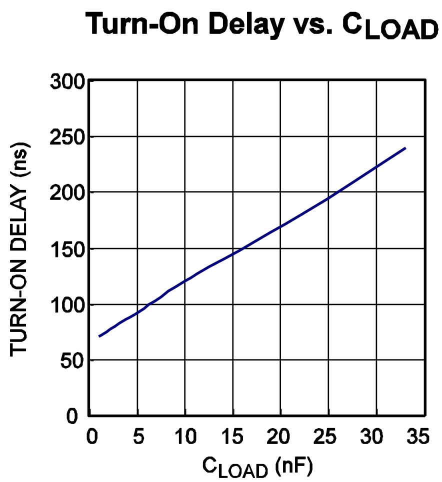

Figure 12: Turn-On Delay vs. C_{load}

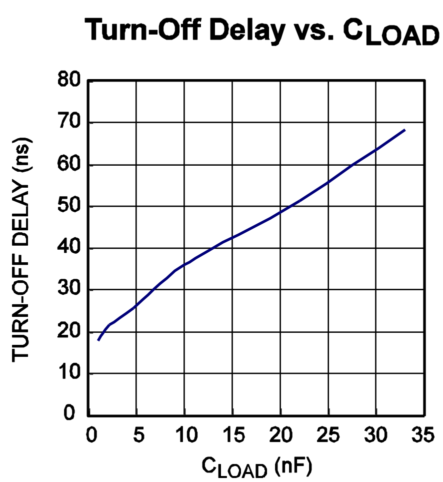

Figure 13: Turn-Off Delay vs. C_{load}

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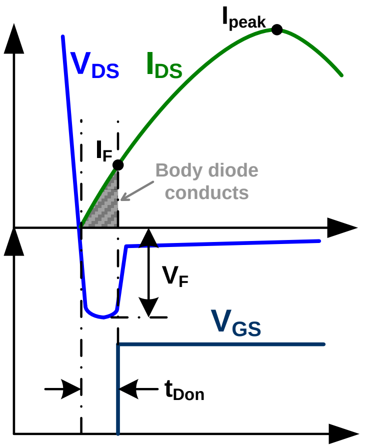

Figure 14: Turn-On Delay Effect on Efficiency

Figure 14 shows how t_{Don} affects system efficiency. During t_{Don}, the body diode of the SR MOSFET conducts, which leads to a power loss that can be calculated with Equation (3):

$$P_{on} \approx \frac{V_F \cdot I_F}{2} \cdot 2f_s \cdot t_{Don} = V_F \cdot I_F \cdot f_s \cdot t_{Don} \quad (3)$$

Where V_F is the body diode forward voltage drop, I_F is the switching current when the turn-on delay (t_{Don}) has ended, and f_s is the switching frequency.

When considering the switching current as a complete sine wave, I_F can be estimated with Equation (4) and Equation (5):

$$I_F = I_{peak} \cdot \sin(2 \cdot f_s \cdot t_{Don} \cdot \pi) \quad (4)$$

$$I_{peak} \approx \frac{\pi}{2} \cdot I_{out} \quad (5)$$

Where I_{peak} is the peak switching current through the MOSFET, and I_{out} is the system output current.

When plugging the values from Equation (4) and Equation (5) into Equation (3), the turn-on delay power loss through the SR MOSFET's body diode can be derived with Equation (6):

$$P_{on} = \frac{\pi}{2} \cdot I_{out} \cdot V_F \cdot f_s \cdot t_{Don} \cdot \sin(2 \cdot f_s \cdot t_{Don} \cdot \pi) \quad (6)$$

Figure 15 shows how different turn-on delay values affect efficiency according to different output voltages. To keep the body diode conduction loss at a fairly low level (below 0.5% of the output power), the turn-on delay is recommended to be less than 5% of the switching cycle. For example, in a f_{sw} = 200kHz LLC system, the switching cycle is ~5µs. It is recommended to select a MOSFET that makes t_{Don} < 250ns.

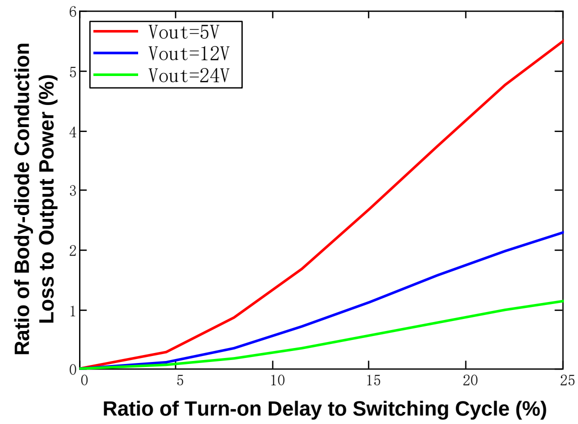

Figure 15: Turn-On Delay vs. Power Loss

The turn-off delay (t_{Doff}) is critical in some fast transient CCM applications. Choose the MOSFET to make t_{Doff} below the CCM current transient duration. Otherwise, the MOSFET may need to be selected with a lower Q_g, or an external totem pole driver circuit may be added to prevent shoot-through.

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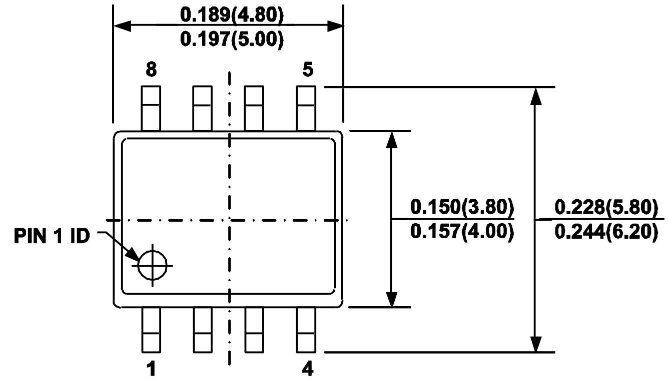
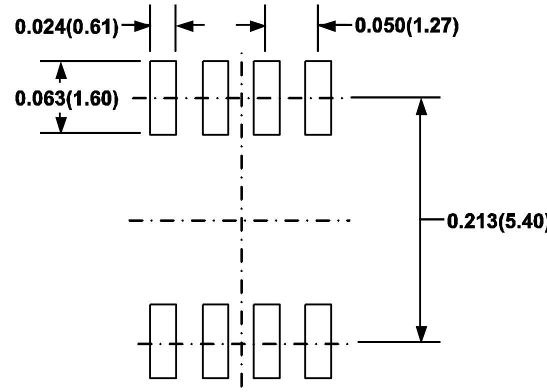
PACKAGE INFORMATION

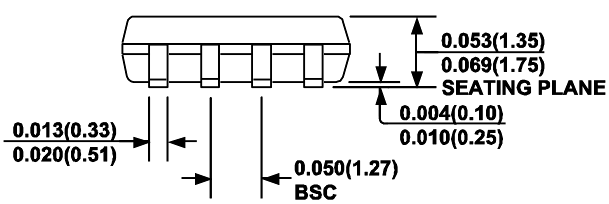
SOIC-8



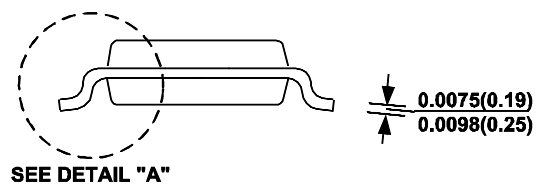
TOP VIEW



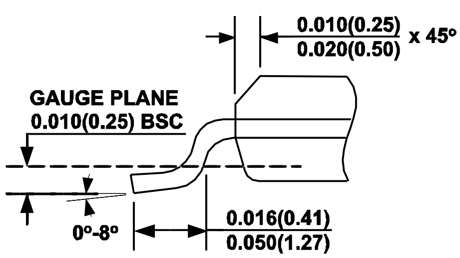
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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