

## J111, J112, J113

## N-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at  $T_A = 25^\circ\text{C}$ 

Reverse Gate Source & Reverse Gate Drain Voltage	- 35 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature  
Static Electrical Characteristics

		J111		J112		J113		Process NJ132	
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	- 35		- 35		- 35		V	$I_G = -1\mu\text{A}, V_{DS} = 0\text{V}$
Gate Reverse Current	$I_{GSS}$		- 1		- 1		- 1	nA	$V_{GS} = -15\text{V}, V_{DS} = 0\text{V}$
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	- 3	- 10	- 1	- 5		- 3	V	$V_{DS} = 5\text{V}, I_D = 1\mu\text{A}$
Drain Saturation Current (Pulsed)	$I_{DSS}$	20		5		2		mA	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}$
Drain Cutoff Current	$I_{D(OFF)}$		- 1		- 1		- 1	nA	$V_{DS} = 15\text{V}, V_{GS} = -10\text{V}$

## Dynamic Electrical Characteristics

Drain Source ON Resistance	$r_{ds(on)}$		30		50		100	$\Omega$	$V_{GS} = 0\text{V}, V_{DS} = 0.1\text{V}$	$f = 1\text{kHz}$
Drain Gate Capacitance	$C_{dg}$		5		5		5	pF	$V_{DS} = 0\text{V}, V_{GS} = -10\text{V}$	$f = 1\text{MHz}$
Source Gate Capacitance	$C_{gs}$		5		5		5	pF	$V_{DS} = 0\text{V}, V_{GS} = -10\text{V}$	$f = 1\text{MHz}$
Drain Gate + Source Gate Capacitance	$C_{gd} + C_{gs}$		28		28		28	pF	$V_{DS} = V_{GS} = 0\text{V}$	$f = 1\text{MHz}$

## Switching Characteristics

		Typ		Typ		Typ						
								J111	J112	J113		
Turn ON Delay Time	$t_{d(on)}$	7		7		7	ns					
Rise Time	$t_r$	6		6		2	ns	$V_{DD}$	10	10	10	V
Turn OFF Delay Time	$t_{d(off)}$	20		20		20	ns	$V_{GS(OFF)}$	- 12	- 7	- 5	V
Fall Time	$t_f$	15		15		15	ns	$R_L$	800	1600	3200	$\Omega$

## TO-226AA Package

Dimensions in Inches (mm)

## Pin Configuration

1 Drain, 2 Source, 3 Gate

## Surface Mount

SMPJ111, SMPJ112, SMPJ113