High Speed Rail-to-Rail Input Comparator with LVDS Compatible Outputs

FEATURES

- **Low Propagation Delay: 1.8ns Typ.**
- **Low Overdrive Dispersion: 1ns Typ. (10mV to 125mV Overdrive)**
- **High Toggle Rate: 890Mbps Typ.**
- **LVDS Compatible Output Stage**
- Rail-to-Rail Inputs Extend Beyond Both Rails
- Low Quiescent Current: 13.4mA
- Supply Range: 2.4V to 5.25V
- Features within the LTC6754 Family:
  - Separate Input and Output Supplies
  - Shutdown Pin for Reduced Power
  - Output Latch and Adjustable Hysteresis
  - SC70 and 3mm ×3mm QFN Packages

APPLICATIONS

- Clock and Data Recovery
- Level Translation
- High Speed Data Acquisition Systems
- Window Comparators
- High Speed Line Receivers
- Time Domain Reflectometry
- Time of Flight Measurements
- Cable Drivers

DESCRIPTION

The LTC®6754 is a high speed rail-to-rail comparator with LVDS compatible outputs. The LTC6754 exhibits 1.8ns of propagation delay, only 1ns of dispersion (10mV to 125mV overdrive) and a toggle rate up to 890Mbps.

The LTC6754 has rail-to-rail inputs, and will operate from a 2.4V to 5.25V supply. For the QFN package, the LVDS output is operated with a separate supply, providing isolation between input and output circuitry, and allowing for logic level translation.

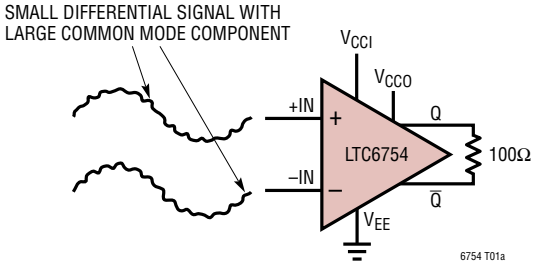
In shutdown mode, power is reduced from 13.4mA to under 1.1mA, and the comparator can wake up in 120ns.

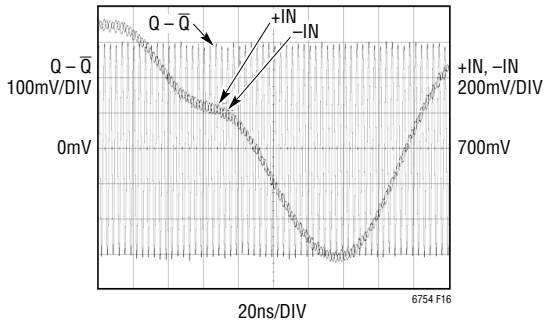
The LTC6754 includes 4.5mV of hysteresis to minimize instability. For the QFN package, a separate pin is available to set the hysteresis from 0mV (off) up to 40mV. The QFN version also features output latching to provide the ability to quickly capture the state of the comparator.

The dispersion of only 1ns combined with excellent propagation delay of 1.8ns makes the device an excellent choice for timing critical applications. Similarly, the 890Mbps toggle rate and low jitter of 1.5ps$_{RMS}$ (200mV$_{P-P}$, 245.76MHz input) make the LTC6754 ideally suited for high frequency line driver and clock recovery circuits.

TYPICAL APPLICATION

High Speed Differential Line Receiver and LVDS Translator with Excellent Common Mode Rejection





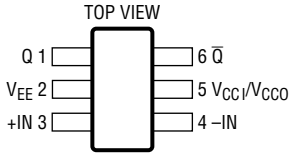
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Input Supply Voltage (V_{EE} to V_{CCI}) 5.5V
Total Output Supply Voltage (V_{EE} to V_{CCO}).....5.5V
Input Voltage
–IN, +IN, $\overline{LE}$/HYST, $\overline{SHDN}$.....V_{EE} – 0.3V, V_{CCI} + 0.3V
Input Current
–IN, +IN, $\overline{LE}$/HYST, $\overline{SHDN}$ (Note 2) ..... ±10mA
Output Current(Q, $\overline{Q}$)..... ±20mA

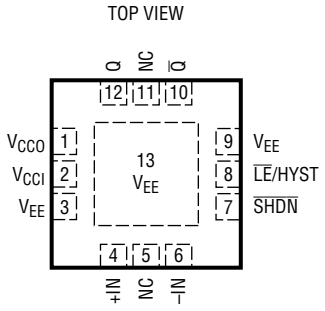
Operating Temperature Range (Note 3).. –40°C to 125°C
Specified Temperature Range (Note 4)
LTC6754I .....–40°C to 85°C
LTC6754H.....–40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Maximum Junction Temperature (Note 4) ..... 150°C
Lead Temperature Soldering
(10 sec) (SC70 Only).....300°C

PIN CONFIGURATION



SC6 PACKAGE
6-LEAD PLASTIC SC70

T_{JMAX} = 150°C, θ_{JA} = 256°C/W (NOTE 3)



UD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 68°C/W (NOTE 3)
EXPOSED PAD (PIN 13) IS V_{EE}, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6754ISC6#TRMPBF	LTC6754ISC6#TRPBF	LGVH	6-Lead Plastic SC-70	–40°C to 85°C
LTC6754HSC6#TRMPBF	LTC6754HSC6#TRPBF	LGVH	6-Lead Plastic SC-70	–40°C to 125°C
LTC6754IUD#PBF	LTC6754IUD#TRPBF	LGVJ	12-Lead Plastic QFN	–40°C to 85°C
LTC6754HUD#PBF	LTC6754HUD#TRPBF	LGVJ	12-Lead Plastic QFN	–40°C to 125°C

TRM = 500 pieces. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

(V_{CCI} = V_{CCO} = 5.0V) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C, $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size, R_L=100Ω , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CCI}–V_{EE}	Input Supply Voltage (Note 5)		●	2.4		5.25	V
V_{CCO}–V_{EE}	Output Supply Voltage (Note 5)		●	2.4		5.25	V
V_{CMR}	Input Voltage Range (Note 7)		●	V_{EE} – 0.2		V_{CCI} + 0.1	
V_{OS}	Input Offset Voltage (Note 6)		 ●	–4 –8.5	±0.75	4 8.5	mV mV
T_CV_{OS}	Input Offset Voltage Drift		●		18		µV/°C
V_{HYST}	Input Hysteresis Voltage (Note 5)	$\overline{LE}$/HYST pin floating			4.5		mV
C_{IN}	Input Capacitance				1.1		pF
R_{DM}	Differential Mode Resistance				55		kΩ
R_{CM}	Common Mode Resistance				6.5		MΩ
I_B	Input Bias Current	V_{CM} = V_{EE} + 0.3V	 ●	–3.8 –4	–1.8		µA µA
		V_{CM} = V_{CCI} – 0.3V	 ●		0.6	1.5 2.5	µA µA
I_{OS}	Input Offset Current		●	–0.7		0.7	µA
CMRR_LV$_{CM}$	Common Mode Rejection Ratio, Low V_{CM} Region	V_{CM} = V_{EE} – 0.2V to V_{CCI} – 1.5V	 ●	58 53	77		dB dB
CMRR_FR	Common Mode Rejection Ratio (Measured at Extreme Ends of V_{CMR})	V_{CM} = V_{EE} – 0.2V to V_{CCI}+0.1V	 ●	60 50	76.5		dB dB
PSRR	Power Supply Rejection Ratio	V_{CCI} = V_{CCO} Varied from 2.45V to 5.25V	 ●	62 59.5	80		dB dB
A_{VOL}	Open Loop Gain	Hysteresis Removed (Note 10)			53		dB
V_{OD}	Differential Output Voltage		●	260	362	420	mV
ΔV_{OD}	Difference in V_{OD} Between Complementary Output States		●	–15	±5	15	mV
V_{OCM}	Output Common Mode Voltage		●	1.18	1.26	1.31	V
ΔV_{OCM}	Difference in V_{OD} Between Complementary Output States		●	–10	±1.8	10	mV
I_{SC_VEE}	Short Circuit Current, through Either Output, both Outputs Connected to V_{EE}		●			20	mA
$I_{SC\_OUT\_SHORT}$	Output Current, Complementary Outputs Shorted		●			5	mA
I_{VCCI}	Input Stage Supply Current, Device On	Comparator On, Input Section Supply Current	 ●		2.4	2.9 3	mA mA
I_{VCCO}	Output Stage Supply Current, Device On	Comparator On, Output Section Supply Current	 ●		11	11.8 12.5	mA mA
I_{VCC}	Total Supply Current, Device On	Comparator On, Single Supply Pin Version,	 ●		13.4	14.7 15.5	mA mA
t_R, t_F	Rise/Fall Time	20% to 80%			0.77		ns
t_{PD}	Propagation Delay (Note 8)	$V_{OVERDRIVE}$ = 50mV	 ●		1.8	2.8 2.9	ns ns
$t_{SKEW\_RISEFALL}$	Propagation Delay Skew, Rising to Falling Transition				40		ps
t_{SKEW_COMP}	Propagation Delay Skew, Q to $\overline{Q}$				50		ps
t_{OD_DISP}	Overdrive Dispersion	Overdrive Varied from 10mV to 125mV			1		ns
t_{CM_DISP}	Common Mode dispersion	V_{CM} Varied from V_{EE} – 0.2V to V_{CCI} + 0.1V			200		ps
TR	Toggle Rate	V_{IN} = 200mV_{P-P} Sine Wave, 50% Output Swing			890		Mbps

ELECTRICAL CHARACTERISTICS

(V_{CCI} = V_{CCO} = 5.0V) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C, $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size, R_L=100Ω , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{JIT_RMS}	RMS Jitter, Sine Wave Input	V_{IN}=200mV_{P-P}					
		f_{IN}=245.76MHz, Jitter BW=10Hz–122.88MHz			1.53		ps
		f_{IN}=245.76MHz, Jitter BW=12kHz–20MHz			0.7		ps
		f_{IN}=100MHz, Jitter BW=10Hz–50MHz			2.2		ps
		f_{IN}=100MHz, Jitter BW=12kHz–20MHz			1.34		ps
		f_{IN}=61.44MHz, Jitter BW=10Hz–30.72MHz			2.93		ps
		f_{IN}=61.44MHz, Jitter BW=12kHz–20MHz			2.37		ps
		f_{IN}=10MHz, Jitter BW=10Hz–5MHz			20		ps
Latching/Adjustable Hysteresis Characteristics							
$V_{\overline{LE}/HYST}$	$\overline{LE}$/HYST Pin Voltage	Open Circuit	●	1.05	1.25	1.45	V
R_{HYST}	Resistor Value at $\overline{LE}$/HYST	$\overline{LE}$/HYST Pin Voltage < Open Circuit Value	●	11.6	14.5	17.6	kΩ
V_{HYST_LARGE}	Hysteresis Voltage	$V_{\overline{LE}/HYST}$ = 800mV			40		mV
V_{IL_LE}	Latch Pin Voltage, Latch Guaranteed		●			0.4	V
V_{IH_LE}	Latch Pin Voltage, Hysteresis Disabled		●	1.7			V
I_{IH_LE}	Latch Pin Current High	$V_{\overline{LE}/HYST}$ = 1.7V	●		31	70	µA
I_{IL_LE}	Latch Pin Current Low	$V_{\overline{LE}/HYST}$ = 0.4V	●	–75	–59		µA
t_{SETUP}	Latch Setup Time				2		ns
t_{HOLD}	Latch Hold Time				–2		ns
t_{PL}	Latch to Output Delay				3		ns
Shutdown Characteristics							
I_{SD_VCCI}	Shutdown Mode Input Stage Supply Current	$V_{\overline{SHDN}}$ = 0.8V			0.78	1.07	mA
			●			1.14	mA
I_{SD_VCCO}	Shutdown Mode Output Stage Supply Current	$V_{\overline{SHDN}}$ = 0.8V			270	410	µA
			●			430	µA
I_{SD_TOT}	Shutdown Mode Total Supply Current	$V_{\overline{SHDN}}$ = 0.8V			1.05	1.48	mA
			●			1.57	mA
t_{SD}	Shutdown Time	Output Hi-Z			110		ns
V_{IH_SD}	Shutdown Pin Voltage High	Part Guaranteed to be Powered On	●	2			V
V_{IL_SD}	Shutdown Pin Voltage Low	Part Guaranteed to be Powered Off				0.8	V
t_{WAKEUP}	Wake-Up Time from Shutdown	$V_{OVERDRIVE}$ = 100mV, Output Valid			120		ns

ELECTRICAL CHARACTERISTICS

(V_{CCI} = V_{CCO} = 2.5V) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C, $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size, R_L=100Ω , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CCI} – V_{EE}$	Input Supply Voltage (Note 5)		●	2.4		5.25	V
$V_{CCO} – V_{EE}$	Output Supply Voltage (Note 5)		●	2.4		5.25	V
V_{CMR}	Input Voltage Range (Note 7)		●	V_{EE} – 0.2		V_{CCI} + 0.1	
V_{OS}	Input Offset Voltage (Note 6)		 ●	–4.2 –7.5	±0.7	4.2 7.5	mV mV
T_CV_{OS}	Input Offset Voltage Drift		●		18		µV/°C
V_{HYST}	Input Hysteresis Voltage (Note 5)	$\overline{LE}$/HYST pin floating			4.9		mV
C_{IN}	Input Capacitance				1.1		pF
R_{DM}	Differential Mode Resistance				55		kΩ
R_{CM}	Common Mode Resistance				6.5		MΩ
I_B	Input Bias Current	V_{CM} = V_{EE} + 0.3V	 ●	–3.8 –4	–1.7		µA µA
		V_{CM} = V_{CCI} – 0.3V	 ●		0.5	1.3 2.3	µA µA
I_{OS}	Input Offset Current		●	–0.7		0.7	µA
CMRR_LVCM	Common Mode Rejection Ratio, Low V_{CM} Region	V_{CM} = V_{EE} – 0.2V to V_{CCI} – 1.5V	 ●	55 47	75		dB dB
CMRR_FR	Common Mode Rejection Ratio (Measured at Extreme Ends of V_{CMR})	V_{CM} = V_{EE} – 0.2V to V_{CCI}+0.1V	 ●	55 45.7	72		dB dB
PSRR	Power Supply Rejection Ratio	V_{CCI} = V_{CCO} Varied from 2.45V to 5.25V	 ●	62 59.5	80		dB dB
A_{VOL}	Open Loop Gain	Hysteresis Removed (Note 10)			53		dB
V_{OD}	Differential Output Voltage		●	260	345	420	mV
ΔV_{OD}	Difference in V_{OD} Between Complementary Output States		●	–15	±5	15	mV
V_{OCM}	Output Common Mode Voltage		●	1.18	1.25	1.31	V
ΔV_{OCM}	Difference in V_{OCM} Between Complementary Output States		●	–10	±1.8	10	mV
I_{SC_VEE}	Short Circuit Current, through Either Output, both Outputs Connected to V_{EE}		●			15.5	mA
$I_{SC\_OUT\_SHORT}$	Output Current, Complementary Outputs Shorted		●			5	mA
I_{VCCI}	Input Stage Supply Current, Device On	Comparator On, Input Section Supply Current	 ●		2.2	2.65 2.9	mA mA
I_{VCCO}	Output Stage Supply Current, Device On	Comparator On, Output Section Supply Current	 ●		10.4	11.5 11.7	mA mA
I_{VCC}	Total Supply Current, Device On	Comparator On, Single Supply Pin Version,	 ●		12.5	14.15 14.6	mA mA
t_R, t_F	Rise/Fall Time	20% to 80%			0.8		ns
t_{PD}	Propagation Delay (Note 8)	$V_{OVERDRIVE}$ = 50mV	 ●		2	2.9 3.0	ns ns
$t_{SKEW\_RISEFALL}$	Propagation Delay Skew, Rising to Falling Transition				50		ps
t_{SKEW_COMP}	Propagation Delay Skew, Q to $\overline{Q}$				40		ps
t_{OD_DISP}	Overdrive Dispersion	Overdrive Varied from 10mV to 125mV			1.1		ns
t_{CM_DISP}	Common Mode Dispersion	V_{CM} Varied from V_{EE} – 0.2V to V_{CCI} + 0.1V			200		ps
TR	Toggle Rate	V_{IN} = 200mV_{P-P} Sine Wave, 50% Output Swing			800		Mbps

ELECTRICAL CHARACTERISTICS

(V_{CCI} = V_{CCO} = 2.5V) The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C, $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size, R_L=100Ω , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{JIT_RMS}	RMS Jitter, Sine Wave Input	V_{IN}=200mV_{P-P}					
		f_{IN}=245.76MHz, Jitter BW=10Hz–122.88MHz			1.6		ps
		f_{IN}=245.76MHz, Jitter BW=12kHz–20MHz			0.73		ps
		f_{IN}=100MHz, Jitter BW=10Hz–50MHz			2.2		ps
		f_{IN}=100MHz, Jitter BW=12kHz–20MHz			1.36		ps
		f_{IN}=61.44MHz, Jitter BW=10Hz–30.72MHz			3		ps
		f_{IN}=61.44MHz, Jitter BW=12kHz–20MHz			2.4		ps
		f_{IN}=10MHz, Jitter BW=10Hz–5MHz			19		ps
Latching/Adjustable Hysteresis Characteristics							
$V_{\overline{LE}/HYST}$	$\overline{LE}$/HYST Pin Voltage	Open Circuit	●	1.05	1.25	1.45	V
R_{HYST}	Resistor Value at $\overline{LE}$/HYST	$\overline{LE}$/HYST Pin Voltage < Open Circuit Value	●	11.6	14.5	17.6	kΩ
V_{HYST_LARGE}	Hysteresis Voltage	$V_{\overline{LE}/HYST}$ = 800mV			43		mV
V_{IL_LE}	Latch Pin Voltage, Latch Guaranteed		●			0.4	V
V_{IH_LE}	Latch Pin Voltage, Hysteresis Disabled		●	1.7			V
I_{IH_LE}	Latch Pin Current High	$V_{\overline{LE}/HYST}$ = 1.7V	●		31	70	µA
I_{IL_LE}	Latch Pin Current Low	$V_{\overline{LE}/HYST}$ = 0.4V	●	–78	–58		µA
t_{SETUP}	Latch Setup Time				2		ns
t_{HOLD}	Latch Hold Time				–2		ns
t_{PL}	Latch to Output Delay				3		ns
Shutdown Characteristics							
I_{SD_VCCI}	Shutdown Mode Input Stage Supply Current	$V_{\overline{SHDN}}$ = 0.8V			650	880	µA
			●			970	µA
I_{SD_VCCO}	Shutdown Mode Output Stage Supply Current	$V_{\overline{SHDN}}$ = 0.8V			240	370	µA
			●			380	µA
I_{SD_TOT}	Shutdown Mode Total Supply Current	$V_{\overline{SHDN}}$ = 0.8V			0.89	1.25	mA
			●			1.35	mA
t_{SD}	Shutdown Time	Output Hi-Z			110		ns
V_{IH_SD}	Shutdown Pin Voltage High	Part Guaranteed to be Powered On	●	2			V
V_{IL_SD}	Shutdown Pin Voltage Low	Part Guaranteed to be Powered Off				0.8	V
t_{WAKEUP}	Wake-Up Time from Shutdown	$V_{OVERDRIVE}$ = 100mV, Output Valid			120		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Reverse biased ESD protection exists on all input, shutdown, latching/hysteresis and output pins. If the voltage on the input, shutdown, or latching/hysteresis pins goes beyond either input supply, the current should be limited to less than 10mA. This parameter is guaranteed to meet specification through design and/or characterization. It is not production tested.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating. This parameter is guaranteed to meet specified performance through design and/or characterization. It is not production tested.

Note 4: The LTC6754I is functional and guaranteed to meet specified performance from –40 °C to 85 °C. The LTC6754H is functional and guaranteed to meet specified performance from –40 °C to 125 °C.

Note 5: Supply voltage range is guaranteed by the PSRR test.

Note 6: Both hysteresis and offset are measured by determining positive and negative trip points (input values needed to change the output in the opposite direction). Hysteresis is defined as the difference of the two trip points and offset as the average of the two trip points.

Note 7: Guaranteed by CMRR spec.

Note 8: Propagation delays are measured with a step size of 150mV.

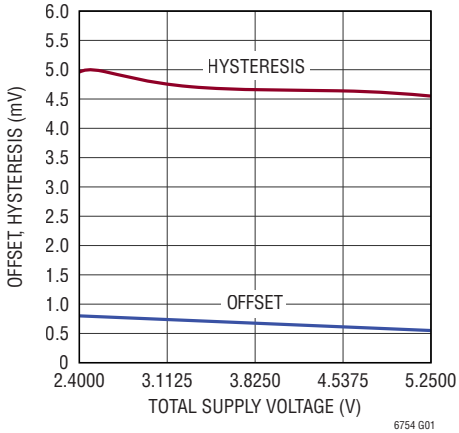
Note 9: Latch setup time is defined as the minimum time before the $\overline{LE}$/HYST pin is asserted low for an input signal change to be acquired and held at the output. Latch hold time is defined as the minimum time before an input signal change for a high to low transition on the $\overline{LE}$/HYST pin to prevent the output from changing. Latch enable pulse width is defined as the minimum time for the $\overline{LE}$/HYST pin to be held high for an input change to affect the output. See Figure 7 for a graphical definition of these terms.

Note 10: The devices have effectively infinite gain when hysteresis is enabled.

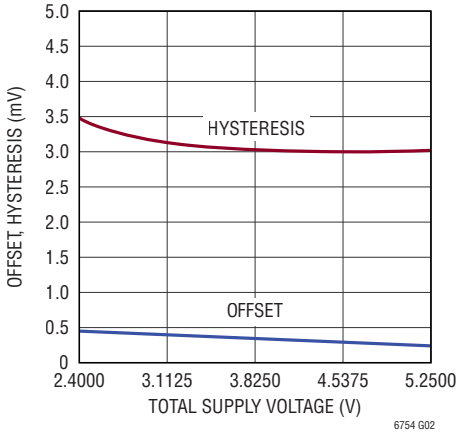
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CCI} = V_{CCO} = 5.0V$, $RL = 100\Omega$, $V_{OVERDRIVE} = 50mV$, $V_{CM} = 300mV$, unless otherwise noted.

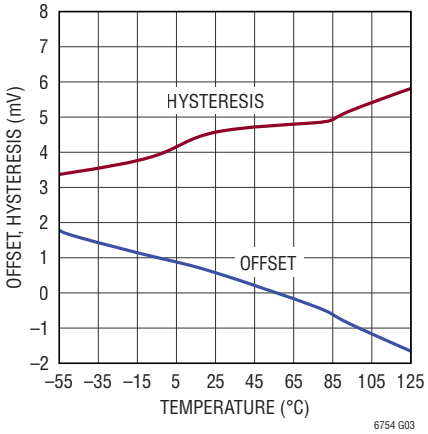
Input Offset and Hysteresis vs Supply Voltage, $V_{CM} = 0.3V$



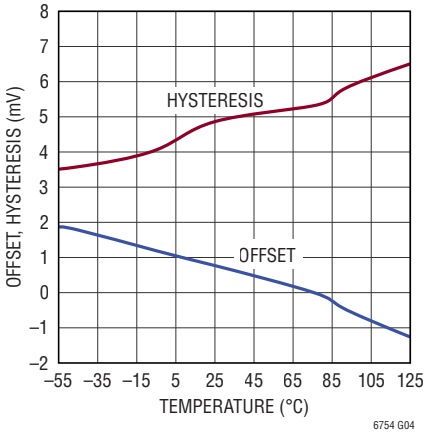
Input Offset and Hysteresis vs Supply Voltage, $V_{CM} = V_{CC} - 0.3V$



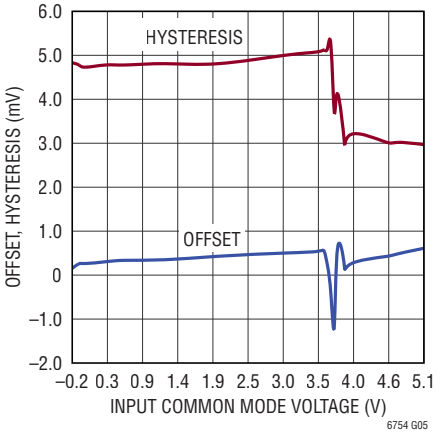
Input Offset and Hysteresis vs Temperature, $V_{CCI} = V_{CCO} = 5.0V$



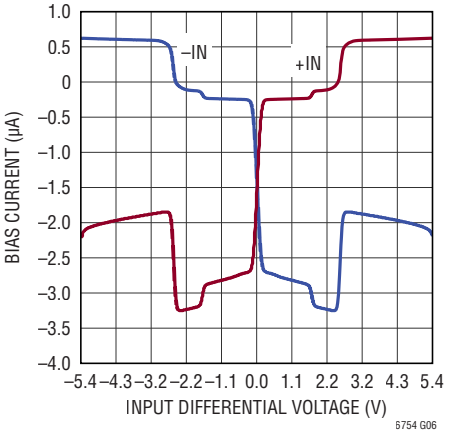
Input Offset and Hysteresis vs Temperature, $V_{CCI} = V_{CCO} = 2.5V$



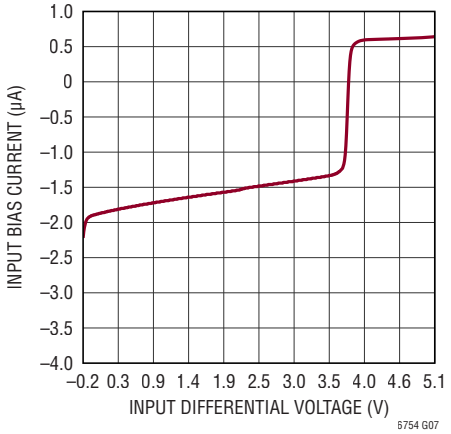
Input Offset, Hysteresis vs Input Common Mode Voltage



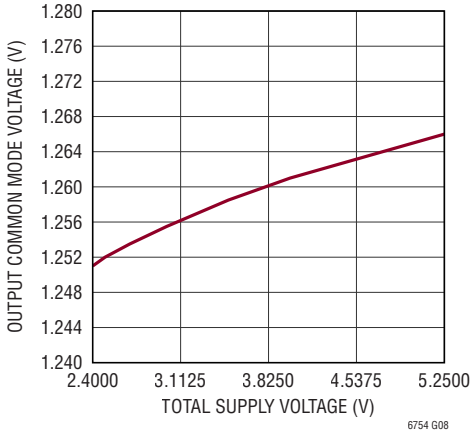
Input Bias Current vs Differential Voltage, $V_{CC} = 5.0V$



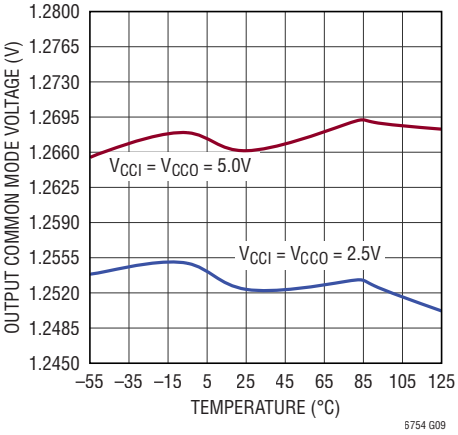
Input Bias Current vs Common Mode Voltage



Output Common Mode Voltage vs Supply Voltage



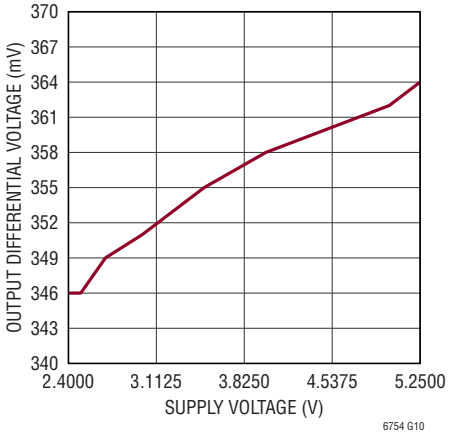
Output Common Mode Voltage vs Temperature



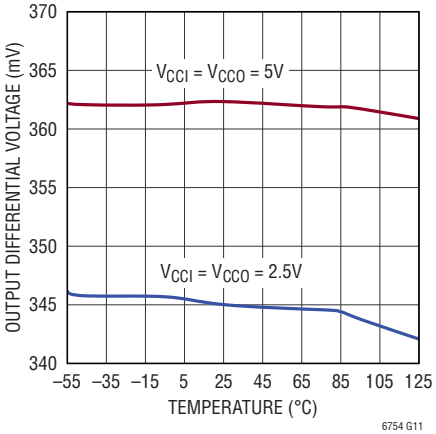
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CCI} = V_{CCO} = 5.0V$, $RL = 100\Omega$, $V_{OVERDRIVE} = 50mV$, $V_{CM} = 300mV$, unless otherwise noted.

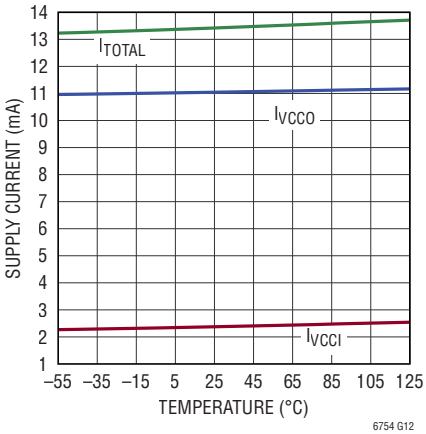
Output Differential Voltage vs Supply Voltage



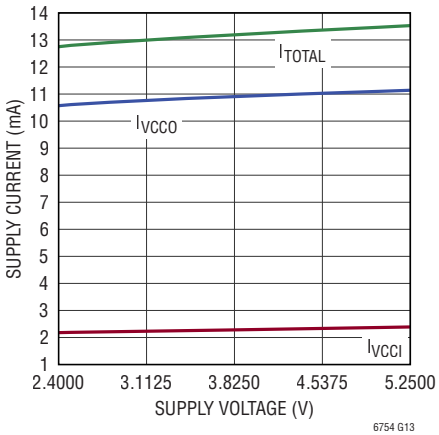
Output Differential Voltage vs Temperature



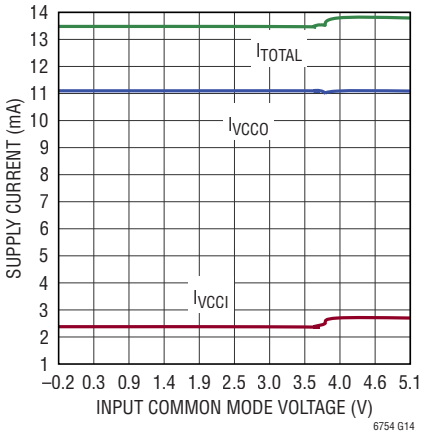
Supply Current vs Temperature



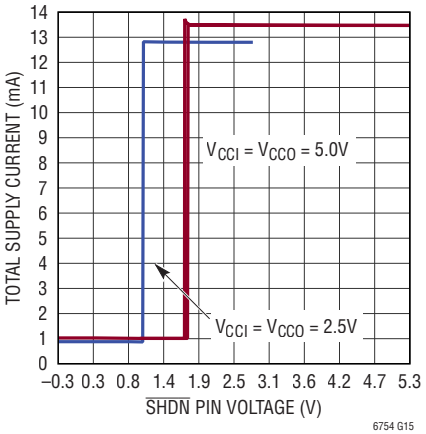
Supply Current vs Supply Voltage



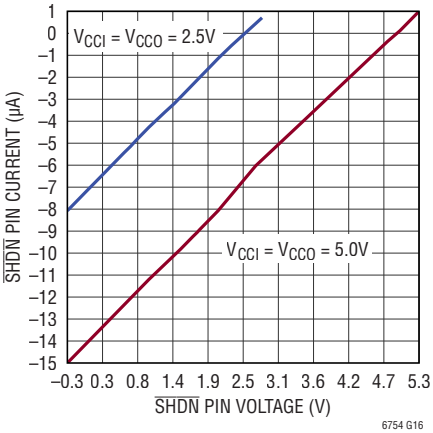
Supply Current vs Common Mode Voltage



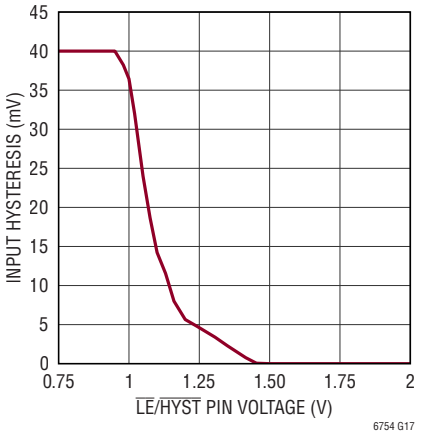
Total Supply Current vs $\overline{SHDN}$ Pin Voltage



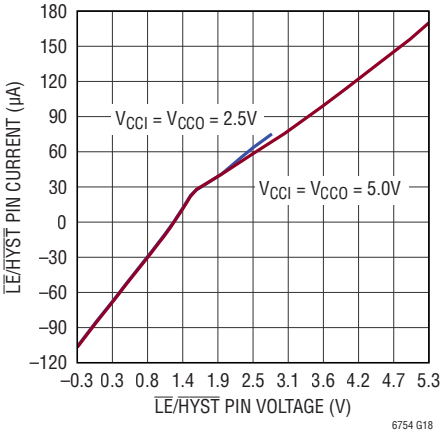
$\overline{SHDN}$ Pin I–V Characteristics



Input Hysteresis vs $\overline{LE/HYST}$ Pin Voltage



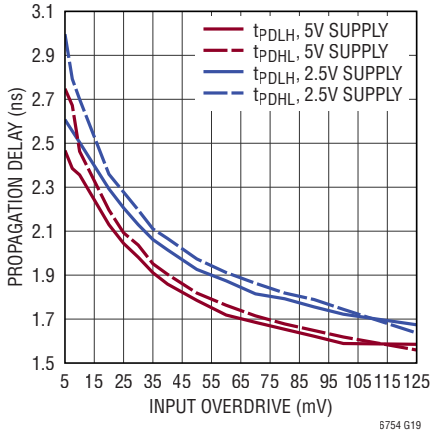
$\overline{LE/HYST}$ Pin I–V Characteristics



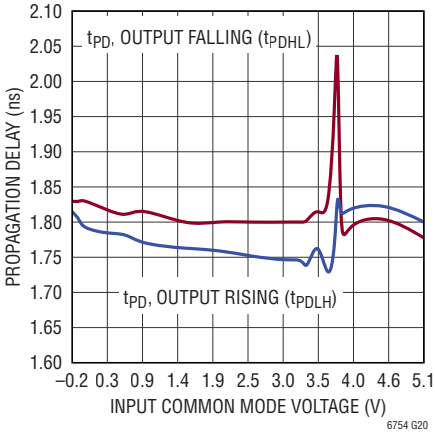
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CCI} = V_{CCO} = 5.0V, RL = 100Ω, $V_{OVERDRIVE}$ = 50mV, V_{CM} = 300mV, transient input voltage 50MHz, 150mV_{P-P} square wave unless otherwise noted.

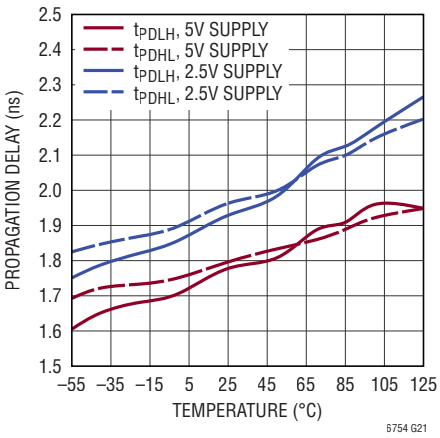
Propagation Delay vs Input Overdrive



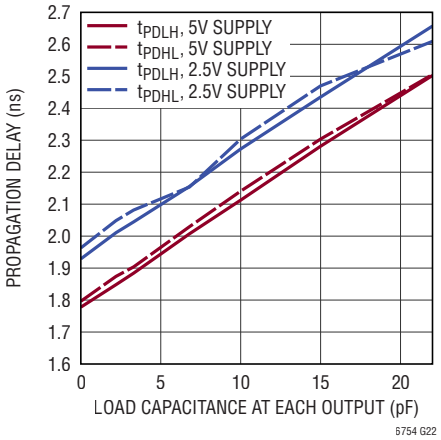
Propagation Delay vs Common Mode Voltage



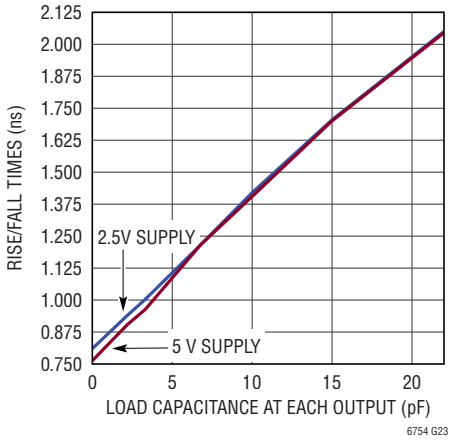
Propagation Delay vs Temperature



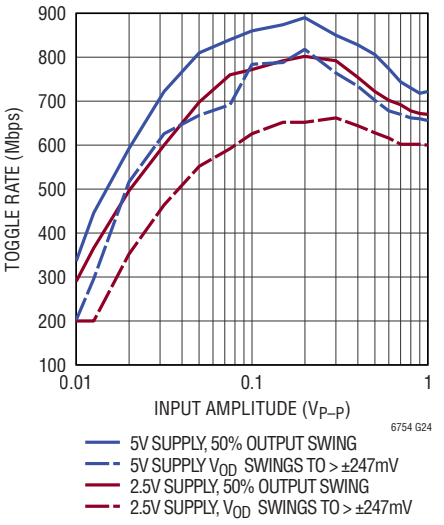
Propagation Delay vs Capacitive Load



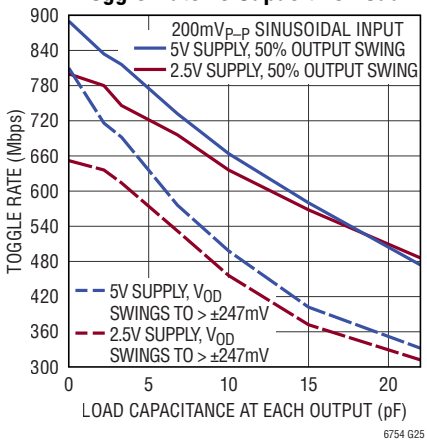
Rise/Fall Times vs Capacitive Load



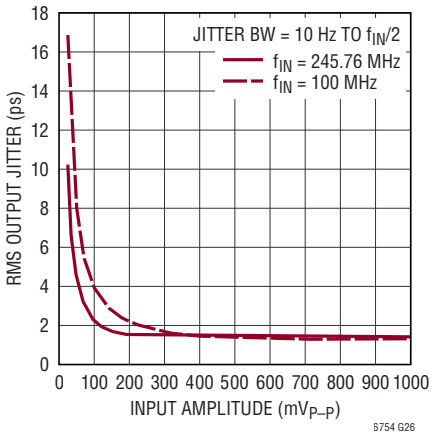
Toggle Rate vs Input Amplitude (Sinusoidal Input)



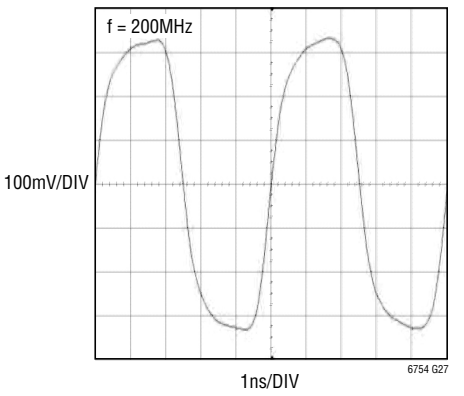
Toggle Rate vs Capacitive Load



Output Jitter vs Input Amplitude (Sinusoidal Input)



Differential Output Toggle Waveform



PIN FUNCTIONS (SC70/QFN)

+IN (Pin 3/Pin 4): Positive Input of the Comparator. The voltage range of this pin can go from V_{EE} (–0.2V) to V_{CCI} (+0.1V).

–IN (Pin 4/Pin 5): Negative Input of the Comparator. The voltage range of this pin can go from V_{EE} (–0.2V) to V_{CCI} (+0.1V).

V_{CCI} (Pin 5/Pin 2): Positive Supply Voltage for the Input Stage. The voltage between V_{CCI} and V_{EE} should be between 2.4V and 5.25V. This pin is combined with V_{CCO} in the SC70 package.

V_{CCO} (Pin 5/Pin 1): Positive Supply Voltage for the LVDS Output Stage. See the section High Speed Board Design Techniques for proper power supply layout and bypassing. The voltage between V_{CCO} and V_{EE} should be between 2.4V and 5.25V.This pin is combined with V_{CCI} in the SC70 package.

V_{EE} (Pin 2/Pins 3, 9): Negative Power Supply, normally tied to ground. This can be tied to a voltage other than ground as long as the constraints for total supply voltage relative to V_{CCI}/V_{CCO} are maintained.

$\overline{SHDN}$ (Pin 7) UD Only: Active Low Comparator Shutdown, threshold is 0.8V above V_{EE}. If left unconnected, the comparator will be fully powered up.

$\overline{LE}$/HYST (Pin 8) UD Only: This pin allows the user to adjust the comparator's hysteresis as well as latch the output if the pin voltage is pulled to within 400mV above V_{EE}. Hysteresis can be increased or disabled by voltage, current or a resistor to V_{EE}. Leaving the pin unconnected results in a typical hysteresis of 4.5mV.

Q (Pin 1/Pin 12): Positive Comparator Output. When the comparator outputs are differentially loaded with a 100Ω resistor, Q swings to V_{OCM} + V_{OD} / 2 when +IN > –IN and V_{OCM} – V_{OD} / 2 when +IN < –IN, where V_{OCM} and V_{OD} are typically 1.26V and 360mV respectively for a supply of 5V.

$\overline{Q}$ (Pin 6/Pin 10): Negative Comparator Output. When the comparator outputs are differentially loaded with a 100Ω resistor, $\overline{Q}$ swings to V_{OCM} + V_{OD} / 2 when +IN < –IN and V_{OCM} – V_{OD} / 2 when +IN > –IN, where V_{OCM} and V_{OD} are typically 1.26V and 360mV respectively for a supply of 5V.

BLOCK DIAGRAM

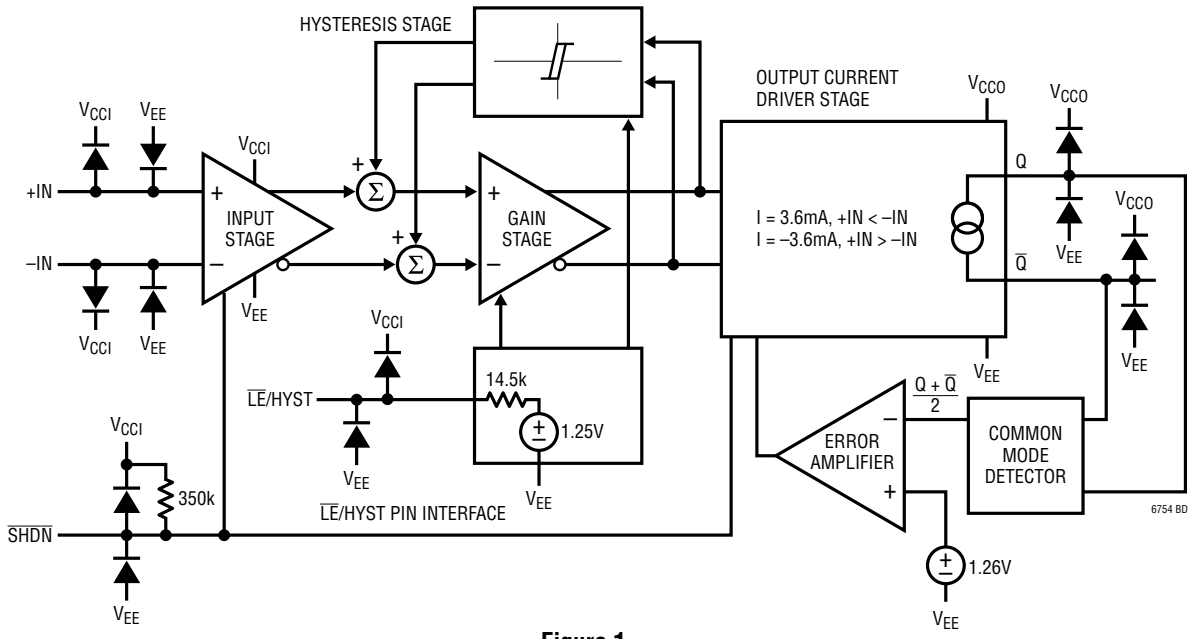


Figure 1.

APPLICATIONS INFORMATION

Circuit Description

The block diagram of the LTC6754 is shown in Figure 1. There are differential inputs (+IN, –IN), a negative power supply (V_{EE}), two positive supply pins: V_{CCI} for the input stage and V_{CCO} for the output stage, two output pins (Q and $\overline{Q}$), a pin for latching and adjusting hysteresis ($\overline{LE}$/HYST), and a pin to put the device in a low power mode ($\overline{SHDN}$). The signal path consists of a rail-to-rail input stage, an intermediate gain stage and an output driver stage to an output stage that sources or sinks 3.6mA between the two output pins, depending on the polarity of the differential input (+IN – –IN). The output stage also has a common mode feedback network that keeps the average of Q and $\overline{Q}$ approximately 1.26V. A Latching/Hysteresis interface block allows the user to latch the output state and/or remove or adjust the comparator input hysteresis. All of the internal signal paths make use of low voltage swings for high speed at low power.

Power Supply Configurations

The LTC6754UD (QFN Package) has separate positive supply pins for the input and output stages that allow for better isolation between the sensitive inputs and circuitry connected to the output load by removing a direct path for noise coupling through the positive supply. This feature also allows the user the ability to decouple input signal range from output stage power consumption (for example by using a 5.25V input supply to allow for > 5V common mode input range and a 2.4V output supply to minimize total power consumption). Figure 2 shows a few possible configurations.

For proper and reliable operation both supply pins should be between 2.4V and 5.25V above the negative supply pin. There are no restrictions regarding the sequence in which the positive or negative supplies are applied as long as the absolute maximum ratings are not violated.

Input Voltage Range and Offset

The LTC6754 family uses a rail-to-rail input stage that consists of a PNP pair and an NPN pair that are active over different input common mode ranges. The PNP pair is active for inputs between V_{EE} – 0.2V and approximately V_{CCI} – 1.5V (low common mode region of operation). The NPN pair is active for inputs between approximately V_{CCI} – 1V and V_{CCI} + 0.1V (high common mode region of operation). Partial activation of both pairs occurs when one input is in the low common mode region of operation and the other input is in the high common mode region of operation, or either of the inputs is between approximately V_{CCI} – 1.5V and V_{CCI} – 1V (transition region). The device has small, trimmed offsets as long as both inputs are completely in the low or high common mode region of operation. In the transition region, the offset voltage may increase. Applications that require good DC precision should avoid the transition region.

Input Bias Current

When both inputs are in the low common mode region, the input bias current is negative, with current flowing out of the input pins. When both inputs are in the high common mode region, the input bias current is positive, with current flowing into the input pins. The input stage has been designed to accommodate large differential input voltages without large increases in input bias current. With one input at the positive input supply rail and the other input at the negative supply rail, the magnitude of the input bias current at either pin is typically less than 3.5µA.

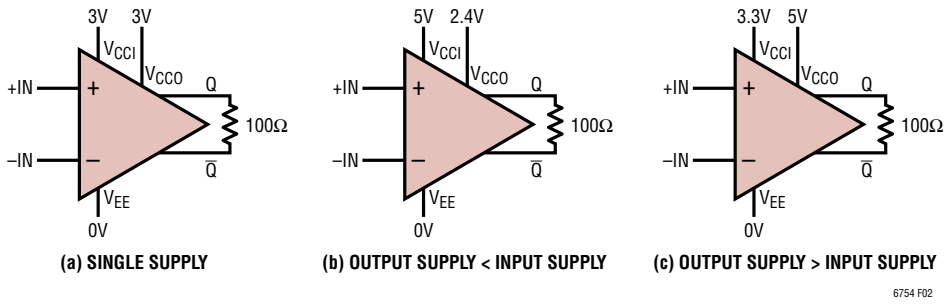


Figure 2. Typical Power Supply Configurations Applicable to the LTC6754UD (QFN Package)

APPLICATIONS INFORMATION

Input Protection

The input stage is protected against damage from conditions where the voltage on either pin exceeds the supply voltage (V_{EE} to V_{CCI}) without external protection. External input protection circuitry is only needed if input currents can exceed the absolute maximum rating. For example, if an input is taken beyond 300mV of either the positive or negative supply, an internal ESD protection diode will conduct and an external series resistor should be used to limit the current to less than 10mA.

Outputs

The LTC6754 has been designed for driving a 100Ω load connected between the output pins to standard LVDS levels, with a differential output voltage of 360mV and a common mode voltage of 1.26V, as described in the Circuit Description Section. See the section on High Speed Board Design Techniques for information on connecting the load to the output pins. The outputs should not be used as CMOS or TTL level outputs, and should not be used for sourcing or sinking excessive load currents.

ESD

The LTC6754 has reverse-biased ESD protection diodes on pins as shown in Figure 1.

There are additional clamps between the positive and negative supplies that further protect the device during ESD strikes. Hot-plugging of the device into a powered socket is not recommended since this can trigger the clamp resulting in large currents flowing between the supply pins.

Hysteresis

Comparators have very high open-loop gain. With slow input signals that are close to each other, input noise can cause the output voltage to switch randomly. Hysteresis is positive feedback that increases the trip point in the direction of the input signal transition when the output switches. This pulls the inputs away from each other, and prevents continuous switching back and forth. The addition of positive feedback also has the effect of making the small signal gain infinite around the trip points. Hysteresis is designed into most comparators and the LTC6754 has adjustable hysteresis with a default hysteresis of 4.5mV. The input-output transfer characteristic is illustrated in Figure 3 showing the definitions of V_{OS} and HYST based upon the two measurable trip points.

In some cases, additional noise immunity is required above what is provided by the nominal 4.5mV hysteresis. Conversely, when processing small or fast differential signals, hysteresis may need to be eliminated.

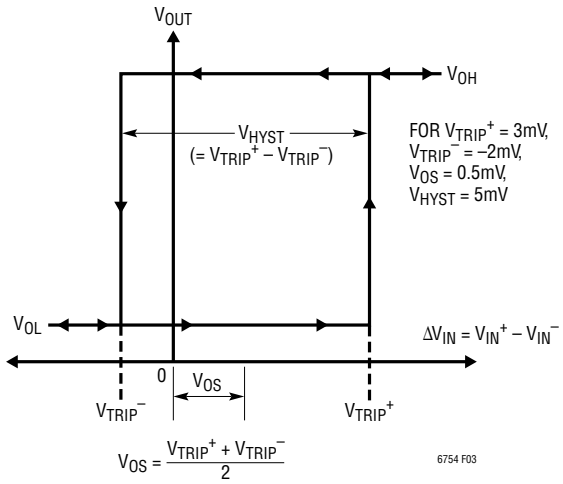


Figure 3.

The LTC6754UD (QFN package) provides a hysteresis pin, $\overline{LE}$/HYST, that can be used to increase the internal hysteresis, completely remove it, or enable the output to latch. The internal hysteresis is disabled when the $\overline{LE}$/HYST pin voltage is above 1.7V. Although eliminating hysteresis does reduce the voltage gain of the comparator to a finite value, in many cases it will be high enough (typically 450V/V) to amplify small input signals to valid LVDS levels. The output will latch when the $\overline{LE}$/HYST pin voltage is below 0.4V. The internal hysteresis will increase as the voltage of the pin is adjusted downward from its default open circuit value of 1.25V to 800mV.

APPLICATIONS INFORMATION

The $\overline{LE}$/HYST pin can be modeled as a 1.25V voltage source in series with a 15kΩ resistor. The simplest method to increase the internal hysteresis is to connect a single resistor between the $\overline{LE}$/HYST pin and V_{EE} to adjust hysteresis as shown in Figure 4. Figure 5 shows how hysteresis typically varies with the value of the resistor.

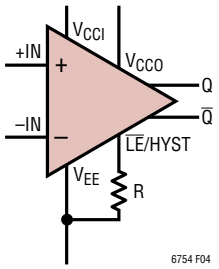


Figure 4. Adjusting Hysteresis Using an External Resistor at the $\overline{LE}$/HYST Pin

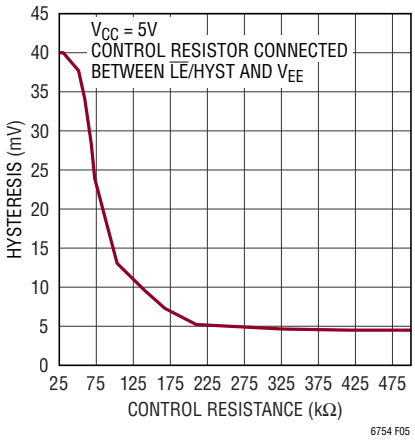


Figure 5. Hysteresis vs Control Resistance

Alternatively, additional hysteresis can be added by using positive feedback as shown in Figure 6.

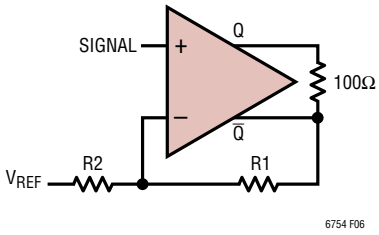


Figure 6. Additional Hysteresis Using positive Feedback

The offset and hysteresis become:

$$V_{OS\_FB} \approx \frac{V_{REF}R1 + V_{CM}R2}{R1+R2} + V_{OS}$$

$$V_{HYST\_FB} \approx \frac{V_{OD}R2}{R1+R2} + V_{HYST}$$

V_{OS_FB} and V_{HYST_FB} denote the values of offset and hysteresis with positive feedback present. V_{HYST} denotes the hysteresis of the device without positive feedback. V_{OCM} and V_{OD} are defined in the Electrical Characteristics Tables. Additional inaccuracies are introduced by ΔV_{OD} and ΔV_{OCM}, which are typically less than 5mV and 1.8mV, respectively. They typically will introduce only a few mV of error, which may be acceptable for large hysteresis settings in many applications.

In order to ensure that V_{OD} does not deviate too much from its value without positive feedback, R1 and R2 should be chosen such that the current through them is much less than 3.5mA by at least an order of magnitude. Extremely high resistance values however can degrade transient performance because of the phase shift caused by the resistors and device input capacitance.

For V_{REF} = 0V, V_{EE} = 0V, an increase in hysteresis of approximately 100mV can be obtained with R1 = 7.5kΩ and R2 = 3.01kΩ, assuming V_{OD} = 350mV and V_{OCM} = 1.25V. Offset induced is approximately 350mV. Similarly for V_{REF} = 1.25V, R2 = 5.9kΩ, R1 = 3.01kΩ, additional hysteresis of approximately 230mV can be obtained with an offset of approximately 1.25V.

APPLICATIONS INFORMATION

Latching

The internal latch of the LTC6754UD (QFN package) retains the output state when the $\overline{LE}$/HYST pin is taken to less than 400mV above the negative supply.

Figures 7a to 7e illustrate the latch timing definitions. The latch setup time is defined as the time for which the input should be stable before the latch pin is asserted low to ensure that the correct state will be held at the output. The latch hold time is the interval after which the latch pin is asserted in which the input signal must remain stable for the output to be the correct state at the time latch was asserted. The latch propagation delay (t_{PL}) is the time taken for the output to return to input control after the latch pin is released. Latching is disabled if the $\overline{LE}$/HYST pin is left floating.

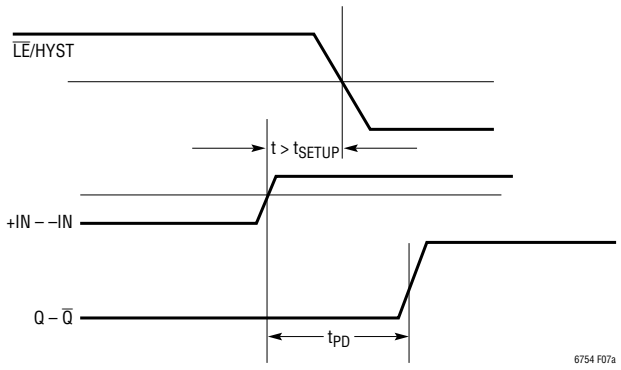


Figure 7a. Input State Change Properly Latched

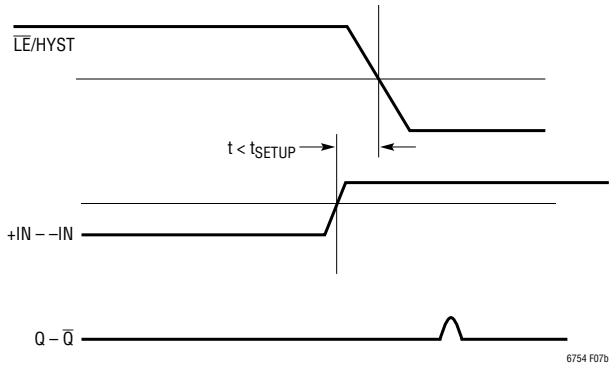


Figure 7b. Input State Change Setup Time Too Short

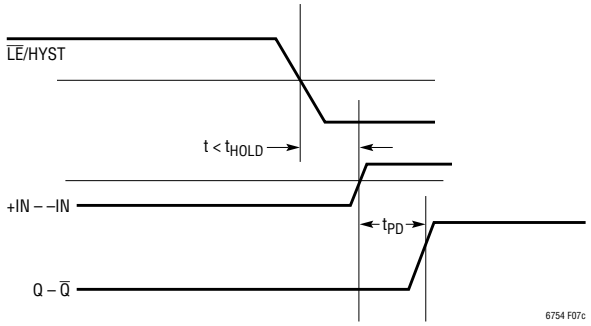


Figure 7c. Input State Not Held Long Enough, Wrong Output State Latched

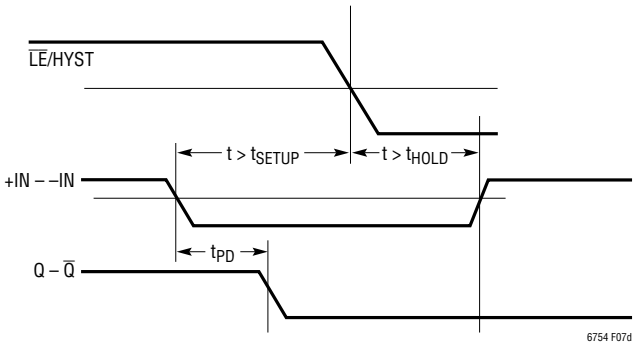


Figure 7d. Short Input Pulse Properly Captured and Latched

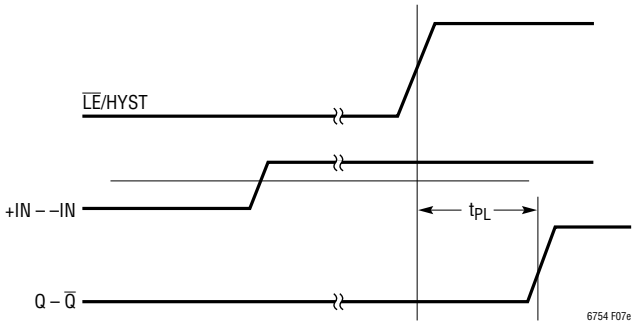


Figure 7e. Latched Output Disabled

APPLICATIONS INFORMATION

Shutdown

The LTC6754UD (QFN package) has a shutdown pin (SHDN, active low) that can reduce the total supply current to a typical value of only 1.05mA. When the part is in shutdown, the outputs are placed in a high impedance state. The shutdown pin needs to be taken to within 800mV of the negative supply for the part to shut down. When left floating, the shutdown pin is internally pulled towards the positive supply and comparators remain fully biased on.

Dispersion

Dispersion is defined as the change in propagation delay for different input overdrive or common mode conditions. It becomes very crucial in timing sensitive applications. Overdrive dispersion from 10mV overdrive to 125mV overdrive (150mV total step size) is typically 1ns. The graph titled Propagation Delay vs Common Mode voltage shows the dispersion due to shifts in input common mode voltage.

Jitter

The LTC6754 has been designed for low phase noise and jitter. This allows it to be used in applications where high frequency low amplitude sine waves need to be converted to full LVDS level outputs with minimal additive jitter. The graph titled Output Jitter vs Input Amplitude demonstrates the additive jitter of the LTC6754 for different amplitudes of a sinusoidal input. Refer to the Electrical Characteristics Table to see how jitter varies with signal frequency.

High Speed Board Design Techniques

In order to obtain optimal performance from the LTC6754, certain guidelines regarding signal routing and power supply bypassing should be carefully followed. If implemented properly, output signal integrity can be maintained, oscillations can be eliminated and electromagnetic interference due to fast switching at the outputs can be minimized.

The LTC6754 has been designed to drive LVDS loads. LVDS receivers are terminated with 100Ω loads connected differentially to the outputs of the transmitter. In order to obtain the fastest performance out of the LTC6754, the 100Ω load should be connected directly across the LTC6754's output pins (Q and $\overline{Q}$) if possible. Surface mounted resistors as opposed to leaded resistors are preferable due to lower parasitic inductances and capacitances. In many situations, however, it may not be possible to keep the LTC6754 close to the LVDS receiver. In such situations, 50Ω transmission lines should be used to route the outputs of the LTC6754 to the 100Ω receiver as shown in Figure 8. Since the outputs of the LTC6754 are fully differential in nature, each output sees a 50Ω load at the receiver. Using 50Ω characteristic impedance transmission lines minimizes reflections from the load and helps to maintain signal integrity. It is crucial, however, that the traces on both outputs be symmetrical, otherwise reflections may occur, since the broadband impedance seen by each single ended output would then deviate from 50Ω.

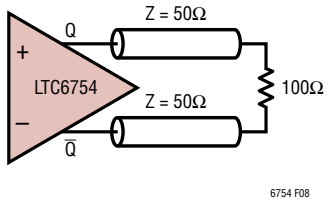


Figure 8. Routing LTC6754 Outputs to a 100Ω LVDS Receiver

Asymmetrical routing on the outputs should also be avoided as this reduces the extent to which EMI induced by the positive and negative outputs cancel each other.

Additional improvements in EMI can be obtained by shielding the output traces with a low impedance ground plane

Parasitic feedback between +IN and $\overline{Q}$ on one hand, and between –IN and Q on the other, should be minimized to avoid oscillations. If the inputs and complementary outputs can't be placed away from each other, a ground trace as a shield should be used to isolate them.

The positive supply pins should be adequately bypassed to the V_{EE} pin to minimize transients on the supply. Low ESR and ESL capacitors are required due to the high speed nature of the device.

Even a few nanohenries of parasitic trace inductance in series with the supply bypassing can cause several hundred millivolts of disturbance on the supply pins during output transitions, especially if the supply is used to power up other devices that are also switching. A 2.2µF capacitor

APPLICATIONS INFORMATION

in parallel with multiple low ESL, low ESR 100nF capacitors connected as close to the supply pins as possible to minimize trace impedance is recommended. In many applications the V_{EE} pin will be connected to ground. In applications where the V_{EE} pin is not connected to ground, the positive supplies should still be bypassed to V_{EE}. The V_{EE} pin should also then be bypassed to a ground plane with a 2.2µF capacitor in parallel with low ESL, low ESR 100nF capacitors if possible.

For devices with separate positive input and output supplies, bypass capacitors should be placed from each positive supply to V_{EE}. Capacitors should NOT be placed between the two positive supplies; otherwise disturbances due to output switching can couple back to the inputs.

When the input slew rate is small, sustained oscillations can occur at the output pin while the input is transitioning due to even one millivolt of ground bounce. For applications where the input slew rate is low, internal hysteresis should not be removed by taking the $\overline{LE}$/HYST pin high, as the addition of hysteresis makes the comparators more immune to disturbances such as ground bounce. Increasing hysteresis by adjusting the $\overline{LE}$/HYST pin voltage or by adding positive feedback as discussed in the section on hysteresis can further improve noise immunity. When adding positive feedback, surface mounted resistors should be used for R1 and R2 in Figure 6. The resistors should be as close to the device as possible.

TYPICAL APPLICATIONS

High Speed Clock Recovery and Level Translation Circuit

High speed comparators are often used in digital systems to recover distorted clock waveforms. The LTC6754 can be used to recover a distorted TTL clock signal, and translate it into a signal suitable for driving an LVDS receiver.

In this application, an input clock signal is required to drive an LVDS receiver. If the input signal gets distorted and its amplitude severely reduced due to stray capacitance, stray inductance or due to reflections on the transmission line, the LTC6754 can be used to convert it into a full scale LVDS signal that can drive the receiver.

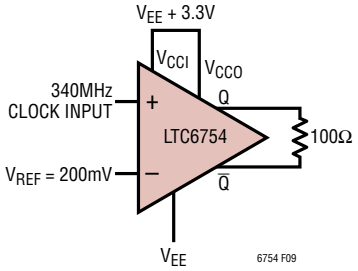


Figure 9. Corrupted Clock Recovery to LVDS Translator Circuit.

Figure 10 shows the input and output waveforms of the LTC6754, used to recover a 400mV$_{P-P}$ 340MHz (680Mbps) corrupted clock signal, into a full scale LVDS output signal. AC-coupling could have been used at the input of the comparator, however to preserve input duty cycle information DC-coupling may be preferable, and that is where having a wide input common mode range is an advantage. The input to output delay on the graph is larger than the actual propagation delay. The additional delay is due to the measurement cables.

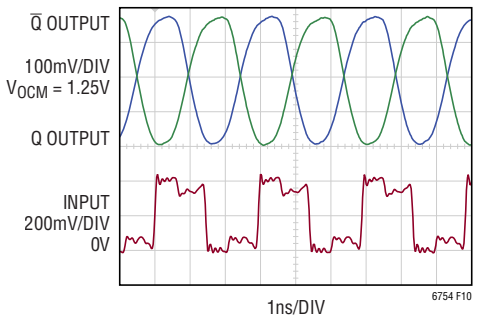


Figure 10. LVDS Output at 340MHz

TYPICAL APPLICATIONS

Optical Receiver Circuit

The LTC6754, along with a high speed high performance FET input operational amplifier like the LTC6268-10, can be used to implement an optical receiver as shown in Figure 11.

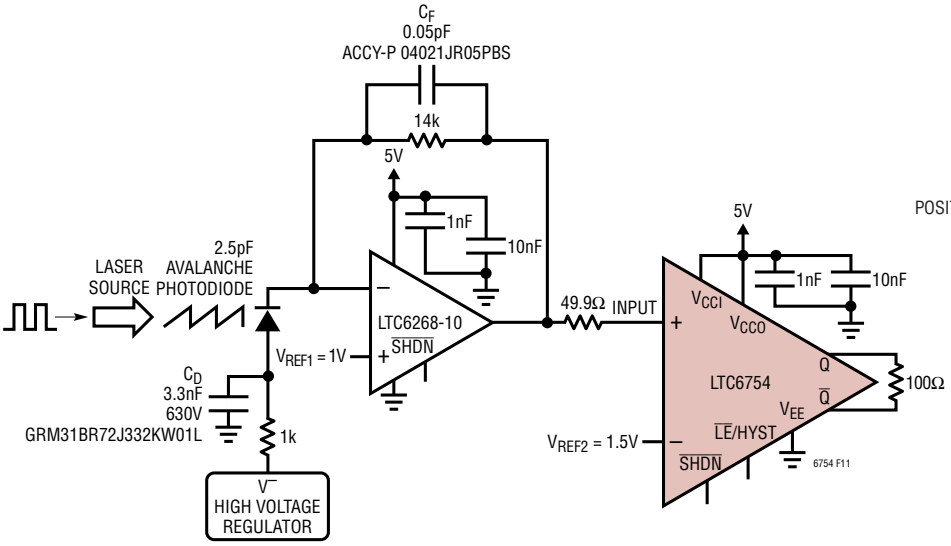


Figure 11. Optical Receiver Circuit

Figure 12 shows the output of the LTC6268-10 driving the +IN pin of the LTC6754 and the LTC6754 outputs. The photodiode is being driven by a pulsed laser.

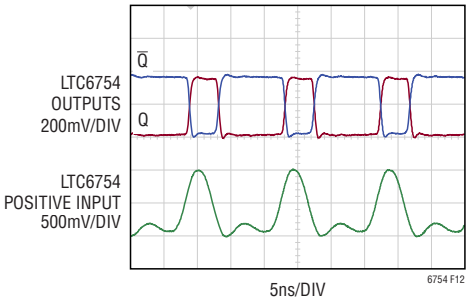


Figure 12. Optical Receiver with LVDS Output

High Performance Sine Wave to LVDS Converter with Low Phase Shift over Amplitude

The LTC6754 can be used to convert low level sine waves to full scale LVDS signals as in Figure 13. The amplitude of the incoming sinusoidal signal was varied from 100mV$_{P-P}$ to 800mV$_{P-P}$, with the frequency being 50MHz. Figure 14 shows a plot of the phase difference between the output and input, normalized to the phase difference for an 800mV$_{P-P}$ signal, versus input amplitude. The phase difference across a 16.47dB span (120mV$_{P-P}$ to 800mV$_{P-P}$) is only 3.06°.

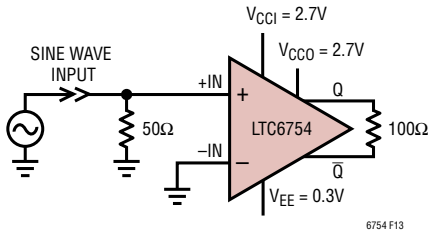


Figure 13. High Performance Sine Wave to LVDS Converter

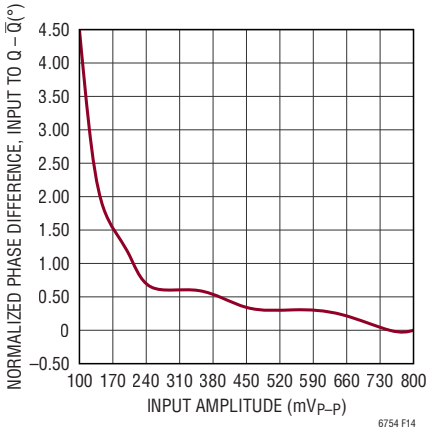


Figure 14. Phase Difference Between the Output and Input

TYPICAL APPLICATIONS

Common Mode Rejecting Line Receiver

Differential electrical signals being transmitted over long cables are often attenuated. Electrical noise on the cables can take the form of common mode signals.

The LTC6754 comparators can be used to retrieve attenuated differential signals that have been corrupted by high frequency common mode noise, as shown in Figure 15.

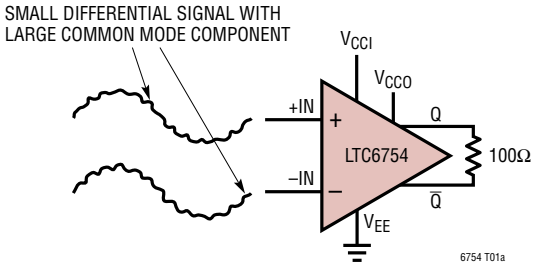


Figure 15. Common Mode Rejecting Line Receiver

Figure 16 shows the inputs and outputs of an LTC6754 retrieving a 300MHz, 140mV$_{P-P}$ differential input signal that has 1.3V of random, common mode noise superimposed on it. The supply used was 3.0V (V_{CCI} and V_{CCO}).

A small amount of modulation is seen at the output due to a small amount of differential modulation at the inputs, which causes cycle to cycle variations in propagation delay.

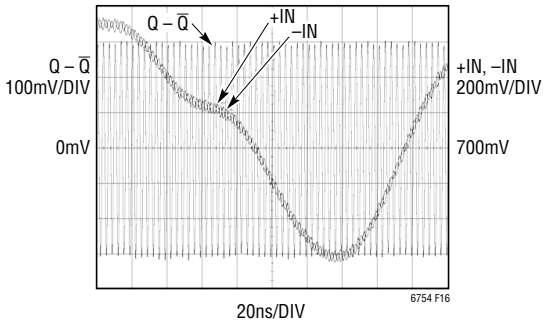


Figure 16.

Logic Clock Source to LVDS Cable Driver and Receiver

Figure 17 shows a 250MHz 1.8V logic clock signal being driven across 8 feet of differential Cat6 cable to generate a 250MHz LVDS clock signal at the receiver end.

Both the cable driver and LVDS receiver are implemented using LTC6754's. Figure 18 shows the input clock signal to the cable driver and the outputs of the receiver.

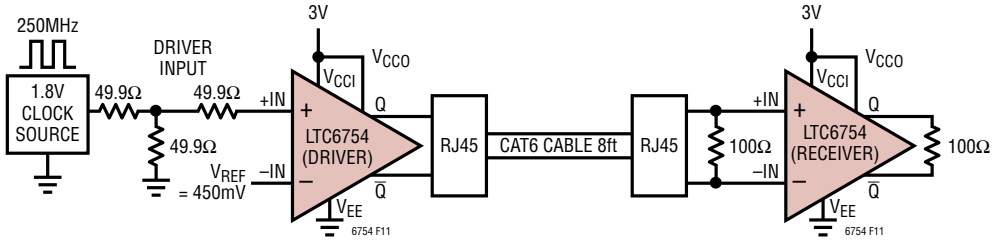


Figure 17. Logic Clock Source to LVDS Cable Driver and Receiver

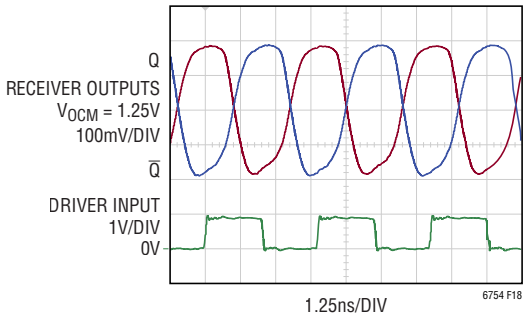


Figure 18. LVDS Receiver Output, 250MHz

TYPICAL APPLICATIONS

Short Pulse to Differential Cable Driver and CMOS Output Receiver

Figure 19 shows a low amplitude short duration pulse being transmitted over 8 feet of Cat6 differential cable and converted to a full level CMOS output signal. The pulse is applied to the input of an LTC6754. A 150Ω resistor is used along with the 1pF input capacitance of the LTC6754 to limit the rise time at the positive input of the LTC6754, in order to minimize coupling between the input and other nodes in the system.

The LTC6754 is used to drive 8 feet of cable terminated in a 100Ω resistive load at the inputs of an LTC6752-2, which generates a full scale CMOS logic signal at its output.

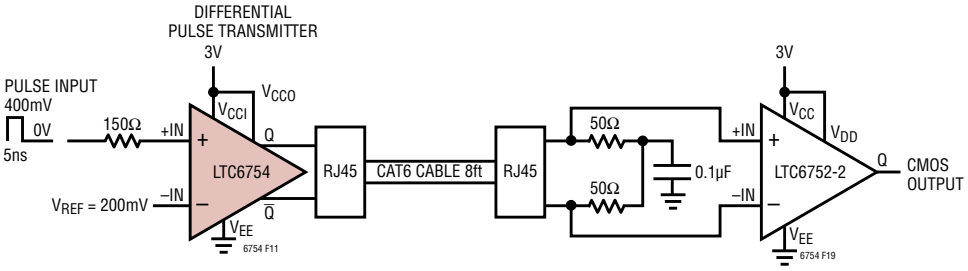


Figure 19. Short Pulse to Differential Cable Driver and CMOS Output Receiver

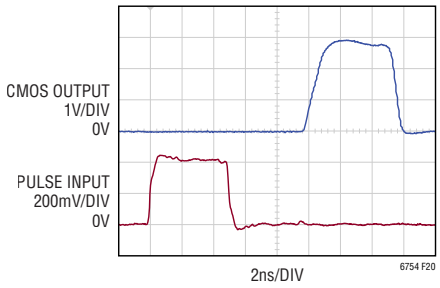
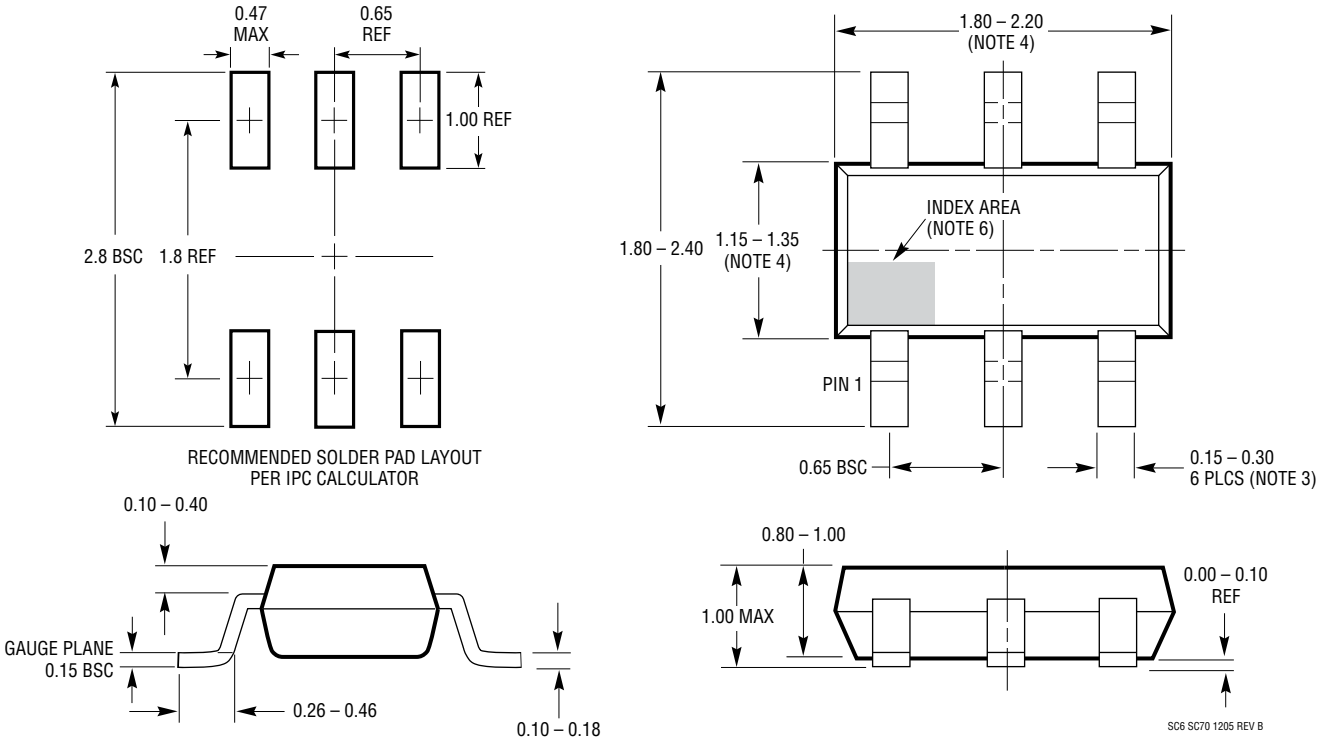


Figure 20. Pulse Input and Output

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

SC6 Package
6-Lead Plastic SC70
(Reference LTC DWG # 05-08-1638 Rev B)

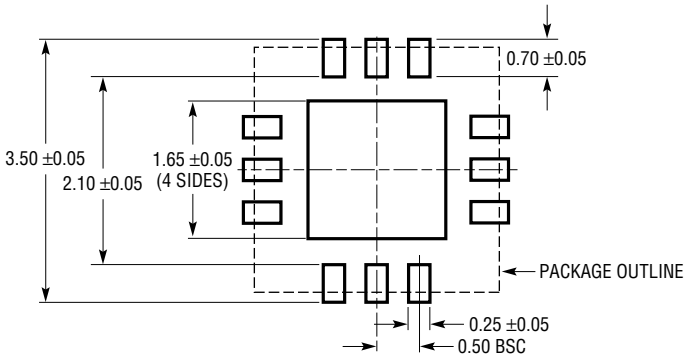


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. DETAILS OF THE PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE INDEX AREA
7. EIAJ PACKAGE REFERENCE IS EIAJ SC-70
8. JEDEC PACKAGE REFERENCE IS MO-203 VARIATION AB

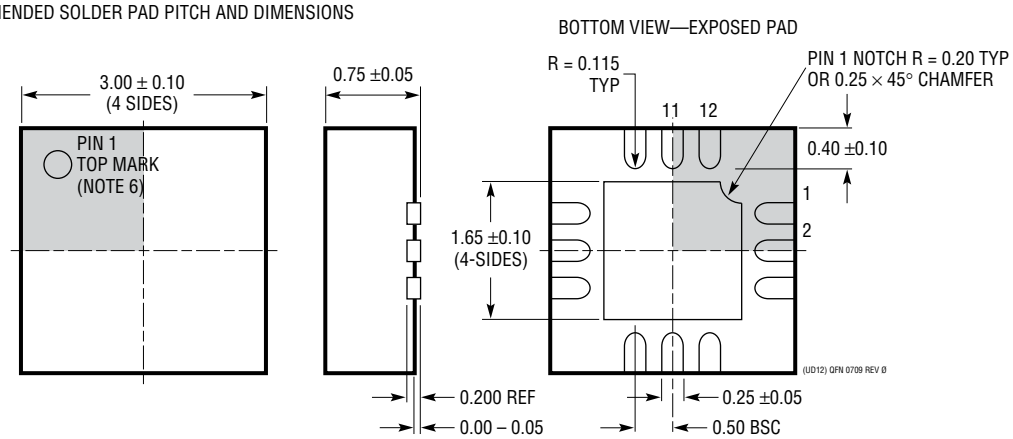
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
12-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1855 Rev Ø)



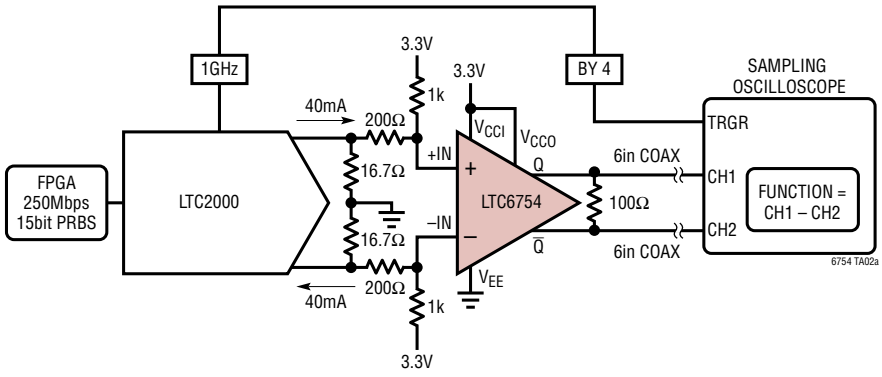
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

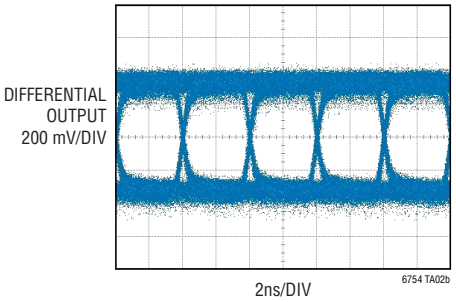


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

15 Bit PRBS 250Mbps Logic Signal to LVDS Converter Eye Diagram Test Setup





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
High Speed Comparators		
LTC6752/LTC6752-1/ LTC6752-2/LTC6752-3/ LTC6752-4	2.9ns 280MHz CMOS Output Comparators	RR Inputs. Can drive 1.8V logic directly (LTC6752-2/LTC6752-3/LTC6752-4)
LT1715	4ns 150MHz Dual Comparators	4.6mA at 3V
LT1720/LT1721	Dual/Quad 4.5ns Single Supply Comparators	4mA/Comparator
LT1711	High Speed Rail-to-Rail Comparators	3V/5V/±5V, 4.5ns at 20mV Overdrive
LT1116	12ns Single Supply Ground Sensing Comparator	Inputs Can Exceed Positive Supply Up to 15V Without Damaging Device
Clock Buffers/Logic Converters		
LTC6957-1/LTC6957-2/ LTC6957-3/LTC6957-4	Low Phase Noise, Dual Output Buffer/Driver/Logic Converter	LVPECL/LVDS/CMOS Outputs, Additive Jitter 45 fs_{RMS}
High Speed Operational Amplifiers		
LTC6252/LTC6253/ LTC6254	Single/Dual/Quad 3.5mA 720 MHz	280V/µs, 2.75nV/√Hz, Rail-to-Rail I/O
LTC6268/LTC6269	Single/Dual 500MHz Ultra Low Bias Current	RR Outputs
LTC6268-10/LTC6269-10	Single/Dual 4GHz Ultra Low Bias Current	RR Outputs, Gain of 10 Stable
LTC6246/LTC6247/ LTC6248	Single/Dual/Quad 1mA, 180MHz	90V/µs, 4.2nV/√Hz,Rail-to-Rail I/O

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(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC6754
LT 0815 • PRINTED IN USA