256Kx8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

JULY 2015

KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 9 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V-2.2V VDD (IS62/65WV2568EALL)
  - 2.2V-3.6V VDD (IS62/65WV2568EBLL)
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

DESCRIPTION

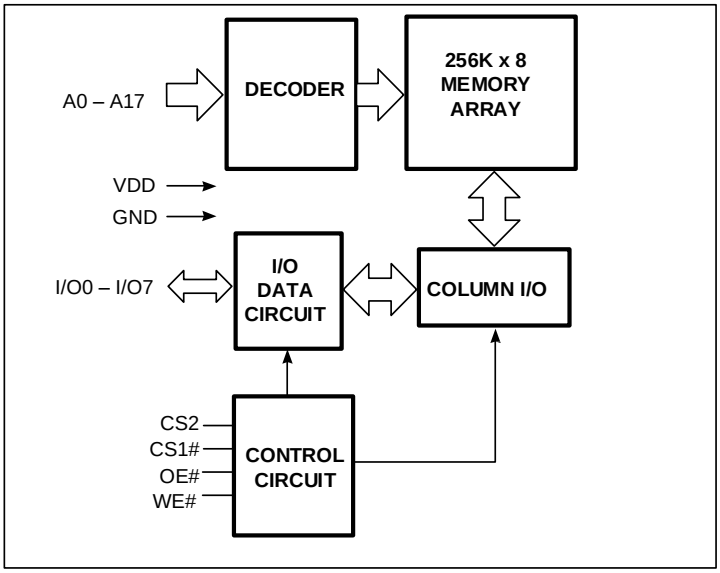
The *ISSI* IS62/65WV2568EALL/EBLL are high-speed, 2M bit static RAMs organized as 256K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS1# is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory.

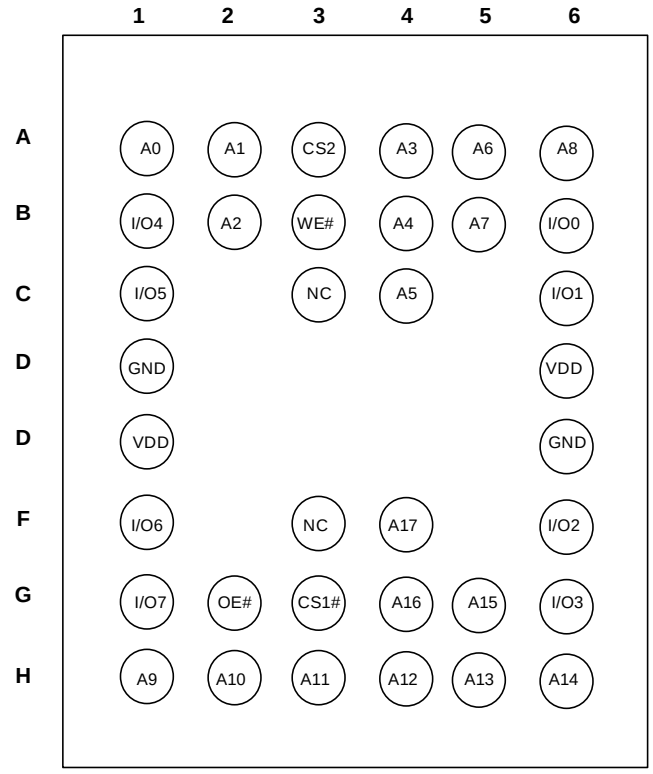
The IS62/65WV2568EALL/EBLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), sTSOP (TYPE I), and 36-pin mini BGA..

FUNCTIONAL BLOCK DIAGRAM

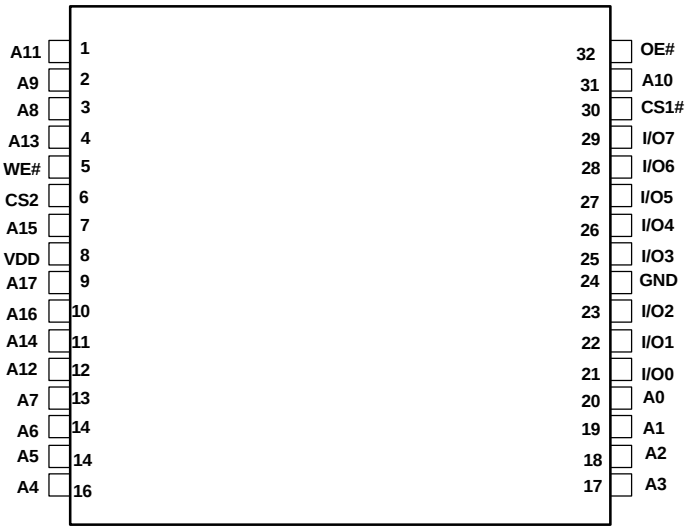


PIN CONFIGURATIONS

48-Pin mini BGA (6mm x 8mm)



32-Pin TSOP (Type I), STSOP (Type I)



PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O7	Data Inputs/Outputs
CS1#, CS2	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
NC	No Connection
V_{DD}	Power
GND	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS1# HIGH or CS2 LOW). The input and output pins (I/O0-7) are placed in a high impedance state. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input LOW. The input and output pins(I/O0-7) are in data input mode. Output buffers are closed during this time even if OE# is LOW.

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READ MODE

Read operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

Mode	CS1#	CS2	WE#	OE#	I/O0-I/O7	VDD Current
Not Selected	H	X	X	X	High-Z	ISB1,ISB2
	X	L	X	X	High-Z	
Output Disabled	L	H	H	H	High-Z	ICC
Write	L	H	H	L	DIN	ICC
Read	L	H	L	X	DOUT	ICC

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to GND	–0.2 to +3.9(V_{DD}+0.3V)	V
tBIAS	Temperature Under Bias	–55 to +125	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.9(V_{DD}+0.3V)	V
tStg	Storage Temperature	–65 to +150	°C
I_{OUT}(2)	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This condition is not per pin. Total current of all pins must meet this value.

OPERATING RANGE(1)

Range	Device Marking	Ambient Temperature	VDD
Commercial	IS62WV2568EALL	0°C to +70°C	1.65V-2.2V
Industrial	IS62WV2568EALL	-40°C to +85°C	1.65V-2.2V
Automotive	IS65WV2568EALL	-40°C to +125°C	1.65V-2.2V
Commercial	IS62WV2568EBLL	0°C to +70°C	2.2V-3.6V
Industrial	IS62WV2568EBLL	-40°C to +85°C	2.2V-3.6V
Automotive	IS65WV2568EBLL	-40°C to +125°C	2.2V-3.6V

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	10	pF
DQ capacitance (IO0–IO7)	$C_{I/O}$		10	pF

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

ELECTRICAL CHARACTERISTICS

IS62(5)WV2568EALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

IS62(5)WV2568EBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.2 ≤ V_{DD} < 2.7, I_{OH} = -0.1 mA	2.0	—	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OH} = -1.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	2.2 ≤ V_{DD} < 2.7, I_{OL} = 0.1 mA	—	0.4	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OL} = 2.1 mA	—	0.4	V
V_{IH}(1)	Input HIGH Voltage	2.2 ≤ V_{DD} < 2.7	1.8	V_{DD} + 0.3	V
		2.7 ≤ V_{DD} ≤ 3.6	2.2	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage	2.2 ≤ V_{DD} < 2.7	–0.3	0.6	V
		2.7 ≤ V_{DD} ≤ 3.6	–0.3	0.8	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
2. VILL(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

IS62(5)WV2568EALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	Typ.	Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max , f = f_{MAX} , CS1# = $V_{IL,}$ CS2 = V_{IH} I_{OUT} = 0 mA	Com.	12	15	mA
			Ind.	-	18	
			Auto.	-	25	
ICC1	V_{DD} Static Operating Supply Current	V_{DD} = Max , f = 0, CS1# = $V_{IL,}$ CS2 = V_{IH} I_{OUT} = 0 mA	Com.	1	3	mA
			Ind.	-	3	
			Auto.	-	4	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max, f = 0 CS1# ≥ V_{DD} - 0.2V or CS2 ≤ 0.2V VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	Com.	2	5	µA
			Ind.	-	12	µA
			Auto.	-	25	µA

Note:
Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25°C

IS62(5)WV2568EBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	Typ.	Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max , f = f_{MAX} , CS1# = $V_{IL,}$ CS2 = V_{IH} I_{OUT} = 0 mA	Com.	12	15	mA
			Ind.	-	18	
			Auto.	-	25	
ICC1	V_{DD} Static Operating Supply Current	V_{DD} = Max , f = 0, CS1# = $V_{IL,}$ CS2 = V_{IH} I_{OUT} = 0 mA	Com.	1	3	mA
			Ind.	-	3	
			Auto.	-	4	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max, f = 0 CS1# ≥ V_{DD} - 0.2V or CS2 ≤ 0.2V VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	Com.	2	5	µA
			Ind.	-	12	µA
			Auto.	-	25	µA

Note:
Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25℃

AC CHARACTERISTICS[6] (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	45	-	55	-	ns	1,5
Address Access Time	tAA	-	45	-	55	ns	1
Output Hold Time	tOHA	8	-	8	-	ns	1
CS1#, CS2 Access Time	tACS1/ACS2	-	45	-	55	ns	1
OE# Access Time	tDOE	-	22	-	25	ns	1
OE# to High-Z Output	tHZOE	-	18	-	18	ns	2
OE# to Low-Z Output	tLZOE	5	-	5	-	ns	2
CS1#, CS2 to High-Z Output	tHZCS1/HZCS2	-	18	-	18	ns	2
CS1#, CS2 to Low-Z Output	tLZCS/LZCS2	10	-	10	-	ns	2

WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Write Cycle Time	tWC	45	-	55	-	ns	1,3,5
CS1#, CS2 to Write End	tSCS1/tSCS2	35	-	40	-	ns	1,3
Address Setup Time to Write End	tAW	35	-	40	-	ns	1,3
Address Hold from Write End	tHA	0	-	0	-	ns	1,3
Address Setup Time	tSA	0	-	0	-	ns	1,3
WE# Pulse Width	tPWE	35	-	40	-	ns	1,3,4
Data Setup to Write End	tSD	28	-	28	-	ns	1,3
Data Hold from Write End	tHD	0	-	0	-	ns	1,3
WE# LOW to High-Z Output	tHZWE	-	18	-	18	ns	2,3
WE# HIGH to Low-Z Output	tLZWE	10	-	10	-	ns	2,3

Notes:

1 Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of CS1# = LOW, CS2=HIGH, and WE# = LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE# is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Symbol	Conditions	Units
Input Rise Time	T_R	1.0	V/ns
Input Fall Time	T_F	1.0	V/ns
Output Timing Reference Level	V_{REF}	½ V_{TM}	V
Output Load Conditions	Refer to Figure 1 and 2		

OUTPUT LOAD CONDITIONS FIGURES

Figure1

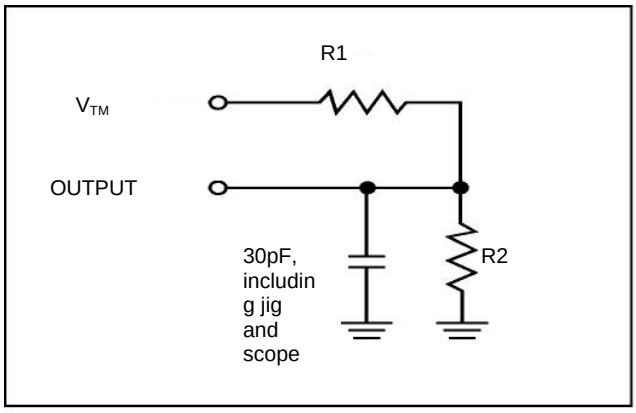
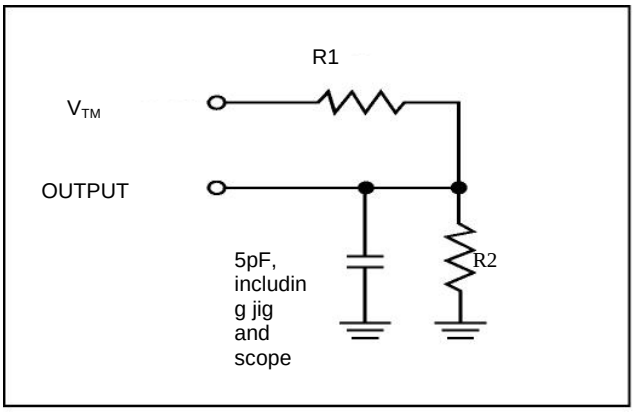


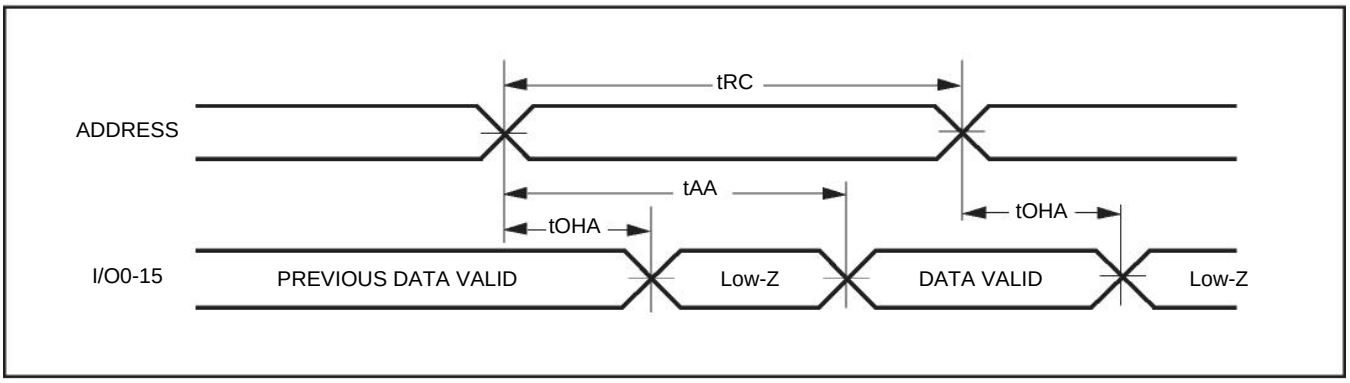
Figure2



Parameters	V_{DD}=1.65~1.98V	V_{DD}=2.2~2.7V	V_{DD}=2.7~3.6V
R1	13500Ω	16667Ω	1103Ω
R2	10800Ω	15385Ω	1554Ω
V_{TM}	VDD	VDD	VDD

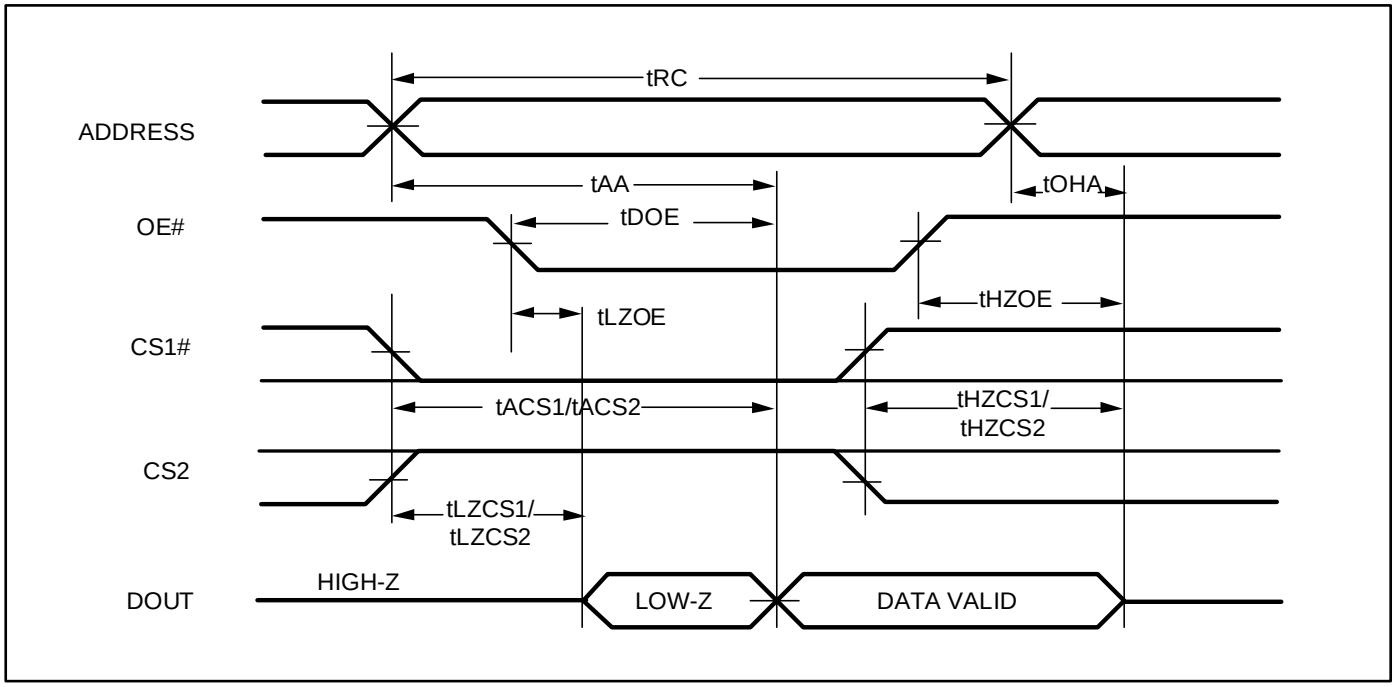
TIMING DIAGRAM

READ CYCLE NO. 1[1] (ADDRESS CONTROLLED) (CS1# = OE# = LOW, CS2 = WE# = HIGH)



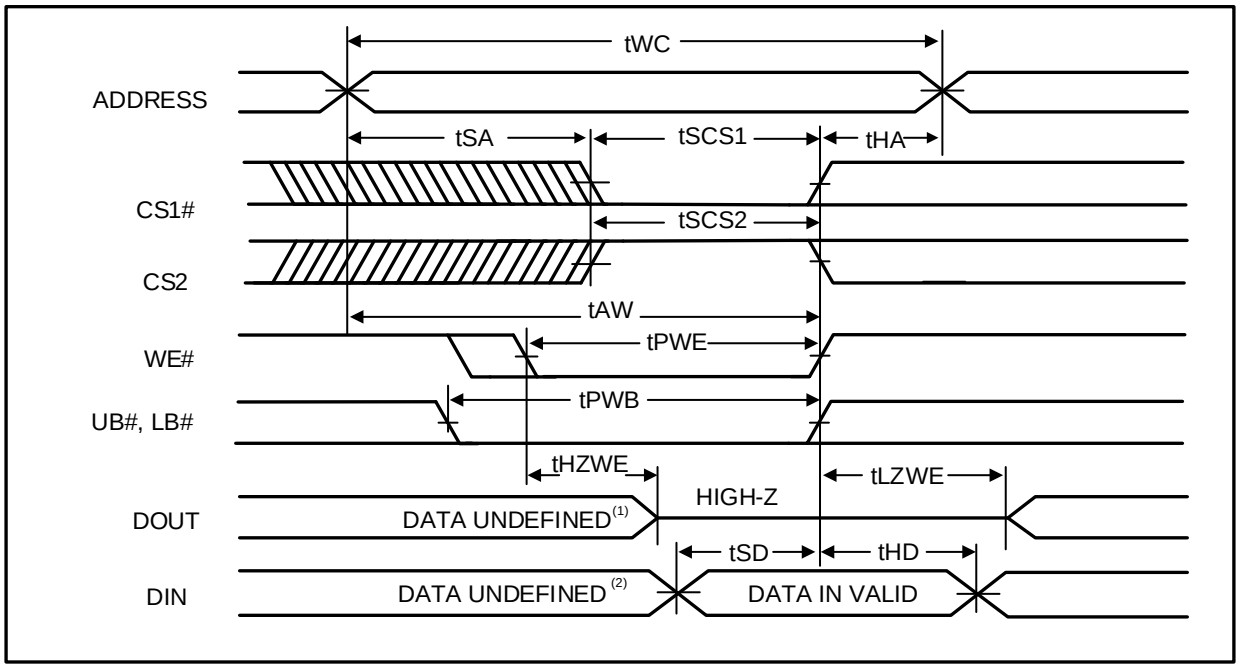
Notes:
1. The device is continuously selected.

READ CYCLE NO. 2[1] (OE# CONTROLLED)



Notes:
1. Address is valid prior to or coincident with CS1# LOW and CS2 HIGH transition.

WRITE CYCLE 1[1,2] (CS1# , CS2 Controlled, OE# = HIGH or LOW)

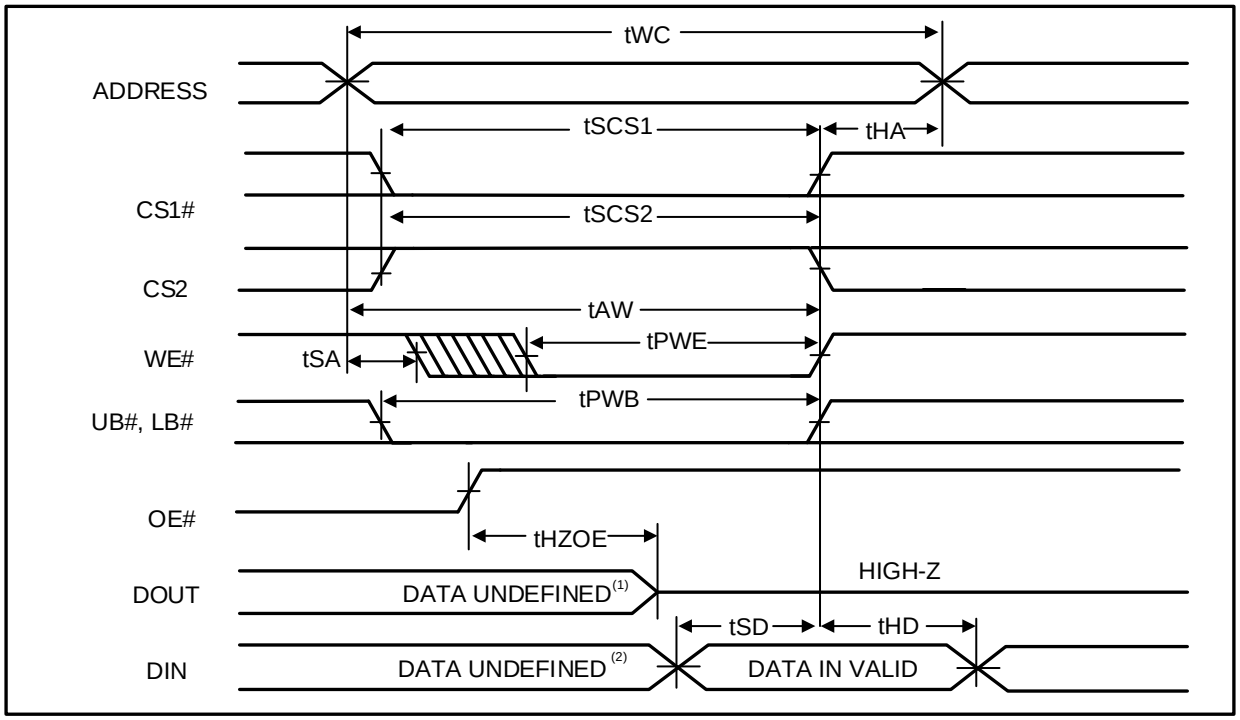


Notes:

1 tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high

2. During this period the I/Os are in output state. Do not apply input signals.

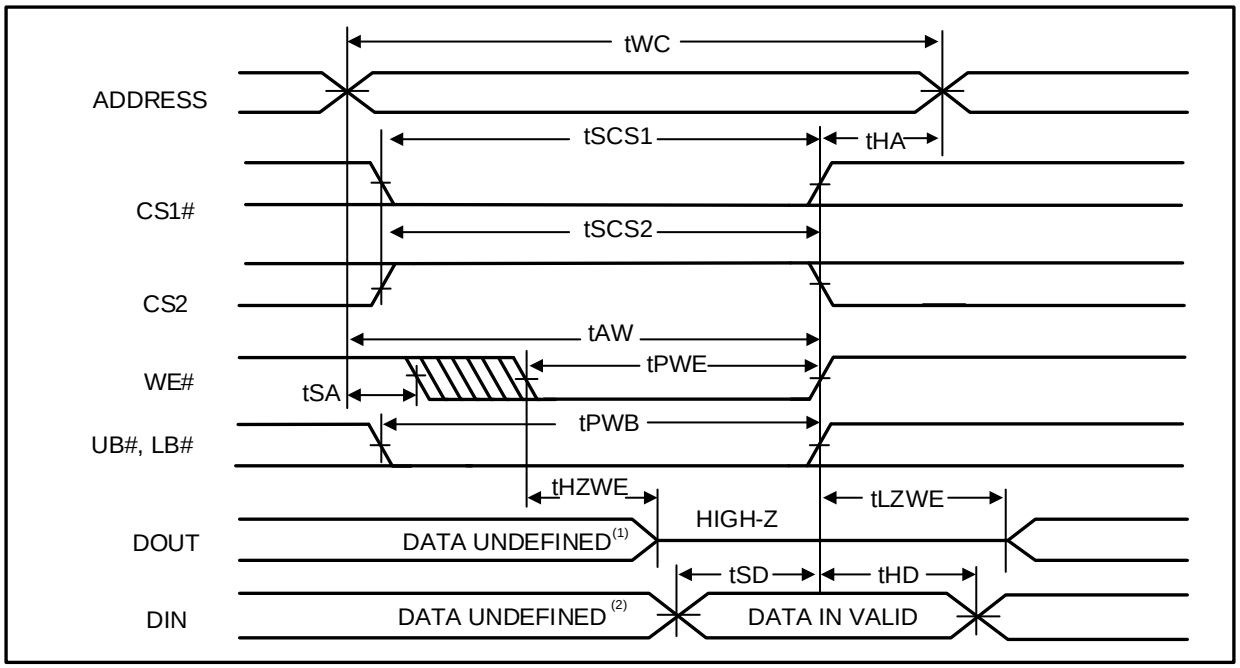
WRITE CYCLE NO. 2[1,2] (WE# Controlled: OE# is HIGH During Write Cycle)



Notes:

1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3[1] (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Notes:

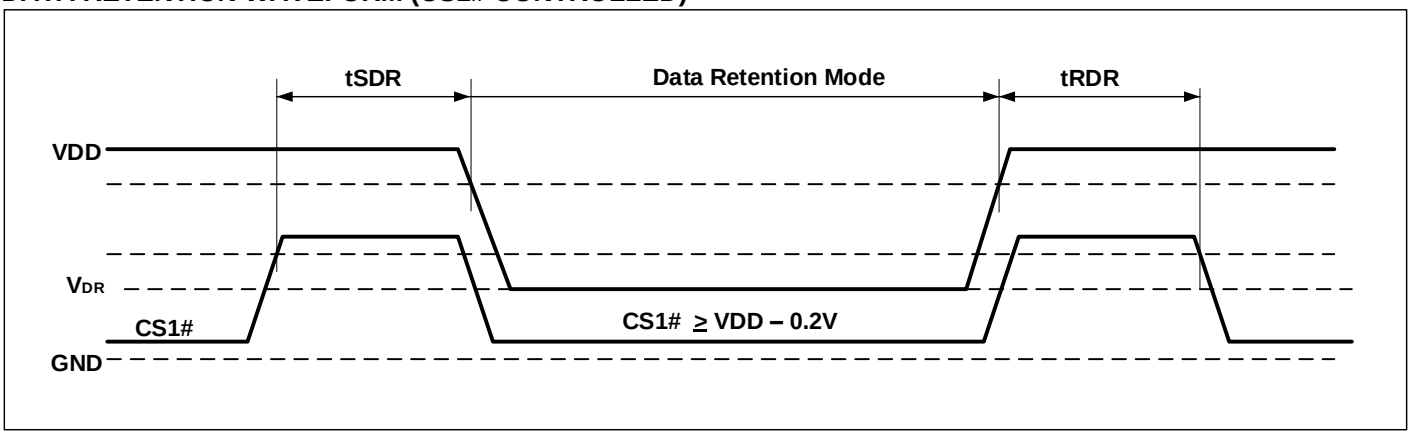
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

DATA RETENTION CHARACTERISTICS

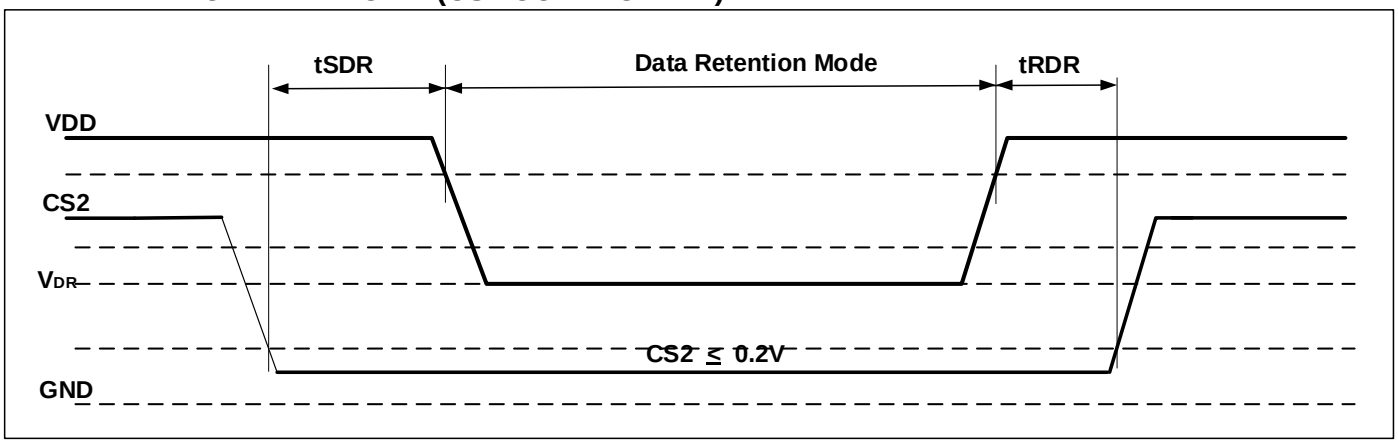
Symbol	Parameter	Test Condition	OPTION	Min.	Typ.(2)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	IS62(5)WV2568EALL	1.5		-	V
			IS62(5)WV2568EBLL	1.5		-	V
I_{DR}	Data Retention Current	V_{DD}= V_{DR}(min), (1) 0V ≤ CS2 ≤ 0.2V, or (2) CS1# ≥ V_{DD} – 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	-	2	5	uA
			Ind.	-	-	12	
			Auto	-	-	25	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Note:
1. If CS1# >VDD–0.2V, all other inputs must meet this condition.
2. Typical values are measured at VDD=3V, TA = 25℃ and not 100% tested.

DATA RETENTION WAVEFORM (CS1# CONTROLLED)



DATA RETENTION WAVEFORM (CS2 CONTROLLED)



ORDERING INFORMATION

IS62WV2568EALL (1.65V - 2.2V)
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV2568EALL-55TI	TSOP (Type I)
55	IS62WV2568EALL-55TLI	TSOP (Type I), Lead-free
55	IS62WV2568EALL-55BI	mini BGA (6mm x 8mm)
55	IS62WV2568EALL-55BLI	mini BGA (6mm x 8mm), Lead-free
55	IS62WV2568EALL-55HI	sTSOP (Type I)
55	IS62WV2568EALL-55HLI	sTSOP (Type I), Lead-free

IS62WV2568EBLL (2.2V - 3.6V)

Industrial Range: –40°C to +85°C

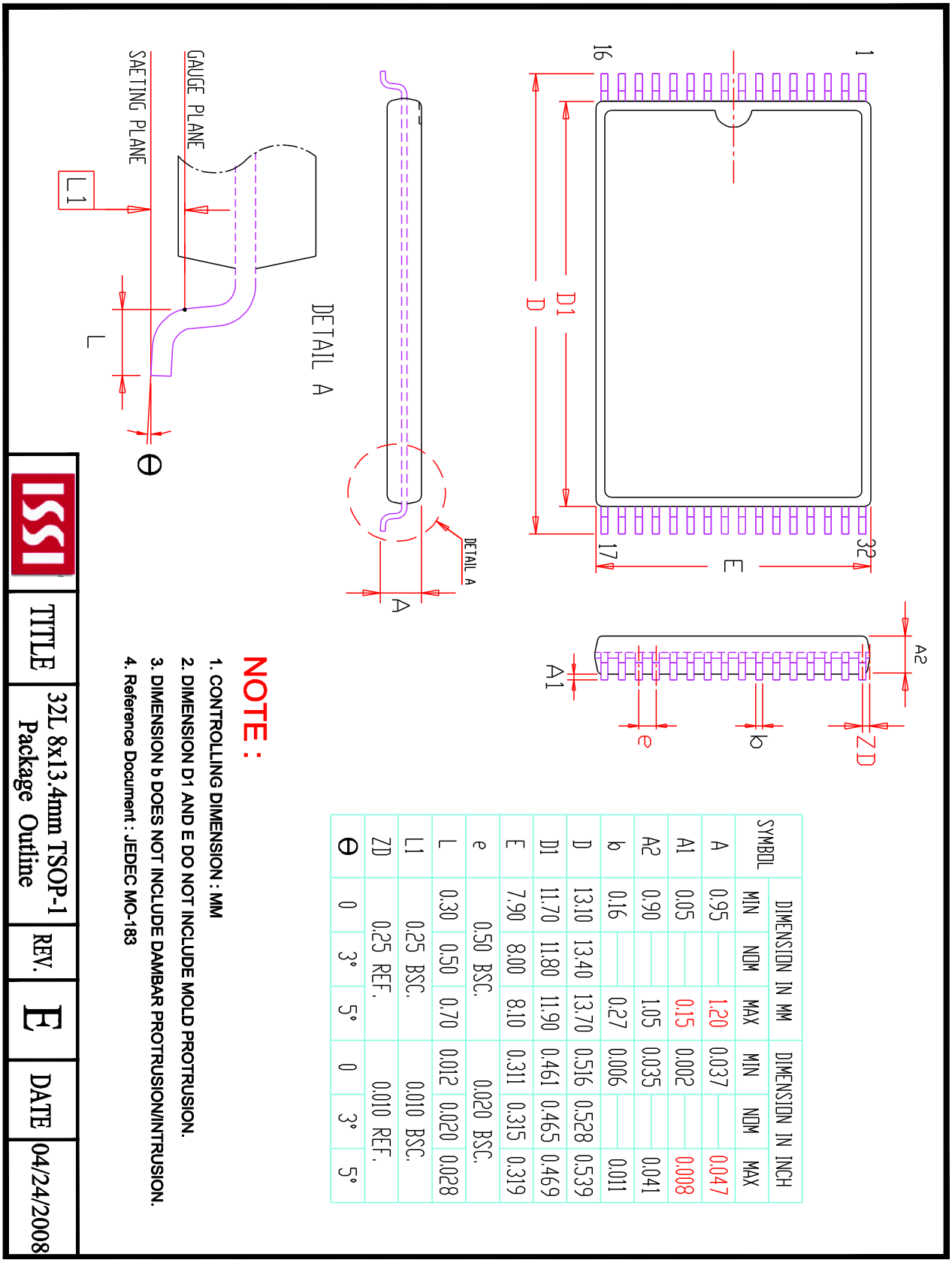
Speed (ns)	Order Part No.	Package
45	IS62WV2568EBLL-45TI	TSOP (Type I)
45	IS62WV2568EBLL-45TLI	TSOP (Type I), Lead-free
45	IS62WV2568EBLL-45BI	mini BGA (6mm x 8mm)
45	IS62WV2568EBLL-45BLI	mini BGA (6mm x 8mm), Lead-free
45	IS62WV2568EBLL-45HI	sTSOP (Type I)
45	IS62WV2568EBLL-45HLI	sTSOP (Type I), Lead-free

IS65WV2568EBLL (2.2V - 3.6V)

Automotive Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
55	IS65WV2568EBLL-55CTLA3	TSOP (Type II), Lead-free
	IS65WV2568EBLL-55HLA3	sTSOP (Type I), Lead-free

PACKAGE INFORMATION

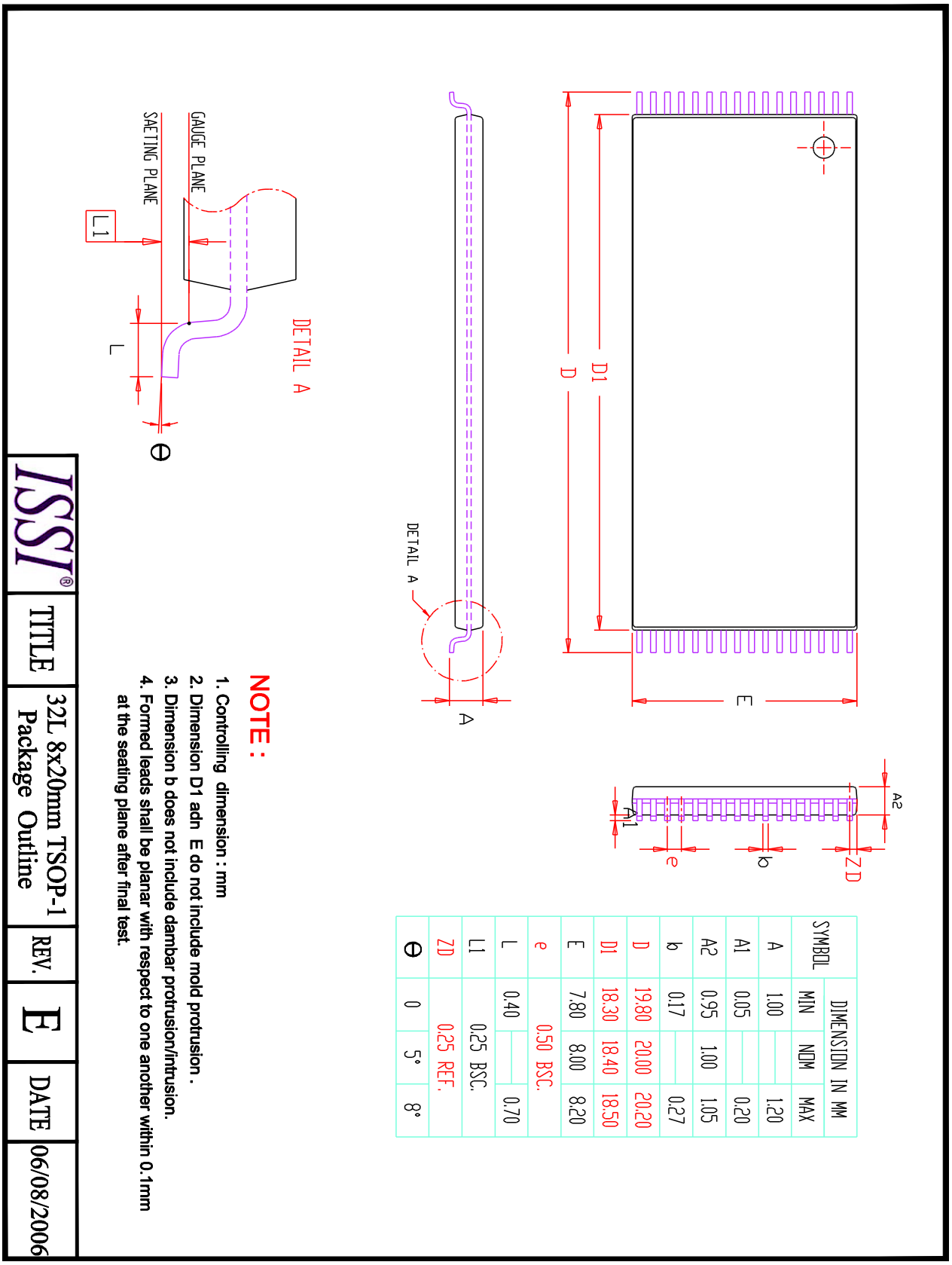


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.20	0.037		0.047
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e		0.50 BSC.			0.020 BSC.	
L	0.30	0.50	0.70	0.012	0.020	0.028
L1		0.25 BSC.			0.010 BSC.	
ZD		0.25 REF.			0.010 REF.	
θ	0	3°	5°	0	3°	5°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

	TITLE		REV.		DATE
ISSI	32L 8x13.4mm TSOP-1 Package Outline		E		04/24/2008

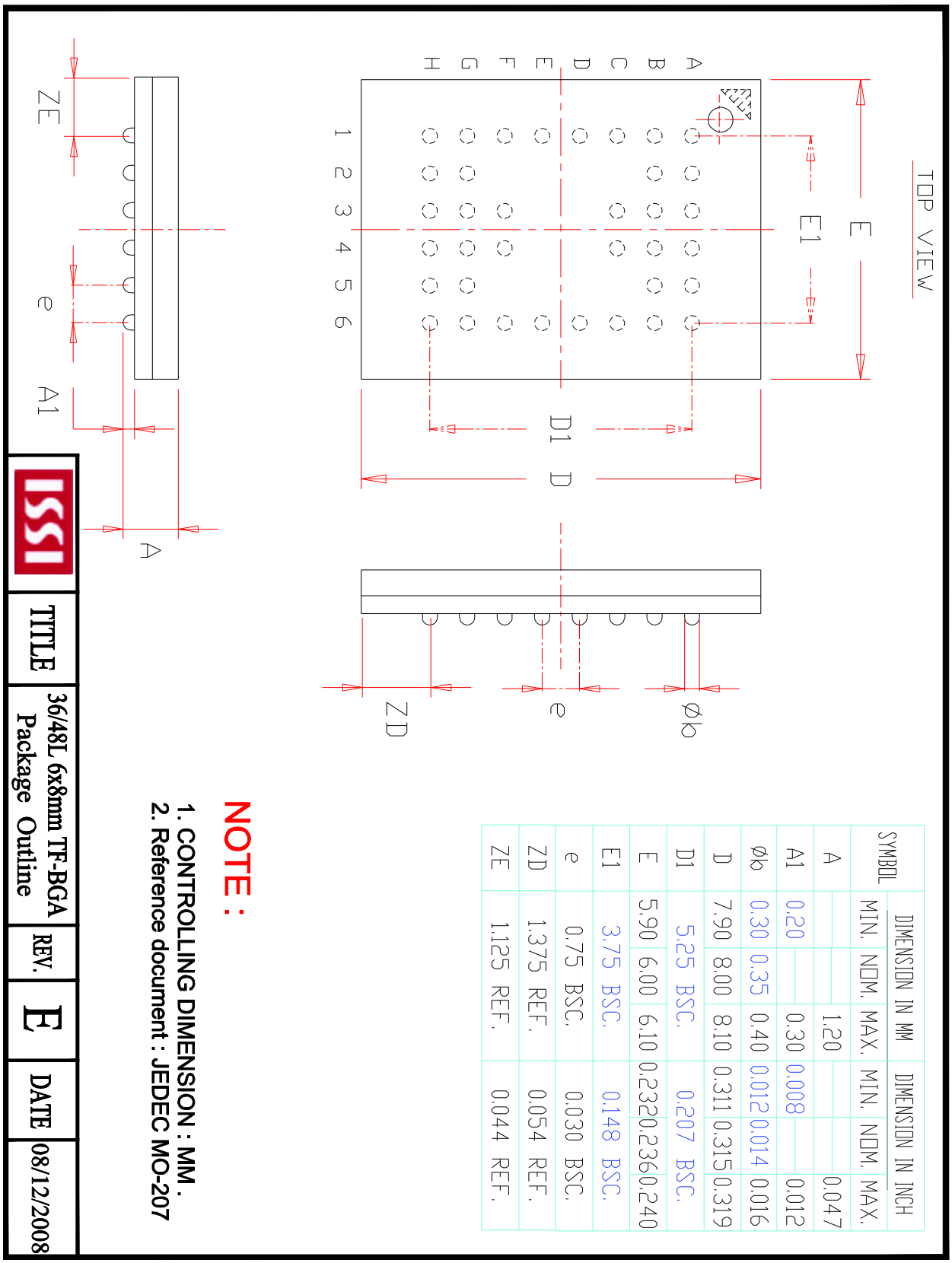


SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A	1.00		1.20
A1	0.05		0.20
A2	0.95	1.00	1.05
b	0.17		0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.80	8.00	8.20
e		0.50 BSC.	
L	0.40		0.70
L1		0.25 BSC.	
ZD		0.25 REF.	
θ	0	5°	8°

NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

ISSI®	TITLE	32L 8x20mm TSOP-1 Package Outline	REV.	E	DATE	06/08/2006



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1		5.25 BSC.			0.207 BSC.	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1		3.75 BSC.			0.148 BSC.	
e		0.75 BSC.			0.030 BSC.	
ZD		1.375 REF.			0.054 REF.	
ZE		1.125 REF.			0.044 REF.	

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

TITLE	36/48L 6x8mm TF-BGA Package Outline	REV.	E	DATE 08/12/2008