

256Kx8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

JULY 2015

KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
 - 36 mW (typical) operating
 - 9 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
 - 1.65V-2.2V V_{DD} (IS62/65WV2568EALL)
 - 2.2V-3.6V V_{DD} (IS62/65WV2568EBLL)
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

DESCRIPTION

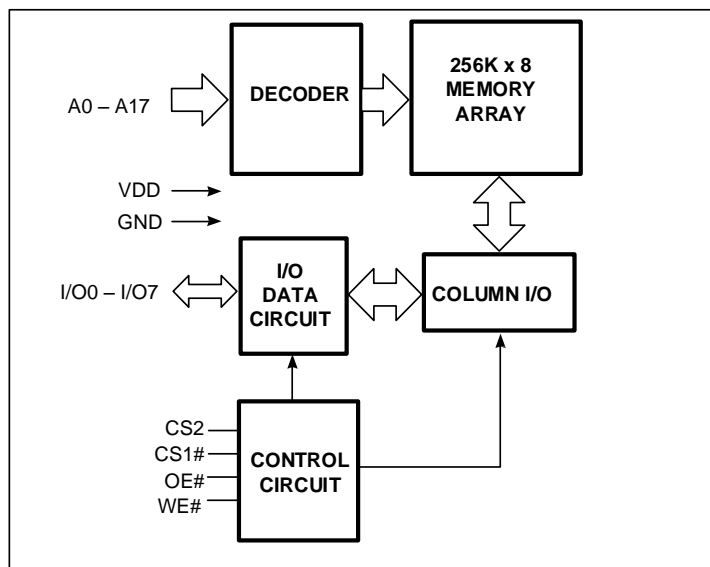
The *ISSI* IS62/65WV2568EALL/EBLL are high-speed, 2M bit static RAMs organized as 256K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS1# is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory.

The IS62/65WV2568EALL/EBLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), sTSOP (TYPE I), and 36-pin mini BGA..

FUNCTIONAL BLOCK DIAGRAM



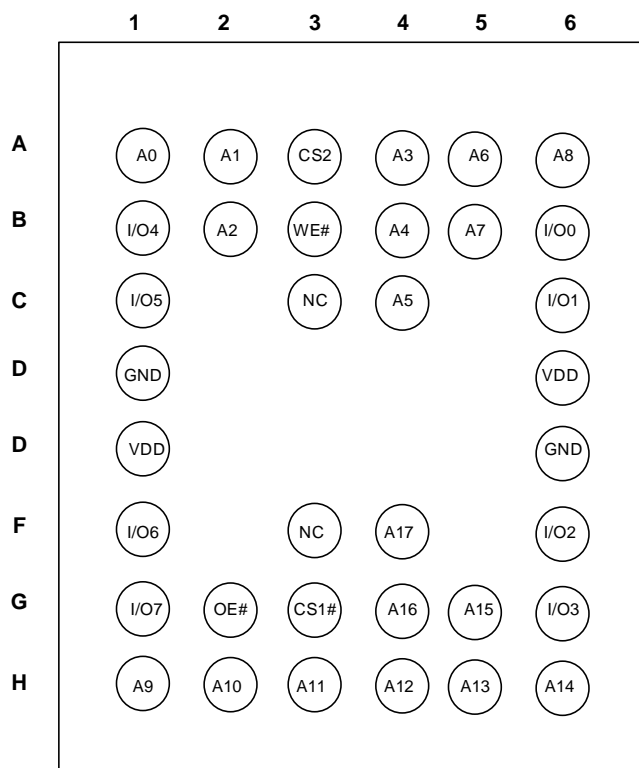
Copyright © 2015 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

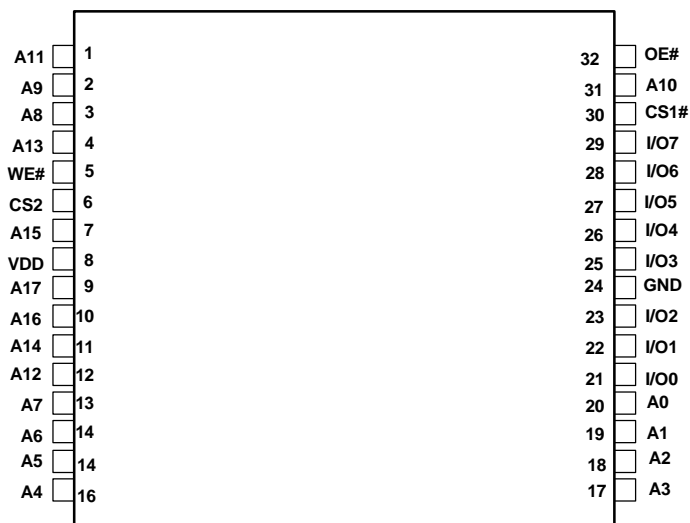
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATIONS

48-Pin mini BGA (6mm x 8mm)



32-Pin TSOP (Type I), STSOP (Type I)



PIN DESCRIPTIONS

| | |
|-----------|---------------------|
| A0-A17 | Address Inputs |
| I/O0-I/O7 | Data Inputs/Outputs |
| CS1#, CS2 | Chip Enable Input |
| OE# | Output Enable Input |
| WE# | Write Enable Input |
| NC | No Connection |
| VDD | Power |
| GND | Ground |

FUNCTION DESCRIPTION

SRAM is one of random access memories. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS1# HIGH or CS2 LOW). The input and output pins (I/O0-7) are placed in a high impedance state. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input LOW. The input and output pins(I/O0-7) are in data input mode. Output buffers are closed during this time even if OE# is LOW.

READ MODE

Read operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

| Mode | CS1# | CS2 | WE# | OE# | I/O0-I/O7 | VDD Current |
|-----------------|------|-----|-----|-----|-----------|-------------|
| Not Selected | H | X | X | X | High-Z | ISB1,ISB2 |
| | X | L | X | X | High-Z | |
| Output Disabled | L | H | H | H | High-Z | ICC |
| Write | L | H | H | L | DIN | ICC |
| Read | L | H | L | X | DOUT | ICC |

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|---------------------------------|--------------------------------------|-------------------------------------|------|
| V _{term} | Terminal Voltage with Respect to GND | -0.2 to +3.9(V _{DD} +0.3V) | V |
| t _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| V _{DD} | V _{DD} Related to GND | -0.2 to +3.9(V _{DD} +0.3V) | V |
| t _{Stg} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} ⁽²⁾ | DC Output Current (LOW) | 20 | mA |

Notes:

- Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- This condition is not per pin. Total current of all pins must meet this value.

OPERATING RANGE⁽¹⁾

| Range | Device Marking | Ambient Temperature | V _{DD} |
|------------|----------------|---------------------|-----------------|
| Commercial | IS62WV2568EALL | 0°C to +70°C | 1.65V-2.2V |
| Industrial | IS62WV2568EALL | -40°C to +85°C | 1.65V-2.2V |
| Automotive | IS65WV2568EALL | -40°C to +125°C | 1.65V-2.2V |
| Commercial | IS62WV2568EBLL | 0°C to +70°C | 2.2V-3.6V |
| Industrial | IS62WV2568EBLL | -40°C to +85°C | 2.2V-3.6V |
| Automotive | IS65WV2568EBLL | -40°C to +125°C | 2.2V-3.6V |

Note:

- Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.

PIN CAPACITANCE⁽¹⁾

| Parameter | Symbol | Test Condition | Max | Units |
|--------------------------|------------------|---|-----|-------|
| Input capacitance | C _{IN} | T _A = 25°C, f = 1 MHz, V _{DD} = V _{DD} (typ) | 10 | pF |
| DQ capacitance (IO0–IO7) | C _{I/O} | | 10 | pF |

Note:

- These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS⁽¹⁾

| Parameter | Symbol | Rating | Units |
|--|------------------|--------|-------|
| Thermal resistance from junction to ambient (airflow = 1m/s) | R _{θJA} | TBD | °C/W |
| Thermal resistance from junction to pins | R _{θJB} | TBD | °C/W |
| Thermal resistance from junction to case | R _{θJC} | TBD | °C/W |

Note:

- These parameters are guaranteed by design and tested by a sample basis only.

ELECTRICAL CHARACTERISTICS

IS62(5)WV2568EALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------------|---------------------|---|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $I_{OH} = -0.1 \text{ mA}$ | 1.4 | — | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 0.1 \text{ mA}$ | — | 0.2 | V |
| $V_{IH}^{(1)}$ | Input HIGH Voltage | | 1.4 | $V_{DD} + 0.2$ | V |
| $V_{IL}^{(1)}$ | Input LOW Voltage | | -0.2 | 0.4 | V |
| I_{LI} | Input Leakage | $GND < V_{IN} < V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND < V_{IN} < V_{DD}$, Output Disabled | -1 | 1 | μA |

Notes:

1. $V_{ILL}(\text{min}) = -1.0\text{V AC}$ (pulse width < 10ns). Not 100% tested.
 $V_{IHH}(\text{max}) = V_{DD} + 1.0\text{V AC}$ (pulse width < 10ns). Not 100% tested.

IS62(5)WV2568EBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------------|---------------------|---|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $2.2 \leq V_{DD} < 2.7$, $I_{OH} = -0.1 \text{ mA}$ | 2.0 | — | V |
| | | $2.7 \leq V_{DD} \leq 3.6$, $I_{OH} = -1.0 \text{ mA}$ | 2.4 | — | V |
| V_{OL} | Output LOW Voltage | $2.2 \leq V_{DD} < 2.7$, $I_{OL} = 0.1 \text{ mA}$ | — | 0.4 | V |
| | | $2.7 \leq V_{DD} \leq 3.6$, $I_{OL} = 2.1 \text{ mA}$ | — | 0.4 | V |
| $V_{IH}^{(1)}$ | Input HIGH Voltage | $2.2 \leq V_{DD} < 2.7$ | 1.8 | $V_{DD} + 0.3$ | V |
| | | $2.7 \leq V_{DD} \leq 3.6$ | 2.2 | $V_{DD} + 0.3$ | V |
| $V_{IL}^{(1)}$ | Input LOW Voltage | $2.2 \leq V_{DD} < 2.7$ | -0.3 | 0.6 | V |
| | | $2.7 \leq V_{DD} \leq 3.6$ | -0.3 | 0.8 | V |
| I_{LI} | Input Leakage | $GND < V_{IN} < V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND < V_{IN} < V_{DD}$, Output Disabled | -1 | 1 | μA |

Notes:

2. $V_{ILL}(\text{min}) = -2.0\text{V AC}$ (pulse width < 10ns). Not 100% tested.
 $V_{IHH}(\text{max}) = V_{DD} + 2.0\text{V AC}$ (pulse width < 10ns). Not 100% tested.

**IS62(5)WV2568EALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER
(OVER THE OPERATING RANGE)**

| Symbol | Parameter | Test Conditions | Grade | Typ. | Max. | Unit |
|--------|--|---|-------|------|------|------|
| ICC | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max, f = f _{MAX} , CS1# = V _{IL} , CS2 = V _{IH} I _{OUT} = 0 mA | Com. | 12 | 15 | mA |
| | | | Ind. | - | 18 | |
| | | | Auto. | - | 25 | |
| ICC1 | V _{DD} Static Operating Supply Current | V _{DD} = Max, f = 0, CS1# = V _{IL} , CS2 = V _{IH} I _{OUT} = 0 mA | Com. | 1 | 3 | mA |
| | | | Ind. | - | 3 | |
| | | | Auto. | - | 4 | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max, f = 0 CS1# ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V VIN ≤ 0.2V or VIN ≥ V _{DD} - 0.2V | Com. | 2 | 5 | μA |
| | | | Ind. | - | 12 | μA |
| | | | Auto. | - | 25 | μA |

Note:

Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25°C

**IS62(5)WV2568EBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER
(OVER THE OPERATING RANGE)**

| Symbol | Parameter | Test Conditions | Grade | Typ. | Max. | Unit |
|--------|--|---|-------|------|------|------|
| ICC | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max, f = f _{MAX} , CS1# = V _{IL} , CS2 = V _{IH} I _{OUT} = 0 mA | Com. | 12 | 15 | mA |
| | | | Ind. | - | 18 | |
| | | | Auto. | - | 25 | |
| ICC1 | V _{DD} Static Operating Supply Current | V _{DD} = Max, f = 0, CS1# = V _{IL} , CS2 = V _{IH} I _{OUT} = 0 mA | Com. | 1 | 3 | mA |
| | | | Ind. | - | 3 | |
| | | | Auto. | - | 4 | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max, f = 0 CS1# ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V VIN ≤ 0.2V or VIN ≥ V _{DD} - 0.2V | Com. | 2 | 5 | μA |
| | | | Ind. | - | 12 | μA |
| | | | Auto. | - | 25 | μA |

Note:

Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25°C

AC CHARACTERISTICS⁽⁶⁾ (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|----------------------------|--------------------------|------|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Read Cycle Time | t _{RC} | 45 | - | 55 | - | ns | 1,5 |
| Address Access Time | t _{AA} | - | 45 | - | 55 | ns | 1 |
| Output Hold Time | t _{OHA} | 8 | - | 8 | - | ns | 1 |
| CS1#, CS2 Access Time | t _{ACS1/ACS2} | - | 45 | - | 55 | ns | 1 |
| OE# Access Time | t _{DOE} | - | 22 | - | 25 | ns | 1 |
| OE# to High-Z Output | t _{HZOE} | - | 18 | - | 18 | ns | 2 |
| OE# to Low-Z Output | t _{LZOE} | 5 | - | 5 | - | ns | 2 |
| CS1#, CS2 to High-Z Output | t _{HZCS1/HZCS2} | - | 18 | - | 18 | ns | 2 |
| CS1#, CS2 to Low-Z Output | t _{LZCS/LZCS2} | 10 | - | 10 | - | ns | 2 |

WRITE CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|---------------------------------|-------------------------|------|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Write Cycle Time | t _{WC} | 45 | - | 55 | - | ns | 1,3,5 |
| CS1#, CS2 to Write End | t _{SCS1/tSCS2} | 35 | - | 40 | - | ns | 1,3 |
| Address Setup Time to Write End | t _{AW} | 35 | - | 40 | - | ns | 1,3 |
| Address Hold from Write End | t _{HA} | 0 | - | 0 | - | ns | 1,3 |
| Address Setup Time | t _{SA} | 0 | - | 0 | - | ns | 1,3 |
| WE# Pulse Width | t _{PWE} | 35 | - | 40 | - | ns | 1,3,4 |
| Data Setup to Write End | t _{SD} | 28 | - | 28 | - | ns | 1,3 |
| Data Hold from Write End | t _{HD} | 0 | - | 0 | - | ns | 1,3 |
| WE# LOW to High-Z Output | t _{HZWE} | - | 18 | - | 18 | ns | 2,3 |
| WE# HIGH to Low-Z Output | t _{LZWE} | 10 | - | 10 | - | ns | 2,3 |

Notes:

1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. t_{HZOE}, t_{HZCS}, t_{HZB}, and t_{HZWE} transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of CS1# = LOW, CS2=HIGH, and WE# = LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. t_{PWE} > t_{HZWE} + t_{SD} when OE# is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

| Parameter | Symbol | Conditions | Units |
|-------------------------------|-------------------------|----------------------|-------|
| Input Rise Time | T_R | 1.0 | V/ns |
| Input Fall Time | T_F | 1.0 | V/ns |
| Output Timing Reference Level | V_{REF} | $\frac{1}{2} V_{TM}$ | V |
| Output Load Conditions | Refer to Figure 1 and 2 | | |

OUTPUT LOAD CONDITIONS FIGURES

Figure1

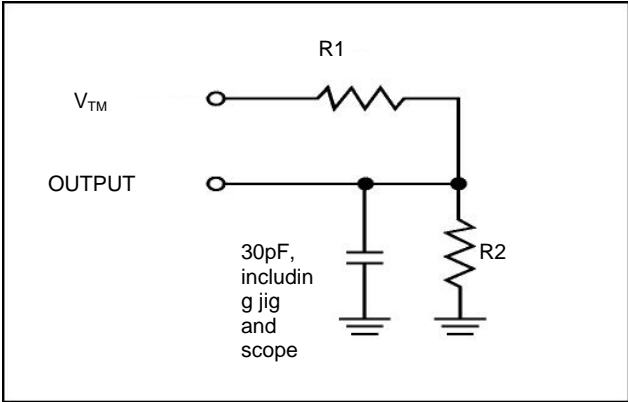
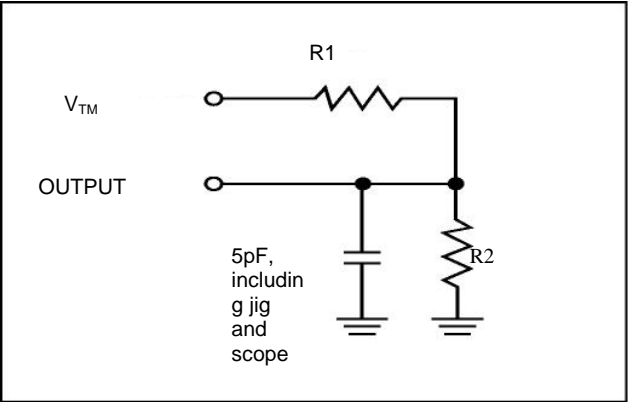


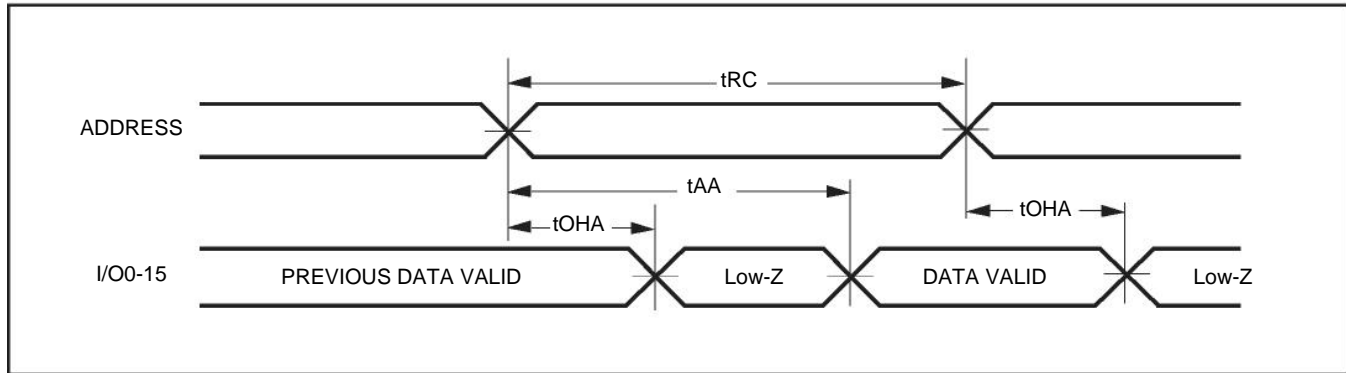
Figure2



| Parameters | $V_{DD}=1.65\sim1.98V$ | $V_{DD}=2.2\sim2.7V$ | $V_{DD}=2.7\sim3.6V$ |
|------------|------------------------|----------------------|----------------------|
| R1 | 13500 Ω | 16667 Ω | 1103 Ω |
| R2 | 10800 Ω | 15385 Ω | 1554 Ω |
| V_{TM} | VDD | VDD | VDD |

TIMING DIAGRAM

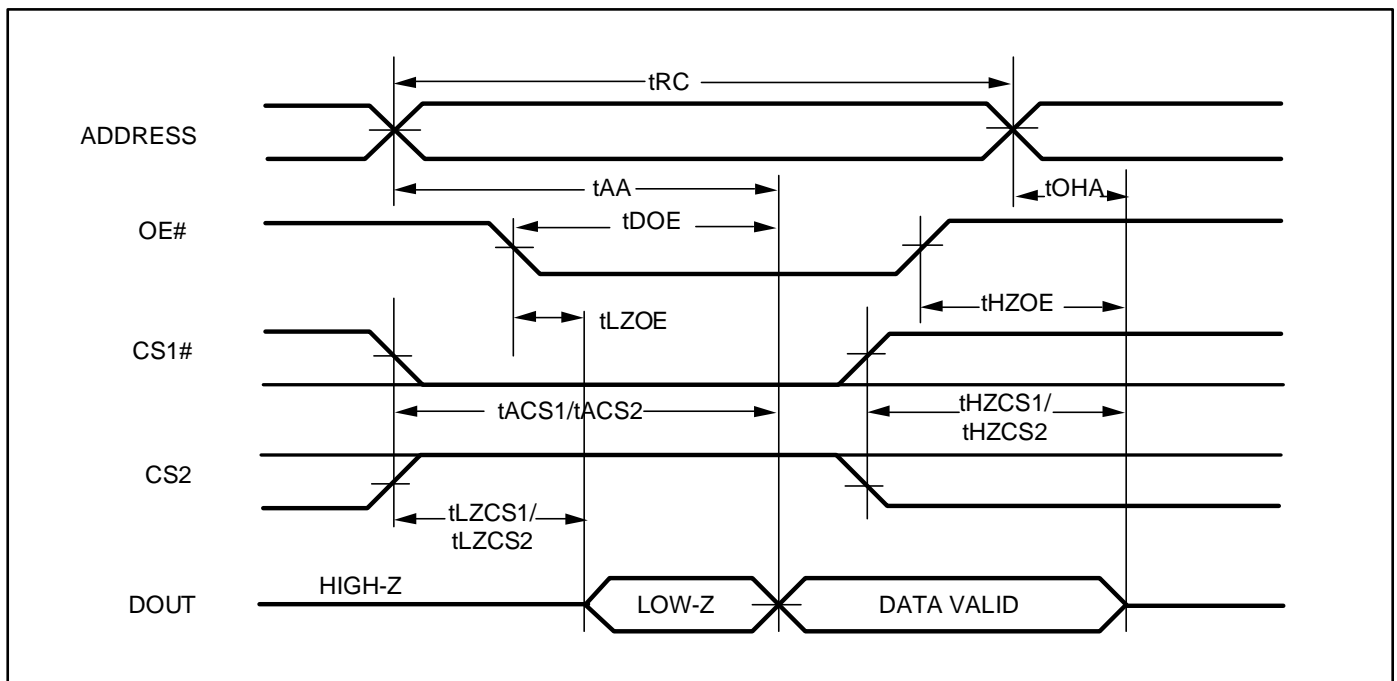
READ CYCLE NO. 1⁽¹⁾ (ADDRESS CONTROLLED) (CS1# = OE# = LOW, CS2 = WE# = HIGH)



Notes:

1. The device is continuously selected.

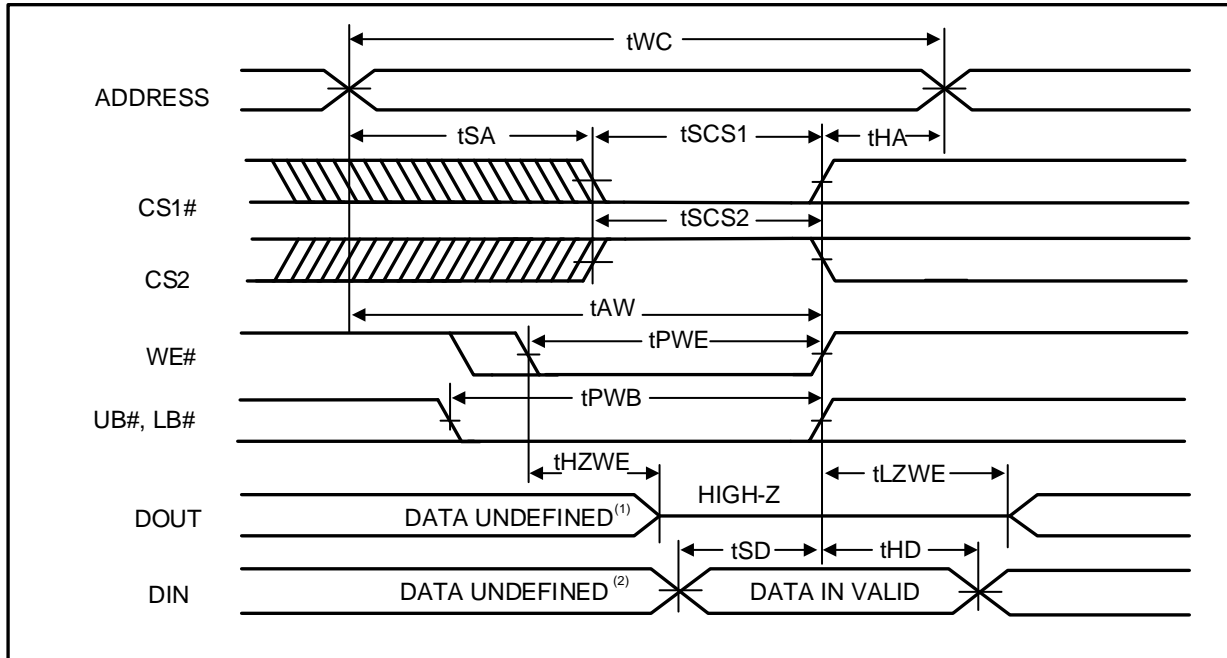
READ CYCLE NO. 2⁽¹⁾ (OE# CONTROLLED)



Notes:

1. Address is valid prior to or coincident with CS1# LOW and CS2 HIGH transition.

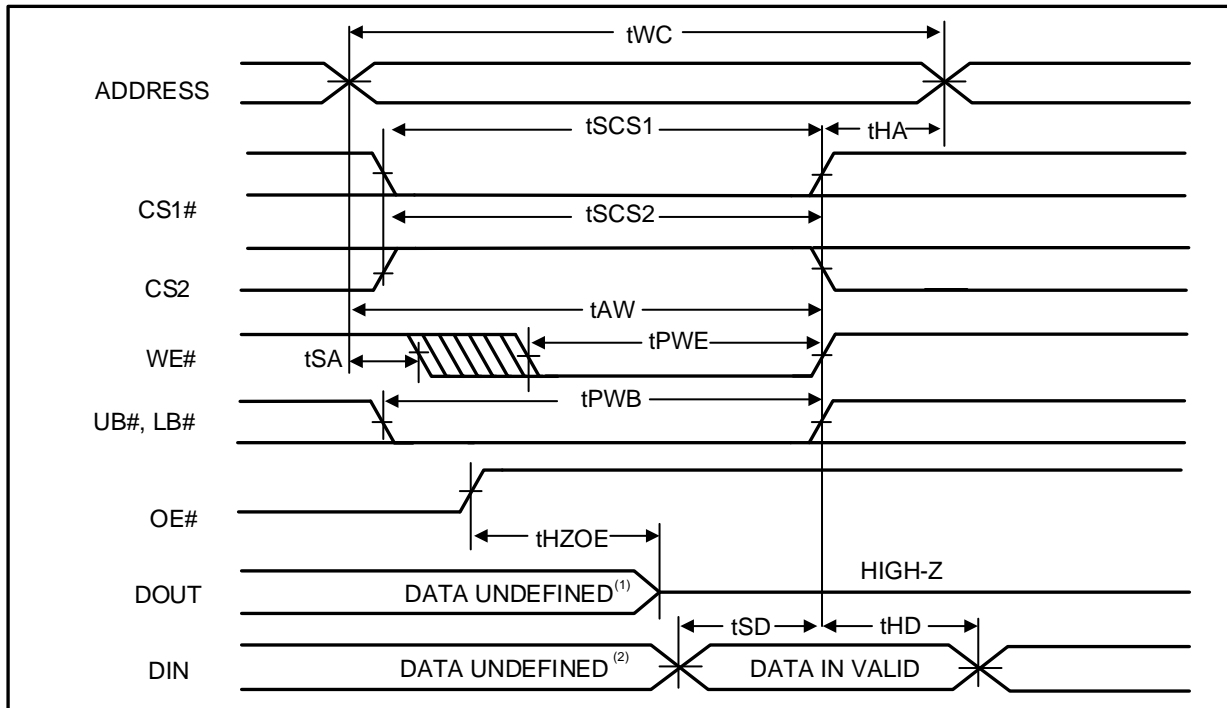
WRITE CYCLE 1^(1,2) (CS1# , CS2 Controlled, OE# = HIGH or LOW)



Notes:

1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high
2. During this period the I/Os are in output state. Do not apply input signals.

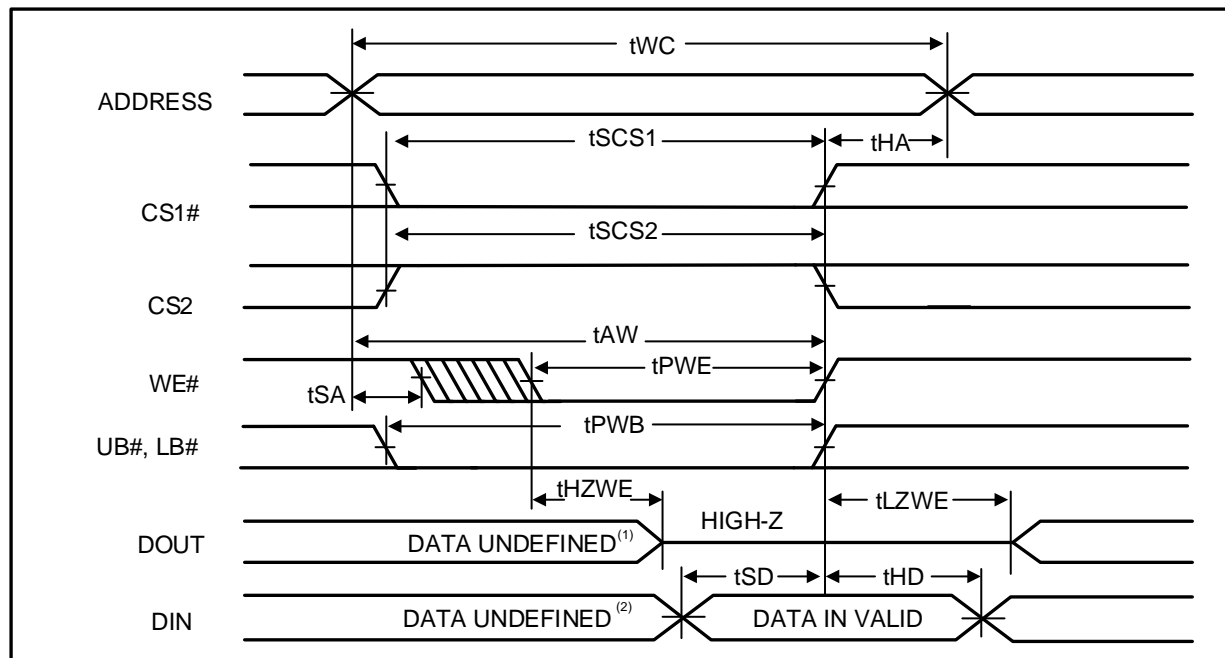
WRITE CYCLE NO. 2^(1,2) (WE# Controlled: OE# is HIGH During Write Cycle)



Notes:

1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3⁽¹⁾ (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Notes:

1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

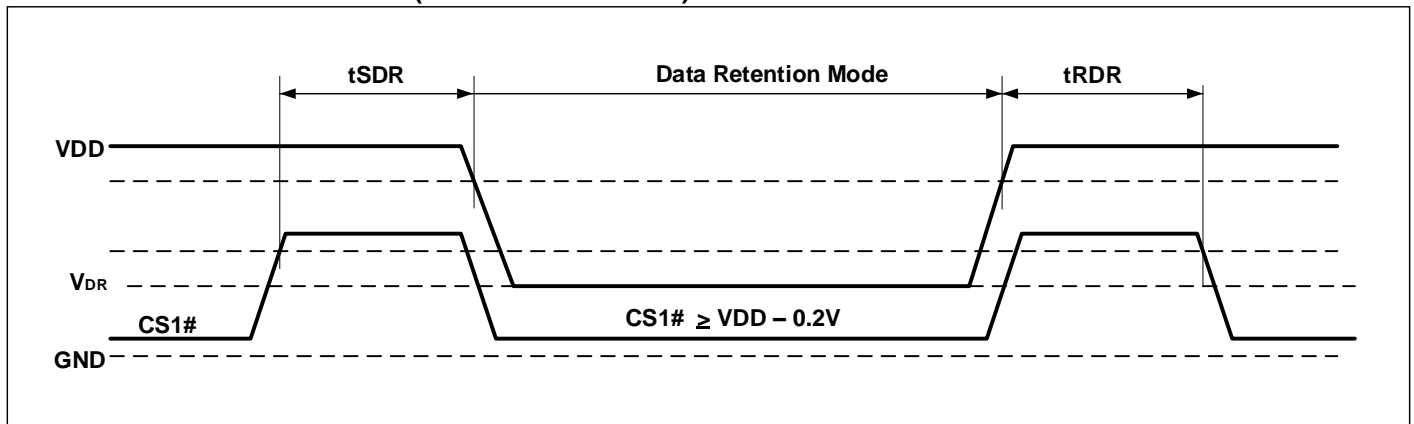
DATA RETENTION CHARACTERISTICS

| Symbol | Parameter | Test Condition | OPTION | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|-----------------------------|---|-------------------|----------|---------------------|------|---------|
| V_{DR} | V_{DD} for Data Retention | See Data Retention Waveform | IS62(5)WV2568EALL | 1.5 | | - | V |
| | | | IS62(5)WV2568EBLL | 1.5 | | - | V |
| I_{DR} | Data Retention Current | $V_{DD} = V_{DR}(\text{min})$, (1) $0V \leq CS2 \leq 0.2V$, or (2) $CS1\# \geq V_{DD} - 0.2V$, $CS2 \geq V_{DD} - 0.2V$ | Com. | - | 2 | 5 | μA |
| | | | Ind. | - | - | 12 | |
| | | | Auto | - | - | 25 | |
| t_{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | - | - | ns |
| t_{RDR} | Recovery Time | See Data Retention Waveform | | t_{RC} | - | - | ns |

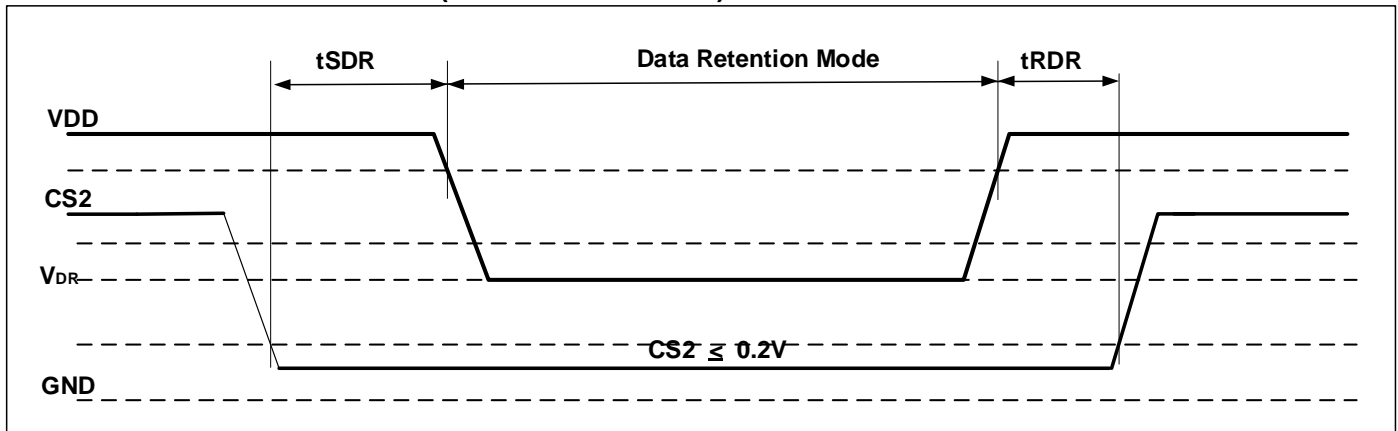
Note:

1. If $CS1\# > V_{DD} - 0.2V$, all other inputs must meet this condition.
2. Typical values are measured at $V_{DD} = 3V$, $T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION WAVEFORM (CS1# CONTROLLED)



DATA RETENTION WAVEFORM (CS2 CONTROLLED)



ORDERING INFORMATION

IS62WV2568EALL (1.65V - 2.2V)
Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|----------------------|---------------------------------|
| 55 | IS62WV2568EALL-55TI | TSOP (Type I) |
| 55 | IS62WV2568EALL-55TLI | TSOP (Type I), Lead-free |
| 55 | IS62WV2568EALL-55BI | mini BGA (6mm x 8mm) |
| 55 | IS62WV2568EALL-55BLI | mini BGA (6mm x 8mm), Lead-free |
| 55 | IS62WV2568EALL-55HI | sTSOP (Type I) |
| 55 | IS62WV2568EALL-55HLI | sTSOP (Type I), Lead-free |

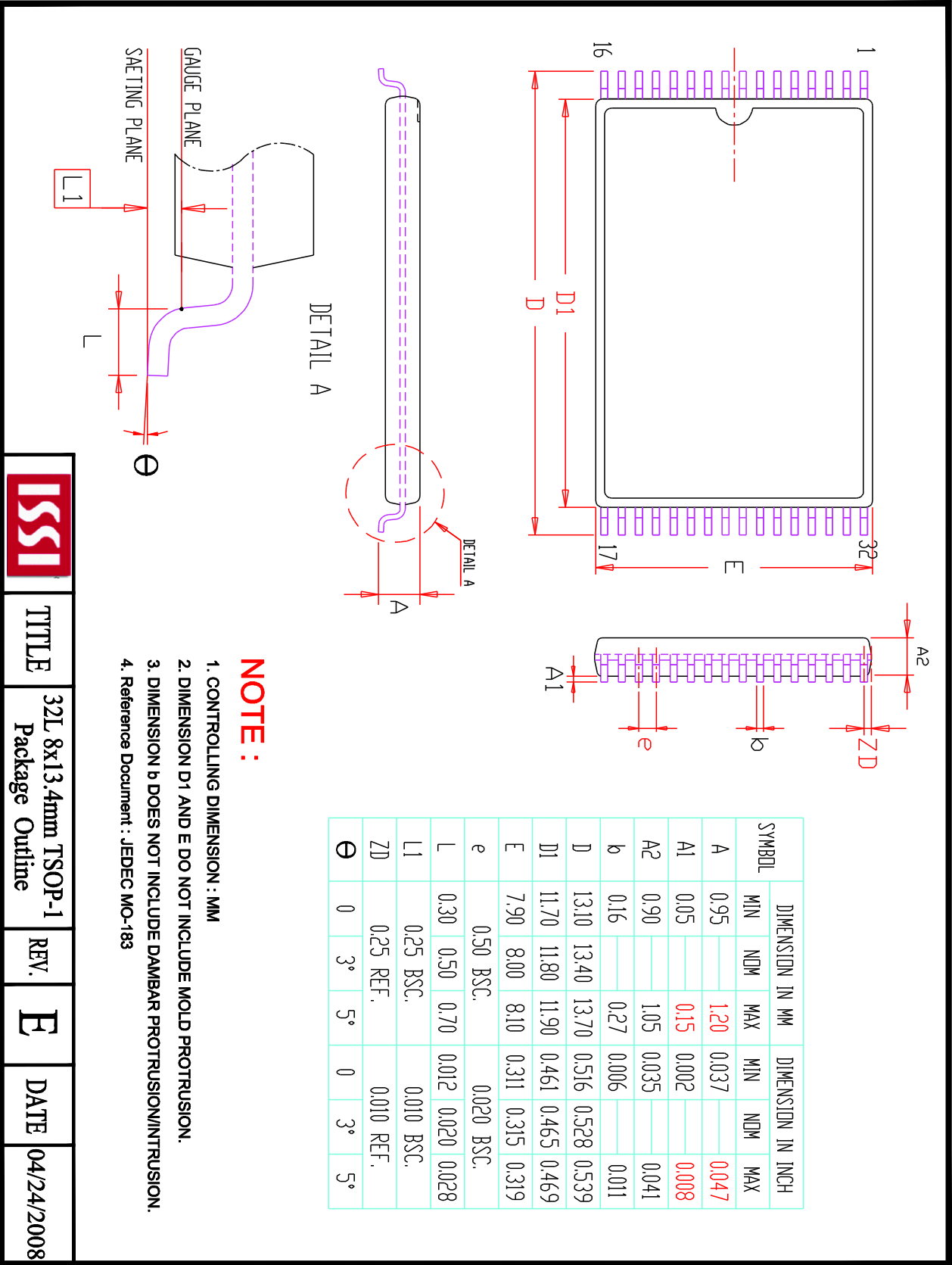
IS62WV2568EBLL (2.2V - 3.6V)
Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|----------------------|---------------------------------|
| 45 | IS62WV2568EBLL-45TI | TSOP (Type I) |
| 45 | IS62WV2568EBLL-45TLI | TSOP (Type I), Lead-free |
| 45 | IS62WV2568EBLL-45BI | mini BGA (6mm x 8mm) |
| 45 | IS62WV2568EBLL-45BLI | mini BGA (6mm x 8mm), Lead-free |
| 45 | IS62WV2568EBLL-45HI | sTSOP (Type I) |
| 45 | IS62WV2568EBLL-45HLI | sTSOP (Type I), Lead-free |

IS65WV2568EBLL (2.2V - 3.6V)
Automotive Range (A3): -40°C to +125°C

| Speed (ns) | Order Part No. | Package |
|------------|------------------------|---------------------------|
| 55 | IS65WV2568EBLL-55CTLA3 | TSOP (Type II), Lead-free |
| | IS65WV2568EBLL-55HLA3 | sTSOP (Type I), Lead-free |

IS62/65WV2568EALL
IS62/65WV2568EBLL
PACKAGE INFORMATION



TITLE

32L 8x13.4mm TSOP-1
Package Outline

REV.

E

DATE

04/24/2008

