

## FEATURES

- 12MHz Gain-Bandwidth
- 400V/ $\mu$ s Slew Rate
- 1.25mA Maximum Supply Current
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 10nV/ $\sqrt{\text{Hz}}$  Input Noise Voltage
- 800 $\mu$ V Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- 70nA Maximum Input Offset Current
- 12V/mV Minimum DC Gain,  $R_L=1\text{k}$
- 230ns Settling Time to 0.1%, 10V Step
- 280ns Settling Time to 0.01%, 10V Step
- $\pm 12\text{V}$  Minimum Output Swing into 500 $\Omega$
- $\pm 2.5\text{V}$  Minimum Output Swing into 150 $\Omega$
- Specified at  $\pm 2.5\text{V}$ ,  $\pm 5\text{V}$ , and  $\pm 15\text{V}$

## APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

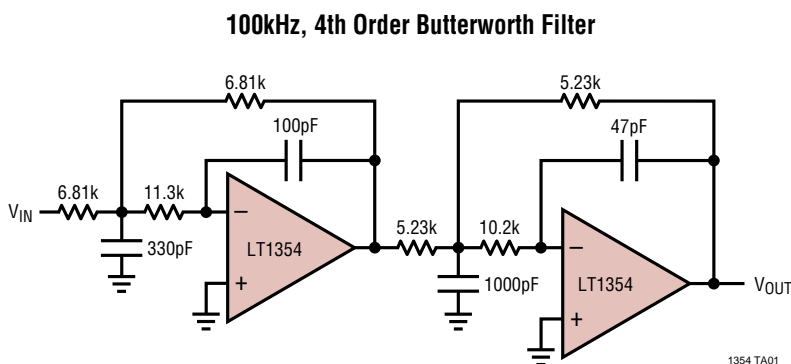
## DESCRIPTION

The LT<sup>®</sup>1354 is a low power, high speed, high slew rate operational amplifier with outstanding AC and DC performance. The LT1354 has much lower supply current, lower input offset voltage, lower input bias current, and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 500 $\Omega$  load to  $\pm 12\text{V}$  with  $\pm 15\text{V}$  supplies and a 150 $\Omega$  load to  $\pm 2.5\text{V}$  on  $\pm 5\text{V}$  supplies. The amplifier is also stable with any capacitive load which makes it useful in buffer or cable driver applications.

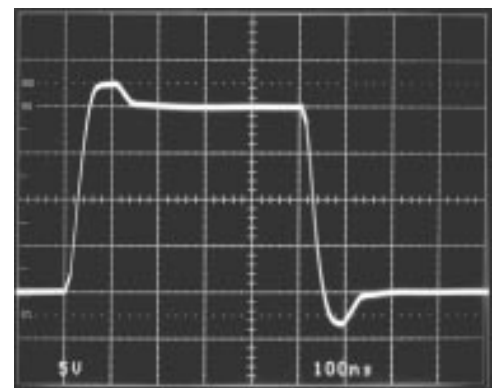
The LT1354 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1354 see the LT1355/LT1356 data sheet. For higher bandwidth devices with higher supply current see the LT1357 through LT1365 data sheets. Singles, duals, and quads of each amplifier are available.

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 C-Load is a trademark of Linear Technology Corporation

## TYPICAL APPLICATION



**$A_V = -1$  Large-Signal Response**



1354 TA02

## ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ( $V^+$ to $V^-$ ) .....	36V	Specified Temperature Range (Note 6) ...	$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$
Differential Input Voltage (Transient Only, Note 1) ...	$\pm 10\text{V}$	Maximum Junction Temperature (See Below)	
Input Voltage .....	$\pm V_S$	Plastic Package .....	$150^{\circ}\text{C}$
Output Short-Circuit Duration (Note 2) .....	Indefinite	Storage Temperature Range .....	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$
Operating Temperature Range .....	$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	Lead Temperature (Soldering, 10 sec) .....	$300^{\circ}\text{C}$

## PACKAGE/ORDER INFORMATION

<p>N8 PACKAGE, 8-LEAD PLASTIC DIP <math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 130^{\circ}\text{C/W}</math></p>	ORDER PART NUMBER	<p>S8 PACKAGE, 8-LEAD PLASTIC SOIC <math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 190^{\circ}\text{C/W}</math></p>	ORDER PART NUMBER
	LT1354CN8		LT1354CS8
			S8 PART MARKING
			1354

Consult factory for Industrial and Military grade parts.

## ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$ , $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	$V_{SUPPLY}$	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage		$\pm 15\text{V}$	0.3	0.8		mV
			$\pm 5\text{V}$	0.3	0.8		mV
			$\pm 2.5\text{V}$	0.4	1.0		mV
$I_{OS}$	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	20	70		nA
$I_B$	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	80	300		nA
$e_n$	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	10			$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input Noise Current	$f = 10\text{kHz}$	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	0.6			$\text{pA}/\sqrt{\text{Hz}}$
$R_{IN}$	Input Resistance	$V_{CM} = \pm 12\text{V}$ Differential	$\pm 15\text{V}$	70	160		$\text{M}\Omega$
			$\pm 15\text{V}$		11		$\text{M}\Omega$
$C_{IN}$	Input Capacitance		$\pm 15\text{V}$	3			pF
	Input Voltage Range $^+$		$\pm 15\text{V}$	12.0	13.4		V
			$\pm 5\text{V}$	2.5	3.5		V
			$\pm 2.5\text{V}$	0.5	1.1		V
	Input Voltage Range $^-$		$\pm 15\text{V}$	-13.2	-12.0		V
			$\pm 5\text{V}$	-3.4	-2.5		V
			$\pm 2.5\text{V}$	-0.9	-0.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	80	97		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	78	84		dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	68	75		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		92	106		dB
$A_{VOL}$	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$ , $R_L = 1\text{k}$	$\pm 15\text{V}$	12	36		V/mV
		$V_{OUT} = \pm 10\text{V}$ , $R_L = 500\Omega$	$\pm 15\text{V}$	5	15		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 1\text{k}$	$\pm 5\text{V}$	12	36		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 500\Omega$	$\pm 5\text{V}$	5	15		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 150\Omega$	$\pm 5\text{V}$	1	4		V/mV
		$V_{OUT} = \pm 1\text{V}$ , $R_L = 500\Omega$	$\pm 2.5\text{V}$	5	20		V/mV

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	$V_{SUPPLY}$	MIN	TYP	MAX	UNITS
$V_{OUT}$	Output Swing	$R_L = 1\text{k}$ , $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	13.3	13.8		$\pm\text{V}$
		$R_L = 500\Omega$ , $V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	12.0	12.5		$\pm\text{V}$
		$R_L = 500\Omega$ , $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	3.5	4.0		$\pm\text{V}$
		$R_L = 150\Omega$ , $V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	2.5	3.1		$\pm\text{V}$
		$R_L = 500\Omega$ , $V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	1.3	1.7		$\pm\text{V}$
$I_{OUT}$	Output Current	$V_{OUT} = \pm 12\text{V}$	$\pm 15\text{V}$	24.0	30		mA
		$V_{OUT} = \pm 2.5\text{V}$	$\pm 5\text{V}$	16.7	25		mA
$I_{SC}$	Short-Circuit Current	$V_{OUT} = 0\text{V}$ , $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	30	42		mA
SR	Slew Rate	$A_V = -2$ , (Note 3)	$\pm 15\text{V}$	200	400		V/ $\mu\text{s}$
			$\pm 5\text{V}$	70	120		V/ $\mu\text{s}$
	Full Power Bandwidth	10V Peak, (Note 4) 3V Peak, (Note 4)	$\pm 15\text{V}$		6.4		MHz
			$\pm 5\text{V}$		6.4		MHz
GBW	Gain-Bandwidth	$f = 200\text{kHz}$ , $R_L = 2\text{k}$	$\pm 15\text{V}$	9.0	12.0		MHz
			$\pm 5\text{V}$	7.5	10.5		MHz
			$\pm 2.5\text{V}$		9.0		MHz
$t_r$ , $t_f$	Rise Time, Fall Time	$A_V = 1$ , 10%-90%, 0.1V	$\pm 15\text{V}$		14		ns
			$\pm 5\text{V}$		17		ns
	Overshoot	$A_V = 1$ , 0.1V	$\pm 15\text{V}$		20		%
			$\pm 5\text{V}$		18		%
	Propagation Delay	50% $V_{IN}$ to 50% $V_{OUT}$ , 0.1V	$\pm 15\text{V}$		16		ns
			$\pm 5\text{V}$		19		ns
$t_s$	Settling Time	10V Step, 0.1%, $A_V = -1$	$\pm 15\text{V}$		230		ns
		10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		280		ns
		5V Step, 0.1%, $A_V = -1$	$\pm 5\text{V}$		240		ns
		5V Step, 0.01%, $A_V = -1$	$\pm 5\text{V}$		380		ns
	Differential Gain	$f = 3.58\text{MHz}$ , $A_V = 2$ , $R_L = 1\text{k}$	$\pm 15\text{V}$		2.2		%
			$\pm 5\text{V}$		2.1		%
	Differential Phase	$f = 3.58\text{MHz}$ , $A_V = 2$ , $R_L = 1\text{k}$	$\pm 15\text{V}$		3.1		Deg
			$\pm 5\text{V}$		3.1		Deg
$R_O$	Output Resistance	$A_V = 1$ , $f = 100\text{kHz}$	$\pm 15\text{V}$		0.7		$\Omega$
$I_S$	Supply Current		$\pm 15\text{V}$		1.0	1.25	mA
			$\pm 5\text{V}$		0.9	1.20	mA

$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	$V_{SUPPLY}$	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage		$\pm 15\text{V}$	●		1.0	mV
			$\pm 5\text{V}$	●		1.0	mV
			$\pm 2.5\text{V}$	●		1.2	mV
	Input $V_{OS}$ Drift	(Note 5)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●	5	8	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		100	nA
$I_B$	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		450	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	●	79		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	77		dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	●	67		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		●	90		dB
$A_{VOL}$	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$ , $R_L = 1\text{k}$	$\pm 15\text{V}$	●	10.0		V/mV
		$V_{OUT} = \pm 10\text{V}$ , $R_L = 500\Omega$	$\pm 15\text{V}$	●	3.3		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 1\text{k}$	$\pm 5\text{V}$	●	10.0		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 500\Omega$	$\pm 5\text{V}$	●	3.3		V/mV
		$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 150\Omega$	$\pm 5\text{V}$	●	0.6		V/mV
		$V_{OUT} = \pm 1\text{V}$ , $R_L = 500\Omega$	$\pm 2.5\text{V}$	●	3.3		V/mV

**ELECTRICAL CHARACTERISTICS**  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	$V_{SUPPLY}$	MIN	TYP	MAX	UNITS
$V_{OUT}$	Output Swing	$R_L = 1\text{k}, V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	13.2		$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	11.5		$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	3.4		$\pm\text{V}$
		$R_L = 150\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	2.3		$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	●	1.2		$\pm\text{V}$
$I_{OUT}$	Output Current	$V_{OUT} = \pm 11.5\text{V}$	$\pm 15\text{V}$	●	23.0		mA
		$V_{OUT} = \pm 2.3\text{V}$	$\pm 5\text{V}$	●	15.3		mA
$I_{SC}$	Short-Circuit Current	$V_{OUT} = 0\text{V}, V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	●	24		mA
SR	Slew Rate	$A_V = -2$ , (Note 3)	$\pm 15\text{V}$	●	150		V/ $\mu\text{s}$
			$\pm 5\text{V}$	●	60		V/ $\mu\text{s}$
GBW	Gain-Bandwidth	$f = 200\text{kHz}, R_L = 2\text{k}$	$\pm 15\text{V}$	●	7.5		MHz
			$\pm 5\text{V}$	●	6.0		MHz
$I_S$	Supply Current		$\pm 15\text{V}$	●		1.45	mA
			$\pm 5\text{V}$	●		1.40	mA

**$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $V_{CM} = 0\text{V}$  unless otherwise noted. (Note 6)**

SYMBOL	PARAMETER	CONDITIONS	$V_{SUPPLY}$	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage		$\pm 15\text{V}$	●		1.5	mV
			$\pm 5\text{V}$	●		1.5	mV
			$\pm 2.5\text{V}$	●		1.7	mV
	Input $V_{OS}$ Drift	(Note 5)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●	5	8	$\mu\text{V}/^{\circ}\text{C}$
$I_{OS}$	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		200	nA
$I_B$	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		550	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$ $V_{CM} = \pm 2.5\text{V}$ $V_{CM} = \pm 0.5\text{V}$	$\pm 15\text{V}$	●	78		dB
			$\pm 5\text{V}$	●	76		dB
			$\pm 2.5\text{V}$	●	66		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		●	90		dB
$A_{VOL}$	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}, R_L = 1\text{k}$	$\pm 15\text{V}$	●	7.0		V/mV
		$V_{OUT} = \pm 10\text{V}, R_L = 500\Omega$	$\pm 15\text{V}$	●	1.7		V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 1\text{k}$	$\pm 5\text{V}$	●	7.0		V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 500\Omega$	$\pm 5\text{V}$	●	1.7		V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 150\Omega$	$\pm 5\text{V}$	●	0.4		V/mV
		$V_{OUT} = \pm 1\text{V}, R_L = 500\Omega$	$\pm 2.5\text{V}$	●	1.7		V/mV
						●	
$V_{OUT}$	Output Swing	$R_L = 1\text{k}, V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	13.0		$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	11.0		$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	3.4		$\pm\text{V}$
		$R_L = 150\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	2.1		$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	●	1.2		$\pm\text{V}$
$I_{OUT}$	Output Current	$V_{OUT} = \pm 11\text{V}$	$\pm 15\text{V}$	●	22		mA
		$V_{OUT} = \pm 2.1\text{V}$	$\pm 5\text{V}$	●	14		mA
$I_{SC}$	Short-Circuit Current	$V_{OUT} = 0\text{V}, V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	●	23		mA
SR	Slew Rate	$A_V = -2$ , (Note 3)	$\pm 15\text{V}$	●	120		V/ $\mu\text{s}$
			$\pm 5\text{V}$	●	50		V/ $\mu\text{s}$
GBW	Gain Bandwidth	$f = 200\text{kHz}, R_L = 2\text{k}$	$\pm 15\text{V}$	●	7.0		MHz
			$\pm 5\text{V}$	●	5.5		MHz
$I_S$	Supply Current		$\pm 15\text{V}$	●		1.50	mA
			$\pm 5\text{V}$	●		1.45	mA

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full specified temperature range.

**Note 1:** Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

**Note 2:** A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

**Note 3:** Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

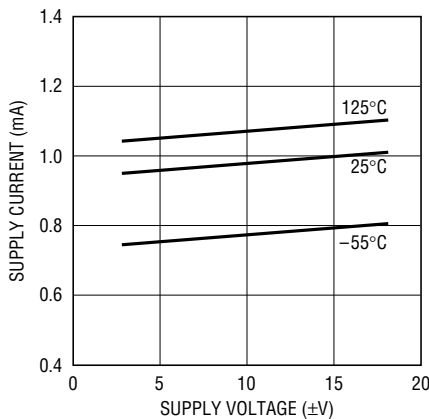
**Note 4:** Full power bandwidth is calculated from the slew rate measurement:  $FPBW = SR/2\pi V_p$ .

**Note 5:** This parameter is not 100% tested.

**Note 6:** The LT1354 is designed, characterized and expected to meet these extended temperature limits, but is not tested at -40°C and at 85°C. Guaranteed I grade parts are available; consult factory.

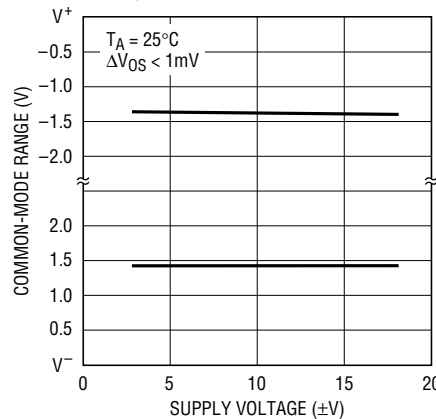
## TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



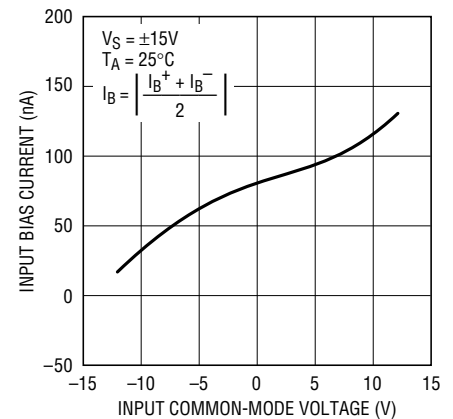
1354 G01

Input Common-Mode Range vs Supply Voltage



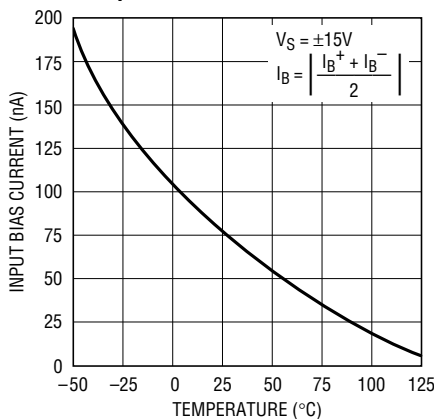
1354 G02

Input Bias Current vs Input Common-Mode Voltage



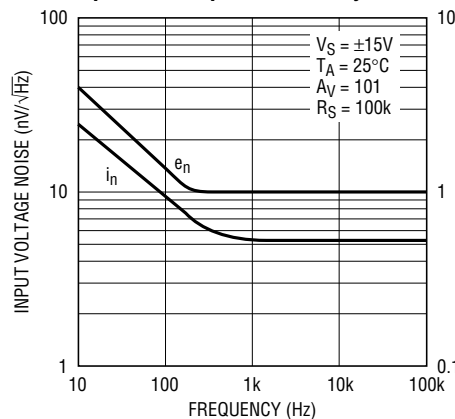
1354 G03

Input Bias Current vs Temperature



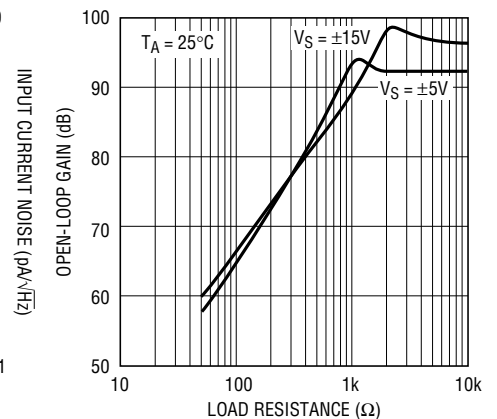
1354 G04

Input Noise Spectral Density



1354 G05

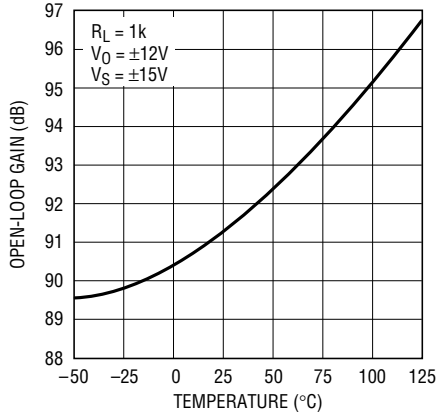
Open-Loop Gain vs Resistive Load



1354 G06

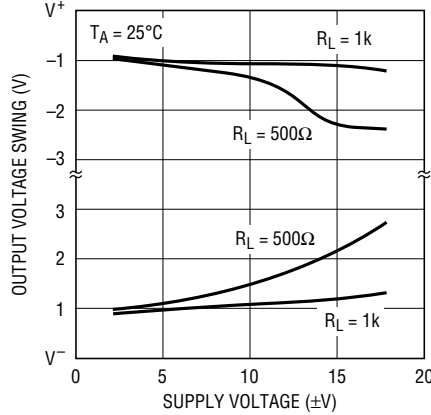
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Gain vs Temperature



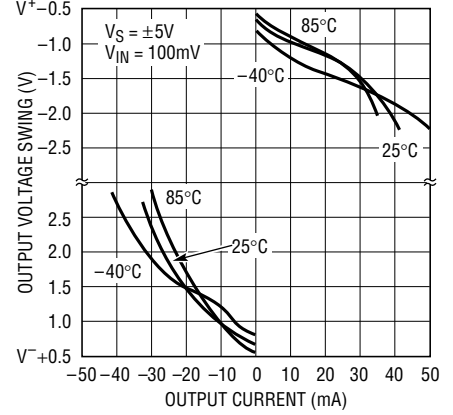
1354 G07

Output Voltage Swing vs Supply Voltage



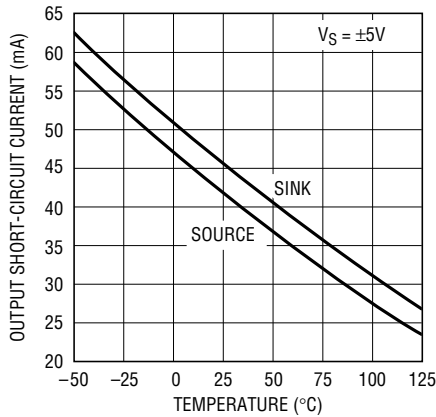
1354 G08

Output Voltage Swing vs Load Current



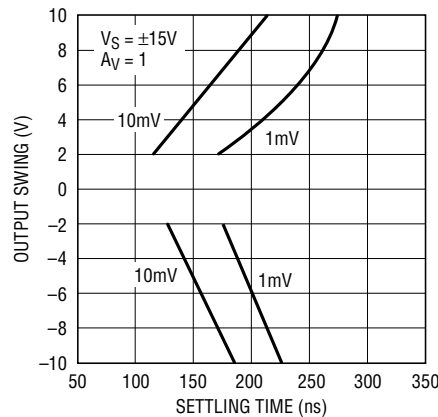
1354 G09

Output Short-Circuit Current vs Temperature



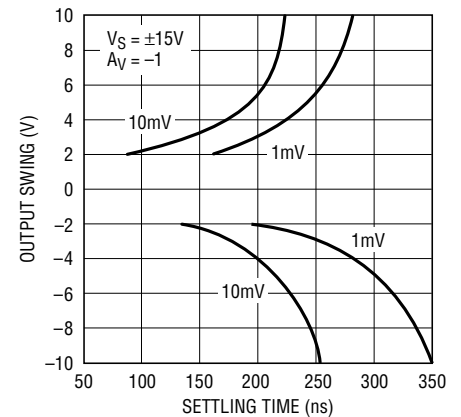
1354 G10

Settling Time vs Output Step (Noninverting)



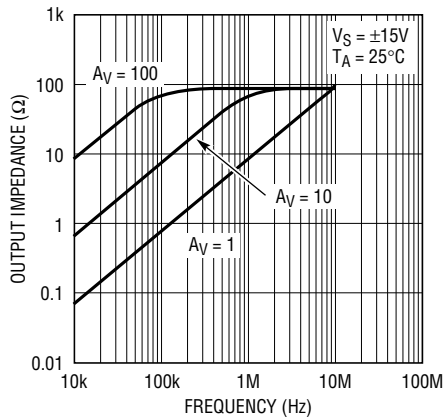
1354 G11

Settling Time vs Output Step (Inverting)



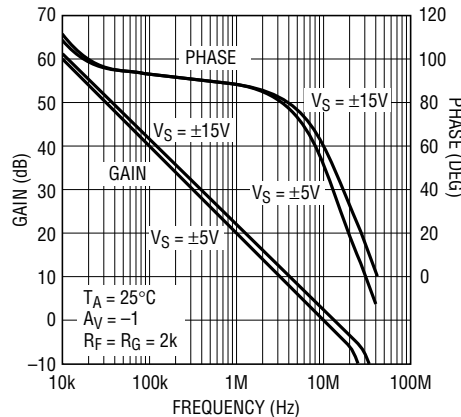
1355/1356 G12

Output Impedance vs Frequency



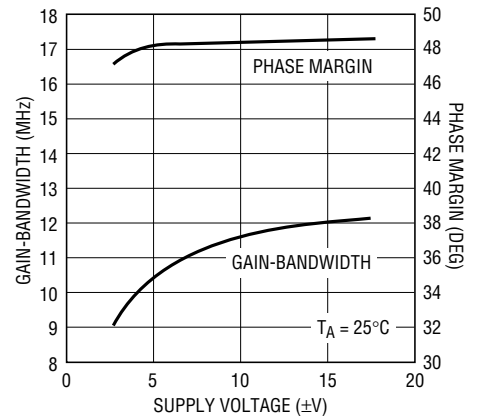
1354 G13

Gain and Phase vs Frequency



1354 G14

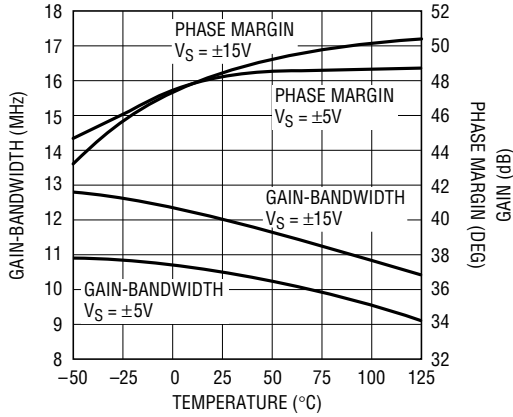
Gain-Bandwidth and Phase Margin vs Supply Voltage



1354 G15

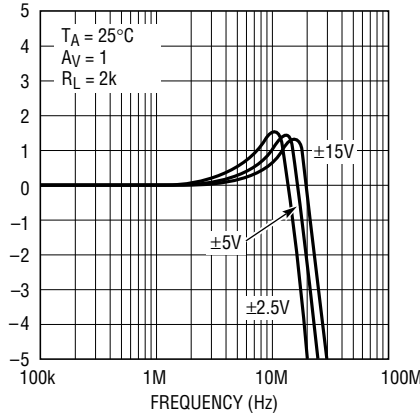
# TYPICAL PERFORMANCE CHARACTERISTICS

**Gain-Bandwidth and Phase Margin vs Temperature**



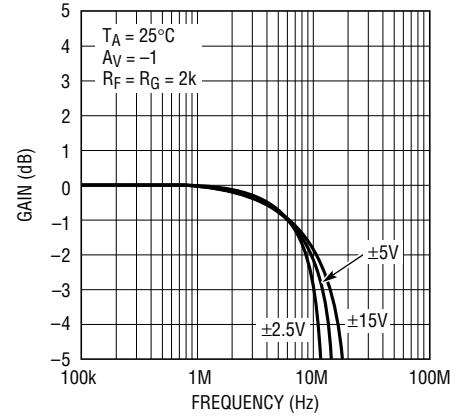
1354 G16

**Frequency Response vs Supply Voltage ( $A_V = 1$ )**



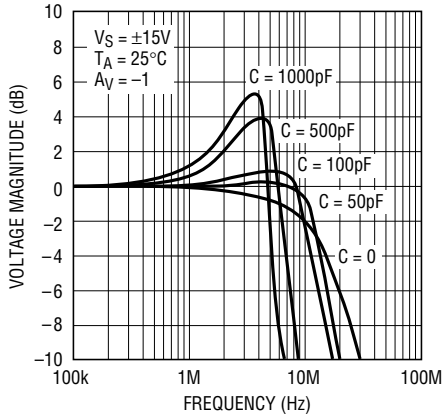
1354 G17

**Frequency Response vs Supply Voltage ( $A_V = -1$ )**



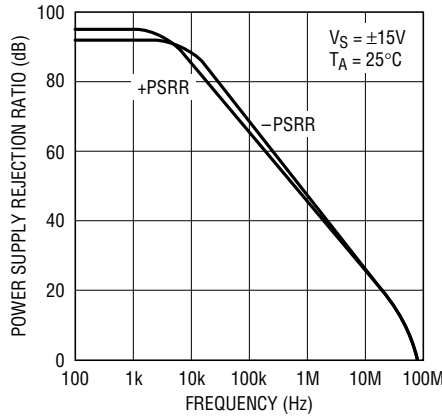
1354 G18

**Frequency Response vs Capacitive Load**



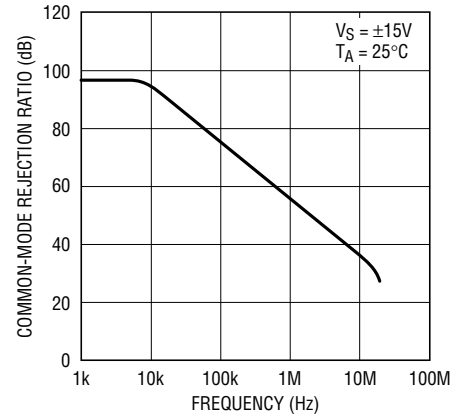
1354 G19

**Power Supply Rejection Ratio vs Frequency**



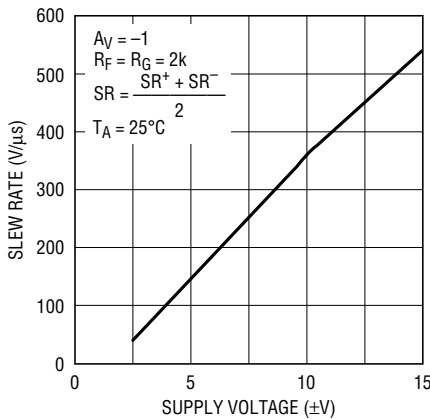
1354 G20

**Common-Mode Rejection Ratio vs Frequency**



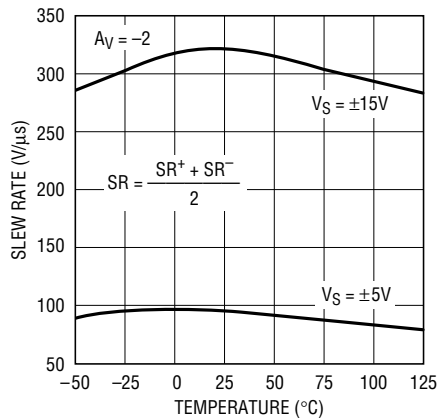
1354 G21

**Slew Rate vs Supply Voltage**



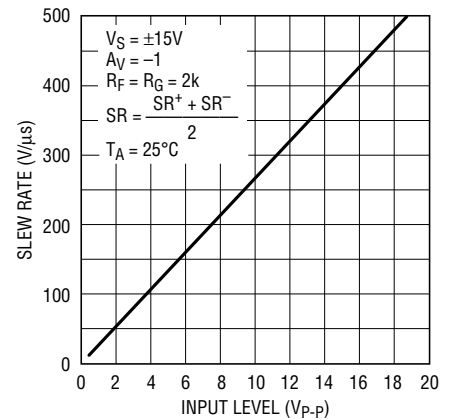
1354 G22

**Slew Rate vs Temperature**



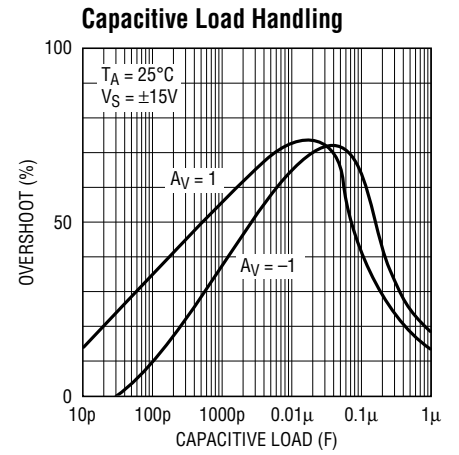
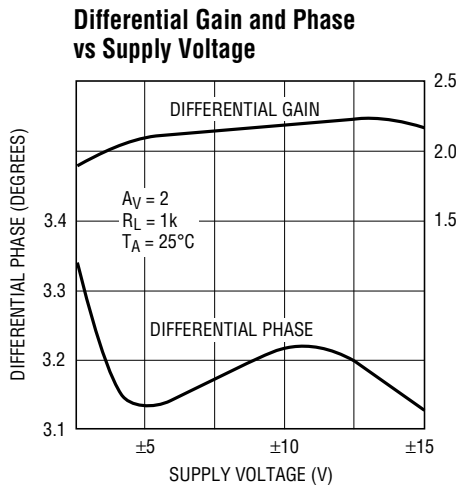
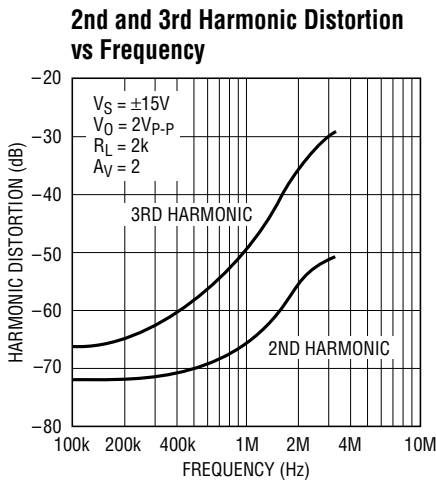
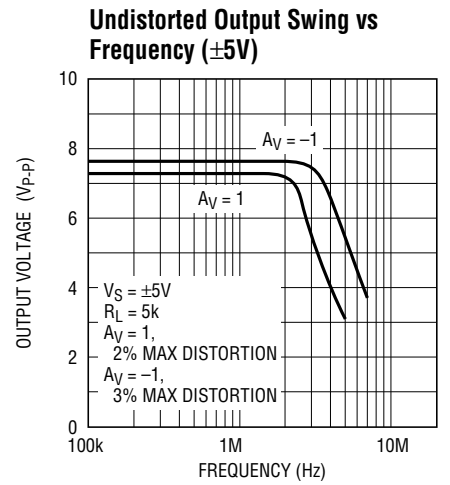
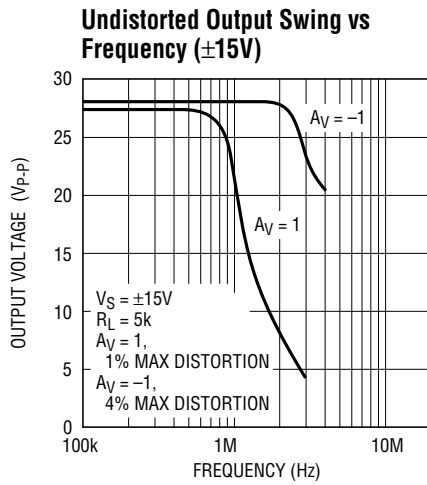
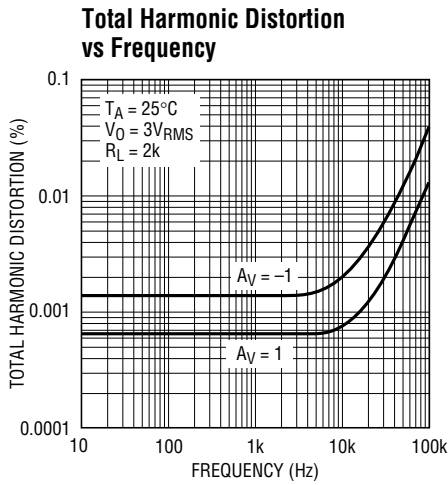
1354 G23

**Slew Rate vs Input Level**

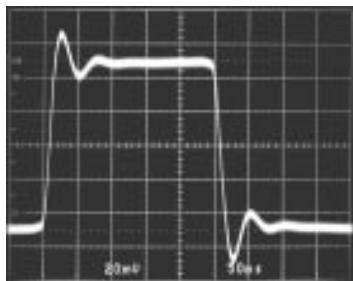


1354 G24

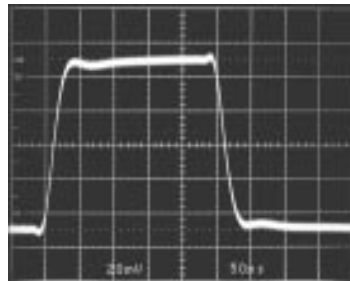
**TYPICAL PERFORMANCE CHARACTERISTICS**



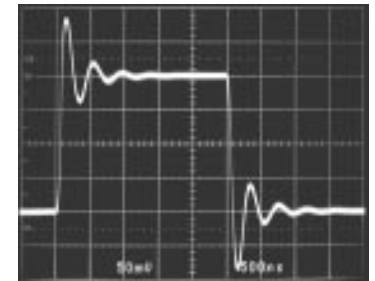
**Small-Signal Transient ( $A_V = 1$ )**



**Small-Signal Transient ( $A_V = -1$ )**



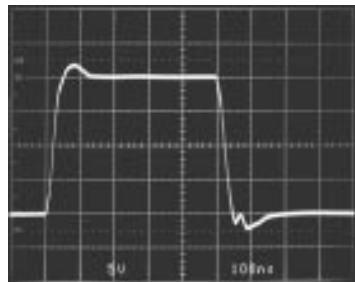
**Small-Signal Transient ( $A_V = -1$ ,  $C_L = 1000\text{pF}$ )**





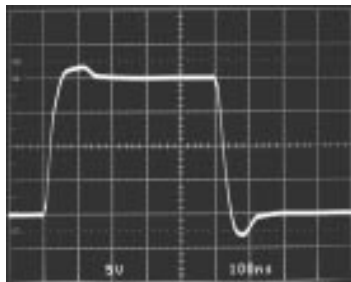
## TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Transient  
( $A_V = 1$ )



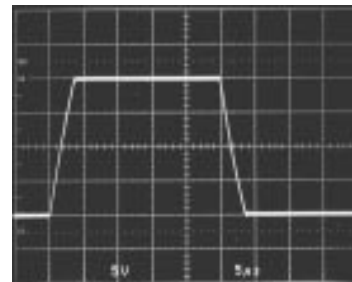
1354 TA34

Large-Signal Transient  
( $A_V = -1$ )



1354 TA35

Large-Signal Transient  
( $A_V = 1, C_L = 10,000\text{pF}$ )

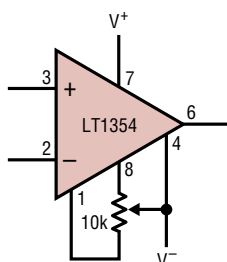


1354 TA36

## APPLICATIONS INFORMATION

The LT1354 may be inserted directly into many high speed amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1354 is shown below.

Offset Nulling



1354 AI01

### Layout and Passive Components

The LT1354 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01 $\mu\text{F}$  to 0.1 $\mu\text{F}$ ). For high drive current applications use low ESR bypass capacitors (1 $\mu\text{F}$  to 10 $\mu\text{F}$  tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than 5k $\Omega$ , a parallel capacitor of value

$$C_F > (R_G \cdot C_{IN})/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used,  $C_F$  should be greater than or equal to  $C_{IN}$ .

### Capacitive Loading

The LT1354 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small-signal response with 1000pF load shows 43% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited to 5V/ $\mu\text{s}$  by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75 $\Omega$ ) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

## APPLICATIONS INFORMATION

### Input Considerations

Each of the LT1354 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. *The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs.* Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

### Power Dissipation

The LT1354 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature ( $T_J$ ) is calculated from the ambient temperature ( $T_A$ ) and power dissipation ( $P_D$ ) as follows:

$$\text{LT1354CN8: } T_J = T_A + (P_D \cdot 130^\circ\text{C/W})$$

$$\text{LT1354CS8: } T_J = T_A + (P_D \cdot 190^\circ\text{C/W})$$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of

either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore  $P_{D\text{MAX}}$  is:

$$P_{D\text{MAX}} = (V^+ - V^-)(I_{S\text{MAX}}) + (V^+/2)^2/R_L$$

Example: LT1354CS8 at 70°C,  $V_S = \pm 15\text{V}$ ,  $R_L = 100\Omega$  (Note: the minimum short-circuit current at 70°C is 24mA, so the output swing is guaranteed only to 2.4V with 100Ω.)

$$P_{D\text{MAX}} = (30\text{V} \cdot 1.45\text{mA}) + (15\text{V} - 2.4\text{V})(24\text{mA}) = 346\text{mW}$$

$$T_{J\text{MAX}} = 70^\circ\text{C} + (346\text{mW} \cdot 190^\circ\text{C/W}) = 136^\circ\text{C}$$

### Circuit Operation

The LT1354 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive an 800Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by  $R_1$ , so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1354 is tested for slew rate in a gain of -2 so higher slew rates can be expected in gains of 1 and -1, and lower slew rates in higher gain configurations.

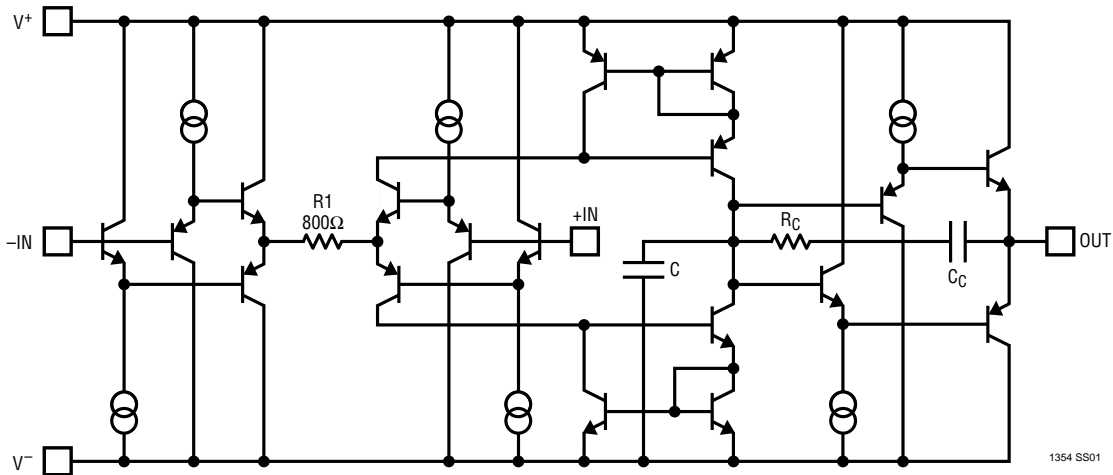
The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance

## APPLICATIONS INFORMATION

slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase

to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

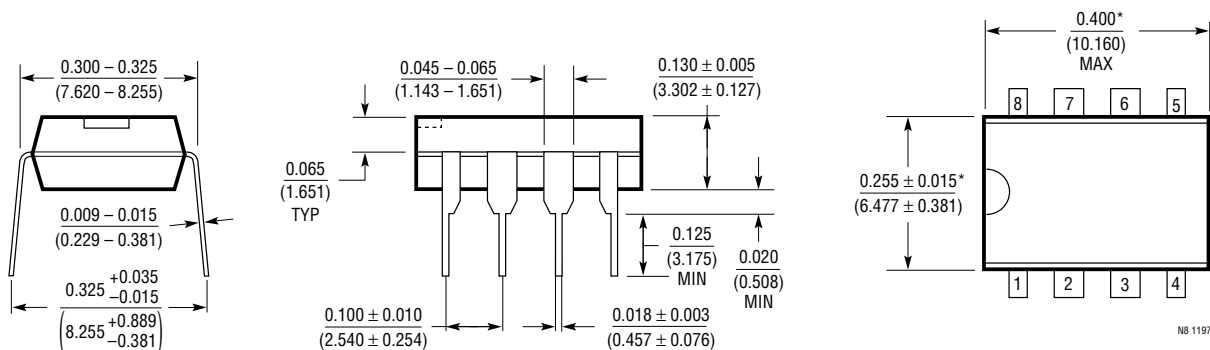
## SIMPLIFIED SCHEMATIC



## PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

**N8 Package**  
**8-Lead PDIP (Narrow 0.300)**  
 (LTC DWG # 05-08-1510)

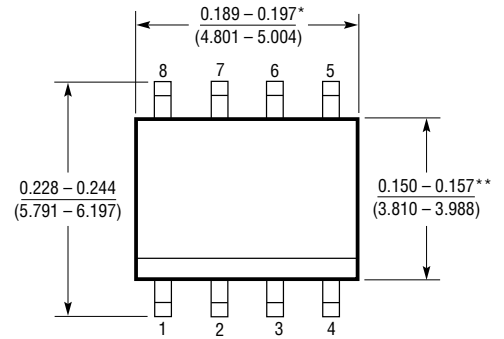
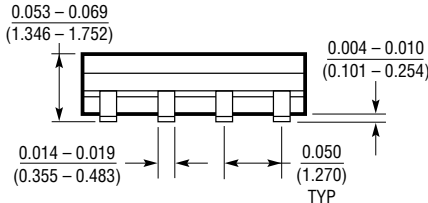
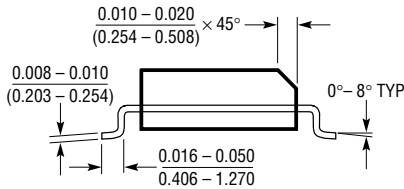


\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

## PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

### S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



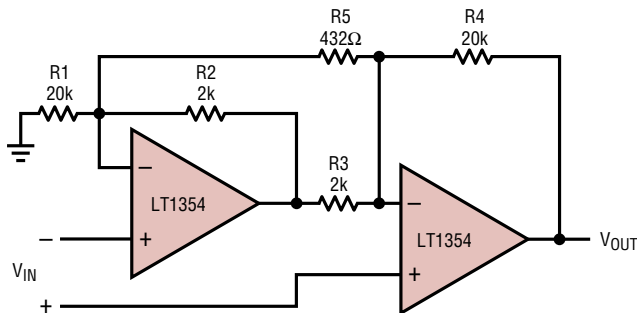
\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

508 0996

## TYPICAL APPLICATIONS

### Instrumentation Amplifier

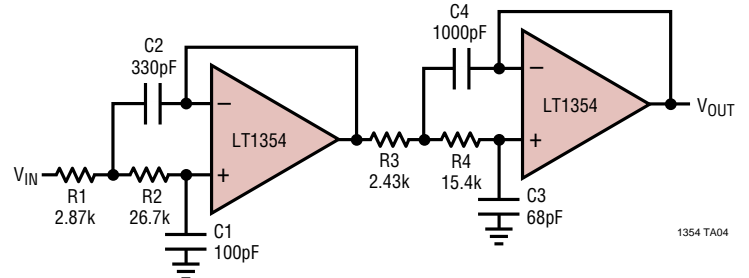


$$A_V = \frac{R_4}{R_3} \left[ 1 + \frac{1}{2} \left( \frac{R_2}{R_1} + \frac{R_3}{R_4} \right) + \frac{R_2 + R_3}{R_5} \right] = 104$$

TRIM R5 FOR GAIN  
TRIM R1 FOR COMMON MODE REJECTION  
BW = 120kHz

1354 TA03

### 100kHz, 4th Order Butterworth Filter (Sallen-Key)



1354 TA04

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1355/LT1356	Dual/Quad 1mA, 12MHz, 400V/μs Op Amp	Good DC Precision, Stable with All Capacitive Loads
LT1357	2mA, 25MHz, 600V/μs Op Amp	Good DC Precision, Stable with All Capacitive Loads
LT1358/LT1359	Dual/Quad 2mA, 25MHz, 600V/μs Op Amp	Good DC Precision, Stable with All Capacitive Loads