KCU1500 Board

User Guide

UG1260 (v1.4) October 12, 2018

XILINX

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/12/2018	1.4	Added Electrostatic Discharge Caution. Revised DDR4 Component Memory.
08/07/2018	1.3	Revised Step 4: Program the Base Platform.
07/09/2018	1.2	Revised Installing the KCU1500 Board in a Server Chassis, Table 3-2, System Clock, QSFP0 Clock, and EMCCLK, and QSFP1 Clock. Removed Xilinx constraints file information. Added Appendix A, Board Installation.
05/23/2018	1.1	Updated Appendix A, Xilinx Constraints File Listing.
08/16/2017	1.0	Initial Xilinx release.

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Chapter 1

Introduction

Overview

The KCU1500 data center board for the Xilinx® Kintex® UltraScale™ FPGA implements a Xilinx FPGA-based PCIe® accelerator add-in card for use in open compute project servers. This accelerator card is PCIe Gen 3 x16 compliant in a full-height half-length form factor, and can be used in servers that support PCIe x16 cards with bifurcation to dual x8 links or single x8 link without bifurcation. The accelerator card is designed for PCIe x16 bifurcated into two PCIe Gen3 x8 (or lower) links. PCIe bifurcation allows the card to enumerate as two independent PCIe links.

The Xilinx PCIe accelerator card functions as a programmable accelerator in data center applications. See Figure 1-1.

Figure 1-1: **KCU1500 PCIe Data Center Board**

Additional Resources

See Appendix C, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the KCU1500 data center board.

Block Diagram

The block diagram of the KCU1500 data center board is shown in Figure 1-2.

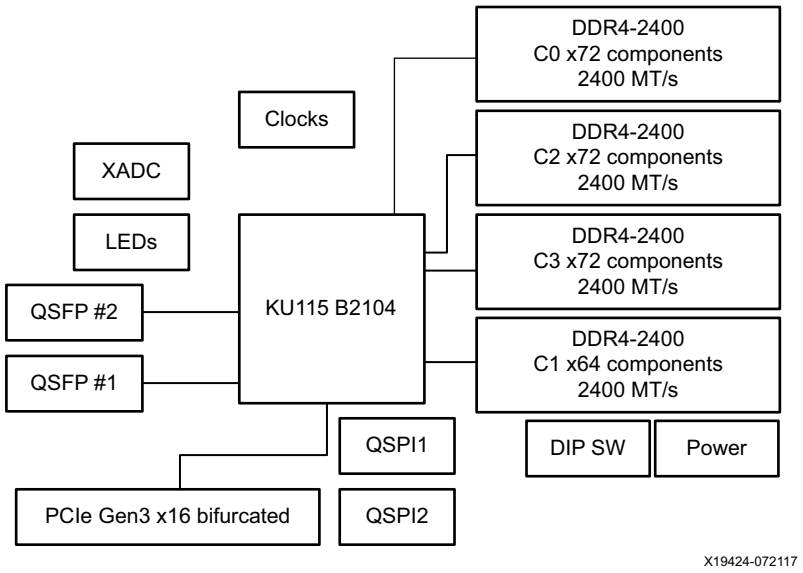


Figure 1-2: **KCU1500 Data Center Board Block Diagram**

Board Features

The KCU1500 data center board features are listed in this section. Detailed information for each feature is provided in Chapter 3, Board Component Descriptions.

- Kintex UltraScale XCKU115-2FLVB2104E FPGA
- Memory (four independent single-rank DDR4 interfaces)
  - 16 GB DDR4 memory
    - 3x DDR4 4GB, 2400MT/s, 64-bit w/ ECC
    - 1x DDR4 4GB, 2400MT/s, 64-bit w/ no ECC
- Configuration options
  - Dual 512 Mb Quad SPI flash memory (1 Gb total)
  - Micro-B USB J34 JTAG configuration port (FT2232 U65 bridge)
  - Platform cable header J2 JTAG configuration port
- 64 GTH transceivers (16 Quads)
  - 16-lane PCI Express® (16 GTH transceivers)
  - 2xQSFP28 connectors (40 Gb Ethernet ports) (Eight GTH transceivers)
  - 40 GTH not used
- Clock sources
  - 2xSI5335A quad clock generator
  - Si570 I2C programmable LVDS clock generator
- USB-to-UART FT2232 bridge with micro-B USB connector
- PCIe endpoint connectivity
  - Gen1, 2, or 3 x8
  - Gen1, 2, or 3 x16 bifurcated into two x8
- I2C bus
- Status LEDs
- User I/O
- Program_B pushbutton
- Power management with PMBus voltage monitoring through Maxim power controllers and GUI

Board Specifications

Dimensions

Height: 3.874 inch (9.84 cm)

Thickness (±5%): 0.062 inch (0.157 cm)

Length: 6.60 inch (16.76 cm)

Note: A 3D model of this board is not available.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: –25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

PCIe slot +12 V_{DC}, +3.3 V_{DC}, +3.3 V_{AUXDC}

Chapter 2

Board Setup and Configuration

Board Component Location

Figure 2-1 shows the KCU1500 board component locations. Each numbered component shown in the figure is keyed to Table 2-1. Table 2-1 identifies the components, references the respective schematic page numbers, and links to a detailed functional description of the components and board features in Chapter 3.

IMPORTANT: *Figure 2-1 is for visual reference only and might not reflect the current revision of the board.*

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.

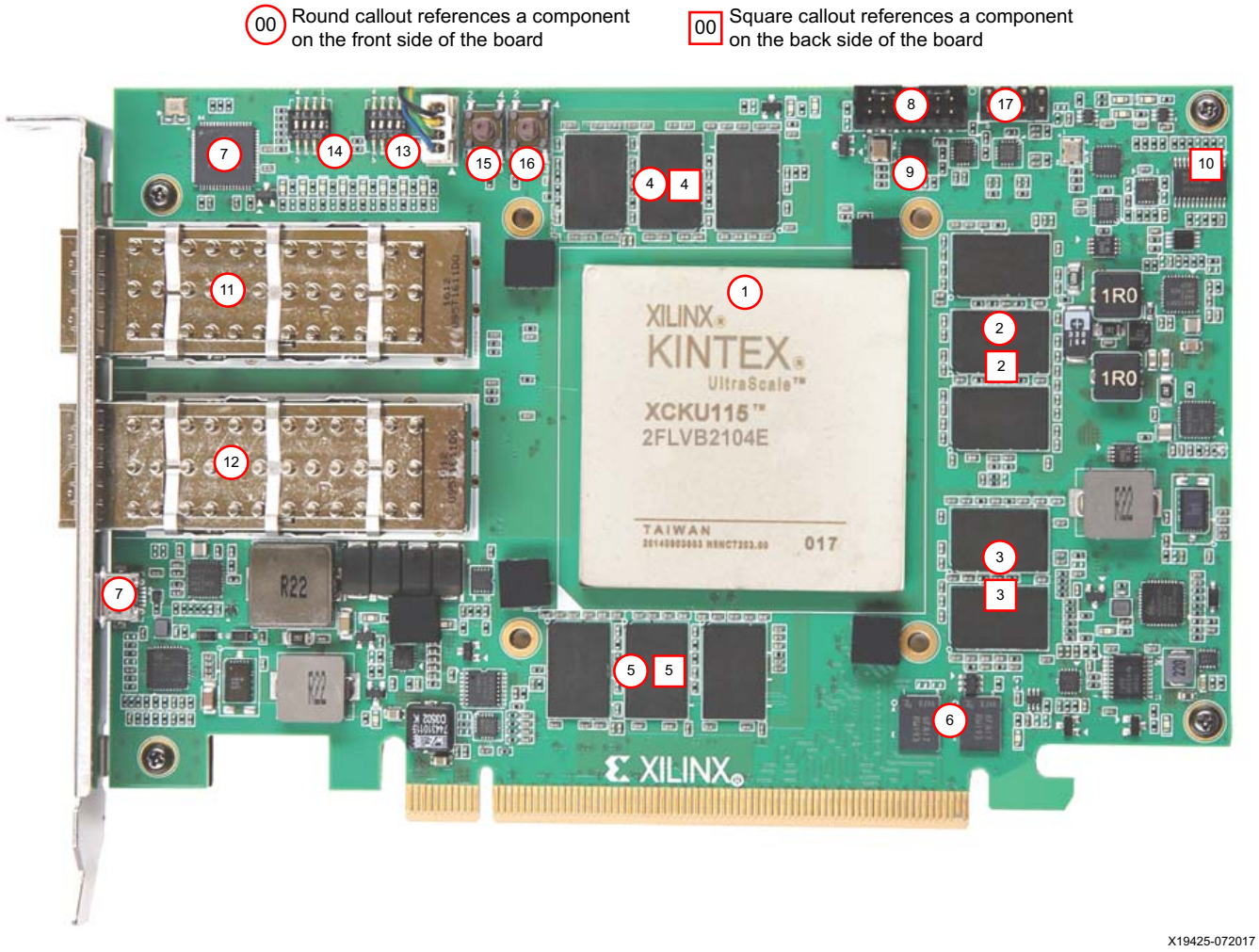


Figure 2-1: **KCU1500 Data Center Board Components**

Table 2-1: **KCU1500 Board Component Descriptions**

Callout Number	Ref. Des.	Feature	Notes	Schematic Page
1	U1	UltraScale™ Kintex®	XCKU115-2FLVB2104E	
2	M2,M3,M4,M5,M7	C0 DDR4 72-bit component memory (4 Gb)	Micron MT40A512M16JY-083E:B	4,5
3	M6,M7,M8,M9	C1 DDR4 64-bit component memory (4 Gb)	Micron MT40A512M16JY-083E:B	7,8
4	M10,M11,M12,M13,M18	C2 DDR4 72-bit component memory (4 Gb)	Micron MT40A512M16JY-083E:B	10,11
5	M14,M15,M16,M17,M19	C3 DDR4 72-bit component memory (4 Gb)	Micron MT40A512M16JY-083E:B	13,14
6	U7,U8	Quad SPI flash memory (1 Gb total)	Micron MT25QU512ABB8E12-0SIT	20
7	U65,J34	USB JTAG module with separate USB micro-B connector	FT2232HQ, E-Call Enterprise Co. 0653-03-2011-1-052	34
8	J2	JTAG 7X2_2MM_SMT connector	E-Call Enterprise Co. 0151-01-229-041140	19
9	U47	SYSCLK, 300 MHz, 1.8V LVDS	SI5335A-B02436-GM	28
10	U40	USER_SI570_CLOCK, 156.25MHz, 3.3V LVDS	Silicon labs SI570BAB000544DG	28
11	J28	QSFP0 (40 Gb Ethernet)	Amphenol FS1-Z38-20Z6-60	28
12	J30	QSFP1 (40 Gb Ethernet)	Amphenol FS1-Z38-20Z6-60	29

Default Switch Settings

Default switch settings are listed in Table 2-2. Switch locations are shown in Figure 2-1.

Table 2-2: **Default Switch Settings**

Switch	Function	Default	Comments	Figure 2-1 Callout	Schematic Page
SW4	4-pole GPIO DIP	[4:1] 0000 where 0 = On	4-POLE USER DIP	13	18
SW5	4-pole MODE DIP	[4:1] 0001 where 0 = On	MODE[0:2] DIP, 1-POLE USER DIP	14	19

Table 2-3 shows other visible switch and connector locations.

Table 2-3: **Other Visible Switches and Connectors**

Component	Function	Comments	Figure 2-1 Callout	Schematic Page
SW2	Pushbutton switch	CPU_RESET_B	15	18
SW3	Pushbutton switch	PROGRAM_B	16	18
J11	8-pin (2X4) male HDR	MAXIM PMBus cable connector	17	35
J2	14-pin (2X7) 2mm JTAG	JTAG flat-cable connector	8	19

Installing the KCU1500 Board in a Server Chassis

Because each server or PC vendors hardware is different, for physical card installation guidance, see the manufacturer's PCIe card installation instructions.

For programming and start-up details, see Appendix A, Board Installation.

FPGA Configuration

The KCU1500 board supports two UltraScale™ FPGA configuration modes:

- Quad SPI flash memory
- JTAG using:
  - Platform cable header J2
  - USB JTAG configuration port (USB J34/FT2232H U65)

At power up, the FPGA is configured by dual Quad SPI NOR flash devices (Micron MT25QU512ABB8E12-0SIT) operating at a clock rate of 90 MHz (EMCCLK) using the "Master Serial" Configuration mode. An external EMCCLK configuration clock is used to allow for the highest configuration speed with SPI flash, and the dual Quad SPI flash memory devices provide a total datapath of 8 bits.

Each of the Quad SPI flash memory NOR devices has a capacity of 512 Mb. The two Quad SPI flash memory devices provide a combined configuration capacity of 1 Gb.

Two configuration modes are supported on the KCU1500, as listed in Table 2-4. While the FPGA mode pins M2, M1, and M0 are wired to the active-Low mode DIP SW5, only M2 on SW5 pin 7 should be toggled to select between M[2:0] = `001` and `101`. The FPGA default mode setting is M[2:0] = `001` = SW5[2:4] = (On, On, Off), selecting the Quad SPI flash memory configuration mode.

For complete details on configuring the FPGA, see the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 1].

Table 2-4: **Configuration Modes**

Configuration Modes	M[2:0]	Bus Width	CCLK Direction
Master SPI	`001`	x1, x2, x4	FPGA output
JTAG	`101`	x1	N/A

The mode DIP SW5 is shown in Figure 2-2.

Note: For this DIP SW5 switch, moving the switch toward the label ON is a 0. DIP switch labels 2, 3, and 4 are equivalent to mode pins M2, M1, and M0. The default = master SPI = M[2:0] = 001 = SW5[2:4] = On, On, Off.

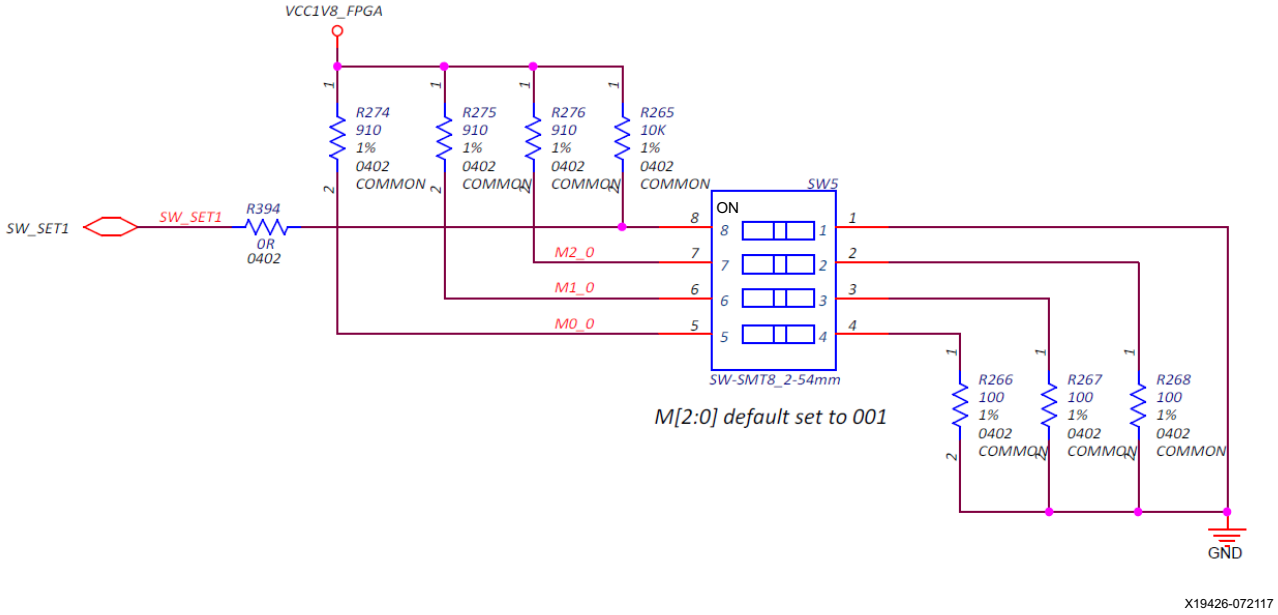


Figure 2-2: **KCU1500 Mode DIP SW5**

Chapter 3

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 2-1, page 11 identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are listed in Table 2-1, page 11.

Component Descriptions

Kintex UltraScale XCKU115-2FLVB2104E Device

[Figure 2-1, callout 1]

The KCU1500 board is populated with the Kintex® UltraScale™ XCKU115-2FLVB2104E device.

For more information on Kintex UltraScale FPGAs, see the *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS892) [Ref 2].

I/O Voltage Rails

There are 15 I/O banks available on the XCKU115 device and the KCU1500 board. The voltages applied to the XCKU115 U1 FPGA I/O banks are listed in Table 3-1.

Table 3-1: **I/O Bank Voltage Rails**

XCKU115	Power Net Name	Voltage	Connected To
Bank 44	VCC1V2_FPGA	1.2V	DDR4 C0 DQ[0:31]
Bank 45	VCC1V2_FPGA	1.2V	DDR4 C0 DQ[64:71], ADDR/CTRL
Bank 46	VCC1V2_FPGA	1.2V	DDR4 C0 DQ[32:63]
Bank 50	VCC1V2_FPGA	1.2V	DDR4 C2 DQ[0:31]
Bank 51	VCC1V2_FPGA	1.2V	DDR4 C2 DQ[64:71], ADDR/CTRL
Bank 52	VCC1V2_FPGA	1.2V	DDR4 C2 DQ[32:63]
Bank 65	VCC1V8_FPGA	1.8V	SPI1,QSFP_CTRL,SYSMON,USER_LED,USER_DIP
Bank 66	VCC1V2_FPGA	1.2V	DDR4 C1 DQ[0:31]
Bank 67	VCC1V2_FPGA	1.2V	DDR4 C1 DQ[32:47], ADDR/CTRL
Bank 68	VCC1V2_FPGA	1.2V	DDR4 C1 DQ[48:63]
Bank 71	VCC1V2_FPGA	1.2V	DDR4 C3 DQ[0:31]
Bank 72	VCC1V2_FPGA	1.2V	DDR4 C3 DQ[64:71], ADDR/CTRL
Bank 73	VCC1V2_FPGA	1.2V	DDR4 C3 DQ[32:63]
Bank 84	VCC1V8_FPGA	1.8V	QSFP_CTRL,I2C_MAIN,USER_SI570_CLOCK
Bank 94	VCC1V8_FPGA	1.8V	USB_UART

DDR4 Component Memory

[Figure 2-1, callout 2, 3, 4, 5]

Four independent single-rank DDR4 interfaces are available on the KCU1500 board, each providing 4 GB of memory and implemented with soldered down DDR4 memory components.

- Manufacturer: Micron
- Part Number: MT40A512M16JY-083E
- Description:
  - 8 Gb (512 Mb x 16)
  - 1.2V 96-ball FBGA
  - DDR4-2400

The KCU1500 XCKU115 FPGA DDR interface performance is documented in the *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS892) [Ref 2].

Three of the interfaces (C0, C2, and C3) are 72-bits wide (support for ECC), and the fourth interface (C1) is 64-bits wide (non-ECC). The component memories are configured in a clamshell topology where the devices for a given interface have different chip selects for the top and bottom mounted components.

The memory interface-to-FPGA bank assignments are listed in Table 3-1. The DDR4 0.6V VTT termination voltages are sourced from four independent TI TPS51200DR regulator circuits.

The KCU1500 DDR4 memory component interfaces adhere to the constraints guidelines documented in the "DDR3/DDR4 Design Guidelines" section of the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150) [Ref 3]. The KCU1500 board DDR4 memory component interfaces are 40Ω impedance implementations. For more details about the Micron DDR4 component memory, see the Micron MT40A512M16JY-083E data sheet at the Micron website [Ref 9].

Dual Quad SPI Flash Memory

[Figure 2-1, callout 6]

The Quad SPI flash memory located at U7 and U8 provides 2 x 512 Mb of nonvolatile storage that can be used for configuration and data storage.

- Part number: MT25QU512ABB8E12-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 8 bits
- Data rate: variable, depending on single, dual, or quad mode and whether the EMCCLK or the internal CCLK is used (bitstream configurable)

For details on bank 0 pins, see the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 1].

Figure 3-1 shows the linear Quad SPI flash memory circuitry on the KCU1500 board. For more flash memory details, see the Micron MT25QU512ABB8E12-0SIT data sheet at the Micron website [Ref 9].

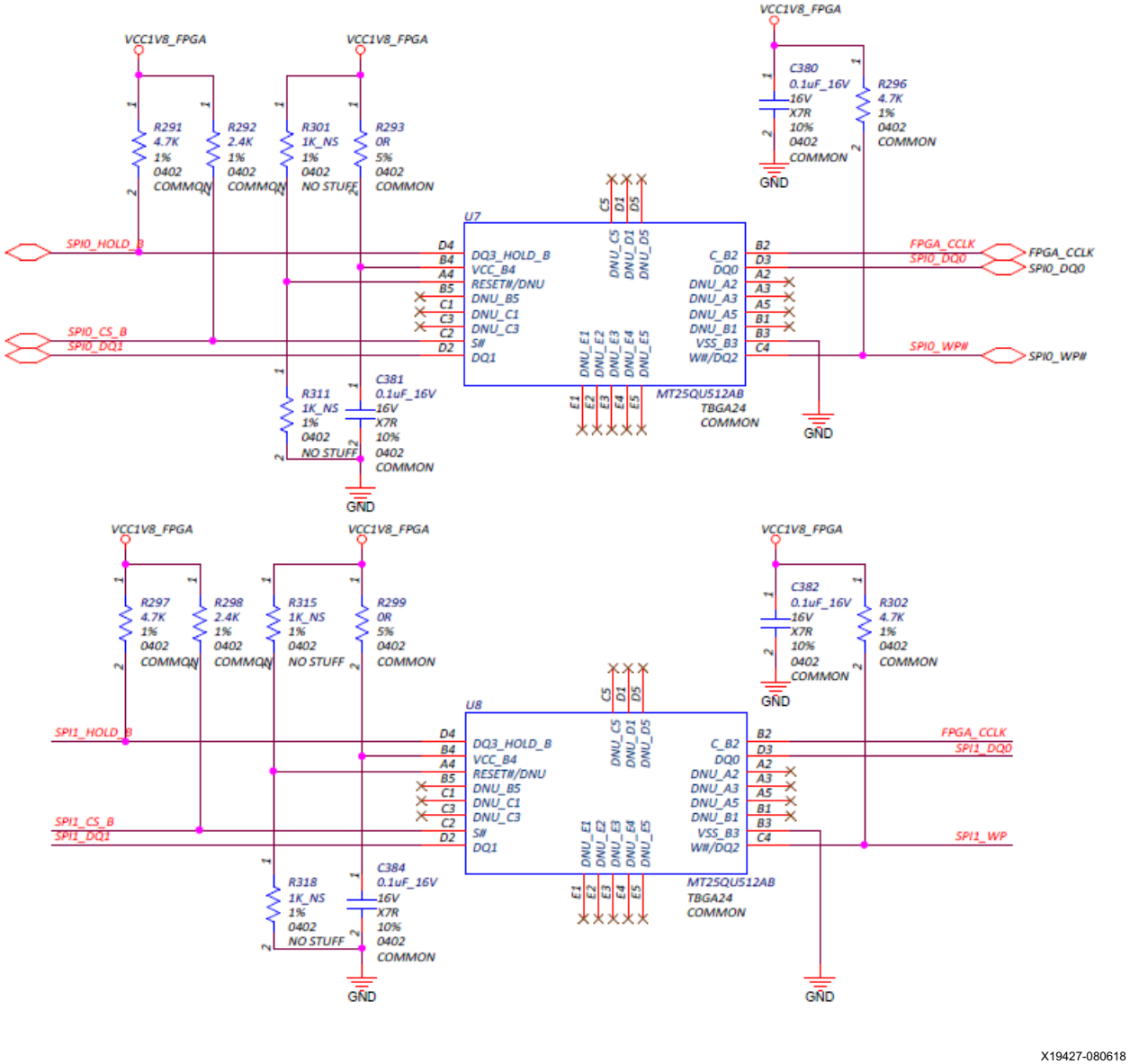


Figure 3-1: **Dual Quad SPI 1 Gb Flash Memory**

USB JTAG Interface

[Figure 2-1, callout 7, 8]

The KCU1500 board XCKU115 FPGA is the only component on the JTAG chain. JTAG configuration is available through a 2 mm JTAG header (J2), providing access by Xilinx® download cables, such as the Platform Cable USB II and the Parallel Cable IV. JTAG configuration is allowed at any time regardless of the FPGA mode pin settings. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pin M2 wired to DIP SW5 pin 7.

Alternate JTAG programming is available via the USB-to-JTAG bridge function provided by the FT2232H device (U65), in which a host computer accesses the KCU1500 board JTAG chain through a type-A (host side) to micro-B (KCU1500 board side J34) USB cable.

For more details about the FT2232H device, see the Future Technology Devices International Ltd. website [Ref 10].

Clock Generation

[Figure 2-1, callout 9, 10]

The KCU1500 board provides eight clock sources to the XCKU115 device as listed in Table 3-2.

Table 3-2: **KCU1500 Board Clock Sources**

Clock Name	Clock Ref. Des.	Description
System clock 300 MHz	U47 (CLK0)	Silicon Labs Si5335A 1.8V LVDS any frequency quad clock generator CLK0. See System Clock, QSFP0 Clock, and EMCCLK (SYSCLK_300_P/N).
QSFP0 clock 156.25 MHz	U47 (CLK1)	Silicon Labs Si5335A 1.8V LVDS any frequency quad clock generator CLK1. See System Clock, QSFP0 Clock, and EMCCLK (QSFP0_CLOCK_P/N).
EMC clock 90 MHz	U47 (CLK2)	Silicon Labs Si5335A 1.8V LVCMOS single-ended any frequency quad clock generator CLK2. See System Clock, QSFP0 Clock, and EMCCLK (FPGA_EMCCLK).
QSFP1 clock 156.25 MHz	U48 (CLK1)	Silicon Labs Si5335A 1.8V LVDS any frequency quad clock generator CLK1. See QSFP1 Clock (QSFP1_CLOCK_P/N).
User MGT clock 10 MHz–810 MHz	U40	Silicon Labs Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default. (USER_SI570_CLOCK_P/N and USER_MGT_SI570_CLOCK[1:0]_P/N). See Programmable MGT and User Clock.
PEX_REFCLK (PCIe® input)	CN1/U55	PCIe edge connector. CN1 input clock 100 MHz to SI53322 U55 1-to-2 clock buffer (PEX_REFCLK_225/226_P/N).

System Clock, QSFP0 Clock, and EMCCLK

[Figure 2-1, callout 9]

The system clock source is a Silicon Labs SI5335A quad clock generator/buffer (U47).

- Clock generator: Silicon Labs SI5335A-B06201-GM (CLK0A 300 MHz)
  - Frequency plan: FS1, FS0=01
    - Input Type: crystal, input frequency 25 MHz
    - Device operating mode: clock generator loop bandwidth 1.6 MHz
    - CLK0A/0B: 300 MHz 1.8V LVDS
    - CLK1A/1B: 156.25 MHz 1.8V LVDS
    - CLK2A/2B: 90 MHz 1.8V CMOS (output on A only)
    - CLK3A/3B: 33.333 MHz 1.8V CMOS (output on A only)
- Low phase jitter of 0.7pS RMS

Three outputs of the SI5335A U47 are used:

- CLK0A/B

  The system clock (SYSCLK) is an LVDS 300 MHz clock wired to SI53340 (U46) 1-to-4 clock buffer, which drives four AC coupled versions of the 300 MHz clock into the clock capable (GC) inputs on the four DDR4 interface banks (C0: bank 45, C1: bank 67, C2: bank 51, and C3: bank 71).

- CLK1A/B

  The QSFP0_CLOCK_P/N clock is an AC coupled LVDS 156.25 MHz clock wired to QSFP0 interface MGTH bank 127 MGTREFCLK1P/N input pins AU36 and AU37.

- CLK2A

  This 90 MHz single-ended series resistor damped LVCMOS18 FPGA_EMCCLK is wired to FPGA U1 dedicated bank 65 EMCCLK input pin.

- CLK3A is not used.

The system, QSFP0, and EMCCLK clock circuit is shown in Figure 3-2.

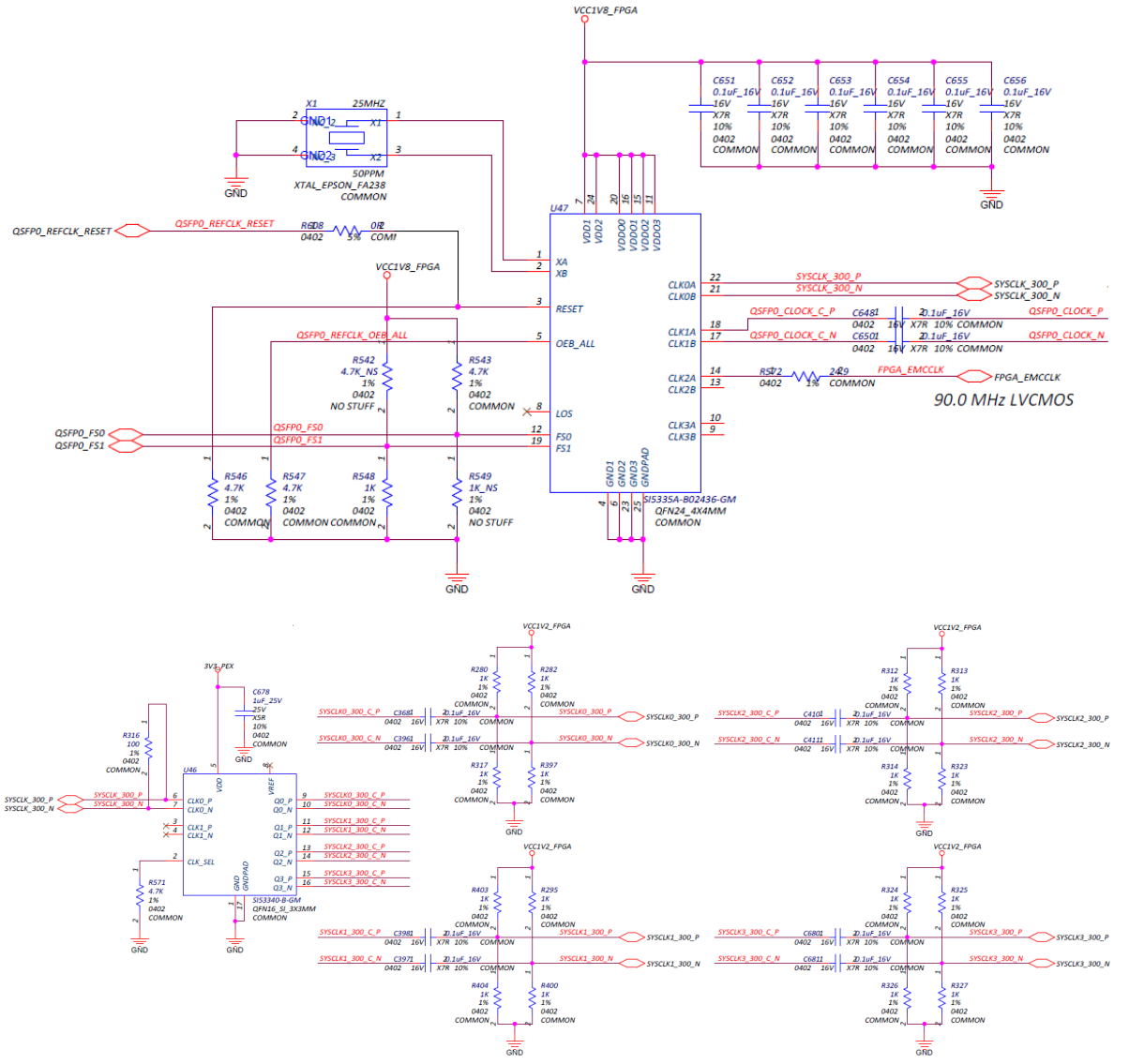


Figure 3-2: **KCU1500 System, QSFP0, and EMCCLK Clock Circuit**

QSFP1 Clock

[Figure 2-1, callout 9]

The QSFP1 clock source is a Silicon Labs SI5335A quad clock generator/buffer (U48).

- Clock generator: Silicon Labs SI5335A-B06201-GM (CLK0A 300 MHz)
  - Frequency plan: FS1, FS0=01
    - Input type: crystal, input frequency 25 MHz
    - Device operating mode: clock generator loop bandwidth 1.6 MHz
    - CLK0A/0B: 300 MHz 1.8V LVDS
    - CLK1A/1B: 156.25 MHz 1.8V LVDS
    - CLK2A/2B: 90 MHz 1.8V CMOS (output on A only)
    - CLK3A/3B: 33.333 MHz 1.8V CMOS (output on A only)
- Low phase jitter of 0.7pS RMS

One output of the SI5335A U48 is used:

- CLK0A/B are not used.
- CLK1A/B

  The QSFP1_CLOCK_P/N clock is an AC coupled LVDS 156.25 MHz clock wired to QSFP1 interface MGTH bank 128 MGTREFCLK1P/N input pins AN36 and AN37.
- CLK2A is not used.
- CLK3A is not used.

The QSFP1 clock circuit is shown in Figure 3-3.

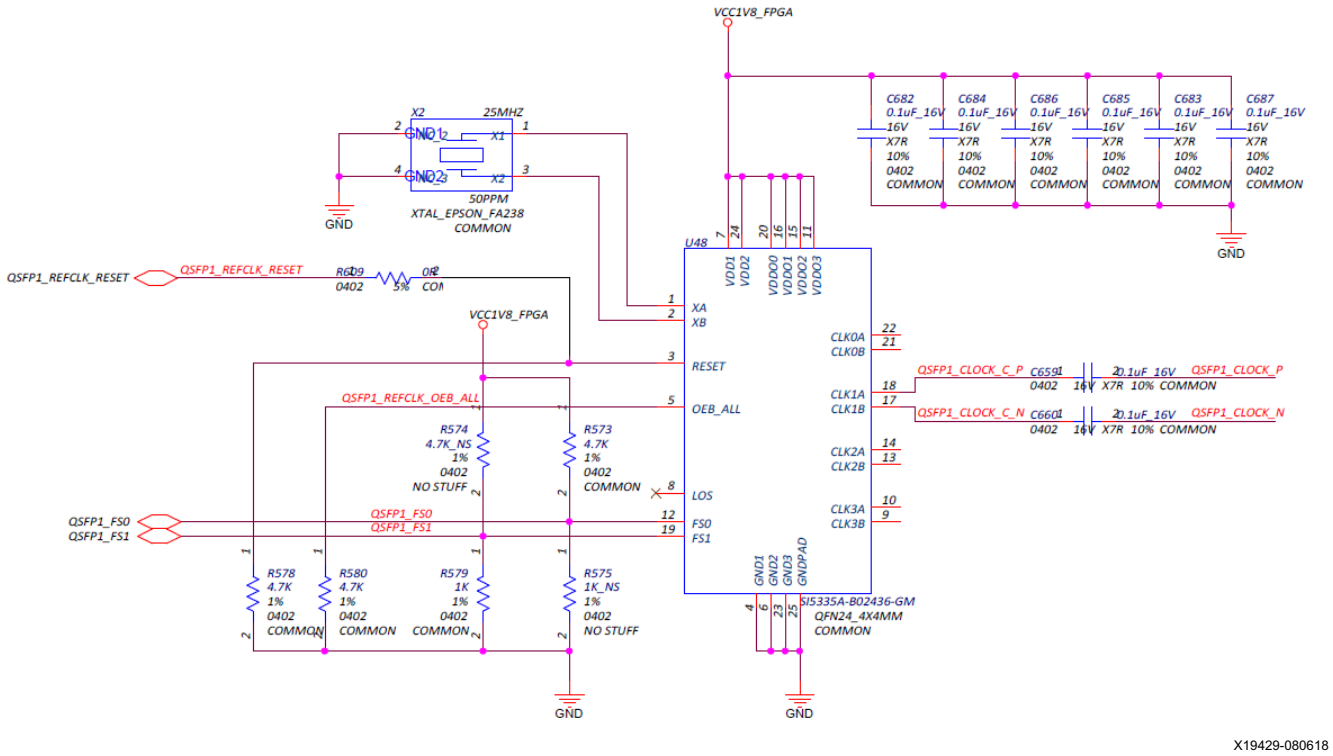


Figure 3-3: **QSFP1 Clock Circuit**

Programmable MGT and User Clock

[Figure 2-1, callout 10]

The KCU1500 board has a SI570 programmable low-jitter 3.3V LVDS differential oscillator (U40) connected to a SI53340 (U41) 1-to-4 LVDS clock buffer.

On power-up, the SI570 user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the KCU1500 board resets this clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz–810 MHz)
- Frequency jitter: 50 ppm
- 3.3V LVDS differential output
- Default frequency 156.250 MHz

Three of the SI53340 (U41) 1-to-4 LVDS clock buffer outputs are used:

- Q0_P/N

  USER_SI570_CLOCK_P/N are wired to QSFP0/1 control I/O bank 84 GC input pins. The I2C_MAIN_SDA/SCL bus is also wired to bank 84.

- Q1_P/N are not used.
- Q2_P/N

  MGT_SI570_CLOCK0_P/N are AC coupled to MGTH bank 127.

- Q3_P/N

  MGT_SI570_CLOCK1_P/N are AC coupled to MGTH bank 128.

The QSFP1 clock circuit is shown in Figure 3-4.

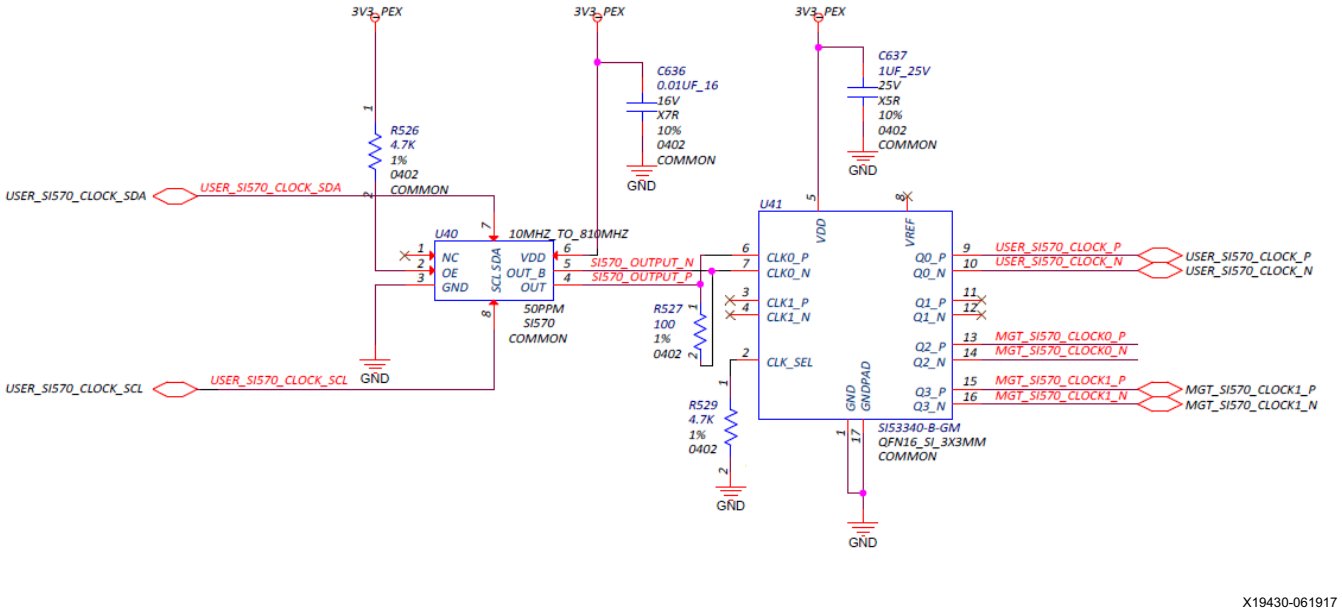


Figure 3-4: **SI570 Clock Circuit**

GTH Transceivers

[Figure 2-1, callout 1]

The KCU1500 board provides access to 24 of the 64 GTH transceivers:

- Four GTH transceivers (bank 127) are wired to QSFP28 connector QSFP0 J28
- Four GTH transceivers (bank 128) are wired to QSFP28 connector QSFP1 J30

Sixteen GTH transceivers are wired to the PCIe edge connector PEX signals:

- Four GTH transceivers (bank 224) are wired to PCIe edge connector CN1 lanes 7:4
- Four GTH transceivers (bank 225) are wired to PCIe edge connector CN1 lanes 3:0
- Four GTH transceivers (bank 226) are wired to PCIe edge connector CN1 lanes 15:12
- Four GTH transceivers (bank 227) are wired to PCIe edge connector CN1 lanes 11:8

The GTH transceivers in the XCKU115 device are grouped into four channels or quads. The reference clock for a quad can be sourced from the quad above or the quad below the GTH quad of interest. The six GTH quads used on the KCU1500 board have the connectivity listed here (also see Figure 3-5):

Quad 127:

- MGTREFCLK0 – MGT_SI570_CLOCK0_C_P/N
- MGTREFCLK1 – QSFP0_CLOCK_P/N
- Contains four GTH transceivers allocated to QSFP0 TX/RX lanes 1–4

Quad 128:

- MGTREFCLK0 – MGT_SI570_CLOCK1_C_P/N
- MGTREFCLK1 – QSFP1_CLOCK_P/N
- Contains four GTH transceivers allocated to QSFP1 TX/RX lanes 1–4

Quad 224:

- MGTREFCLK0 – not connected
- MGTREFCLK1 – not connected
- Contains four GTH transceivers allocated to PCIe lanes 7–4

Quad 225:

- MGTREFCLK0 – PEX_REFCLK_225_P/N buffered PCIe edge connector clock
- MGTREFCLK1 – not connected
- Contains four GTH transceivers allocated to PCIe lanes 3–0

Quad 226:

- MGTREFCLK0 – PEX_REFCLK_226_P/N buffered PCIe edge connector clock
- MGTREFCLK1 – not connected
- Contains four GTH transceivers allocated to PCIe lanes 15–12

Quad 227:

- MGTREFCLK0 – not connected
- MGTREFCLK1 – not connected
- Contains four GTH transceivers allocated to PCIe lanes 11–8

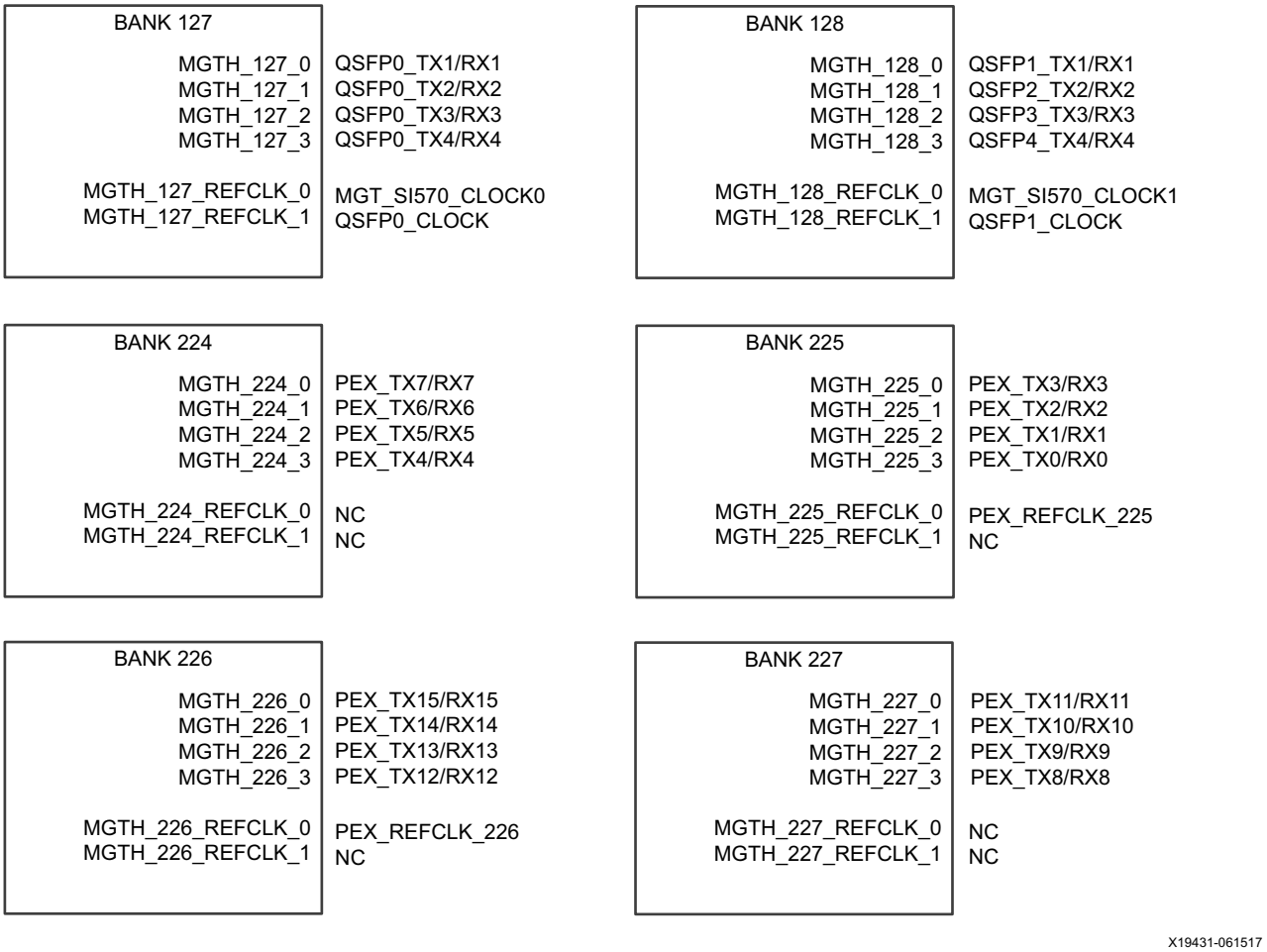


Figure 3-5: **GTH Bank Assignments**

PCI Express Endpoint Connectivity

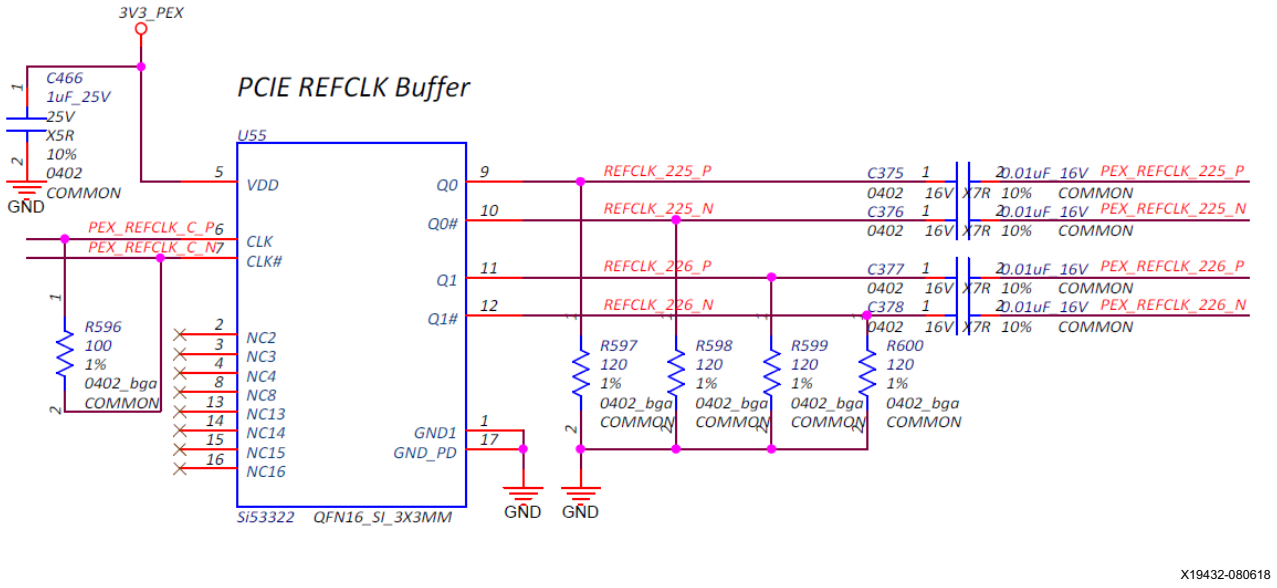
[Figure 2-1, PCIe Edge Connector]

The 16-lane PCI Express® edge connector CN1 performs data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications, and 8.0 GT/s for Gen3 applications. The PCIe transmit and receive signal data paths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair.

The XCKU115-2FLVB2104E device (–2 speed grade) included with the KCU1500 board supports up to Gen3 x16 bifurcated into two Gen3 x8 channels.

The PCIe clock is input from the CN1 edge connector and AC coupled to a 1-to-2 SI53322 clock buffer. The clock buffer outputs are AC coupled to FPGA U1 MGTREFCLK0 pins of Quad 225 and 226 to support two x8 bifurcated channels (also see Figure 3-5).

The PCI Express clock circuit is shown in Figure 3-6.



X19432-080618

Figure 3-6: **PCI Express Clock Buffer**

28 Gb/s QSFP+ Module Connector

[Figure 2-1, callout 11, 12]

The KCU1500 board hosts dual quad (4-channel) small form-factor pluggable (28 Gb/s QSFP+) connectors (J28, J30) that accept 28 Gb/s QSFP+ optical modules. Each connector is housed within a single 28 Gb/s QSFP+ cage assembly. The QSFP0 RX/TX lanes are wired to GTH bank/quad 127, and the QSFP1 RX/TX lanes are wired to GTH bank/quad 128. Figure 3-7 shows the 28 Gb/s QSFP+ module connector circuitry typical to each connector.

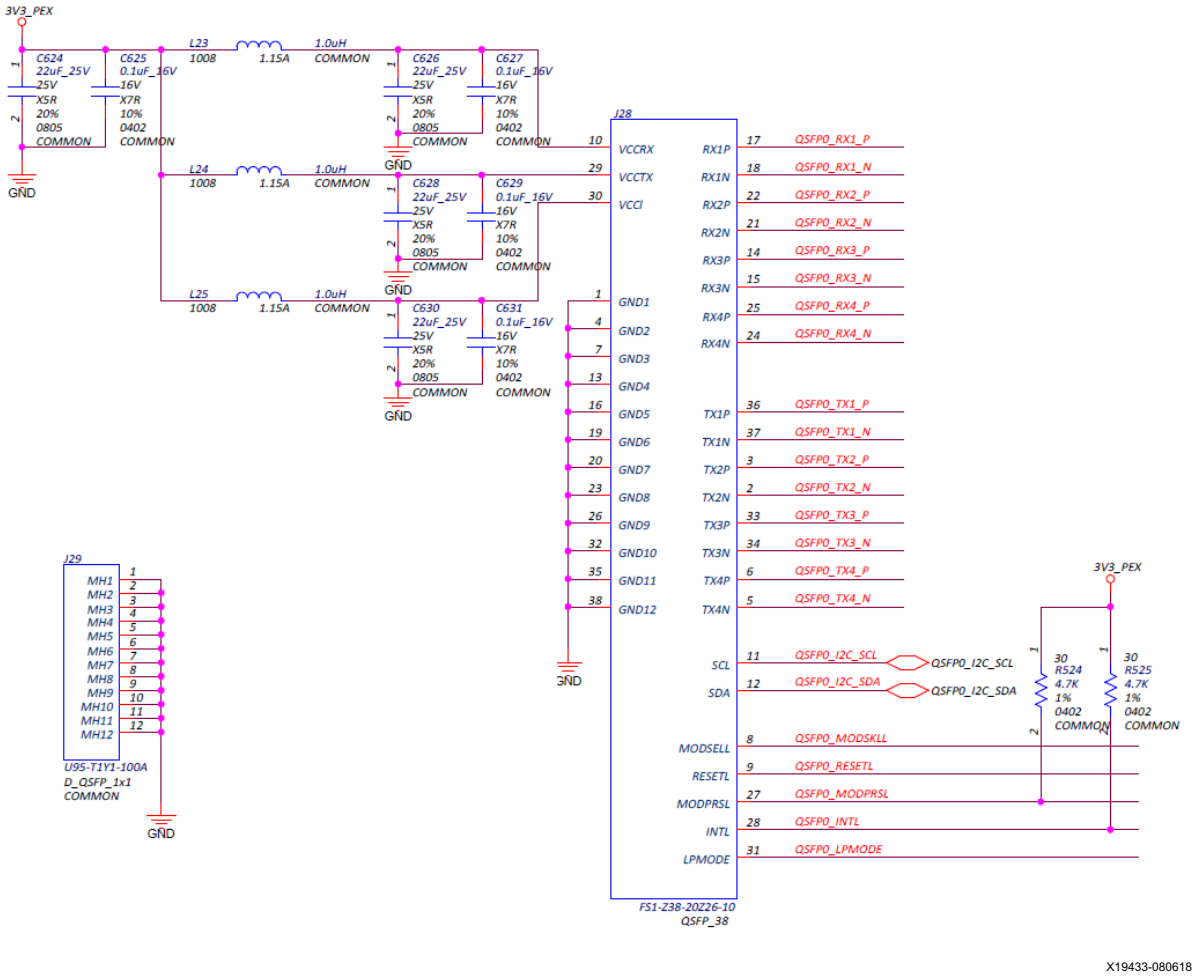


Figure 3-7: **28 Gb/s QSFP+ Module Connector**

The QSFP+ connectors J28 and J30 I2C SCL/SDA are accessible through the I2C switch U44 IIC_MAIN_SCL/SDA bus. See I2C Bus.

The QSFP+ connectors J28 and J30 I2C control signals are level-shifted by U39 and U43, respectively, and are connected to FPGA U1 bank 84.

For additional information about the quad small form-factor pluggable (28 Gb/s QSFP+) module, see the SFF-8663 specification for the 28 Gb/s QSFP+ at the SFF-8663 specification website [Ref 13].

I2C Bus

The KCU1500 board implements a single I2C bus (IIC_MAIN_SCL/SDA_LS), wired through level-shifter U45 and then routed to a 1-to-8 channel I2C TI PCA9548 bus switch (U44). The bus switch can operate at speeds up to 400 kHz.

The KCU1500 board I2C bus topology is shown in Figure 3-8.

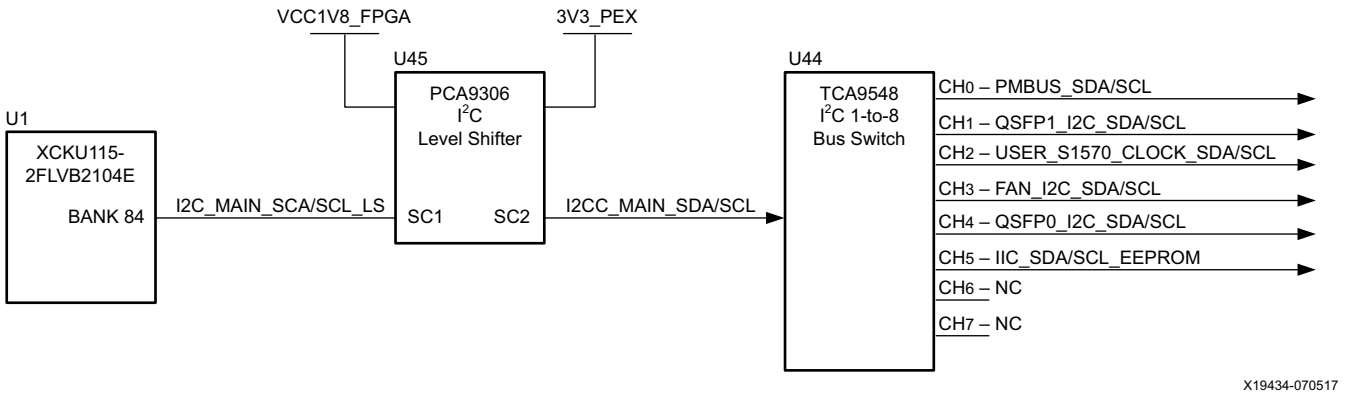


Figure 3-8: **I2C Bus Topology**

User applications that communicate with devices on one of the downstream I2C buses must first set up a path to the desired target bus through the U44 bus switch at I2C address 0x74 (0b1110100). Table 3-3 lists the I2C address of the TCA9548 U44 bus switch target devices.

Table 3-3: **I2C Bus Addresses**

I2C Bus	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
TCA9548 8-channel bus switch	N/A	0b1110100	0x74	U44 TCA9548
PMBUS_SDA/SCL	0		0x0A, 0x12, 0x14, 0x72, 0x73	MAX15301, MAX20751
QSFP1_I2C_SDA/SCL	1	0b1010000	0x50	J30 QSFP1
USER_SI570_CLOCK_SDA/SCL	2	0b1011101	0x5D	U32 SI570
FAN_I2C_SDA/SCL	3	0b1001100	0x4C	U53 LM96063
QSFP0_I2C_SDA/SCL	4	0b1010000	0x50	J28 QSFP0
EEPROM_IIC_SDA/SCL	5	0b1010000	0x50	U119 M24C08
Not used	6	N/A	N/A	N/A
Not used	7	N/A	N/A	N/A

Status and User LEDs

Table 3-4 defines KCU1500 board status and user LEDs.

Table 3-4: **Status and User LEDs**

Reference Designator	Description
DS1	USER_LED_0
DS2	USER_LED_1
DS3	USER_LED_2
DS4	USER_LED_3
DS5	USER_LED_4
DS6	USER_LED_5
DS7	USER_LED_6
DS8	USER_LED_7
DS9	12V POWER ON
DS10	MGTAVCC_PGOOD
DS11	MGTAVTT_PGOOD
DS12	DONE
DS13	INIT_B LOW
DS14	INIT_B HIGH
DS15	DDR4 POWER GOOD
DS17	SYS_2V5 ON
DS18	DDR4 C1 VTT ON
DS20	SYS_5V0 ON
DS21	DDR4 C3 VTT ON
DS22	FPGA CORE POWER GOOD
DS23	DDR4 C0 VTT ON
DS24	DDR4 C2 VTT ON

User I/O

[Figure 2-1, callouts 15, 13]

The KCU1500 board provides these user and general purpose I/O capabilities:

- Eight active-high user LEDs
  - USER_LED_[0:7]: DS1, DS2, DS3, DS4, DS5, DS6, DS7, DS8
- One active-low user pushbutton (assigned as CPU_RESET) (callout 15)
  - CPU_RESET PB: SW2
- 4-position active-low user DIP switch (callout 13)
  - USER_SW_DP[0:3]: SW4

KCU1500 Board Power System

The KCU1500 hosts a Maxim PMBus based power system. Each individual Maxim MAX15301 and MAX20751 voltage regulator has a PMBus interface. Figure 3-9 shows the KCU1500 power system block diagram.

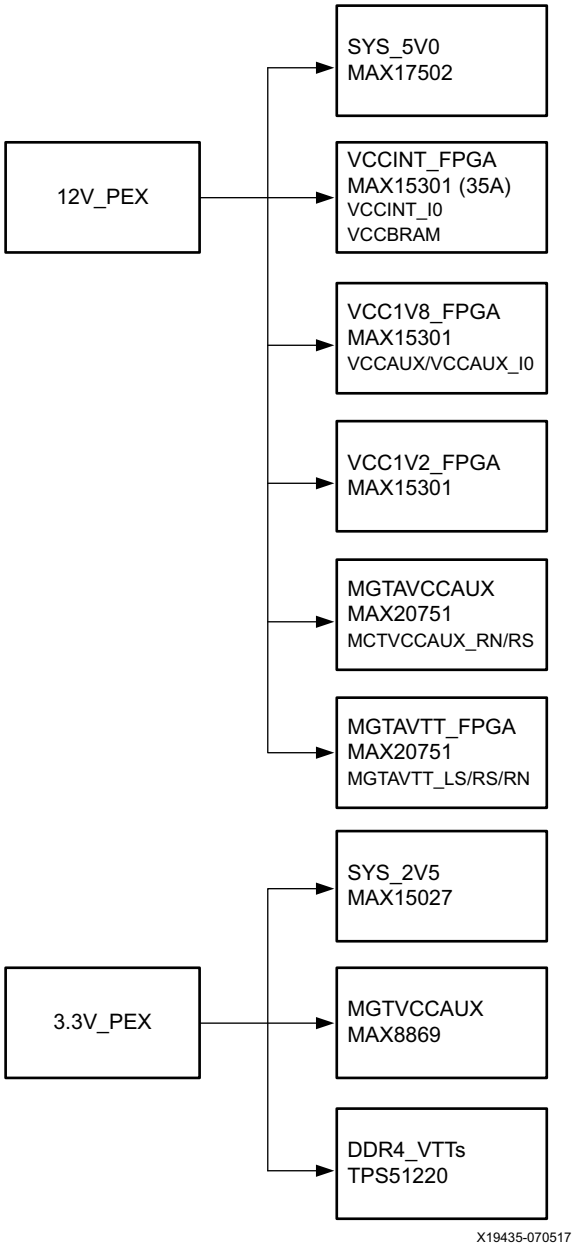


Figure 3-9: **Power System Block Diagram**

The KCU1500 board uses power regulators and PMBus compliant point of load (POL) controllers from Maxim Integrated Circuits to supply the core and auxiliary voltages listed in Table 3-5.

Table 3-5: **Onboard Power System Devices**

Rail Name	Power System Regulators					U18 Current Sense SYSMON Multiplexer Port		Schematic Page Number
	Ref. Des.	Device Type	Vout (V)	Max. I (A)	Addr.	Bin. Addr.	Port	
VCCINT_FPGA	U20	MAX15301	0.95	30	0x0A	NA	NA	22
VCC1V8_FPGA	U21	MAX15301	1.80	10	0x14	001	S2	23
VCC1V2_FPGA	U25	MAX15301	1.20	10	0x12	100	S5	24
MGTAVCC_FPGA	U28	MAX20751	0.95	30	0x72	NA	NA	25
MGTAVTT_FPGA	U37	MAX20751	1.20	30	0x73	111	S8	27
Non-PMBus Regulators								
SYS_5V0	U34	MAX17502	5.00	1	NA	NA	NA	26
SYS_2V5	U27	MAX15027	2.50	1	NA	NA	NA	26
MGTVCCAUX	U30	MAX8869E	1.81	1	NA	NA	NA	26
DDR4_C0_VTT	U117	TPS51200	0.60	3	NA	NA	NA	26
DDR4_C1_VTT	U32	TPS51200	0.60	3	NA	NA	NA	26
DDR4_C2_VTT	U118	TPS51200	0.60	3	NA	NA	NA	26
DDR4_C3_VTT	U35	TPS51200	0.60	3	NA	NA	NA	26

Documentation describing PMBus programming for the Maxim InTune™ power controllers is available at the Maxim website [Ref 16]. The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 4].

Monitoring Voltage and Current

Voltage and current monitoring and control are available for the Maxim power system controllers via the Maxim PowerTool software graphical user interface. The onboard Maxim PMBus MAX15301, MAX15303, and MAX20751 power controllers listed in Table 3-5 are accessed through the 2x4 PMBus connector J11, which is provided for use with the Maxim PowerTool USB cable (Maxim part number MAXPOWERTOOL001#). This cable can be ordered from the Maxim Integrated website [Ref 16]. The associated Maxim PowerTool GUI can be downloaded from the Maxim website. This is the simplest and most convenient way to monitor the voltage and current values for the PMBus power rails listed in Table 3-5.

V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} rail voltages can also be displayed via the SYSMON internal voltage measurement capability.

SYSMON Power System Measurement

The ZCU1500 board SYSMON interface includes additional power system voltage and current measuring capability. The MGTAVCC_FPGA and MGTAVTT_FPGA voltages sensed at the FPGA power pins are each scaled through a resistor attenuator network and the resulting scaled voltage is connected to XCKU115 FPAG U1 bank 65 SYSMON channel AD0 and AD8, respectively.

VCC1V8_FPGA, VCC1V2_FPGA, and MGTAVTT_FPGA rail load current measurements are available through an external Analog Devices ADG707BRU multiplexer U18. Each rail has a TI INA333 operational amplifier strapped across its series current sense resistor Kelvin terminals. This operational amplifier has its gain adjusted to give approximately 1V at the expected full scale current value for the rail.

Figure 3-10 shows a simplified SYSMON external multiplexer diagram.

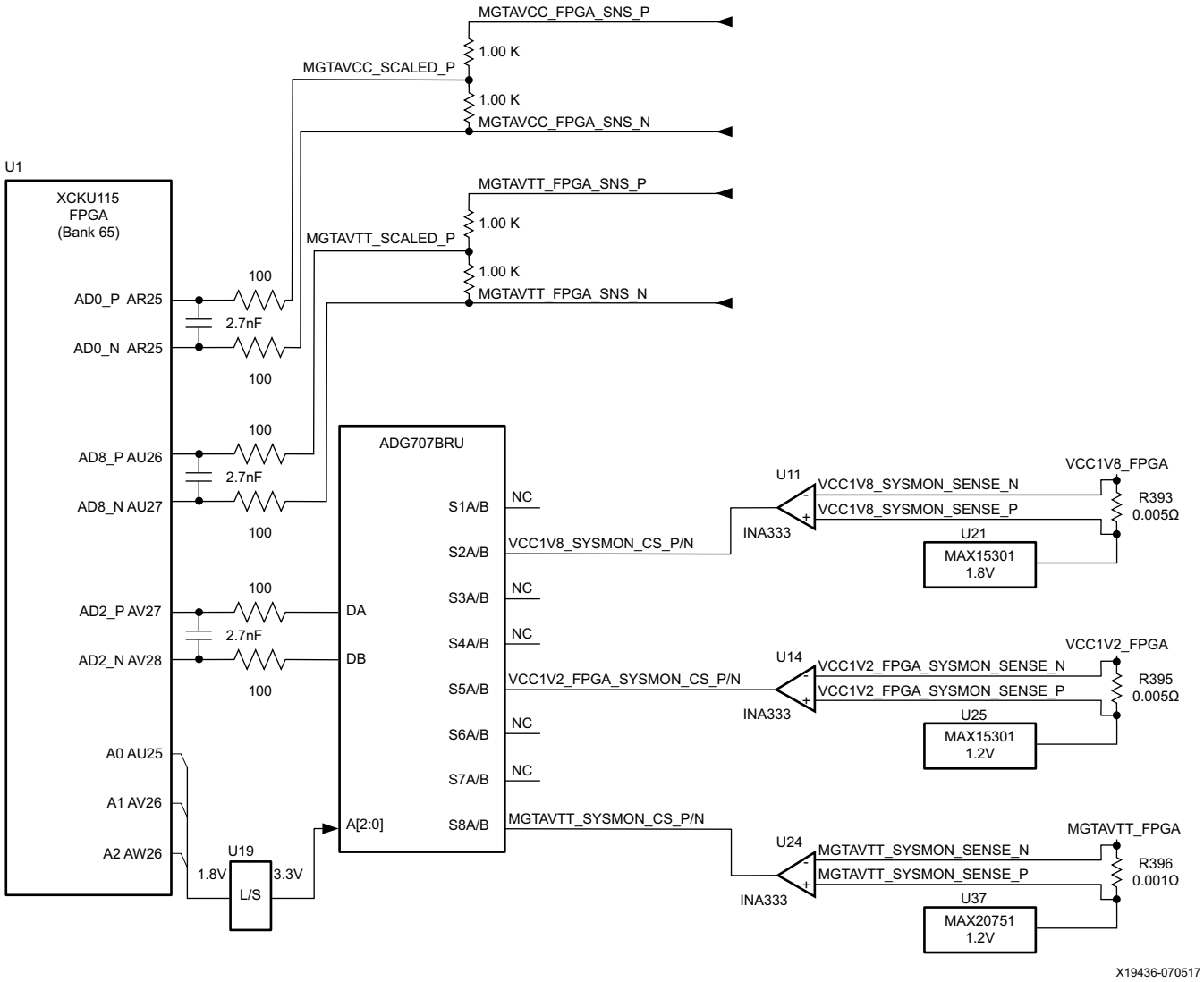


Figure 3-10: **Simplified Power Measurement Diagram**

Cooling Fan Connector

The KCU1500 cooling fan connector is shown in Figure 2-1, located between callouts 13 and 15.

The KCU1500 uses a TI LM96063 (U53) fan controller, which autonomously controls the fan speed by controlling the pulse width modulation (PWM) signal to the fan based on the die temperature via the FPGA's DXP and DXN pins. The fan rotates slowly (acoustically quiet) when the FPGA is cool and rotates faster as the FPGA heats up (acoustically noisy).

The fan speed versus the FPGA die temperature algorithm along with the over temperature (OT) set point and fan failure alarm mechanisms are defined by user values programmed into the LM96063 device register set. The LM96063 OT TCRIT# output is wired to a MAX16052 (U52) supervisory device that turns off the KCU1500 power system voltage regulators if an OT condition is detected.

See the LM96063 [Ref 15] data sheet for more information on the device circuit implementation on this board.

Board Installation

Introduction

This appendix provides the information required to install, program, debug, and deploy a Xilinx® accelerator board to execute applications created with the SDx® environment. The SDx environment executes in hardware using one of the FPGA boards listed in the application.

Installing a Board

The KCU1500 card is a high-performance reconfigurable computing card for data center applications and includes these features:

- XCKU1500-2FLVB2104E FPGA
- Four 4 GB DDR4 banks (16 GB total)

The following sections describe how to install a board.

Step 1: Set Up the Card and Computer

1. Make sure the host computer is completely turned off.
2. Install the FPGA board in an open PCIe® slot on the host computer.
3. Turn on the host computer.

   Note: Follow the host computer manufacturer recommendations to ensure proper mounting and adequate cooling.

Step 2: Prepare Board Installation Files

The SDx environment provides the `xbinst` utility, which generates firmware and driver files for the target board plugged into the deployment computer.

1. Run the following commands to prepare files for the target board installation.

   See the *SDx Command and Utility Reference Guide* (UG1279) [Ref 6] for more details on the `xbinst` utility. Depending on the target location, some commands must be run with `root` or `sudo` privilege. Otherwise, access permissions must be changed to enable read access for all users on that system.

2. Use the following commands to create the deployment area inside `/opt/dsa/`:

   ```
   $ mkdir /opt/dsa
   $ mkdir /opt/dsa/xilinx_vcu1525_dynamic_5_1
   $ cd /opt/dsa/xilinx_vcu1525_dynamic_5_1
   ```

   Note: To install and deploy the KCU1500 files, use `xilinx_kcu1500_dynamic_5_0` in step 2 and 3.

3. Execute `xbinst` to install the files needed for the deployment machine. Output similar to the following is displayed:

   ```
   $ xbinst --platform xilinx_vcu1525_dynamic_5_1 -d .

   ****** xbinst v2018.2 (64-bit)
     **** SW Build 2254440 on Sun Jun 10 18:05:35 MDT 2018
       ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

   Attempting to get a license: ap_opencl
   Feature available: ap_opencl
   INFO: [XBINST 60-895]   Target platform:
   /opt/Xilinx/SDx/2018.2/platforms/xilinx_vcu1525_dynamic_5_1/xilinx_vcu1525_dynamic_
   5_1.xpfm
   INFO: [XBINST 60-267] Packaging for PCIe...
   INFO: [XBINST 60-1032] Extracting DSA to
   ./.Xil/xbinst-1273/xilinx_vcu1525_dynamic_5_1
   INFO: Adding section [FIRMWARE (3)] using: 'mgmt' (23192 Bytes)
   INFO: Adding section [SCHED_FIRMWARE (5)] using: 'sched' (9748 Bytes)
   Successfully completed 'xclbincat'
   INFO: [XBINST 60-268] Packaging for PCIe...COMPLETE
   INFO: [XBINST 60-667] xbinst has successfully created a board installation directory
   at /opt/dsa/xilinx_vcu1525_dynamic_5_1.
   ```

   The files are installed in this location:
   `/opt/dsa/xilinx_vcu1525_dynamic_5_1/xbinst`:

   Make a note of the deployment location area because it is required at a later stage.

   This section refers to this location as the `<xbinst-area>` or as the deployment directory.

4. Install the drivers as described in Step 3: Install Board Drivers.

Step 3: Install Board Drivers

The drivers for the card must be installed before it can be used to run SDx applications.

1. Go to the board deployment directory generated previously and run the installation script:

   ```
   $ cd <xbinst-area>/xbinst
   $ sudo ./install.sh -f yes
   ```

   The script performs the following:

   - Compiles and installs the Linux kernel device drivers. The force option (`-f yes`) ensures that the previous drivers are removed first.
   - Installs the firmware to the Linux firmware area.
   - Installs the Xilinx installable client driver (ICD) to `/etc/OpenCL/vendors`. The OpenCL® ICD allows multiple implementations of OpenCL to co-exist on the same system. It allows applications to choose a platform from the list of installed platforms and dispatches OpenCL API calls to the underlying implementation.
   - Generates a `setup.sh` (Bash shell) or `setup.csh` (for `csh/tcsh` shells) to set up the run-time environment. To run applications, the setup script must be sourced before running any application on the target FPGA card, as follows:

     ```
     $ source <xbinst-area>/setup.sh
     ```

   Note: To generate only the setup scripts, use `./install.sh -k no`. The install script does not try to install the drivers so this can be run without `sudo` privileges.

   This command must be run if the `xbinst` installation area is moved to another directory location because the setup scripts generated export environment variables that use absolute paths. Re-running the command ensures the scripts are updated accordingly.

Step 4: Program the Base Platform

This section describes how to program the board using the `xbsak flash` command directly from the deployment computer and its Linux OS. The command line prompt is used to program the configuration memory (flash memory device) on the FPGA board with specified configuration files from which the FPGA can boot.

1. Before programming the board, check which device support archive (DSA) is currently programmed onto the configuration memory of the board as follows:

   ```
   $ sudo <xbinst-area>/runtime/bin/xbsak flash scan
   ```

   or equivalently:

   ```
   $ sudo 'which xbsak flash scan';
   ```

Typical output is:

```
$ sudo `which xbsak` flash scan
XBFLASH -- Xilinx Board Flash Utility
SCAN found the following devices:
[0]
    DBDF:  0000:03:00.1
    DSA:   xilinx_vcu1525_dynamic_5_1
    Flash: SPI
```

In this example, the board does not need to be re-flashed because it is already up-to-date.

All of the Xilinx boards are already programmed and are visible with the following command, which confirms that the board is programmable using the `xbsak` flash because it is visible as a PCI device:

```
$ lspci -d 10ee:
03:00.0 Serial controller: Xilinx Corporation Device 6a90
03:00.1 Serial controller: Xilinx Corporation Device 6a8f
```

2. Source the `setup.{sh,csh}` from the `xbinst` area to use `xbsak` flash:

```
$ source <xbinst-area>/setup.{sh|csh}
```

3. Find the necessary MCS files:

```
$ find <xbinst-area> -name '*.mcs'
```

   - For a Kintex UltraScale KCU1500 board, this command returns two MCS files—the primary and the secondary MCS files that are needed for the `xbsak` flash command:

```
$ find -name '*.mcs'
./firmware/xilinx_kcu1500_dynamic_5_0_primary.mcs
./firmware/xilinx_kcu1500_dynamic_5_0_secondary.mcs
$ xbsak flash -m <primary mcs file> -n <secondary mcs file>
```

   - For a Virtex UltraScale+-based VCU1525 board, this command returns one MCS file needed for the `xbsak` flash command:

```
$ find -name '*.mcs
./firmware/xilinx_vcu1525_dynamic_5_1.mcs
$ xbsak flash -m <mcs file>
```

Step 5: Verify Successful Board Installation

During execution of `xbinst`, a simple, prebuilt executable and the associated `xclbin` is included in the `<xbinst-area>/test` directory. This executable checks that the drivers and the DSA are correctly installed and that the setup is operating as expected. These steps are required to perform the installation validation:

1. Source the `setup.sh` (Bash) or `setup.csh` (`csh/tcsh`):

   ```
   $ source <xbinst-area>/setup.[sh|csh]
   ```

2. Change to the test directory and run the validation executable.

   If the test directory is not write-enabled, it might be necessary to run the executable from a different directory with an absolute path to the `verify.exe`.

3. Execute the following:

   ```
   $ cd /tmp/
   $ <xbinst-area>/test/verify.exe <xbinst-area>/test/verify.xclbin
   ```

   The system is correctly functioning if the output looks similar to the following:

   ```
   CL_PLATFORM_VENDOR Xilinx
   CL_PLATFORM_NAME Xilinx
   Get 1 devices
   Using 1th device
   loading <..path to..>/verify.xclbin

   RESULT:
   Hello World
   ```

Debugging the Installation

This section covers debugging and troubleshooting. For software support and related software debug techniques, see the *SDx Command and Utility Reference Guide* (UG1279) [Ref 6]. For more information, see Answer Record 43745.

This section lists the commands used to query and investigate different scenarios such as:

- A sanity check needs to be performed on a new board.
- The host application is abruptly interrupted and the board or the driver is in a stale or unknown mode.
- The deployment machine needs to be rebooted to set everything back to a working state.

The commands in this section are used for debugging. The first two commands are SDAccel board utility tools that are further detailed in the *SDx Command and Utility Reference Guide* (UG1279) [Ref 6]. The other commands are Linux command line tools: `lspci` and `dmesg`.

The utilities for the board installation tool are:

```
xbsak xbinst
```

Two common scenarios that require debugging are:

- A new board is not showing as an SDAccel device using the `lspci` command, which indicates that the board is probably not programmed. The board's firmware needs to be installed as listed in the installation directory. After the firmware is installed, a sanity check can be performed before using the application.
- A working board is not behaving properly after an accelerator function design was running on the board. In this case, an OS or driver issue needs to be resolved.

SDx Debug Command Options

The `xbsak scan` scans for devices and associated drivers for the host machine. A normal output is as follows:

```
$ xbsak scan
Linux:4.4.0-116-generic:#140-Ubuntu SMP Mon Feb 12 21:23:04 UTC 2018:x86_64
Distribution: Ubuntu 16.04.3 LTS
GLIBC: 2.23
---
XILINX_OPENCL="/opt/dsa/<board_name>/xbinst"
LD_LIBRARY_PATH="/opt/dsa/<board_name>/xbinst/runtime/lib/x86_64:"
---
[0]mgmt:0x6a8f:0x4351:[xclmgmt:2017.4.4:0]
[0]user:0x6a90:0x4351:[xocl:2017.4.5:129]
Determining if Output is Showing an Error
```

When the `xbsak scan` command is used, results are as follows:

```
[0]mgmt:0x6a8f:0x4351:[???:???:???]
[0]user:0x6a90:0x4351:[xocl:2017.4.5:129]
```

Such output indicates that the management driver, `xclmgmt` is not loaded; it could either have been unloaded using the Linux command, `$ sudo rmmod xclmgmt`, or there was an error at the OS level.

To fix an unloaded management driver, use this command:

```
$ sudo modprobe xclmgmt
```

Otherwise, if the `xbsak scan` command is used, the results are as follows:

```
[0]mgmt:0x6a8f:0x4351:[xclmgmt:2017.4.4:0]
[0]user:0x6a90:0x4351:[???:???:???]
```

This indicates that the user function driver `xocl` is not loaded; it could have either have been unloaded with the `xbsak list $ sudo rmmod xocl` command or there was an error at the OS level.

To fix this issue, use this command:

```
$ sudo modprobe xocl
```

dmatest Command

Use the `xbsak dmatest` command to confirm that there are no issues accessing the DDR device memory from the host, or to ensure that the path from the host to PCIe to device DDR and corresponding reverse path DDR to device to PCIe to host are still working and functioning as expected.

The `xbsak dmatest` command also provides a bandwidth test/benchmark and confirmation that the board and host computer are operating at the optimum speed. The maximum performance is achieved with Gen3 by 16 lanes and write speeds of around 7 GB/s and read speeds of around 11 GB/s.

Example Output using VCU1525

A typical output for VCU1525 is:

```
$ xbsak dmatest
Linux:3.10.0-327.el7.x86_64:#1 SMP Thu Nov 19 22:10:57 UTC 2015:x86_64
Distribution: CentOS Linux release 7.2.1511 (Core)
GLIBC: 2.17
---
XILINX_OPENCL="/opt/dsa/<board_name>/xbinst"
LD_LIBRARY_PATH="/opt/dsa/<board_name>/xbinst/runtime/lib/x86_64:"
---
INFO: Found 1 device(s)
Total DDR size: 65536 MB
Reporting from mem_topology:
Data Validity & DMA Test on DDR[0]
INFO: Host -> PCIe -> MIG write bandwidth = 7284.55 MB/s
INFO: Host <- PCIe <- MIG read bandwidth = 11192 MB/s
Data Validity & DMA Test on DDR[1]
INFO: Host -> PCIe -> MIG write bandwidth = 7514.58 MB/s
INFO: Host <- PCIe <- MIG read bandwidth = 11523.6 MB/s
Data Validity & DMA Test on DDR[2]
INFO: Host -> PCIe -> MIG write bandwidth = 7539.88 MB/s
INFO: Host <- PCIe <- MIG read bandwidth = 11238.2 MB/s
Data Validity & DMA Test on DDR[3]
INFO: Host -> PCIe -> MIG write bandwidth = 7840.42 MB/s
INFO: Host <- PCIe <- MIG read bandwidth = 11264.1 MB/s
INFO: xbsak dmatest successful.
```

In the previous output, the memory topology of the programmed design is used by the four memory banks on the card. Other designs, such as the verify design only, use one DDR memory bank so the output would show only one channel.

Use the `xbsak` query command to check the general status of the board. A typical output is:

```
---
INFO: Found 1 device(s)
DSA name:       xilinx_vcu1525_dynamic_5_1
Vendor:         10ee
Device:         6a8f
SDevice:        4350
SVendor:        10ee
DDR size:       0x4000000 KB
DDR count:      4
OnChip Temp:    35 C
Power(Beta):    **Unable to estimate power**
OCL Frequency:
        0:      300 MHz
        1:      500 MHz
PCIe:           GEN3 x 16
DMA bi-directional threads:    2
MIG Calibrated: true

Device DDR Usage:
  Bank[0].mem:  0x0 KB
  Bank[0].bo:   0
  Bank[1].mem:  0x0 KB
  Bank[1].bo:   0
  Bank[2].mem:  0x0 KB
  Bank[2].bo:   0
  Bank[3].mem:  0x0 KB
  Bank[3].bo:   0

Total DMA Transfer Metrics:
  Chan[0].h2c:  0x2d1ea5a KB
  Chan[0].c2h:  0x2c3383b KB
  Chan[1].h2c:  0x24a7a51 KB
  Chan[1].c2h:  0x232b000 KB

Firewall Last Error Status:
        0:      0x0 (GOOD)
        1:      0x0 (GOOD)
        2:      0x0 (GOOD)

Xclbin ID:  0x5ade7395

Mem Topology:
     Bank       Type       Base Address     Size (KB)
  [0] bank0     MEM_DDR4            0x0     0x1000000
  [1] bank2     MEM_DDR4    0x800000000     0x1000000
  [2] bank3     MEM_DDR4    0xc00000000     0x1000000
  [3] bank1     MEM_DDR4    0x400000000     0x1000000

Compute Unit Status:
  CU[0]: sdx_kernel_wizard_0@0x1800000 (IDLE)
INFO: xbsak query successful.
```

Failure to Create a Compute Program

To check potential issues, use the `clCreateProgramWithBinary()` function. This function can identify issues that occur when programming the FPGA with the provided `xclbin` file. One scenario is that the program is not compatible with the currently programmed bitstream, which derived from the programmed firmware DSA on the configuration flash memory of the card.

There are several ways to determine if the DSA matches, but they all need to check the timestamp programmed into the bitstream of the programmed DSA against the `xclbin`, by checking the output of `dmesg`:

```
xclbin: TimeStamp:5a27f562 VBNV:
ROM: TimeStamp:5aace1cf VBNV:<board_name>
TimeStamp of ROM did not match Xclbin
```

If the `xbinst` installation area used to program the device configuration memory is accessible, the `dsa` bin in the `firmware` directory can be checked using the following command, which shows the timestamp programmed into the device configuration memory:

```
/opt/dsa/<board_name>/xbinst/firmware/10ee-6a90-4350-00000000M<####
###>.dsabin
```

If the `xclbin` file is accessible, use the `xclbinsplit` option to split the `xclbin` into several files as follows:

- On the deployment machine (after sourcing setup.sh|csh), type the following:

  ```
  $ $XILINX_OPENCL/runtime/bin/xclbinsplit verify.xclbin
  ```

- Alternatively, use the following command:

  ```
  $ xclbinsplit verify.xclbin
  ```

When the SDx tool is setup on the development machine, type the following:

```
$ $XILINX_SDX/runtime/bin/xclbinsplit verify.xclbin
```

This produces a set of files for which the `split-xclbin.xml` lists the timestamp of the DSA that was used to create it:

```
<platform vendor="xilinx" boardid="vcu1525" name="dynamic"
featureRomTime="#####">
```

The output is in decimal representation. To convert to a hexadecimal representation:

```
$ printf "%x\n" 1512568162
5a27f562
```

Also, to look directly into the DSA archive file for the same information:

```
$ unzip $XILINX_SDX/platforms/<board_name>/hw/<board_name>.dsa dsa.xml -d unzip_dsa
[...]  inflating: unzip_dsa/dsa.xml
$ grep -i time unzip_dsa/dsa.xml
< ... FeatureRomTimestamp="#####">
```

Useful Debug Operating System Commands

This section includes some typical outputs for a VCU1525 board when running debug commands. Only the relevant output relating to accelerator boards is included. Some numbers can change depending on the deployment machine.

- `lspci`: command on Unix-like operating systems that prints ("lists") detailed information about all buses and devices in the system. It is based on a common portable library, `libpci`, that provides access to the configuration space on a variety of operating systems. Use this command to check if the accelerator board is booted up correctly, is recognized as a device, and is enumerated. The `lspci` command lists the controller addresses as follows:

```
$ lspci
...
03:00.0 Serial controller: Xilinx Corporation Device 6a90
03:00.1 Serial controller: Xilinx Corporation Device 6a8f
...
```

Output lines for this command have been omitted for brevity here.

If using a board (as opposed to a board in a cloud environment), use the following command to query using only the `vendor_ID` (`10ee` for Xilinx):

```
$ lspci -d 10ee:
03:00.0 Serial controller: Xilinx Corporation Device 6a90
03:00.1 Serial controller: Xilinx Corporation Device 6a8f
```

Where:

- `-d` is the device.
- `10ee` is the ID.

A more verbose output can be generated as follows:

```
$ lspci -vv -d 10ee:
03:00.0 Serial controller: Xilinx Corporation Device 6a90 (prog-if 01 [16450])
  Subsystem: Xilinx Corporation Device 4351
  Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR-
FastB2B- DisINTx-
  Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
>SERR- <PERR- INTx-
  Latency: 0, Cache Line Size: 64 bytes
  Interrupt: pin A routed to IRQ 46
  Region 0: Memory at f6000000 (32-bit, non-prefetchable) [size=32M]
  Region 1: Memory at f8040000 (32-bit, non-prefetchable) [size=64K]
```

```
  Capabilities: <access denied>
  Kernel driver in use: xocl
  Kernel modules: xocl
03:00.1 Serial controller: Xilinx Corporation Device 6a8f (prog-if 01 [16450])
  Subsystem: Xilinx Corporation Device 4351
  Control: I/O+ Mem+ BusMaster- SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR-
FastB2B- DisINTx-
  Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
>SERR- <PERR- INTx-
  Region 0: Memory at f4000000 (32-bit, non-prefetchable) [size=32M]
  Region 2: Memory at f8020000 (32-bit, non-prefetchable) [size=128K]
  Region 4: Memory at f8000000 (32-bit, non-prefetchable) [size=128K]
  Capabilities: <access denied>
  Kernel driver in use: xclmgmt
  Kernel modules: xclmgmt

//Using the verbose option shows:
$ lspci -v
03:00.0 Serial controller: Xilinx Corporation Device 6a90 (prog-if 01 [16450])
  Subsystem: Xilinx Corporation Device 4351
  Flags: bus master, fast devsel, latency 0, IRQ 46
  Memory at f6000000 (32-bit, non-prefetchable) [size=32M]
  Memory at f8040000 (32-bit, non-prefetchable) [size=64K]
  Capabilities: <access denied>
  Kernel driver in use: xocl
  Kernel modules: xocl

03:00.1 Serial controller: Xilinx Corporation Device 6a8f (prog-if 01 [16450])
  Subsystem: Xilinx Corporation Device 4351
  Flags: fast devsel
  Memory at f4000000 (32-bit, non-prefetchable) [size=32M]
  Memory at f8020000 (32-bit, non-prefetchable) [size=128K]
  Memory at f8000000 (32-bit, non-prefetchable) [size=128K]
  Capabilities: <access denied>
  Kernel driver in use: xclmgmt
  Kernel modules: xclmgmt
```

When required, run the `lspci` command in super-user (`sudo`) mode to show the information hidden under the access-denied entries. The output is as follows:

```
$ sudo lspci -v
...
03:00.0 Serial controller: Xilinx Corporation Device 6a90 (prog-if 01 [16450])
  Subsystem: Xilinx Corporation Device 4351
  Flags: bus master, fast devsel, latency 0, IRQ 46
  Memory at f6000000 (32-bit, non-prefetchable) [size=32M]
  Memory at f8040000 (32-bit, non-prefetchable) [size=64K]
  Capabilities: [40] Power Management version 3
  Capabilities: [60] MSI-X: Enable+ Count=33 Masked-
  Capabilities: [70] Express Endpoint, MSI 00
  Capabilities: [100] Advanced Error Reporting
  Capabilities: [1c0] #19
  Capabilities: [350] Vendor Specific Information: ID=0001 Rev=1 Len=02c <?>
  Capabilities: [400] Access Control Services
  Kernel driver in use: xocl
  Kernel modules: xocl

03:00.1 Serial controller: Xilinx Corporation Device 6a8f (prog-if 01 [16450])
```

```
Subsystem: Xilinx Corporation Device 4351
Flags: fast devsel
Memory at f4000000 (32-bit, non-prefetchable) [size=32M]
Memory at f8020000 (32-bit, non-prefetchable) [size=128K]
Memory at f8000000 (32-bit, non-prefetchable) [size=128K]
Capabilities: [40] Power Management version 3
Capabilities: [70] Express Endpoint, MSI 00
Capabilities: [100] Advanced Error Reporting
Capabilities: [400] Access Control Services
Kernel driver in use: xclmgmt
Kernel modules: xclmgmt
```

- `dmesg`: use to view the messages from the drivers:

```
$ dmesg
```

Another `dmesg` option is `dmesg -T`. This option provides a timestamp that is human-readable instead of using the time in seconds since the machine has booted.

If the `dmesg` command returns too much information, use the following variation, which clears the buffer before the next use:

```
$ sudo dmesg -C
lsmod: Lets you check if driver modules are loaded in the OS, as follows:
lsmod | grep -E "^xocl|^xclmgmt"
The output would be similar to the following:
xocl     94208  0
xclmgmt  69632  0
```

The first column shows the `xocl` and `xclmgmt` that are driver modules.The second column is the size in memory of the drivers.The third column with the 0 indicates the drivers are currently not in use, also indicating that no application is running on the host and using or accessing the accelerator board.

Other OS Commands

To insert or remove drivers, use the `modprobe` and `rmmod` functions.

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Appendix B

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

KCU1500 Evaluation Kit — Master Answer Record (AR 69280)

For Technical Support, open a Support Service Request.

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the KCU1500 board and its documentation is available on the following websites.

KCU1500 Data Center Board

KCU1500 Data Center Board — Master Answer Record (AR 69280)

These Xilinx documents provide supplemental material useful with this guide:

1. *UltraScale Architecture Configuration User Guide* (UG570)
2. *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS892)
3. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
4. *UltraScale Architecture PCB Design User Guide* (UG583)
5. *Vivado Design Suite User Guide: Using Constraints* (UG903)
6. *SDx Command and Utility Reference Guide* (UG1279)
7. For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

The following websites provide supplemental material useful with this guide:

8. Xilinx, Inc: www.xilinx.com
   (XCKU115-2FLVB2104E)
9. Micron Technology: www.micron.com
   (MT40A512M16JY-083E:B, MT25QU512ABB8E12-0SIT)
10. Future Technology Devices International Ltd.: www.ftdichip.com
    (FT2232H)
11. Silicon Labs: www.silabs.com
    (Si5335A, Si570, Si53340, Si5322)
12. PCI Express® standard: www.pcisig.com/specifications
13. SFF-8663 specification: https://www.snia.org/sff/specifications2
14. Analog Devices: www.analog.com/en/index.html
    (ADG707)
15. Texas Instruments: www.ti.com
    (INA333, TXS0108E, TCA9548, PCA9306, LM96063)
16. Maxim Integrated: http://www.maximintegrated.com/products/power/intune/ and http://www.maxim-ic.com/xilinx
    (Maxim power system devices, InTune™ Digital Power Solutions)

InTune™ Digital PowerTool Software Version 1.08.02 is available. Users must create a Maxim account and login before they can see the link to download the GUI.

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