

## FEATURES

Frequency range: 17.7 GHz to 19.7 GHz

Typical gain of >25.1 dB

Low noise input

Noise figure: 2.4 dB typical

High linearity input

>-1.5 dBm typical input third-order intercept (IIP3)

-11.5 dBm input 1 dB compression point (P1dB) at 19.7 GHz

Matched 50  $\Omega$  single-ended input

Matched 100  $\Omega$  differential outputs

8-lead, 2.00 mm  $\times$  2.00 mm LFCSP microwave packaging

## APPLICATIONS

Point to point microwave radios

Instrumentation

Satellite communications (SATCOM)

Phased arrays

## GENERAL DESCRIPTION

The [ADL5725](#) is a narrow-band, high performance, low noise amplifier (LNA) targeting microwave radio link receiver designs. The monolithic silicon germanium (SiGe) design is optimized for microwave radio link bands ranging from 17.7 GHz to 19.7 GHz. The unique design offers a single-ended 50  $\Omega$  input impedance and provides a 100  $\Omega$  balanced differential output that is ideal for driving Analog Devices, Inc., differential downconverters and radio frequency (RF) sampling analog-to-digital converters (ADCs).

## FUNCTIONAL BLOCK DIAGRAM

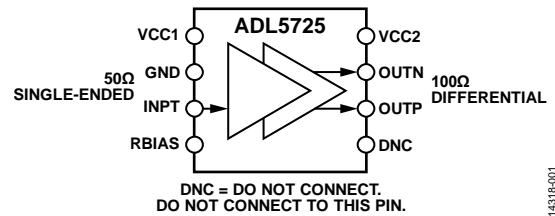


Figure 1.

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This low noise amplifier provides noise figure performance that, in the past, required more expensive three-five (III-V) compounds process technology to achieve.

The [ADL5721](#) and [ADL5723](#) to [ADL5726](#) family of narrow-band LNAs are each packaged in a tiny, thermally enhanced, 2.00 mm  $\times$  2 mm LFCSP package. The [ADL5721](#) and [ADL5723](#) to [ADL5726](#) family operates over the temperature range of -40°C to +85°C.

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**REVISION HISTORY**

**4/16—Revision 0: Initial Version**

## SPECIFICATIONS

### AC SPECIFICATIONS

VCC1 = 1.8 V, VCC2 = 3.3 V, RBIAS = 357  $\Omega$ , T = 25°C, Z<sub>SOURCE</sub> = 50  $\Omega$ , Z<sub>LOAD</sub> = 100  $\Omega$  differential, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		17.7		19.7	GHz
FREQUENCY = 17.7 GHz					
Gain (S21)	$\Delta f = 1$ MHz, input power (P <sub>IN</sub> ) = -30 dBm per tone		27.8		dB
Noise Figure			2.4		dB
Input Third-Order Intercept (IIP3)			-1.5		dBm
Input 1 dB Compression Point (P1dB)			-14		dBm
Input Return Loss (S11)			7		dB
Output Return Loss (S22)			8		dB
FREQUENCY = 19.7 GHz					
Gain (S21)	$\Delta f = 1$ MHz, P <sub>IN</sub> = -30 dBm per tone		25.1		dB
Noise Figure			2.4		dB
Input Third-Order Intercept (IIP3)			2.0		dBm
Input 1 dB Compression Point (P1dB)			-11.5		dBm
Input Return Loss (S11)			10		dB
Output Return Loss (S22)			10		dB

### DC SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INTERFACE					
Voltage					
VCC1		1.65	1.8	1.95	V
VCC2		3.1	3.3	3.5	V
Quiescent Current vs. Temperature					
VCC1	T <sub>A</sub> = 25°C -40°C ≤ T <sub>A</sub> ≤ +85°C		18		mA
VCC2		T <sub>A</sub> = 25°C -40°C ≤ T <sub>A</sub> ≤ +85°C		88	
			89		mA

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltages	
VCC1	2.25 V
VCC2	4.1 V
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature Range (Soldering, 60 sec)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is thermal resistance, junction to ambient (°C/W),  $\theta_{JB}$  is thermal resistance, junction to board (°C/W), and  $\theta_{JC}$  is thermal resistance, junction to case (°C/W).

Table 4. Thermal Resistance

Package Type	$\theta_{JA}^1$	$\theta_{JB}^1$	$\theta_{JC}^1$	Unit
8-Lead LFCSP	39.90	23.88	3.71	°C/W

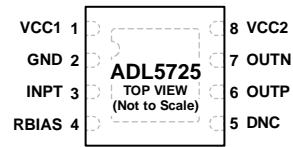
<sup>1</sup> See JEDEC standard JESD51-2 for additional information on optimizing the thermal impedance for a printed circuit board (PCB) with 3 × 4 vias.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



### NOTES

1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD MUST BE SOLDERED TO A LOW IMPEDANCE GROUND PLANE.
3. THE DEVICE NUMBER ON THE FIGURE DOES NOT INDICATE THE LABEL ON THE PACKAGE. REFER TO THE PIN 1 INDICATOR FOR THE PIN LOCATIONS.

14318-002

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC1	1.8 V Power Supply. It is recommended to place the decoupling capacitors as close to this pin as possible.
2	GND	Ground.
3	INPT	RF Input. This is a 50 $\Omega$ single-ended input.
4	RBIAS	Resistor Bias. For typical operation, connect a 357 $\Omega$ resistor from RBIAS to GND. It is recommended to place the RBIAS resistor as close to the pin as possible.
5	DNC	Do Not Connect. Do not connect to this pin.
6, 7	OUTP, OUTN	RF Outputs. These pins are 100 $\Omega$ differential outputs.
8	VCC2	3.3 V Power Supply. It is recommended to place the decoupling capacitors as close to this pin as possible.
	EPAD (EP)	Exposed Pad. The exposed pad must be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

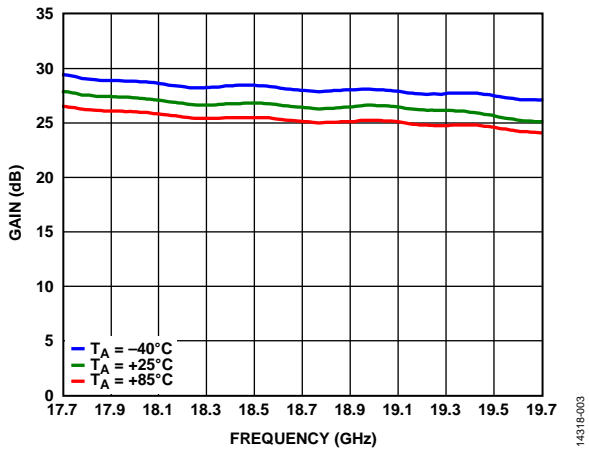


Figure 3. Gain vs. Frequency for Various Temperatures

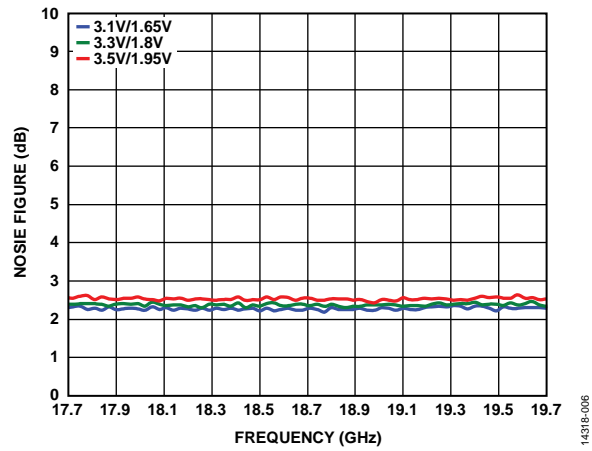


Figure 6. Noise Figure vs. Frequency for Various Supply Voltages

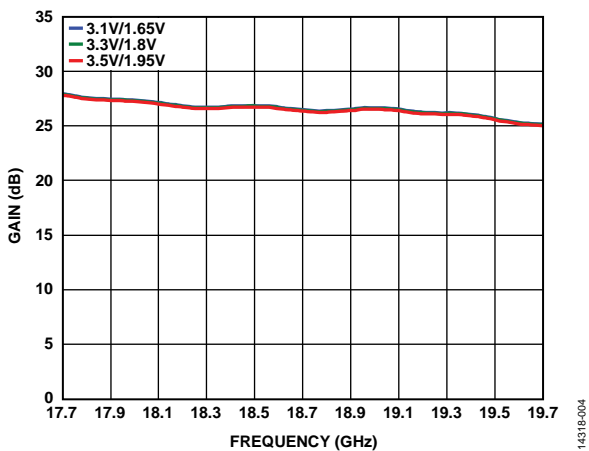


Figure 4. Gain vs. Frequency for Various Supply Voltages

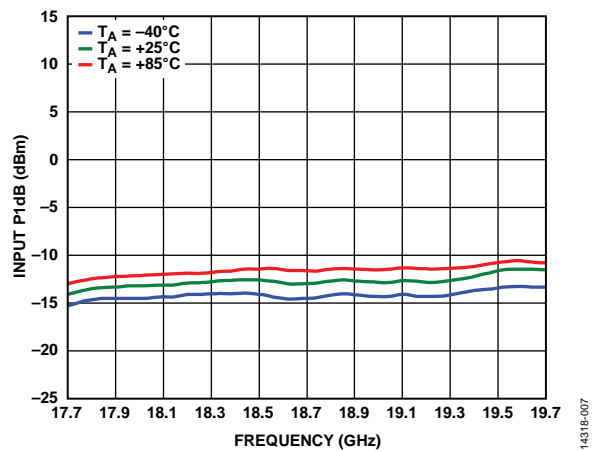


Figure 7. Input P1dB vs. Frequency for Various Temperatures

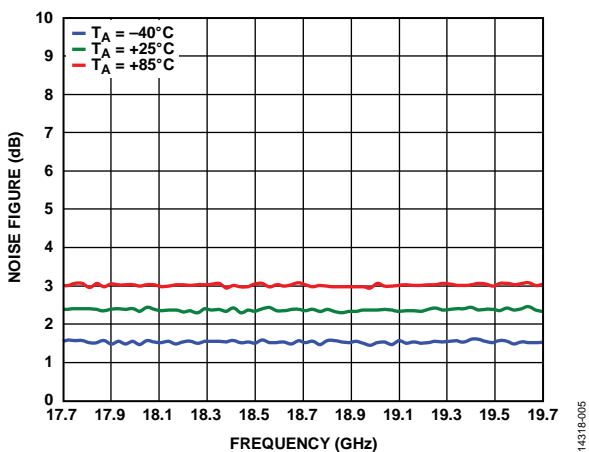


Figure 5. Noise Figure vs. Frequency for Various Temperatures

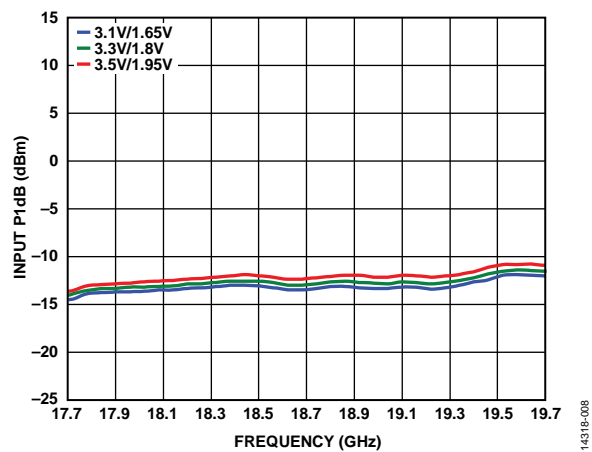


Figure 8. Input P1dB vs. Frequency for Various Supply Voltages

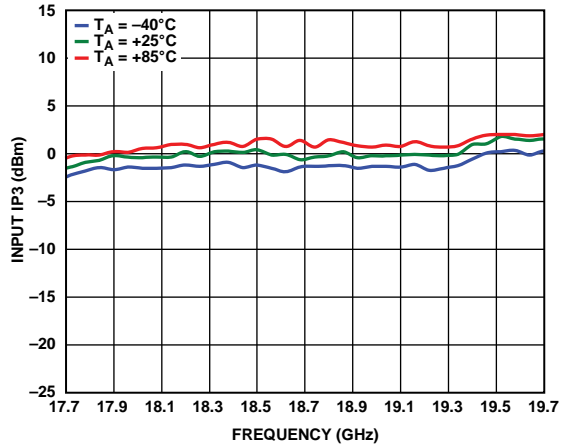


Figure 9. Input IP3 vs. Frequency for Various Temperatures

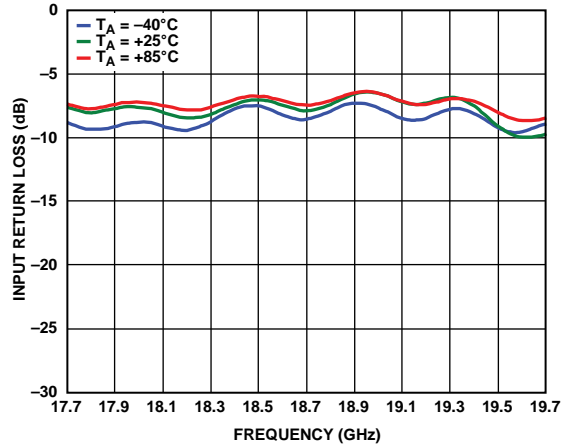


Figure 11. Input Return Loss vs. Frequency for Various Temperatures

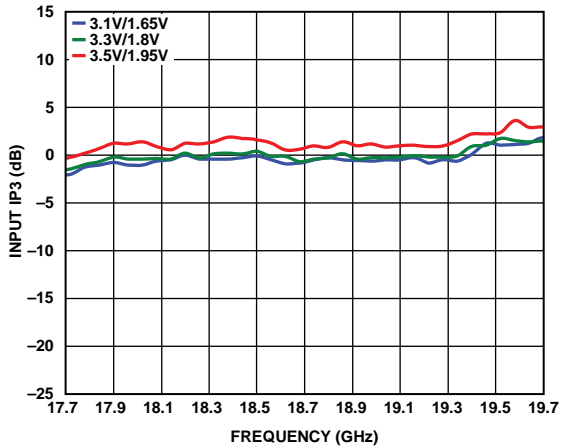


Figure 10. Input IP3 vs. Frequency for Various Supply Voltages

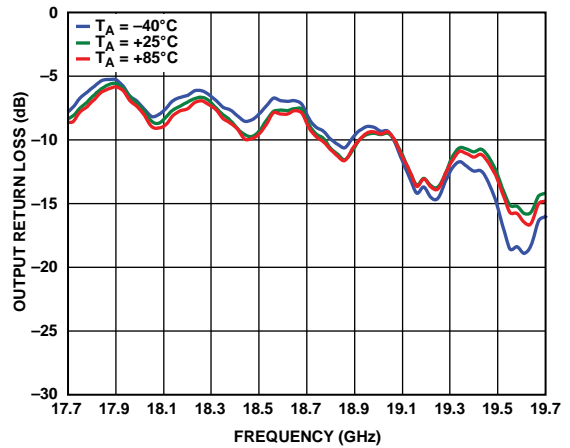


Figure 12. Output Return Loss vs. Frequency for Various Temperatures

## THEORY OF OPERATION

The [ADL5725](#) is a narrow-band, high performance, low noise amplifier targeting microwave radio link receiver designs. The monolithic SiGe design is optimized for microwave radio link bands ranging from 17.7 GHz to 19.7 GHz.

The unique design of the [ADL5725](#) offers a single-ended 50  $\Omega$  input impedance via the INPT pin, and provides a 100  $\Omega$  balanced differential output via the OOTP and OUTN pins.

This LNA is ideal for driving Analog Devices differential downconverters and RF sampling ADCs.

The [ADL5725](#) provides cost-effective noise figure performance without requiring more expensive III-V compounds process technology.

The [ADL5725](#) is available in a 2.00 mm  $\times$  2.00 mm LFCSP package, and operates over the temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



# APPLICATIONS INFORMATION

## LAYOUT

Solder the exposed pad on the underside of the ADL5725 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect the ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package.

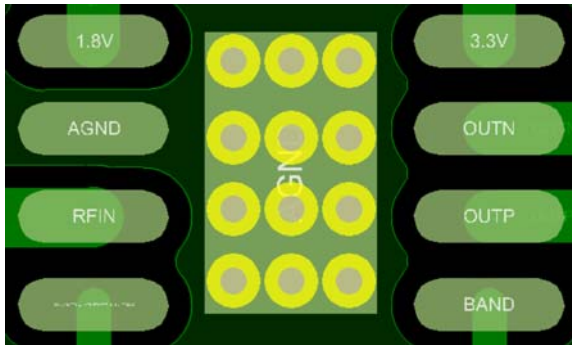


Figure 13. Evaluation Board Layout for the ADL5725 Package

## DIFFERENTIAL vs. SINGLE-ENDED OUTPUT

This section provides the test results that compare the ADL5725 using a differential vs. single-ended output. When using the device as a single-ended output, use the RFOP output of the evaluation board and terminate RFON to 50 Ω. Note that the converse can be done as well; however, doing so produces slightly different results from the plots shown in this section because there is some amplitude imbalance between the two differential ports, RFOP and RFON. The output trace and connector loss were not deembedded for these measurements.

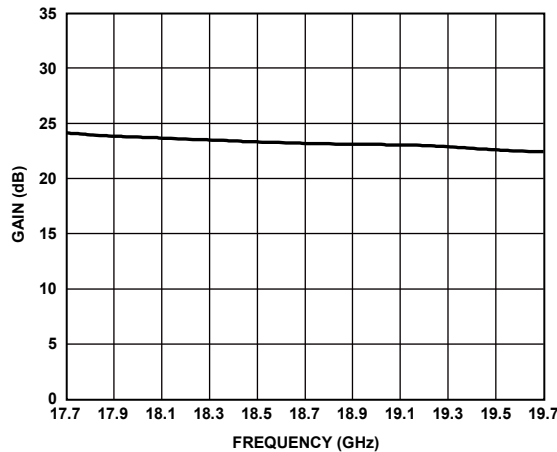


Figure 14. Gain vs. Frequency

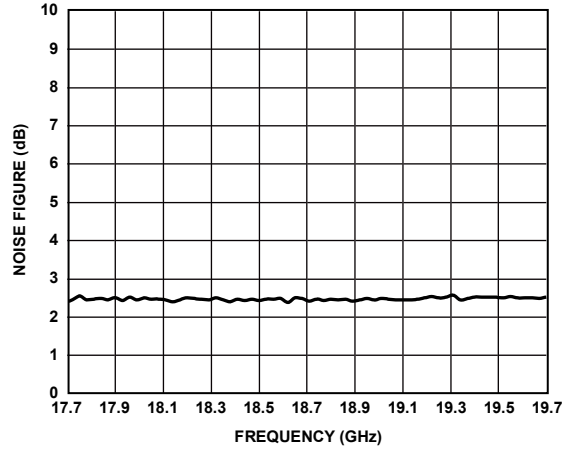


Figure 15. Noise Figure vs. Frequency

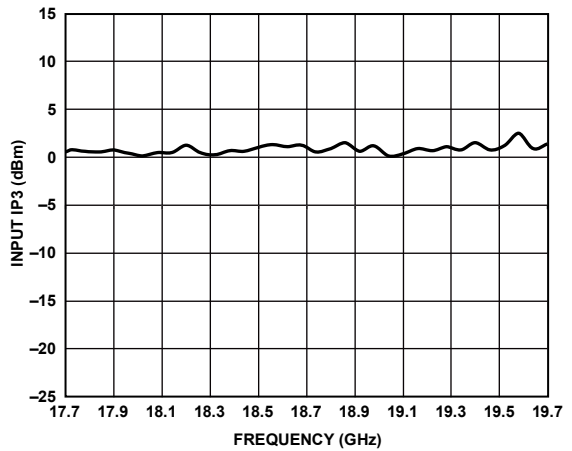


Figure 16. Input IP3 vs. Frequency

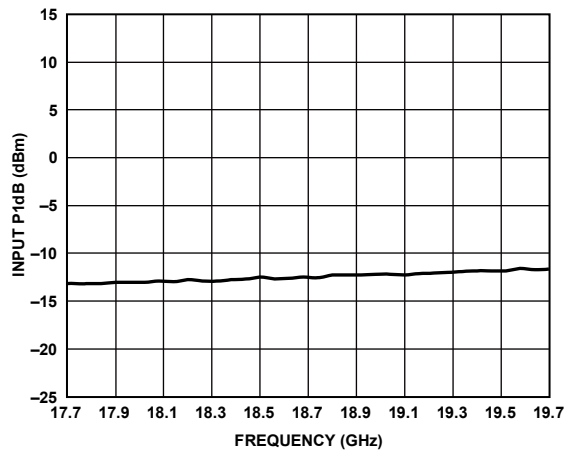


Figure 17. Input P1dB vs. Frequency

## EVALUATION BOARD

The [ADL5725-EVALZ](#) comes with an [ADL5725](#) chip. It supports a single 5 V supply for ease of use. For 5 V operation, use the 3.3 V and 1.8 V test loops for evaluation purposes only. When using a 3.3 V or 1.8 V supply, remove the R1 and R2 resistors from the evaluation board. Figure 19 shows the [ADL5725-EVALZ](#) evaluation board lab bench setup.

### INITIAL SETUP

To set up the [ADL5725-EVALZ](#), take the following steps:

1. Power up the [ADL5725-EVALZ](#) with a 5 V dc supply. The supply current of the evaluation board is approximately 111 mA, which is a combination of the VCC1 (1.8 V) and the VCC2 (3.3 V) currents.
2. Connect the signal generator to the input of the [ADL5725-EVALZ](#).
3. Connect RFOP and RFON to a 180° hybrid that works within the 17.7 GHz to 19.7 GHz frequency range.
4. Connect the difference output of the hybrid to the spectrum analyzer. The sum port of hybrid must be terminated to 50 Ω.

See Figure 19 for the [ADL5725-EVALZ](#) lab bench setup.

### RESULTS

Figure 18 shows the expected results when testing the [ADL5725-EVALZ](#) using the Rev. A version of the evaluation board and its software. Note that future iterations of the software may produce different results. See the [ADL5725](#) product page for the most recent software version.

Figure 18 shows the results of the differential output for an input of 17.7 GHz at -15 dBm. The hybrid and board loss were not deembedded.

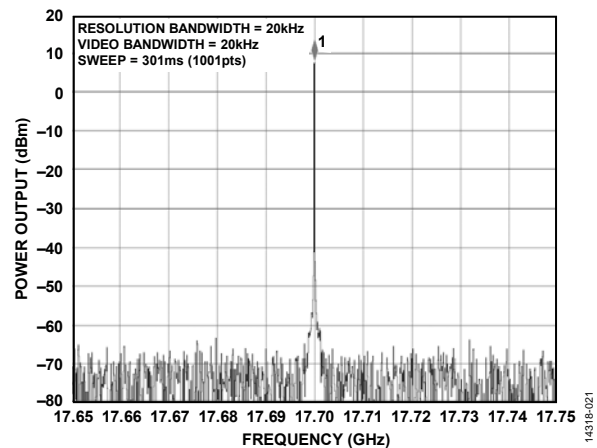


Figure 18. Test Results at 17.7 GHz

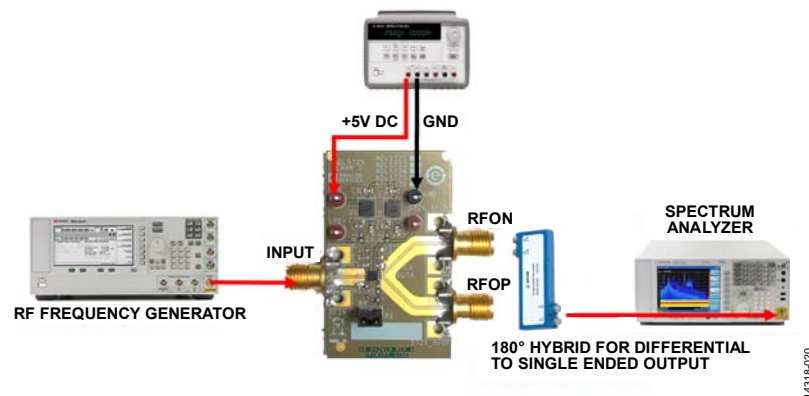


Figure 19. [ADL5725-EVALZ](#) Lab Bench Setup

**BASIC CONNECTIONS FOR OPERATION**

Figure 20 shows the basic connections for operating the ADL5725 as it is implemented on the evaluation board of the device.

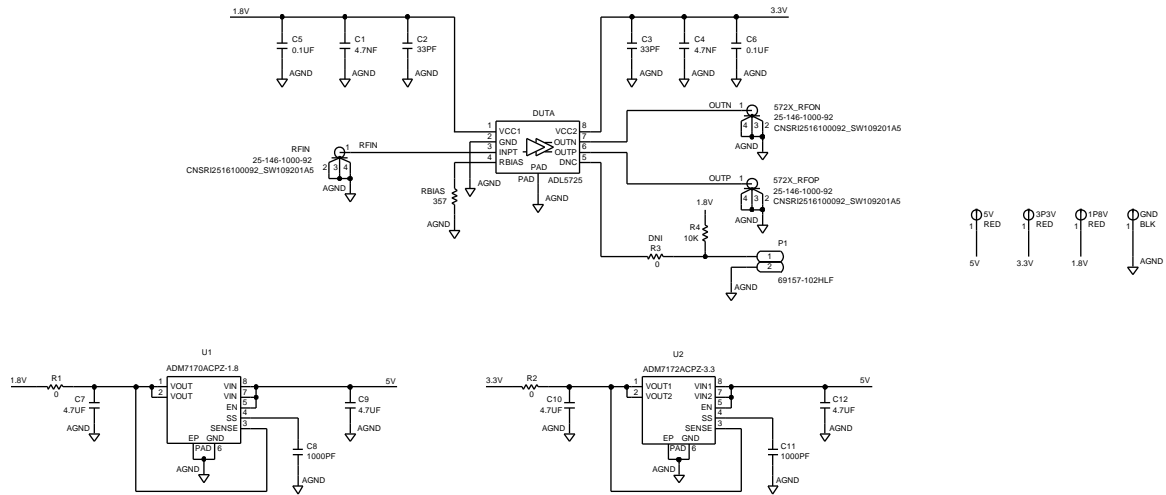
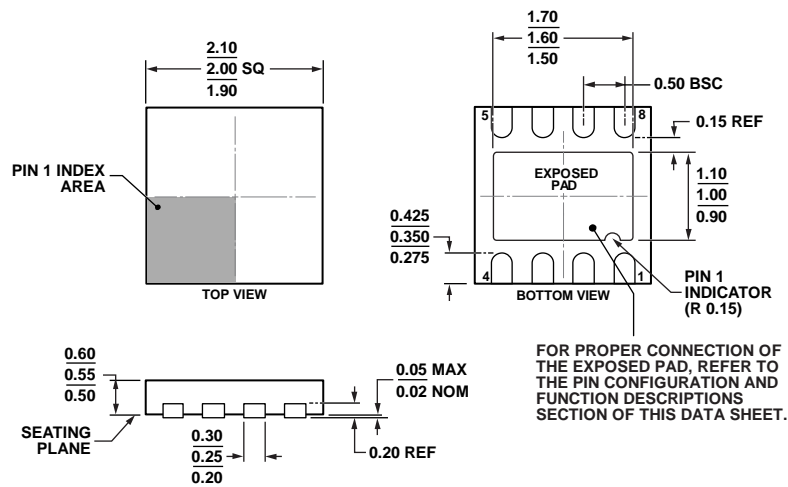


Figure 20. Evaluation Board Schematic

**Table 6. Evaluation Board Configuration Options**

Component	Function	Default Condition
3P3V, 1P8V, GND, 5V	Power supplies and ground.	Not applicable
RFIN, 572X_RFOP, 572x_RFON	Input, output, and data.	Not applicable
RBIAS	357 Ω for RBIAS.	RBIAS = 357 Ω (0402)
R1, R2	1.8 V and 3.3 V regulator connections.	R1, R2 = 0 Ω (0402)
R3	Do not install (DNI).	R3 = DNI (0402)
R4	Pull-up or pull-down resistor.	R4 = 10 kΩ (0402)
C1 to C12	The capacitors provide the required decoupling for the supply related pins.	C1, C4 = 4.7 nF (0402), C2, C3 = 33 pF (0402), C5, C6 = 0.1 μF (0402), C7, C9, C10, C12 = 4.7 μF (0603), C8, C11 = 1000 pF (0603)
P1	Jumper to change bands, 2-pin jumper.	Not applicable
U1	ADM7170ACPZ-1.8 1.8 V regulator.	Not applicable
U2	ADM7172ACPZ-3.3 3.3 V regulator.	Not applicable
DUTA	ADL5725 device under test (DUT).	Not applicable

OUTLINE DIMENSIONS



01-14-2013-C

Figure 21. 8-Lead Lead Frame Chip Scale Package [LFCSP]  
 2.00 mm × 2.00 mm Body, and 0.55 mm Package Height  
 (CP-8-10)  
 Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADL5725ACPZN-R7	-40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-10
ADL5725-EVALZ		Evaluation Board	

<sup>1</sup> Z = RoHS-Compliant Part.