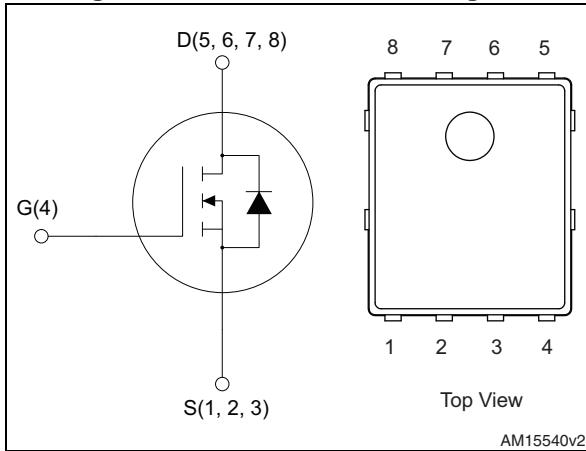


## N-channel 650 V, 0.215 $\Omega$ typ., 15 A MDmesh™ V Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet – preliminary data



**Figure 1. Internal schematic diagram**



## Features

Order code	$V_{DS}$	$R_{DS(on)max.}$	$I_D$
STL18N65M5	710 V	0.240 $\Omega$	15 A <sup>(1)</sup>

1. The value is rated according to  $R_{thj-case}$  and limited by package.

- Outstanding  $R_{DS(on)}^*$ area
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitance
- 100% avalanche tested

## Applications

- Switching applications

## Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL18N65M5	18N65M5	PowerFLAT™ 5x6 HV	Tape and reel

## Contents

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# 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	15	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	6.5	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	60	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	57	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	210	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-case}$  and limited by package.

2. Pulse width limited by safe operating area.

3.  $I_{SD} \leq 15\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{Peak} \leq V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.2	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-amb max	59	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_C = 25^\circ\text{C}$  unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1 \text{ mA}$	650			V
$I_{\text{DSS}}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650 \text{ V}$ $V_{DS} = 650 \text{ V}, T_C = 125^\circ\text{C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{\text{GSS}}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25 \text{ V}$			$\pm 100$	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$		0.215	0.240	$\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	1240	-	pF
$C_{\text{oss}}$	Output capacitance		-	32	-	pF
$C_{\text{rss}}$	Reverse transfer capacitance		-	3	-	pF
$C_{o(\text{tr})}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0 \text{ to } 520 \text{ V}, V_{GS} = 0$	-	99	-	pF
$C_{o(\text{er})}^{(2)}$	Equivalent capacitance energy related		-	30	-	pF
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz}$ open drain	-	3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520 \text{ V}, I_D = 7.5 \text{ A},$ $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 16</a> )	-	31	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	8	-	nC
$Q_{\text{gd}}$	Gate-drain charge		-	14	-	nC

1.  $C_{\text{oss eq}}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2.  $C_{\text{oss eq}}$  energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{\text{oss}}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400 \text{ V}$ , $I_D = 9.5 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 17</a> and <a href="#">20</a> )	-	36	-	ns
$t_r$	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	9	-	ns
$t_f$	Fall time		-	11	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		15	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 15 \text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 15 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 17</a> )	-	290		ns
$Q_{rr}$	Reverse recovery charge		-	3.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	23.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 15 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150^\circ\text{C}$ (see <a href="#">Figure 17</a> )	-	352		ns
$Q_{rr}$	Reverse recovery charge		-	4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	24		A

1. The value is rated according to  $R_{thj-case}$  and limited by package.

2. Pulse width limited by safe operating area

3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

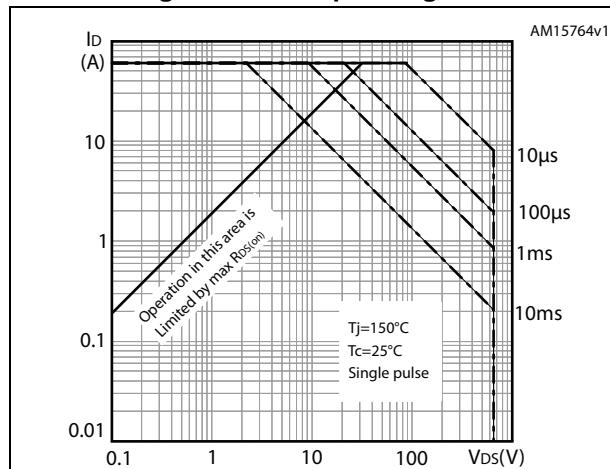


Figure 3. Thermal impedance

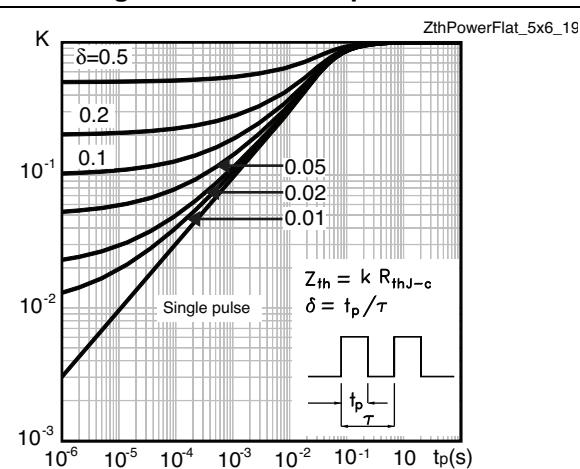


Figure 4. Output characteristics

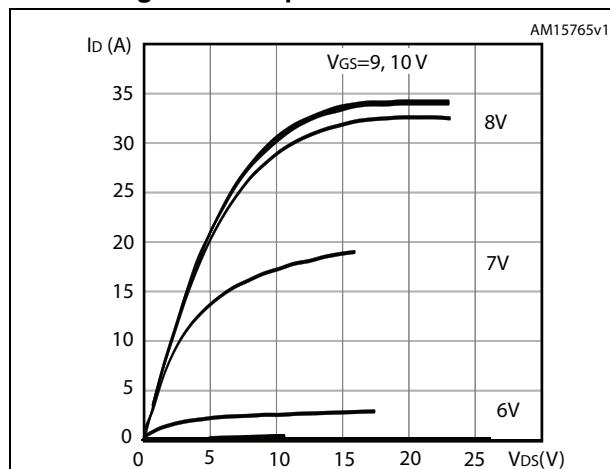


Figure 5. Transfer characteristics

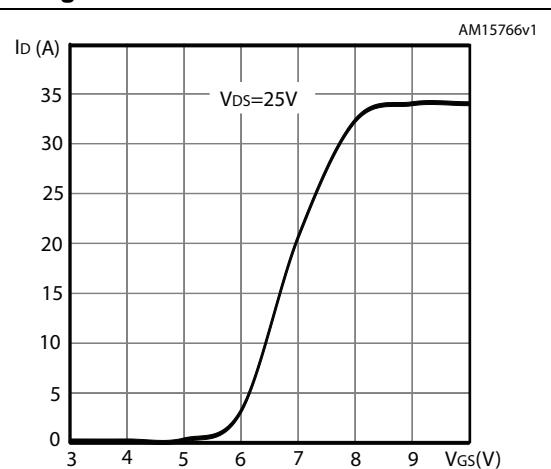


Figure 6. Gate charge vs gate-source voltage

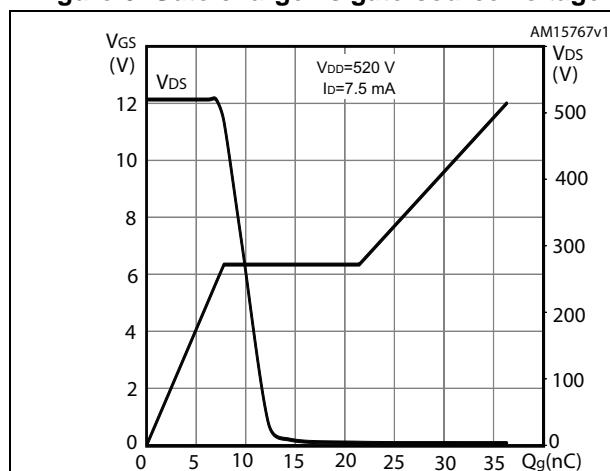


Figure 7. Static drain-source on-resistance

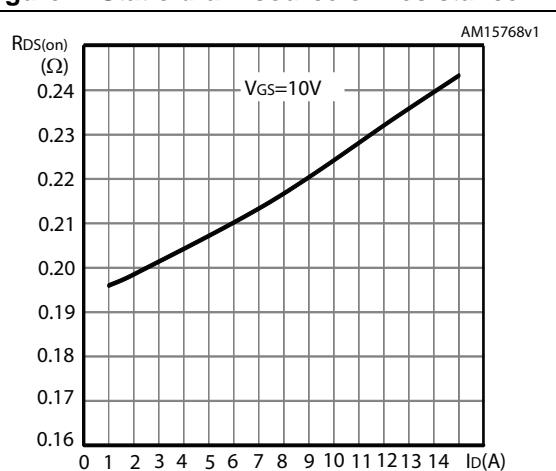


Figure 8. Capacitance variations

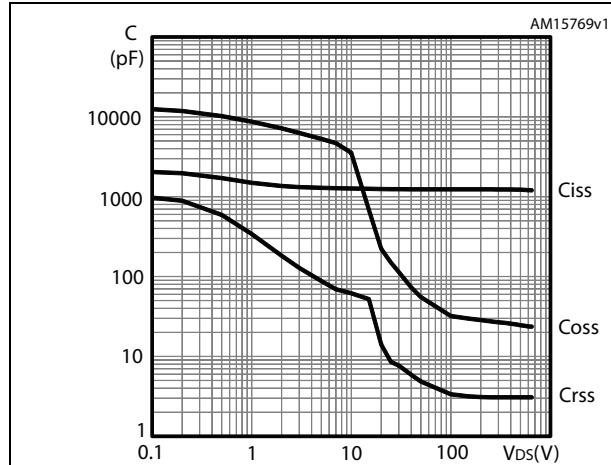


Figure 9. Output capacitance stored energy

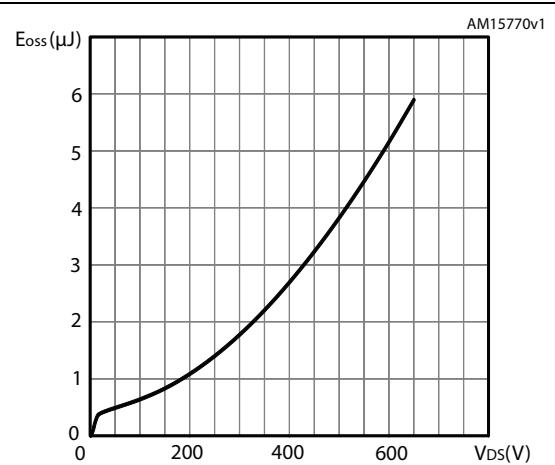


Figure 10. Normalized gate threshold voltage vs. temperature

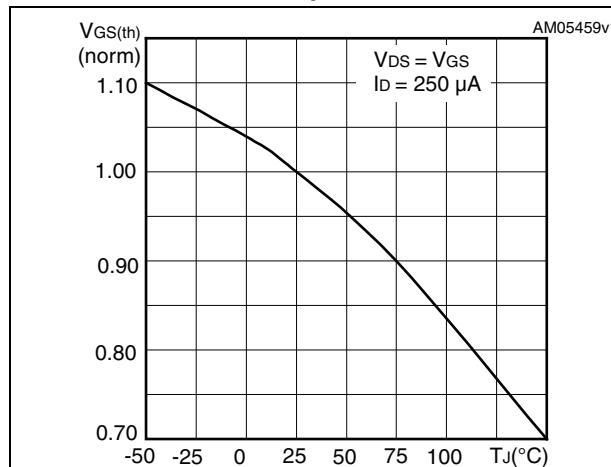


Figure 11. Normalized on-resistance vs. temperature

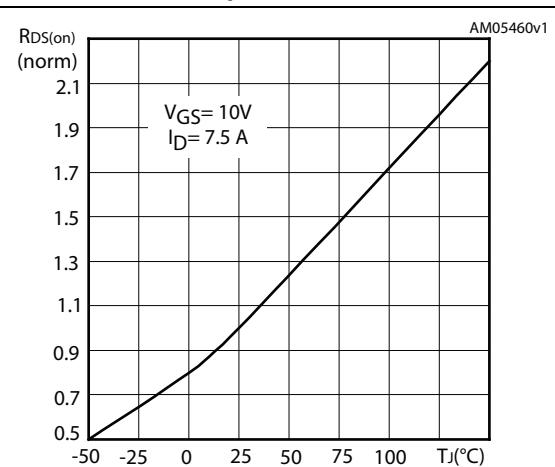
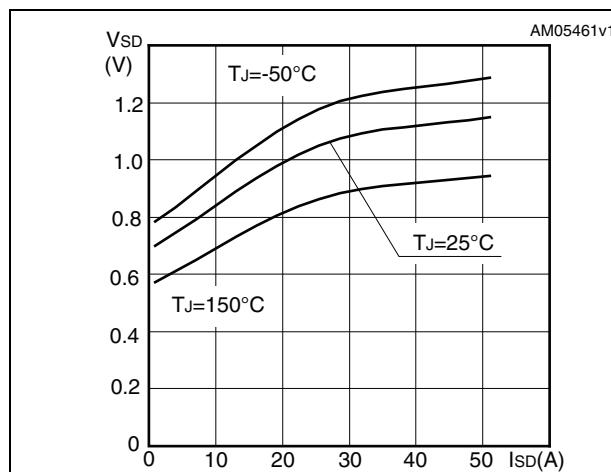
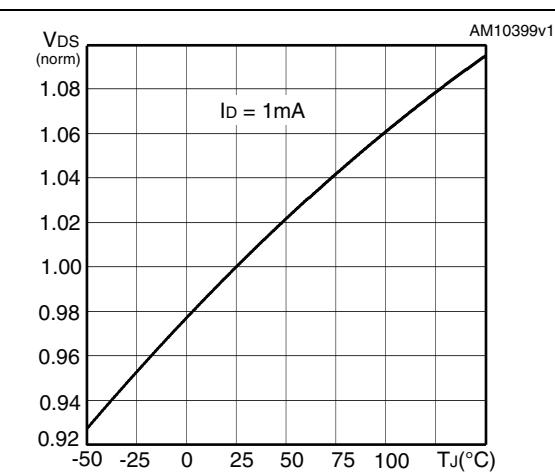
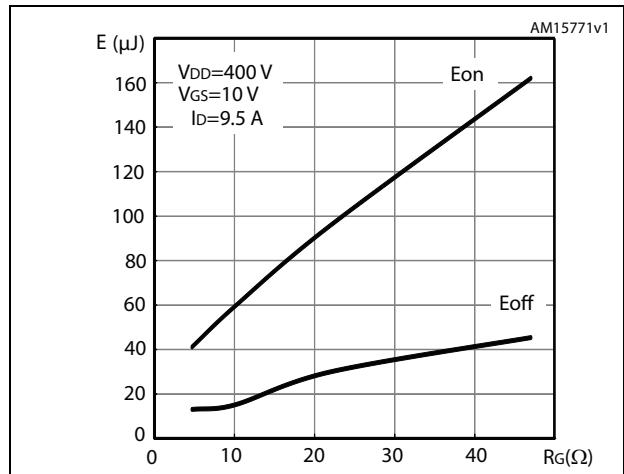


Figure 12. Drain-source diode forward characteristics

Figure 13. Normalized  $B_{VDSS}$  vs. temperature

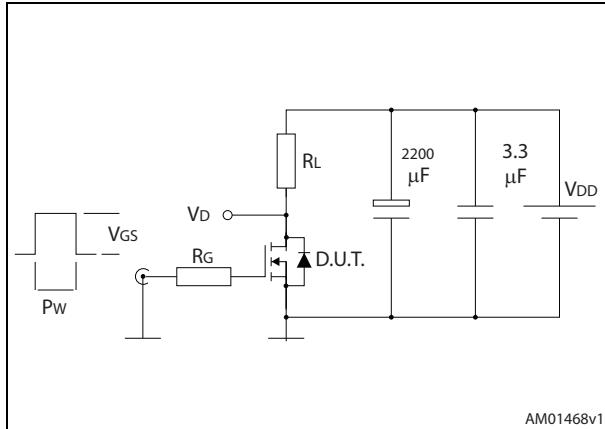
**Figure 14. Switching losses vs gate resistance (1)**



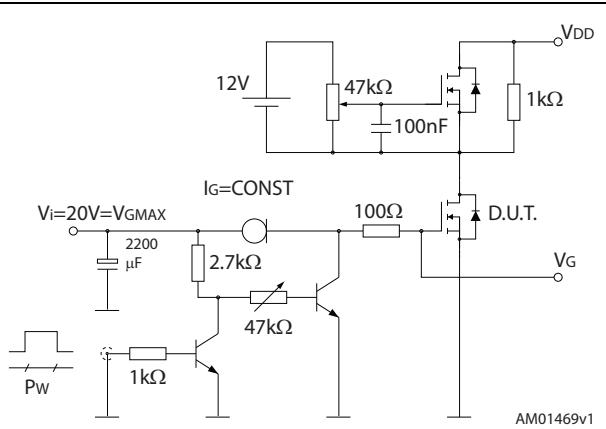
1. Eon including reverse recovery of a SiC diode

### 3 Test circuits

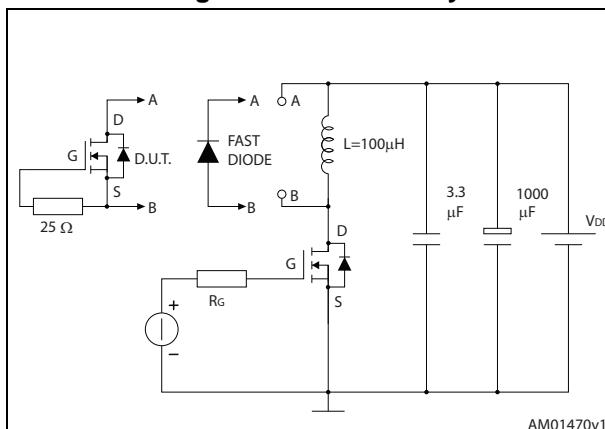
**Figure 15. Switching times test circuit for resistive load**



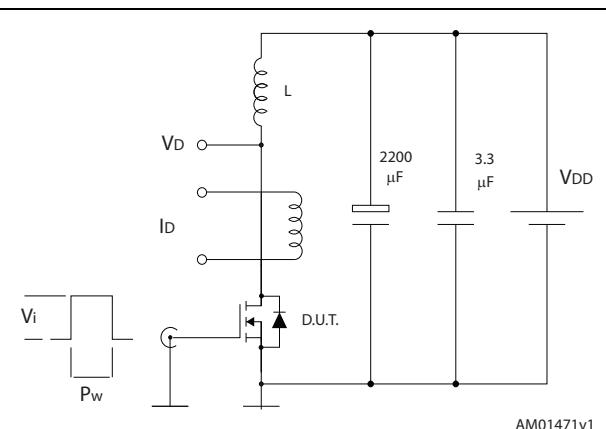
**Figure 16. Gate charge test circuit**



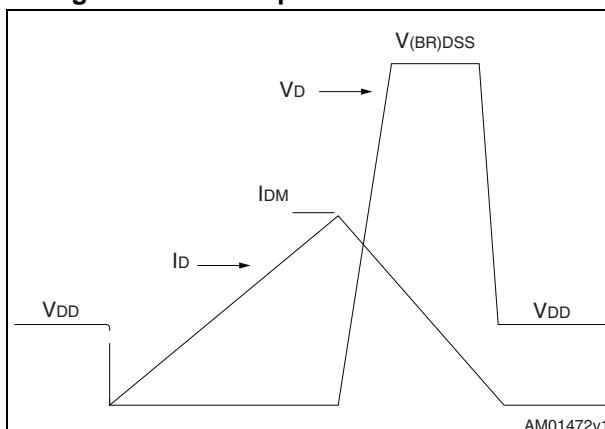
**Figure 17. Test circuit for inductive load switching and diode recovery times**



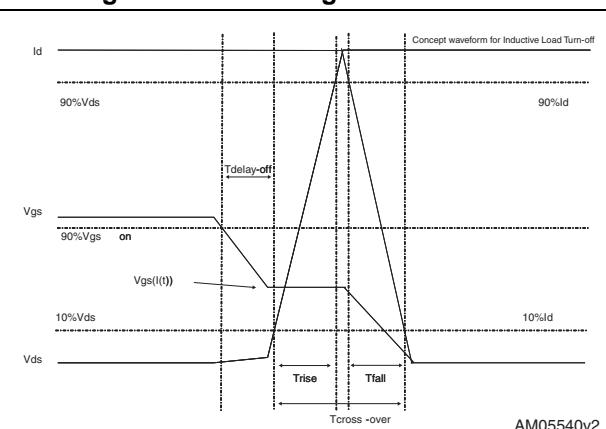
**Figure 18. Unclamped inductive load test circuit**



**Figure 19. Unclamped inductive waveform**



**Figure 20. Switching time waveform**



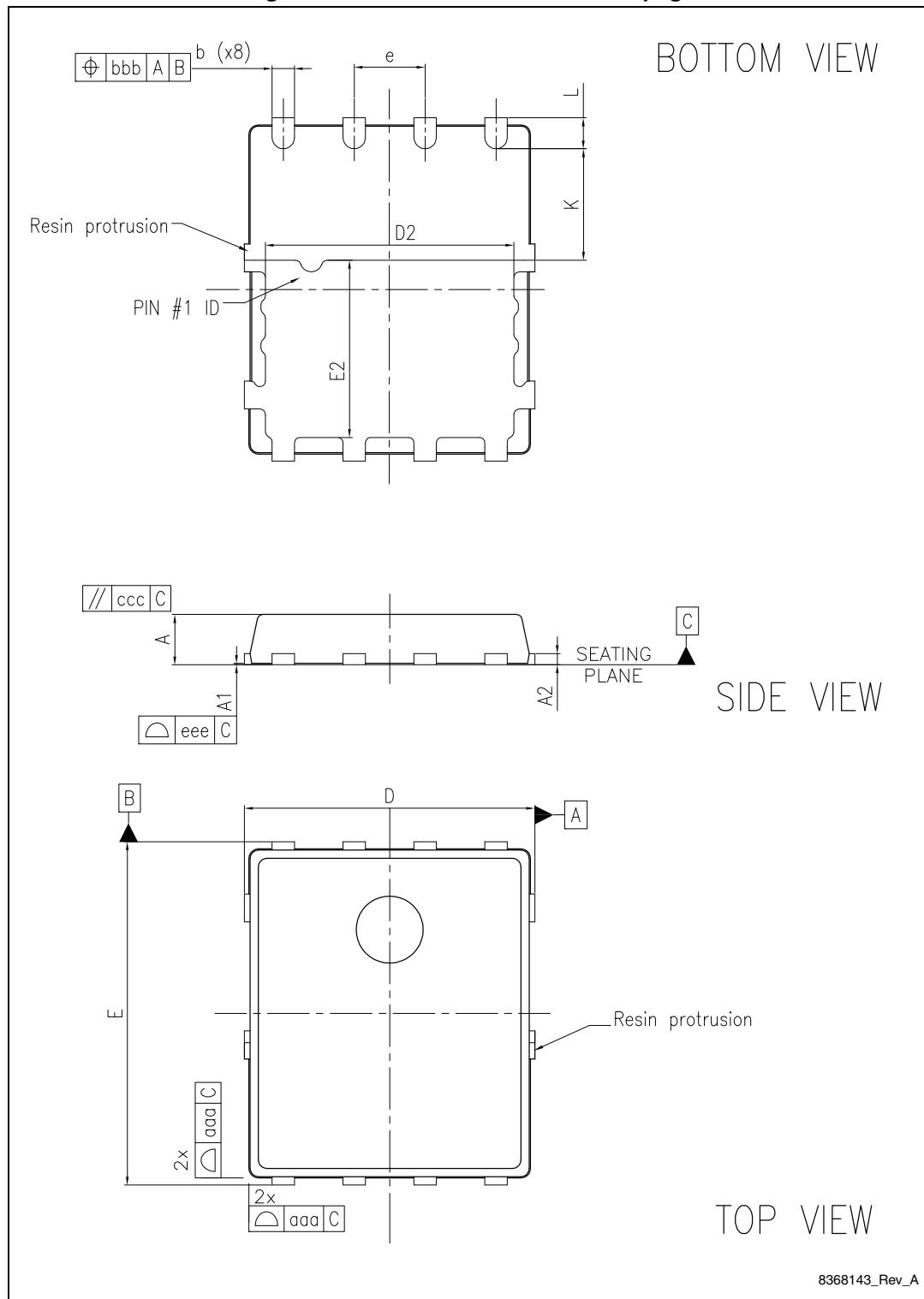
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
ECOPACK® is an ST trademark.

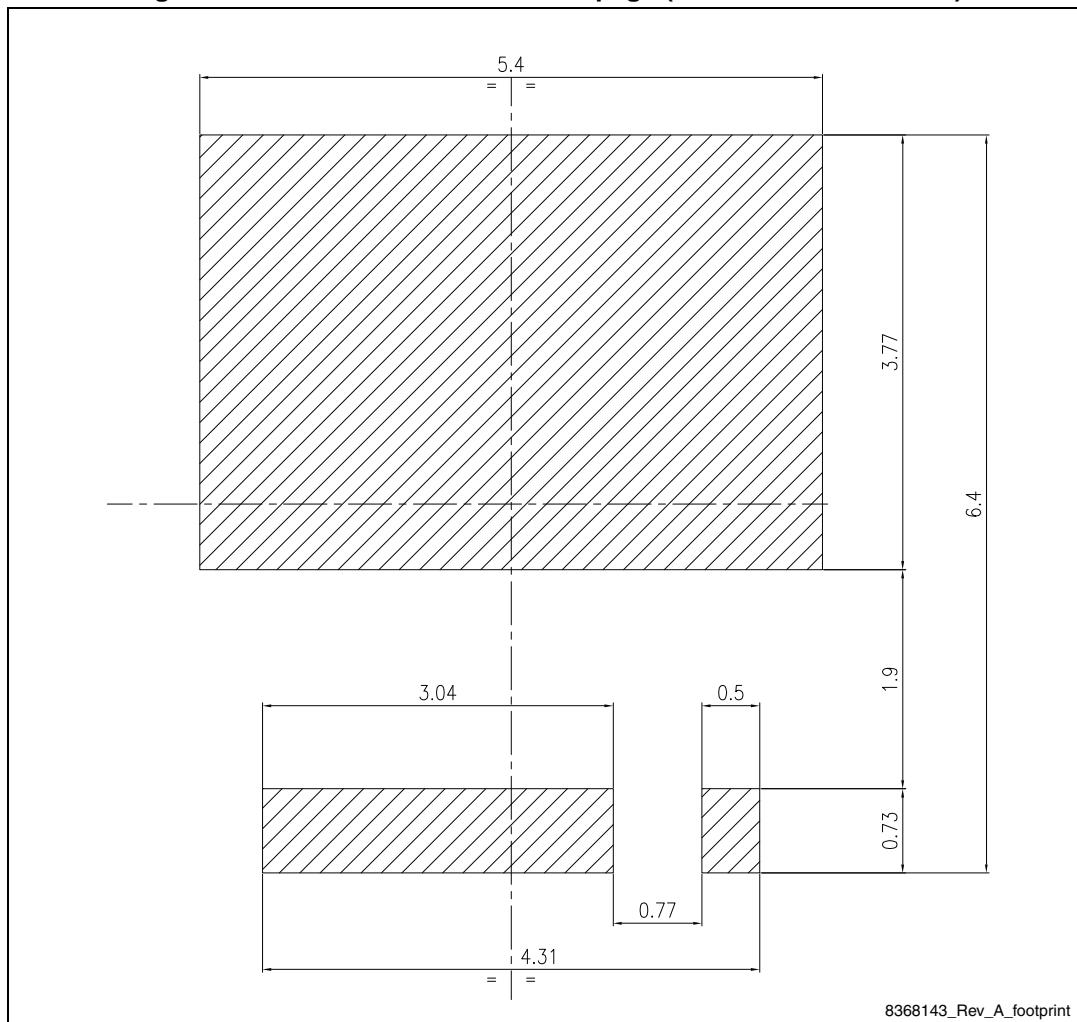
**Table 8. PowerFLAT™ 5x6 HV creepage**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10
aaa		0.15	
bbb		0.15	
ccc		0.10	
eee		0.10	

Figure 21. PowerFLATTM 5x6 HV creepage



8368143\_Rev\_A

**Figure 22. PowerFLAT™ 5x6 HV creepage (dimensions are in mm)**

## 5 Packaging mechanical data

Figure 23. PowerFLAT™ 5x6 tape

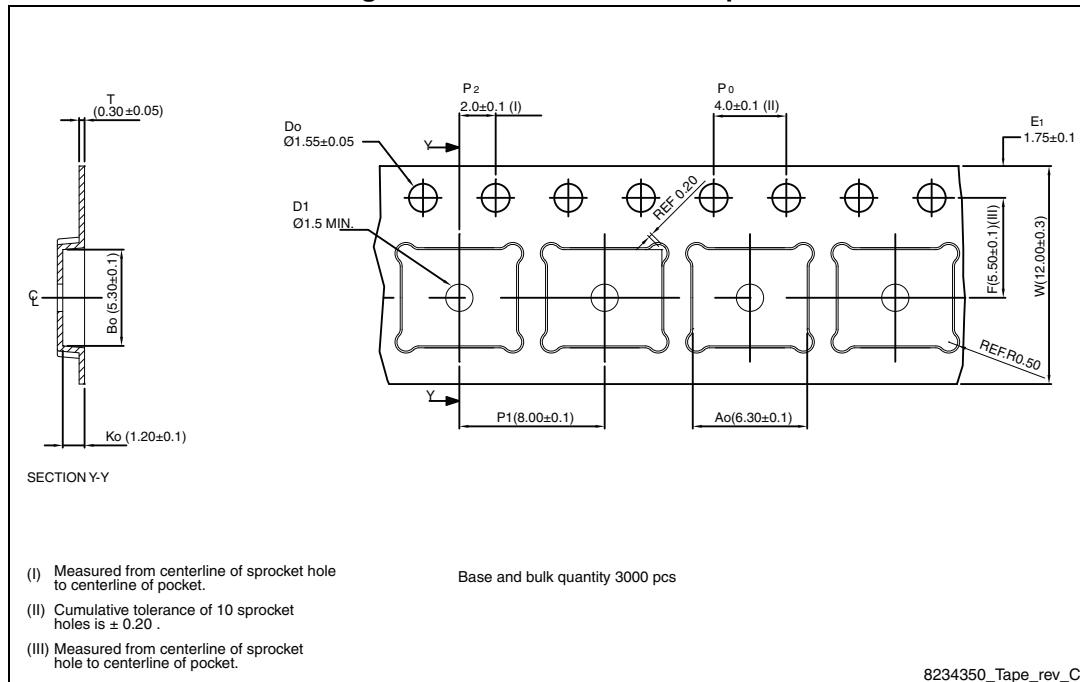


Figure 24. PowerFLAT™ 5x6 package orientation in carrier tape.

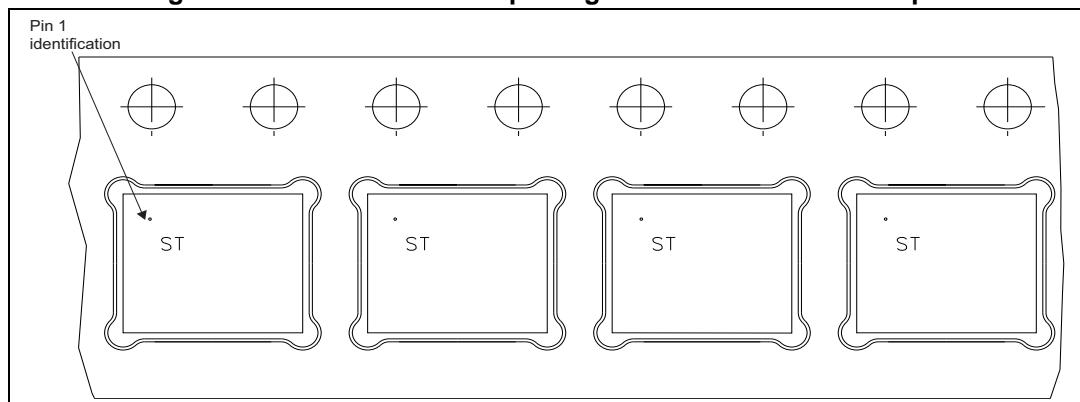
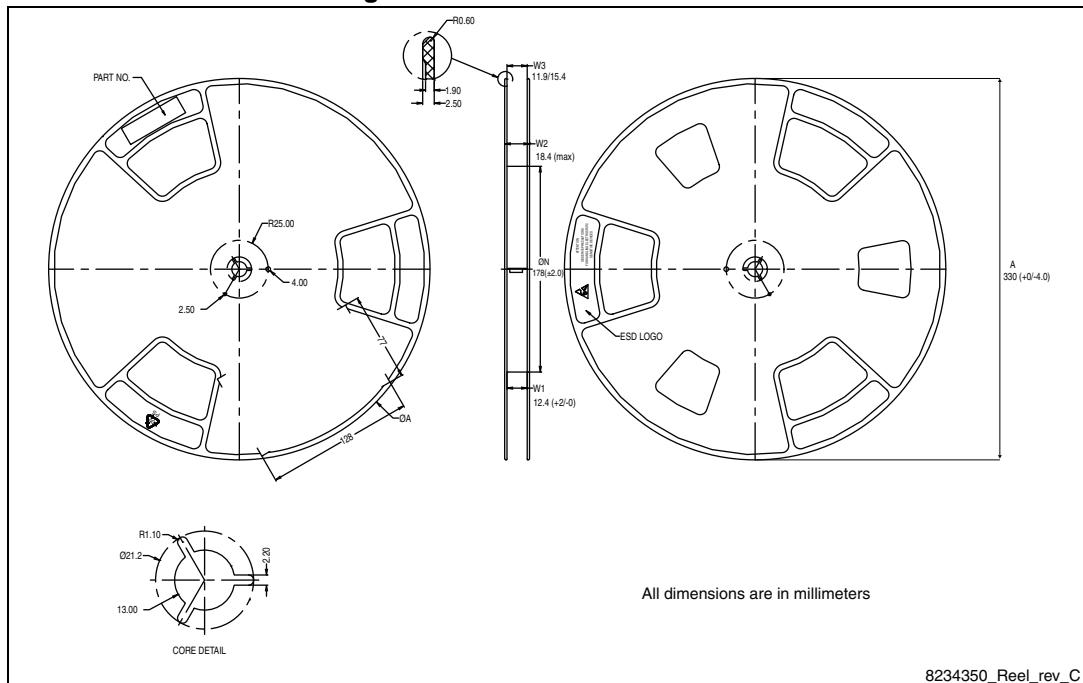


Figure 25. PowerFLAT™ 5x6 reel



## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
24-Apr-2013	1	First release
26-Jun-2013	2	<ul style="list-style-type: none"><li>– Modified: <i>Figure 6, 15, 16, 17, 18</i></li><li>– Minor text changes</li></ul>

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