DESCRIPTION

Demonstration circuit 854 supports a family of 16/14-Bit 130Msps ADCs. Each assembly features one of the following devices: LTC2208, LTC2208-14 high speed, high dynamic range ADCs.

This Demonstration circuit only supports CMOS output operation. For demonstration of LVDS output signaling, please see DC996.

The versions of the DC854C and DC854D demo board that support the LTC2208 16-Bit and LTC2208-14 14-Bit series of A/D converters are listed in Table 1. Depending on the required resolution, sample rate and input frequency, the DC854 is supplied with the appropriate ADC and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies below 70MHz or from 70MHz to 140MHz. Refer to the datasheet for applications information.

Design files for this circuit board are available. Call the LTC factory.

1. DC854 Variants

DC854 VARIANTS	ADC PART NUMBER	RESOLUTION*	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
854D-A	LTC2208	16-Bit	130Msps	1MHz - 70MHz
854D-B	LTC2208	16-Bit	130Msps	70MHz -140MHz
854D-C	LTC2208-14	14-Bit	130Msps	1MHz - 70MHz
854D-D	LTC2208-14	14-Bit	130Msps	70MHz -140MHz
854C-P	LTC2208	16-Bit	130Msps	>140MHz
854C-Q	LTC2208-14	14-Bit	130Msps	>140MHz

2. Performance Summary (T_A = 25°C)

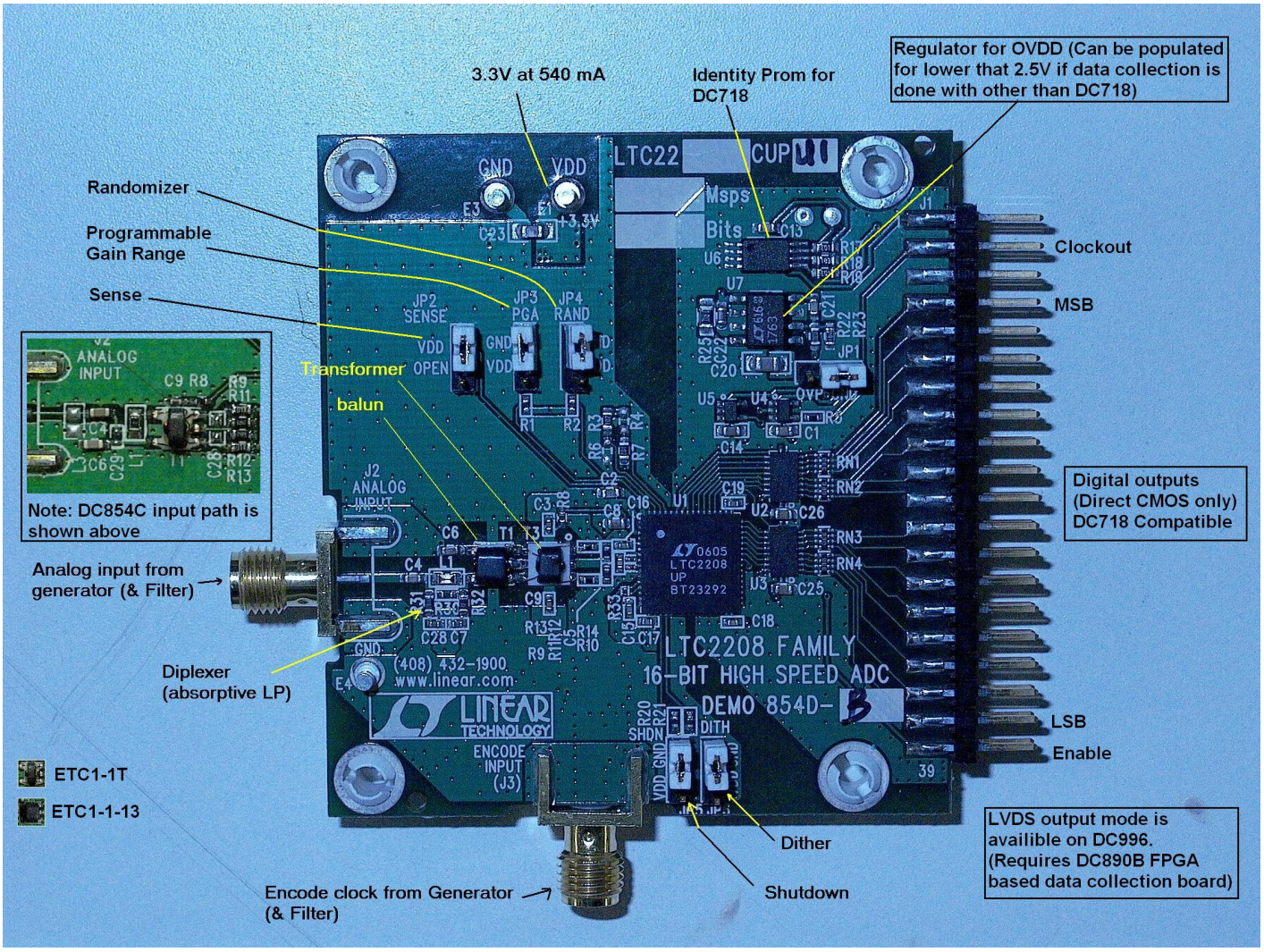
PARAMETER	CONDITION	VALUE
Supply Voltage	Depending on sampling rate and the A/D converter provided, this supply must provide up to 500mA.	Optimized for 3.3V [3.15V ⇔3.45V min/max]
Analog input range	Depending on PGA Pin Voltage	$1.5V_{PP}$ to $2.25V_{PP}$
Logic Input Voltages	Minimum Logic High	2.4V
	Maximum Logic Low	0.8V
Logic Output Voltage (74VCX245 output buffer, V_{cc} = 2.5V)	Minimum Logic High @ -1.6mA	2.3V (33Ω Series terminations)
	Maximum Logic Low @ 1.6mA	0.7V (33Ω Series terminations)
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	50 Ω Source Impedance, AC coupled or ground referenced (Convert Clock input is capacitor coupled on board and terminated with 50Ω.)	$2V_{P-P}$ ⇔$2.5V_{P-P}$ Sine Wave or Square wave
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 854 is easy to set up to evaluate the performance of most members of the LTC2208 family of A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

If a DC718 QuickDAACS Data Analysis and Collection System was supplied with the DC854 demonstration circuit, follow the DC718 Quick Start Guide to install the required software and for connecting the DC718 to the DC854 and to a PC running Windows98, 2000 or XP.



1) **DC854 Setup (zoom for detail)**

JUMPERS

The DC854 demonstration circuit board should have the following jumper settings as default: (as per figure 1)

JP1: Output clock polarity: GND
JP2: SENSE: VDD, (Internal reference)
JP3: PGA: GND 2.25V range
JP4: RAND: GND Not randomized
JP5: SHDN: GND Not Shutdown
JP6: DITH: GND No internal dithering

POWER

If a DC718 is used to acquire data from the DC854, the DC718 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE applying +3.3V across the pins marked "+3.3V" and "PWR GND" on the DC854. The DC854 demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC718 data collection board is normally powered by the USB cable and does not require an external power supply unless it is connected to the PC through an un-powered hub. In this case it must be supplied with 6-9V on turrets G7 (+) and G1 (-) or the adjacent 2.1mm power jack.

ENCODE CLOCK

NOTE: This is not a logic compatible input. It is terminated with 50 Ohms. Apply an encode clock to the SMA connector on the DC854 demonstration circuit board marked "J3 ENCODE INPUT". The transformer is terminated on the secondary side with 100 ohms, and further terminated at the ADC (at C11).

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be large, up to $3V_{P-P}$ or +13dBm. Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input.

Apply the analog input signal of interest to the SMA connectors on the DC854 demonstration circuit board marked "J2 ANALOG INPUT". These inputs are capacitive coupled to Balun transformers ETC1-1-13, or directly coupled through Flux coupled transformers ETC1-1T. (See Schematic)

ANALOG INPUT NETWORK

For optimal distortion and noise performance the RC network on the analog inputs should be optimized for different analog input frequencies. Refer to the provided schematics. These two input networks cover a broad bandwidth and are not optimized for operation at a specific input frequency. For input frequencies less than 5MHz, or greater than 150MHz, other input networks may be more appropriate.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

DC854D has provision for additional components that may be used to implement a band pass filter, or more optimal return loss in a given frequency range. The default population is a simple network as shown in the schematic.

In some cases, 3-10dB pads may be required to obtain low distortion.

If your generator cannot deliver full scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively low Q filter used between the amplifier and the demo circuit.

DIGITAL OUTPUTS

An internally generated conversion clock output is available on pin 3 of J1 and the data output is available on Pins 7-37 for 16-Bits (or 7-33 for 14-Bits) of J1 which can be collected via a logic analyzer, cabled to a development system through a SHORT 2 to 4 inch long 40-pin ribbon cable or collected by the DC718 QuickEval-II Data Acquisition Board.

SOFTWARE

The DC718B board is configurable by *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC718 was provided, follow the DC718 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC854 demonstration circuit is properly connected to the DC718, PSCOPE should automatically detect the DC854, and configure itself accordingly. If necessary the procedure below explains how to manually configure PSCOPE.

Configure PScope for the appropriate variant of the DC854 demonstration circuit by selecting the correct A/D Converter as installed on the DC854. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, LTC2208, through LTC2208-14. Select the part in the Device List and PScope will automatically blank the last two LSBs when using a DC854 supplied with a 14-Bit part. If you are operating with a version of PScope that does not include LTC2208 in the device menu, you may manually configure as:

User configure

16-Bit (or 14-Bit if using LTC2208-14)

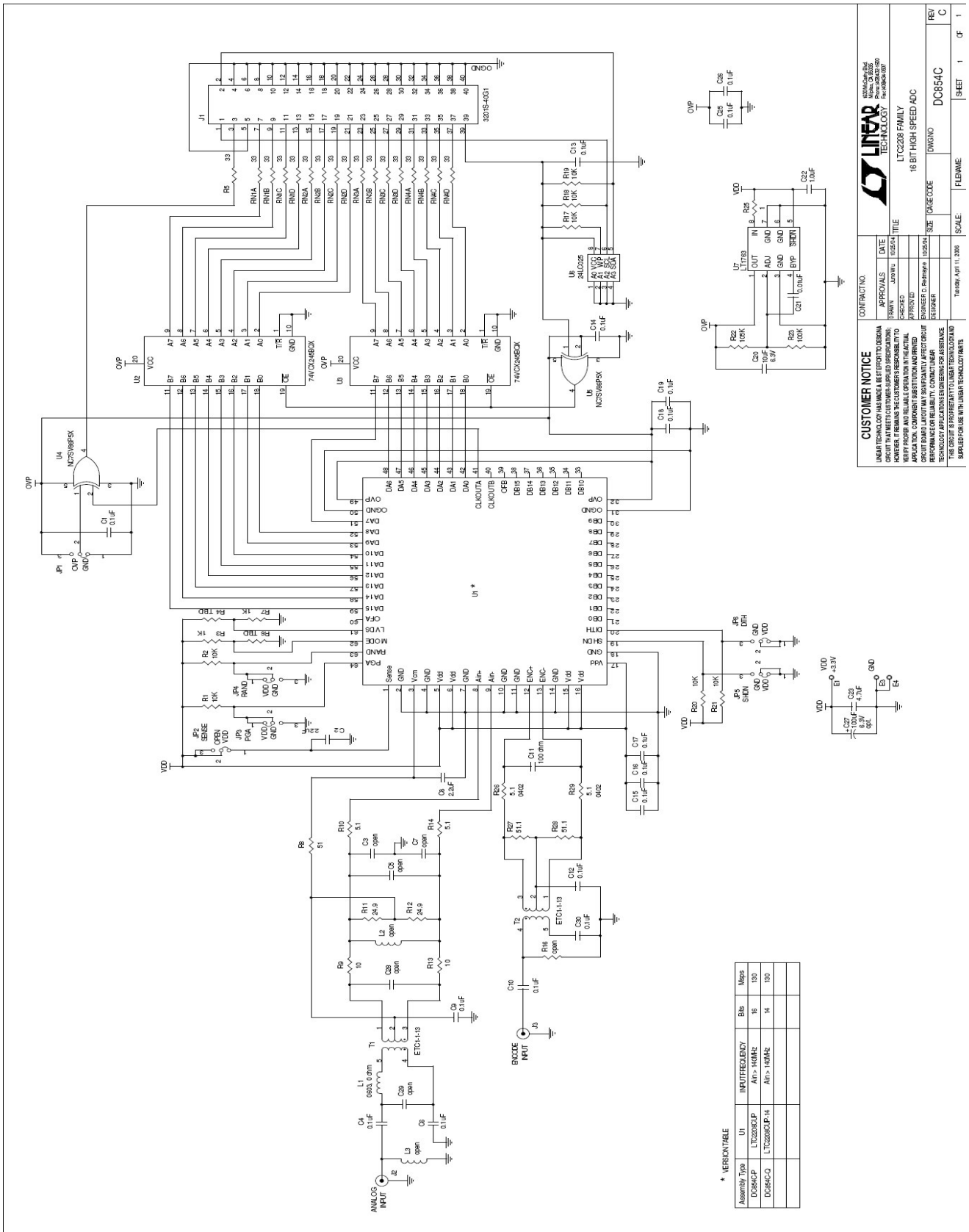
Alignment: Left-16

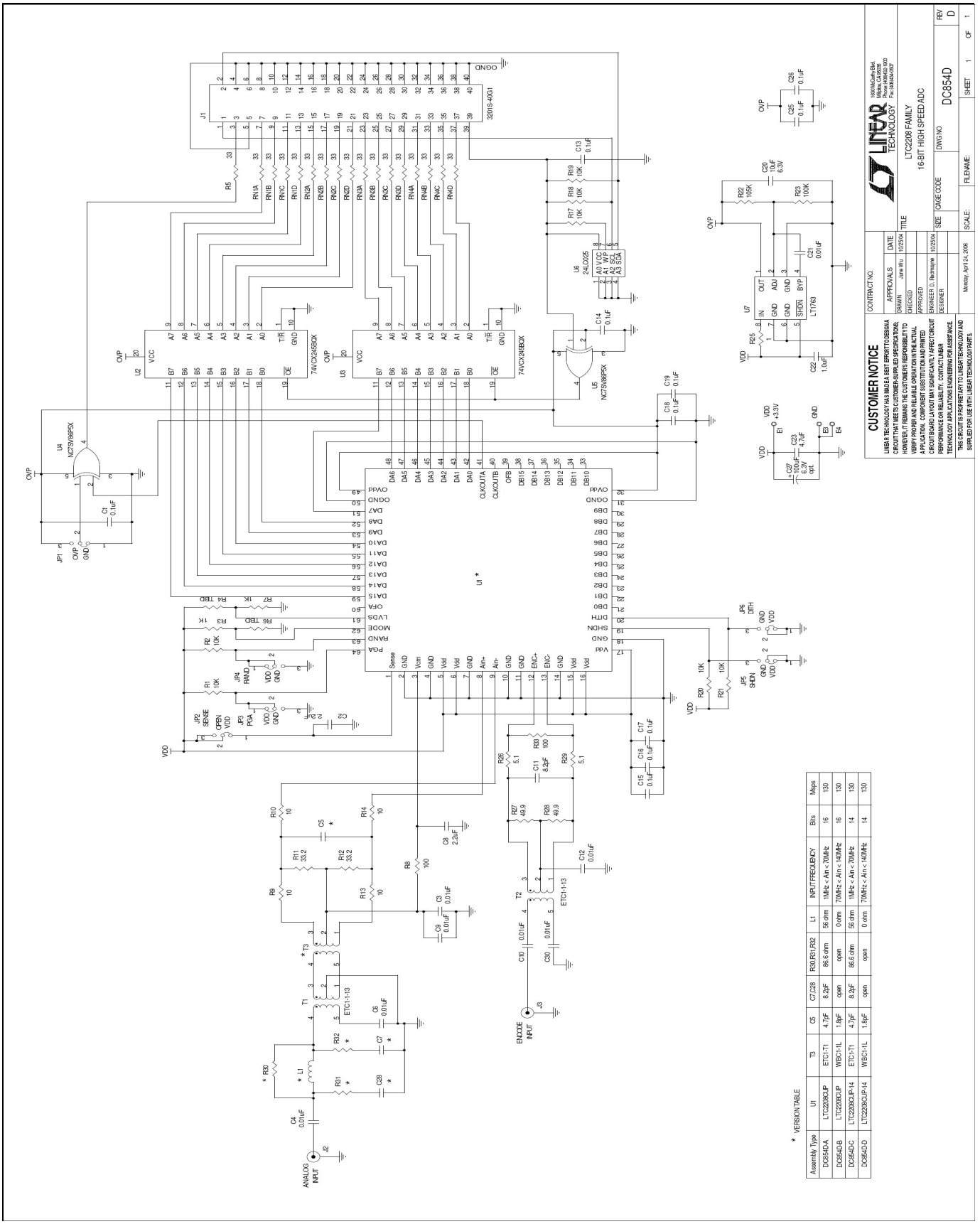
Bipolar (2's complement)

Positive clock edge

Type: CMOS

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC718 Quick Start Guide and in the online help available within the *PScope* program itself.


CUSTOMER NOTICE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS
LINEAR TECHNOLOGY
LTC2208 FAMILY
16 BIT HIGH SPEED ADC
DC854C
* VERSION TABLE
Assembly Type | U1 | INPUT FREQUENCY | Bits | Msps
DC854C-P | LTC2208CUP | Ain> 140MHz | 16 | 130
DC854C-Q | LTC2208CUP-14 | Ain> 140MHz | 14 | 130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CONTRACT NO.
APPROVALS
DRAWN Jane Wu 10/25/04
CHECKED
APPROVED
ENGINEER D. Reinmuth 10/25/04
DESIGNER
Monday, April 24, 2006
LINEAR TECHNOLOGY
1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408)432-1900 Fax: (408)434-0507
LTC2208 FAMILY
16-BIT HIGH SPEED ADC
SIZE
CAGE CODE
DWG NO
DC854D
REV D
SCALE:
FILENAME:
SHEET 1 OF 1
* VERSION TABLE
Assembly Type | U1 | T3 | C5 | C7,C28 | R30,R31,R32 | L1 | INPUT FREQUENCY | Bits | Msps
DC854D-A | LTC2208CUP | ETC1-T1 | 4.7pF | 8.2pF | 86.6 ohm | 56 ohm | 1MHz < Ain < 70MHz | 16 | 130
DC854D-B | LTC2208CUP | WBC1-1L | 1.8pF | open | open | 0 ohm | 70MHz < Ain < 140MHz | 16 | 130
DC854D-C | LTC2208CUP-14 | ETC1-T1 | 4.7pF | 8.2pF | 86.6 ohm | 56 ohm | 1MHz < Ain < 70MHz | 14 | 130
DC854D-D | LTC2208CUP-14 | WBC1-1L | 1.8pF | open | open | 0 ohm | 70MHz < Ain < 140MHz | 14 | 130