HMC305SLP4E

v01.1015

GLITCH FREE 0.5 dB 5-BIT SERIAL CONTROL SILICON DIGITAL ATTENUATOR, 0.4 - 7.0 GHz

Typical Applications

The HMC305SLP4E is ideal for both RF and IF applications:

- Cellular Infrastructure
- Wireless Infrastructure
- Microwave Radio & VSAT
- Test Instrumentation

Features

Glitch Free State Transitions

0.5 dB LSB Steps to 15.5 dB

TTL/CMOS Compatible Serial Data Interface

SPI Compatible Serial Output

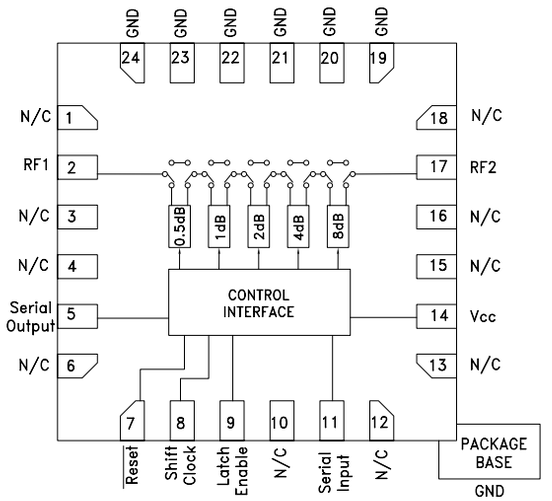
Excellent Attenuation Accuracy: ± 0.25 dB Typical Bit Error

Single + 3.3V to 5V Supply

ESD rating: Class 2 (2kV HBM)

Drop-in Replacement for HMC305ALP4E

Functional Diagram



General Description

The HMC305SLP4E is a broadband 5-bit positive control Silicon IC digital attenuator with CMOS compatible serial-to-parallel driver package in a leadless QFN 4x4 mm SMT package. Covering 0.4 to 6 GHz, the insertion loss is typically less than 1.6 dB. The attenuator bit values are 0.5 (LSB), 1, 2, 4, and 8 dB for a total attenuation of 15.5 dB. Attenuation accuracy is excellent at ±0.25 dB typical with an IIP3 of up to +52 dBm. Five bit serial control words are used to select each attenuation state. A single Vcc bias of +3.3V to +5V is required.

Electrical Specifications, T_A = +25° C, Vcc = +3.3V to +5V

Parameter	Frequency	Min.	Typical	Max.	Units
Insertion Loss	0.4 - 1.4 GHz 1.4 - 2.3 GHz 2.3 - 2.7 GHz 2.7 - 3.8 GHz 3.8 - 6.0 GHz 6.0 - 7.0 GHz		1.0 1.1 1.2 1.3 1.6 1.8	1.5 2.0 2.3 2.5 2.5 2.5	dB dB dB dB dB dB
Attenuation Range	0.4 - 7.0 GHz		15.5		dB
Return Loss (RF1 & RF2, All Atten. States)	0.4 - 1.4 GHz 1.4 - 2.3 GHz 2.3 - 2.7 GHz 2.7 - 3.8 GHz 3.8 - 6.0 GHz 6.0 - 7.0 GHz		25 25 25 25 20 15		dB dB dB dB dB dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States	0.4 - 0.9 GHz 0.9 - 2.2 GHz 2.2 - 3.8 GHz 6.0 - 7.0 GHz	± (0.5 +5% of Atten. Setting) Max ± (0.3 +4% of Atten. Setting) Max ± (0.5 +5% of Atten. Setting) Max ± (0.5 +5% of Atten. Setting) Max			dB dB dB dB
Input Power for 0.1 dB Compression	0.4 - 6.0 GHz		28		dBm
Input Third Order Intercept Point (Two-tone Input Power = 16 dBm Each Tone)	0.4 - 3.8 GHz 3.8 - 6.0 GHz 6.0 - 7.0 GHz		52 50 48		dBm dBm dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (Latch Enable to 10/90% RF)	0.4 - 7.0 GHz		70 160		ns ns

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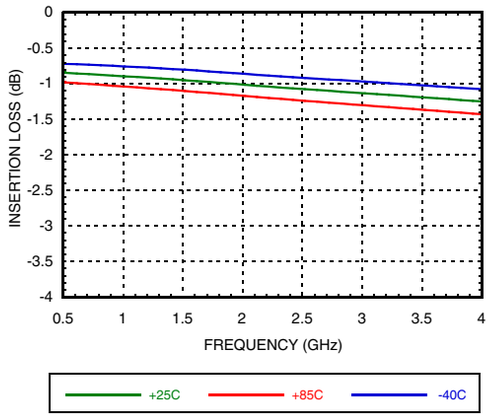
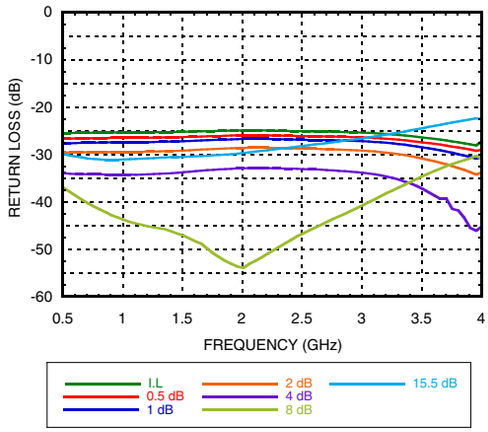
Frequency Response Plots 0.5 to 4 GHz

Insertion Loss



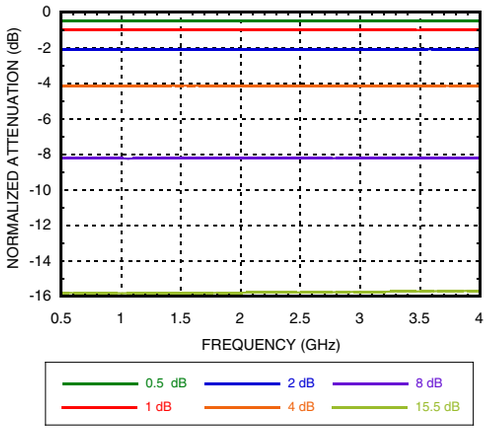
Return Loss RF1, RF2

(Only Major States are Shown)

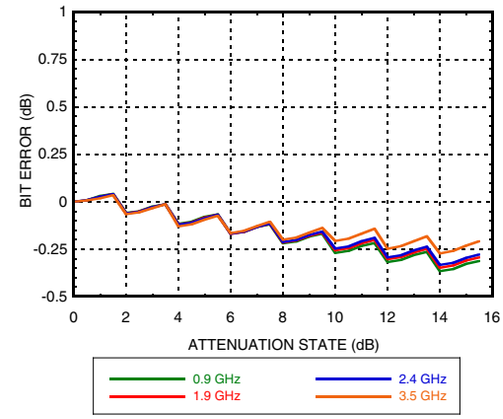


Normalized Attenuation

(Only Major States are Shown)

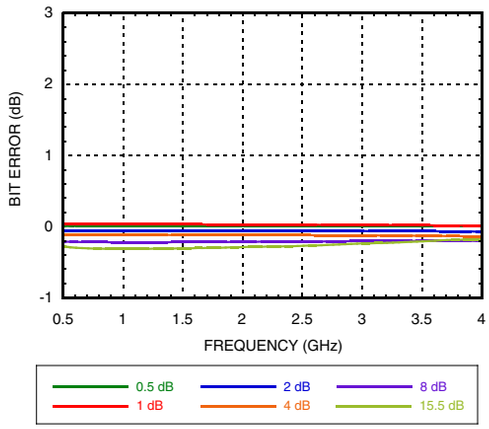


Bit Error vs. Attenuation State



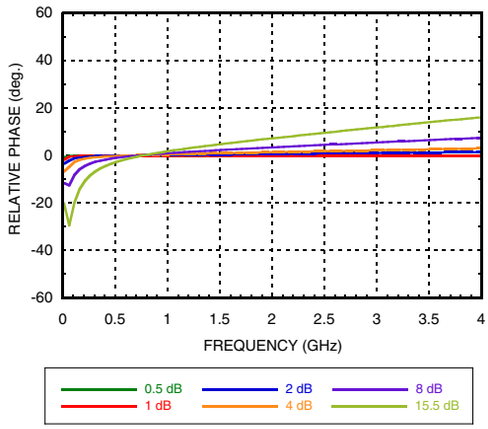
Bit Error vs. Frequency

(Only Major States are Shown)



Relative Phase vs. Frequency

(Only Major States are Shown)



Note: All Data Typical Over Voltage (+3V to +5V) & Temperature (-40°C to +85°C).

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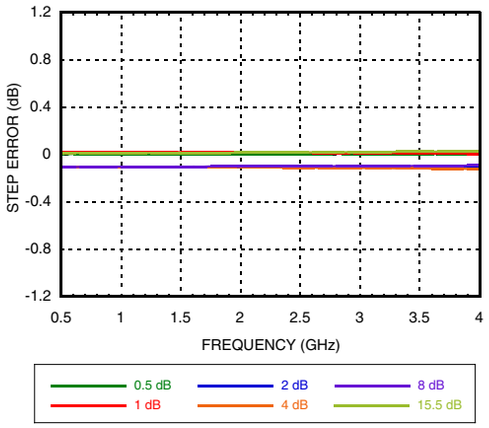
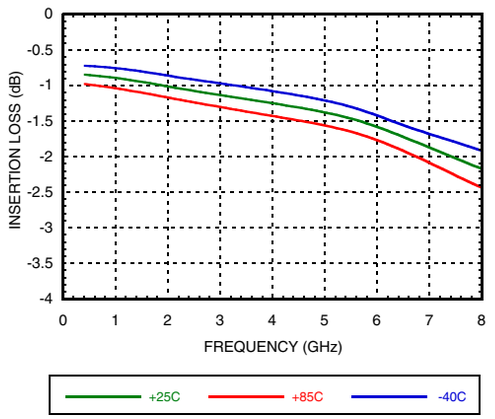
Step Error vs. Frequency



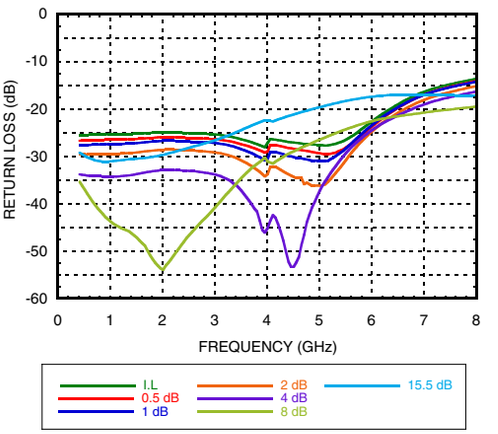
Frequency Response Plots 0.4 to 8 GHz

Insertion Loss



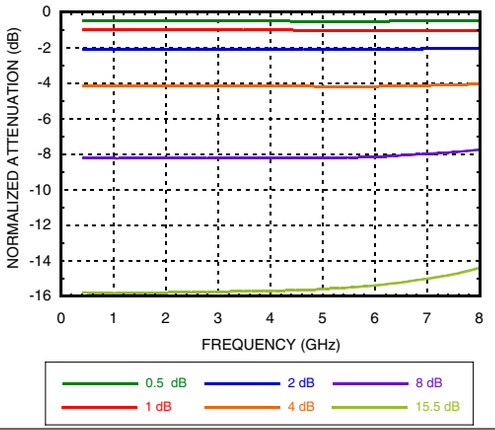
Return Loss RF1, RF2

(Only Major States are Shown)

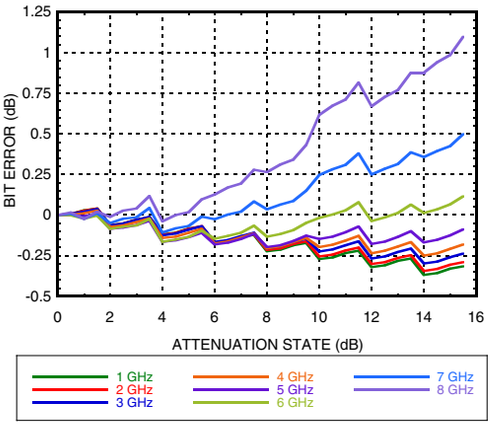


Normalized Attenuation

(Only Major States are Shown)



Bit Error vs. Attenuation State



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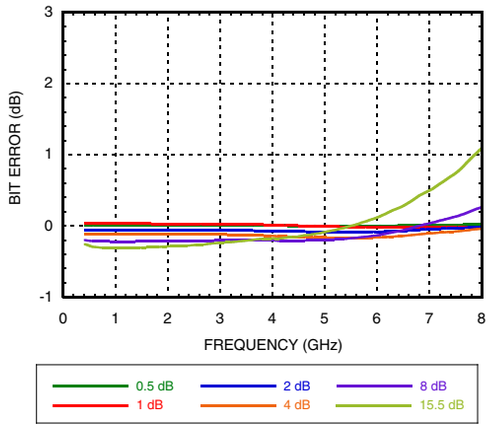
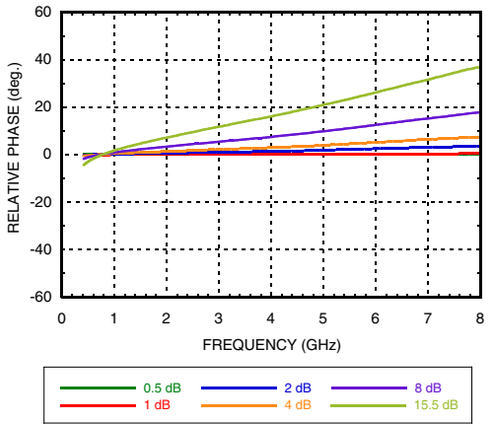
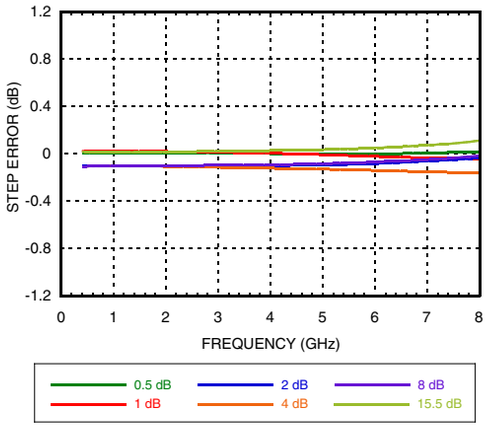
Bit Error vs. Frequency
(Only Major States are Shown)



Relative Phase vs. Frequency
(Only Major States are Shown)



Step Error vs. Frequency



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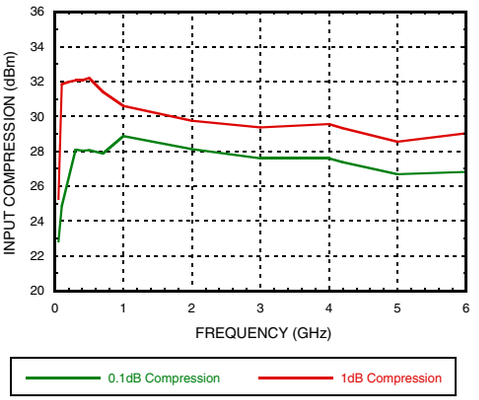
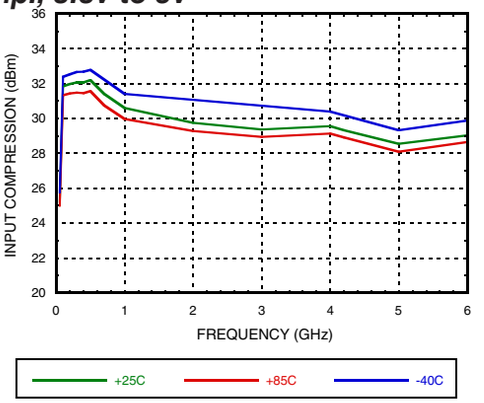
Power Handling Plots 0.1 to 6 GHz

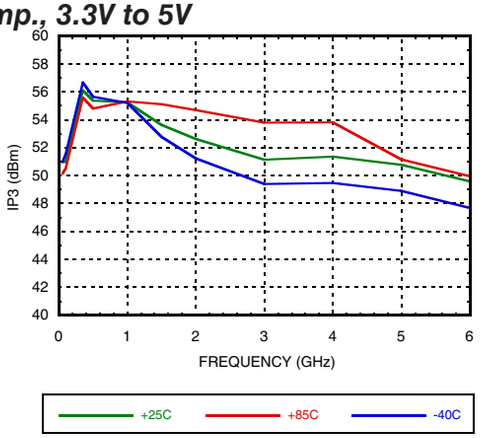
0.1 dB and 1 dB Input Compression Point, 3.3V to 5V



1 dB Input Compression Point, Over Temp., 3.3V to 5V



Input Third Order Intercept Point over Temp., 3.3V to 5V



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Timing

Parameter	Symbol	Vcc = +5V		Vcc = +3V		Units
		Min.	Max.	Min.	Max.	
Serial Input Setup Time	ts	20	-	100	-	ns
Hold time from Serial Input to Shift Clock	th	0	-	5	-	ns
Setup time from Shift Clock to Latch Enable	tlsup	40	-	100	-	ns
Propagation delay, Latch Enable to C0.5 through C8	tpd	-	30	-	70	ns
Setup time from Reset to Shift Clock	-	20	-	50	-	ns
$\overline{\text{Clock}}$ Frequency (1/tclk)	fclk	-	30	-	10	MHz

Digital Control Voltages

State	Vcc = +5V	Vcc = +3V
Low	0 to 1.3V	0 to 0.7V
High	3.5 to 5V	2.3 to 3V

Serial Input Truth Table

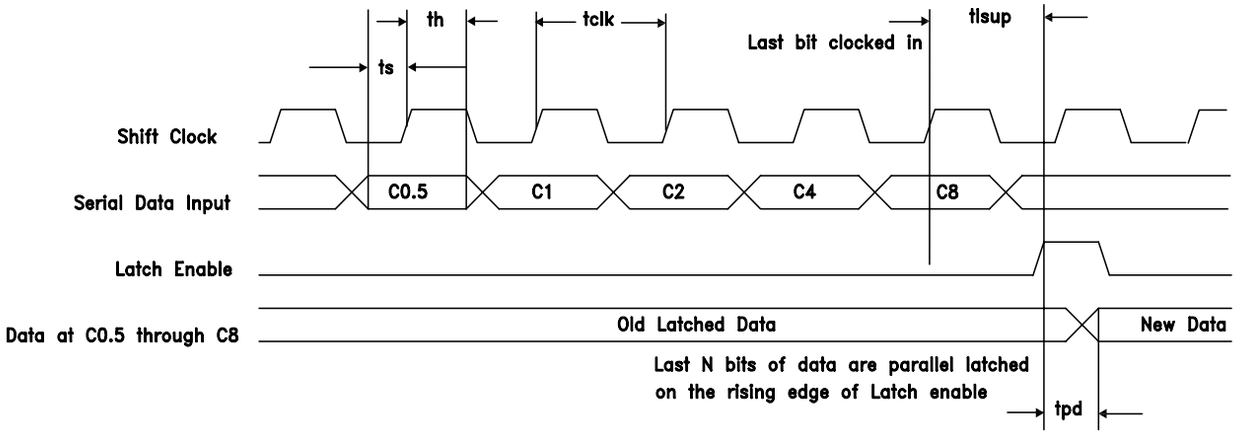
Latch Enable	Shift Clock	$\overline{\text{Reset}}$	Function
X	X	L	Shift register cleared
X	↑	H	Shift register clocked
↑	X	H	Contents of shift register transferred to Digital Attenuator

Truth Table

Serial Control Input					Attenuation Setting RF1 - RF2
C 0.5	C 1	C 2	C 4	C 8	
High	High	High	High	High	Reference I.L.
Low	High	High	High	High	0.5 dB
High	Low	High	High	High	1 dB
High	High	Low	High	High	2 dB
High	High	High	Low	High	4 dB
High	High	High	High	Low	8 dB
Low	Low	Low	Low	Low	15.5 dB Max. Atten.
Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.					

Timing Diagram

Serial data is shifted in on the rising edge of the Shift Clock, LSB first, and is latched on the rising edge of Latch Enable.



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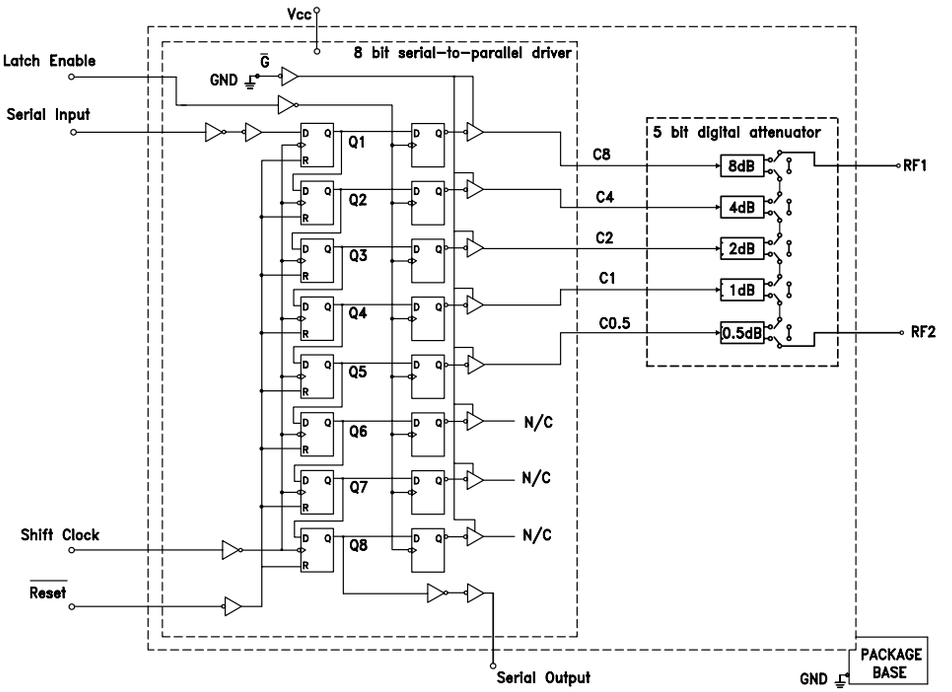
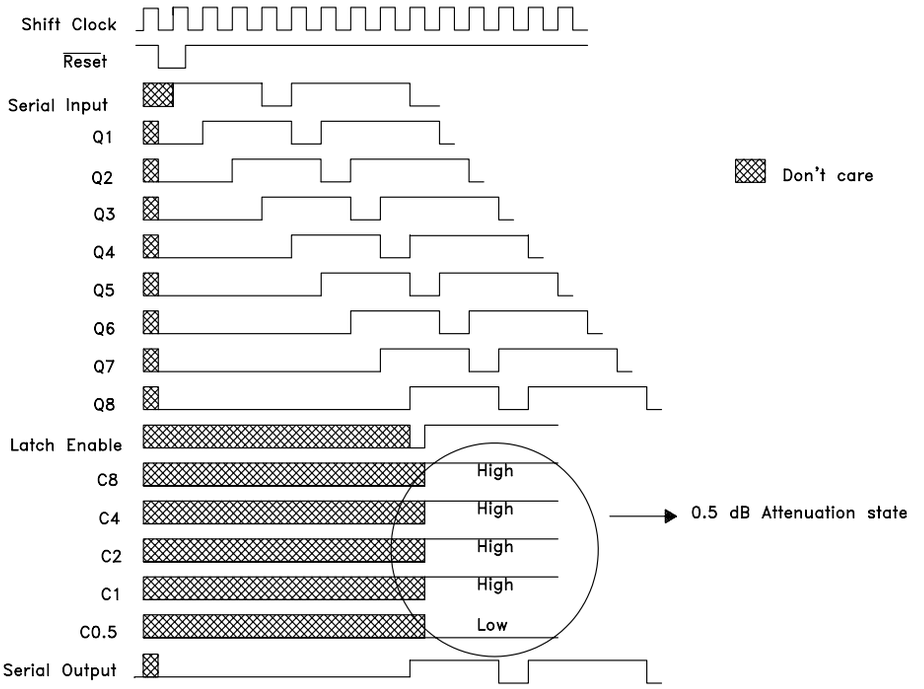
Logic / Functional Diagram



Programming Example to Select 0.5 dB Attenuation State



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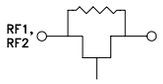
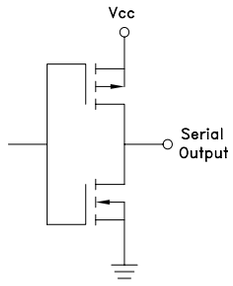
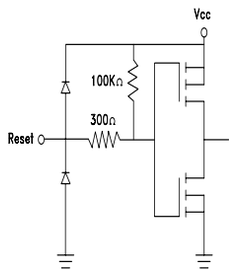
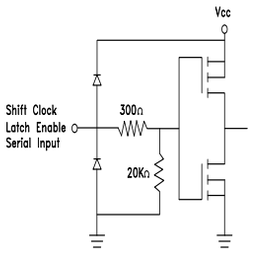
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 4, 6, 10, 12, 13, 15, 16, 18	N/C	These pins are not connected internally. However, all data shown herein was measured with these pins connected to RF/DC Ground.	
2, 17	RF1, RF2	This pin is DC coupled and matched to 50 Ohms Blocking capacitors are required. Select value based on lowest frequency of operation.	
5	Serial Output	Serial data output. Serial input data delayed by 8 clock cycles	
7	$\overline{\text{Reset}}$	See truth table, control voltage table and timing diagram.	
8	Shift Clock		
9	Latch Enable		
11	Serial Input		
14	Vcc	Supply Voltage.	
19 - 24	GND	Package bottom has an exposed metal paddle that must also be connected to RF/DC Ground.	

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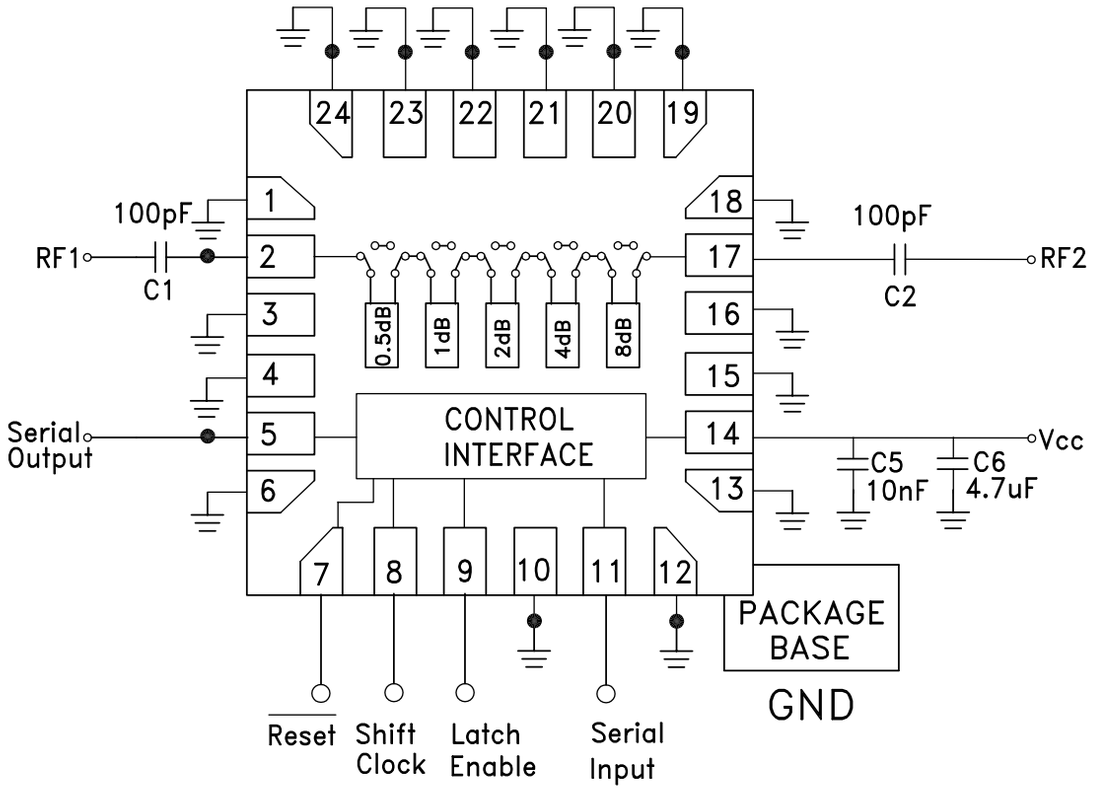
Application Circuit



DC blocking capacitors C1 & C2 are required on RF1 & RF2. Choose C1 = C2 = 100 ~ 300 pF to allow lowest customer specific frequency to pass with minimal loss.

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Absolute Maximum Ratings

Digital Inputs ($\overline{\text{Reset}}$, Shift Clock, Latch Enable & Serial Input)	-0.3 to Vcc + 0.5 V
Bias Voltage (Vcc)	-0.3 to 5.5 V
RF Input Power at 85 °C	+27 dBm
RF Input Power at 105 °C	+26 dBm
Storage Temperature	-65 to +150 °C
Thermal Resistance (at maximum power dissipation)	82 °C/W
ESD Sensitivity (HBM)	Class 2 (2kV)

Operating Range

Digital Inputs ($\overline{\text{Reset}}$, Shift Clock, Latch Enable & Serial Input)	0 to Vcc V
Bias Voltage (Vcc)	+3.0 to 5.4 V
RF Input Power at 85 °C	+24 dBm
RF Input Power at 105 °C	+22.5 dBm
Operating Temperature	-40 to +105 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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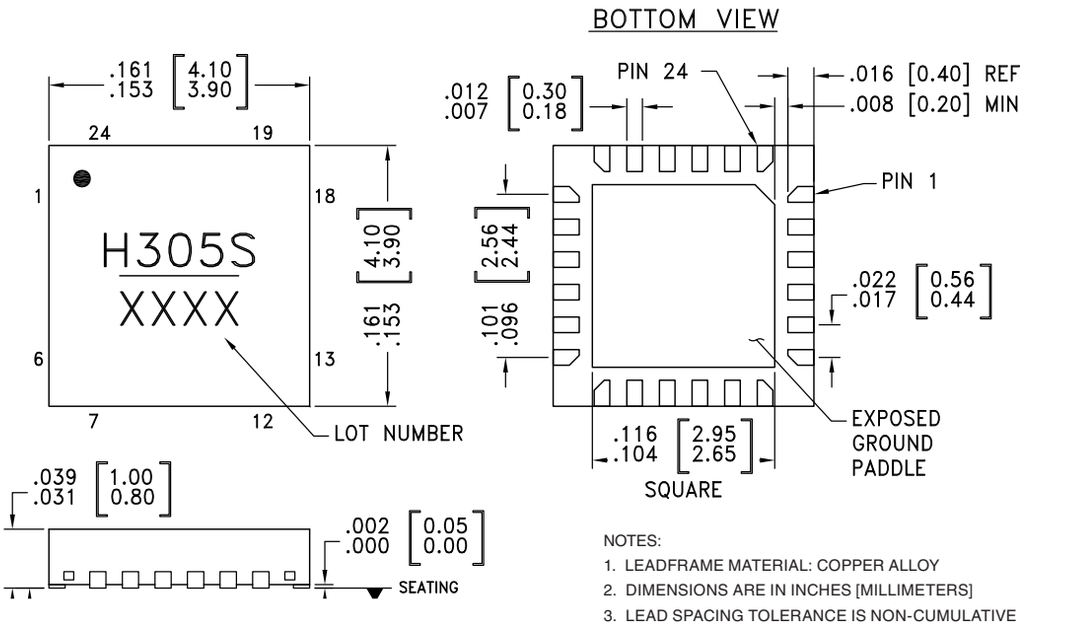
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC305SLP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3 [1]	H305S XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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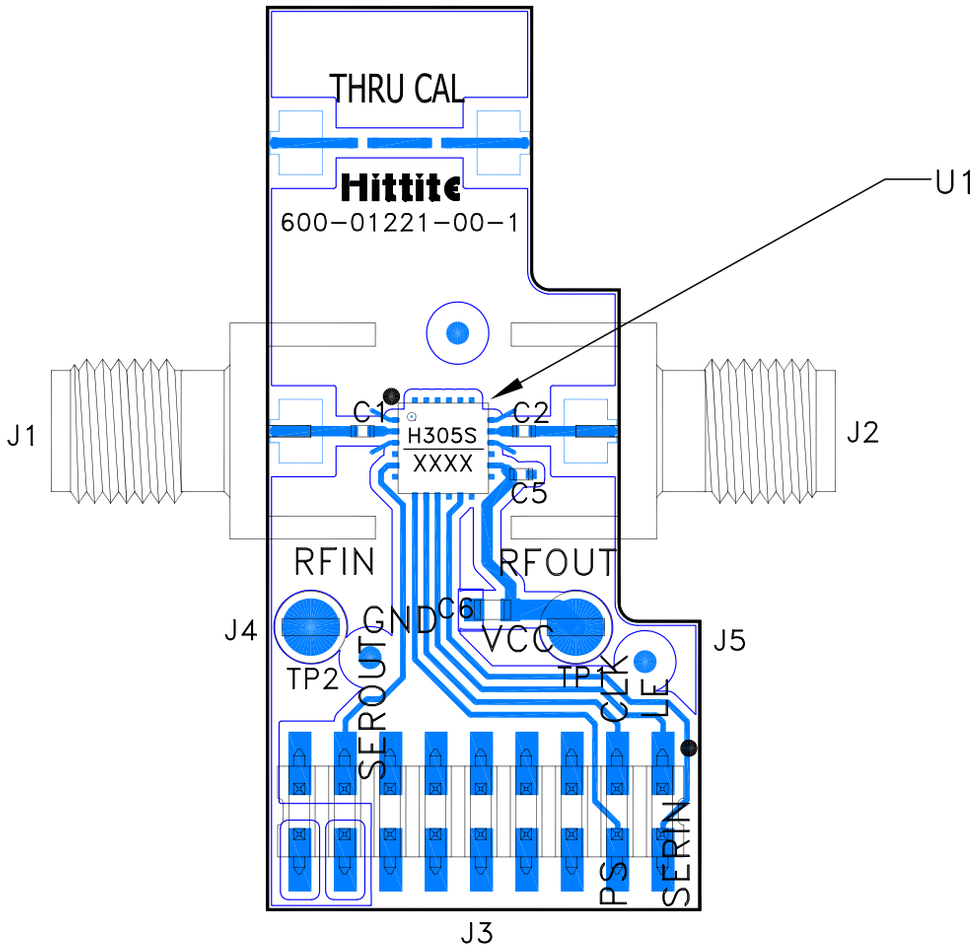
Evaluation Circuit Board



List of Materials for Evaluation PCB EV1HMC305SLP4 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	18 Pin DC Connector
J4, J5	Thru Hole Mount Test Point
C1, C2	100 pF Capacitor, 0402 Pkg.
C5	10000 µF Capacitor, 0402 Pkg.
C6	4.7 uF Capacitor, 0603 Pkg.
U1	HMC305SLP4E Digital Attenuator
PCB [2]	600-01221-00 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed ground paddle should be connected directly to the ground plane similar to that shown below. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Analog Devices Inc. upon request.

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