

#### Features

---

- Low current consumption:  $I_{VDD} < 25\mu A$
- RC oscillator
- Internal reset during power-up and supply voltage drops (POR)
- “Short” trigger window for active mode
- “Long” trigger window for sleep mode
- Cyclical wake-up of the microcontroller in sleep mode
- Trigger input
- Single wake-up input
- Reset output
- Enable output



## 2. Pin Configuration

Figure 2-1. Pinning SO8

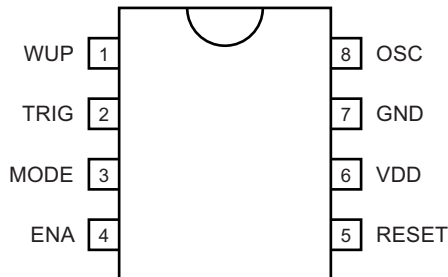


Table 2-1. Pin Description

Pin	Symbol	Function
1	WUP	Wake-up input (pull-down resistor) There is one digitally debounced wake-up input. During the long watchdog window, each signal slope at the input initiates a reset pulse at pin 5.
2	TRG	Trigger input (pull-up resistor) It is connected to the microprocessor's trigger signal.
3	MODE	Mode input (pull-up resistor) The processor's mode signal initiates the switchover between the long and the short watchdog time.
4	ENA	Enable output (push-pull) It is used for the control of peripheral components. It is activated after the processor triggers three times correctly.
5	RESET	Reset output (open drain) Resets the processor in the case of under-voltage condition, a wrong trigger event or if a wake-up event occurs during long watchdog period.
6	VDD	Supply voltage
7	GND	Ground, reference voltage
8	OSC	RC oscillator

### 3. Functional Description

#### 3.1 Supply Voltage, Pin 6

The Atmel® ATA5021 requires a stabilized supply voltage  $V_{DD} = 5V \pm 10\%$  to comply with its electrical characteristics. An external buffer capacitor of  $C = 10nF$  may be connected between pin 6 and GND.

#### 3.2 RC Oscillator, Pin 8

The clock frequency,  $f$ , can be adjusted by the components  $R_1$  and  $C_1$  according to the formula:

$$f = \frac{1}{T} \text{ with}$$

$$T = 0.18 \times (C_1 + C_{\text{board}} + 0.016) + 0.35 + [1.59 - (C_1 + C_{\text{board}} + 0.016)/85] \times R_1 \times (C_1 + C_{\text{board}} + 0.016)$$

$R_1$  (k $\Omega$ ) = external resistor at pin 8

$C_1$  (nF) = external capacitor at pin 8

$C_{\text{board}} = 0.004nF$ ; this is the typical parasitic board capacity.

**Table 3-1. Comparison Table Clock Period Calculation versus Measurement on Test Board**

R1 (k $\Omega$ )	C1 (nF)	Period "T" ( $\mu$ s) by New Formula	Period "T" ( $\mu$ s) by Measurement	Deviation of New Formula versus Measurement
10.00	0.23	4.36	4.33	-0.9%
10.00	0.47	8.20	8.30	1.2%
10.00	1.04	17.26	17.10	-0.9%
10.00	4.75	74.40	74.50	0.1%
10.00	10.49	156.30	152.00	-2.8%
32.91	0.23	13.45	13.25	-1.5%
32.91	0.47	25.99	26.13	0.5%
32.91	1.04	55.57	55.00	-1.0%
32.91	4.75	242.10	241.50	-0.2%
32.91	10.49	509.25	505.00	-0.8%
46.70	0.23	18.92	18.50	-2.2%
46.70	0.47	36.69	36.63	-0.2%
46.70	1.04	78.63	78.25	-0.5%
46.70	4.75	343.03	341.25	-0.5%
46.70	10.49	721.70	700.00	-3.0%
68.00	0.23	27.38	26.75	-2.3%
68.00	0.47	53.22	53.25	0.0%
68.00	1.04	114.25	112.50	-1.5%
68.00	4.75	498.94	497.50	-0.3%
68.00	10.49	1049.85	1020.00	-2.8%
81.20	0.23	32.61	31.88	-2.3%
81.20	0.47	63.47	63.75	0.4%
81.20	1.04	136.32	135.00	-1.0%
81.20	4.75	595.56	592.50	-0.5%
81.20	10.49	1253.21	1240.00	-1.1%

**Table 3-1. Comparison Table Clock Period Calculation versus Measurement on Test Board (Continued)**

R1 (kΩ)	C1 (nF)	Period “T” (μs) by New Formula	Period “T” (μs) by Measurement	Deviation of New Formula versus Measurement
100.00	0.23	40.07	38.88	-3.0%
100.00	0.47	78.07	78.00	-0.1%
100.00	1.04	167.76	164.00	-2.2%
100.00	4.75	733.17	730.00	-0.4%
100.00	10.49	1542.84	1530.00	-0.8%
119.50	0.23	47.81	46.38	-3.0%
119.50	0.47	93.20	93.00	-0.2%
119.50	1.04	200.37	200.25	-0.1%
119.50	4.75	875.90	870.00	-0.7%%
119.50	10.49	1843.26	1835.00	-0.4%%

The clock frequency determines all time periods of the logical part as shown in [Section 7. “Electrical Characteristics” on page 9](#) under the subheading “Timing”.

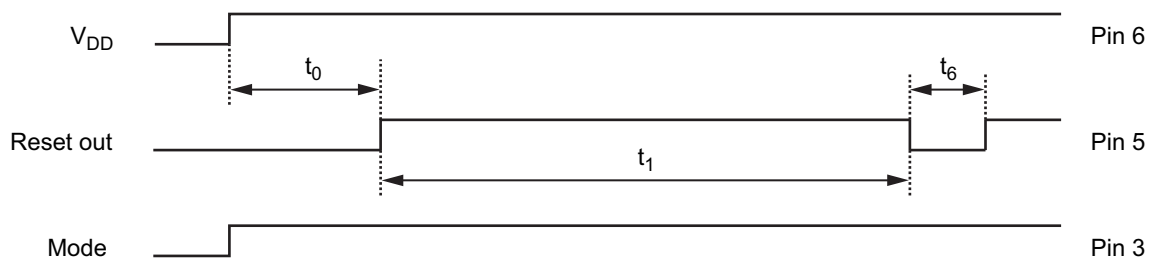
### 3.3 Supply Voltage Monitoring, Pin 5

During ramp-up of the supply voltage and in the case of supply-voltage drops, the integrated power-on reset (POR) circuitry sets the internal logic to a defined basic status and generates a reset pulse at the reset output, pin 5. A hysteresis in the POR threshold prevents the circuit from oscillating. During ramp-up of the supply voltage, the reset output stays active for a specified period of time ( $t_0$ ) in order to bring the microcontroller into its defined reset status (see [Figure 3-1 on page 5](#)).

### 3.4 Switch-over Mode Time, Pin 3

The switch-over mode time enables the synchronous operation of microcontroller and watchdog. When the power-on reset time has elapsed, the watchdog has to be switched to monitoring mode by the microcontroller by a “low” signal transmitted to the mode pin (pin 3) within the time-out period,  $t_1$ . If the low signal does not occur within  $t_1$  (see [Figure 3-1 on page 5](#)), the watchdog generates a reset pulse,  $t_6$ , and  $t_1$  starts again. Microcontroller and watchdog are synchronized with the switch-over mode time,  $t_1$ , each time a reset pulse is generated.

**Figure 3-1. Power-on Reset and Switch-over Mode**



## 3.5 Microcontroller in Active Mode

### 3.5.1 Monitoring with the “Short” Trigger Window

After the switch-over mode, the watchdog operates in short watchdog mode and expects a trigger pulse from the microcontroller within the defined time window,  $t_3$ , (enable time). The watchdog generates a reset pulse which resets the microcontroller if:

- the trigger pulse duration is too long
- the trigger pulse is within the disable time,  $t_2$
- there is no trigger pulse

Figure 3-2 shows the pulse diagram with a missing trigger pulse.

**Figure 3-2. Pulse Diagram with no Trigger Pulse during the Short Watchdog Time**

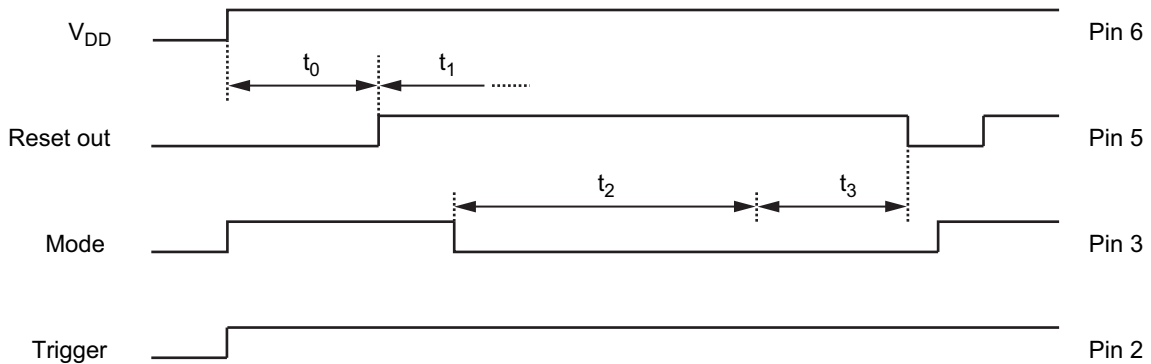
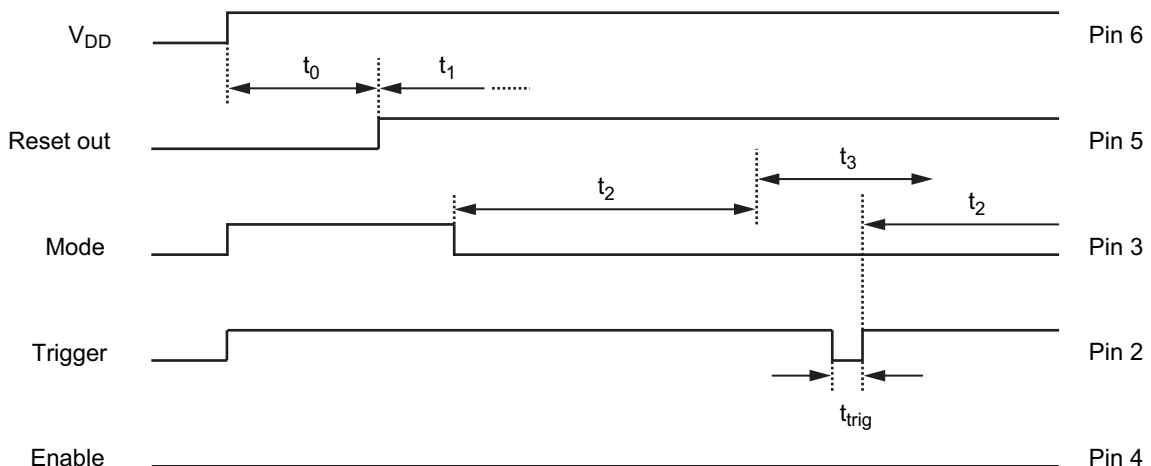


Figure 3-3 shows a correct trigger sequence. The positive edge of the trigger signal starts a new monitoring cycle with the disable time,  $t_2$ . To ensure correct operation of the microcontroller, the watchdog needs to be triggered three times correctly before it sets its enable output. This feature is used to activate or deactivate safety-critical components, which have to be switched to a certain condition (emergency status) in the case of a microcontroller malfunction. As soon as there is an incorrect trigger sequence, the enable signal is reset and it takes a sequence of three correct triggers before enable is active. For proper operation, the trigger pulse duration must be longer than the input signal debounce time (see item 4.2 in Section 7. “Electrical Characteristics” on page 9) and must not exceed the maximum duration of 45 clock cycles (see item 4.4 in Section 7. “Electrical Characteristics” on page 9).

**Figure 3-3. Pulse Diagram of a Correct Trigger Sequence during the Short Watchdog Time**



## 3.6 Microcontroller in Sleep Mode

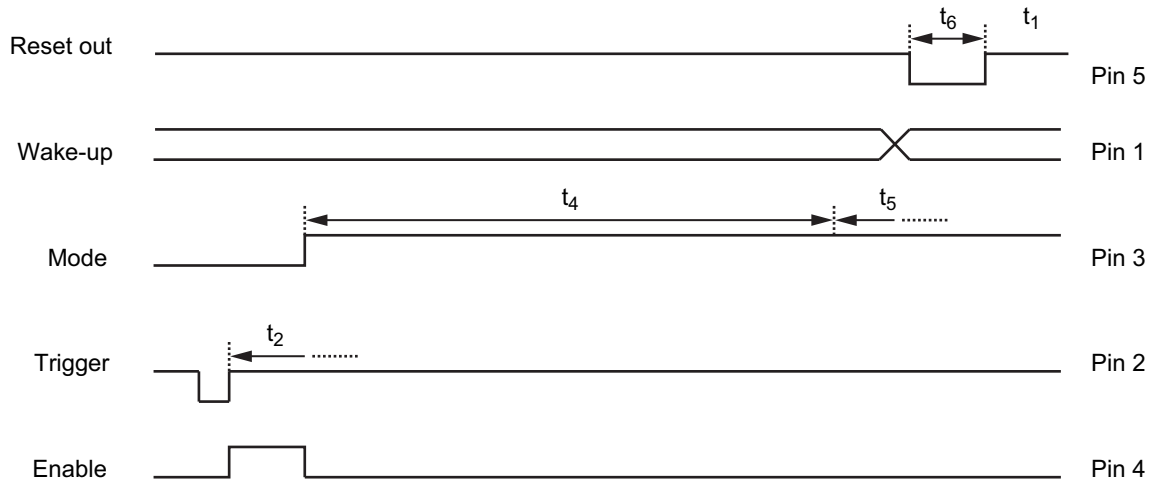
### 3.6.1 Monitoring with the “Long” Trigger Window

The long watchdog mode allows cyclical wake-up of the microcontroller during sleep mode. As in short watchdog mode, there is a disable time,  $t_4$ , and an enable time,  $t_5$ , in which a trigger signal is accepted. The watchdog can be switched from the short trigger window to the long trigger window with a “high” potential at the mode pin (pin 3). In contrast to the short watchdog mode, the time periods are now much longer and the enable output remains inactive so that other components can be switched off to effect a further decrease in current consumption. As soon as a wake-up signal at the wake-up input (pins 1) is detected, the long watchdog mode ends, a reset pulse wakes-up the sleeping microcontroller and the normal monitoring cycle starts with the mode switch-over time.

Figure 3-4 shows the switch-over from the short to the long watchdog mode. The wake-up signal during the enable time,  $t_5$ , activates a reset pulse,  $t_6$ .

The watchdog can be switched back from the long to the short watchdog mode with a low potential at the mode pin (pin 3).

Figure 3-4. Pulse Diagram of the Long Watchdog Time



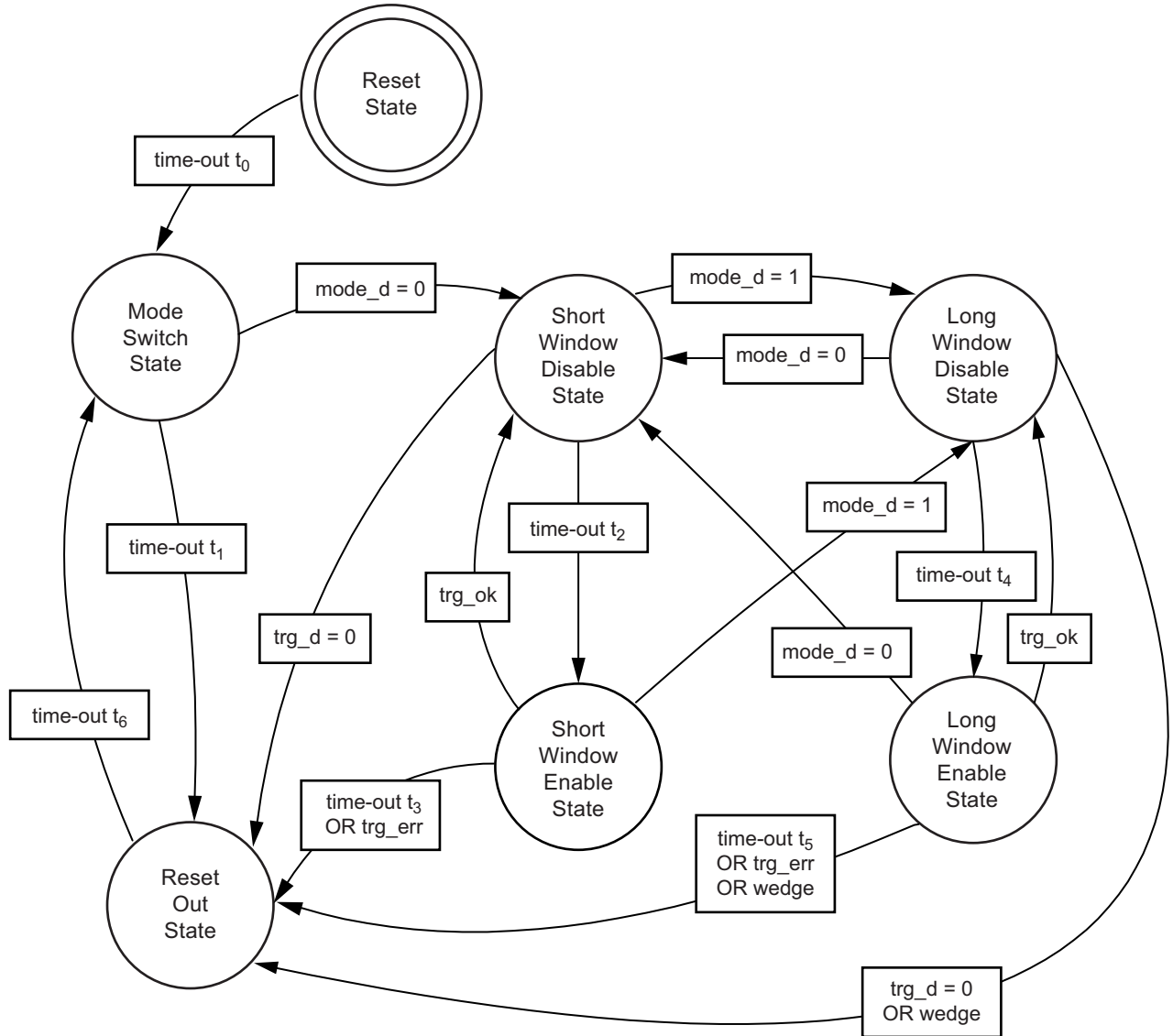
### 3.7 Reset-Out, Pin 5

The Reset-out pin functionality is guaranteed for supply voltage down to 1V. In case of a voltage drop, the microcontroller gets a reset up to that value.

## 4. State Diagram

The kernel of the watchdog is a finite state machine. Figure 4-1 shows the state diagram with all possible states and transmissions. Many transmissions are controlled by an internal timer. The numbers for the time-outs are the same as on the pulse diagrams.

Figure 4-1. State Diagram of the Finite State Machine



Notes:

1. mode\_d and trg\_d are the debounced signals of the MODE and TRG pins
2. wedge is the detection of a signal edge on the wake-up pin after the debouncing time
3. trg\_ok is valid for once cycle after the rising edge on trg\_d
4. trg\_err is valid if the low period of trg\_d is too long



## 5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pin	Symbol	Min.	Max.	Unit
Voltage range on pin VDD		$V_{VDD,max}$	-0.4	+6.5	V
Voltage range on pins		$V_{IO,max}$	-0.4	$V_{VDD} + 0.4$	V
Output current		$I_{OUT,max}$	-2	+2	mA
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		$V_{ESD,HBM}$	±2		kV
Ambient temperature range		$T_{amb}$	-40	+125	°C
Storage temperature range		$T_{sto}$	-55	+150	°C

## 6. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal case resistance junction ambient	$R_{thJA}$	180	K/W

## 7. Electrical Characteristics

$V_{VDD} = 5V$ ,  $T_{amb} = -40^{\circ}C$  to  $+125^{\circ}C$ , reference point is pin 7, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
<b>Power Supply</b>									
1.1	Current Consumption	$V_{VDD} = 5V$ $R_1 = 66k\Omega$ $C_1 = 470pF$	6	$I_{VDD}$			25	$\mu A$	A
1.2	Power-on-reset	Release reset state with rising supply voltage	6	$V_{POR1}$	3.9		4.5	V	A
1.3		Get reset state with falling supply voltage	6	$V_{POR2}$	3.8		4.4	V	A
1.4	POR hysteresis		6	$V_{POR,hys}$	40		200	mV	A
1.5	Reset Level for low $V_{DD}$	$V_{VDD} = 1V$ to $V_{POR1}$ $I_{RTO} = 300\mu A$	5	$V_{RST}$			0.1	$V_{VDD}$	A
<b>Inputs</b>									
2.1	Logical “high”	$V_{VDD} = 5V$	1, 2, 3	$V_{IH}$	3.4			V	A
2.2	Logical “low”	$V_{VDD} = 5V$	1, 2, 3	$V_{IL}$			1.6	V	A
2.3	Hysteresis	$V_{VDD} = 5V$	1, 2, 3	$V_{IN,hys}$	0.6	1	1.4	V	A
2.4	Pull-down current	$V_{IN} = 5V$ $V_{VDD} = 5V$	1	$I_{PD}$	5		20	$\mu A$	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

- Notes:
1. Frequency deviation also depends on the tolerances of the external components
  2. Cycle = Period of clock frequency (see [Section 3.2 on page 4](#))

## 7. Electrical Characteristics (Continued)

$V_{VDD} = 5V$ ,  $T_{amb} = -40^{\circ}C$  to  $+125^{\circ}C$ , reference point is pin 7, unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.5	Pull-up current	$V_{IN} = 0V$ $V_{VDD} = 5V$	2, 3	$I_{PU}$	-20		-5	$\mu A$	A
<b>Outputs</b>									
3.1	Maximum output current		4, 5	$I_{OUT}$	-2		+2	mA	C
3.2	Logical output "low"	$I_{OUT} = 1mA$	4, 5	$V_{OL}$			0.2	V	A
3.3	Logical output "high"	$I_{OUT} = -1mA$	4	$V_{OH}$	$V_{VDD} - 0.2$			V	A
3.4	Leakage current	$V_{OUT} = 5V$	5	$I_{leak}$			2	$\mu A$	A
<b>Timing</b>									
4.1	Frequency deviation <sup>(1)</sup>	$R_1 = 66k\Omega$ $C_1 = 470pF$ $V_{VDD} = 4.5V$ to $5V^{(2)}$	8	$f_{dev}$			5	%	C
4.2	Debounce time		2,3	$t_{deb1}$	3		4	Cycle	D
4.3			1	$t_{deb2}$	96		128	Cycle	D
4.4	Maximum trigger pulse length		3	$t_{trgmax}$		45		Cycle	D
4.5	Power-up reset time			$t_0$		201		Cycle	D
4.6	Switch-over mode time			$t_1$		1112		Cycle	D
4.7	Disable time	Short watchdog window		$t_2$		130		Cycle	D
4.8	Enable time	Short watchdog window		$t_3$		124		Cycle	D
4.9	Disable time	Long watchdog window		$t_4$		71970		Cycle	D
4.10	Enable time	Long watchdog window		$t_5$		30002		Cycle	D
4.11	Reset-out time			$t_6$		40		Cycle	D

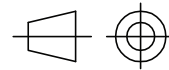
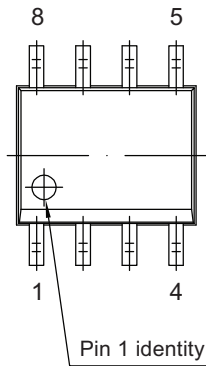
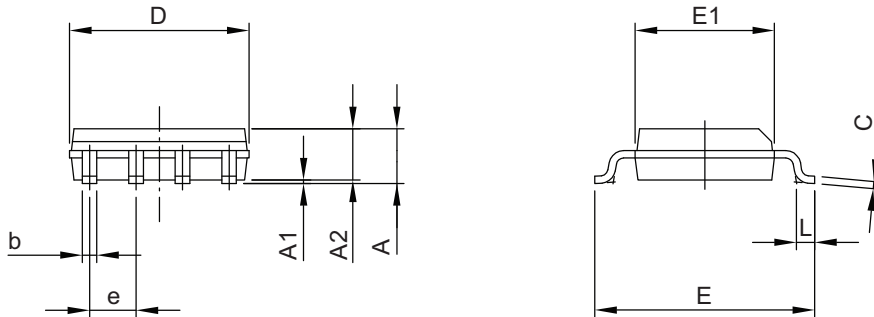
\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

- Notes:
1. Frequency deviation also depends on the tolerances of the external components
  2. Cycle = Period of clock frequency (see [Section 3.2 on page 4](#))

## 8. Ordering Information

Extended Type Number	Package	Remarks
ATA5021-GAQW	SO8	Taped and reeled, Pb-free, big reel

## 9. Package Information



technical drawings  
according to DIN  
specifications

Dimensions in mm

COMMON DIMENSIONS				
(Unit of Measure = mm)				
Symbol	MIN	NOM	MAX	NOTE
A	1.5	1.65	1.8	
A1	0.1	0.15	0.25	
A2	1.4	1.47	1.55	
D	4.8	4.9	5	
E	5.8	6	6.2	
E1	3.8	3.9	4	
L	0.4	0.65	0.9	
C	0.15	0.2	0.25	
b	0.3	0.4	0.5	
e		1.27 BSC		

05/08/14

**Atmel** Package Drawing Contact:  
packagedrawings@atmel.com

**TITLE**  
Package: SO8

**GPC**

**DRAWING NO.**  
6.543-5185.01-4

**REV.**  
1

## 10. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9145I-AUTO-10/14	<ul style="list-style-type: none"><li>• Section 8 “Ordering Information” on page 11 updated</li></ul>
9145H-AUTO-08/14	<ul style="list-style-type: none"><li>• Put datasheet in the latest template</li></ul>
9145G-AUTO-09/12	<ul style="list-style-type: none"><li>• Figure 1-1 “Block Diagram with External Circuit” on page 2 updated</li></ul>
9145F-AUTO-01/12	<ul style="list-style-type: none"><li>• Section 3.2 “RC Oscillator, Pin 8” on pages 4 to 5 changed</li><li>• Column “Deviation of New Formula versus Measurement” in Table 3-1 changed</li></ul>
9145E-AUTO-11/11	<ul style="list-style-type: none"><li>• Figure 4-1 “State Diagram of the Finite State Machine” on page 9 changed</li></ul>
9145D-AUTO-05/10	<ul style="list-style-type: none"><li>• Section 3.2 “RC Oscillator, Pin 8” on pages 4 to 5 changed</li></ul>
9145C-AUTO-09/09	<ul style="list-style-type: none"><li>• Section 3.2 “RC Oscillator, Pin 8” on page 4 changed</li><li>• El. Char. Table: rows 3.1, 3.2, 3.3 changed</li></ul>
9145B-AUTO-05/09	<ul style="list-style-type: none"><li>• Put datasheet in the newest template</li><li>• Section 3.2 “RC Oscillator, Pin 8” on pages 4 to 6 updated</li><li>• Section 3.5 “Microcontroller in Active Mode” on page 7 updated</li><li>• Section 7 “Electrical Characteristics” numbers 1.1 and 4.1 on pages 10 to 11 updated</li></ul>



**Atmel Corporation** 1600 Technology Drive, San Jose, CA 95110 USA T: (+1)(408) 441.0311 F: (+1)(408) 436.4200 | [www.atmel.com](http://www.atmel.com)

© 2014 Atmel Corporation. / Rev.: Rev.: 9145I-AUTO-10/14

Atmel®, Atmel logo and combinations thereof, Enabling Unlimited Possibilities®, SMART-I.S.™, and others are registered trademarks or trademarks of Atmel Corporation in U.S. and other countries. Other terms and product names may be trademarks of others.

DISCLAIMER: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN THE ATMEL TERMS AND CONDITIONS OF SALES LOCATED ON THE ATMEL WEBSITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS AND PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and products descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

SAFETY-CRITICAL, MILITARY, AND AUTOMOTIVE APPLICATIONS DISCLAIMER: Atmel products are not designed for and will not be used in connection with any applications where the failure of such products would reasonably be expected to result in significant personal injury or death ("Safety-Critical Applications") without an Atmel officer's specific written consent. Safety-Critical Applications include, without limitation, life support devices and systems, equipment or systems for the operation of nuclear facilities and weapons systems. Atmel products are not designed nor intended for use in military or aerospace applications or environments unless specifically designated by Atmel as military-grade. Atmel products are not designed nor intended for use in automotive applications unless specifically designated by Atmel as automotive-grade.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Atmel:](#)

[ATA5021-GAPW](#) [ATA5021-GAQW](#)