NCP1871

Narrow Voltage DC Battery Charger

The NCP1871 is a NVDC switching battery charger designed for 2−3−4 battery cell applications such as ultra books or tablets. It is optimized for use with the mobile computing chipsets, and is also compatible with most mobile solutions.

The NCP1871 is designed around a full NMOS DC to DC controller that brings down the high voltage charger adapter voltage to a regulated system supply that is in the same range as the battery pack voltage. This limits the variation on the system supply voltage, and improves the efficiency of the core converters. The device includes a voltage droop monitor, charger adapter validation and blocking as well as an intelligent battery connection control. The adapter current, charge current and system current are closely monitored and an image is provided to the host. The NCP1871 is fully programmable through an I^2C friendly SMBus Interface.

Features

- SMBus Host−controlled NVDC−1 2S−4S Battery Charge Controller
- Instant−on Works with No Battery or Deeply Discharged Battery
- Automatic Supplement Mode with BATFET Control
- Battery Removal Sensor
- Programmable Switching Frequency
- SMBUS Clock up to 400 kHz (I^2C compatible)
- Programmable Charge Current, Charge Voltage, Input Current Limit with Interrupt Management
  - ♦ ±0.5% Charge Voltage Regulation up to 18.08 V
  - ♦ ±3% Input/Charge Current Regulation up to 8.064 A
- Support Battery LEARN Function
- Support Shipping Mode and Hard System Reset
- Ultra−Low Quiescent Current of 10 μA at OFF Mode and High PFM Light Load Efficiency 80% at 20 mA Load to Meet Energy Star and ErP Lot6
- Full NMOS Solution
- Current and Power Monitoring
- 3.5 mm x 3.5 mm QFN−20 Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Ultrabook
- Notebook
- Tablet PC

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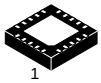


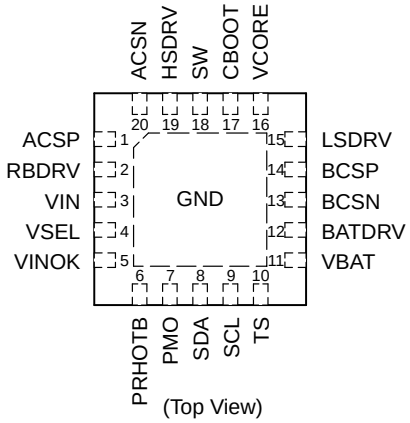
QFN20
MN SUFFIX
CASE 485CP

MARKING DIAGRAM

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1871MNTXG	QFN20 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

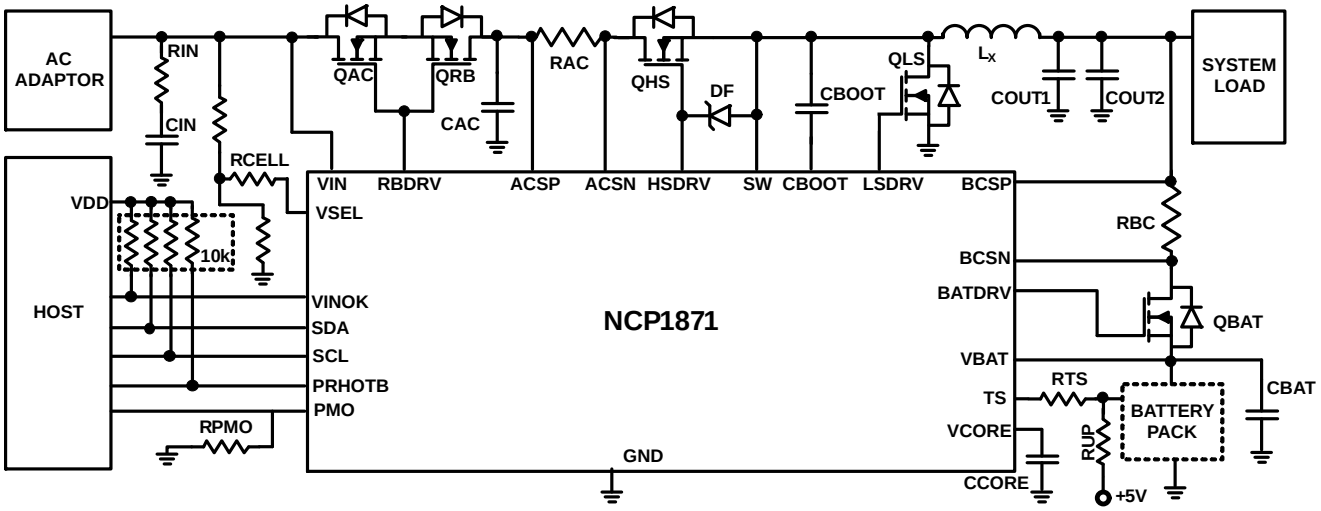


Figure 1. Typical Application Circuit

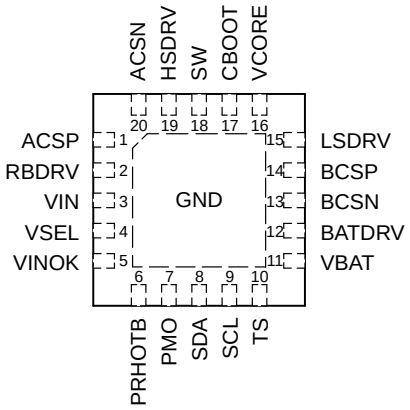


Figure 2. Pin Out Description (Top View)

Table 1. PIN FUNCTIONAL DESCRIPTION

Pin	Name	Type	Description
1	ACSP	ANALOG INPUT	Charger Adapter Current Sense Positive terminal. Use a 10 mΩ sense resistor RAC. Bypass ACSP with a 10 μF capacitor
2	RBDRV	ANALOG OUTPUT	Reverse Blocking FET Driver. Drives the gate of the RBFET NMOS Can also drive gate optional ACFET NMOS.
3	VIN	ANALOG INPUT	Charger Adapter Input. Bypass with a Damping network
4	VSEL	ANALOG INPUT	Adapter detection input. Program adapter valid input threshold by connecting a resistor divider from adapter input to VSEL pin to GND pin. Connect a serial resistance of 220 kΩ to select 3−4 Cells default setting.
5	VINOK	OPEN DRAIN OUTPUT	Charge Adapter Valid Output. Signals the VIN is within the target range. Open drain output requiring an external pull up. Also use for short pulse signal interrupt generation
6	PRHOTB	OPEN DRAIN OUTPUT	Processor Hot Signal Output. Pulled low to reduce processor speed based on BCSP.
7	PMO	ANALOG OUTPUT	Current based indication of system power. Amplified version of the adapter power, the battery power or sum of both.
8	SDA	DIGITAL IN/OUT	Control Bus Data Line.
9	SCL	DIGITAL INPUT	Control Bus Clock Line.
10	TS	ANALOG INPUT	Battery Presence Detection. Connect this pin to the battery thermistor sensor.
11	VBAT	ANALOG IN/OUT	Battery Connection. Bypass with at least 10 μF capacitor.
12	BATDRV	ANALOG OUTPUT	Battery FET Driver.
13	BCSN	ANALOG INPUT	Battery Current Sense Negative Terminal. Use a 10 mΩ sense resistor RBC.
14	BCSP	ANALOG INPUT	Battery Current Sense Positive Terminal. Use a 10 mΩ sense resistor RBC.
15	LSDRV	ANALOG OUTPUT	Low Side Switch Driver. Drives the gate of the DC to DC low side NMOS.
16	VCORE	ANALOG OUTPUT	Core Voltage. Do not connect load on this pin. Bypass with a 2.2 μF capacitor
17	CBOOT	ANALOG IN/OUT	Bootstrap Capacitor Connection.
18	SW	ANALOG OUTPUT	Switching Node. Connection to the 2.2 μH inductor.
19	HSDRV	ANALOG OUTPUT	High Side Switch Driver. Drives the gate of the DC to DC high side NMOS. Supplied from the bootstrap capacitor.
20	ACSN	ANALOG INPUT	Charger Adapter Current Sense Negative terminal. Use a 10 mΩ sense resistor RAC.
−	EXPOSE PAD	GROUND	Internally connected to ground

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VIN , RBDRV (Note 1)	V_{MR_AC}	−0.3 to +30	V
ACSP, ACSN, HSDRV, SW, CBOOT, BCSP, BCSN, BATDRV, VBAT (Note 1)	V_{MR_ACS}	−0.3 to +30	V
TS (Note 1)	V_{MR_DRP}	−0.3 to +7.0	V
CBOOT with respect to SW (JEDEC standard JESD22−A108)	V_{MR_CBOOT}	−0.3 to +7.0	V
LSDRV, VCORE, PRHOTB, PMO, VINOK, VSEL (Note 1)	V_{MR_LV}	−0.3 to +7.0	V
Digital Input: SCL, SDA (Note 1) Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to +7.0 V 20	 V mA
Human Body Model (HBM) ESD Rating are (Note 2)	ESD HBM	1500	V
Charged Device Model (CDM) ESD Rating are (Note 2)	ESD CDM	750	V
Latch up Current (Note 3): All Digital pins(V_{DG}) VINOK, VSEL All others pins.	I_{LU}	 ±10 ±30 ±100	mA
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Maximum Junction Temperature (Note 4)	T_J	−40 to + TSD	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. With Respect to GND. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:. Human Body Model (HBM) ±1.5 kV per JEDEC standard: JESD22−A114. Charged Device Model (CDM) ±750 V per JEDEC standard: JESD22−C101.
3. Latch up Current Maximum Rating: ±100 mA or per ±10 mA JEDEC standard: JESD78 class II.
4. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

Table 3. OPERATING CONDITION

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operational Power Supply		4.5		V_{INOV}	V
V_{DG}	Digital input voltage level		0		5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
I_{SINK}	VINOK sink current				10	mA
C_{IN}	Decoupling input capacitor			4.7		μF
R_{IN}	Damping resistor			2		Ω
C_{AC}	Decoupling Switcher capacitor			10		μF
C_{BOOT}	Bootstrap capacitor			100		nF
C_{CORE}	Decoupling core supply capacitor			2.2		μF
C_{OUT1}, C_{OUT2}	Decoupling system capacitor			47		μF
L_X	Switcher Inductor			2.2		μH
R_{AC}, R_{BC}	Current sense resistor			10		mΩ
$R_{DSONQRB}$, $R_{DSONQHS}$, $R_{DSON\ QLS}$, R_{DSONQB}	RDSON resistance	N−channel MOSFET V_{GS} = 5 V		10		mΩ
C_{GQRB},C_{GQHS}, C_{GQLS}, C_{GQB}	Total Gate Charge			10		nC
$R_{\theta JA}$	Thermal Resistance Junction to Air	(Notes 4 and 6)		50		°C/W
T_J	Junction Temperature Range		−40	25	+125	°C

6. The $R_{\theta JA}$ is dependent on the PCB heat dissipation. Board used to drive this data was a 2s2p JEDEC PCB standard.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −20°C to +85°C and T_J up to + 125°C for V_{IN} between 4.5 V to 22 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 12 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
INPUT VOLTAGE							
V_{INDET}	Presence input detection threshold	V_{IN} rising		3.2	3.5	3.8	V
		Hysteresis			175		mV
V_{INSYS}	Charger mode detection threshold voltage	$V_{IN} – V_{BCSP}$, V_{IN} rising		95	150	200	mV
		$V_{IN} – V_{BCSP}$, V_{IN} falling		10	50	90	mV
V_{INLO}		V_{SEL} rising		1.188	1.2	1.212	V
		Hysteresis		25	50	75	mV
V_{CELL}	Cells detection threshold	V_{SEL} rising		0.4	0.45	0.5	V
		Hysteresis			50		mV
$V_{INMINOK}$	Operating charger valid threshold	V_{IN} rising, Ratio of V_{SYSMIN}		103.4	106	108.6	%
		Hysteresis		101.4	104	106.6	%
V_{INOV}	Valid input high threshold	V_{IN} rising (Note 7)		22	22.5	23	V
		Hysteresis			125		mV
T_{VINOV}	Max Hot Plug Rise time	ACFET present, from 0 to 30 V, no overvoltage on ACSP			10		V/μs
		RBFET only, from 0 to 30 V, no overvoltage on BCSP			10		
INPUT CURRENT LIMITING							
I_{INLIM}	Input current limit	Input Current Limit Range, Average value.		128		8064	mA
		Input Current Limit Default. (Note 8)			3328		mA
		Input Current Granularity			128		mA
		Input Current Accuracy	128 mA to 2048 mA	−64		+64	mA
			2048 mA to 4096 mA	−3		+3	%
T_{IIN}	Current Ramping				128/16		mA/μs
$I_{INSHORT}$	Short Circuit Detect	Input Current Limit ILIM		10	11	12	A
$T_{INSHORT}$	Short Circuit Detect Delay				10		μs
BATTERY AND SYSTEM VOLTAGE							
V_{CHG}	Output voltage range	Programmable		3328		18080	mV
		Default value, (Note 9)			V_{SYSMIN} + V_{SYSOFF}		
	Voltage regulation accuracy	Constant voltage mode, ICHG>=500 mA		−0.5		0.5	%
	Programmable granularity				16		mV
	Voltage Ramping				64/16		mV/μs
V_{SYSOV}	System OVP	VBCSP Rising	VCHG ≤ 9V		10.8		V
			9 V ≤ VCHG ≤ 13.5 V		14.4		V
			VCHG > 13.5 V		21.6		V
	SYSOV Release Threshold	Hysteresis, Ratio of V_{CHG} Rising Edge			102		%
V_{BUCKOV}	Buck Out of Regulation	VBCSP Rising, Ratio of V_{CHG} Rising Edge			104		%
	BUCKOV Release Threshold	Hysteresis			102		%

7. 19 V and 14.5 V versions are available upon request
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BATTERY AND SYSTEM VOLTAGE						
V_{SYSMIN}	Minimum System Voltage Range		3328		17792	mV
	Minimum System Voltage Default	RCELL = 0 Ω (2−3 cells)		7936		mV
		RCELL = 220 kΩ (3−4 cells)		12032		mV
		Hysteresis		50		mV
	Minimum System Voltage Granularity			128		mV
V_{SYSOFF}	System Voltage Regulation Offset	SYSOFF_SEL = 0, Default		384		mV
		SYSOFF_SEL = 1		256		mV
CHARGE CURRENT						
I_{CHG}	Charge current range	Programmable	128		8064	mA
		Default value, (Note 10)		128		mA
	Charge current accuracy	128 mA to 2048 mA	−64		+64	mA
		2048 mA to 8064 mA	−3		3	%
	I^2C Programmable granularity			128		mA
T_{ICHG}	Current Ramping			128/16		mA/μs
I_{EOC}	End of Charge Current Range		128		1024	mA
	End of Charge Current Default			256		mA
	End of Charge Current Granularity			128		mA
	End of Charge Current Accuracy		−64		+64	mA
REVERSE BLOCKING FET						
T_{RBDR}	RBDRV Rise Time	3 nC Load		2		ms
T_{RBDF}	RBDRV Fall Time	10 nC Load		1		μs
R_{RBDL}	RBDRV Output High	Referred to ground			30	V
R_{RBDH}		Referred to VIN, VIN ≥ 9 V	4.45	5	5.5	V
V_{RBDL}	RBDRV Output Low	$V_{IN} < V_{ACSP}$, Referred to VIN		0		V
V_{RBDH}		$V_{IN} > V_{ACSP}$, Referred to ACSP		0		V
VINOK PIN						
V_{OL}	FLAG output low voltage	I_{VINOK} = 3 mA			0.4	V
I_{INOKLK}	Off−state leakage	V_{VINOK} = 5 V			1	μA
BATTERY MOSFET FET and PRECHARGE MODE						
V_{PRERED}	Precharge Current Reduction Range	SYSOFF_SEL = 0, BCSP−VSYSMIN, IBAT(DC) = 0 A.	49		399	mV
$V_{PRESTOP}$	Precharge Current Reduction Range	BCSP−VSYSMIN, IBAT(AC) = 0 A.	0		128	
V_{DRCON}	Battery FET Reconnect Detection Threshold	End of Charge, VBAT−BCSP		256		mV
V_{DOPEN}	Battery FET Re−open Detection Threshold	Supplement, VBAT−BCSP	−1		+5	mV

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BATTERY MOSFET FET and PRECHARGE MODE						
V_{PRE}	Precharge voltage threshold	V_{BAT} rising, Ratio of V_{SYSMIN}		100		%
		Accuracy	−2		+2	%
		Hysteresis		98		%
I_{PREMAX}	Precharge Current Range		128		512	mA
	Precharge Current Default	Default value (Note 11)		512		mA
	Precharge Current Accuracy		−64		+64	mA
V_{BFH}	BATDRV Output High	VBAT ≥ 3.3 V, Referred to VBAT	4.5	5	8	V
V_{BFL}	BATDRV Output Low	Referred to GND	−0.3	0	0.3	V
T_{FBF}	BATDRV Fall Time	From V_{BFH} to V_{BFL}, 10 nC Load		200		μs
T_{FBR}	BATDRV Rise Time	From V_{BFL} to V_{BFH} 3 nC Load, From End of Charge to Supplement mode		2		μs
		From V_{BFL} to V_{BFH}, 3 nC Load.		5		ms
I²C/SMBus						
F_{SCL}	Bus operating frequency		10		400	kHz
T_{I2CTO}	Bus Timeout		25		35	ms
VI_{2CINT}	Peak voltage at SCL line		2.7		5.5	V
V_{I2CIL}	SCL, SDA low input voltage		−0.5		0.5	V
V_{I2CIH}	SCL, SDA high input voltage		1.7		5.5	V
V_{I2COL}	SDA low output voltage	Sink 3 mA	0		0.4	V
BUCK CONVERTER						
F_{SWCHG}	Switching Frequency Range		600		1200	kHz
	Switching Frequency Default			800		kHz
	Switching Frequency Granularity			200		kHz
	Switching Frequency Accuracy		−10		+10	%
F_{SWSMB}	Spread Spectrum Modulation Bandwidth	Ratio of FSW		6		%
F_{SWSMR}	Spread Spectrum Modulation Rate			23		kHz
I_{OUTMAX}	Output Current Capability		8			A
I_{PKMAX}	Maximum peak inductor current			9		A
GENERAL PARAMETERS						
I_{OFF}	OFF Mode quiescent current (Measured on BAT)	PMO_EN = 0, VDROOP_EN = 0, VIN = 0 V, 2~3 Cells			10	μA
		PMO_EN = 0, VDROOP_EN = 0, VIN = 0 V, 4 Cells			12	
I_{QLB}	Drop Detection Quiescent Current (Measured on BAT)	OFF mode. PMO_EN = 0, VDROOP_EN = 1 VIN = 0 V, VBAT> V_{LOBAT}, VDRP_SEL ! = 00, 2~3 Cells			80	μA
		OFF mode. PMO_EN = 0, VDROOP_EN = 1 VIN =0V, VBAT> V_{LOBAT},VDRP_SEL ! = 00, 4 Cells			140	
I_{STBY}	PMO block quiescent current (Measured on BAT)	OFF mode. PMO_EN = 1, VDROOP_EN = 0 VIN = 0 V, VBAT> 4 V			1500	μA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GENERAL PARAMETERS						
E_{ECO}	NCP1871 Efficiency	With Recommended operating condition, VIN = 12 V , VBAT = 8.4 V, PMO_EN = 0, VDROOP_EN = 0 ECO_MODE = 1, 20 mA load		80		%
V_{CORE}	Core supply voltage	VIN > 5.5 V		5		V
V_{UVLO}	System UVLO	VIN or VBAT rising, SMBus register available			4	V
T_{SD}	Thermal Shutdown			135		°C
CURRENT AND POWER MONITORING						
G_{BC}	Battery Current Sense Gain	GBC_SEL = 0, Default		0.2		μA/mV
		GBC_SEL = 1		0.4		μA/mV
A_{BC}	Battery Voltage Sense Scaling			2		μA/V
G_{AC}	Adapter Current Sense Gain			0.2		μA/mV
A_{AC}	Adapter Voltage Sense Scaling			2		μA/V
K_{AC}, K_{BC}	Mixer Gain	GAIN_SEL = 0, Default		250		kA/A^2
		GAIN_SEL = 1		500		kA/A^2
I_{PMO}	Power Monitor Output Current	Full Scale		100		μA
I_{PAC},I_{PBC}	Power Monitor Accuracy per channel	1.00x Full Scale	−5		5	%
		0.10x Full Scale	−8.5		8.5	%
		0.03x Full Scale	−20		20	%
F_{PMO}	Power Monitor Bandwidth			8		kHz
V_{DRPREF}	VDRP Fast Comparator Reference Voltage	DRP_SEL = 00, Relative to V_{SYSMIN}		97		%
		DRP_SEL = 01		5.6		V
		DRP_SEL = 10, Default		5.8		V
		DRP_SEL = 11		6		V
	VDRP Fast Comparator Accuracy		−2.1		+2.1	%
	VDRP Fast Comparator Debounce			2		μs
V_{LOBAT}	VDRP Slow Comparator Detection Level	VLOBAT_REG = 00, Ratio of VDRPREF		OFF		%
		VLOBAT_REG = 01		105		
		VLOBAT_REG = 10, Default		107.5		
		VLOBAT_REG = 11		110		
T_{LBDEB}	VDRP Slow Comparator Debounce			128		ms
I_{LBSK}	PRHOTB Sink Capability	Output 0.4 V	40			mA
T_{LBPS}	Pulse Stretch Duration			10		ms
V_{BAT_RMV}	Battery Removal Detection Threshold	BATRMV_SEL = 0, Default	2.7	2.85	3	V
		BATRMV_SEL = 1	1.5	1.6	1.7	
	Battery Removal Detection time			4		μs
I_{BAT_RMV}	TS Input Leakage				100	nA

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Charging Process

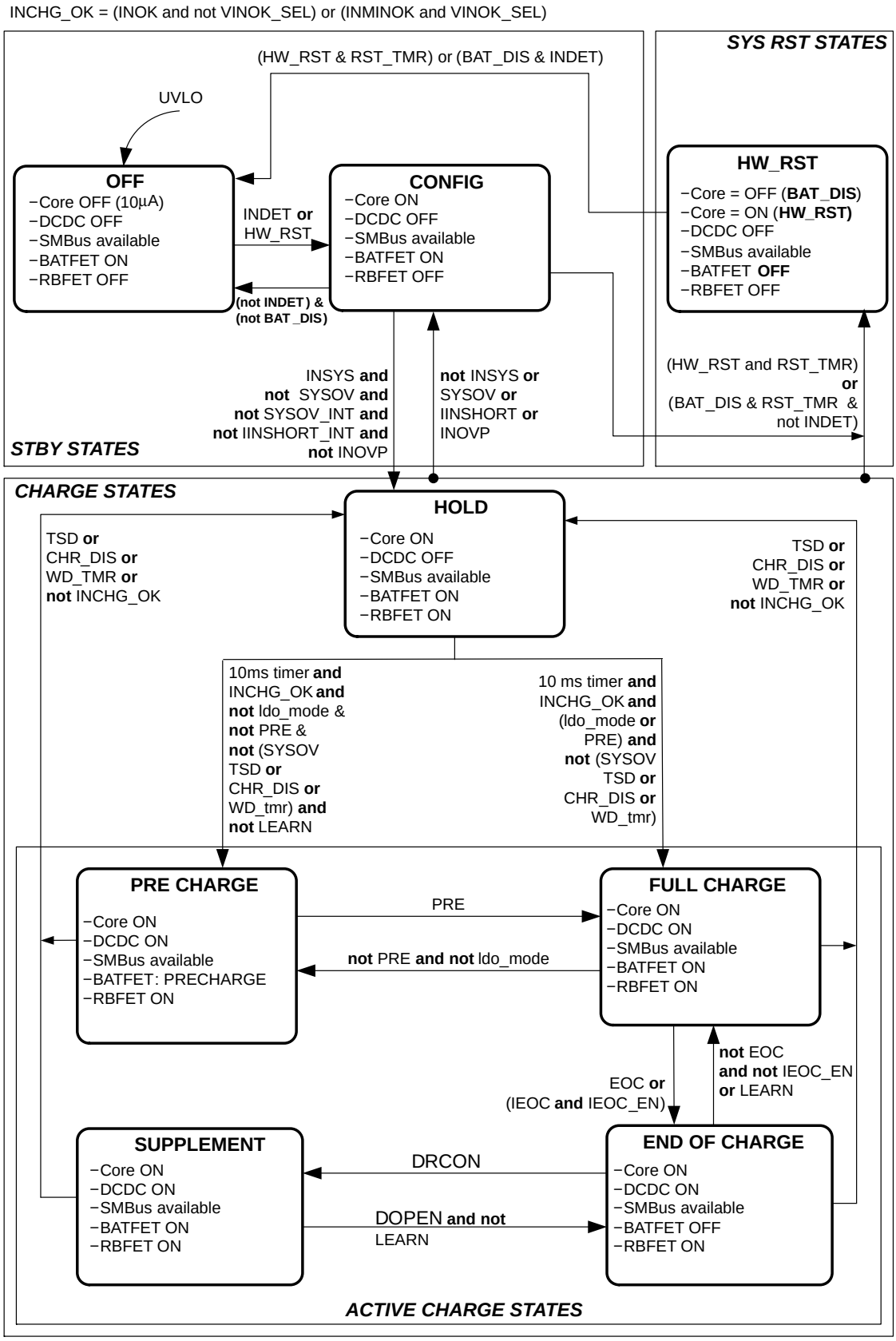


Figure 3. Charging State Machine

Block Diagram

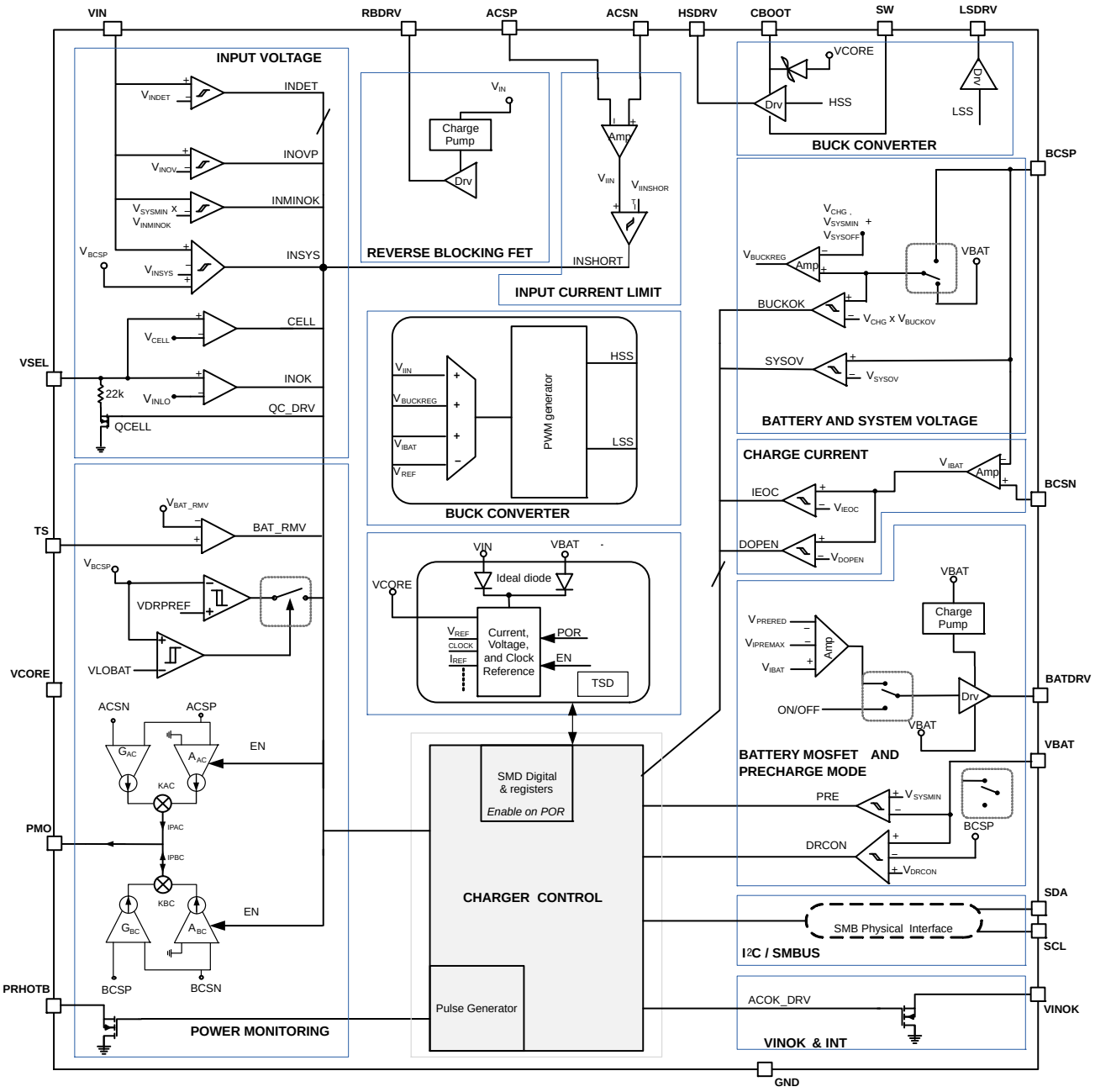


Figure 4. Detailed Block Diagram

SMBUS Registers Map

SMBUS slave address (binary): b0001001x.

ChargeOption Register − Memory Location : 12h					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	RW	POR, TR_OFF	CHR_DIS	0	Charge is suspend when set 1
1	RW	POR, TR_OFF	EOC	0	Set 1 will jump to End of Charge state from FULL charge: signal dictated by the Fuel Gauge
2	RW	POR, TR_OFF	IEOC_EN	0	Set 1 enable the charger end of charge detection
3	RW	POR, TR_OFF	LEARN	0	Set 1 enable the LEARN mode
4	RW	POR, TR_OFF	PMOBAT_EN	0	Set 1 enable the Battery Power monitoring circuitry
5	RW	POR, TR_OFF	PMOAC_EN	0	Set 1 enable the Input Power monitoring circuitry
6	RW	POR, TR_OFF	GAIN_SEL	0	Multiplier Gain selection 0: Full scale 100 W 1: Full scale 50 W
7	RW	POR, TR_OFF	PMO_IMO_SEL	0	0 : PMO selected 1: IMO selected
8	RW	POR, TR_OFF	GBC_SEL	0	0: Battery Current Sense Gain is 10 1: Battery Current Sense Gain is 20
9	RW	POR, TR_OFF	WDTMR_SET[0]	1	Watchdog timer [1:0]: 00: Disable 01: 32s 10: 64s 11: 128s
10	RW	POR, TR_OFF	WDTMR_SET[1]	0	
11	RW	POR, TR_OFF	FREQ_SEL[0]	01	DCDC frequency selection[1:0]: 00: 600 kHz 01: 800 kHz 10: 1000 kHz 11: 1200 kHz
12	RW	POR, TR_OFF	FREQ_SEL[1]		
13	RW	POR, TR_OFF	VLOBAT_REG[0]	0	Ratio of VDRPREF[1:0]: 00: Off 01: 105% 10: 107.5% 11: 110%
14	RW	POR, TR_OFF	VLOBAT_REG[1]	1	
15	RW	POR, TR_OFF	VDROOP_EN	0	0: Critical Voltage Monitoring disable 1: Critical Voltage Monitoring enable

ChargeCurrent Register − Memory Location : 14h					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	RW	POR, TR_OFF	IPRE_0	11	00: 0 mA 01: 128 mA 10: 256 mA 11: 512 mA
1	RW	POR, TR_OFF	IPRE_1		
2	R				Not Used
3	R				Not Used
4	R				Not Used
5	R				Not Used
6	R				Not Used
7	RW	POR, TR_OFF	ICHG_0	000001	000001 : 128 mA (Lower Clamp) 111111: 8064 mA (Higher Clamp) Step : 128 mA
8	RW	POR, TR_OFF	ICHG_1		
9	RW	POR, TR_OFF	ICHG_2		
10	RW	POR, TR_OFF	ICHG_3		
11	RW	POR, TR_OFF	ICHG_4		
12	RW	POR, TR_OFF	ICHG_5		
13	R				Not Used
14	R				Not Used
15	R				Not Used

ChargeVoltage Register − Memory Location : 15h					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	R				Not Used
1	R				Not Used
2	R				Not Used
3	R				Not Used
4	RW	POR, TR_OFF	VCHG_0	VSYSMIN + VSYSOFF	00000000000 : 3.328 V 00011010000 : 3.328 V (Lower Clamp) 10001101010 : 18.080 V (Higher Clamp) 11111111111 : 18.080 V Step : 16 mV
5	RW	POR, TR_OFF	VCHG_1		
6	RW	POR, TR_OFF	VCHG_2		
7	RW	POR, TR_OFF	VCHG_3		
8	RW	POR, TR_OFF	VCHG_4		
9	RW	POR, TR_OFF	VCHG_5		
10	RW	POR, TR_OFF	VCHG_6		
11	RW	POR, TR_OFF	VCHG_7		
12	RW	POR, TR_OFF	VCHG_8		
13	RW	POR, TR_OFF	VCHG_9		
14	RW	POR, TR_OFF	VCHG_10		
15	R				Not Used

ChargeOption2 Register − Memory Location : 3Ch					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	RW	POR, TR_OFF	HW_RST	0	Set 1 will disconnect the battery after RST_TMR
1	RW	POR, TR_OFF	BAT_DIS	0	Set 1 disconnect the battery when IN unplug until the next IN plug
2	RW	POR, TR_OFF	FAULT_MSK	0	Set 1 Mask fault interuption
3	RW	POR, TR_OFF	STATUS_MSK	0	Set 1 Mask Status interruption
4	R		STATE[0]		Charge state [2:0]: 000: OFF 001: CONFIG 010: HOLD 011: PRECHARGE 100: FULLCHARGE 101: SUPPLEMENT 110: END OF CHARGE 111: HW_RST
5	R		STATE[1]		
6	R		STATE[2]		
7	RW	POR, TR_OFF	RST_TMR_SET[0]	0	Reset Timer 00: 0 ms 01: 512 ms 10: 1024 ms 11: 2048 ms
8	RW	POR, TR_OFF	RST_TMR_SET[1]	1	
9	RW	POR, TR_OFF	FREQ_S_EN	0	Frequency Spread Spectrum enable 0: Disable 1: Enable
10	RW	POR, TR_OFF	CPEXIT_EN	0	0: CP exit disable 1: CP exit Enable
11	RW	POR, TR_OFF	IEOC[0]	1	000: 128 mA 001: 256 mA 010: 384 mA 011: 512 mA 100: 640 mA 101: 768 mA 110: 896 mA 111: 1024 mA
12	RW	POR, TR_OFF	IEOC[1]	0	
13	RW	POR, TR_OFF	IEOC[2]	0	
14	RW	POR, TR_OFF	LDO_MODE	0	Set 1 select LDO mode
15	RW	POR, TR_OFF	ECO_MODE	1	0: No Eco Mode 1: Eco Mode

Interrupt Register − Memory Location : 3Dh					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	RC	POR, OFF	EOC_INT	0	Flag End of Charge State is reached
1	RC	POR, OFF	PRE_INT	0	Flag Precharge state is reached
2	RC	POR, OFF	LEARNB_INT	0	Flag entering/exiting Learn mode
3	RC	POR, OFF	WDOG_INT	0	Flag a WatchDog Timer expired
4	RC	POR, OFF	IPEAK_INT	0	Flag IPEAK MAX is reached
5	RC	POR, OFF	INOVP_INT	0	Flag VIN> VINOV
6	RC	POR, OFF	BUCK_OVP_INT	0	Flag BUCK OV
7	R	POR, OFF	IINSHORT_INT	0	Flag IIN> IINSHORT
8	RC	POR	HW_RST_INT	0	Flag HW_RST state and HW_RST=1
9	RC	POR	BAT_DIS_INT	0	Flag HW_RST state and BAT_DIS=1
10	W1C	POR, OFF	SYSOV_INT	0	Flag System Overvoltage
11	RC	POR, OFF	BAT_RMV_INT	0	Flag battery is removed
12	R				Not Used
13	R				Not Used
14	R				Not Used
15	R				Not Used

MinSysVoltage Register − Memory Location : 3Eh					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	RW	POR, TR_OFF	VDYNPRE_EN	1	0: Dynamic precharge disable 1: Dynamic precharge enable
1	RW	POR, TR_OFF	VINOK_SEL	0	Control VINOK signal 0: INOK is set by VSEL 1 INOK is set by VSYSMIN
2	R				Not Used
3	R				Not Used
4	R				Not Used
5	R				Not Used
6	R				Not Used
7	RW	POR, TR_OFF	VSYSMIN_0	See electrical characteristics	00000000 : 3.328 V 00011010 : 3.328 V (Lower Clamp) 10001011 : 17.792 V (Higher Clamp) 11111111 : 17.792 V Step : 128 mV
8	RW	POR, TR_OFF	VSYSMIN_1		
9	RW	POR, TR_OFF	VSYSMIN_2		
10	RW	POR, TR_OFF	VSYSMIN_3		
11	RW	POR, TR_OFF	VSYSMIN_4		
12	RW	POR, TR_OFF	VSYSMIN_5		
13	RW	POR, TR_OFF	VSYSMIN_6		
14	RW	POR, TR_OFF	VSYSMIN_7		
15	RW	POR, TR_OFF	N_CELL_EN	1	0: VSYSMIN default value detection disable 1: VSYSMIN default value detection enable

Reset Legend:

- OFF: Set bit to RST VALUE when the charging state machine is in OFF state.
- TR_OFF: Set bit to RST VALUE when the charging state machine transits to OFF state.
- POR: Set bit to RST VALUE on power on reset.
- W1C : Need to write 1 to reset this bit to 0
- RC : Read this bit to reset to 0

InputCurrent Register − Memory Location : 3Fh					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	R				Not Used
1	R				Not Used
2	R				Not Used
3	R				Not Used
4	R				Not Used
5	R				Not Used
6	R				Not Used
7	RW	POR, TR_OFF	IINLIM_0	011010	000000: 128 mA 000001 : 128 mA (Lower Clamp) 111111 : 8064 mA Step : 128 mA
8	RW	POR, TR_OFF	IINLIM_1		
9	RW	POR, TR_OFF	IINLIM_2		
10	RW	POR, TR_OFF	IINLIM_3		
11	RW	POR, TR_OFF	IINLIM_4		
12	RW	POR, TR_OFF	IINLIM_5		
13	R				Not Used
14	R				Not Used
15	R				Not Used

ChargeOption3 Register − Memory Location : 40h					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	RW	POR, TR_OFF	SYSOFF_SEL	0	VSYS offset selection: 0 : 384 mV 1 : 256 mV
1	RW	POR, TR_OFF	DRP_SEL[0]	10	VDROOP threshold selection: 00 : 97% Relative to V_{SYSMIN} 01 : 5.6 V 10 : 5.8 V 11 : 6 V
2	RW	POR, TR_OFF	DRP_SEL[1]		
3	RW	POR, TR_OFF	BATRMV_SEL	0	Battery removal threshold selection: 0 : 2.85 V 1 : 1.6 V
4	R				Not Used
5	R				Not Used
6	R				Not Used
7	R				Not Used
8	R				Not Used
9	R				Not Used
10	R				Not Used
11	R				Not Used
12	R				Not Used
13	R				Not Used
14	R				Not Used
15	R				Not Used

ManufacturerID Register − Memory Location : FEh					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	R		MAN_ID[15:0]	0	
1	R			0	
2	R			0	
3	R			0	
4	R			0	
5	R			0	
6	R			0	
7	R			0	
8	R			0	
9	R			0	
10	R			0	
11	R			0	
12	R			0	
13	R			1	
14	R			1	
15	R			1	

DeviceID Register − Memory Location : FFh					
Bit	**Type**	**Reset**	**Name**	**RST Value**	**Function**
0	R		DEV_ID[15:0]	0	
1	R			0	
2	R			0	
3	R			0	
4	R			0	
5	R			0	
6	R			0	
7	R			0	
8	R			0	
9	R			0	
10	R			0	
11	R			0	
12	R			0	
13	R			1	
14	R			1	
15	R			1	

FUNCTIONAL DESCRIPTION

Overview

The NCP1871 is part of On Semiconductor's growing switching battery charger family for wireless and mobile computing. The NCP1871 is a NVDC switching battery charger with characteristics that makes it perfectly suited for 2−stacked battery cell applications such as ultrabooks or tablets.

The NCP1871 is designed around a full NMOS DC to DC controller that brings down the high voltage charger adapter voltage to a regulated system supply that is in the same range as the battery pack voltage. This limits the variation on the system supply voltage, hence the name Narrow Voltage DC (NVDC), and improves efficiency of the core converters. The device includes a voltage droop monitor, charger adapter validation and blocking as well as an intelligent battery connection control. The adapter current, charge current and system current are closely monitored and an image is provided to the host. The NCP1871 is fully programmable through an I^2C compatible SMBus interface.

In below figure, the block diagram of the NCP1871 in its typical application is shown.

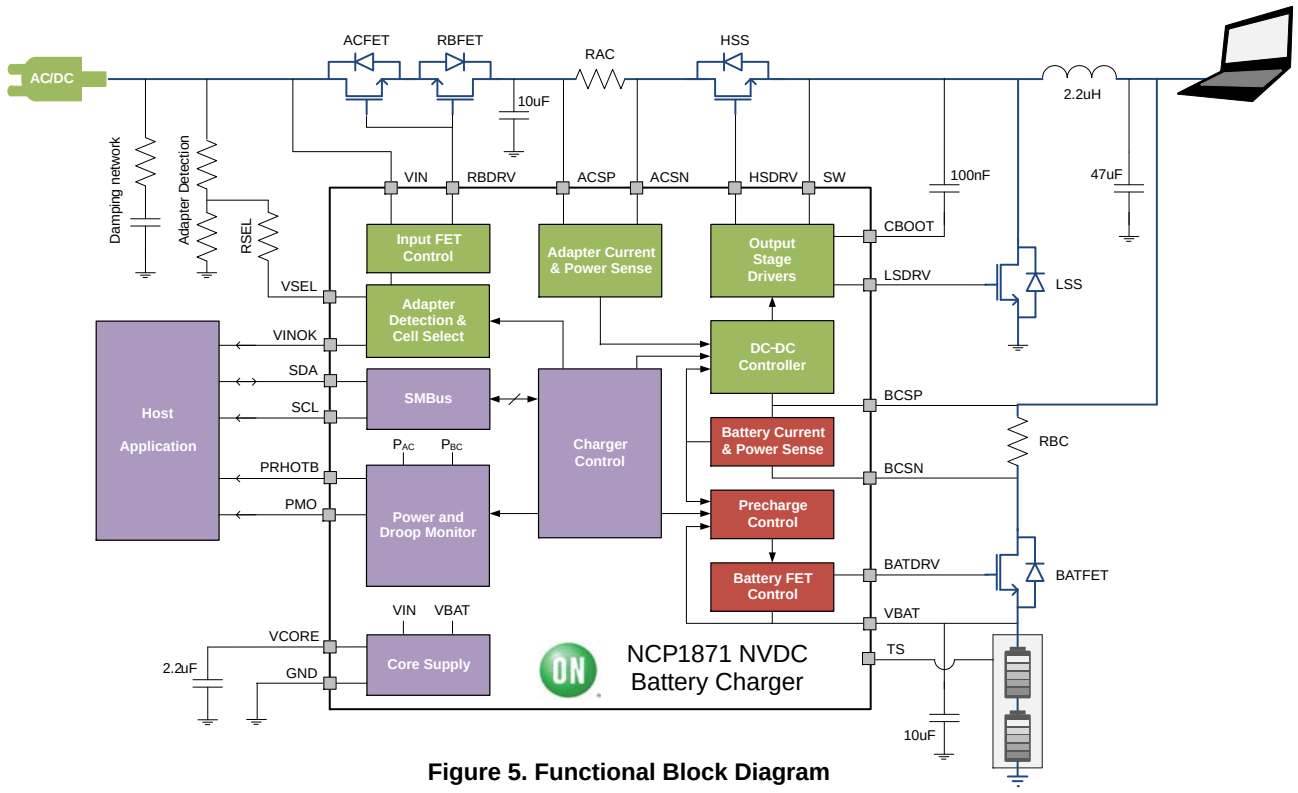


Figure 5. Functional Block Diagram

The charger adapter is connected to the application through a reverse blocking FET that avoids the leakage from the battery to input. The FET is made conducting when a valid charger is detected. At the same time a signal is generated to inform the host. Overvoltage detection will reject high voltage charge sources while protecting the application by blocking the high side FET of the DC to DC converter.

The adapter current is measured by means of a low impedance sense resistor. This information is used by the DC to DC converter to limit the average input current. Optionally, a second FET can be placed back−to−back in series with the reverse blocking FET to provide additional isolation towards the application.

The DC to DC converter supplies both the application and charges the battery pack. It regulates its output voltage, the input current as well as the battery charge current. The latter is measured by means of a low impedance sense resistor.

The battery pack is connected to the system through a low impedance NMOS. This battery FET is opened in case the battery is depleted while the DC to DC directly supplies the application using the system voltage as its feedback.

When charging, the battery FET is closed and the charge current is monitored. The battery voltage is used as the feedback voltage for the DC to DC.

When the battery is fully charged to End of Charge state, the battery FET is opened to preserve its charge but will assist the system in case it draws more peak power than the charge adapter can deliver.

The DC to DC converter runs in fixed frequency PWM mode with pulse skipping capabilities. To reduce EMI issues, the switching frequency is selectable and a frequency

spreading feature can be enabled which can reduce peak amplitude of the EMI energy by 10 dB. Soft start of both output voltage and output current moderate the inrush current.

The DC to DC converter uses external NMOS switches to handle the high currents involved. the NCP1871 has the capability to deliver up to 8 A. Though optimized for 2−stacked cell battery packs the NCP1871 also supports 3 and 4−stacked cell batteries.

Additional features include a voltage drop monitor that can supervise critical system voltage, a learn mode that allows to cycle a battery pack to re−initiate the battery pack's fuel gauge, and a system power monitor providing a true analog image of the system power to the host.

The NCP1871 is controllable through a SMBus interface that is also compatible with a 400 kHz I^2C control. A sideband interrupt signal informs the system of any event occurring. The bus allows reading out the device status as well as programming the different voltage and current levels and operating modes. The NCP1871 comes in a small 3.5 x 3.5 mm QFN−20 package at 0.5 mm pitch.

CORE

The IC core is supplied from a locally generated VCORE. The VCORE is a regulated supply that automatically takes the highest of the AC adapter input VIN and the battery connection VBAT as its input. The core includes a bandgap and generates all necessary references for the circuit. VCORE requires a bypass capacitor.

The core operates in two distinct modes: Off and Active. In Off mode only imprecise detectors are active monitoring the VIN pin and SMBus activity while keeping the battery pack connected to the system. All other circuitries are disabled. When a VIN or SMBus activity is detected, the core transitions to the active mode where the entire core is active including the precise bandgap and clocking. In active mode the different functions of the IC can be enabled such as the DCDC converter or power monitors.

The core does not operate for voltages below the under voltage lockout threshold (V_{UVLO}) and all internal circuitry, both analog and digital, is held in reset.

Charge Profile

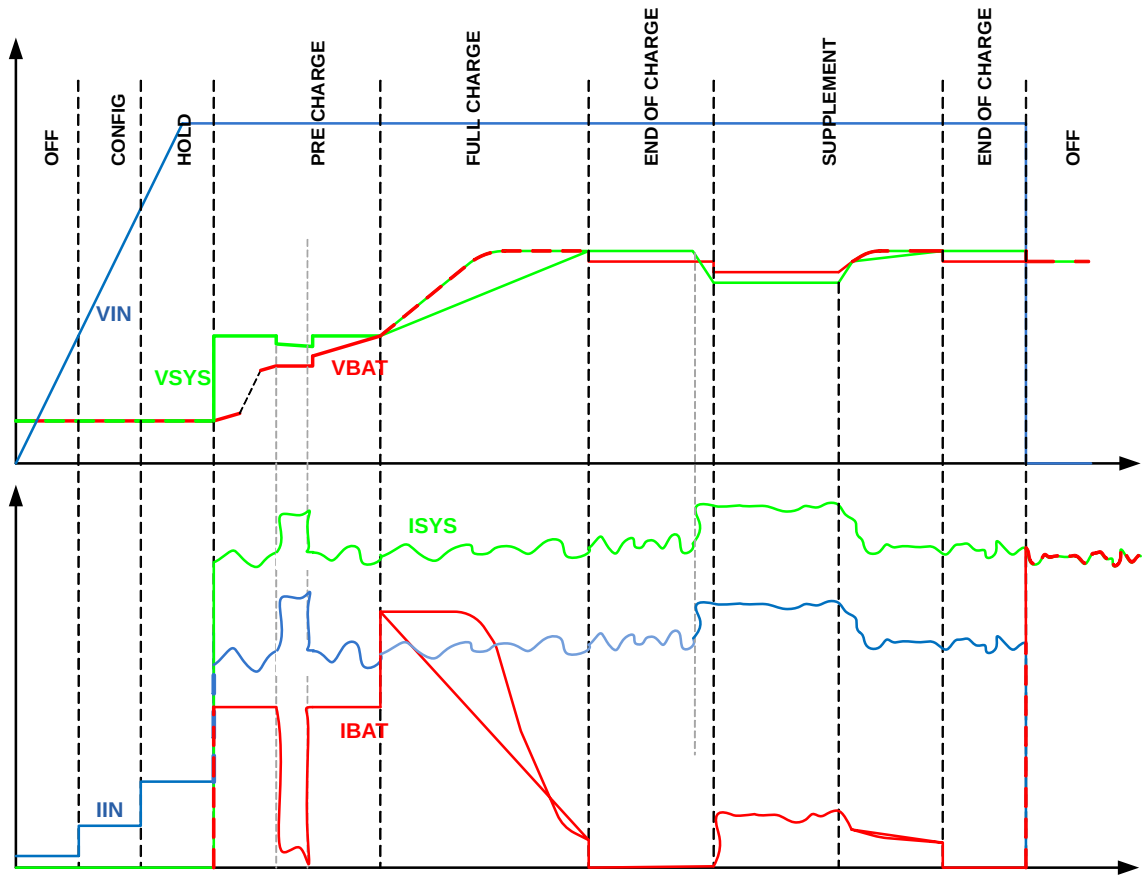


Figure 6. Typical Charge Profile

Pre Charge

In case of a depleted battery, attaching a valid charger will enable the DC to DC and the output voltage will be raised to VCHG. The feedback of the DC to DC converter is taken from BCSP. The battery FET will be used in a linear mode to precharge the battery pack at a current IPRE. Once the battery voltage reaches the minimum system operating voltage VSYSMIN, the battery FET is slowly turned on and the feedback is now taken from VBAT. Note that VSYSMIN is to be programmed to a value lower than VCHG.

When precharging the battery, the voltage at BCSP is permanently monitored. When the output drops towards the VSYSMIN level, the precharge current is reduced to zero in an analog fashion starting with BCSP being VPRERED above the VSYSMIN level. The precharge current will drop to zero immediately if BCSP drops across VPRESTOP above the VSYSMIN level. The above described precharge behavior is the default. By opting for a LDO_MODE option, the precharge phase will be skipped. This should only be done if the battery pack can handle a safe precharge on its own.

Full Charge

In case of an already connected battery, attaching a valid charger will enable the DC to DC with VBAT as the feedback voltage. If at the end of the voltage ramp the VBAT is greater than VSYSMIN, the battery FET remains closed and full charging is engaged. For VBAT below the VSYSMIN however, the battery FET is automatically made non−conducting, the pin BCSP taken as the feedback, and the battery pack pre−charged as described above. By this overlapped approach the system will remain correctly supplied when opening the battery FET.

End of Charge

Once the battery is fully charged the battery FET is made non−conducting. This avoids wear and tear of the battery cells and enhances the battery pack's lifetime. The fully charged state is determined by the battery pack's fuel gauge. Through SMBus the battery charger is then disabled. This does not mean that the DC to DC converter is disabled, just that the battery is no longer charged. Normally, it was still being charged with a small current before disabling charging for a full battery, so after the battery FET is opened, the system voltage is slightly above the battery voltage.

The end of charge detection by the charger is not the preferred method; termination by the fuel gauge is preferred at large due to the correlation between end of charge and 100% battery capacity. However, the end of charge detection may be helpful as an additional means of protection. The end of charge detection should therefore be set low. Upon an end of charge detection an interrupt is generated.

Supplement Mode

With the FET non−conducting, the system current may exceed the power rating of the wall charger. As a result the system voltage will drop. When a significant BCSP drop of VDRCON is detected, the battery FET will be turned on and the battery will supplement the remainder of the current to avoid further drop. Once the system current is reduced below the adapter current, the system voltage will again rise above the battery voltage and the FET is opened. The battery will not get recharged in the process as long as the charger is not re−enabled through SMBus.

DCDC Converter

The DC to DC converter uses external NMOS pass devices for both the low side and the high side switches. To drive the gate of the high side switch at HSDRV, a bootstrap capacitor is used that is connected between SW and CBOOT. This capacitor is precharged from the VCORE reference. The gate of the low side switch is directly driven at LSDRV. Not the drain of the high side switch, but the hot side of the sense resistor should be considered as the input of the converter and therefore a capacitor has to be placed at ACSP. To avoid too high ripple in the application, the capacitor is to be grounded to the source of the low side switch before connecting to the system ground.

The output voltage of the DC to DC converter is regulated to the level VCHG as set in the ChargeVoltage register. Depending on the state of the battery FET the voltage at pin BCSP (FET open) or the voltage at pin VBAT (FET closed) is taken as the feedback voltage. The latter is done to avoid any early charge current reduction due to the IR drop between BCSP and VBAT.

Apart from the output voltage regulation, the DC to DC converter control loop will also limit the amount of input power from the AC adapter and the amount of current provided to the battery. In other words, the DC to DC converter will only be at the set output voltage if the current limits are not hit. The input current limit is set in the InputCurrent register, the charge current in the ChargeCurrent register. Note that when the input current limit is reached, the output voltage will drop automatically thus reducing the amount of current provided to the battery. In other words, priority is given to the system current over the battery charge current.

When enabled, the reference for the DC to DC output voltage is smoothly ramped. Once the output voltage ramp has finished, the charge current is ramped up. When reprogramming an established output voltage to a higher or lower value, the voltage ramp is also applied. The combination of these mechanisms limits the peak inrush current at startup and during the transitions after SMBus programming.

Once enabled, the converter operates in a fixed frequency PWM mode and will pulse skip automatically when needed. The switching frequency is selectable over a small range, it is however not advised to apply 'on the fly' changes but to use a device instance with a different default value.

During specific mode, the power consumption of the whole system is intended to be very low. An Eco mode can be enabled through I^2C, (bit ECO_MODE, register ChargeOption2) which increases the efficiency at very light load (10−20 mA).

This particular skip mode is active when the input current is lower than 100 mA. If so, the T_{ONMIN} is extended to reduce switching activity and frequency as a consequence. The buck also regulates in asynchronous mode. As soon as ECO_MODE is set to '0' whatever the input current is, the eco mode is disabled.

The DC to DC converter switches at fairly significant current levels which could cause conducted and radiated EMI issues. A frequency spreading option can be enabled to reduce the side−effects of this. By varying the switching frequency at a constant low rate (i.e. a modulation with a triangular waveform), the peak amplitude of the EMI energy in the output spectrum can be reduced by about 10 dB. Note that the amount of power itself is not reduced, just its allocation over the frequency band.

When pulse skipping, the current in the inductor will fall to zero for each cycle (discontinuous operation). At that point both the low side and high side switches are non−conducting, and the SW node will be ringing caused by the LC resonance created on the switch node. In absence of prolonged switching activity, the bootstrap capacitor will discharge. In order to maintain the capacitor charge, the low side FET will be turned on periodically so that the bootstrap capacitor can be recharged again to VCORE level.

To protect the DC to DC converter output transistors as well as the inductor, a peak current limiter will limit the cycle to cycle peak current. It uses the voltage drop over the input current sense resistor to monitor the peak current. A flag bit is set to inform the host about the event but the DC to DC converter is not automatically disabled.

Current and Power Monitoring

The current and power monitoring block consists of an analog output signal reflecting the amount of power taken by the system and an open drain output signaling the host that excessive power is drawn by the system.

The below diagram depicts the power monitoring functionality.

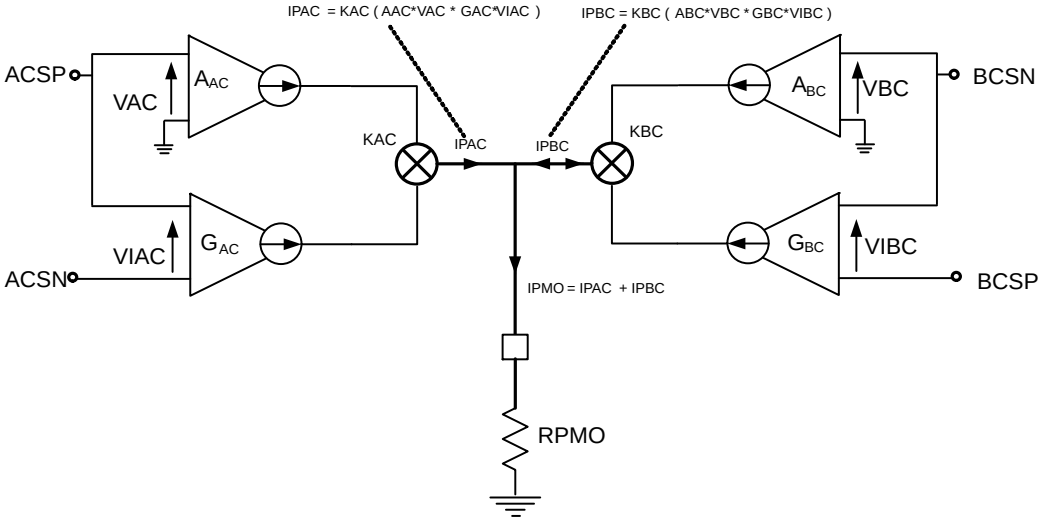


Figure 7. Power Monitoring Diagram

In order to inform the Host about the amount of power used by the system, an image of the power taken from the charger input and the battery pack is provided at the power monitor output PMO. PMO does take into account the power that is sourced to the battery during the charge cycle. Based on this information, the host can determine if it is reaching the maximum power level it is allowed to take from either source.

The adapter current is sensed through the sense resistor R_{AC} connected between the pins ACSP and ACSN. The measurement is low pass filtered to remove the current ripple due to the DC to DC activity. The resulting signal is multiplied with the adapter voltage at ACSP and amplified to the PMO output. The current measurement signal is also used by the DC to DC converter to limit the input currents and by the adapter over current protection circuitry.

The current flowing out of and into the battery is sensed through the sense resistor R_{BC} connected between the pins BCSP and BCSN. The measurement is low pass filtered to remove any current spikes due to the transient load response of the system. The resulting signal is multiplied with the battery voltage at BCSN and amplified to the PMO output. The current measurement signal is also used by the DC to DC converter to control the charge current. The battery power sense circuitry can be enabled in both charging and non charging modes.

VOLTAGE DROOP MONITOR

The below diagram depicts the voltage monitoring functionality.

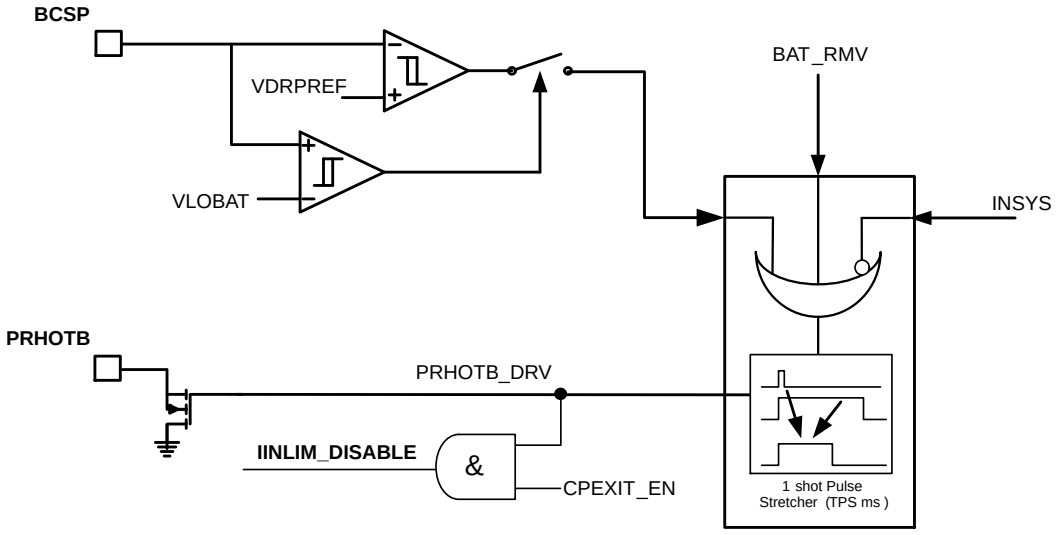


Figure 8. Critical Voltage Monitor Diagram

The critical system voltage node, is connected to BCSP and is monitored for a sudden drop due to high loading conditions. A comparator with a programmable threshold is used for this. This comparator is enable when bit VDROOP_EN is set to 1 (register ChargeOption). For additional adjustment, the detection level can be adjusted with VDRP_SEL bit of ChargeOption3 register. This comparator can be disabled under low battery conditions to avoid false triggering (bits VLOBAT_REG, register ChargeOption). The overall system can be enabled in both charging and non charging modes. Note that under low battery conditions the processor peak current will be automatically reduced by the system so that critical voltage droops are avoided.

The output of the drop monitor is fed into a pulse stretcher that will ensure the PRHOTB pin will be pulled low for a guaranteed minimum period TPS which will reduce the processor speed (PROCHOT# pin) and thus the power consumed. BAT_RMV and INSYS signal leads to a PRHOTB generation as well.

Watchdog Timer Description

The battery charging cycle is under control of the host. It may happen that the host is too busy to survey the charger or that the system is stuck. As a safety measure therefore a watchdog timer is started after each I^2C write in charge current or/and voltage setting registers during active charge states. When the watchdog timer is enabled, the charge will be suspended if IC does not receive any write charge voltage or write charge current command within the watchdog time period. This timer can be set or disabled through SMBus registers.

Input Current Limitation

Apart from the output voltage regulation, the DC to DC converter control loop will also limit the amount of input power from the AC adapter and the amount of current provided to the battery. In other words, the DC to DC converter will only be at the set output voltage if the current limits are not hit. The input current limit is set in the InputCurrent register. Note that when the input current limit is reached, the output voltage will drop thus automatically reducing the amount of current provided to the battery.

Battery FET

The battery pack is connected to the system voltage rail through the NMOS battery FET (BATFET), driven from BATDRV. In order to support all operating modes of the application, the battery FET can be operated in three states; fully conducting, non−conducting and linear mode.

When the application is in off mode and no charger is attached, the system voltage is maintained by the battery. The BATFET is fully conducting by BATDRV being driven high through a charge pump to VBAT plus VPUMP. The charge pump features a very low bias current when maintaining BATDRV high. This current is accounted for in the core quiescent current. When the application is operating without any charger attached, the battery FET is by default fully conducting when the VBAT is greater than the undervoltage threshold UVLO while non−conducting for lower voltages (fully depleted battery).

Adapter Detection and Removal

The AC adapter is connected to the input VIN which is permanently monitored by a set of comparators. A first imprecise low current comparator will detect the presence of an input voltage greater than VINDET. This comparator is always enabled even when the core of the circuit is in off mode. Once detected, the more precise input voltage detectors are enabled.

The precise voltage detectors will validate if the applied charger is in the proper input range bounded by VINLO (on VSEL pin) and VINOV(on VIN pin) or VINMINOK depending on VINOK_SEL (see SMBUS Registers Map). To guarantee a robust detection, debounce timers are added to the VINLO detection. The VINOV acts as an overvoltage protection that rejects too high voltage chargers in order to avoid damage to the application.

VINOK Output

When the input voltage is valid (VSEL > VINLO and VIN < VINOV) or (VINMINOK < VIN < VINOV) depending on VINOK_SEL bit (register MinSysVoltage), the open drain VINOK pin is released and pulled high by the external pull up resistor thus signaling the host that a valid supply is attached. When becoming invalid the opposite applies.

The SMBus doesn't has a slave interrupt feature. To inform the host about an event a sideband signal is to be used. On the NCP1871 the VINOK pin flags to the host when a valid charger is attached. Given the non critical timing of the VINOK signal for this use case, an interrupt is signaled as a short 'not VINOK' pulse. The short period of the pulse allows distinguishing an interrupt from a charger removal. An interrupt can only be generated when a valid charger is attached. The interrupt feature can be enabled and disabled through the control bus (Bit FAULT_MSK and STATUS_MSK, Register ChargeOption2). Register Interrupt inform the system about the nature of interruption.

I²C Signal	Nature	Flagged on VINOK	Associated Mask Bit	Description
EOC_INT	RC Dual Edge	Yes	STATUS_MSK	0: Not in End of Charge state 1: End of charge state
PRE_INT	RC Dual Edge	Yes	STATUS_MSK	0: Not in Precharge State 1: Precharge state
LEARNB_INT	RC Dual Edge	Yes	STATUS_MSK	1: Enter/Exit Learn Mode
WDOG_INT	RC Single Edge	Yes	STATUS_MSK	1: Wd timer expired
IPEAK_INT	RC Single Edge	Yes	FAULT_MSK	1: IPKMAX reached.
INOVP_INT	RC Dual Edge	Yes	FAULT_MSK	0: INOVP = 0 1: INOVP = 1
BUCK_OVP_INT	RC Dual Edge	Yes	FAULT_MSK	0: BUCKOV = 0 1: BUCKOV = 1
SYSOV_INT	Write 1 to Clear	Yes	FAULT_MSK	1: SYSOV
HW_RST_INT	RC Single Edge	No	NA	1: HW_RST state **and** HW_RST=1
BAT_DIS_INT	RC Single Edge	No	NA	1: HW_RST state **and** BAT_DIS=1
INSHORT_INT	No Clear	Yes	FAULT_MSK	1: INSHORT = 1
BAT_RMV_INT	RC Single Edge	Yes	STATUS_MSK	0: Battery is present 1: Battery is removed

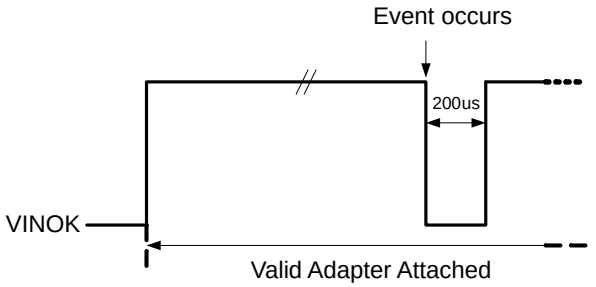


Figure 9. Interrupt Signaling

Battery Removal

A battery removal pin TS can be used to monitor battery presence. This allows the charger to anticipate a potential voltage drop of the system rail in case of battery removal. If a battery is suddenly removed, a PRHOTB is immediately generated, informing the system that the battery is no longer available for supplement. If this event appears during learn mode, the buck is immediately forced to VCHG. The PRHOTB length is 10 ms allowing enough time for the system to take into account this event, and adapt its power management accordingly.

VSYSMIN Default Value Detection

User can select the VSYSMIN default value thanks to an external resistor RCELL. The resistance should be put in series with VSEL pin as follows:

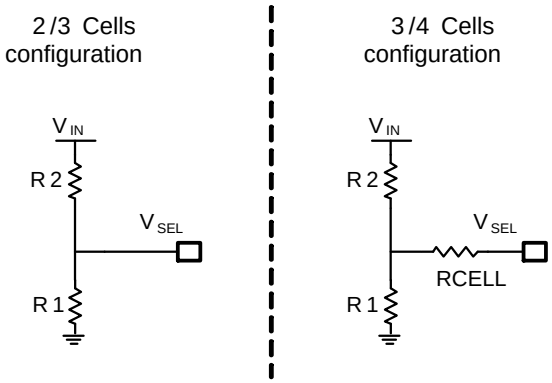


Figure 10. Resistor Network for CELL Detection

RCELL must be 220 kΩ if 3/4 cells config selected. R1 is also fixed to 22 kΩ, and R2 is used to select VINOK threshold. The following table illustrates VINOK versus R2.

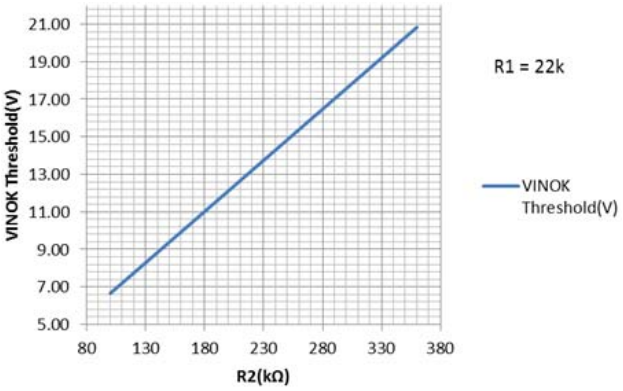


Figure 11. VINOK versus R2 Table

This function can be defeated through I^2C (bit N_CELL_EN, register MinSysVoltage).

Upfront Protection

To avoid the battery voltage supplying the AC adapter input pin, a reverse blocking element is required. One could use a Schottky diode but given the high current levels in play, the dissipation would be excessively high and overall efficiency degraded. This is resolved by using a reverse blocking FET (RBFET) function that simulates an ideal diode. The RBFET is an NMOS type and its gate driven from RBDRV. An internal charge pump will provide a RBDRV drive voltage of VIN plus VCORE.

When attaching a charger, the DC to DC converter is not yet operational and the system is isolated from the charger by the DC to DC converter high side switch. Therefore, upon attachment the capacitive loading seen from the battery charger through the body diode of the RBFET remains limited to the capacitor at ACSP. It is therefore thought that a back to back configuration of a reverse blocking FET RBFET with an input FET ACFET is not necessarily required, By using a back to back FET configuration however, the charger can be isolated from the application thus providing additional protection against system short circuits and overvoltages. A back to back FET combination also allows connecting some additional charging related circuitry just right after the input FETs while taking advantage of the overvoltage protection.

When a system short circuit occurs that exceeds the input and peak to peak current limits, the RBDRV pin will be made low and the charger will have to be removed to unlatch this condition. When exceeding the system overvoltage threshold VSYSOV, SYSOV_INT bit will be triggered as system over voltage, need to Write 1 to Clear this bit and release this protection.

For effective isolation the ACFET will have to be added to create a back to back configuration with the RBFET. Both mechanisms add additional safety in case the DC to DC converter does not manage to limit the voltage or current due to for instance a shorted high side switch or other malfunctioning.

Learn Mode

The NCP1871 provides a special battery learning cycle that helps to calibrate the battery fuel gauge. This cycle is performed while an adapter is attached. Upon the SMBus LEARN command the DC to DC converter is immediately forced to VSYSMIN+VSYSOFF, so the application would be supplied from the battery therefore discharging the latter. When LEARN is finished (normally by fuel gauge) or battery is removed, the charge can resume normally.

Constant Power Exit

In case a PRHOTB generation is not sufficient to stop the voltage drop during a very strong load transient, some AC adapters are designed to provide more power than their nominal value. In that case, the charger must disable the input current limit to allow full power to flow through it. This mode is enabled thanks to CPEXIT_EN bit in register ChargeOption2. If this bit is set to 1, the input current limit will immediately be disabled during PRHOTB generation. As soon as PRHOTB disappears, the input current limit is enabled again.

AC Adapter Overvoltage Protection

In case of an overvoltage, the DC to DC converter is immediately disabled and the RBDRV pin made low, so a−synchronously with the core logic. The converter and RBDRV are enabled again when the overvoltage condition disappears. The converter is definitely disabled by the core logic and the charger rejected when the overvoltage condition persists. When connecting an AC adapter, transient voltages greater than the maximum ratings of the IC can occur. Appropriate filtering will have to be placed upfront to stay below these levels.

Hard System Reset

A hard system reset is initiated after the user has pressed the power button for a long period, usually 8 seconds. The keyboard controller can then through SMBus program the system reset bit after which the BATDRV pin is temporarily made low to GND and the system reset bit cleared. To totally isolate the battery pack from application, back to back configuration of BATFET will be needed. Upon HW_RST bit is set to 1, a RST_TMR timer is launched and BATFETs are made non conducting when this timer is expired. This RST_TMR timer ensures the system can turn off correctly after HW_RST bit is set 1. The Timer also determines the BATFET OFF duration.

Battery Disconnect

In web tablets and ultrabooks, the battery pack is embedded and is shipped while being partially charged. To avoid the battery getting slowly discharged by the application while being on the shelf, the battery pack is totally isolated from the application by adding a second MOS in a back to back configuration. By setting the battery disconnect bit through SMBus, after a delay of RST_TMR, the BATDRV pin will be made low to GND when the adapter is removed and will be kept low as long as the battery power remains available. To exit this state a valid charger will have to be inserted which will reconnect the battery pack and reset the disconnect bit.

Serial Interface (SMBUS)

The device is widely programmable through the SMBus interface. The SMBus is based on the I^2C interface with some exceptions. These exceptions are documented in the SMBus specification 2.0 that is available at smbus.org. The I^2C specification is available from the NXP website or through i2c−bus.org.

The SMBus implementation on the NVDC charger is I^2C friendly allowing it to be used on non SMBus applications. The most noticeable differences between the two standards to the NVDC charger are listed below.

For SMBus the SDA and SCL logic low and high levels are defined as absolute voltages, where they are relative to the supply for I^2C. Although specification wise this may lead to conflicting situations, in practice this does not cause an issue when operating from 3 V and 5 V supply rails. The interface of the NCP1871 uses absolute levels and is supplied by the bus lines itself.

For SMBus the clock frequency is within 10 kHz and 100 kHz where I^2C allows for 0 Hz while in the widespread fast mode it can run up to 400 kHz.

The minimum clock frequency for SMBus allows for implementing a bus timeout mechanism. When the master keeps the bus clock low the slave will release the data lines and the transaction is aborted (equivalent to an I^2C STOP command).

Limiting the clock frequency of the interface to the SMBus standard could lead to conflicts on an I^2C bus. The NCP1871 therefore supports up to 400 kHz. This has no side effects on the SMBus operation itself. Note that the bus clocking is independent from the core logic clocking.

For SMBus a slave should always ACK its device address but is allowed to NACK after any of the data bytes. On I^2C one is allowed to NACK the address. The NCP1871 will actually never respond with a NACK and therefore always provide an ACK.

A smart battery charger on a SMBus has an imposed bus address of 0001001b. Optionally, the NCP1871 includes a different I^2C address (available upon request).

The smart battery charger protocol imposes a word (low byte, high byte) write/read protocol with one address per 2 bytes. In I^2C, the single byte write/read is more common where each byte of data has its own individual address. However, most I^2C masters can perform an auto increment to perform a 2 bytes consecutive write/read starting with the low byte, also see the appendix. The diagram below summarizes this.

Write Word Protocol Format

Start	Slave Address	W	ACK	Register Address	ACK	LowData Byte	ACK	High Data Byte	ACK	Stop
	0001001	0	0	[7:0]	0	[7:0]	0	[15:8]	0	

Read Word Protocol Format

Start	Slave Address	W	ACK	Register Address	ACK	Start	Slave Address	R	ACK	LowData Byte	ACK	High Data Byte	NACK	Stop
	0001001	0	0	[7:0]	0		0001001	1	0	[7:0]	0	[15:8]	1	

Application Information

Typical Application

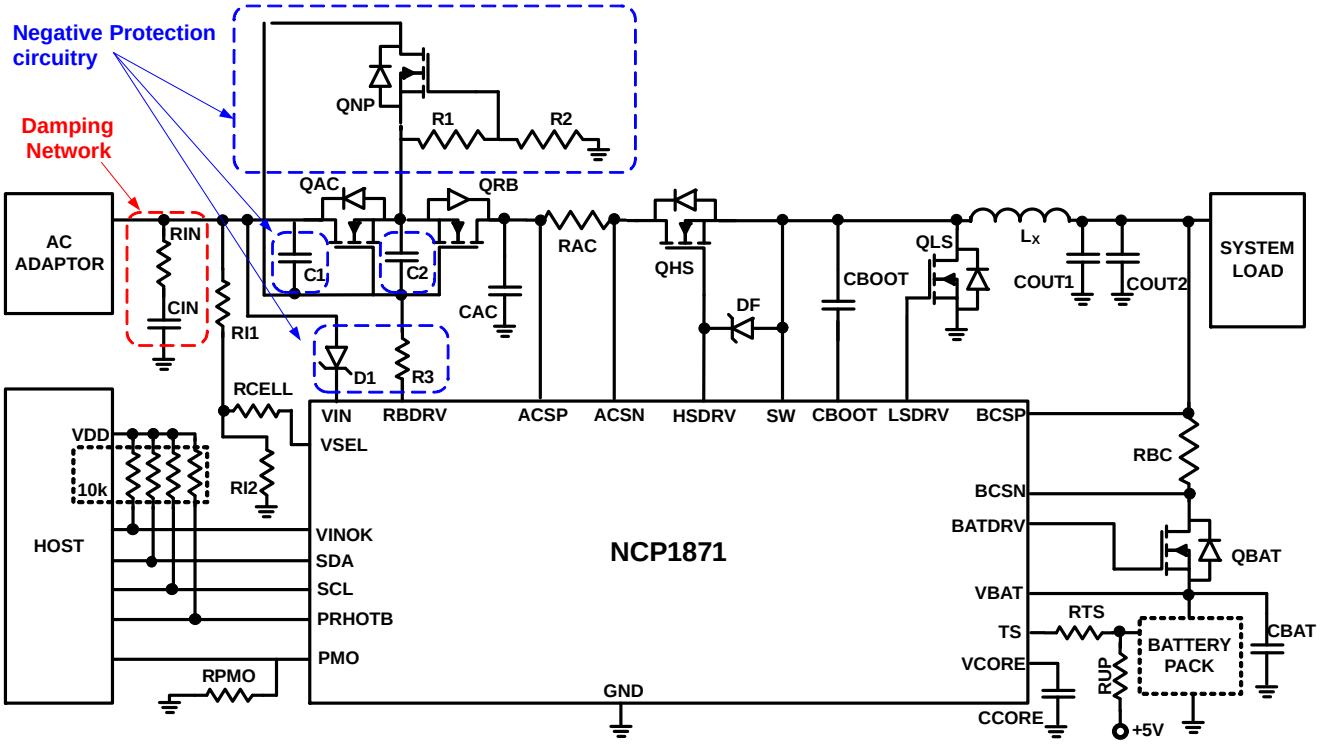


Figure 12. Additional Circuitry for Negative Protection

Table 5. BILL OF MATERIAL

Reference	Description	Manufacturer / Part Number	Value
C_{IN}	Decoupling input capacitor		4.7 μF / 50 V
R_{IN}	Damping Resistor		2 Ω / 0.5 W
C_{AC}	Decoupling Switcher capacitor		10 μF / 50 V
C_{BOOT}	Bootstrap capacitor		100 nF / 25 V
C_{CORE}	Decoupling core supply capacitor		2.2 μF / 6.3 V
C_{OUT1}, C_{OUT2}	Decoupling system capacitor		47 μF / 25 V
C_{BAT}	Decoupling battery capacitor		10 μF / 50 V
D_F	Clamping Schottky Diode	MBRM120E / ONSEMI	20 V / 1 A
L_X	Switcher Inductor	IHLP−2525CZ−01 / VISHAY	2.2 μH / 8 A
R_{AC}, R_{BC}	Current sense resistor		10 mΩ / 1 W
Q_{AC}, Q_{RB}, Q_{HS}, Q_{LS}, Q_{BAT}	Power MOSFET N−channel	NTTFS4C10N / ONSEMI	10 mΩ / 30 V
R_{TS}	Battery Hotplug Current Limit Resistor		1 kΩ / 0.1 W
R_{UP}	Battery Removal Pull Up resistor		100 kΩ / 0.1 W
R_1	Q_{RB} Reverse protection biasing resistor		3.01 MΩ / 0.25 W
R_2	Q_{RB} Reverse protection biasing resistor		1 MΩ / 0.25 W
R_3	R_{BDRV} Reverse protection resistor		4 kΩ / 0.5 W
R_{PMO}	Power Monitor Resistor		33 kΩ / 0.1 W
C_1	Reverse protection capacitor		2.2 nF / 50 V
C_2	Reverse protection capacitor		0.1 μF / 50 V
Q_{NP}	Reverse protection NMOS	2N7002L / ONSEMI	7.5 Ω / 60 V
D_1	Schottky Barrier Rectifier	MBRA340T3G / ONSEMI	3 A / 40 V
R_{I1}, R_{I2}	Minimum input voltage valid resistor		See VSYSMIN Default Value Detection
R_{CELL}	Number of cell selection resistor		

Input Damping Network

A Damping network is recommended in order to avoid voltage ringing on the input. On the following example (see Figure 13) with a 1 μH / 0.1 Ω cable, the maximum input voltage is higher than 30 V and can damage the application. In Figure 14, a damping network 1 μF / 2 Ω is added so the input voltage is smoothed to 22−24 V maximum.

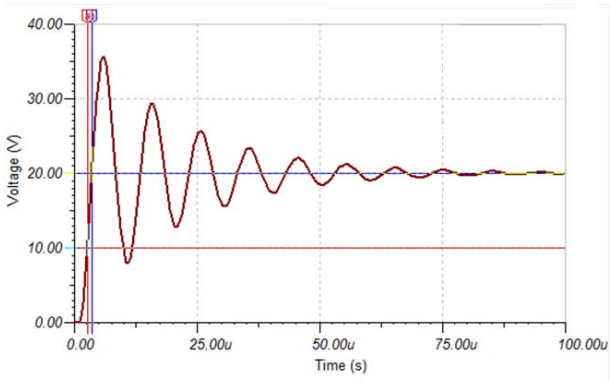


Figure 13. Hot Plug Behavior without Damping Network

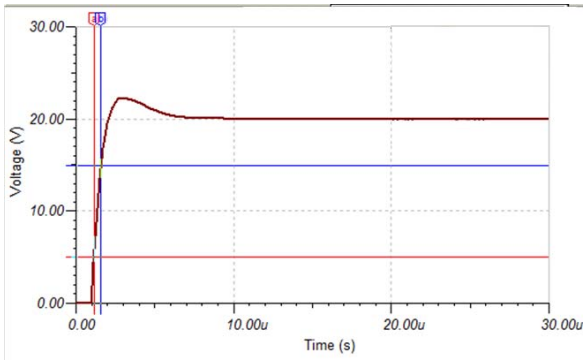


Figure 14. Hot Plug Behavior with Damping Network

Input Negative Protection

A negative voltage protection on input is defined by the negative protection circuitry (see Figure 12). In normal operation, Q_{NP} is off (VGS < 0 V). D1 is conducting and R1, C1 and C2 have no continuous effect. When adapter voltage is reversed, Q_{NP} V_{GS} is positive causing Q_{NP} to turn on. As a consequence, the source and gate node of Q_{RB} is shorted so Q_{RB} is off and the battery side circuitry is protected by the body diode of Q_{RB}. At the same time, D1 is protecting input charger circuitry by blocking the negative voltage and R3 limits the current flowing into the ESD protection circuitry thus avoiding damage. C1 and C2 ensure the V_{GS} of Q_{RB} and Q_{AC} remains 0 V during negative hot plug.

Components Selection

Inductor Selection

Inductor electrical selection depends on maximum current, frequency and duty cycle. The saturation and DC current are defined by:

$$I_{SAT} = I_{CHG} + 0.5 \times I_{RIPPLE}$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT} / V_{IN}$), switching frequency (F_{SWCHG}) and inductance (L_X):

$$I_{RIPPLE} = \frac{\left(V_{IN} \times D \times (1 - D)\right)}{\left(F_{SWCHG} \times L_X\right)}$$

The maximum inductor ripple current happens for D = 0.5

$I_{RIPPLE} = V_{IN} / (4 \times F_{SWCHG} \times L_X)$ So maximum current is given by $I_{SAT} = I_{CHG} + 0.5 \times V_{IN} / (4 \times F_{SWCHG} \times L_X)$

Please note that the NCP1871 switching frequency is selectable.

Power MOSFETs Selection

NCP1871 is designed to drive N−Chanel MOSFET with 5 V gate drive voltage and an operating voltage up to 24 V. Due to voltage transient, a 30 V N−MOSFET is preferred. Q_{AC}, Q_{RB}, Q_{HS}, Q_{LS} and Q_{BAT} are all N−Chanel MOSFET and can be identical. It is also recommended to select a very low RDSON MOSFET (10 mΩ typically for V_{GS} = 4.5 V) with a total gate charge around 10 nC typically. NTTFS4C10N from ON SEMICONDUCTOR is the perfect fit with NCP1871.

For Q_{BAT}, one more thing needs mention: since BATDRV would be pulled low to GND during shipping mode or hard system reset action, which means VGS at this time would be (–VBAT), the NFET needs to be selected with enough VGS rating especially for 3 or 4 cells application.

PCB Layout Recommendation

Proper layout of the components is recommended in order to minimize high frequency current path loop and to prevent high frequency resonant problems and electrical magnetic field radiation.

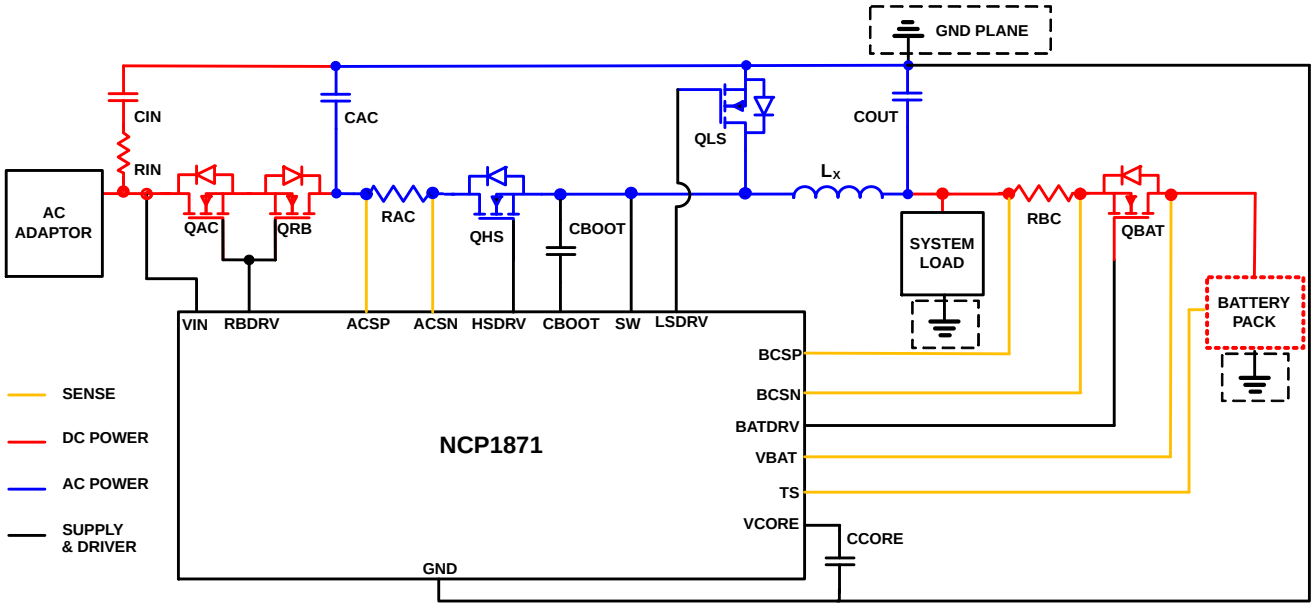


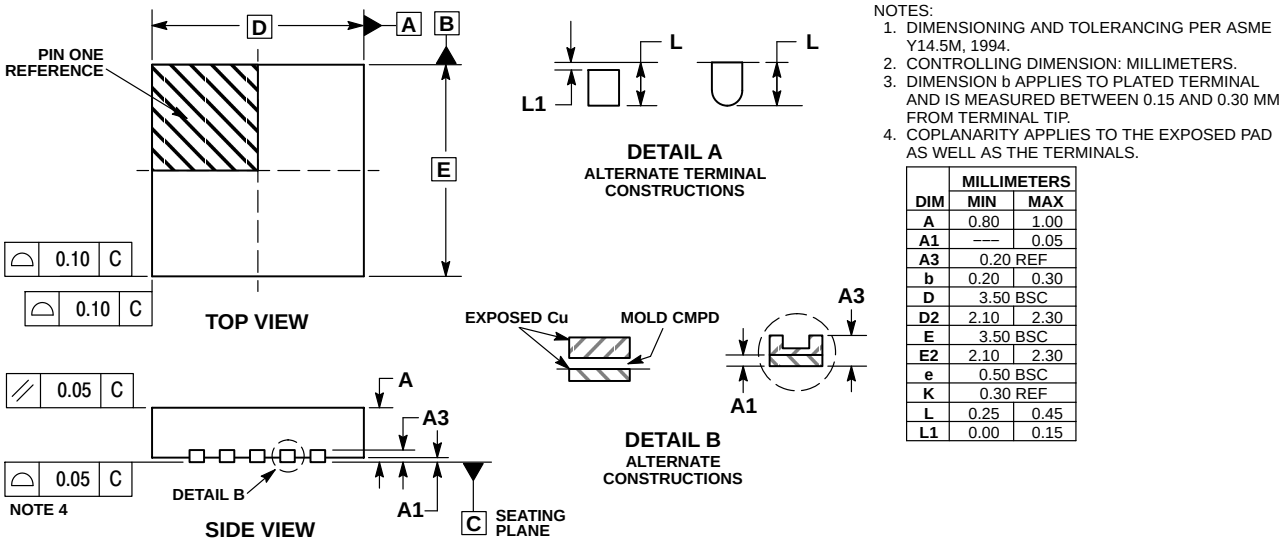
Figure 15. Typical Layout Recommendation

It is crucial to take the following rules into account.

- The switching loop (AC power track) composed by C_{AC}, R_{AC}, Q_{HS}, Q_{LS}, L_X, C_{OUT} must be as short as possible and placed on the same layer of PCB. This track must be isolated from GND plane, only C_{OUT} cold node is connected to the GND plane. This track must be large enough to reduce impedance of track (8 A typ).
- The impedance of DC power track composed by Q_{AC}, Q_{RB}, R_{BC} and Q_{BAT} must be as low as possible and placed on the same PCB layer as the AC power track. This track also must be large enough (8 A typ).
- C_{CORE} Capacitor must be placed as close as possible to the IC and routed on the same PCB layer as the IC. The connection to GND (expose pad) should be short and connected to C_{OUT} cold node with a unique track.
- Use Kelvin connection for RAC and RBC sensing and do not route these sense leads through a high di/dt or dv/dt path.
- Supply and driver track must be large enough (1 A max). LSDRV and HSDRV are switching nodes; track must be shortened to reduce parasitic inductance.

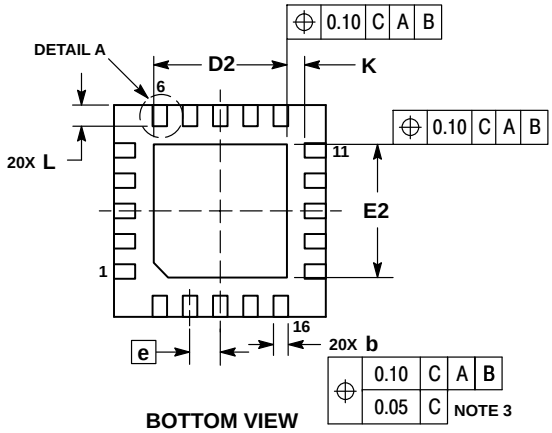
PACKAGE DIMENSIONS

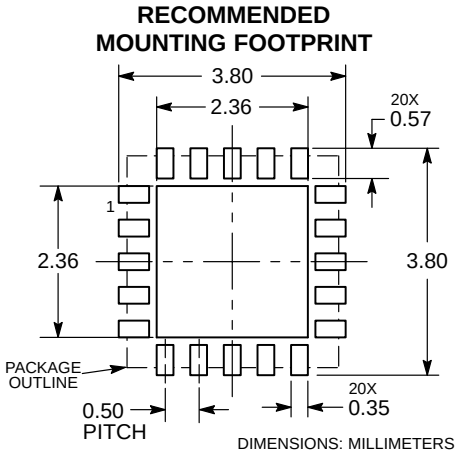
QFN20 3.5x3.5, 0.5P
CASE 485CP
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	−−−	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.50 BSC	
D2	2.10	2.30
E	3.50 BSC	
E2	2.10	2.30
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15





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