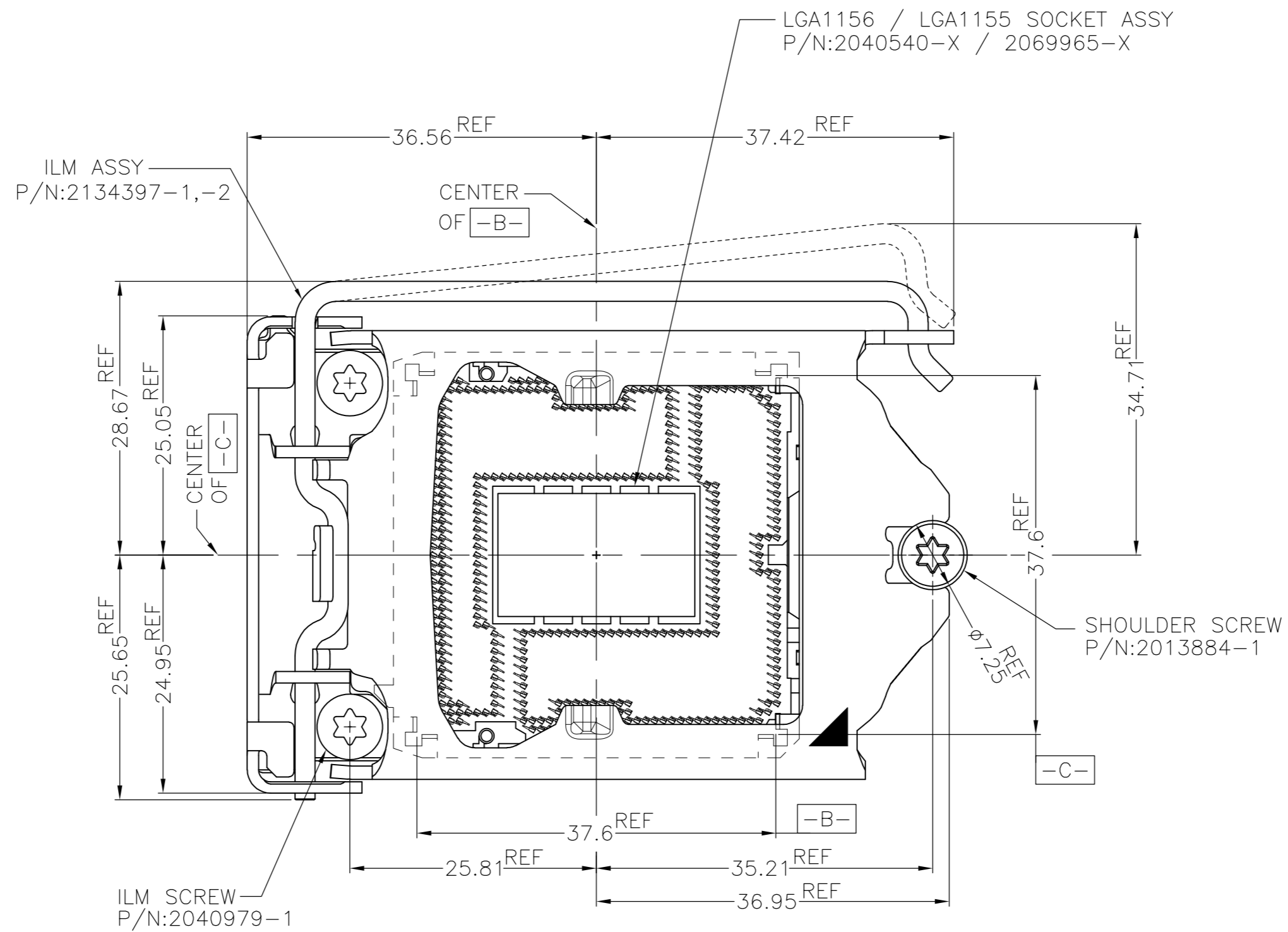


THIS DRAWING IS UNPUBLISHED. RELEASED FOR PUBLICATION
 © COPYRIGHT - By Tyco Electronics Japan G.K. ALL RIGHTS RESERVED.

LOC	DIST	REVISIONS					
		P	LTR	DESCRIPTION	DATE	DWN	APVD
J	-	-	-	SEE SHEET 1	-	-	-



ILM ASSEMBLY OCCUPATION AREA
(REFERENCE)

DATUM B AND C ARE REFERRED TO THE CENTER OF LGA SOCKET DATUM WALL

FOR GENERAL BOARD DESIGN, PLEASE REFER TO THE THERMAL AND MECHANICAL DESIGN GUIDELINES(TMDG) PROVIDED BY INTEL CORPORATION

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN	TE TE Connectivity	
DIMENSIONS: 単位: 寸 mm		CHK		
TOLERANCES UNLESS OTHERWISE SPECIFIED: 一般公差		APVD	NAME 名称	
0-PLC ±		PRODUCT SPEC 製品規格	ILM ASSY	
1-PLC ±		APPLICATION SPEC 取付適用規格	LGA115X	
2-PLC ±		WEIGHT	SIZE	RESTRICTED TO
3-PLC ±		CUSTOMER DRAWING	CAGE CODE	-
4-PLC ±			DRAWING NO 番号	
ANGLES 仕上		SCALE 尺度	2134397	2 OF 2
FINISH 仕上		NTS	REV	B