165-Bump BGA
Commercial Temp
Industrial Temp

# 144Mb SigmaQuad-II+ Burst of 4 SRAM

500 MHz–350 MHz
1.8 V $V_{DD}$
1.8 V or 1.5 V I/O

## Features

- 2.5 Clock Latency
- Simultaneous Read and Write SigmaQuad™ Interface
- JEDEC-standard pinout and package
- Dual Double Data Rate interface
- Byte Write controls sampled at data-in time
- Burst of 4 Read and Write
- Dual-Range On-Die Termination (ODT) on Data (D), Byte Write ($\overline{BW}$), and Clock (K, $\overline{K}$) intputs
- 1.8 V +100/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- Data Valid Pin (QVLD) Support
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump, 15 mm x 17 mm, 1 mm bump pitch BGA package
- RoHS-compliant 165-bump BGA package available

## SigmaQuad™ Family Overview

The GS81302DT06/11/20/38E are built in compliance with the SigmaQuad-II+ SRAM pinout standard for Separate I/O synchronous SRAMs. They are 150,994,944-bit (144Mb) SRAMs. The GS81302DT06/11/20/38E SigmaQuad SRAMs are just one element in a family of low power, low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

## Clocking and Addressing Schemes

The GS81302DT06/11/20/38E SigmaQuad-II+ SRAMs are synchronous devices. They employ two input register clock inputs, K and $\overline{K}$. K and $\overline{K}$ are independent single-ended clock inputs, not differential inputs to a single differential clock input buffer.

Each internal read and write operation in a SigmaQuad-II+ B4 RAM is four times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore the address field of a SigmaQuad-II+ B4 RAM is always two address pins less than the advertised index depth (e.g., the 16M x 8 has a 4M addressable index).

Not Recommended for New Design

## Parameter Synopsis

| | -500 | -450 | -400 | -350 |
|---|---|---|---|---|
| tKHKH | 2.0 ns | 2.2 ns | 2.5 ns | 2.86 ns |
| tKHQV | 0.45 ns | 0.45 ns | 0.45 ns | 0.45 ns |

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## 4M x 36 SigmaQuad-II+ SRAM—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | $\overline{CQ}$ | NC/SA (288Mb) | SA | $\overline{W}$ | $\overline{BW2}$ | $\overline{K}$ | $\overline{BW1}$ | $\overline{R}$ | SA | SA | CQ |
| B | Q27 | Q18 | D18 | SA | $\overline{BW3}$ | K | $\overline{BW0}$ | SA | D17 | Q17 | Q8 |
| C | D27 | Q28 | D19 | $V_{SS}$ | SA | NC | SA | $V_{SS}$ | D16 | Q7 | D8 |
| D | D28 | D20 | Q19 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | Q16 | D15 | D7 |
| E | Q29 | D29 | Q20 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | Q15 | D6 | Q6 |
| F | Q30 | Q21 | D21 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | D14 | Q14 | Q5 |
| G | D30 | D22 | Q22 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | Q13 | D13 | D5 |
| H | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| J | D31 | Q31 | D23 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | D12 | Q4 | D4 |
| K | Q32 | D32 | Q23 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | Q12 | D3 | Q3 |
| L | Q33 | Q24 | D24 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | D11 | Q11 | Q2 |
| M | D33 | Q34 | D25 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | D10 | Q1 | D2 |
| N | D34 | D26 | Q25 | $V_{SS}$ | SA | SA | SA | $V_{SS}$ | Q10 | D9 | D1 |
| P | Q35 | D35 | Q26 | SA | SA | QVLD | SA | SA | Q9 | D0 | Q0 |
| R | TDO | TCK | SA | SA | SA | ODT | SA | SA | SA | TMS | TDI |

11 x 15 Bump BGA—15 x 17 $mm^2$ Body—1 mm Bump Pitch

Notes:
1. $\overline{BW0}$ controls writes to D0:D8; $\overline{BW1}$ controls writes to D9:D17; $\overline{BW2}$ controls writes to D18:D26; $\overline{BW3}$ controls writes to D27:D35
2. Pin A2 is the expansion address.

Not Recommended for New Design

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## 8M x 18 SigmaQuad-II+ SRAM—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | $\overline{CQ}$ | SA | SA | $\overline{W}$ | $\overline{BW1}$ | $\overline{K}$ | NC/SA (288Mb) | $\overline{R}$ | SA | SA | CQ |
| B | NC | Q9 | D9 | SA | NC | K | $\overline{BW0}$ | SA | NC | NC | Q8 |
| C | NC | NC | D10 | $V_{SS}$ | SA | NC | SA | $V_{SS}$ | NC | Q7 | D8 |
| D | NC | D11 | Q10 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | D7 |
| E | NC | NC | Q11 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | D6 | Q6 |
| F | NC | Q12 | D12 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | Q5 |
| G | NC | D13 | Q13 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | D5 |
| H | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| J | NC | NC | D14 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | Q4 | D4 |
| K | NC | NC | Q14 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | D3 | Q3 |
| L | NC | Q15 | D15 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | Q2 |
| M | NC | NC | D16 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | Q1 | D2 |
| N | NC | D17 | Q16 | $V_{SS}$ | SA | SA | SA | $V_{SS}$ | NC | NC | D1 |
| P | NC | NC | Q17 | SA | SA | QVLD | SA | SA | NC | D0 | Q0 |
| R | TDO | TCK | SA | SA | SA | ODT | SA | SA | SA | TMS | TDI |

11 x 15 Bump BGA—15 x 17 $mm^2$ Body—1 mm Bump Pitch

Notes:
1. $\overline{BW0}$ controls writes to D0:D8. $\overline{BW1}$ controls writes to D9:D17.
2. Pin A7 is the expansion address.

Not Recommended for New Design

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## 16M x 9 SigmaQuad-II SRAM—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | $\overline{CQ}$ | SA | SA | $\overline{W}$ | NC | $\overline{K}$ | SA | $\overline{R}$ | SA | SA | CQ |
| B | NC | NC | NC | SA | NC/SA (288Mb) | K | $\overline{BW0}$ | SA | NC | NC | Q4 |
| C | NC | NC | NC | $V_{SS}$ | SA | NC | SA | $V_{SS}$ | NC | NC | D4 |
| D | NC | D5 | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| E | NC | NC | Q5 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | D3 | Q3 |
| F | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| G | NC | D6 | Q6 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| H | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| J | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | Q2 | D2 |
| K | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| L | NC | Q7 | D7 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | Q1 |
| M | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | D1 |
| N | NC | D8 | NC | $V_{SS}$ | SA | SA | SA | $V_{SS}$ | NC | NC | NC |
| P | NC | NC | Q8 | SA | SA | QVLD | SA | SA | NC | D0 | Q0 |
| R | TDO | TCK | SA | SA | SA | ODT | SA | SA | SA | TMS | TDI |

11 x 15 Bump BGA—15 x 17 $mm^2$ Body—1 mm Bump Pitch

Notes:
1. $\overline{BW0}$ controls writes to D0:D8.
2. Pin B5 is the expansion address.

Not Recommended for New Design

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## 16M x 8 SigmaQuad-II SRAM—Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | $\overline{CQ}$ | SA | SA | $\overline{W}$ | $\overline{NW1}$ | $\overline{K}$ | SA | $\overline{R}$ | SA | SA | CQ |
| B | NC | NC | NC | SA | NC/SA (288Mb) | K | $\overline{NW0}$ | SA | NC | NC | Q3 |
| C | NC | NC | NC | $V_{SS}$ | SA | NC | SA | $V_{SS}$ | NC | NC | D3 |
| D | NC | D4 | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| E | NC | NC | Q4 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | D2 | Q2 |
| F | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| G | NC | D5 | Q5 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| H | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| J | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | Q1 | D1 |
| K | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| L | NC | Q6 | D6 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | Q0 |
| M | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | D0 |
| N | NC | D7 | NC | $V_{SS}$ | SA | SA | SA | $V_{SS}$ | NC | NC | NC |
| P | NC | NC | Q7 | SA | SA | QVLD | SA | SA | NC | NC | NC |
| R | TDO | TCK | SA | SA | SA | ODT | SA | SA | SA | TMS | TDI |

11 x 15 Bump BGA—15 x 17 $mm^2$ Body—1 mm Bump Pitch

Notes:
1. $\overline{NW0}$ controls writes to D0:D3. $\overline{NW1}$ controls writes to D4:D7.
2. Pin B5 is the expansion address.

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## Pin Description Table

| Symbol | Description | Type | Comments |
|---|---|---|---|
| SA | Synchronous Address Inputs | Input | — |
| $\overline{R}$ | Synchronous Read | Input | Active Low |
| $\overline{W}$ | Synchronous Write | Input | Active Low |
| $\overline{BW0}$–$\overline{BW3}$ | Synchronous Byte Writes | Input | Active Low<br>x18/x36 only |
| K | Input Clock | Input | Active High |
| $\overline{K}$ | Input Clock | Input | Active Low |
| TMS | Test Mode Select | Input | — |
| TDI | Test Data Input | Input | — |
| TCK | Test Clock Input | Input | — |
| TDO | Test Data Output | Output | — |
| $V_{REF}$ | HSTL Input Reference Voltage | Input | — |
| ZQ | Output Impedance Matching Input | Input | — |
| Qn | Synchronous Data Outputs | Output | — |
| Dn | Synchronous Data Inputs | Input | — |
| $\overline{D}_{\overline{off}}$ | Disable DLL when low | Input | Active Low |
| CQ | Output Echo Clock | Output | — |
| $\overline{CQ}$ | Output Echo Clock | Output | — |
| $V_{DD}$ | Power Supply | Supply | 1.8 V Nominal |
| $V_{DDQ}$ | Isolated Output Buffer Supply | Supply | 1.5 V or 1.8 V Nominal |
| $V_{SS}$ | Power Supply: Ground | Supply | — |
| QVLD | Q Valid Output | Output | — |
| ODT | On-Die Termination | Input | Low = Low Impedance Range<br>High/Float = High Impedance Range |
| NC | No Connect | — | — |

Notes:
1. NC = Not Connected to die or any other pin
2. When ZQ pin is directly connected to $V_{DDQ}$, output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. K and $\overline{K}$ cannot be set to $V_{REF}$ voltage.

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## Background

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the SigmaQuad-II+ SRAM interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads or multiple writes are needed because burst read or write transfers from Separate I/O SRAMs can cut the RAM's bandwidth in half.

### SigmaQuad-II+ Burst of 4 SRAM DDR Read

The status of the Address Input, $\overline{W}$, and $\overline{R}$ pins are sampled by the rising edges of K. $\overline{W}$ and $\overline{R}$ high causes chip disable. A Low on the Read Enable pin, $\overline{R}$, begins a read cycle. $\overline{R}$ is always ignored if the previous command loaded was a read command. Clocking in a High on the Read Enable pin, $\overline{R}$, begins a read port deselect cycle.

### SigmaQuad-II+ Burst of 4 SRAM DDR Write

The status of the Address Input, $\overline{W}$, and $\overline{R}$ pins are sampled by the rising edges of K. $\overline{W}$ and $\overline{R}$ High causes chip disable. A Low on the Write Enable pin, $\overline{W}$, and a High on the Read Enable pin, $\overline{R}$, begins a write cycle. $\overline{W}$ is always ignored if the previous command was a write command. Data is clocked in by the next rising edge of K, the rising edge of $\overline{K}$ after that, the next rising edge of K, and finally by the next rising edge of $\overline{K}$.

## Special Functions

### Byte Write and Nybble Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A High on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{BW0}$ controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven High or Low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 4-beat data transfer. The x18 version of the RAM, for example, may write 72 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Nybble Write (4-bit) control is implemented on the 8-bit-wide version of the device. For the x8 version of the device, "Nybble Write Enable" and "$\overline{NWx}$" may be substituted in all the discussion above.

## Example x18 RAM Write Sequence using Byte Write Enables

| Data In Sample Time | $\overline{BW0}$ | $\overline{BW1}$ | D0–D8 | D9–D17 |
|---|---|---|---|---|
| Beat 1 | 0 | 1 | Data In | Don't Care |
| Beat 2 | 1 | 0 | Don't Care | Data In |
| Beat 3 | 0 | 0 | Data In | Data In |
| Beat 4 | 1 | 0 | Don't Care | Data In |

## Resulting Write Operation

| Byte 1 D0–D8 | Byte 2 D9–D17 | Byte 1 D0–D8 | Byte 2 D9–D17 | Byte 1 D0–D8 | Byte 2 D9–D17 | Byte 1 D0–D8 | Byte 2 D9–D17 |
|---|---|---|---|---|---|---|---|
| Written | Unchanged | Unchanged | Written | Written | Written | Unchanged | Written |
| Beat 1 | | Beat 2 | | Beat 3 | | Beat 4 | |

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## FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaQuad-II+ SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to $V_{SS}$ via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the desired RAM output impedance. The allowable range of RQ to guarantee impedance matching continuously is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

## Input Termination Impedance Control

These SigmaQuad-II+ SRAMs are supplied with programmable input termination on Data (D), Byte Write ($\overline{BW}$), and Clock (K,$\overline{K}$) input receivers. The input termination is always enabled, and the impedance is programmed via the same RQ resistor (connected between the ZQ pin and $V_{SS}$) used to program output driver impedance, in conjuction with the ODT pin (6R). When the ODT pin is tied Low, input termination is "strong" (i.e., low impedance), and is nominally equal to RQ*0.3 Thevenin-equivalent when RQ is between 175Ω and 350Ω. When the ODT pin is tied High (or left floating—the pin has a small pull-up resistor), input termination is "weak" (i.e., high impedance), and is nominally equal to RQ*0.6 Thevenin-equivalent when RQ is between 175Ω and 250Ω. Periodic readjustment of the termination impedance occurs to compensate for drifts in supply voltage and temperature, in the same manner as for driver impedance (see above).

**Note:**
D, $\overline{BW}$, K, $\overline{K}$ inputs should always be driven High or Low; they should never be tri-stated (i.e., in a High-Z state). If the inputs are tri-stated, the input termination will pull the signal to $V_{DDQ}/2$ (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state, resulting in the receiver consuming more power than it normally would. This could result in the device's operating currents being higher.

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## Separate I/O SigmaQuad II+ B4 SRAM Truth Table

| Previous Operation | A | $\overline{R}$ | $\overline{W}$ | Current Operation | D | D | D | D | Q | Q | Q | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K ↑ ($t_{n-1}$) | K ↑ ($t_n$) | K ↑ ($t_n$) | K ↑ ($t_n$) | K ↑ ($t_n$) | K ↑ ($t_{n+1}$) | $\overline{K}$ ↑ ($t_{n+1½}$) | K ↑ ($t_{n+2}$) | $\overline{K}$ ↑ ($t_{n+2½}$) | $\overline{K}$ ↑ ($t_{n+2½}$) | K ↑ ($t_{n+3}$) | $\overline{K}$ ↑ ($t_{n+3½}$) | K ↑ ($t_{n+4}$) |
| Deselect | X | 1 | 1 | Deselect | X | X | — | — | Hi-Z | Hi-Z | — | — |
| Write | X | 1 | X | Deselect | D2 | D3 | — | — | Hi-Z | Hi-Z | — | — |
| Read | X | X | 1 | Deselect | X | X | — | — | Q2 | Q3 | — | — |
| Deselect | V | 1 | 0 | Write | D0 | D1 | D2 | D3 | Hi-Z | Hi-Z | — | — |
| Deselect | V | 0 | X | Read | X | X | — | — | Q0 | Q1 | Q2 | Q3 |
| Read | V | X | 0 | Write | D0 | D1 | D2 | D3 | Q2 | Q3 | — | — |
| Write | V | 0 | X | Read | D2 | D3 | — | — | Q0 | Q1 | Q2 | Q3 |

Notes:
1. "1" = input "high"; "0" = input "low"; "V" = input "valid"; "X" = input "don't care"
2. "—" indicates that the input requirement or output state is determined by the next operation.
3. Q0, Q1, Q2, and Q3 indicate the first, second, third, and fourth pieces of output data transferred during Read operations.
4. D0, D1, D2, and D3 indicate the first, second, third, and fourth pieces of input data transferred during Write operations.
5. Users should not clock in metastable addresses.

Not Recommended for New Design

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## Byte Write Clock Truth Table

| $\overline{BW}$ | $\overline{BW}$ | $\overline{BW}$ | $\overline{BW}$ | Current Operation | D | D | D | D |
|---|---|---|---|---|---|---|---|---|
| K ↑ ($t_{n+1}$) | $\overline{K}$ ↑ ($t_{n+1½}$) | K ↑ ($t_{n+2}$) | $\overline{K}$ ↑ ($t_{n+2½}$) | K ↑ ($t_n$) | K ↑ ($t_{n+1}$) | $\overline{K}$ ↑ ($t_{n+1½}$) | K ↑ ($t_{n+2}$) | $\overline{K}$ ↑ ($t_{n+2½}$) |
| T | T | T | T | Write Dx stored if $\overline{BWn}$ = 0 in all four data transfers | D0 | D2 | D3 | D4 |
| T | F | F | F | Write Dx stored if $\overline{BWn}$ = 0 in 1st data transfer only | D0 | X | X | X |
| F | T | F | F | Write Dx stored if $\overline{BWn}$ = 0 in 2nd data transfer only | X | D1 | X | X |
| F | F | T | F | Write Dx stored if $\overline{BWn}$ = 0 in 3rd data transfer only | X | X | D2 | X |
| F | F | F | T | Write Dx stored if $\overline{BWn}$ = 0 in 4th data transfer only | X | X | X | D3 |
| F | F | F | F | Write Abort No Dx stored in any of the four data transfers | X | X | X | X |

Notes:
1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more $\overline{BWn}$ = 0, then $\overline{BW}$ = "T", else $\overline{BW}$ = "F".

Not Recommended for New Design

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## x36 Byte Write Enable ($\overline{BWn}$) Truth Table

| $\overline{BW0}$ | $\overline{BW1}$ | $\overline{BW2}$ | $\overline{BW3}$ | D0–D8 | D9–D17 | D18–D26 | D27–D35 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Don't Care | Don't Care | Don't Care | Don't Care |
| 0 | 1 | 1 | 1 | Data In | Don't Care | Don't Care | Don't Care |
| 1 | 0 | 1 | 1 | Don't Care | Data In | Don't Care | Don't Care |
| 0 | 0 | 1 | 1 | Data In | Data In | Don't Care | Don't Care |
| 1 | 1 | 0 | 1 | Don't Care | Don't Care | Data In | Don't Care |
| 0 | 1 | 0 | 1 | Data In | Don't Care | Data In | Don't Care |
| 1 | 0 | 0 | 1 | Don't Care | Data In | Data In | Don't Care |
| 0 | 0 | 0 | 1 | Data In | Data In | Data In | Don't Care |
| 1 | 1 | 1 | 0 | Don't Care | Don't Care | Don't Care | Data In |
| 0 | 1 | 1 | 0 | Data In | Don't Care | Don't Care | Data In |
| 1 | 0 | 1 | 0 | Don't Care | Data In | Don't Care | Data In |
| 0 | 0 | 1 | 0 | Data In | Data In | Don't Care | Data In |
| 1 | 1 | 0 | 0 | Don't Care | Don't Care | Data In | Data In |
| 0 | 1 | 0 | 0 | Data In | Don't Care | Data In | Data In |
| 1 | 0 | 0 | 0 | Don't Care | Data In | Data In | Data In |
| 0 | 0 | 0 | 0 | Data In | Data In | Data In | Data In |

## x18 Byte Write Enable ($\overline{BWn}$) Truth Table

| $\overline{BW0}$ | $\overline{BW1}$ | D0–D8 | D9–D17 |
|---|---|---|---|
| 1 | 1 | Don't Care | Don't Care |
| 0 | 1 | Data In | Don't Care |
| 1 | 0 | Don't Care | Data In |
| 0 | 0 | Data In | Data In |

## x09 Byte Write Enable ($\overline{BWn}$) Truth Table

| $\overline{BW0}$ | D0–D8 |
|---|---|
| 1 | Don't Care |
| 0 | Data In |
| 1 | Don't Care |
| 0 | Data In |

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## Nybble Write Clock Truth Table

| $\overline{NW}$ | $\overline{NW}$ | $\overline{NW}$ | $\overline{NW}$ | Current Operation | D | D | D | D |
|---|---|---|---|---|---|---|---|---|
| K ↑ ($t_{n+1}$) | $\overline{K}$ ↑ ($t_{n+1½}$) | K ↑ ($t_{n+2}$) | $\overline{K}$ ↑ ($t_{n+2½}$) | K ↑ ($t_n$) | K ↑ ($t_{n+1}$) | $\overline{K}$ ↑ ($t_{n+1½}$) | K ↑ ($t_{n+2}$) | $\overline{K}$ ↑ ($t_{n+2½}$) |
| T | T | T | T | Write Dx stored if $\overline{NWn}$ = 0 in all four data transfers | D0 | D2 | D3 | D4 |
| T | F | F | F | Write Dx stored if $\overline{NWn}$ = 0 in 1st data transfer only | D0 | X | X | X |
| F | T | F | F | Write Dx stored if $\overline{NWn}$ = 0 in 2nd data transfer only | X | D1 | X | X |
| F | F | T | F | Write Dx stored if $\overline{NWn}$ = 0 in 3rd data transfer only | X | X | D2 | X |
| F | F | F | T | Write Dx stored if $\overline{NWn}$ = 0 in 4th data transfer only | X | X | X | D3 |
| F | F | F | F | Write Abort No Dx stored in any of the four data transfers | X | X | X | X |

Notes:
1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more $\overline{NWn}$ = 0, then $\overline{NW}$ = "T", else $\overline{NW}$ = "F".

## x8 Nybble Write Enable ($\overline{NWn}$) Truth Table

| $\overline{NW0}$ | $\overline{NW1}$ | D0–D3 | D4–D7 |
|---|---|---|---|
| 1 | 1 | Don't Care | Don't Care |
| 0 | 1 | Data In | Don't Care |
| 1 | 0 | Don't Care | Data In |
| 0 | 0 | Data In | Data In |

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## Absolute Maximum Ratings

(All voltages reference to $V_{SS}$)

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ Pins | –0.5 to 2.9 | V |
| $V_{DDQ}$ | Voltage in $V_{DDQ}$ Pins | –0.5 to $V_{DD}$ | V |
| $V_{REF}$ | Voltage in $V_{REF}$ Pins | –0.5 to $V_{DDQ}$ | V |
| $V_{I/O}$ | Voltage on I/O Pins | –0.5 to $V_{DDQ}$ +0.5 (≤ 2.9 V max.) | V |
| $V_{IN}$ | Voltage on Other Input Pins | –0.5 to $V_{DDQ}$ +0.5 (≤ 2.9 V max.) | V |
| $I_{IN}$ | Input Current on Any Pin | +/–100 | mA dc |
| $I_{OUT}$ | Output Current on Any I/O Pin | +/–100 | mA dc |
| $T_J$ | Maximum Junction Temperature | 125 | °C |
| $T_{STG}$ | Storage Temperature | –55 to 125 | °C |

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

## Recommended Operating Conditions

### Power Supplies

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 1.7 | 1.8 | 1.9 | V |
| I/O Supply Voltage | $V_{DDQ}$ | 1.4 | — | $V_{DD}$ | V |
| Reference Voltage | $V_{REF}$ | $V_{DDQ}/2 - 0.05$ | — | $V_{DDQ}/2 + 0.05$ | V |

Notes:
The power supplies need to be powered up simultaneously or in the following sequence: $V_{DD}$, $V_{DDQ}$, $V_{REF}$, followed by signal inputs. The power down sequence must be the reverse. $V_{DDQ}$ must not exceed $V_{DD}$. For more information, read AN1021 SigmaQuad and SigmaDDR Power-Up.

### Operating Temperature

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Junction Temperature (Commercial Range Versions) | $T_J$ | 0 | 25 | 85 | °C |
| Junction Temperature (Industrial Range Versions)* | $T_J$ | –40 | 25 | 100 | °C |

Note:
* The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

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## Thermal Impedance

| Package | Test PCB Substrate | θ JA (C°/W) Airflow = 0 m/s | θ JA (C°/W) Airflow = 1 m/s | θ JA (C°/W) Airflow = 2 m/s | θ JB (C°/W) | θ JC (C°/W) |
|---|---|---|---|---|---|---|
| 165 BGA | 4-layer | 16.4 | 13.4 | 12.4 | 8.6 | 1.2 |

Notes:
1. Thermal Impedance data is based on a number of of samples from mulitple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

## HSTL I/O DC Input Characteristics

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Reference Voltage | $V_{REF}$ | $V_{DDQ}$ /2 – 0.05 | $V_{DDQ}$ /2 + 0.05 | V | — |
| Input High Voltage | $V_{IH1}$ | $V_{REF}$ + 0.1 | $V_{DDQ}$ + 0.3 | V | 1 |
| Input Low Voltage | $V_{IL1}$ | –0.3 | $V_{REF}$ – 0.1 | V | 1 |
| Input High Voltage | $V_{IH2}$ | 0.7 * $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V | 2,3 |
| Input Low Voltage | $V_{IL2}$ | –0.3 | 0.3 * $V_{DDQ}$ | V | 2,3 |

Notes:
1. Parameters apply to K, $\overline{K}$, SA, D, $\overline{R}$, $\overline{W}$, $\overline{BW}$ during normal operation and JTAG boundary scan testing.
2. Parameters apply to Doff, ODT during normal operation and JTAG boundary scan testing.
3. Parameters apply to ZQ during JTAG boundary scan testing only.

## HSTL I/O AC Input Characteristics

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Reference Voltage | $V_{REF}$ | $V_{DDQ}$ /2 – 0.08 | $V_{DDQ}$ /2 + 0.08 | V | — |
| Input High Voltage | $V_{IH1}$ | $V_{REF}$ + 0.2 | $V_{DDQ}$ + 0.5 | V | 1,2,3 |
| Input Low Voltage | $V_{IL1}$ | –0.5 | $V_{REF}$ – 0.2 | V | 1,2,3 |
| Input High Voltage | $V_{IH2}$ | $V_{DDQ}$ – 0.2 | $V_{DDQ}$ + 0.5 | V | 4,5 |
| Input Low Voltage | $V_{IL2}$ | –0.5 | 0.2 | V | 4,5 |

Notes:
1. $V_{IH(MAX)}$ and $V_{IL(MIN)}$ apply for pulse widths less than one-quarter of the cycle time.
2. Input rise and fall times must be a minimum of 1 V/ns, and within 10% of each other.
3. Parameters apply to K, $\overline{K}$, SA, D, $\overline{R}$, $\overline{W}$, $\overline{BW}$ during normal operation and JTAG boundary scan testing.
4. Parameters apply to Doff, ODT during normal operation and JTAG boundary scan testing.
5. Parameters apply to ZQ during JTAG boundary scan testing only.

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## Capacitance

($T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 1.8 V)

| Parameter | Symbol | Test conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0 V | 4 | 5 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V | 6 | 7 | pF |
| Clock Capacitance | $C_{CLK}$ | $V_{IN}$ = 0 V | 5 | 6 | pF |

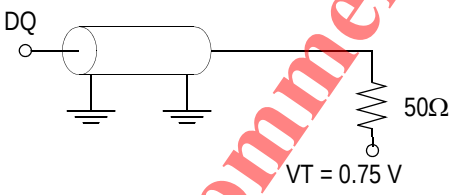
Note:
This parameter is sample tested.

## AC Test Conditions

| Parameter | Conditions |
|---|---|
| Input high level | 1.25 V |
| Input low level | 0.25 V |
| Max. input slew rate | 2 V/ns |
| Input reference level | 0.75 V |
| Output reference level | $V_{DDQ}$/2 |

Note:
Test conditions as specified with output loading as shown unless otherwise noted.

### AC Test Load Diagram




RQ = 250 Ω (HSTL I/O)
$V_{REF}$ = 0.75 V

## Input and Output Leakage Characteristics

| Parameter | Symbol | Test Conditions | Min. | Max |
|---|---|---|---|---|
| Input Leakage Current (except mode pins) | $I_{IL}$ | $V_{IN}$ = 0 to $V_{DD}$ | –2 uA | 2 uA |
| $\overline{\text{Doff}}$ | $I_{IL\overline{DOFF}}$ | $V_{IN}$ = 0 to $V_{DD}$ | –2 uA | 100 uA |
| ODT | $I_{IL\ ODT}$ | $V_{IN}$ = 0 to $V_{DD}$ | –100 uA | 2 uA |
| Output Leakage Current | $I_{OL}$ | Output Disable, $V_{OUT}$ = 0 to $V_{DDQ}$ | –2 uA | 2 uA |

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## Programmable Impedance HSTL Output Driver DC Electrical Characteristics

| Parameter | Symbol | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH1}$ | $V_{DDQ}/2 - 0.12$ | $V_{DDQ}/2 + 0.12$ | V | 1, 3 |
| Output Low Voltage | $V_{OL1}$ | $V_{DDQ}/2 - 0.12$ | $V_{DDQ}/2 + 0.12$ | V | 2, 3 |
| Output High Voltage | $V_{OH2}$ | $V_{DDQ} - 0.2$ | $V_{DDQ}$ | V | 4, 5 |
| Output Low Voltage | $V_{OL2}$ | Vss | 0.2 | V | 4, 6 |

Notes:

1. $I_{OH} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OH} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
2. $I_{OL} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OL} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
3. Parameter tested with $RQ = 250\Omega$ and $V_{DDQ} = 1.5$ V or 1.8 V.
4. $0\Omega \leq RQ \leq \infty\Omega$
5. $I_{OH} = -1.0$ mA
6. $I_{OL} = 1.0$ mA

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## Operating Currents

| Parameter | Symbol | Test Conditions | -500 | | -450 | | -400 | | -350 | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0° to 70°C | –40° to 85°C | 0° to 70°C | –40° to 85°C | 0° to 70°C | –40° to 85°C | 0° to 70°C | –40° to 85°C | |
| Operating Current (x36): DDR | $I_{DD}$ | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA Cycle Time ≥ $t_{KHKH}$ Min | 1660 mA | 1670 mA | 1530 mA | 1540 mA | 1400 mA | 1410 mA | 1170 mA | 1180 mA | 2, 3 |
| Operating Current (x18): DDR | $I_{DD}$ | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA Cycle Time ≥ $t_{KHKH}$ Min | 1360 mA | 1370 mA | 1260 mA | 1270 mA | 1175 mA | 1185 mA | 1055 mA | 1065 mA | 2, 3 |
| Operating Current (x9): DDR | $I_{DD}$ | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA Cycle Time ≥ $t_{KHKH}$ Min | 1260 mA | 1270 mA | 1175 mA | 1185 mA | 1055 mA | 1065 mA | 940 mA | 950 mA | 2, 3 |
| Operating Current (x8): DDR | $I_{DD}$ | $V_{DD}$ = mAx, $I_{OUT}$ = 0 mA Cycle Time ≥ $t_{KHKH}$ Min | 1260 mA | 1270 mA | 1175 mA | 1185 mA | 1055 mA | 1065 mA | 940 mA | 950 mA | 2, 3 |
| Standby Current (NOP): DDR | $I_{SB1}$ | Device deselected, $I^{OUT}$ = 0 mA, f = mAx, All Inputs ≤ 0.2 V or ≥ $V_{DD}$ – 0.2 V | 305 mA | 315 mA | 290 mA | 300 mA | 275 mA | 285 mA | 260 mA | 270 mA | 2, 4 |

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Notes:

1. Power measured with output pins floating.
2. Minimum cycle, $I_{OUT}$ = 0 mA
3. Operating current is calculated with 50% read cycles and 50% write cycles.
4. Standby Current is only after all pending read and write burst operations are completed.


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## AC Electrical Characteristics

| Parameter | Symbol | -500 | | -450 | | -400 | | -350 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| **Clock** | | | | | | | | | | | |
| K, $\overline{K}$ Clock Cycle Time | $t_{KHKH}$ | 2.0 | 8.4 | 2.2 | 8.4 | 2.5 | 8.4 | 2.86 | 8.4 | ns | |
| tK Variable | $t_{KVar}$ | — | 0.15 | — | 0.15 | — | 0.2 | — | 0.2 | ns | 4 |
| K, $\overline{K}$ Clock High Pulse Width | $t_{KHKL}$ | 0.4 | — | 0.4 | — | 0.4 | — | 0.4 | — | cycle | |
| K, $\overline{K}$ Clock Low Pulse Width | $t_{KLKH}$ | 0.4 | — | 0.4 | — | 0.4 | — | 0.4 | — | cycle | |
| K to $\overline{K}$ High | $t_{KH\overline{K}H}$ | 0.85 | — | 0.94 | — | 1.06 | — | 1.23 | — | ns | |
| $\overline{K}$ to K High | $t_{\overline{K}HKH}$ | 0.85 | — | 0.94 | — | 1.06 | — | 1.23 | — | ns | |
| DLL Lock Time | $t_{KLock}$ | 2048 | — | 2048 | — | 2048 | — | 2048 | — | cycle | 5 |
| K Static to DLL reset | $t_{KReset}$ | 30 | — | 30 | — | 30 | — | 30 | — | ns | |
| **Output Times** | | | | | | | | | | | |
| K, $\overline{K}$ Clock High to Data Output Valid | $t_{KHQV}$ | — | 0.45 | — | 0.45 | — | 0.45 | — | 0.45 | ns | |
| K, $\overline{K}$ Clock High to Data Output Hold | $t_{KHQX}$ | –0.45 | — | –0.45 | — | –0.45 | — | –0.45 | — | ns | |
| K, $\overline{K}$ Clock High to Echo Clock Valid | $t_{KHCQV}$ | — | 0.45 | — | 0.45 | — | 0.45 | — | 0.45 | ns | |
| K, $\overline{K}$ Clock High to Echo Clock Hold | $t_{KHCQX}$ | –0.45 | — | –0.45 | — | –0.45 | — | –0.45 | — | ns | |
| CQ, $\overline{CQ}$ High Output Valid | $t_{CQHQV}$ | — | 0.15 | — | 0.15 | — | 0.2 | — | 0.23 | ns | |
| CQ, $\overline{CQ}$ High Output Hold | $t_{CQHQX}$ | –0.15 | — | –0.15 | — | –0.2 | — | –0.23 | — | ns | |
| CQ, $\overline{CQ}$ High to QLVD | $t_{QVLD}$ | –0.15 | 0.15 | –0.15 | 0.15 | –0.2 | 0.2 | –0.23 | 0.23 | ns | |
| CQ Phase Distortion | $t_{CQH\overline{CQ}H}$<br>$t_{\overline{CQ}HCQH}$ | 0.75 | — | 0.85 | — | 1.0 | — | 1.18 | — | ns | |
| K Clock High to Data Output High-Z | $t_{KHQZ}$ | — | 0.45 | — | 0.45 | — | 0.45 | — | 0.45 | ns | |
| K Clock High to Data Output Low-Z | $t_{KHQX1}$ | –0.45 | — | –0.45 | — | –0.45 | — | –0.45 | — | ns | |
| **Setup Times** | | | | | | | | | | | |
| Address Input Setup Time | $t_{AVKH}$ | 0.25 | — | 0.275 | — | 0.4 | — | 0.4 | — | ns | 1 |
| Control Input Setup Time ($\overline{R}$, $\overline{W}$) | $t_{IVKH}$ | 0.25 | — | 0.275 | — | 0.4 | — | 0.4 | — | ns | 2 |
| Control Input Setup Time ($\overline{BWX}$) | $t_{IVKH}$ | 0.2 | — | 0.22 | — | 0.28 | — | 0.28 | — | ns | 3 |
| Data Input Setup Time | $t_{DVKH}$ | 0.2 | — | 0.22 | — | 0.28 | — | 0.28 | — | ns | |
| **Hold Times** | | | | | | | | | | | |
| Address Input Hold Time | $t_{KHAX}$ | 0.25 | — | 0.275 | — | 0.4 | — | 0.4 | — | ns | 1 |
| Control Input Hold Time ($\overline{R}$, $\overline{W}$) | $t_{KHIX}$ | 0.25 | — | 0.275 | — | 0.4 | — | 0.4 | — | ns | 2 |
| Control Input Hold Time ($\overline{BWX}$) | $t_{KHIX}$ | 0.2 | — | 0.22 | — | 0.28 | — | 0.28 | — | ns | 3 |
| Data Input Hold Time | $t_{KHDX}$ | 0.2 | — | 0.22 | — | 0.28 | — | 0.28 | — | ns | |

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Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are $\overline{R}$, $\overline{W}$.
3. Control signals are $\overline{BW0}$, $\overline{BW1}$ and ($\overline{BW2}$, $\overline{BW3}$ for x36).
4. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
5. $V_{DD}$ slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once $V_{DD}$ and input clock are stable.

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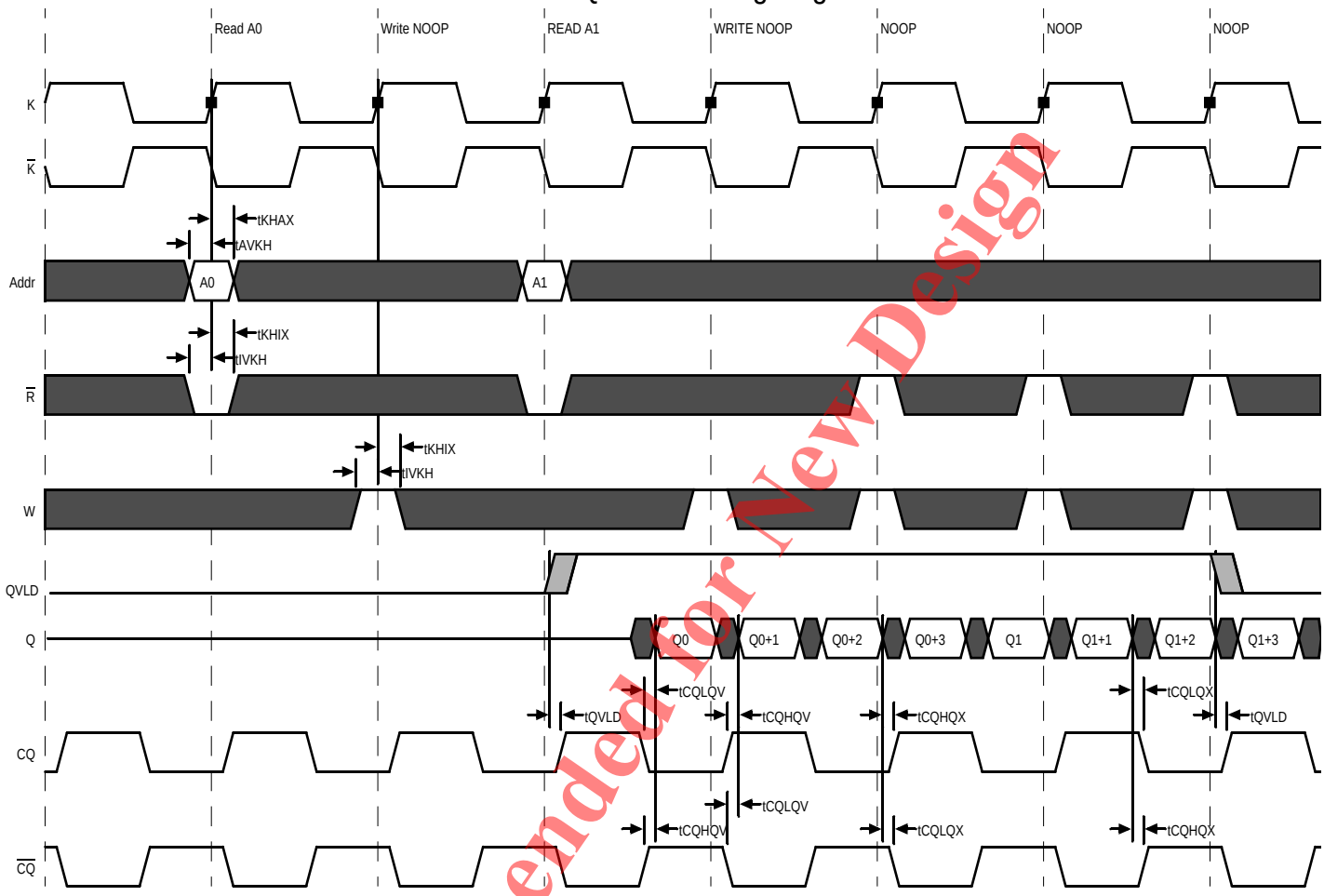
## Read NOP CQ-Based Timing Diagram

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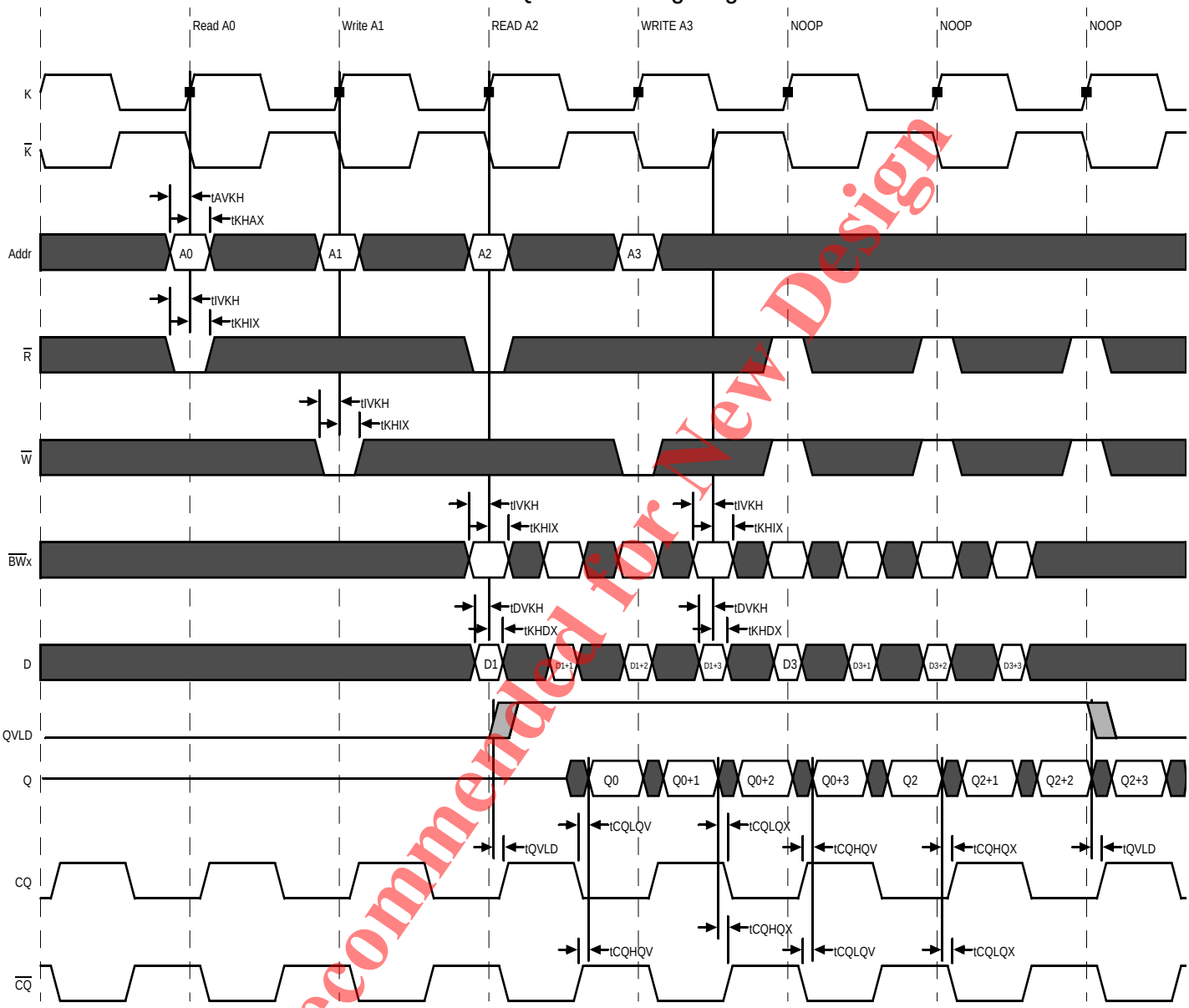
## Read-Write CQ-Based Timing Diagram

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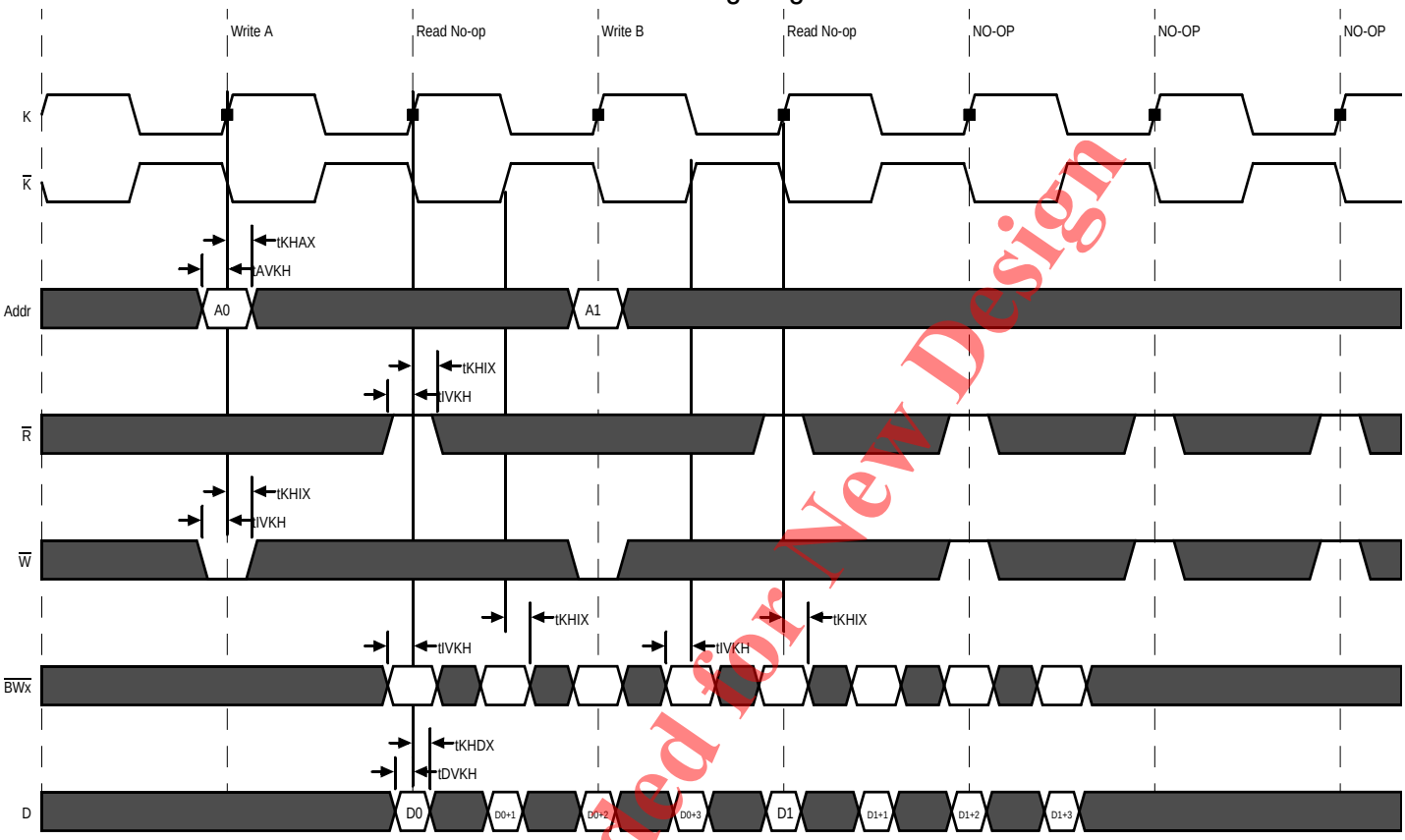
## Write NOP Timing Diagram

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## JTAG Port Operation

### Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with $V_{DD}$. The JTAG output drivers are powered by $V_{DD}$.

### Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either $V_{DD}$ or $V_{SS}$. TDO should be left unconnected.

## JTAG Pin Descriptions

| Pin | Pin Name | I/O | Description |
|---|---|---|---|
| TCK | Test Clock | In | Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK. |
| TMS | Test Mode Select | In | The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level. |
| TDI | Test Data In | In | The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level. |
| TDO | Test Data Out | Out | Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO. |

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

## JTAG Port Registers

### Overview

The various JTAG registers, refered to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

### Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

### Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

### Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan

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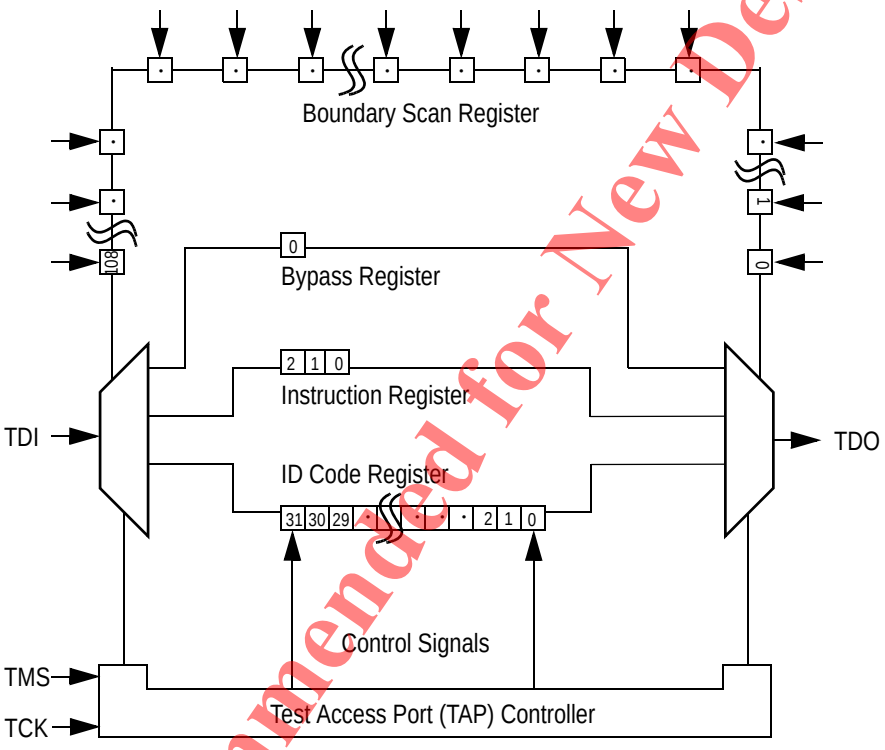
Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram

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### Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

### ID Register Contents

| | See BSDL Model | | | | | | | | | | | | | | | | | | | GSI Technology JEDEC Vendor ID Code | | | | | | | | | | Presence Register |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

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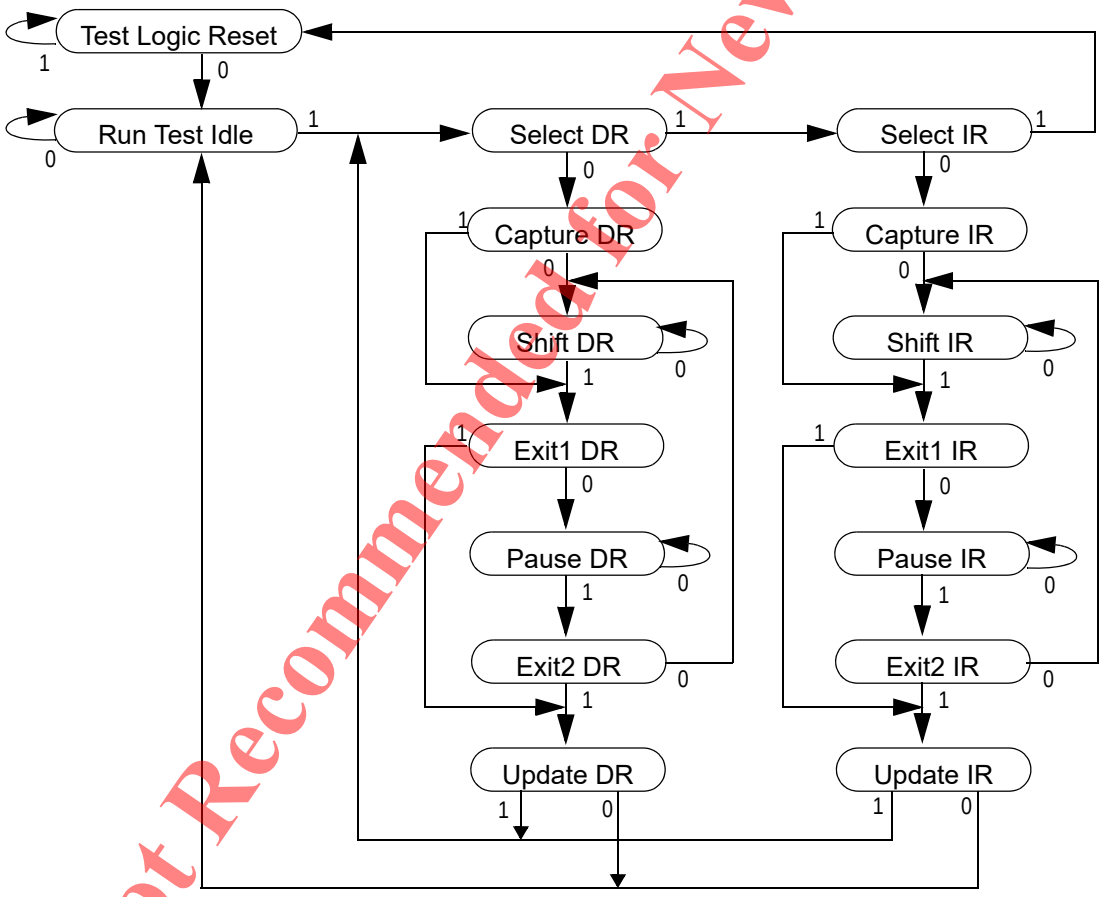
## Tap Controller Instruction Set

### Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram

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### Instruction Descriptions

#### BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

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### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

### EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

### IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

### SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

## JTAG TAP Instruction Set Summary

| Instruction | Code | Description | Notes |
|---|---|---|---|
| EXTEST | 000 | Places the Boundary Scan Register between TDI and TDO. | 1 |
| IDCODE | 001 | Preloads ID Register and places it between TDI and TDO. | 1, 2 |
| SAMPLE-Z | 010 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z. | 1 |
| GSI | 011 | GSI Private Instruction. | 1 |

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## JTAG TAP Instruction Set Summary

| | | | |
|---|---|---|---|
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. | 1 |
| GSI | 101 | GSI Private Instruction. | 1 |
| GSI | 110 | GSI Private Instruction. | 1 |
| BYPASS | 111 | Places Bypass Register between TDI and TDO. | 1 |

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

## JTAG Port Recommended Operating Conditions and DC Characteristics

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Test Port Input Low Voltage | $V_{ILJ}$ | –0.3 | 0.3 * $V_{DD}$ | V | 1 |
| Test Port Input High Voltage | $V_{IHJ}$ | 0.7 * $V_{DD}$ | $V_{DD}$ +0.3 | V | 1 |
| TMS, TCK and TDI Input Leakage Current | $I_{INHJ}$ | –300 | 1 | uA | 2 |
| TMS, TCK and TDI Input Leakage Current | $I_{INLJ}$ | –1 | 100 | uA | 3 |
| TDO Output Leakage Current | $I_{OLJ}$ | –1 | 1 | uA | 4 |
| Test Port Output High Voltage | $V_{OHJ}$ | $V_{DD}$ – 0.2 | — | V | 5, 6 |
| Test Port Output Low Voltage | $V_{OLJ}$ | — | 0.2 | V | 5, 7 |
| Test Port Output CMOS High | $V_{OHJC}$ | $V_{DD}$ – 0.1 | — | V | 5, 8 |
| Test Port Output CMOS Low | $V_{OLJC}$ | — | 0.1 | V | 5, 9 |

Notes:
1. Input Under/overshoot voltage must be –1 V < Vi < $V_{DDn}$ +1 V not to exceed 2.9 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
3. $0\ V \leq V_{IN} \leq V_{ILJn}$
4. Output Disable, $V_{OUT}$ = 0 to $V_{DDn}$
5. The TDO output driver is served by the $V_{DD}$ supply.
6. $I_{OHJ}$ = –2 mA
7. $I_{OLJ}$ = + 2 mA
8. $I_{OHJC}$ = –100 uA
9. $I_{OLJC}$ = +100 uA

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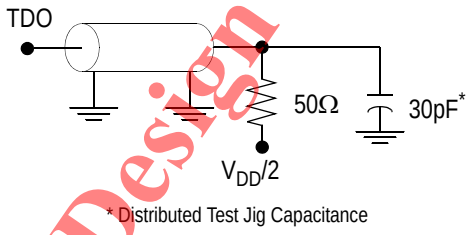
## JTAG Port AC Test Conditions

| Parameter | Conditions |
|---|---|
| Input high level | $V_{DD}$ – 0.2 V |
| Input low level | 0.2 V |
| Input slew rate | 1 V/ns |
| Input reference level | $V_{DD}/2$ |
| Output reference level | $V_{DD}/2$ |

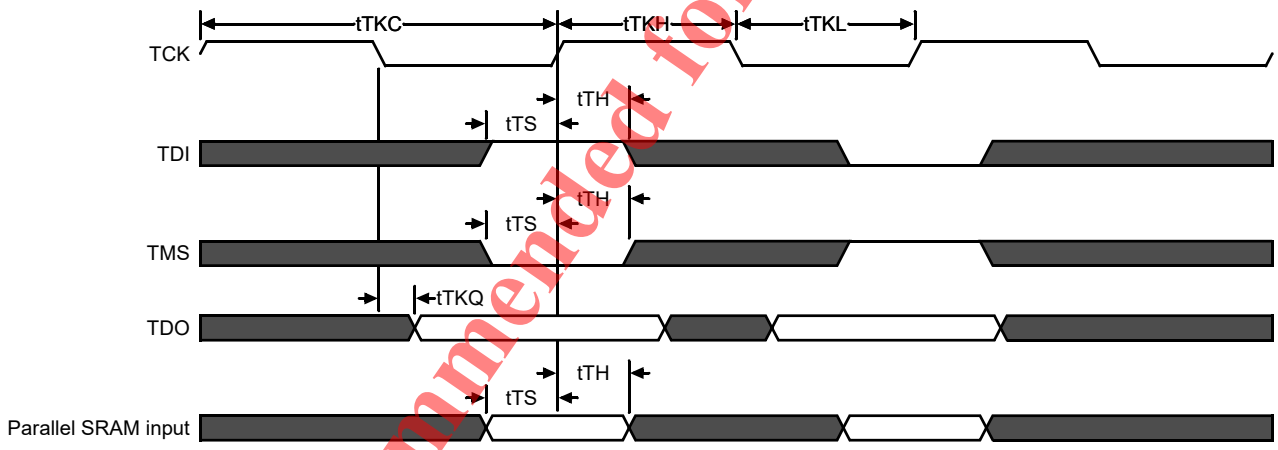
JTAG Port AC Test Load




* Distributed Test Jig Capacitance

Notes:
1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

JTAG Port Timing Diagram




## JTAG Port AC Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| TCK Cycle Time | tTKC | 50 | — | ns |
| TCK Low to TDO Valid | tTKQ | — | 20 | ns |
| TCK High Pulse Width | tTKH | 20 | — | ns |
| TCK Low Pulse Width | tTKL | 20 | — | ns |
| TDI & TMS Set Up Time | tTS | 10 | — | ns |
| TDI & TMS Hold Time | tTH | 10 | — | ns |

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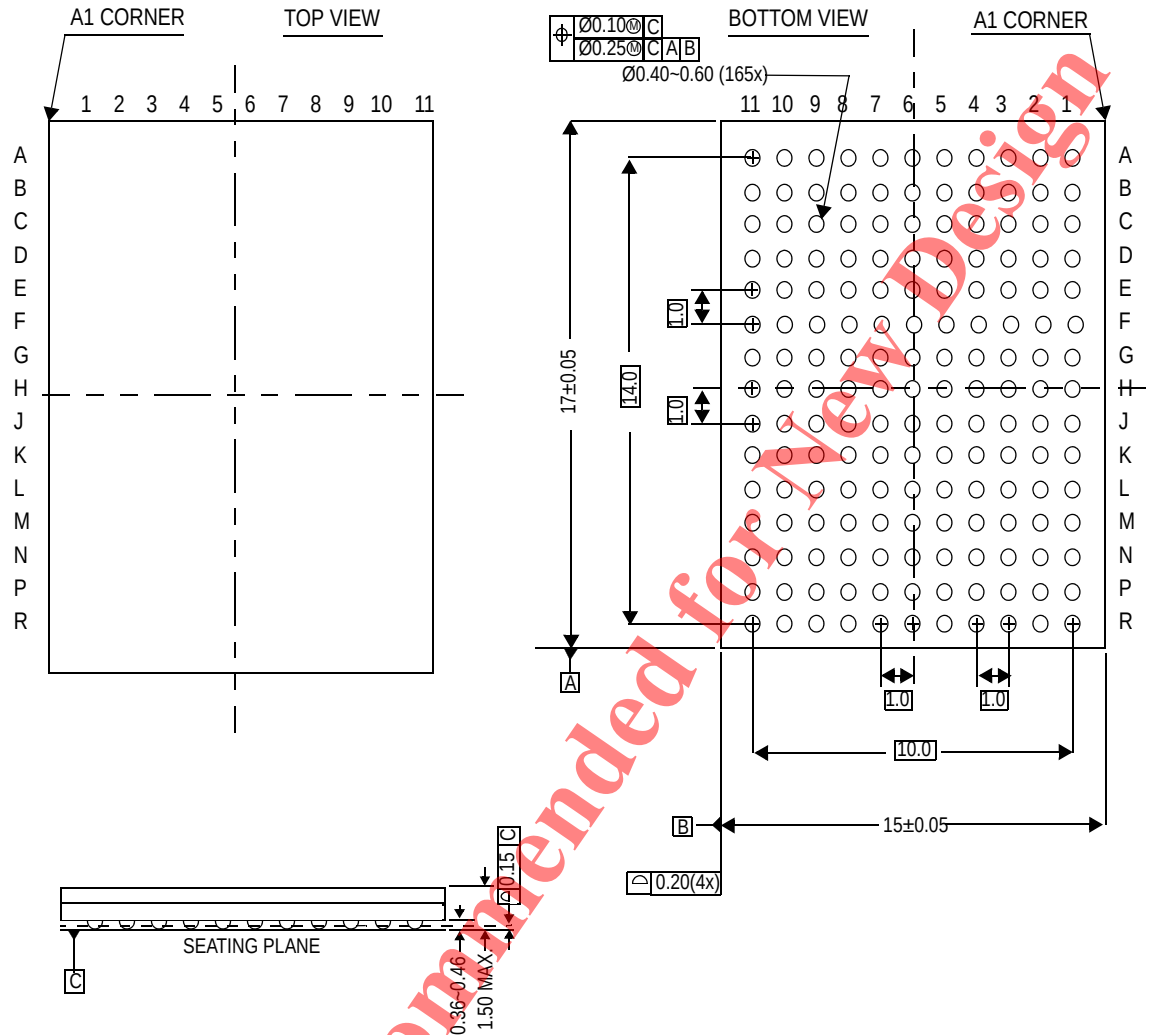
## Package Dimensions—165-Bump FPBGA (Package E)

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## Ordering Information GSI SigmaQuad-II+ SRAM

| Org | Part Number[1] | Type | Package | Speed (MHz) | $T_J$[2] |
|---|---|---|---|---|---|
| 16M x 8 | GS81302DT06E-500 | SigmaQuad-II+ SRAM | 165-bump BGA | 500 | C |
| 16M x 8 | GS81302DT06E-450 | SigmaQuad-II+ SRAM | 165-bump BGA | 450 | C |
| 16M x 8 | GS81302DT06E-400 | SigmaQuad-II+ SRAM | 165-bump BGA | 400 | C |
| 16M x 8 | GS81302DT06E-350 | SigmaQuad-II+ SRAM | 165-bump BGA | 350 | C |
| 16M x 8 | GS81302DT06E-500I | SigmaQuad-II+ SRAM | 165-bump BGA | 500 | I |
| 16M x 8 | GS81302DT06E-450I | SigmaQuad-II+ SRAM | 165-bump BGA | 450 | I |
| 16M x 8 | GS81302DT06E-400I | SigmaQuad-II+ SRAM | 165-bump BGA | 400 | I |
| 16M x 8 | GS81302DT06E-350I | SigmaQuad-II+ SRAM | 165-bump BGA | 350 | I |
| 16M x 8 | GS81302DT06GE-500 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 500 | C |
| 16M x 8 | GS81302DT06GE-450 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 450 | C |
| 16M x 8 | GS81302DT06GE-400 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 400 | C |
| 16M x 8 | GS81302DT06GE-350 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 350 | C |
| 16M x 8 | GS81302DT06GE-500I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 500 | I |
| 16M x 8 | GS81302DT06GE-450I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 450 | I |
| 16M x 8 | GS81302DT06GE-400I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 400 | I |
| 16M x 8 | GS81302DT06GE-350I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 350 | I |
| 16M x 9 | GS81302DT11E-500 | SigmaQuad-II+ SRAM | 165-bump BGA | 500 | C |
| 16M x 9 | GS81302DT11E-450 | SigmaQuad-II+ SRAM | 165-bump BGA | 450 | C |
| 16M x 9 | GS81302DT11E-400 | SigmaQuad-II+ SRAM | 165-bump BGA | 400 | C |
| 16M x 9 | GS81302DT11E-350 | SigmaQuad-II+ SRAM | 165-bump BGA | 350 | C |
| 16M x 9 | GS81302DT11E-500I | SigmaQuad-II+ SRAM | 165-bump BGA | 500 | I |
| 16M x 9 | GS81302DT11E-450I | SigmaQuad-II+ SRAM | 165-bump BGA | 450 | I |
| 16M x 9 | GS81302DT11E-400I | SigmaQuad-II+ SRAM | 165-bump BGA | 400 | I |
| 16M x 9 | GS81302DT11E-350I | SigmaQuad-II+ SRAM | 165-bump BGA | 350 | I |
| 16M x 9 | GS81302DT11GE-500 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 500 | C |
| 16M x 9 | GS81302DT11GE-450 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 450 | C |
| 16M x 9 | GS81302DT11GE-400 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 400 | C |
| 16M x 9 | GS81302DT11GE-350 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 350 | C |
| 16M x 9 | GS81302DT11GE-500I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 500 | I |
| 16M x 9 | GS81302DT11GE-450I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 450 | I |
| 16M x 9 | GS81302DT11GE-400I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 400 | I |

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Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS81302DT38E-400T.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.

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## Ordering Information GSI SigmaQuad-II+ SRAM

| Org | Part Number[1] | Type | Package | Speed (MHz) | $T_J$[2] |
|---|---|---|---|---|---|
| 16M x 9 | GS81302DT11GE-350I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 350 | I |
| 8M x 18 | GS81302DT20E-500 | SigmaQuad-II+ SRAM | 165-bump BGA | 500 | C |
| 8M x 18 | GS81302DT20E-450 | SigmaQuad-II+ SRAM | 165-bump BGA | 450 | C |
| 8M x 18 | GS81302DT20E-400 | SigmaQuad-II+ SRAM | 165-bump BGA | 400 | C |
| 8M x 18 | GS81302DT20E-350 | SigmaQuad-II+ SRAM | 165-bump BGA | 350 | C |
| 8M x 18 | GS81302DT20E-500I | SigmaQuad-II+ SRAM | 165-bump BGA | 500 | I |
| 8M x 18 | GS81302DT20E-450I | SigmaQuad-II+ SRAM | 165-bump BGA | 450 | I |
| 8M x 18 | GS81302DT20E-400I | SigmaQuad-II+ SRAM | 165-bump BGA | 400 | I |
| 8M x 18 | GS81302DT20E-350I | SigmaQuad-II+ SRAM | 165-bump BGA | 350 | I |
| 8M x 18 | GS81302DT20GE-500 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 500 | C |
| 8M x 18 | GS81302DT20GE-450 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 450 | C |
| 8M x 18 | GS81302DT20GE-400 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 400 | C |
| 8M x 18 | GS81302DT20GE-350 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 350 | C |
| 8M x 18 | GS81302DT20GE-500I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 500 | I |
| 8M x 18 | GS81302DT20GE-450I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 450 | I |
| 8M x 18 | GS81302DT20GE-400I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 400 | I |
| 8M x 18 | GS81302DT20GE-350I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 350 | I |
| 4M x 36 | GS81302DT38E-500 | SigmaQuad-II+ SRAM | 165-bump BGA | 500 | C |
| 4M x 36 | GS81302DT38E-450 | SigmaQuad-II+ SRAM | 165-bump BGA | 450 | C |
| 4M x 36 | GS81302DT38E-400 | SigmaQuad-II+ SRAM | 165-bump BGA | 400 | C |
| 4M x 36 | GS81302DT38E-350 | SigmaQuad-II+ SRAM | 165-bump BGA | 350 | C |
| 4M x 36 | GS81302DT38E-550I | SigmaQuad-II+ SRAM | 165-bump BGA | 550 | I |
| 4M x 36 | GS81302DT38E-500I | SigmaQuad-II+ SRAM | 165-bump BGA | 500 | I |
| 4M x 36 | GS81302DT38E-450I | SigmaQuad-II+ SRAM | 165-bump BGA | 450 | I |
| 4M x 36 | GS81302DT38E-400I | SigmaQuad-II+ SRAM | 165-bump BGA | 400 | I |
| 4M x 36 | GS81302DT38E-350I | SigmaQuad-II+ SRAM | 165-bump BGA | 350 | I |
| 4M x 36 | GS81302DT38GE-500 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 500 | C |
| 4M x 36 | GS81302DT38GE-450 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 450 | C |
| 4M x 36 | GS81302DT38GE-400 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 400 | C |
| 4M x 36 | GS81302DT38GE-350 | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 350 | C |
| 4M x 36 | GS81302DT38GE-500I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 500 | I |

Not Recommended for New Design

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS81302DT38E-400T.
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## Ordering Information GSI SigmaQuad-II+ SRAM

| Org | Part Number[1] | Type | Package | Speed (MHz) | $T_J$[2] |
|---|---|---|---|---|---|
| 4M x 36 | GS81302DT38GE-450I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 450 | I |
| 4M x 36 | GS81302DT38GE-400I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 400 | I |
| 4M x 36 | GS81302DT38E-350I | SigmaQuad-II+ SRAM | RoHS-compliant 165-bump BGA | 350 | I |

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS81302DT38E-400T.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.

## SigmaQuad-II+ SRAM Revision History

| File Name | Format/Content | Description of changes |
|---|---|---|
| 81302DT2038E_r1 | Content | • Creation of datasheet<br>• (Rev1.00a: Added missing x18/x36 IDD numbers)<br>• (Rev1.00b: Editorial updates) |
| 81302DT2038E_r1_01 | Content | • Addition of 550 MHz for x18/x36<br>• Update for MP status |
| 81302DT2038E_r1_02 | Content | • Removed 550 MHz speed bin<br>• (Rev1.02a: Added missing IDD numbers for x36/x18)<br>• (Rev1.02b: Corrected note column information on op curr table)<br>• (Rev1.02c: Corrected erroneous information in Input and Output Leakage Characteristics table) |

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