

16-Mbit (512 K words × 32 bits) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
 - $t_{AA} = 10 \text{ ns}/15 \text{ ns}$
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby current
 - $I_{CC} = 90 \text{ mA}$ typical
 - $I_{SB2} = 20 \text{ mA}$ typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V
- 1.0-V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 119-ball plastic ball grid array (PBGA) package

Functional Description

CY7C1062G and CY7C1062GE are high-performance CMOS fast static RAM devices with embedded ECC. Both have three chip enables, giving easy memory expansion features. The CY7C1062GE device includes an error indication pin that signals the host processor in the case of a single bit error-detection and correction event.

To write to the device, take Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW) and Write Enable ($\overline{WE}$) input LOW. If Byte Enable A ($\overline{B}_A$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{18}). If Byte Enable B ($\overline{B}_B$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}). Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond with the I/O pins I/O_{16} to I/O_{23} and I/O_{24} to I/O_{31} , respectively.

To read from the device, take Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If the first $\overline{B}_A$ is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If $\overline{B}_B$ is LOW, then data from memory appears on I/O_8 to I/O_{15} . Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond to the third and fourth bytes. See [Truth Table – CY7C1062G/CY7C1062GE on page 15](#) for a complete description of read and write modes.

The input and output pins (I/O_0 through I/O_{31}) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the byte selects are disabled ($\overline{B}_{A-D}$ HIGH), or during a write operation ($\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$ LOW and $\overline{WE}$ LOW).

On the CY7C1062GE device, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High)^[1].

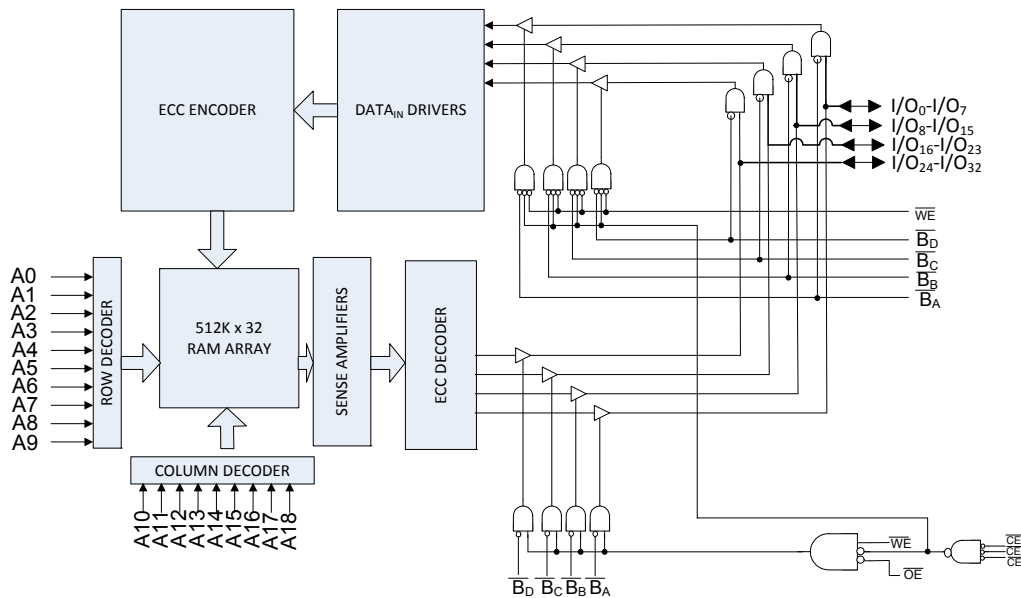
CY7C1062G and CY7C1062GE devices are available in Pb-free 119-ball plastic ball grid array (PBGA) package.

For a complete list of related documentation, click [here](#).

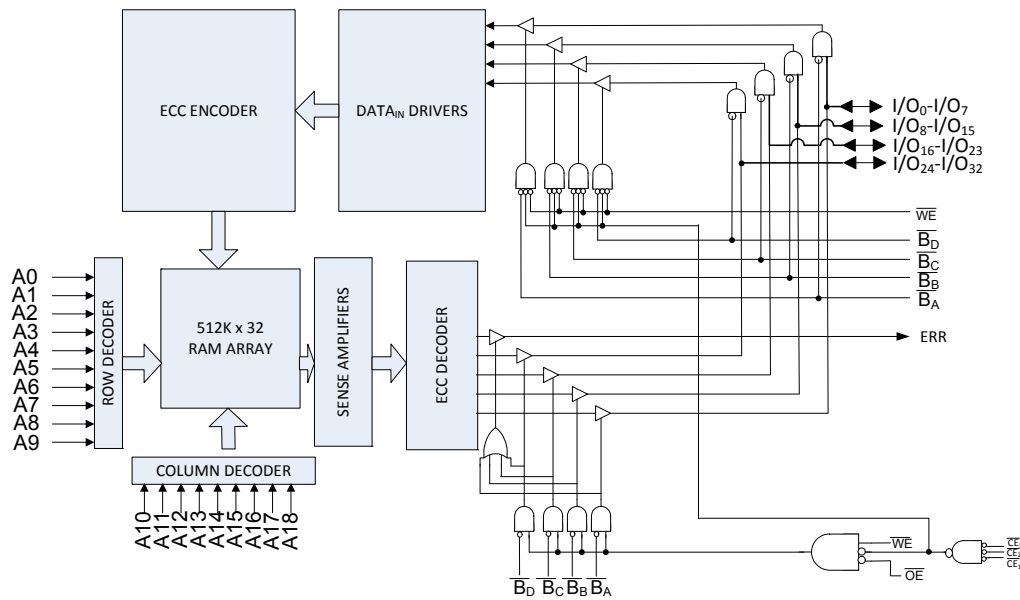
Note

1. This device does not support automatic write-back on error detection.

Logic Block Diagram – CY7C1062G



Logic Block Diagram – CY7C1062GE



Contents

Pin Configurations	4	Ordering Information	16
Product Portfolio	5	Ordering Code Definitions	16
Maximum Ratings	6	Package Diagrams	17
Operating Range	6	Acronyms	18
DC Electrical Characteristics	6	Document Conventions	18
Capacitance	7	Units of Measure	18
Thermal Resistance	7	Document History Page	19
AC Test Loads and Waveforms	7	Sales, Solutions, and Legal Information	20
Data Retention Characteristics	8	Worldwide Sales and Design Support	20
Data Retention Waveform	8	Products	20
AC Switching Characteristics	9	PSoC® Solutions	20
Switching Waveforms	10	Cypress Developer Community	20
Truth Table – CY7C1062G/CY7C1062GE	15	Technical Support	20
ERR Output – CY7C1062GE	15		

Pin Configurations

Figure 1. 119-ball PBGA Pinout (Top View) - CY7C1062G ^[2]

	1	2	3	4	5	6	7
A	I/O ₁₆	A ₄	A ₃	A ₂	A ₁	A ₀	I/O ₀
B	I/O ₁₇	A ₁₈	A ₁₇	$\overline{CE}_1$	A ₁₆	A ₁₅	I/O ₁
C	I/O ₁₈	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O ₂
D	I/O ₁₉	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₃
E	I/O ₂₀	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₄
F	I/O ₂₁	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₅
G	I/O ₂₂	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₆
H	I/O ₂₃	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₇
J	NC	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	NC
K	I/O ₂₄	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₈
L	I/O ₂₅	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₉
M	I/O ₂₆	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₀
N	I/O ₂₇	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₁₁
P	I/O ₂₈	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₂
R	I/O ₂₉	A ₁₄	B _d	NC	B _b	A ₁₃	I/O ₁₃
T	I/O ₃₀	A ₁₂	A ₁₁	$\overline{WE}$	A ₁₀	A ₉	I/O ₁₄
U	I/O ₃₁	A ₈	A ₇	$\overline{OE}$	A ₆	A ₅	I/O ₁₅

Figure 2. 119-ball PBGA Pinout (Top View) - CY7C1062GE ^[2]

	1	2	3	4	5	6	7
A	I/O ₁₆	A ₄	A ₃	A ₂	A ₁	A ₀	I/O ₀
B	I/O ₁₇	A ₁₈	A ₁₇	$\overline{CE}_1$	A ₁₆	A ₁₅	I/O ₁
C	I/O ₁₈	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O ₂
D	I/O ₁₉	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₃
E	I/O ₂₀	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₄
F	I/O ₂₁	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₅
G	I/O ₂₂	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₆
H	I/O ₂₃	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₇
J	ERR	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	NC
K	I/O ₂₄	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₈
L	I/O ₂₅	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₉
M	I/O ₂₆	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₀
N	I/O ₂₇	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₁₁
P	I/O ₂₈	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₂
R	I/O ₂₉	A ₁₄	B _d	NC	B _b	A ₁₃	I/O ₁₃
T	I/O ₃₀	A ₁₂	A ₁₁	$\overline{WE}$	A ₁₀	A ₉	I/O ₁₄
U	I/O ₃₁	A ₈	A ₇	$\overline{OE}$	A ₆	A ₅	I/O ₁₅

Note

- NC pins are not connected internally to the die.
- ERR is an Output pin. If not used, this pin should be left floating.

Product Portfolio

Product	Features and Options (see Pin Configurations on page 4)	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I _{CC} , (mA)		Standby, I _{SB2} (mA)	
					f = f _{max}			
					Typ ^[4]	Max	Typ ^[4]	Max
CY7C1062G18	Embedded ECC. No ERR output pin	Industrial	1.65 V–2.2 V	15	70	80	20	30
CY7C1062G30			2.2 V–3.6 V	10	90	110		
CY7C1062GE18	Embedded ECC. Optional ERR output pin		1.65 V–2.2 V	15	70	80		
CY7C1062GE30			2.2 V–3.6 V	10	90	110		

Notes

4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V and (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} relative to GND -0.5 V to $V_{CC} + 0.5$ V

DC voltage applied to outputs in High Z State ^[5] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[5] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range of -40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit
			Min	Typ ^[6]	Max	
V_{OH}	Output HIGH Voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA	1.4	—	—	V
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0$ mA	2.0	—	—	
		2.7 V to 3.0 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.2	—	—	
		3.0 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.4	—	—	
V_{OL}	Output LOW Voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OL} = 0.1$ mA	—	—	0.2	
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2$ mA	—	—	0.4	
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8$ mA	—	—	0.4	
V_{IH}	Input HIGH Voltage	1.65 V to 2.2 V —	1.4	—	$V_{CC} + 0.2$	
		2.2 V to 2.7 V —	2.0	—	$V_{CC} + 0.3$	
		2.7 V to 3.6 V —	2.0	—	$V_{CC} + 0.3$	
V_{IL}	Input LOW Voltage ^[5]	1.65 V to 2.2 V —	-0.2	—	0.4	
		2.2 V to 2.7 V —	-0.3	—	0.6	
		2.7 V to 3.6 V —	-0.3	—	0.8	
I_{IX}	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	-1.0	—	+1.0	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled	-1.0	—	+1.0	
I_{CC}	Operating Supply Current	$V_{CC} = \text{Max}, I_{OUT} = 0$ mA, CMOS levels $f = 100$ MHz	—	90.0	110.0	mA
		$f = 66.7$ MHz	—	70.0	80.0	
I_{SB1}	Automatic CE Power-down Current – TTL Inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$ ^[7] , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	—	—	40.0	
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.2$ V ^[7] , $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$	—	20.0	30.0	

Notes

5. $V_{IL(\text{min})} = -2.0$ V and $V_{IH(\text{max})} = V_{CC} + 2$ V for pulse durations of less than 20 ns.

6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8$ V (for V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3$ V (for V_{CC} range of 2.2 V–3.6 V), and $T_A = 25$ °C.

7. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.

Capacitance

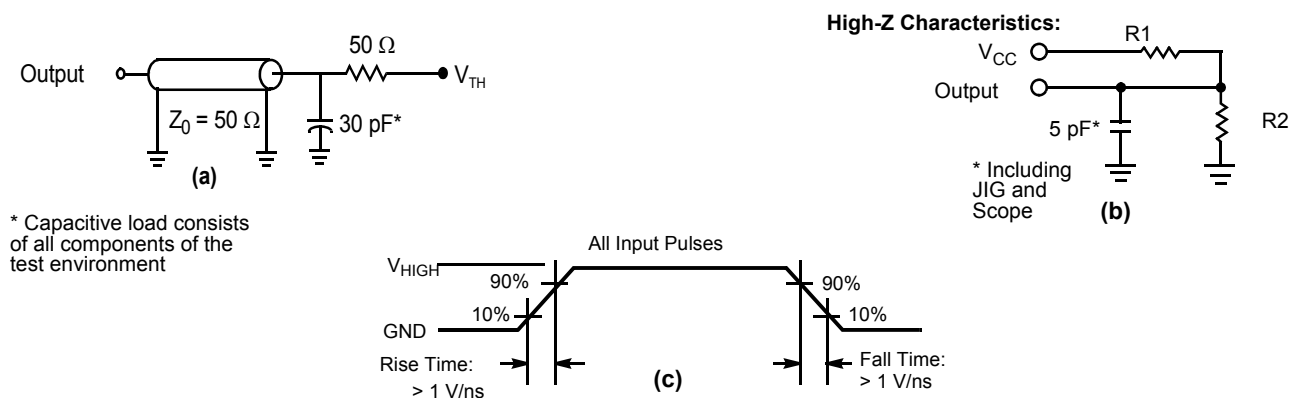
Parameter ^[8]	Description	Test Conditions	119-ball PBGA	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	I/O Capacitance			

Thermal Resistance

Parameter ^[8]	Description	Test Conditions	119-ball PBGA	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	20.92	$^\circ\text{C/W}$
Θ_{JC}	Thermal Resistance (junction to case)		15.84	

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[9]



Parameters	1.8 V	3.0 V	Unit
R1	1667	317	Ω
R2	1538	351	
V_{TH}	0.9	1.5	V
V_{HIGH}	1.8	3.0	

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device AC operation assumes a 100- μs ramp time from 0 to V_{CC} (min) and 100- μs wait time after V_{CC} stabilizes to its operational value.

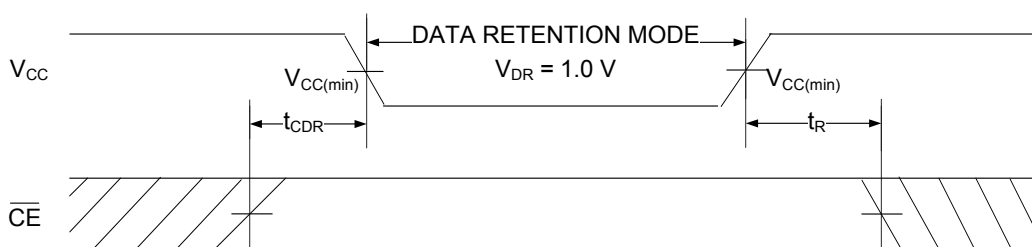
Data Retention Characteristics

Over the Operating Range of -40°C to 85°C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	–	1.0	–	V
I_{CCDR}	Data Retention Current	$V_{\text{CC}} = V_{\text{DR}}$, $\overline{\text{CE}} \geq V_{\text{CC}} - 0.2 \text{ V}$ [10], $V_{\text{IN}} \geq V_{\text{CC}} - 0.2 \text{ V}$ or $V_{\text{IN}} \leq 0.2 \text{ V}$	–	30.0	mA
$t_{\text{CDR}}^{[11]}$	Chip Deselect to Data Retention Time	–	0.0	–	ns
$t_{\text{R}}^{[11, 12]}$	Operation Recovery Time	$V_{\text{CC}} \geq 2.2 \text{ V}$	10.0	–	
		$V_{\text{CC}} < 2.2 \text{ V}$	15.0	–	

Data Retention Waveform

Figure 4. Data Retention Waveform [10]



Notes

10. $\overline{\text{CE}}$ indicates a combination of all three chip enables. When active LOW, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, and $\overline{\text{CE}}_3$ LOW. When HIGH, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ HIGH.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{\text{CC(min.)}} \geq 100 \mu\text{s}$ or stable at $V_{\text{CC(min.)}} \geq 100 \mu\text{s}$.

AC Switching Characteristics

Over the Operating Range of -40 °C to 85 °C

Parameter ^[13]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{POWER}	V _{CC} (stable) to the first access ^[14, 15]	100.0	–	100.0	–	μs
t _{RC}	Read cycle time	10.0	–	15.0	–	ns
t _{AA}	Address to data / ERR valid	–	10.0	–	15.0	
t _{OHA}	Data / ERR hold from address change	3.0	–	3.0	–	
t _{ACE}	$\overline{CE}$ LOW to data / ERR valid ^[16]	–	10.0	–	15.0	
t _{DOE}	$\overline{OE}$ LOW to data / ERR valid	–	5.0	–	8.0	
t _{LZOE}	$\overline{OE}$ LOW to low Z ^[17, 18]	0.0	–	1.0	–	
t _{HZOE}	$\overline{OE}$ HIGH to high Z ^[17, 18]	–	5.0	–	8.0	
t _{LZCE}	$\overline{CE}$ LOW to low Z ^[16, 17, 18]	3.0	–	3.0	–	
t _{HZCE}	$\overline{CE}$ HIGH to high Z ^[16, 17, 18]	–	5.0	–	8.0	
t _{PU}	$\overline{CE}$ LOW to power-up ^[15, 16]	0.0	–	0.0	–	
t _{PD}	$\overline{CE}$ HIGH to power-down ^[15, 16]	–	10.0	–	15.0	
t _{DBE}	Byte enable to data valid	–	5.0	–	8.0	
t _{LZBE}	Byte enable to low Z	0.0	–	1.0	–	
t _{HZBE}	Byte disable to high Z	–	6.0	–	8.0	
Write Cycle ^[19, 20]						
t _{WC}	Write cycle time	10.0	–	15.0	–	ns
t _{SCE}	$\overline{CE}$ LOW to write end ^[16]	7.0	–	12.0	–	
t _{AW}	Address setup to write end	7.0	–	12.0	–	
t _{HA}	Address hold from write end	0.0	–	0.0	–	
t _{SA}	Address setup to write start	0.0	–	0.0	–	
t _{PWE}	$\overline{WE}$ pulse width	7.0	–	12.0	–	
t _{SD}	Data setup to write end	5.0	–	8.0	–	
t _{HD}	Data hold from write end	0.0	–	0.0	–	
t _{LZWE}	$\overline{WE}$ HIGH to low Z ^[17, 18]	3.0	–	3.0	–	
t _{HZWE}	$\overline{WE}$ LOW to high Z ^[17, 18]	–	5.0	–	8.0	
t _{BW}	Byte Enable to write end	7.0	–	12.0	–	

Notes

13. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V_{CC} ≥ 3 V) and V_{CC}/2 (for V_{CC} < 3 V), and input pulse levels of 0 to 3 V (for V_{CC} ≥ 3 V) and 0 to V_{CC} (for V_{CC} < 3V). Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 7, unless specified otherwise.

14. t_{POWER} gives minimum amount of time that the power supply is at stable V_{CC} until first memory access is performed.

15. These parameters are guaranteed by design and are not tested.

16. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{CE}_3$ HIGH.

17. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 7. Transition is measured ±200 mV from steady state voltage.

18. Tested initially and after any design or process changes that may affect these parameters.

19. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

20. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ Low) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY7C1062G (Address Transition Controlled) [21, 22]

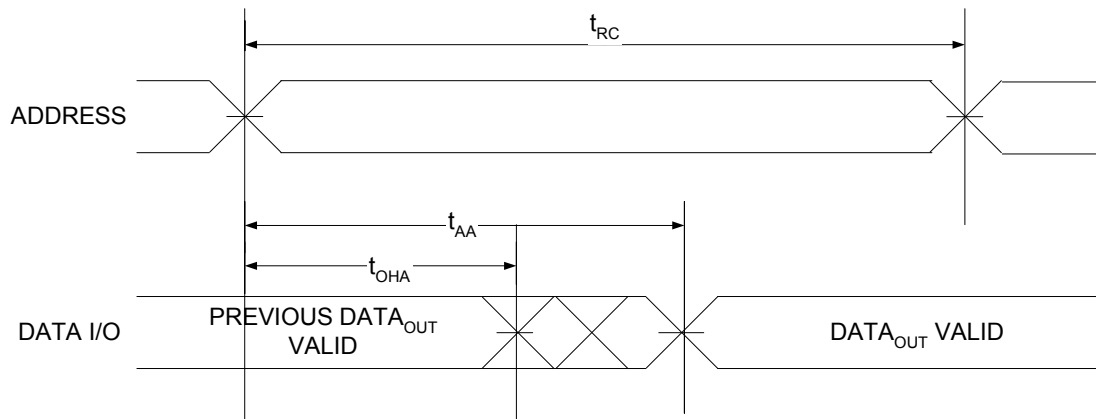
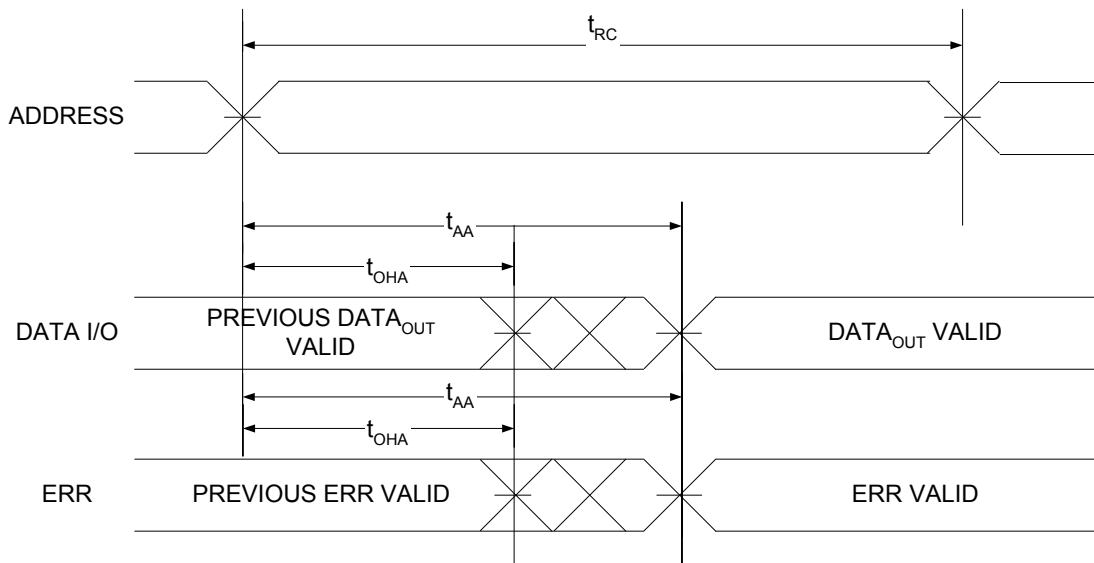


Figure 6. Read Cycle No. 1 of CY7C1062GE (Address Transition Controlled) [21, 22]

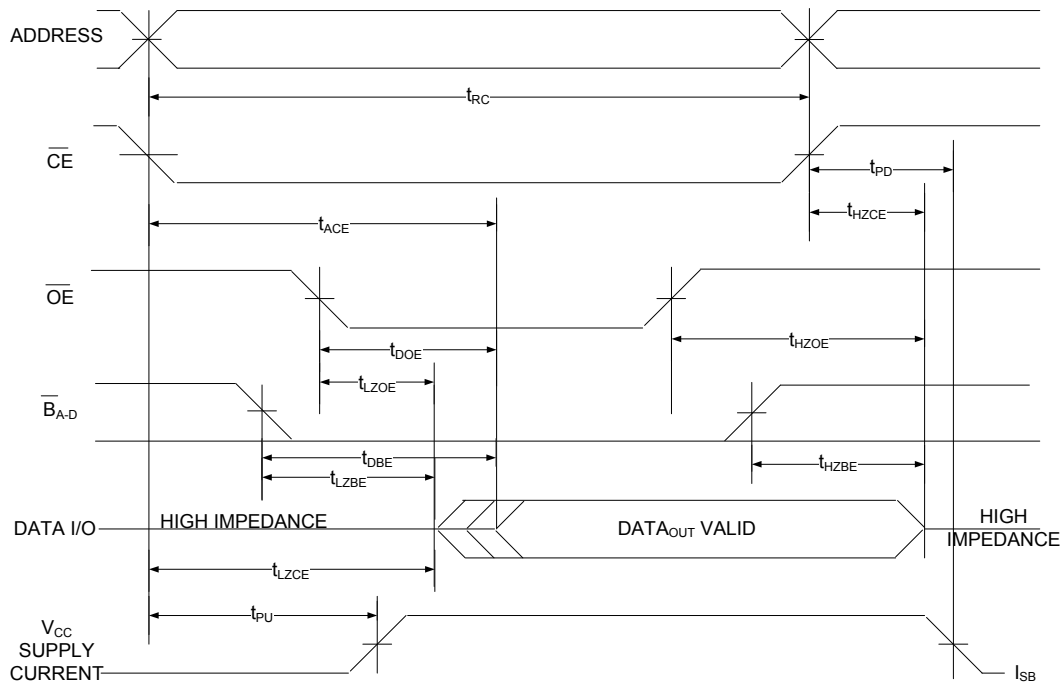


Notes

21. The device is continuously selected, $\overline{OE}$, $\overline{CE}$, $\overline{BA}$, $\overline{BB}$, $\overline{BC}$, $\overline{BD}$ = V_{IL} .
22. WE is HIGH for read cycle.

Switching Waveforms (continued)

Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [23, 24, 25]



Notes

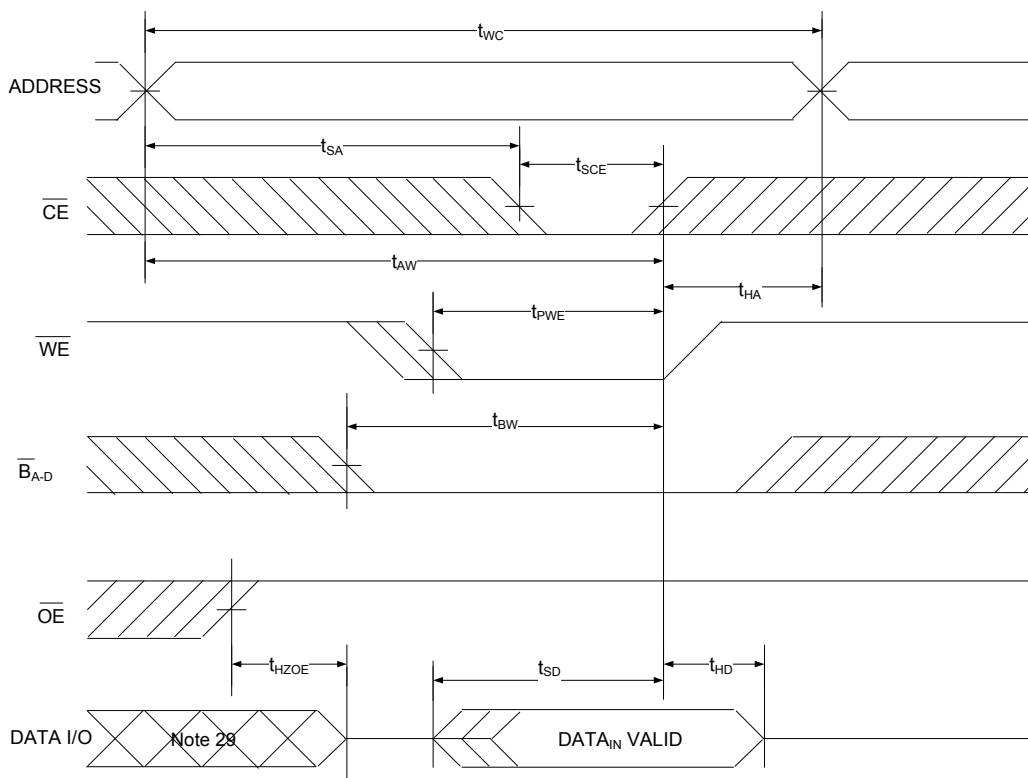
23. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.

24. $\overline{WE}$ is HIGH for read cycle.

25. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [26, 27, 28]



Notes

26. $\overline{\text{CE}}$ indicates a combination of all three chip enables. When active LOW, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, and $\overline{\text{CE}}_3$ LOW. When HIGH, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ HIGH.

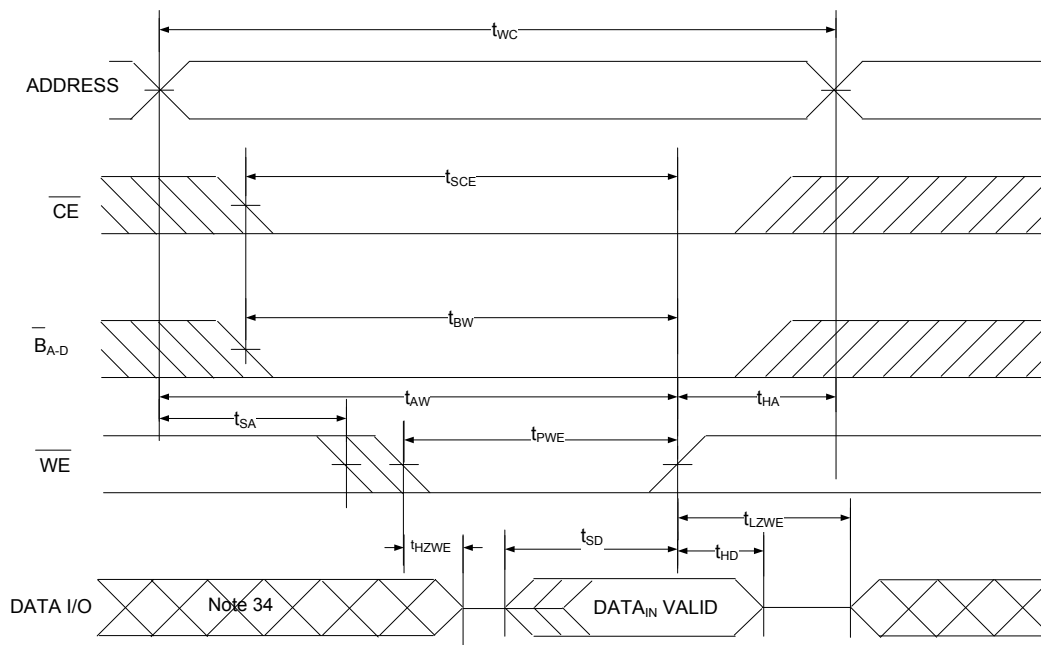
27. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

28. Data I/O is high impedance if $\overline{\text{CE}}$ or $\overline{\text{OE}}$ or $\overline{\text{BA}}_A$, $\overline{\text{BA}}_B$, $\overline{\text{BA}}_C$, $\overline{\text{BA}}_D = V_{IH}$.

29. During this period I/O are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ Low) [30, 31, 32, 33]

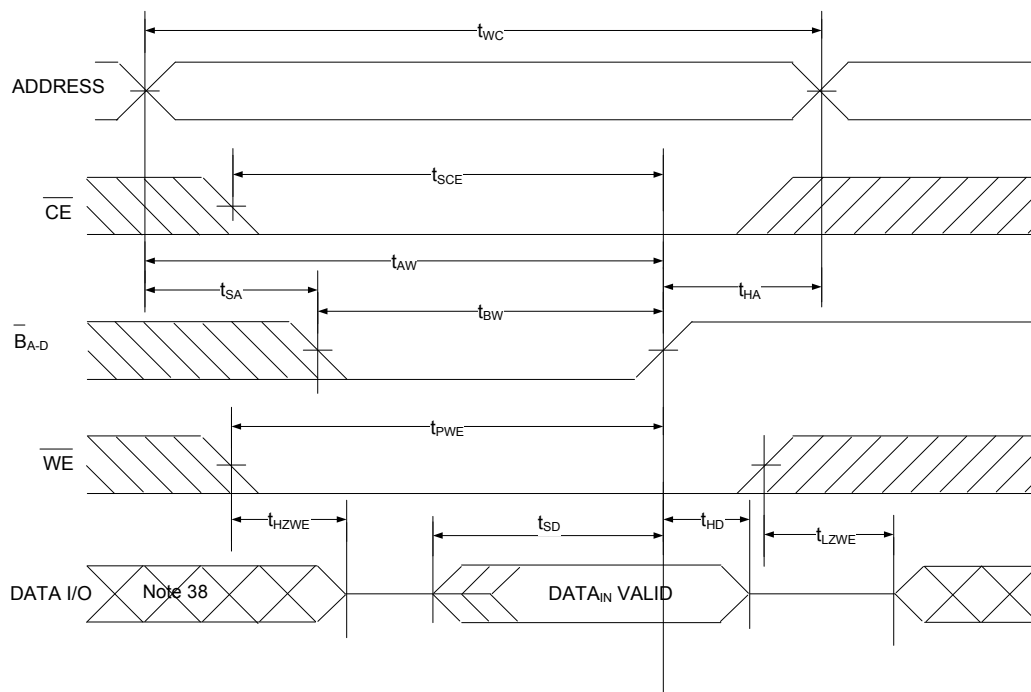


Notes

30. $\overline{\text{CE}}$ indicates a combination of all three chip enables. When active LOW, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, and $\overline{\text{CE}}_3$ LOW. When HIGH, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ HIGH.
31. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
32. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{B}}_{\text{A}}$, $\overline{\text{B}}_{\text{B}}$, $\overline{\text{B}}_{\text{C}}$, $\overline{\text{B}}_{\text{D}} = V_{\text{IH}}$.
33. The minimum write cycle pulse width should be equal to sum of t_{HZWE} and t_{SD} .
34. During this period I/O are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ Controlled) [35, 36, 37]



Notes

35. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH.
36. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
37. Data I/O is high impedance if $\overline{OE}$ or $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D = V_{IH}$.
38. During this period I/O are in output state. Do not apply input signals.

Truth Table – CY7C1062G/CY7C1062GE

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{CE}_3$	$\overline{OE}$	$\overline{WE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	I/O ₁₆ –I/O ₂₃	I/O ₂₄ –I/O ₃₁	Mode	Power
H	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	High Z	High Z	High Z	High Z	power-down	(I _{SB})
X ^[39]	H	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	High Z	High Z	High Z	High Z	power-down	(I _{SB})
X ^[39]	X ^[39]	H	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	X ^[39]	High Z	High Z	High Z	High Z	power-down	(I _{SB})
L	L	L	L	H	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	(I _{CC})
L	L	L	L	H	L	H	H	H	Data out	High Z	High Z	High Z	Read byte A bits only	(I _{CC})
L	L	L	L	H	H	L	H	H	High Z	Data out	High Z	High Z	Read byte B bits only	(I _{CC})
L	L	L	L	H	H	H	L	H	High Z	High Z	Data out	High Z	Read byte C bits only	(I _{CC})
L	L	L	L	H	H	H	H	L	High Z	High Z	High Z	Data out	Read Byte D bits only	(I _{CC})
L	L	L	X ^[39]	L	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	(I _{CC})
L	L	L	X ^[39]	L	L	H	H	H	Data in	High Z	High Z	High Z	Write byte A bits only	(I _{CC})
L	L	L	X ^[39]	L	H	L	H	H	High Z	Data in	High Z	High Z	Write byte B bits only	(I _{CC})
L	L	L	X ^[39]	L	H	H	L	H	High Z	High Z	Data in	High Z	Write byte C bits only	(I _{CC})
L	L	L	X ^[39]	L	H	H	H	L	High Z	High Z	High Z	Data in	Write byte D bits only	(I _{CC})
L	L	L	H	H	X ^[39]	X ^[39]	X ^[39]	X ^[39]	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I _{CC})
L	L	L	X ^[39]	X ^[39]	H	H	H	H	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I _{CC})

ERR Output – CY7C1062GE

Output ^[40]	Mode
0	Read Operation, no single-bit error in the stored data.
1	Read Operation, single bit error detected and corrected.
High Z	Device deselected or Outputs disabled or Write Operation.

Notes

39. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

40. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

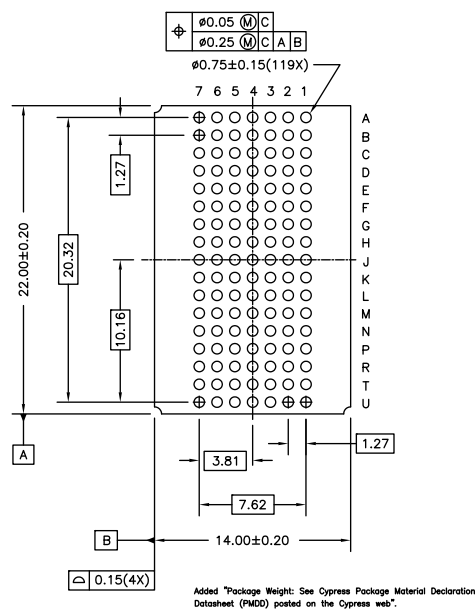
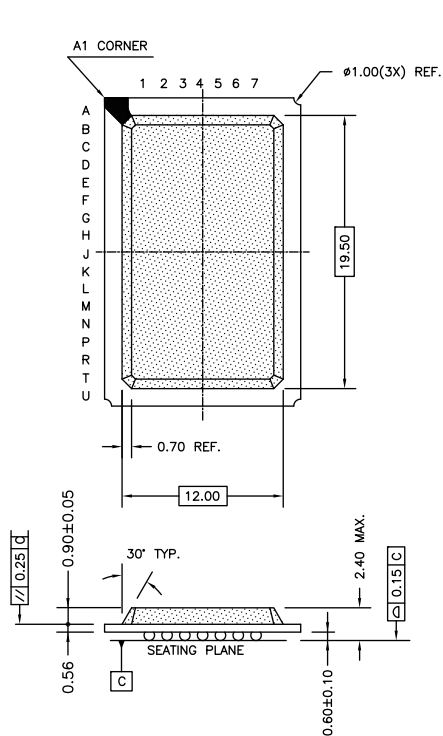
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (Pb-free)	ERR Ball	Operating Range
10	2.2 V–3.6 V	CY7C1062G30-10BGXI	51-85115	119-ball PBGA	No	Industrial
		CY7C1062G30-10BGXIT		119-ball PBGA, Tape & Reel	No	
		CY7C1062GE30-10BGXI		119-ball PBGA	Yes	
		CY7C1062GE30-10BGXIT		119-ball PBGA, Tape & Reel	Yes	

Ordering Code Definitions

CY	7	C	1	06	2	G	E	30	-	10	BG	X	I	X
X: T = Tape & Reel; Blank = Bulk Temperature Range: I = Industrial Pb-free Package Type: BG = 119-ball PBGA Speed: 10 ns Voltage Range: 30 = 2.2 V–3.6 V ERR output Single bit error indication Process Technology: 65 nm Data width: 2 = × 32-bits Density: 06 = 16-Mbit Family Code: 1 = Fast Asynchronous SRAM family Technology Code: C = CMOS Marketing Code: 7 = SRAM Company ID: CY = Cypress														

Package Diagrams

Figure 11. 119-pin PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115



NOTE:
Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85115 *D

Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
PBGA	Plastic Ball Grid Array
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1062G/CY7C1062GE, 16-Mbit (512 K words × 32 bits) Static RAM with Error-Correcting Code (ECC)
Document Number: 001-81609

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*E	4800546	NILE	07/31/2015	Changed status from Preliminary to Final.
*F	5434962	NILE	09/13/2016	Updated DC Electrical Characteristics : Enhanced V _{OH} for voltage range 3.0 V to 3.6 V from 2.2 V to 2.4 V. Updated Footnote 5. Updated part numbers in Ordering Information . Added Tape & Reel ordering codes. Updated copyright notice and Sales, Solutions, and Legal Information .
*G	5975045	AESATP12	11/30/2017	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2012-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.