

CMLDM7005**SURFACE MOUNT SILICON
DUAL N-CHANNEL
ENHANCEMENT-MODE
MOSFET**www.centrasemi.com**SOT-563 CASE****DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CMLDM7005 consists of dual N-Channel enhancement-mode silicon MOSFETs designed for high speed pulsed amplifier and driver applications. These MOSFETs offer very low $r_{DS(ON)}$ and low threshold voltage.

MARKING CODE: CC7**FEATURES:**

- ESD protection up to 2kV (Human Body Model)
- 350mW power dissipation
- Very low $r_{DS(ON)}$
- Low threshold voltage
- Logic level compatible
- Small, SOT-563 surface mount package
- Complementary dual P-Channel device: CMLDM8005

APPLICATIONS:

- Load switch/Level shifting
- Battery charging
- Boost switch
- Electro-luminescent backlighting

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage
Gate-Source Voltage
Continuous Drain Current (Steady State - Note 1)
Continuous Source Current (Body Diode)
Maximum Pulsed Drain Current
Power Dissipation (Note 1)
Power Dissipation (Note 2)
Power Dissipation (Note 2)
Operating and Storage Junction Temperature
Thermal Resistance (Note 1)

SYMBOL		UNITS
V_{DS}	20	V
V_{GS}	8.0	V
I_D	650	mA
I_S	280	mA
I_{DM}	1.3	A
P_D	350	mW
P_D	300	mW
P_D	150	mW
T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
θ_{JA}	357	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=4.5V, V_{DS}=0$			1.0	μA
I_{DSS}	$V_{DS}=16V, V_{GS}=0$			100	nA
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	20			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.5		1.1	V
V_{SD}	$V_{GS}=0, I_S=200\text{mA}$			1.1	V
$r_{DS(ON)}$	$V_{GS}=4.5V, I_D=600\text{mA}$		0.14	0.23	Ω
$r_{DS(ON)}$	$V_{GS}=2.5V, I_D=500\text{mA}$		0.2	0.275	Ω
$r_{DS(ON)}$	$V_{GS}=1.8V, I_D=350\text{mA}$			0.7	Ω
gFS	$V_{DS}=10V, I_D=400\text{mA}$	1.0			S

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm²(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm²(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm²

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CMLDM7005

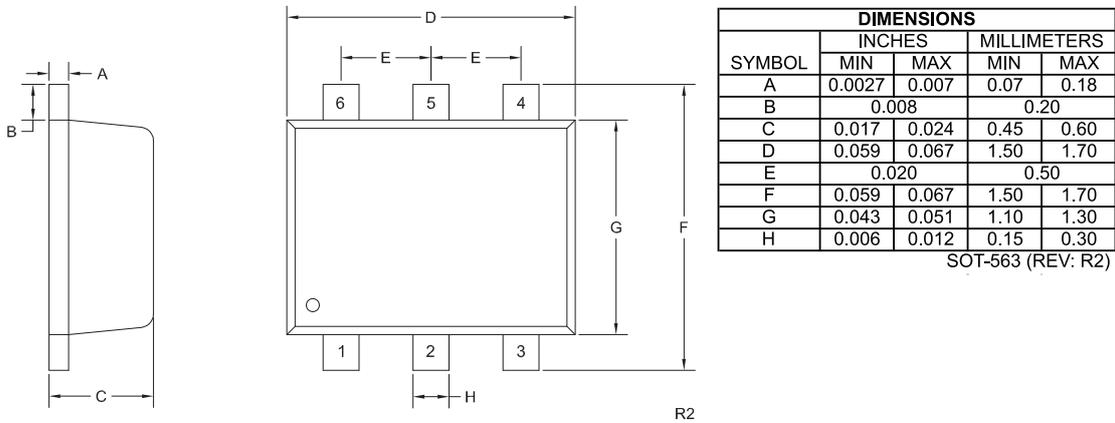
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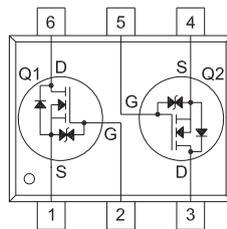
ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	TYP	UNITS
$C_{r_{ss}}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	18	pF
$C_{i_{ss}}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	100	pF
$C_{o_{ss}}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	16	pF
$Q_{g(\text{tot})}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	1.58	nC
Q_{gs}	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	0.17	nC
Q_{gd}	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	0.24	nC
t_{on}	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}, R_G=10\Omega$	10	ns
t_{off}	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}, R_G=10\Omega$	25	ns

SOT-563 CASE - MECHANICAL OUTLINE



PIN CONFIGURATION



LEAD CODE:

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

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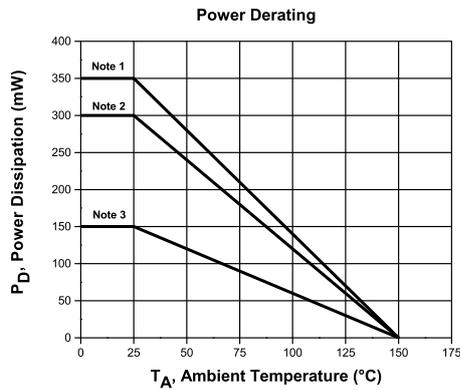
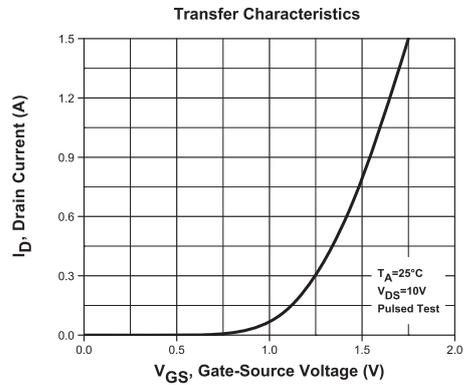
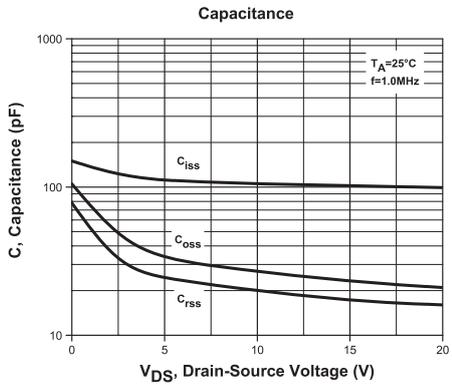
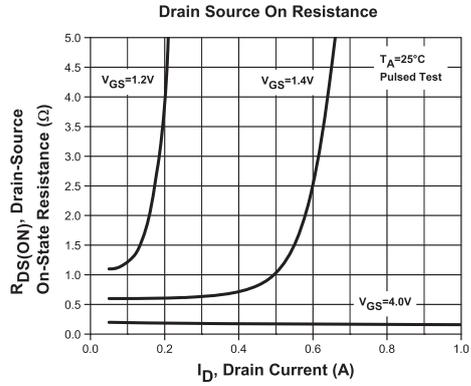
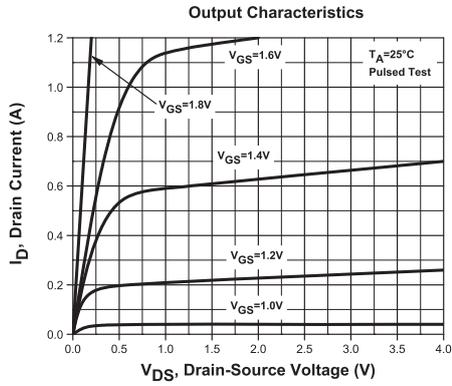
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N-CHANNEL TYPICAL ELECTRICAL CHARACTERISTICS



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