# Four-Channel Multiplexed Transimpedance Amplifier with Output Multiplexing

## FEATURES

- **220MHz –3dB Bandwidth with 2pF Input Capacitance**
- **Single-Ended Output**
- **74kΩ Transimpedance Gain**
- **4.8pA/√Hz Input Current Noise Density at 200MHz (2pF)**
- **64nA$_{RMS}$ Integrated Input Current Noise Over 200MHz (2pF)**
- **Linear Input Range 0µA to 30µA**
- Overload Current > ±400mA Peak
- Fast Overload Recovery 12ns, 1mA
- Fast Channel Switchover < 50ns
- Single 5V Supply
- 200mW Power Dissipation for 4 Channels
- 2V$_{P-P}$ Output Swing on 100Ω Load
- 4mm × 4mm, 24-Lead QFN Package
- Output MUX Combines Multiple 4-Channel Devices to Create 4, 8,12,16, 24, 32 Channel Solutions
- AEC-Q100 Qualified for Automotive Applications

## APPLICATIONS

- LIDAR Receiver
- Industrial Imaging

## DESCRIPTION

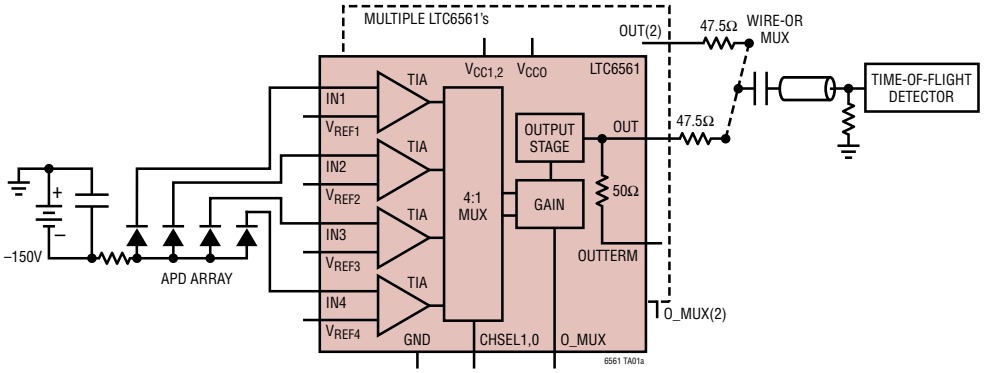
The LTC®6561 is a low-noise four-channel, transimpedance amplifier (TIA)with 220MHz bandwidth. The LTC6561 multi-channel transimpedance amplifier's low noise, high transimpedance, and low power dissipation are ideal for LIDAR receivers using Avalanche Photodiodes (APDs). The amplifier features 74kΩ transimpedance gain and 30µA linear input current range. Using an APD input circuit with a total capacitance of 2pF, the input current noise density is 4.5pA/√Hz at 200MHz. With lower capacitance, noise and bandwidth improve further. Only a 5V single supply is needed and the device consumes only 200mW. Utilizing the internal 4-to-1 MUX along with the LTC6561's output MUX; multiple 4-channel LTC6561 devices can be combined to directly interface with 8, 12, 16 and 32-channel APD arrays. The LTC6561's fast overload recovery and fast channel switchover make it well suited for LIDAR receivers with multiple APDs. Its single-ended output can swing 2V$_{P-P}$ on a 100Ω load. While its low impedance op amp-style output can drive back-terminated 50Ω cables.

The LTC6561 is packaged in a compact 4mm × 4mm 24-pin leadless QFN package with an exposed pad for thermal management and low inductance.

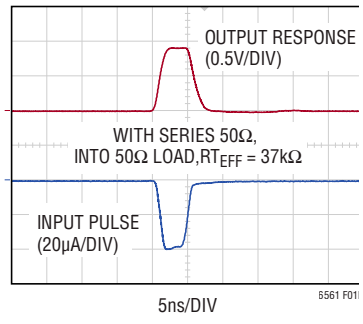


## TYPICAL APPLICATION

**Typical Application with DC-Coupled Inputs Driving a Time-to-Digital Converter with Back-Terminated Cable**




**Pulse Response at the Edge of the Overload Region (40µA)**



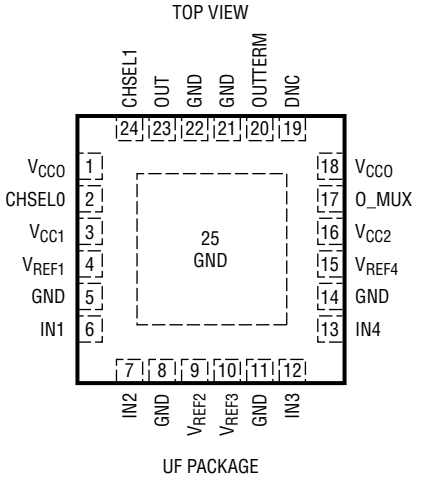

Rev. C

## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Total Supply Voltage ($V_{CC1}$, $V_{CC2}$, $V_{CCO}$ to GND)..... 5.5V
Voltage (CHSEL0, CHSEL1, O_MUX)..... –0.3V to 5.5V
Amplifier Reference Current ($V_{REF1}$, $V_{REF2}$, $V_{REF3}$, $V_{REF4}$) ..... ±10mA
Amplifier Reference Voltage ($V_{REF1}$, $V_{REF2}$, $V_{REF3}$, $V_{REF4}$) ..... –0.3V to 3.5V
Amplifier Input Current (IN1, IN2, IN3, IN4) .....±400mA RMS ±2A Transient (10ns)
Amplifier Output Current (OUT, OUTTERM) ..... +80mA
Operating Temperature Range
LTC6561I (Note 2).....–40°C to 85°C
LTC6561H (Note 3) .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
Junction Temperature ..... 150°C

## PIN CONFIGURATION




UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 47°C/W, $\theta_{JC}$ = 4.5°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| TUBE | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC6561IUF#PBF | LTC6561IUF#TRPBF | 6561 | 24-LEAD (4mm × 4mm) PLASTIC QFN | –40°C to 85°C |
| LTC6561HUF#PBF | LTC6561HUF#TRPBF | 6561 | 24-LEAD (4mm × 4mm) PLASTIC QFN | –40°C to 125°C |
| **AUTOMOTIVE PRODUCTS**** | | | | |
| LTC6561HUF#WPBF | LTC6561HUF#WTRPBF | 6561 | 24-LEAD (4mm × 4mm) PLASTIC QFN | –40°C to 125°C |

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

## AC ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C, $V_{CC1,2}$ = $V_{CCO}$ = 5V, O_MUX = 0V, GND = 0V, $Z_{LOAD}$ = 100Ω. Output is AC-coupled. Output taken from OUT pin.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| BW | –3dB Bandwidth | 200mV$_{P-P,OUT}$ and $C_{IN,TOT}$ = 2pF | | | 220 | | MHz |
| $R_T$ | Small Signal Transimpedance | $I_{IN}$ < 2µA$_{P-P}$ | <br>● | 63<br>47.7 | 74 | 85<br>101 | kΩ |
| $R_{IN}$ | Input Impedance | f = 100kHz | | | 236 | | Ω |
| $R_{OUT}$ | Output Impedance | f = 100kHz | | | 3 | | Ω |

## AC ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C, $V_{CC1,2}$ = $V_{CC0}$ = 5V, O_MUX = 0V, GND = 0V, $Z_{LOAD}$ = 100Ω. Output is AC-coupled. Output taken from OUT pin.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_n$ | Input Current Noise Density | f = 100MHz, $C_{IN,TOT}$ = 2pF | | | 4.3 | | pA/√Hz |
| | | f = 200MHz, $C_{IN,TOT}$ = 2pF | | | 4.8 | | pA/√Hz |
| | Integrated Input Current Noise | f = 0.1MHz to 100MHz, $C_{IN,TOT}$ = 2pF | | | 43 | | $nA_{RMS}$ |
| | | f = 0.1MHz to 200MHz, $C_{IN,TOT}$ = 2pF | | | 64 | | $nA_{RMS}$ |
| | Adjacent Channel to Channel Isolation | f = 100MHz | | | –45 | | dB |
| | Non Adjacent Channel Isolation | f = 100MHz | | | –65 | | dB |
| $t_{RECOVER}$ | Overload Recovery Time | Input Pulse = 1mA | | | 12 | | ns |
| $t_{SWITCH}$ | Channel Switchover Time | DC Coupled Input | | | 50 | | ns |
| $t_{OMUX\_SWITCH}$ | Output MUX Switchover Time | DC Coupled Input | | | 50 | | ns |

## DC ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C, $V_{CC1,2}$ = $V_{CC0}$ = 5V, O_MUX = 0V, GND = 0V, $Z_{LOAD}$ = 100Ω. Output is AC-coupled. Output taken from OUT pin.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **IN1,2,3,4 Pins and $V_{REF1,2,3,4}$ Pins** | | | | | | | |
| $V_{IN}$ | Input Bias Voltage | Active Channel | | 1.43 | 1.55 | 1.64 | V |
| | | | ● | 1.25 | | 1.76 | V |
| | | Inactive Channel | | 0.78 | 0.93 | 1.38 | V |
| | | | ● | 0.70 | | 1.53 | V |
| $V_{REF}$ | Input Reference Voltage | Active Channel | | 1.43 | 1.55 | 1.63 | V |
| | | Inactive Channel | | 1.34 | 1.50 | 1.67 | V |
| Offset | $V_{IN}$ – $V_{REF}$ | Active Channel | | –12 | | 12 | mV |
| | | Inactive Channel | | –741 | | –116 | mV |
| **OUT Pin** | | | | | | | |
| $V_{OUT}$ | Output Default Voltage | O_MUX = 0V | | 0.83 | 1.10 | 1.47 | V |
| | | | ● | 0.79 | | 1.67 | V |
| | | O_MUX = 3.3V, Standalone Device | | 0.32 | 0.60 | 0.88 | V |
| | | | ● | 0.28 | | 0.92 | V |
| OVR | Output Voltage Range | $I_{IN}$ Current Range = 0 to –50µA | | 1.22 | 1.90 | 2.58 | $V_{P-P}$ |
| | | | ● | 0.98 | | 2.80 | $V_{P-P}$ |
| OUTTERM | Internal Series Resistor for Optional Output | | | 44 | 56 | 70.8 | Ω |
| **CHSEL0, CHSEL1, O_MUX Pins with Internal Pull-Down Resistors** | | | | | | | |
| $V_{IL}$ | | | ● | | | 0.7 | V |
| $V_{IH}$ | | | ● | 1.5 | | | V |
| $I_{IL}$ | Pin Voltage = 0.7V | | | 16.9 | 20.7 | 26.0 | µA |
| | | | ● | 15.4 | | 28.0 | µA |
| $I_{IH}$ | Pin Voltage = 1.5V | | | 37 | 47 | 57 | µA |
| | | | ● | 34 | | 62 | µA |
| $C_{IN}$ | Input Capacitance | | | | 1.5 | | pF |
| $R_{IN}$ | Input Resistance | | | 22 | 29 | 35 | kΩ |
| | | | ● | 21 | | 37 | kΩ |

## DC ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C, $V_{CC1,2}$ = $V_{CCO}$ = 5V, O_MUX = 0V, GND = 0V, $Z_{LOAD}$ = 100Ω. Output is AC-coupled. Output taken from OUT pin.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | | |
| $V_S$ | Operating Supply Range | | | 4.75 | 5 | 5.25 | V |
| $I_{CC1,2}$ | Input Supply Current | $V_{CC1}$ and $V_{CC2}$ Are Internally Tied Together | <br>● | 29.0<br>26.8 | 36.3 | 44.0<br>45.8 | mA<br>mA |
| $I_{CCO}$ | Output Supply Current | Both $V_{CCO}$ Pins Are Internally Tied Together | <br>● | 1.8<br>1.7 | 2.3 | 2.8<br>2.9 | mA<br>mA |
| $I_S$ | Total Supply Current ($I_{S(VCC1,2)}$ + $I_{S(VCCO)}$) | | <br>● | 30.8<br>28.5 | 38.6 | 46.8<br>48.7 | mA<br>mA |
| PSRR($V_{CC1,2}$) | Input Power Supply Rejection Ratio | $V_{CC1,2}$ = 4.75V to 5.25V, $V_{CCO}$ = 5V | <br>● | 21<br>15 | 25 | | dB<br>dB |
| PSRR($V_{CCO}$) | Output Power Supply Rejection Ratio | $V_{CCO}$ = 4.75V to 5.25V, $V_{CC1,2}$ = 5V | <br>● | 34<br>33 | 40 | | dB<br>dB |

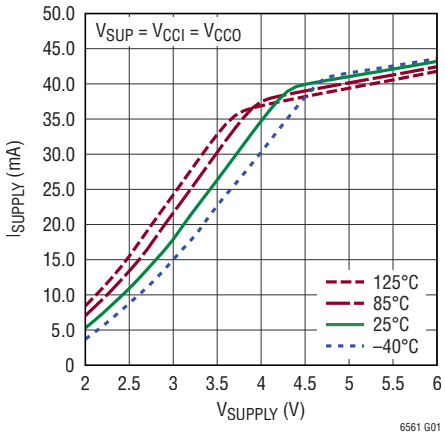
**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC6561I is guaranteed to meet specified performance from –40°C to 85°C.

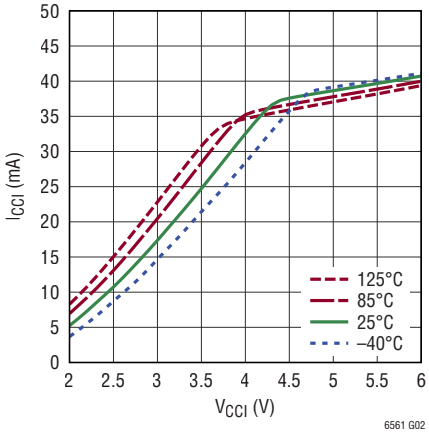
**Note 3:** The LTC6561H is guaranteed to meet specified performance from –40°C to 125°C.

## TYPICAL PERFORMANCE CHARACTERISTICS

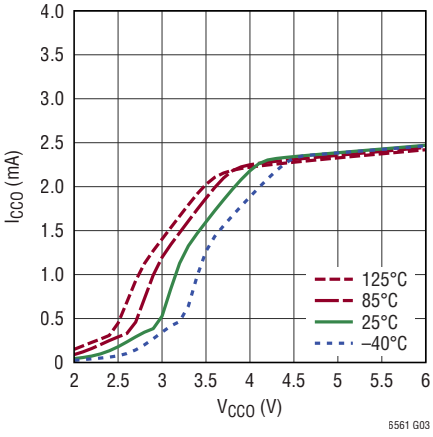
**$I_{SUPPLY}$ vs $V_{SUPPLY}$ Over Temperature**




**$I_{CCI}$ vs $V_{CCI}$ Over Temperature**

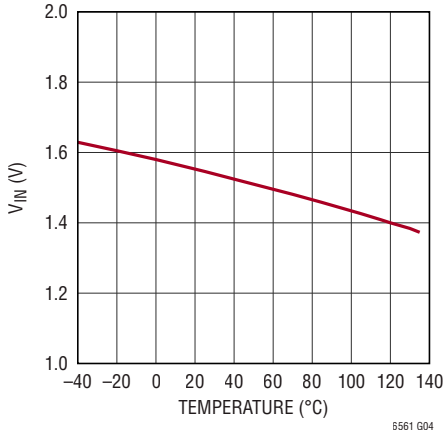



**$I_{CCO}$ vs $V_{CCO}$ Over Temperature**

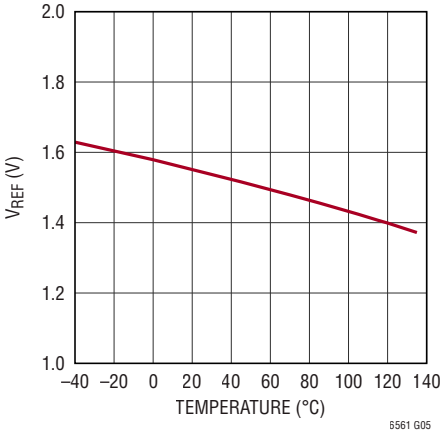


# TYPICAL PERFORMANCE CHARACTERISTICS

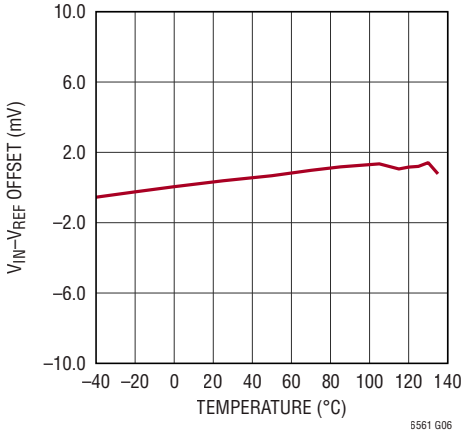
**$V_{IN}$ vs Temperature**



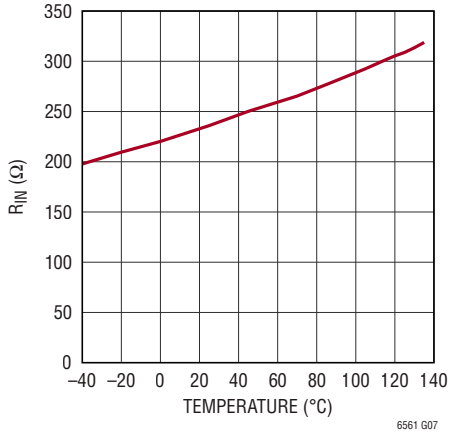

**$V_{REF}$ vs Temperature**



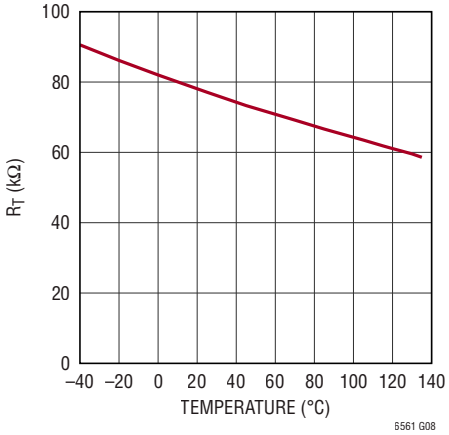

**$V_{IN}$–$V_{REF}$ Offset vs Temperature**



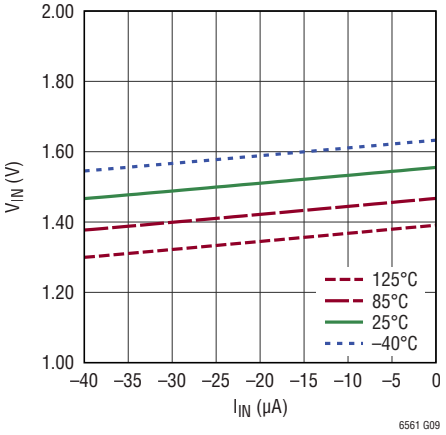

**$R_{IN}$ vs Temperature**



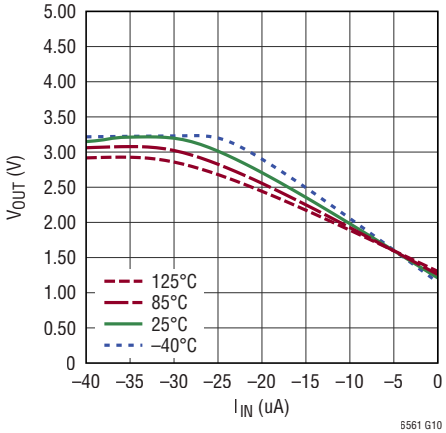

**$R_T$ Transimpedance vs Temperature**



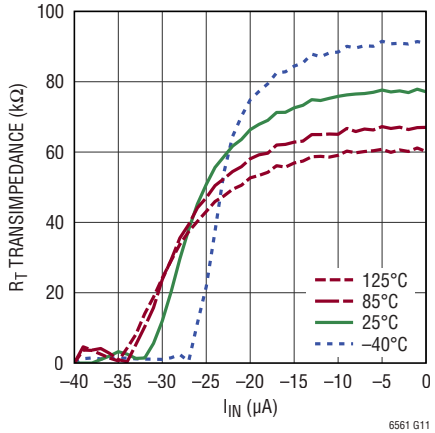

**$V_{IN}$ vs $I_{IN}$ Over Temperature**



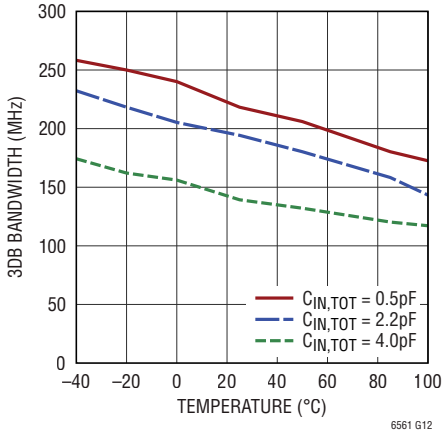

**$V_{OUT}$ vs $I_{IN}$ Over Temperature**




**$R_T$ Transimpedance vs $I_{IN}$ Over Temperature**

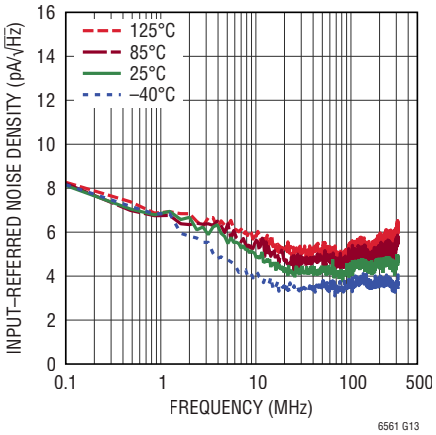



**3dB Bandwidth vs Temperature Over $C_{IN,TOT}$**

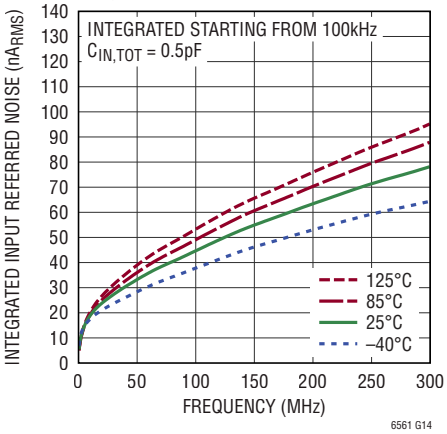


# TYPICAL PERFORMANCE CHARACTERISTICS

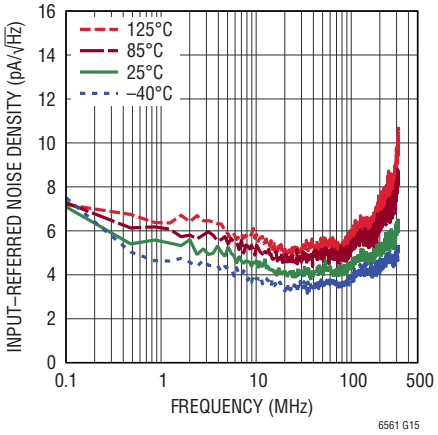
### Input-Referred Noise Density with $C_{IN,TOT}$ = 0.5pF



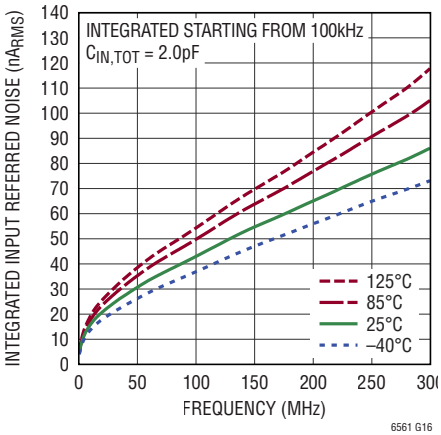

### Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 0.5pF



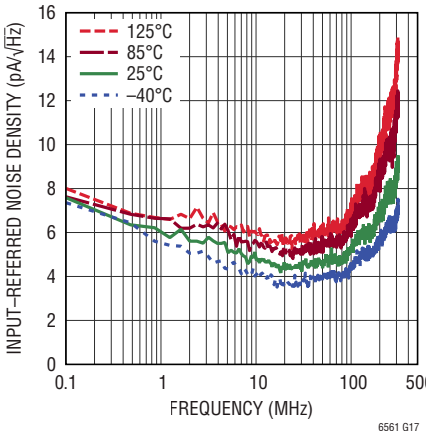

### Input-Referred Noise Density with $C_{IN,TOT}$ = 2.0pF



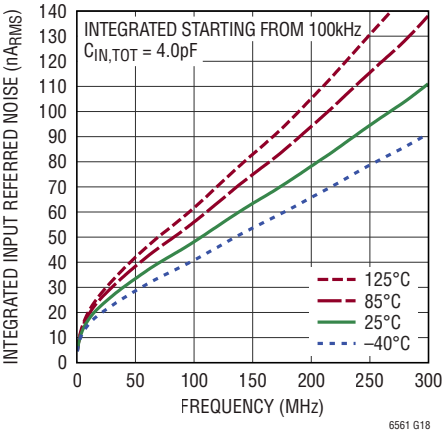

### Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 2.0pF



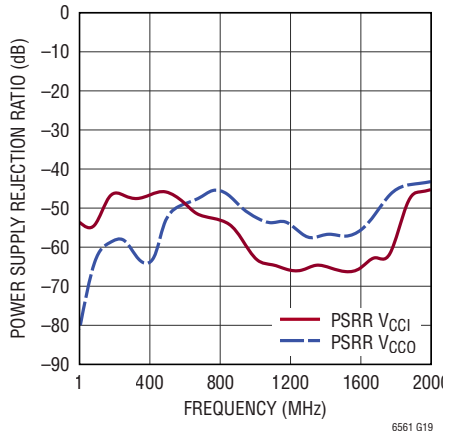

### Input-Referred Noise Density with $C_{IN,TOT}$ = 4.0pF



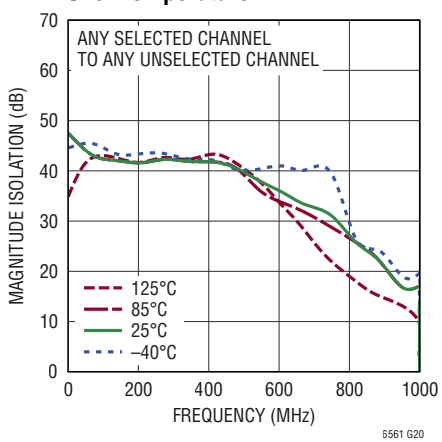

### Integrated Input-Referred Noise vs Bandwidth Over Temperature $C_{IN,TOT}$ = 4.0pF



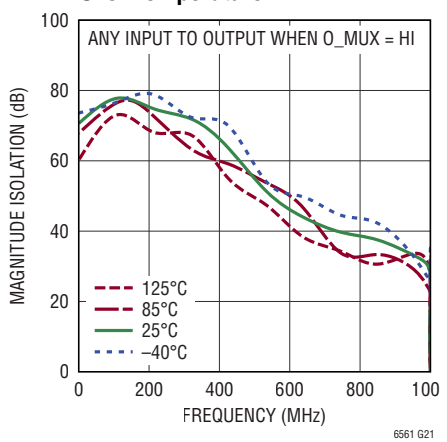

### PSRR Out to $V_{CCI}$, $V_{CCO}$




### Ch to Ch Isolation vs Frequency Over Temperature

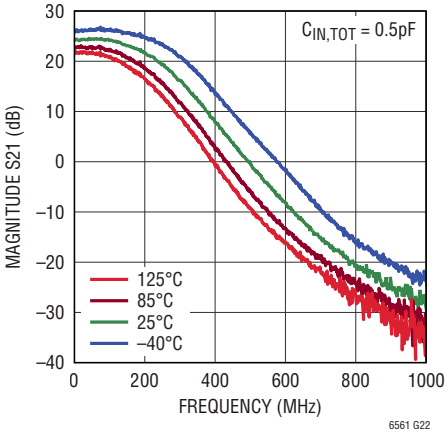



### O_MUX Isolation vs Frequency Over Temperature

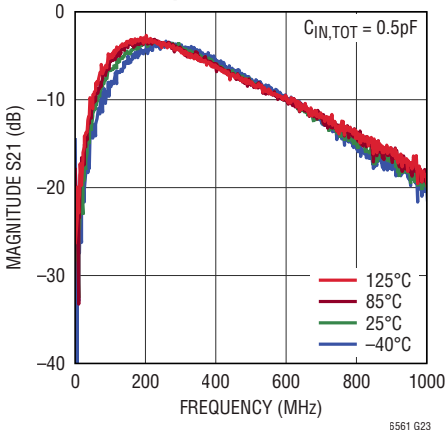


# TYPICAL PERFORMANCE CHARACTERISTICS

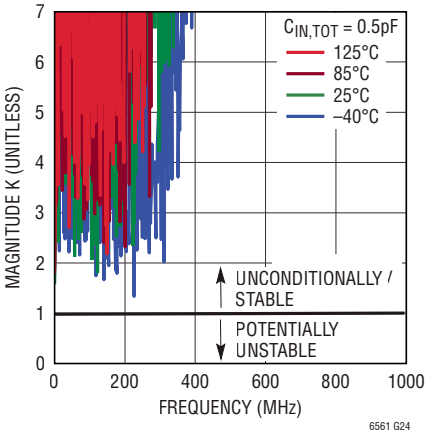
**S21(Gain) vs Frequency Over Temperature**



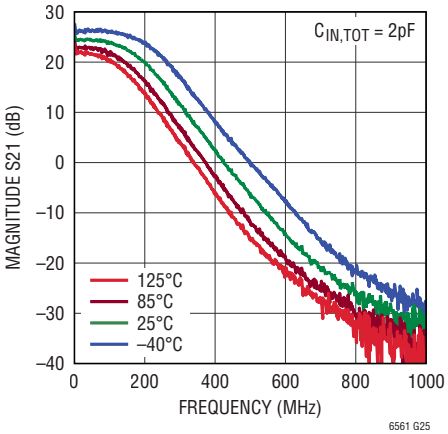

**S22 vs Frequency Over Temperature**



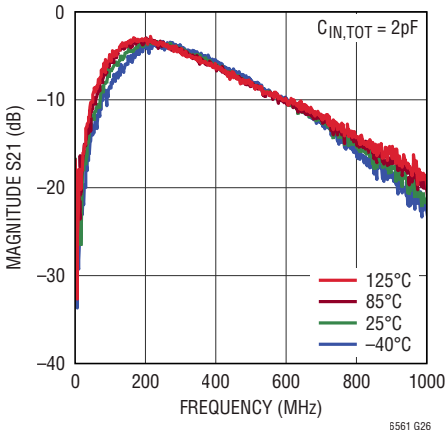

**Stability Factor K vs Frequency Over Temperature**



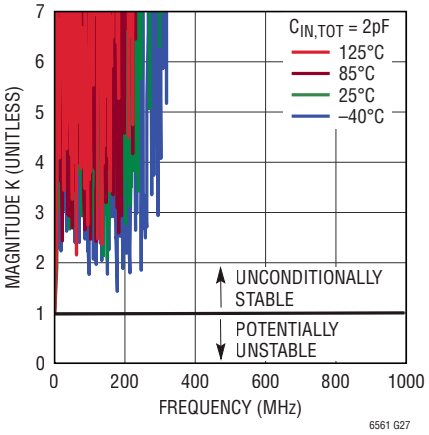

**S21(Gain) vs Frequency Over Temperature**



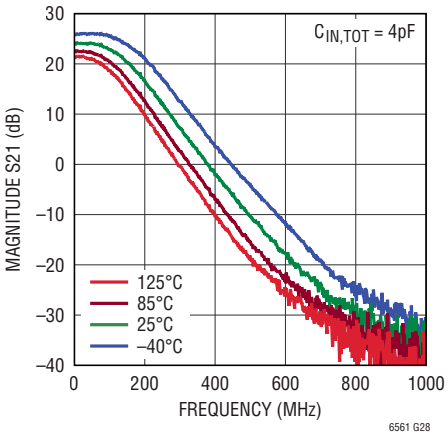

**S22 vs Frequency Over Temperature**



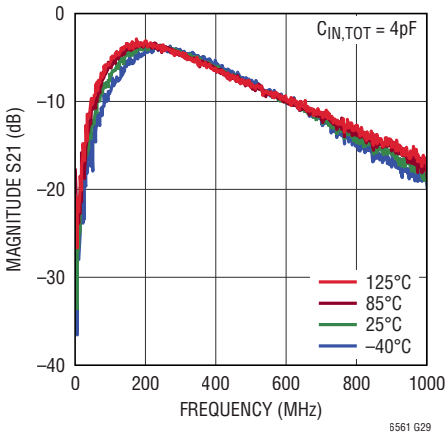

**Stability Factor K vs Frequency Over Temperature**



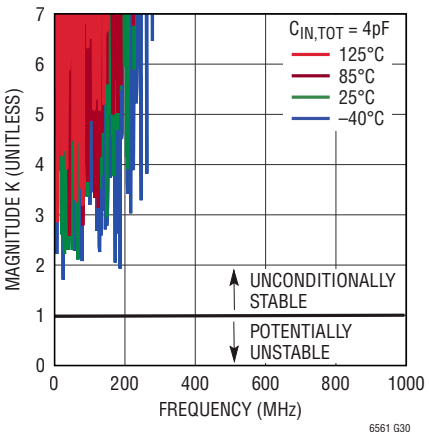

**S21(Gain) vs Frequency Over Temperature**



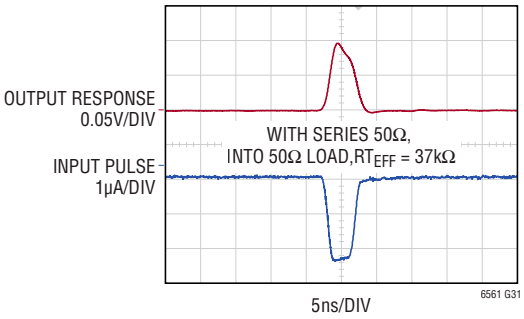

**S22 vs Frequency Over Temperature**



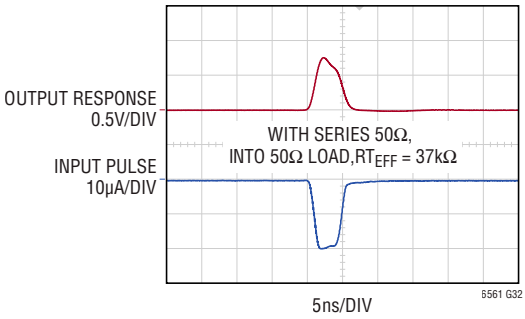

**Stability Factor K vs Frequency Over Temperature**



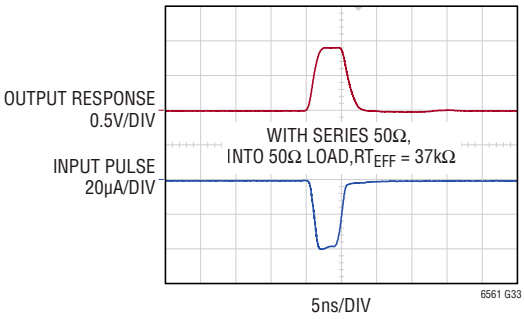
**Pulse Response**
**Linear Range (2.5µA)**



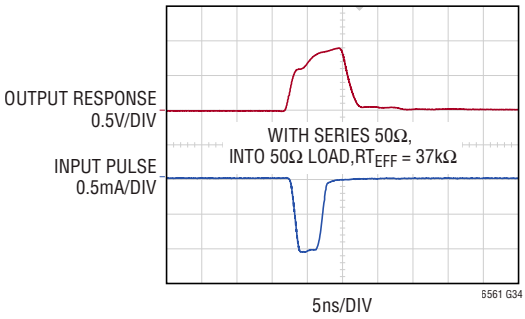

**Pulse Response**
**Linear Range (20µA)**



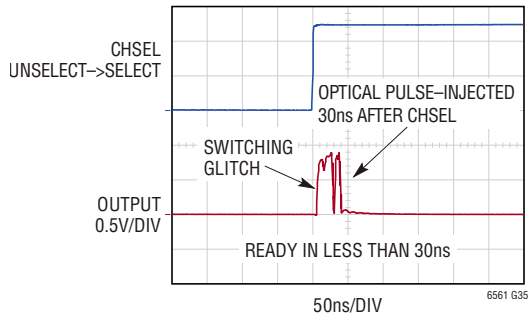

**Pulse Response**
**Overload Region (40µA)**



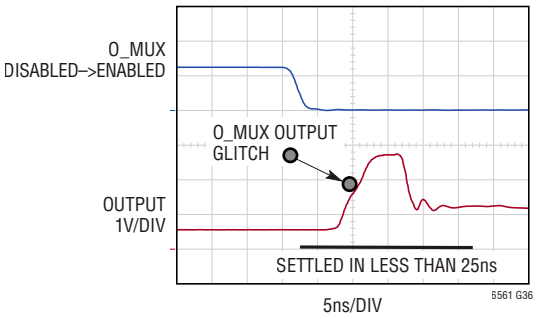

**Pulse Response**
**Overload Region (1mA)**



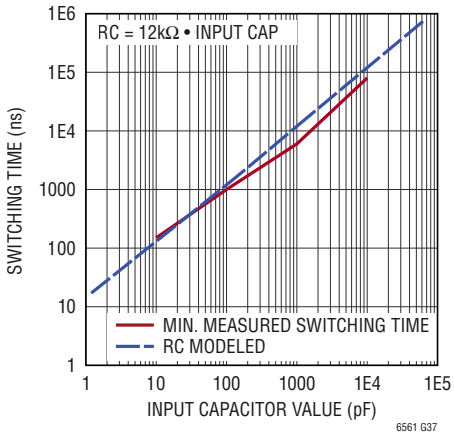

**Channel Select Switching Time**
**DC Coupled Input**



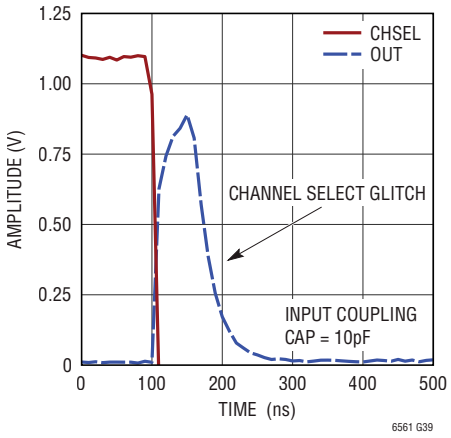

**O_MUX Switching Time**
**DC Coupled Input**



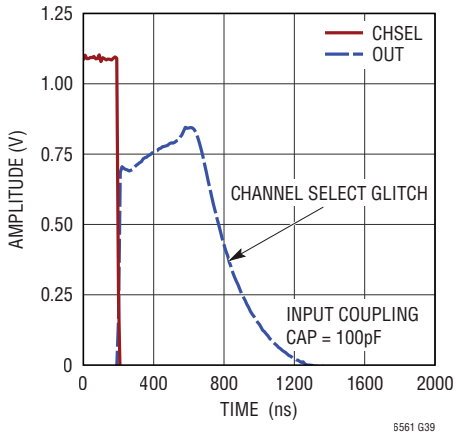
### O_MUX and Channel Switching Time for AC Coupled Input



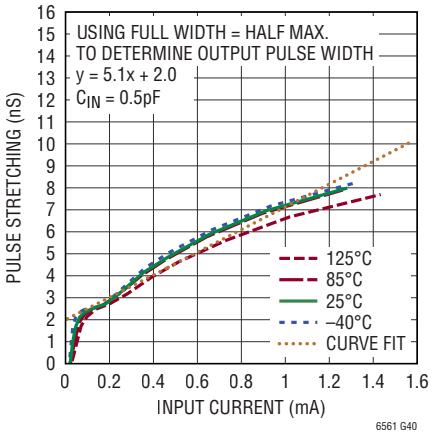

### Channel Switching Glitch AC Coupled Input, 10pF



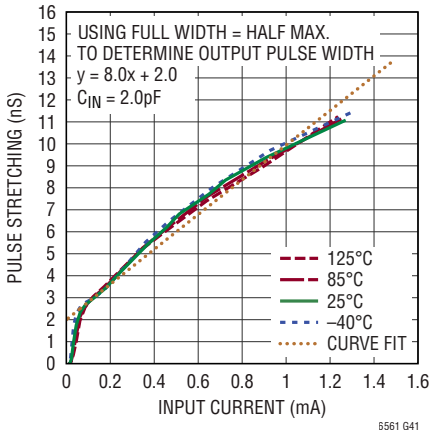

### Channel Switching Glitch AC Coupled Input, 100pF



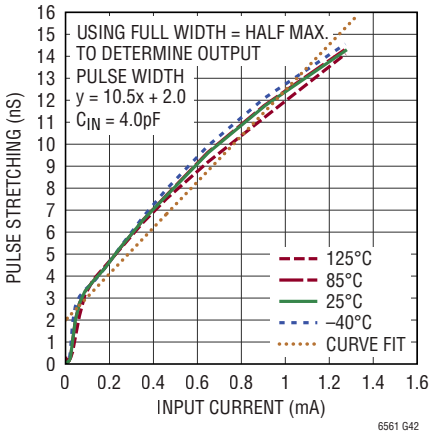

### Pulse Stretching $C_{IN}$ = 0.5pF, Using FWHM



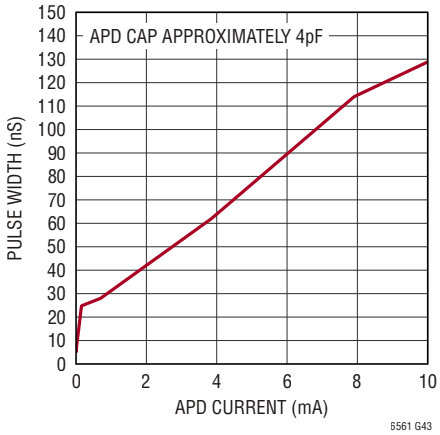

### Pulse Stretching $C_{IN}$ = 2.0pF, Using FWHM




### Pulse Stretching $C_{IN}$ = 4.0pF, Using FWHM




### Pulse Width vs ADP Current Optical Measurement



## PIN FUNCTIONS

**$V_{CCO}$ (Pins 1, 18):** Positive Power Supply for the output stage. Typically 5V. $V_{CCO}$ can be tied to $V_{CC1}$ or $V_{CC2}$ for single supply operation. Bypass capacitors of 1000pF and 0.1µF should be placed as close as possible between $V_{CCO}$ and ground. Both $V_{CCO}$ pins are internally tied together.

**CHSEL0 (Pin 2):** LSB for Channel Selection. CMOS input. The CHSEL0 pin has a 29kΩ internal pull-down resistor. Default value is 0V.

**$V_{CC1}$, $V_{CC2}$ (Pins 3, 16):** Positive Power Supply. Typically 5V. Bypass capacitors of 1000pF and 0.1µF should be placed as close as possible between $V_{CC1,2}$ and ground. $V_{CC1}$ (Pin 3) and $V_{CC2}$ (Pin 16) are internally tied together.

**$V_{REF1}$, $V_{REF2}$, $V_{REF3}$, $V_{REF4}$ (Pins 4, 9, 10, 15):** Reference Voltage Pins for Transimpedance Amplifier for Channels 1, 2, 3, and 4 Respectively. This pin sets the input voltage for each transimpedance amplifier. The $V_{REF}$ pin has a Thevenin equivalent resistance of approximately 1.4k and can be overdriven by an external voltage. If no voltage is applied to $V_{REF}$, it will float to a default voltage of approximately 1.55V on a 5V supply. Each $V_{REF}$ pin should be bypassed with a high quality ceramic bypass capacitor of at least 0.1µF. The bypass cap should be located close to its $V_{REF}$ pin.

**GND(Pins 5,8,11,14,21,22,Exposed Pad Pin 25):** Negative Power Supply. Normally tied to ground. All GND pins and the exposed pad must be tied to the same voltage. The exposed pad (pin 25) should have multiple via holes to underlying ground plane for low inductance and good heat transfer.

**IN1, IN2, IN3, IN4 (Pin 6, 7, 12, 13):** Input Pin for Transimpedance Amplifier for Channels 1, 2, 3, and 4 respectively. This pin is internally biased to 1.55V. See the Applications section for specific recommendations.

**O_MUX(Pin 17):** Output MUX is a digital input controlling the output multiplexing function. The pin is functional when multiple LTC6561s are combined at the output. When O_MUX is low, the output is enabled. When O_MUX is high, all 4 inputs are decoupled from the output. Its default value is 0V. This MUX pin is ineffective effect unless a 2nd LTC6561 is DC-coupled at the output. See Applications section on how to use O_MUX to expand the channel count with multiple LTC6561s. The O_MUX pin has a 29kΩ internal pull-down resistor.

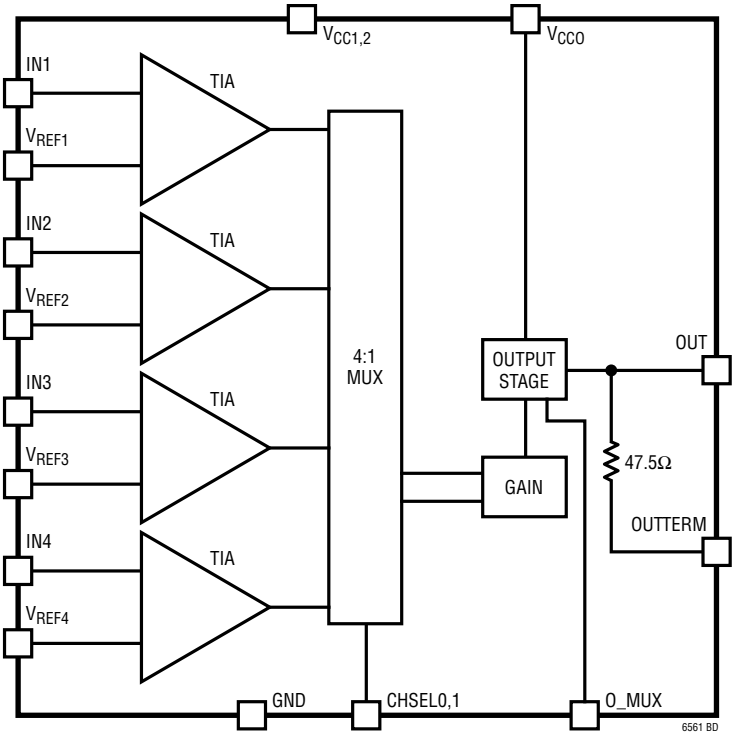
**DNC(Pin 19):** No Connection. Do not connect.

**OUTTERM (Pin 20):** TIA Output with an Internal Series 50Ω Resistor.

**OUT (Pin 23):** TIA Output without an internal series 50Ω

**CHSEL1 (Pins 24):** MSB for Channel Selection. CMOS input. The CHSEL1 pin has a 29kΩ internal pull-down resistor. Default value is 0V.

## BLOCK DIAGRAM



## OPERATION

The LTC6561 is a four channel transimpedance amplifier (TIA) with an integrated 4-to-1 multiplexer. Each of the transimpedance amplifiers converts an input current to an output voltage. The integrated multiplexer simplifies the system design while saving space and power. In addition, the Output Multiplexer capability (O_MUX) allows multiple 4-channel LTC6561 devices to be combined. 8, 12, 16 or 32 input channels are easily multiplexed into a single output.

In typical LIDAR applications, the LTC6561 amplifies the output current of an APD. APD are biased near breakdown to achieve high current gain Under intense optical illumination they can conduct large currents, often in excess of 1A. The LTC6561 survives and quickly recovers from large overload currents of this magnitude. During recover, any TIA is blinded from subsequent pulses. The LTC6561 recovers from 1mA saturation events in less than 12ns without phase reversal, minimizing this form of data loss. As the level of input current exceeds the linear range, the output pulse width will widen. However, the recovery time remains in the 10's of ns. See Figure 7b and Figure 8a plots of pulse stretching versus input current.

Internally the LTC6561 consists of multiple stages. The first stage is a transimpedance amplifier. A second voltage gain stage leads to a final output buffer that can drive a $2V_{P-P}$ swing on a 100Ω load.

To increase the LIDAR's spatial resolution many APDs are deployed, often in an array. To achieve maximum bandwidth each APD pixel must have a dedicated TIA as increasing $C_{IN}$ will reduce bandwidth. The LTC6561 multiplexing capability allows compact multichannel designs without external multiplexers. The use of multiple LTC6561's works well with an APD array to minimize trace capacitance and solution size.

**Channel Selection**

| CHSEL1 | CHSEL0 | O_MUX | ACTIVE CHANNEL |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 2 |
| 1 | 0 | 0 | 3 |
| 1 | 1 | 0 | 4 |
| X | X | 1 | High Z |

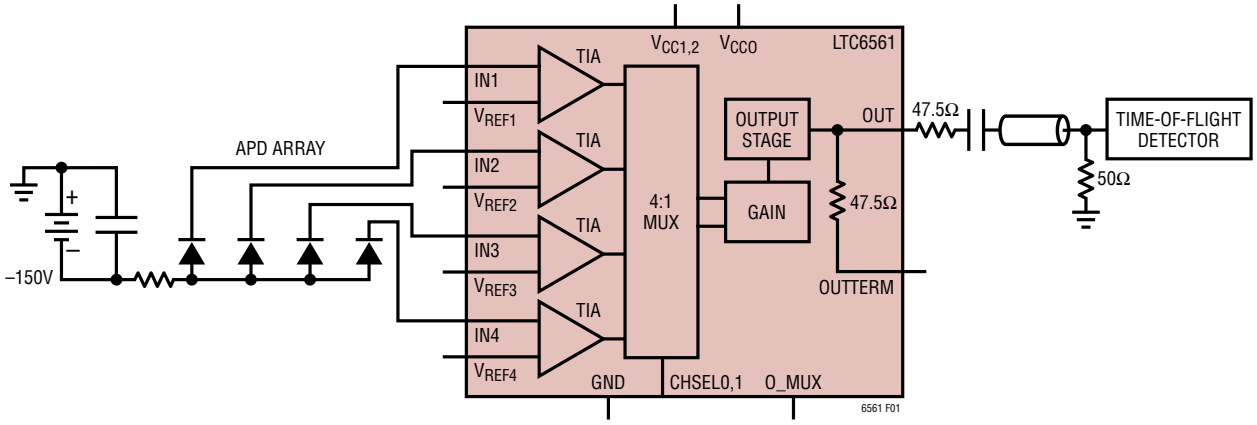



**Figure 1. Typical Application with DC-Coupled Inputs Driving a TDC with Back-Terminated Cable**

## APPLICATIONS INFORMATION

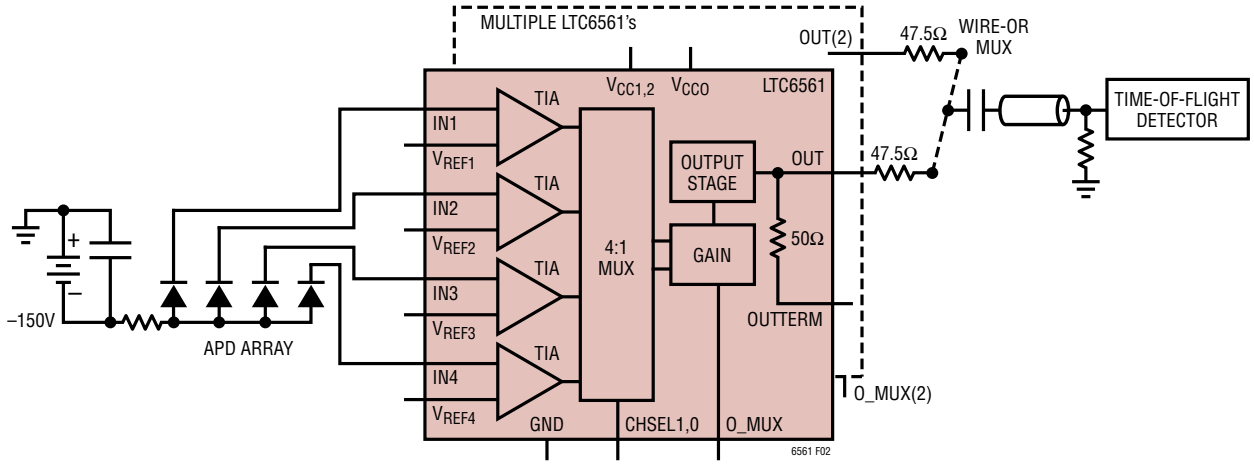



**Figure 2. Typical Application with Multiplexed Output**

### PCB Layout

The LTC6561 has separate supply pins for input ($V_{CC1,2}$) and output ($V_{CCO}$). $V_{CC1}$ (Pin 3) and $V_{CC2}$ (Pin 16) are internally tied together. $V_{CCO}$ pins (Pins 1 and 18) are internally tied together as well. Duplicate supply pins are provided to ease layout. One set of supply pins should be bypassed with 1000pF and 0.1µF capacitors to ground. For best operation, the output and input supplies should be set to the same voltage.

At each $V_{REF}$ pin the LTC6561 has small internal bypass capacitors connected between pin and ground to ensure low input noise. For the lowest possible input noise, the $V_{REF}$ pin at each TIA should be bypassed with a high quality 1000pF ceramic capacitor to ground. This bypass cap should be located physically close to each $V_{REF}$ pin and far from input pins to avoid unintentional coupling to the output.

### Output Considerations

The LTC6561's output stage is a low impedance driver. When using the OUT pin, a series 47.5Ω resistor must be added to match to 50Ω transmission lines and equipment. If the OUTTERM pin is utilized, the 47.5Ω resistor is internal and no external component is needed. Only one of the outputs should be utilized at a time. At the single ended output, the resting voltage is approximately 1.0V. Loaded with 100Ω or higher load, the output can swing to 3V. This is equivalent to a $2V_{P-P}$ swing. If loaded with 50Ω, only a $1V_{P-P}$ swing is possible since half of the voltage is dropped across the series output resistor. The output must be terminated with a low impedance load <400Ω. If the output is measured directly into a high impedance oscilloscope, the output falling edge will be distorted as the LTC6561 has limited ability to sink current. When monitoring the output, be sure to set the oscilloscope's input termination to 50Ω.

### Input Considerations AC- or DC-Coupling

Input coupling the APD to the TIA is a critical design aspect with many trade-offs to consider. The DC coupled input is the simplest, requiring minimal components to directly couple the APD to the TIA. In the DC case switching times are fast <50nS and saturation recovery times are minimized. However, DC coupling allows APD dark current, and ambient light components to leak through. These DC components can diminish the TIA's dynamic range. DC current cancellation can be used to restore the TIA's dynamic range by injecting current at the TIA input to offset the APD's DC current component. Care must be taken at the TIA's input as current injection can also inject noise.

The AC coupled input case will block all DC inputs, preserving the TIA's full dynamic range. See Figure 3.

## APPLICATIONS INFORMATION

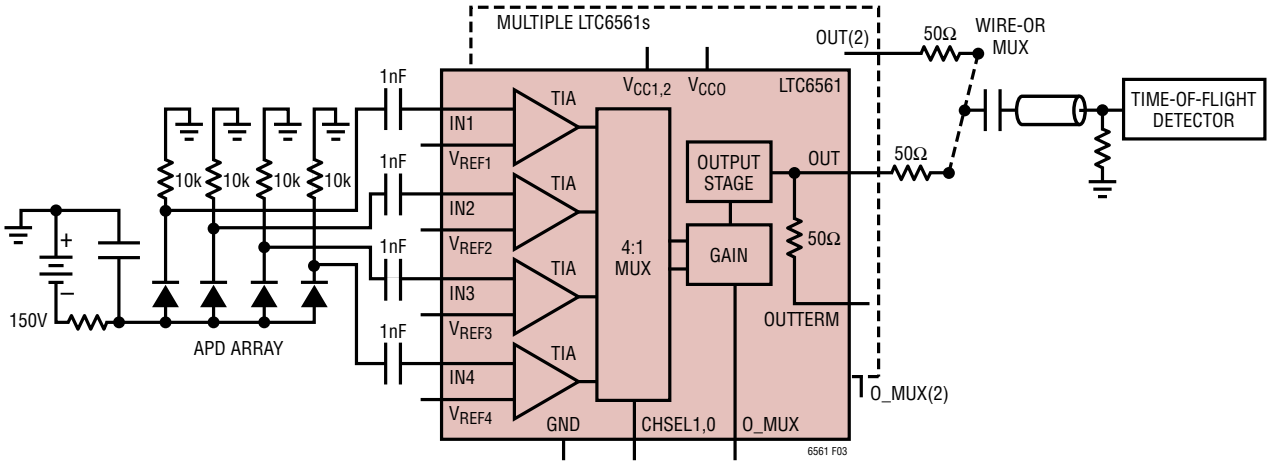



**Figure 3. Typical Application with Multiplexed Output**

However, switching times will be affected depending on the choice of AC coupling capacitor. When a channel is switched from inactive to active using either the CHSEL or O_MUX control, a glitch will appear at the output. (See Figure 5 and Figure 6) The TIA will not be ready for a desired input pulse until the glitch has settled. The glitch settling time is dependent upon the AC coupling capacitor value. The value of the AC coupling cap must be carefully considered. A plot of switching times vs. coupling capacitor is shown in Figure 4.

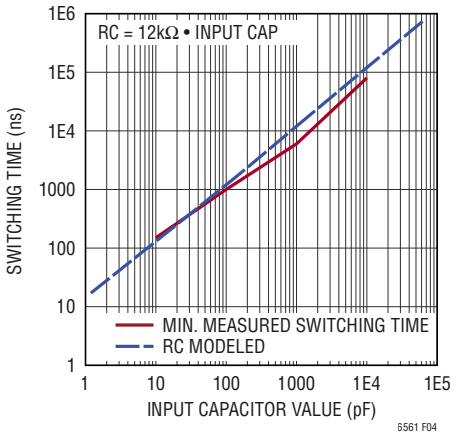



**Figure 4. AC Switching Times**

To maximize dynamic range, the LTC6561's input is limited to negative current pulses (current flowing out of the LTC6561). When using a negatively biased APD, the TIA input can be AC or DC coupled to the APD cathode.

When using a positively biased APD, the input must be AC coupled off of the APD's anode.

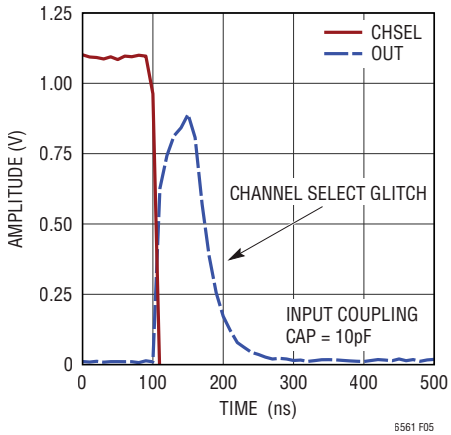



**Figure 5. Switching Glitch 10pF**

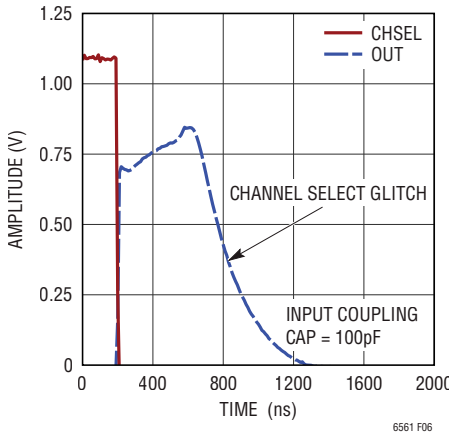



**Figure 6. Switching Glitch 100pF**

Rev. C

## APPLICATIONS INFORMATION

Coupling the APD to the TIA is critical, direct DC coupling or AC coupling, using a small AC coupling capacitor from 10pF to 100pF is recommended.

### Channel Selection

There are four TIA inputs to the LTC6561. The active channel is selected using the two channel selection bits CHSEL0 and CHSEL1. When a channel is selected, its DC input voltage is approximately 1.5V; when deselected its input voltage drops to 0.9V. A reselected channel will not be active until its AC-coupling cap is recharged to 1.5V, leading to slow switching times. With a large AC-coupling cap, switching time can stretch into the µS range. When DC- coupled, the LTC6561 will switch channels in less than 50nS. Inactive channels have more than 45dB of isolation to the active channel to prevent cross-talk. It is critical to route adjacent channel input lines with ground isolation between them to minimize channel to channel coupling.

### Output MUXing

The Output MUX (O_MUX) requires at least one additional LTC6561 devices to operate in a master/slave relationship. To MUX multiple LTC6561's they need to share a DC connection at their outputs. One LTC6561 output must be selected at all times by asserting its O_MUX pin low. To disable the rest of the outputs, drive the other O_MUX pins high. The chosen LTC6561 effectively commands the others. It is recommended to DC couple the outputs after the series 40-50Ω resistor as this will limit reflection from unselected outputs. At least one LTC6561 output must be selected at all times.

In its default mode O_MUX is low, so the LTC6561 output is enabled. Obviously, if there is only one LTC6561, then setting the O_MUX pin high will not MUX anything, however the output will be isolated from all the inputs.

### Input Capacitance

As with most TIAs, bandwidth and rise time of the output pulse are a strong function of the input capacitance. To receive narrow pulses, a low capacitance APD sensor is recommended. As well, trace capacitance and parasitic pad capacitance should be minimized at the input. All LTC6561 plots reference $C_{IN,TOT}$ which is the total input capacitance including APD sensor, trace routing and parasitics. The LTC6561's MUX capability allows short input coupling to individual APDs and a more compact solution size for APD arrays.

Internal protection circuitry at each TIA input can protect the LTC6561 even under strong overdrive conditions. Most application circuits will not need external protection diodes which add to the total input capacitance and slow the rise time. Output rise time can be estimated from the amplifier bandwidth using the following relationship:

$$RISETIME = \frac{0.35}{BW}$$

### APD Biasing

Proper APD biasing is key to producing a high fidelity output and protecting both the APD and TIA. As suggested earlier a negatively biased APD provides the lowest input capacitance and allows the APD to be DC coupled to the TIA. To keep the optical gain stable the APD bias should be temperature compensated. Quenching resistors in series are required to limit the maximum current, thereby protecting the APD and TIA from damage. An example of a typical APD bias network is shown in Figure 9. Starting at the Negative bias input, two physically large 10kW resistors can dissipate the maximum pulse power. They are decoupled with a 1nF capacitor. Moving towards the APD, a second smaller quenching resistor 50Ω is decoupled by two 0.047µF capacitors. This smaller quenching resistor acts to dampen ringing especially under high slew rates due to large optical inputs pulses. All capacitors must be rated for high voltage as APD bias voltages can run above 200V.

### Dramatically Improving the LTC6561's Dynamic Range

While the LTC6561's 30µA of linear input range is quite respectable, it is possible to dramatically improve the range over which input current can be accurately measured. The measurement range can be increased from 30µA to at least 3mA, a 100x improvement in current measurement range! As the input current exceeds the linear range, the output pulse amplitude saturates. Once

## APPLICATIONS INFORMATION

in saturation, the pulse width widens in a predictable manner. Pulse stretching is a function of input capacitance, but fortunately insensitive to temperature.

This behavior is demonstrated using the FT2563 evaluation board. This evaluation board uses a series 2k resistor to convert a voltage pulse to a current pulse as it is difficult to obtain a fast current pulse generator. The input is terminated in 50Ω so that current pulses of known quantity are generated at the TIA input using a voltage source. Sweeping the TIA pulse input current from 2.8µA to 3mA, we see that as the current surpasses the 30µA saturation point, the output pulse width increases (Figure 7b).

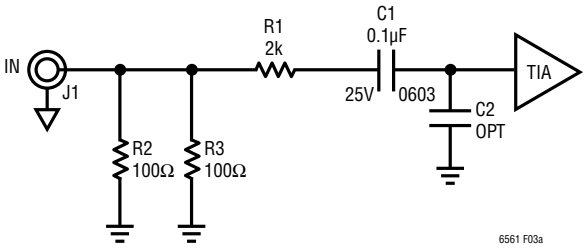



**Figure 7a.**

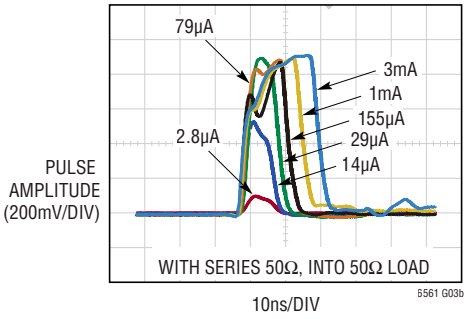



**Figure 7b. Output Pulse Over Input Current**

When we plot the pulse stretching (output response width – input pulse width), we see that the stretching is linearly proportional to the input current. Below, the saturation point of 30µA the pulse stretching falls to zero. Here we have used the simple FWHM (full width half max) criteria to establish the pulse width. The pulse width is taken at half of the maximum swing, usually around 0.45V. A more sophisticated algorithm could be used to gain greater accuracy assuming the pulse shape is accurately captured by an ADC. A plot of pulse stretching vs input current with $C_{IN}$ = 0.5pF is shown in Figure 8a. Figure 8b shows pulse stretching with 4pF on input capacitance. current range in.

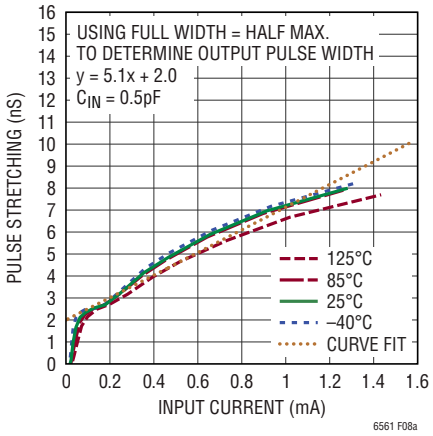



**Figure 8a. Pulse Stretching $C_{IN}$ = 0.5pF, Using FWHM**

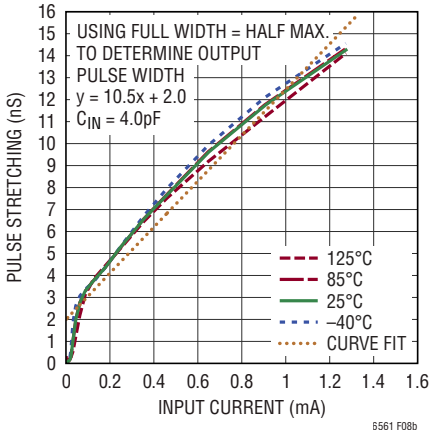
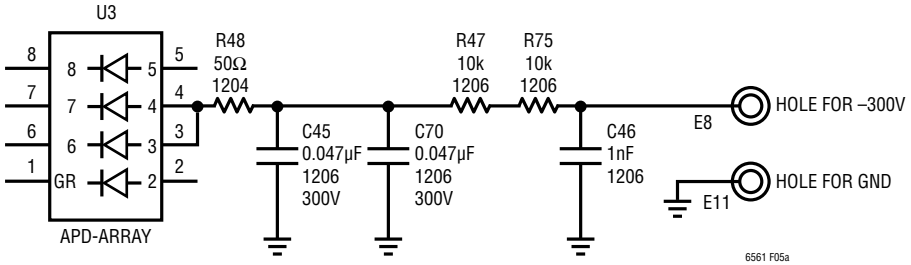



**Figure 8b. Pulse Stretching $C_{IN}$ = 4pF, Using FWHM**

The same pulse stretching has been demonstrated using optical excitation. Independently measuring the current generated during an optical pulse impinging on an APD is quite difficult. The parasitics of any measuring device will impair the actual pulse input. Refer to Figure 9. Using a balun across series resistor R48 feeding the APD, we can get an independent determination of APD current to the TIA for moderate laser input powers. Again, when this APD current is plotted versus pulse stretching, we find a nearly linear relationship under moderate illumination.

## APPLICATIONS INFORMATION



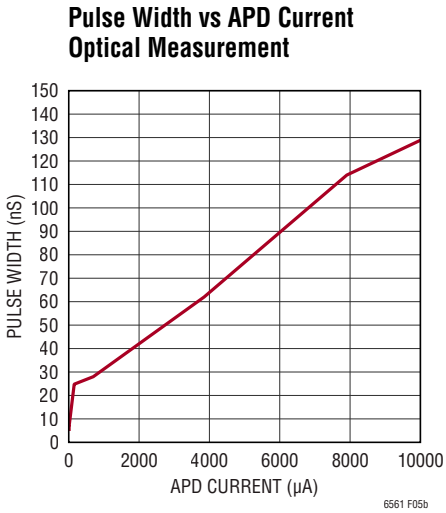




**Figure 9. Typical APD Bias Circuit**

Using a calibrated laser source, we find that pulse stretching continues even at extremely high laser power levels of 50 Watts! At high illumination levels, the relationship no longer appears perfectly linear, but the potential to measure these high power levels is possible. Of course, with any system, a calibration of optical input power to pulse stretching should be done as the optical gain is a strong function of the APD reverse bias, temperature and the choice of APD.

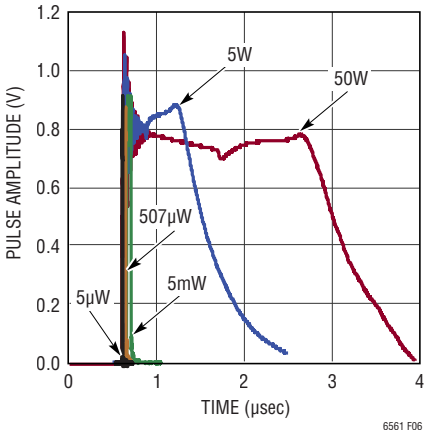
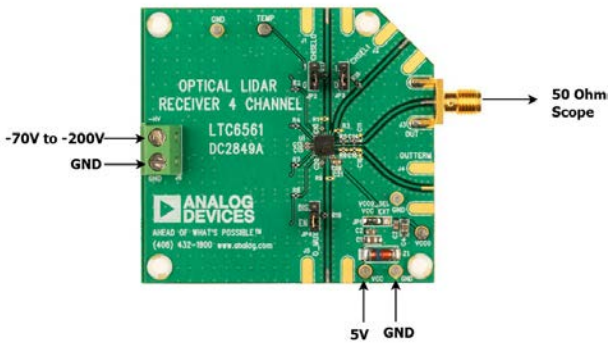


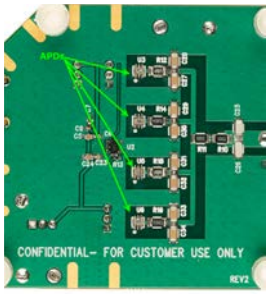

**Figure 10. Pulse Width vs Input Hi Power Optical**

# APPLICATIONS INFORMATION

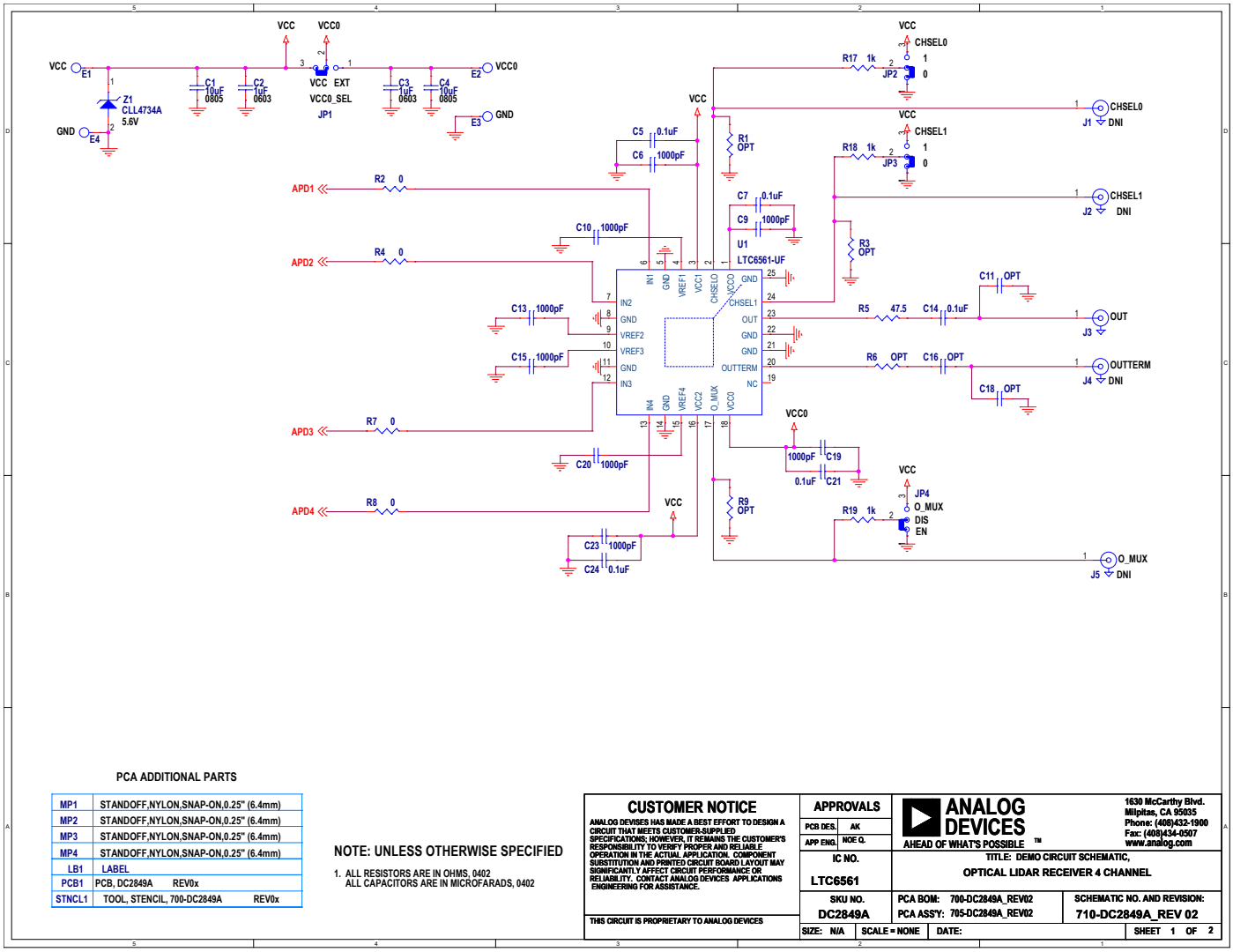
## DC2849 4-Channel Demonstration Circuit for Optical Evaluation




DC2849 Front Side



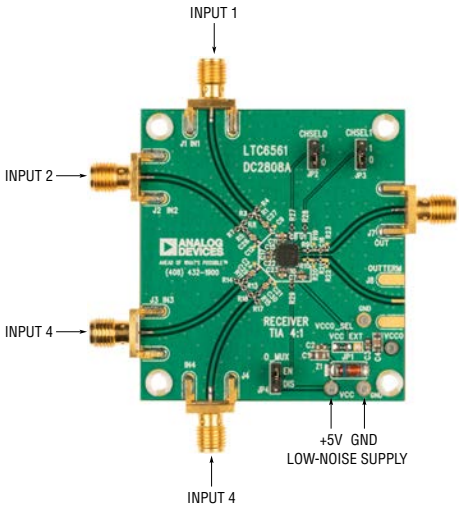

DC2849 Back Side

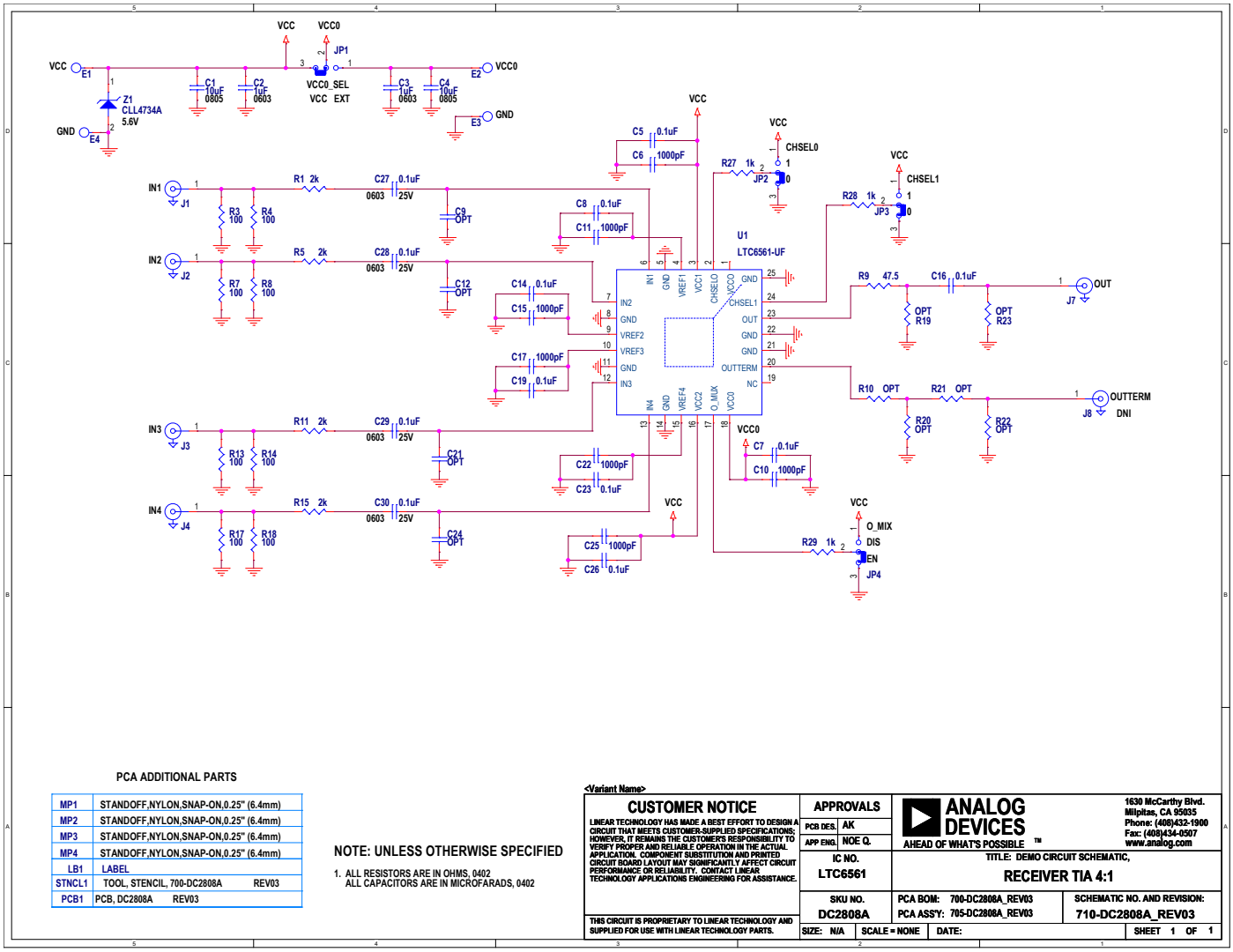



Rev. C

# APPLICATIONS INFORMATION

## DC2808 4-Channel Demonstration Circuit for Electrical Evaluation




PCA ADDITIONAL PARTS

| | | |
|---|---|---|
| MP1 | STANDOFF,NYLON,SNAP-ON,0.25" (6.4mm) | |
| MP2 | STANDOFF,NYLON,SNAP-ON,0.25" (6.4mm) | |
| MP3 | STANDOFF,NYLON,SNAP-ON,0.25" (6.4mm) | |
| MP4 | STANDOFF,NYLON,SNAP-ON,0.25" (6.4mm) | |
| LB1 | LABEL | |
| STNCL1 | TOOL, STENCIL, 700-DC2808A | REV03 |
| PCB1 | PCB, DC2808A | REV03 |

NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 0402
   ALL CAPACITORS ARE IN MICROFARADS, 0402

<Variant Name>

**CUSTOMER NOTICE**

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.

THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

| APPROVALS | |
|---|---|
| PCB DES. | AK |
| APP ENG. | NOE Q. |

IC NO. LTC6561

SKU NO. DC2808A

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TITLE: DEMO CIRCUIT SCHEMATIC,
RECEIVER TIA 4:1

PCA BOM: 700-DC2808A_REV03
PCA ASSY: 705-DC2808A_REV03

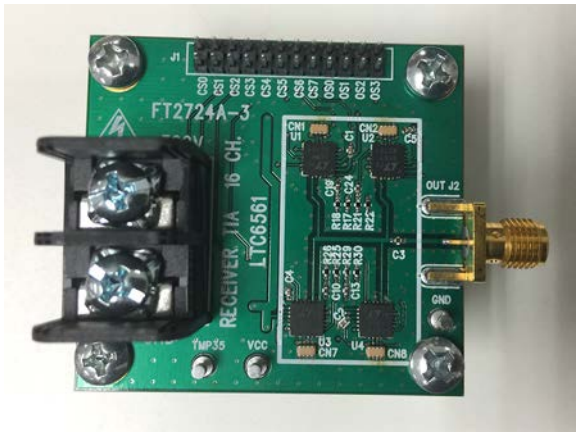
SCHEMATIC NO. AND REVISION: 710-DC2808A_REV03

SIZE: N/A | SCALE = NONE | DATE: | SHEET 1 OF 1

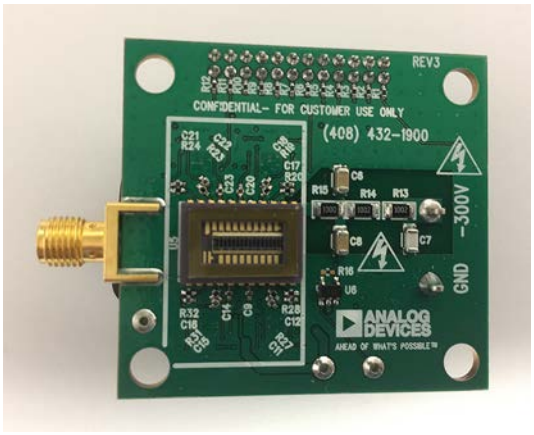
Rev. C

# APPLICATIONS INFORMATION

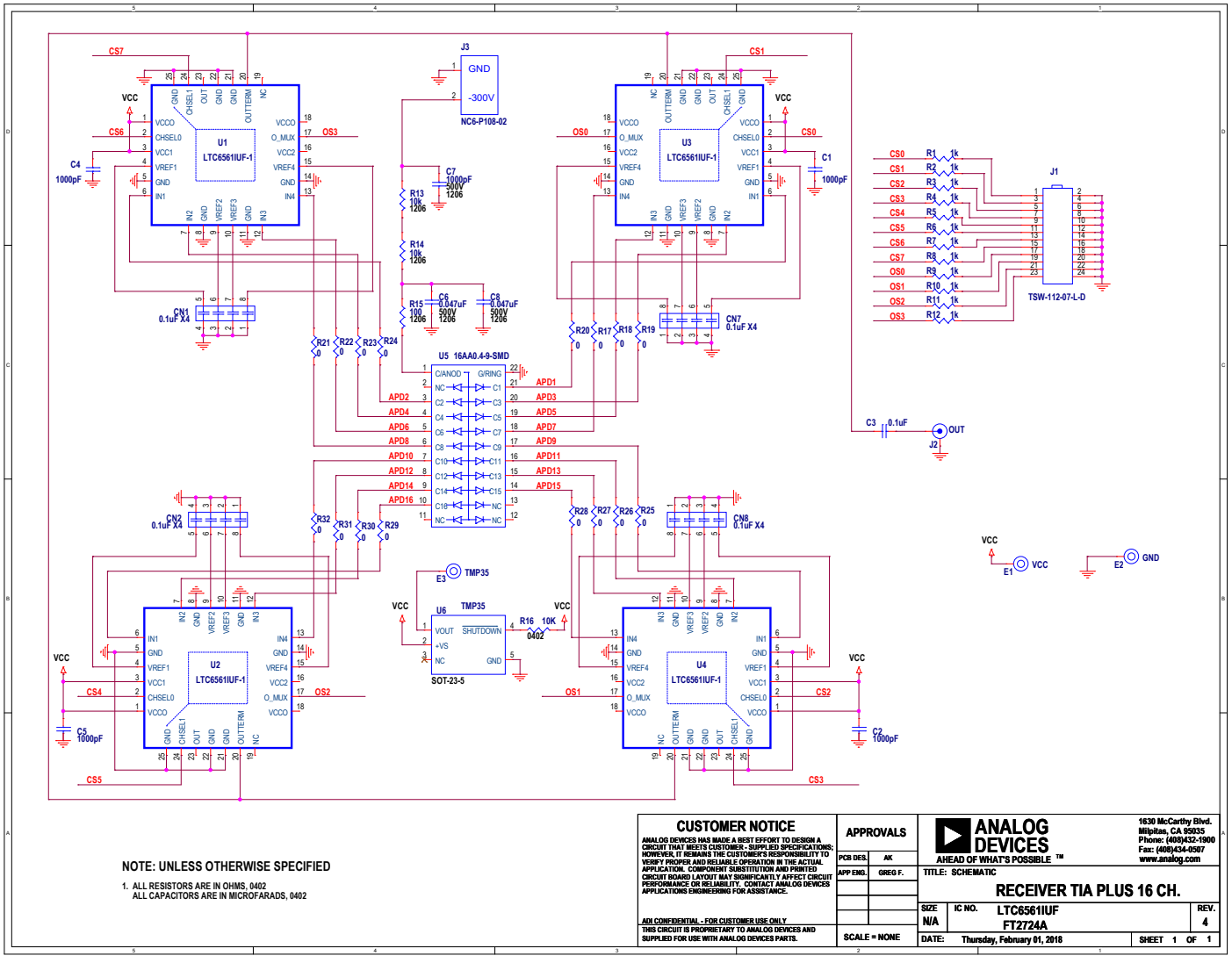
### FT2724 16-Channel Demonstration Circuit for Optical or Electrical Evaluation




FT2724 Front Side



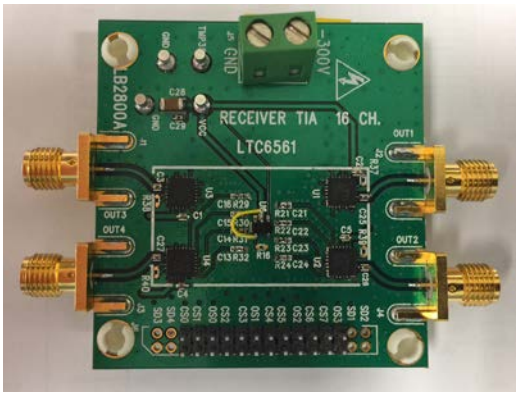

FT2724 Back Side



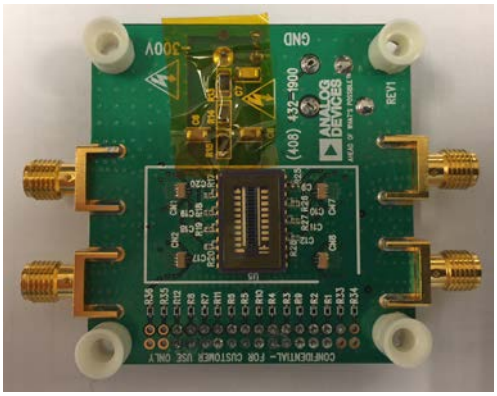

Rev. C

# APPLICATIONS INFORMATION

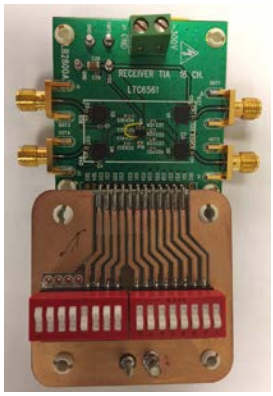
### LB2800 16:4 Channel Demonstration Circuit for Optical Evaluation



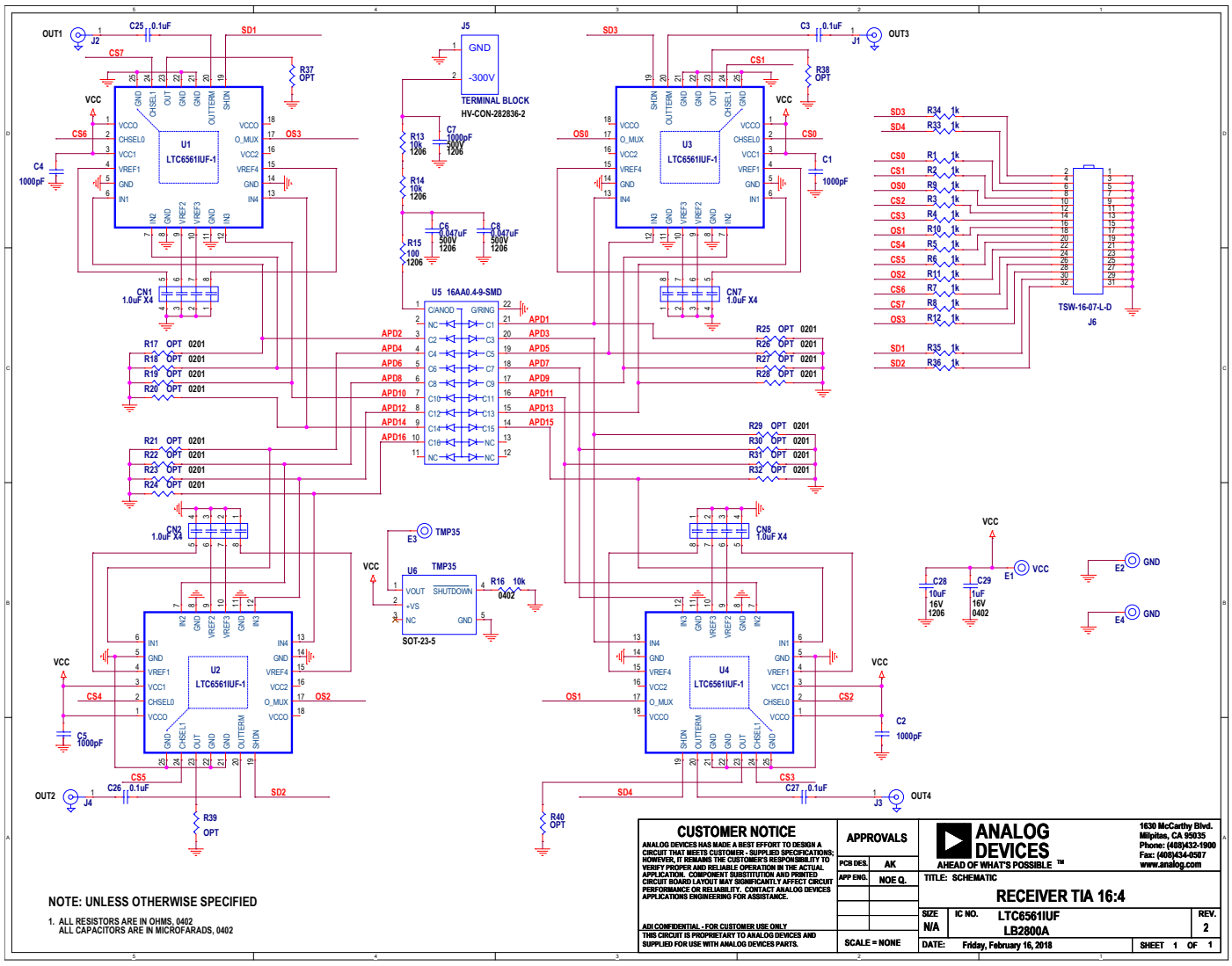

LB2800 Front Side




LB2800 Back Side

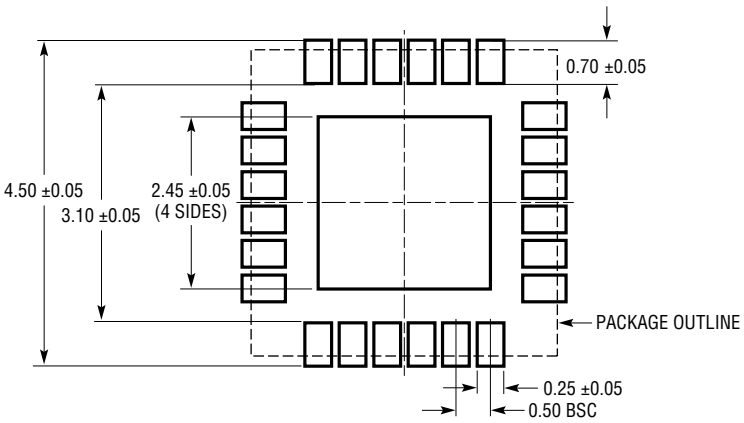



FT2724 with Switch Board

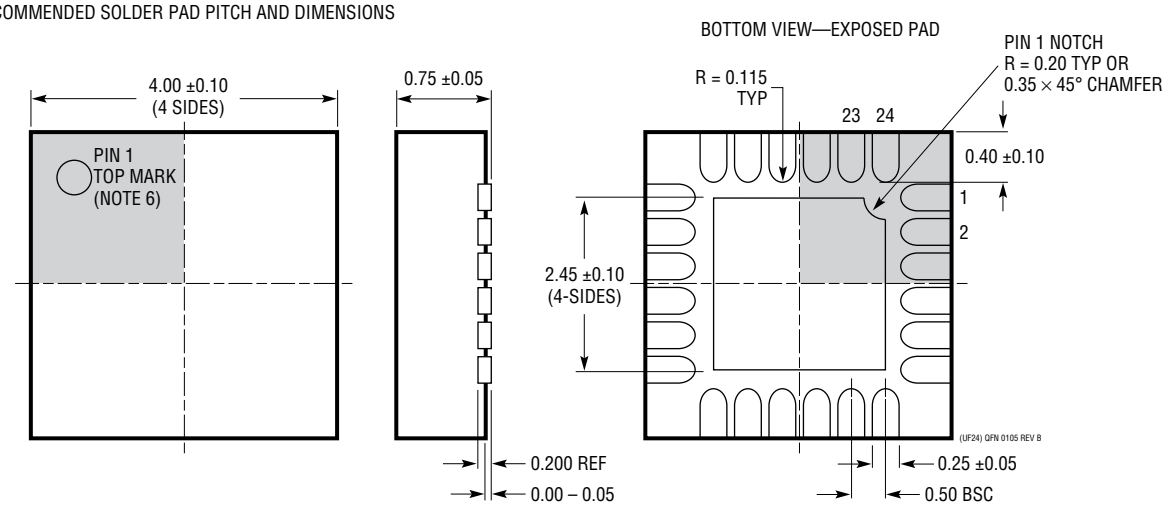


# PACKAGE DESCRIPTION

**UF Package**
**24-Lead Plastic QFN (4mm × 4mm)**
(Reference LTC DWG # 05-08-1697 Rev B)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



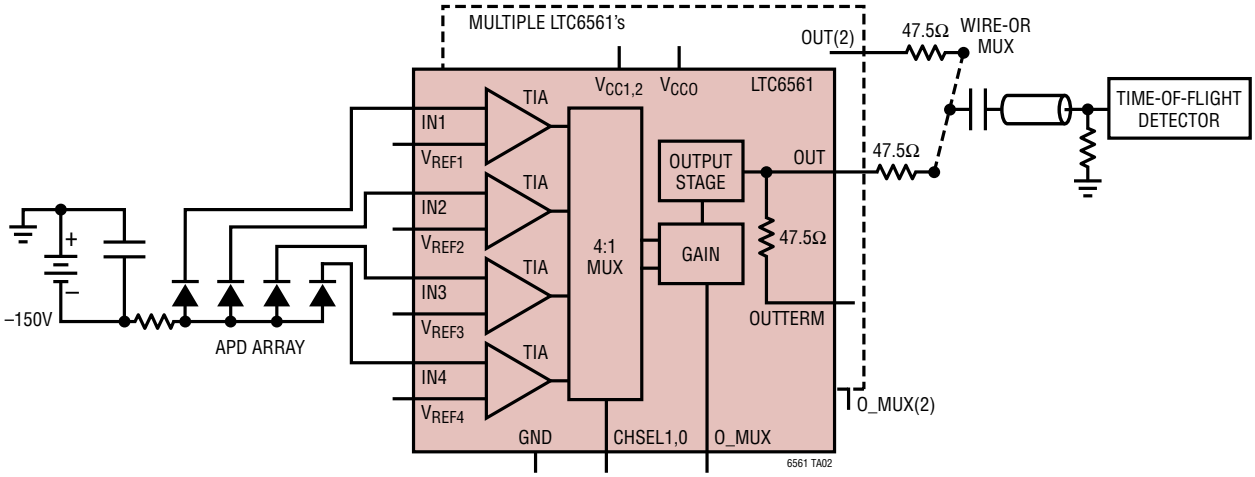

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 09/18 | Edited Description | 1 |
| | | Edited Absolute Maximum Ratings | 2 |
| B | 11/18 | Added H-Grade option (–40°C to 125°C) | All |
| C | 11/19 | Added W-Grade (Automotive) option | All |

## TYPICAL APPLICATION

**Typical Application with Multiplexed Output**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC6560 | Single Channel 220MHz 74k TIA | Single Channel Version of the LTC6561 |
| LTC6268 | 500MHz Ultra Low Bias Current FET Input Op Amp | GBW = 500MHz, –3dB BW = 350MHz, Ib = ±3FA |
| LTC6268-10 | 4GHz Ultra Low Bias Current FET Input Op Amp | De-Comped Version of the LTC6268, GBW = 4GHz |
| LTC6244 | Dual 50MHz, Low Noise, Rail-to-Rail CMOS Op Amp | GBW = 50MHz, Ib = 1pA |
| LTC6240/LTC6241/ LTC6242 | Single/Dual/Quad 18MHz, Low Noise, Rail-to-Rail Output CMOS Op Amps | GBW = 18MHz, Ib = 0.2pA, 0.1Hz-10Hz, Noise 550nV$_{P-P}$ |
| LTC6409 | 10GHz Bandwidth, 1.1nV/√Hz Differential Amplifier/ADC Driver | GBW = 10GHz, en = 1.1nV/√Hz |
| ADA4939-1 | Ultralow Distortion Differential ADC Driver | Slew Rate: 6800V/µs |
| AD9694 | Quad 14-Bit, 500Msps, 1.2V/2.5V ADC | JESD204B |
| AD9695-625 | 14-Bit, 1300Msps/625Msps, JESD204B, Dual ADC | JESD204B |
| HMCAD1511 | High Speed Multi-Mode 8-Bit GSPS A/D Converter | Serial LVDS |