

# Twelve Output Differential Buffer for PCIe Gen3

**9DB1233**

## Recommended Application

12 output PCIe Gen3 zero-delay/fanout buffer

## General Description

The 9DB1233 zero-delay buffer supports PCIe Gen3 requirements, while being backwards compatible to PCIe Gen2 and Gen1. The 9DB1233 is driven by a differential SRC output pair from an IDT 932S421 or 932SQ420 or equivalent main clock generator. It attenuates jitter on the input clock and has a selectable PLL bandwidth to maximize performance in systems with or without Spread-Spectrum clocking.

## Output Features

- 12 - 0.7V current mode differential HCSL output pairs

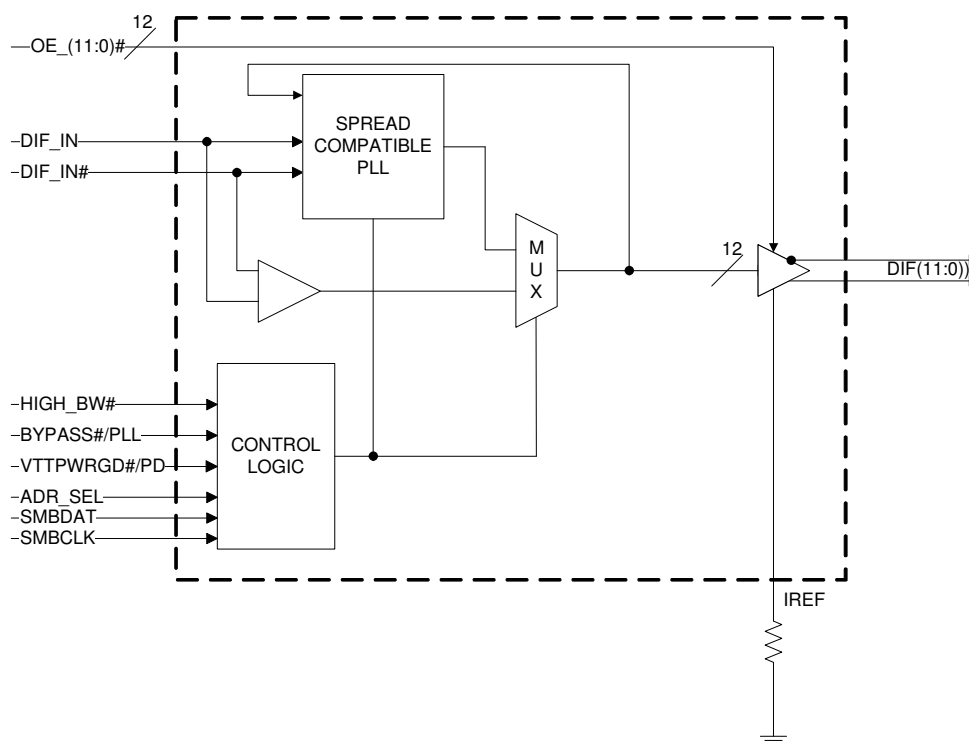
## Features/Benefits

- 3 Selectable SMBus Addresses/Multiple devices can share the same SMBus Segment
- 12 OE# pins/Hardware control of each output
- PLL or bypass mode/PLL can dejitter incoming clock
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- SMBus Interface/unused outputs can be disabled
- Supports undriven differential outputs in Power Down mode for power management

## Key Specifications

- Output cycle-cycle jitter < 50ps.
- Output-to-output skew < 50 ps
- PCIe Gen3 phase jitter < 1.0ps RMS
- Pin compatible with DB1200 Yellow Cover Device

## Functional Block Diagram



## Pin Configuration

|           |    |    |               |
|-----------|----|----|---------------|
| VDD       | 1  | 64 | VDDA          |
| DIF_IN    | 2  | 63 | AGND          |
| DIF_IN#   | 3  | 62 | IREF          |
| GND       | 4  | 61 | VDD           |
| OE0#      | 5  | 60 | OE11#         |
| DIF_0     | 6  | 59 | DIF_11        |
| DIF_0#    | 7  | 58 | DIF_11#       |
| VDD       | 8  | 57 | VDD           |
| GND       | 9  | 56 | GND           |
| OE1#      | 10 | 55 | OE10#         |
| DIF_1     | 11 | 54 | DIF_10        |
| DIF_1#    | 12 | 53 | DIF_10#       |
| OE2#      | 13 | 52 | OE9#          |
| DIF_2     | 14 | 51 | DIF_9         |
| DIF_2#    | 15 | 50 | DIF_9#        |
| GND       | 16 | 49 | GND           |
| VDD       | 17 | 48 | VDD           |
| OE3#      | 18 | 47 | OE8#          |
| DIF_3     | 19 | 46 | DIF_8         |
| DIF_3#    | 20 | 45 | DIF_8#        |
| OE4#      | 21 | 44 | OE7#          |
| DIF_4     | 22 | 43 | DIF_7         |
| DIF_4#    | 23 | 42 | DIF_7#        |
| VDD       | 24 | 41 | VDD           |
| GND       | 25 | 40 | GND           |
| OE5#      | 26 | 39 | OE6#          |
| DIF_5     | 27 | 38 | DIF_6         |
| DIF_5#    | 28 | 37 | DIF_6#        |
| **ADR_SEL | 29 | 36 | VTTTPWRGD#/PD |
| HIGH_BW#  | 30 | 35 | BYPASS#/PLL   |
| VDD       | 31 | 34 | GND           |
| SMBCLK    | 32 | 33 | SMBDAT        |

**64-TSSOP**

\*\* Indicates 120K ohm Pulldown

### SMBus Address Selection (Pin 29)

| ADR_SEL | Voltage      | SMBus Adr (Wr/Rd) |
|---------|--------------|-------------------|
| Low     | <0.8V        | DC/DD             |
| Mid     | 1.2<Vin<1.8V | D6/D7             |
| High    | Vin > 2.0V   | D4/D5             |

### Power Groups

| Pin Number            |                       | Description                   |
|-----------------------|-----------------------|-------------------------------|
| VDD                   | GND                   |                               |
| 1                     | 4                     | DIF_IN/DIF_IN#                |
| 8, 17, 24, 41, 48, 57 | 9, 16, 25, 40, 49, 56 | DIF(11:0)                     |
| N/A                   | 63                    | IREF                          |
| 64                    | 63                    | Analog VDD & GND for PLL core |

Note: Please treat pin 1 as an analog VDD.

## Pin Description

| PIN # | PIN NAME  | TYPE | DESCRIPTION                                                                                                  |
|-------|-----------|------|--------------------------------------------------------------------------------------------------------------|
| 1     | VDD       | PWR  | Power supply, nominal 3.3V                                                                                   |
| 2     | DIF_IN    | IN   | 0.7 V Differential TRUE input                                                                                |
| 3     | DIF_IN#   | IN   | 0.7 V Differential Complementary Input                                                                       |
| 4     | GND       | PWR  | Ground pin.                                                                                                  |
| 5     | OE0#      | IN   | Active low input for enabling DIF pair 0.<br>1 =disable outputs, 0 = enable outputs                          |
| 6     | DIF_0     | OUT  | 0.7V differential true clock output                                                                          |
| 7     | DIF_0#    | OUT  | 0.7V differential Complementary clock output                                                                 |
| 8     | VDD       | PWR  | Power supply, nominal 3.3V                                                                                   |
| 9     | GND       | PWR  | Ground pin.                                                                                                  |
| 10    | OE1#      | IN   | Active low input for enabling DIF pair 1.<br>1 =disable outputs, 0 = enable outputs                          |
| 11    | DIF_1     | OUT  | 0.7V differential true clock output                                                                          |
| 12    | DIF_1#    | OUT  | 0.7V differential Complementary clock output                                                                 |
| 13    | OE2#      | IN   | Active low input for enabling DIF pair 2.<br>1 =disable outputs, 0 = enable outputs                          |
| 14    | DIF_2     | OUT  | 0.7V differential true clock output                                                                          |
| 15    | DIF_2#    | OUT  | 0.7V differential Complementary clock output                                                                 |
| 16    | GND       | PWR  | Ground pin.                                                                                                  |
| 17    | VDD       | PWR  | Power supply, nominal 3.3V                                                                                   |
| 18    | OE3#      | IN   | Active low input for enabling DIF pair 3.<br>1 =disable outputs, 0 = enable outputs                          |
| 19    | DIF_3     | OUT  | 0.7V differential true clock output                                                                          |
| 20    | DIF_3#    | OUT  | 0.7V differential Complementary clock output                                                                 |
| 21    | OE4#      | IN   | Active low input for enabling DIF pair 4<br>1 =disable outputs, 0 = enable outputs                           |
| 22    | DIF_4     | OUT  | 0.7V differential true clock output                                                                          |
| 23    | DIF_4#    | OUT  | 0.7V differential Complementary clock output                                                                 |
| 24    | VDD       | PWR  | Power supply, nominal 3.3V                                                                                   |
| 25    | GND       | PWR  | Ground pin.                                                                                                  |
| 26    | OE5#      | IN   | Active low input for enabling DIF pair 5.<br>1 =disable outputs, 0 = enable outputs                          |
| 27    | DIF_5     | OUT  | 0.7V differential true clock output                                                                          |
| 28    | DIF_5#    | OUT  | 0.7V differential Complementary clock output                                                                 |
| 29    | **ADR_SEL | IN   | This tri-level input selects one of 3 SMBus addresses. See the SMBus Address Select Table for the addresses. |
| 30    | HIGH_BW#  | IN   | 3.3V input for selecting PLL Band Width<br>0 = High, 1= Low                                                  |
| 31    | VDD       | PWR  | Power supply, nominal 3.3V                                                                                   |
| 32    | SMBCLK    | IN   | Clock pin of SMBUS circuitry, 5V tolerant                                                                    |

## Pin Description (cont.)

| PIN # | PIN NAME    | TYPE | DESCRIPTION                                                                                                                                                                                                                           |
|-------|-------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 33    | SMBDAT      | I/O  | Data pin of SMBUS circuitry, 5V tolerant                                                                                                                                                                                              |
| 34    | GND         | PWR  | Ground pin.                                                                                                                                                                                                                           |
| 35    | BYPASS#/PLL | IN   | Input to select Bypass(fan-out) or PLL (ZDB) mode<br>0 = Bypass mode, 1= PLL mode                                                                                                                                                     |
| 36    | VTPWRGD#/PD | IN   | VTPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.  |
| 37    | DIF_6#      | OUT  | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 38    | DIF_6       | OUT  | 0.7V differential true clock output                                                                                                                                                                                                   |
| 39    | OE6#        | IN   | Active low input for enabling DIF pair 6.<br>1 =disable outputs, 0 = enable outputs                                                                                                                                                   |
| 40    | GND         | PWR  | Ground pin.                                                                                                                                                                                                                           |
| 41    | VDD         | PWR  | Power supply, nominal 3.3V                                                                                                                                                                                                            |
| 42    | DIF_7#      | OUT  | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 43    | DIF_7       | OUT  | 0.7V differential true clock output                                                                                                                                                                                                   |
| 44    | OE7#        | IN   | Active low input for enabling DIF pair 7.<br>1 =disable outputs, 0 = enable outputs                                                                                                                                                   |
| 45    | DIF_8#      | OUT  | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 46    | DIF_8       | OUT  | 0.7V differential true clock output                                                                                                                                                                                                   |
| 47    | OE8#        | IN   | Active low input for enabling DIF pair 8.<br>1 =disable outputs, 0 = enable outputs                                                                                                                                                   |
| 48    | VDD         | PWR  | Power supply, nominal 3.3V                                                                                                                                                                                                            |
| 49    | GND         | PWR  | Ground pin.                                                                                                                                                                                                                           |
| 50    | DIF_9#      | OUT  | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 51    | DIF_9       | OUT  | 0.7V differential true clock output                                                                                                                                                                                                   |
| 52    | OE9#        | IN   | Active low input for enabling DIF pair 9.<br>1 =disable outputs, 0 = enable outputs                                                                                                                                                   |
| 53    | DIF_10#     | OUT  | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 54    | DIF_10      | OUT  | 0.7V differential true clock output                                                                                                                                                                                                   |
| 55    | OE10#       | IN   | Active low input for enabling DIF pair 10.<br>1 =disable outputs, 0 = enable outputs                                                                                                                                                  |
| 56    | GND         | PWR  | Ground pin.                                                                                                                                                                                                                           |
| 57    | VDD         | PWR  | Power supply, nominal 3.3V                                                                                                                                                                                                            |
| 58    | DIF_11#     | OUT  | 0.7V differential Complementary clock output                                                                                                                                                                                          |
| 59    | DIF_11      | OUT  | 0.7V differential true clock output                                                                                                                                                                                                   |
| 60    | OE11#       | IN   | Active low input for enabling DIF pair 11.<br>1 =disable outputs, 0 = enable outputs                                                                                                                                                  |
| 61    | VDD         | PWR  | Power supply, nominal 3.3V                                                                                                                                                                                                            |
| 62    | IREF        | OUT  | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 63    | AGND        | PWR  | Analog Ground pin for Core PLL                                                                                                                                                                                                        |
| 64    | VDDA        | PWR  | 3.3V power for the PLL core.                                                                                                                                                                                                          |

**Electrical Characteristics - Absolute Maximum Ratings**

| PARAMETER                 | SYMBOL             | CONDITIONS                 | MIN     | TYP | MAX                   | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage  | VDDA               |                            |         |     | 4.6                   | V     | 1,2   |
| 3.3V Logic Supply Voltage | VDD                |                            |         |     | 4.6                   | V     | 1,2   |
| Input Low Voltage         | V <sub>IL</sub>    |                            | GND-0.5 |     |                       | V     | 1     |
| Input High Voltage        | V <sub>IH</sub>    | Except for SMBus interface |         |     | V <sub>DD</sub> +0.5V | V     | 1     |
| Input High Voltage        | V <sub>IHSMB</sub> | SMBus clock and data pins  |         |     | 5.5V                  | V     | 1     |
| Storage Temperature       | T <sub>s</sub>     |                            | -65     |     | 150                   | °C    | 1     |
| Junction Temperature      | T <sub>j</sub>     |                            |         |     | 125                   | °C    | 1     |
| Input ESD protection      | ESD prot           | Human Body Model           | 2000    |     |                       | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

**Electrical Characteristics - Input/Supply/Common Parameters**

T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER                     | SYMBOL                | CONDITIONS                                                                                                                                              | MIN       | TYP    | MAX                   | UNITS  | NOTES |
|-------------------------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature | T <sub>COM</sub>      | Commercial range                                                                                                                                        | 0         |        | 70                    | °C     | 1     |
| Input High Voltage            | V <sub>IH</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs                                                                                   | 2         |        | V <sub>DD</sub> + 0.3 | V      | 1     |
| Input Low Voltage             | V <sub>IL</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs                                                                                   | GND - 0.3 |        | 0.8                   | V      | 1     |
| Input Current                 | I <sub>IN</sub>       | Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD                                                                                       | -5        |        | 5                     | uA     | 1     |
|                               | I <sub>INP</sub>      | Single-ended inputs<br>V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors<br>V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors | -200      |        | 200                   | uA     | 1     |
| Input Frequency               | F <sub>ibyp</sub>     | V <sub>DD</sub> = 3.3 V, Bypass mode                                                                                                                    | 10        |        | 166                   | MHz    | 2     |
|                               | F <sub>ipll</sub>     | V <sub>DD</sub> = 3.3 V, 100MHz PLL mode                                                                                                                | 90        | 100.00 | 110                   | MHz    | 2     |
| Pin Inductance                | L <sub>pin</sub>      |                                                                                                                                                         |           |        | 7                     | nH     | 1     |
| Capacitance                   | C <sub>IN</sub>       | Logic Inputs, except DIF_IN                                                                                                                             | 1.5       |        | 5                     | pF     | 1     |
|                               | C <sub>INDIF_IN</sub> | DIF_IN differential clock inputs                                                                                                                        | 1.5       |        | 5                     | pF     | 1,4   |
|                               | C <sub>OUT</sub>      | Output pin capacitance                                                                                                                                  |           |        | 6                     | pF     | 1     |
| Clk Stabilization             | T <sub>STAB</sub>     | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock                                                   |           |        | 1.8                   | ms     | 1,2   |
| Input SS Modulation Frequency | f <sub>MODIN</sub>    | Allowable Frequency (Triangular Modulation)                                                                                                             | 30        |        | 33                    | kHz    | 1     |
| OE# Latency                   | t <sub>LATOE#</sub>   | DIF start after OE# assertion<br>DIF stop after OE# deassertion                                                                                         | 4         |        | 12                    | cycles | 1,3   |
| Tdrive_PD#                    | t <sub>DRVPD</sub>    | DIF output enable after PD# de-assertion                                                                                                                |           |        | 300                   | us     | 1,3   |
| Tfall                         | t <sub>F</sub>        | Fall time of control inputs                                                                                                                             |           |        | 5                     | ns     | 1,2   |
| Trise                         | t <sub>R</sub>        | Rise time of control inputs                                                                                                                             |           |        | 5                     | ns     | 1,2   |
| SMBus Input Low Voltage       | V <sub>ILSMB</sub>    |                                                                                                                                                         |           |        | 0.8                   | V      | 1     |
| SMBus Input High Voltage      | V <sub>IHSMB</sub>    |                                                                                                                                                         | 2.1       |        | V <sub>DDSMB</sub>    | V      | 1     |
| SMBus Output Low Voltage      | V <sub>OLSMB</sub>    | @ I <sub>PULLUP</sub>                                                                                                                                   |           |        | 0.4                   | V      | 1     |
| SMBus Sink Current            | I <sub>PULLUP</sub>   | @ V <sub>OL</sub>                                                                                                                                       | 4         |        |                       | mA     | 1     |
| Nominal Bus Voltage           | V <sub>DDSMB</sub>    | 3V to 5V +/- 10%                                                                                                                                        | 2.7       |        | 5.5                   | V      | 1     |
| SCLK/SDATA Rise Time          | t <sub>RSMB</sub>     | (Max VIL - 0.15) to (Min VIH + 0.15)                                                                                                                    |           |        | 1000                  | ns     | 1     |
| SCLK/SDATA Fall Time          | t <sub>FSMB</sub>     | (Min VIH + 0.15) to (Max VIL - 0.15)                                                                                                                    |           |        | 300                   | ns     | 1     |
| SMBus Operating Frequency     | f <sub>MAXSMB</sub>   | Maximum SMBus operating frequency                                                                                                                       |           |        | 100                   | kHz    | 1,5   |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active

**Electrical Characteristics - Clock Input Parameters**T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER                          | SYMBOL             | CONDITIONS                                                | MIN                   | TYP | MAX  | UNITS | NOTES |
|------------------------------------|--------------------|-----------------------------------------------------------|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN        | V <sub>IHDIF</sub> | Differential inputs<br>(single-ended measurement)         | 600                   | 800 | 1150 | mV    | 1     |
| Input Low Voltage - DIF_IN         | V <sub>ILDIF</sub> | Differential inputs<br>(single-ended measurement)         | V <sub>SS</sub> - 300 | 0   | 300  | mV    | 1     |
| Input Common Mode Voltage - DIF_IN | V <sub>COM</sub>   | Common Mode Input Voltage                                 | 300                   |     | 1000 | mV    | 1     |
| Input Amplitude - DIF_IN           | V <sub>SWING</sub> | Peak to Peak value                                        | 300                   |     | 1450 | mV    | 1     |
| Input Slew Rate - DIF_IN           | dv/dt              | Measured differentially                                   | 0.4                   |     | 8    | V/ns  | 1,2   |
| Input Leakage Current              | I <sub>IN</sub>    | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND | -5                    |     | 5    | uA    | 1     |
| Input Duty Cycle                   | d <sub>tin</sub>   | Measurement from differential wavefrom                    | 45                    |     | 55   | %     | 1     |
| Input Jitter - Cycle to Cycle      | J <sub>DIFIn</sub> | Differential Measurement                                  | 0                     |     | 125  | ps    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.<sup>2</sup> Slew rate measured through +/-75mV window centered around differential zero**Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs**T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER              | SYMBOL                 | CONDITIONS                                                                                            | MIN  | TYP | MAX  | UNITS | NOTES   |
|------------------------|------------------------|-------------------------------------------------------------------------------------------------------|------|-----|------|-------|---------|
| Slew rate              | Trf                    | Scope averaging on                                                                                    | 1    | 2.4 | 4    | V/ns  | 1, 2, 3 |
| Slew rate matching     | ΔTrf                   | Slew rate matching, Scope averaging on                                                                |      |     | 20   | %     | 1, 2, 4 |
| Voltage High           | V <sub>High</sub>      | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660  | 800 | 850  | mV    | 1       |
| Voltage Low            | V <sub>Low</sub>       |                                                                                                       | -150 | 20  | 150  |       | 1       |
| Max Voltage            | V <sub>max</sub>       | Measurement on single ended signal using absolute value. (Scope averaging off)                        |      | 850 | 1150 | mV    | 1       |
| Min Voltage            | V <sub>min</sub>       |                                                                                                       | -300 |     |      |       | 1       |
| Vswing                 | V <sub>swing</sub>     | Scope averaging off                                                                                   | 300  |     |      | mV    | 1, 2    |
| Crossing Voltage (abs) | V <sub>cross_abs</sub> | Scope averaging off                                                                                   | 250  |     | 550  | mV    | 1, 5    |
| Crossing Voltage (var) | ΔV <sub>cross</sub>    | Scope averaging off                                                                                   |      |     | 140  | mV    | 1, 6    |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production. I<sub>REF</sub> = VDD/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub>=50Ω (100Ω differential impedance).<sup>2</sup> Measured from differential waveform<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.<sup>5</sup> V<sub>cross</sub> is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).<sup>6</sup> The total variation of all V<sub>cross</sub> measurements in any particular system. Note that this is a subset of V<sub>cross\_min/max</sub> (V<sub>cross</sub> absolute) allowed. The intent is to limit V<sub>cross</sub> induced modulation by setting V<sub>cross\_delta</sub> to be smaller than V<sub>cross</sub> absolute.**Electrical Characteristics - Current Consumption**T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER                | SYMBOL                | CONDITIONS                                              | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-----------------------|---------------------------------------------------------|-----|-----|-----|-------|-------|
| Operating Supply Current | I <sub>DD3.3OP</sub>  | All outputs active @100MHz, C <sub>L</sub> = Full load; |     | 300 | 375 | mA    | 1     |
| Powerdown Current        | I <sub>DD3.3PD</sub>  | All diff pairs driven                                   |     | NA  |     | mA    | 1     |
|                          | I <sub>DD3.3PDZ</sub> | All differential pairs tri-stated                       |     | 21  | 24  | mA    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

**Electrical Characteristics - Output Duty Cycle, Jitter, Skew and PLL Characteristics**TA = T<sub>COM</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER              | SYMBOL               | CONDITIONS                                   | MIN  | TYP  | MAX  | UNITS | NOTES |
|------------------------|----------------------|----------------------------------------------|------|------|------|-------|-------|
| PLL Bandwidth          | BW                   | -3dB point in High BW Mode                   | 2    | 3    | 4    | MHz   | 1     |
|                        |                      | -3dB point in Low BW Mode                    | 0.7  | 1    | 1.4  | MHz   | 1     |
| PLL Jitter Peaking     | t <sub>JPEAK</sub>   | Peak Pass band Gain                          |      | 1.5  | 2    | dB    | 1     |
| Duty Cycle             | t <sub>DC</sub>      | Measured differentially, PLL Mode            | 45   | 49.5 | 55   | %     | 1     |
| Duty Cycle Distortion  | t <sub>DCD</sub>     | Measured differentially, Bypass Mode @100MHz | -2   | 0    | 2    | %     | 1,4   |
| Skew, Input to Output  | t <sub>pdBYP</sub>   | Bypass Mode, V <sub>T</sub> = 50%            | 2500 |      | 4500 | ps    | 1     |
|                        | t <sub>pdPLL</sub>   | PLL Mode V <sub>T</sub> = 50%                | -250 |      | 250  | ps    | 1     |
| Skew, Output to Output | t <sub>sk3</sub>     | V <sub>T</sub> = 50%                         |      | 45   | 50   | ps    | 1     |
| Jitter, Cycle to cycle | t <sub>jcc-cyc</sub> | PLL mode                                     |      | 25   | 50   | ps    | 1,3   |
|                        |                      | Additive Jitter in Bypass Mode               |      | 25   | 50   | ps    | 1,3   |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.<sup>2</sup>I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub>=50Ω.<sup>3</sup>Measured from differential waveform<sup>4</sup>Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.**Electrical Characteristics - PCIe Phase Jitter Parameters**TA = T<sub>COM</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER                             | SYMBOL                 | CONDITIONS                                           | MIN | TYP  | MAX | UNITS    | Notes     |
|---------------------------------------|------------------------|------------------------------------------------------|-----|------|-----|----------|-----------|
| Phase Jitter, PLL Mode                | t <sub>jphPCIeG1</sub> | PCIe Gen 1                                           |     | 34   | 86  | ps (p-p) | 1,2,3     |
|                                       | t <sub>jphPCIeG2</sub> | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz             |     | 1.1  | 3   | ps (rms) | 1,2       |
|                                       |                        | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz) |     | 2.2  | 3.1 | ps (rms) | 1,2       |
|                                       | t <sub>jphPCIeG3</sub> | PCIe Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)        |     | 0.4  | 1   | ps (rms) | 1,2,4,5   |
| Additive Phase Jitter,<br>Bypass Mode | t <sub>jphPCIeG1</sub> | PCIe Gen 1                                           |     | 2    | 5   | ps (p-p) | 1,2,3     |
|                                       | t <sub>jphPCIeG2</sub> | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz             |     | 0.5  | 0.6 | ps (rms) | 1,2,6     |
|                                       |                        | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz) |     | 0.8  | 1   | ps (rms) | 1,2,6     |
|                                       | t <sub>jphPCIeG3</sub> | PCIe Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)        |     | 0.35 | 0.5 | ps (rms) | 1,2,4,5,6 |

<sup>1</sup>Applies to all outputs when driven by 932SQ420DGLF or equivalent.<sup>2</sup>See <http://www.pcisiq.com> for complete specs<sup>3</sup>Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.<sup>4</sup>Subject to final radification by PCI SIG.<sup>5</sup>Calculated from Intel-supplied Clock Jitter Tool v 1.6.4<sup>6</sup>For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter) = SQRT{(total jitter)^2 - (input jitter)^2}

### Clock Periods Differential Outputs with Spread Spectrum Enabled

| Measurement Window |         | 1 Clock                 | 1us                     | 0.1s                    | 0.1s     | 0.1s              | 1us                | 1 Clock  | Units | Notes |
|--------------------|---------|-------------------------|-------------------------|-------------------------|----------|-------------------|--------------------|----------|-------|-------|
| Symbol             |         | Lg-                     | -SSC                    | -ppm error              | 0ppm     | + ppm error       | +SSC               | Lg+      |       |       |
| Definition         |         | Absolute Period         | Short-term Average      | Long-Term Average       | Period   | Long-Term Average | Short-term Average | Period   |       |       |
|                    |         | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal  | Maximum           | Maximum            | Maximum  |       |       |
| DIF                | DIF 100 | 9.87400                 | 9.99900                 | 9.99900                 | 10.00000 | 10.00100          | 10.05130           | 10.17630 | ns    | 1,2,3 |

### Clock Periods Differential Outputs with Spread Spectrum Disabled

| Clock: On-chip Differential Outputs with Spread Spectrum Disabled |         |                         |                         |                         |          |                   |                    |          |       |       |
|-------------------------------------------------------------------|---------|-------------------------|-------------------------|-------------------------|----------|-------------------|--------------------|----------|-------|-------|
| Measurement Window                                                |         | 1 Clock                 | 1us                     | 0.1s                    | 0.1s     | 0.1s              | 1us                | 1 Clock  |       |       |
| Symbol                                                            |         | Lg-                     | -SSC                    | -ppm error              | 0ppm     | + ppm error       | +SSC               | Lg+      |       |       |
| Definition                                                        |         | Absolute Period         | Short-term Average      | Long-Term Average       | Period   | Long-Term Average | Short-term Average | Period   |       |       |
|                                                                   |         | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal  | Maximum           | Maximum            | Maximum  | Units | Notes |
| DIF                                                               | DIF 100 | 9.87400                 |                         | 9.99900                 | 10.00000 | 10.00100          |                    | 10.17630 | ns    | 1,2,3 |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK420BQ accuracy requirements. The 9DB1233 itself does not contribute to ppm error.

<sup>3</sup> Driven by SRC output of main clock, PLL or Bypass mode



| DIF Reference Clock                             |  |                    |      |
|-------------------------------------------------|--|--------------------|------|
| Common Recommendations for Differential Routing |  | Dimension or Value | Unit |
| L1 length, route as non-coupled 50ohm trace     |  | 0.5 max            | inch |
| L2 length, route as non-coupled 50ohm trace     |  | 0.2 max            | inch |
| L3 length, route as non-coupled 50ohm trace     |  | 0.2 max            | inch |
| Rs                                              |  | 33                 | ohm  |
| Rt                                              |  | 49.9               | ohm  |

| Down Device Differential Routing                                 |  |                     |      |
|------------------------------------------------------------------|--|---------------------|------|
| L4 length, route as coupled microstrip 100ohm differential trace |  | 2 min to 16 max     | inch |
| L4 length, route as coupled stripline 100ohm differential trace  |  | 1.8 min to 14.4 max | inch |

| Differential Routing to PCI Express Connector                    |  |                       |      |
|------------------------------------------------------------------|--|-----------------------|------|
| L4 length, route as coupled microstrip 100ohm differential trace |  | 0.25 to 14 max        | inch |
| L4 length, route as coupled stripline 100ohm differential trace  |  | 0.225 min to 12.6 max | inch |

Figure 1: Down Device Routing

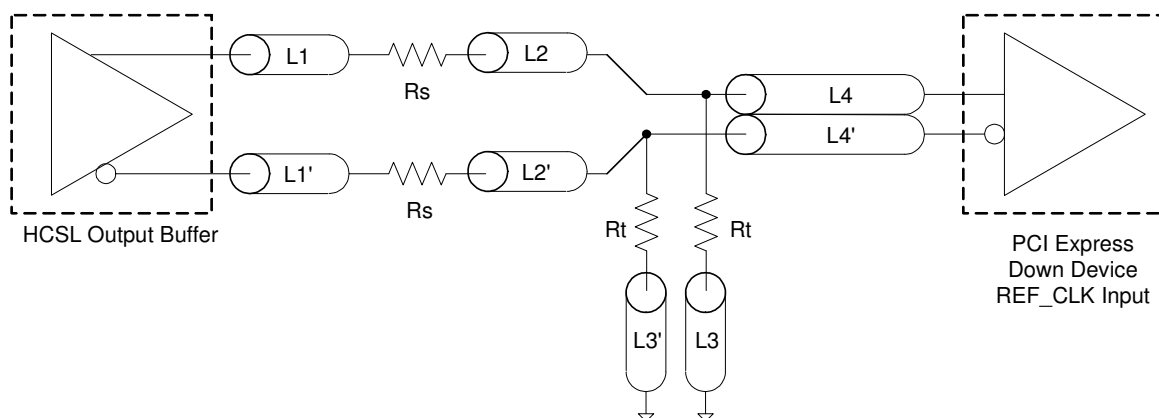
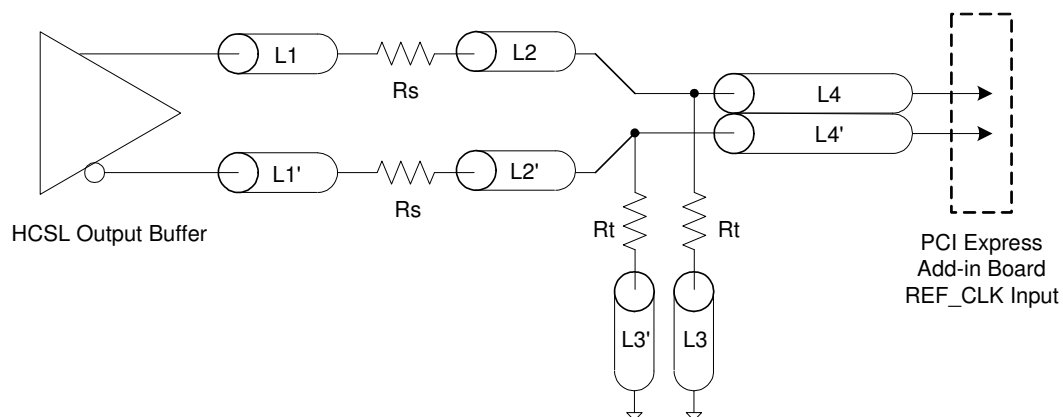


Figure 2: PCI Express Connector Routing

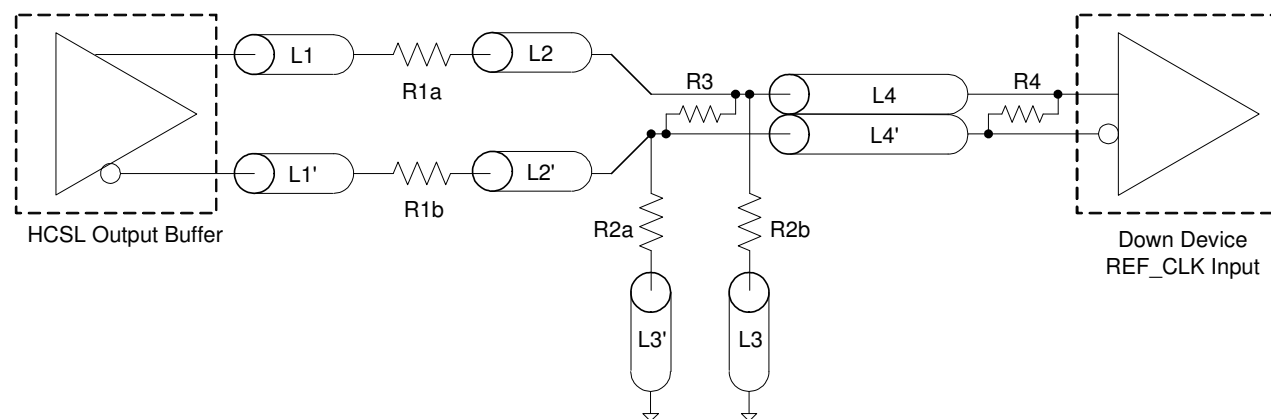


| Alternative Termination for LVDS and other Common Differential Signals (figure 3) |                  |                 |    |      |      |     |                                |
|-----------------------------------------------------------------------------------|------------------|-----------------|----|------|------|-----|--------------------------------|
| V <sub>diff</sub>                                                                 | V <sub>p-p</sub> | V <sub>cm</sub> | R1 | R2   | R3   | R4  | Note                           |
| 0.45v                                                                             | 0.22v            | 1.08            | 33 | 150  | 100  | 100 |                                |
| 0.58                                                                              | 0.28             | 0.6             | 33 | 78.7 | 137  | 100 |                                |
| 0.80                                                                              | 0.40             | 0.6             | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60                                                                              | 0.3              | 1.2             | 33 | 174  | 140  | 100 | Standard LVDS                  |

R1a = R1b = R1

R2a = R2b = R2

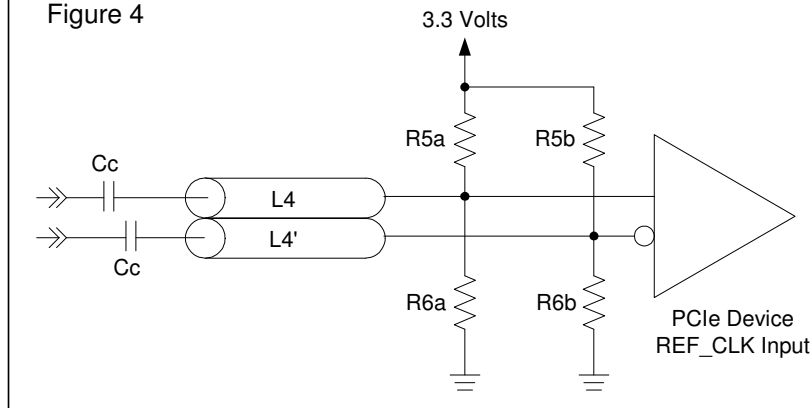
Figure 3



Cable Connected AC Coupled Application (figure 4)

| Component       | Value       | Note |
|-----------------|-------------|------|
| R5a, R5b        | 8.2K 5%     |      |
| R6a, R6b        | 1K 5%       |      |
| Cc              | 0.1 $\mu$ F |      |
| V <sub>cm</sub> | 0.350 volts |      |

Figure 4



## General SMBus serial interface information for the 9DB1233

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $DC_{(h)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the data byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $DC_{(h)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $DD_{(h)}$
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends **Byte N + X - 1**
- IDT clock sends **Byte 0 through byte X (if  $X_{(h)}$  was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation     |           |                      |     |
|---------------------------------|-----------|----------------------|-----|
| Controller (Host)               |           | IDT (Slave/Receiver) |     |
| T                               | starT bit |                      |     |
| Slave Address DC <sub>(h)</sub> |           |                      |     |
| WR                              | WRite     |                      |     |
|                                 |           | ACK                  |     |
| Beginning Byte = N              |           |                      |     |
|                                 |           | ACK                  |     |
| Data Byte Count = X             |           |                      |     |
|                                 |           | ACK                  |     |
| Beginning Byte N                |           | X Byte               |     |
|                                 |           |                      | ACK |
| ◊                               |           |                      |     |
| ◊                               |           |                      | ◊   |
| ◊                               |           |                      | ◊   |
|                                 |           |                      | ◊   |
| Byte N + X - 1                  |           |                      |     |
|                                 |           | ACK                  |     |
| P                               | stoP bit  |                      |     |

| Index Block Read Operation      |                 |                      |                  |
|---------------------------------|-----------------|----------------------|------------------|
| Controller (Host)               |                 | IDT (Slave/Receiver) |                  |
| T                               | starT bit       |                      |                  |
| Slave Address DC <sub>(h)</sub> |                 |                      |                  |
| WR                              | WRite           |                      |                  |
|                                 |                 | ACK                  |                  |
| Beginning Byte = N              |                 |                      |                  |
|                                 |                 | ACK                  |                  |
| RT                              | Repeat starT    |                      |                  |
| Slave Address DD <sub>(h)</sub> |                 |                      |                  |
| RD                              | ReaD            |                      |                  |
|                                 |                 | ACK                  |                  |
|                                 |                 |                      |                  |
|                                 |                 | Data Byte Count = X  |                  |
| ACK                             |                 |                      |                  |
|                                 |                 | X Byte               | Beginning Byte N |
| ACK                             |                 |                      |                  |
|                                 |                 |                      | ◇                |
| ◇                               |                 |                      | ◇                |
| ◇                               |                 |                      | ◇                |
| ◇                               |                 |                      |                  |
|                                 |                 |                      | Byte N + X - 1   |
| N                               | Not acknowledge |                      |                  |
| P                               | stoP bit        |                      |                  |

Note: Addresses show assumes pin 29 is low.

SMBus Table: Frequency Select Register

| Byte 0 | Pin # | Name        | Control Function                  | Type | 0        | 1      | Default |
|--------|-------|-------------|-----------------------------------|------|----------|--------|---------|
| Bit 7  | -     | HIGH_BW#    | High or Low BW                    | RW   | High BW  | Low BW | Latch   |
| Bit 6  | -     | BYPASS#/PLL | Bypass (non-PLL Mode) or PLL Mode | RW   | Bypass   | PLL    | Latch   |
| Bit 5  | -     | Reserved    | Reserved                          | RW   | Reserved |        | X       |
| Bit 4  | -     | Reserved    | Reserved                          | RW   | Reserved |        | X       |
| Bit 3  | -     | Reserved    | Reserved                          | RW   | Reserved |        | X       |
| Bit 2  | -     | Reserved    | Reserved                          | RW   | Reserved |        | 1       |
| Bit 1  | -     | Reserved    | Reserved                          | RW   | Reserved |        | 0       |
| Bit 0  | -     | Reserved    | Reserved                          | RW   | Reserved |        | 1       |

SMBus Table: Output Control Register

| Byte 1 | Pin # | Name  | Control Function                | Type | 0       | 1      | Default |
|--------|-------|-------|---------------------------------|------|---------|--------|---------|
| Bit 7  | 43,42 | DIF_7 | Output Control (Disable = Hi-Z) | RW   | Disable | Enable | 1       |
| Bit 6  | 38,37 | DIF_6 | Output Control (Disable = Hi-Z) | RW   | Disable | Enable | 1       |
| Bit 5  | 27,28 | DIF_5 | Output Control (Disable = Hi-Z) | RW   | Disable | Enable | 1       |
| Bit 4  | 22,23 | DIF_4 | Output Control (Disable = Hi-Z) | RW   | Disable | Enable | 1       |
| Bit 3  | 19,20 | DIF_3 | Output Control (Disable = Hi-Z) | RW   | Disable | Enable | 1       |
| Bit 2  | 14,15 | DIF_2 | Output Control (Disable = Hi-Z) | RW   | Disable | Enable | 1       |
| Bit 1  | 11,12 | DIF_1 | Output Control (Disable = Hi-Z) | RW   | Disable | Enable | 1       |
| Bit 0  | 6,7   | DIF_0 | Output Control (Disable = Hi-Z) | RW   | Disable | Enable | 1       |

SMBus Table: Output Control Register

| Byte 2 | Pin # | Name     | Control Function                | Type | 0        | 1      | Default |
|--------|-------|----------|---------------------------------|------|----------|--------|---------|
| Bit 7  | -     | Reserved | Reserved                        | RW   | Reserved |        | 0       |
| Bit 6  | -     | Reserved | Reserved                        | RW   | Reserved |        | 0       |
| Bit 5  | -     | Reserved | Reserved                        | RW   | Reserved |        | 0       |
| Bit 4  | -     | Reserved | Reserved                        | RW   | Reserved |        | 0       |
| Bit 3  | 58,59 | DIF_11   | Output Control (Disable = Hi-Z) | RW   | Disable  | Enable | 1       |
| Bit 2  | 53,54 | DIF_10   | Output Control (Disable = Hi-Z) | RW   | Disable  | Enable | 1       |
| Bit 1  | 50,51 | DIF_9    | Output Control (Disable = Hi-Z) | RW   | Disable  | Enable | 1       |
| Bit 0  | 45,46 | DIF_8    | Output Control (Disable = Hi-Z) | RW   | Disable  | Enable | 1       |

SMBus Table: Output Enable Readback

| Byte 3 | Pin # | Name | Control Function | Type | 0       | 1        | Default |
|--------|-------|------|------------------|------|---------|----------|---------|
| Bit 7  | 43,42 | OE7# | OE# Pin Readback | R    | Enabled | Disabled | X       |
| Bit 6  | 38,37 | OE6# | OE# Pin Readback | R    | Enabled | Disabled | X       |
| Bit 5  | 27,28 | OE5# | OE# Pin Readback | R    | Enabled | Disabled | X       |
| Bit 4  | 22,23 | OE4# | OE# Pin Readback | R    | Enabled | Disabled | X       |
| Bit 3  | 19,20 | OE3# | OE# Pin Readback | R    | Enabled | Disabled | X       |
| Bit 2  | 14,15 | OE2# | OE# Pin Readback | R    | Enabled | Disabled | X       |
| Bit 1  | 11,12 | OE1# | OE# Pin Readback | R    | Enabled | Disabled | X       |
| Bit 0  | 6,7   | OE0# | OE# Pin Readback | R    | Enabled | Disabled | X       |

SMBus Table: Output Enable Readback

| Byte 4 | Pin # | Name     | Control Function                | Type | 0        | 1        | Default |
|--------|-------|----------|---------------------------------|------|----------|----------|---------|
| Bit 7  | -     | Reserved | Reserved                        | R    | Reserved |          | 0       |
| Bit 6  | -     | Reserved | Reserved                        | R    | Reserved |          | 0       |
| Bit 5  | -     | Reserved | Reserved                        | R    | Reserved |          | 0       |
| Bit 4  | -     | Reserved | Reserved                        | R    | Reserved |          | 0       |
| Bit 3  | 58,59 | OE11#    | Output Control (Disable = Hi-Z) | R    | Enabled  | Disabled | X       |
| Bit 2  | 53,54 | OE10#    | Output Control (Disable = Hi-Z) | R    | Enabled  | Disabled | X       |
| Bit 1  | 50,51 | OE9#     | Output Control (Disable = Hi-Z) | R    | Enabled  | Disabled | X       |
| Bit 0  | 45,46 | OE8#     | Output Control (Disable = Hi-Z) | R    | Enabled  | Disabled | X       |

Note: For an output to be enabled, BOTH the Output Enable Bit and the OE# pin must be enabled. This means that the Output Enable Bit must be '1' and the corresponding OE# pin must be '0'.

SMBus Table: Vendor &amp; Revision ID Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  | -     | RID3 | REVISION ID      | R    | - | - | 0       |
| Bit 6  | -     | RID2 |                  | R    | - | - | 0       |
| Bit 5  | -     | RID1 |                  | R    | - | - | 1       |
| Bit 4  | -     | RID0 |                  | R    | - | - | 0       |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | - | - | 0       |
| Bit 2  | -     | VID2 |                  | R    | - | - | 0       |
| Bit 1  | -     | VID1 |                  | R    | - | - | 0       |
| Bit 0  | -     | VID0 |                  | R    | - | - | 1       |

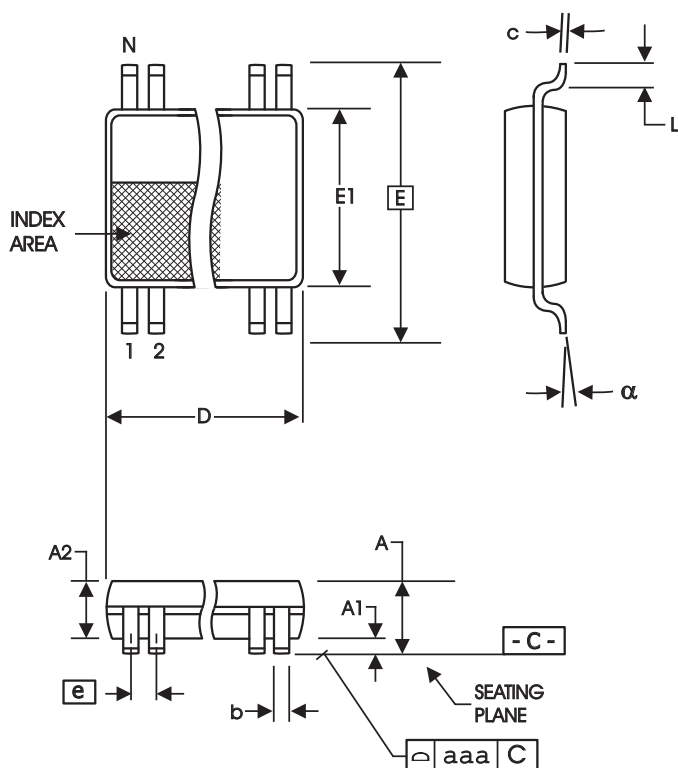
SMBus Table: DEVICE ID

| Byte 6 | Pin # | Name              | Control Function | Type | 0                   | 1 | Default |
|--------|-------|-------------------|------------------|------|---------------------|---|---------|
| Bit 7  | -     | Device ID 7 (MSB) |                  | RW   | Device ID is C0 Hex |   | 1       |
| Bit 6  | -     | Device ID 6       |                  | RW   |                     |   | 1       |
| Bit 5  | -     | Device ID 5       |                  | RW   |                     |   | 0       |
| Bit 4  | -     | Device ID 4       |                  | RW   |                     |   | 0       |
| Bit 3  | -     | Device ID 3       |                  | RW   |                     |   | 0       |
| Bit 2  | -     | Device ID 2       |                  | RW   |                     |   | 0       |
| Bit 1  | -     | Device ID 1       |                  | RW   |                     |   | 0       |
| Bit 0  | -     | Device ID 0       |                  | RW   |                     |   | 0       |

SMBus Table: Byte Count Register

| Byte 7 | Pin # | Name | Control Function                                                      | Type | 0 | 1 | Default |
|--------|-------|------|-----------------------------------------------------------------------|------|---|---|---------|
| Bit 7  | -     | BC7  | Writing to this register configures how many bytes will be read back. | RW   | - | - | 0       |
| Bit 6  | -     | BC6  |                                                                       | RW   | - | - | 0       |
| Bit 5  | -     | BC5  |                                                                       | RW   | - | - | 0       |
| Bit 4  | -     | BC4  |                                                                       | RW   | - | - | 0       |
| Bit 3  | -     | BC3  |                                                                       | RW   | - | - | 0       |
| Bit 2  | -     | BC2  |                                                                       | RW   | - | - | 1       |
| Bit 1  | -     | BC1  |                                                                       | RW   | - | - | 1       |
| Bit 0  | -     | BC0  |                                                                       | RW   | - | - | 1       |

# 9DB1233 Twelve Output Differential Buffer for PCIe Gen3



6.10 mm. Body, 0.50 mm. Pitch TSSOP  
(240 mil) (20 mil)

| SYMBOL | In Millimeters    |      | In Inches         |      |
|--------|-------------------|------|-------------------|------|
|        | COMMON DIMENSIONS |      | COMMON DIMENSIONS |      |
|        | MIN               | MAX  | MIN               | MAX  |
| A      | --                | 1.20 | --                | .047 |
| A1     | 0.05              | 0.15 | .002              | .006 |
| A2     | 0.80              | 1.05 | .032              | .041 |
| b      | 0.17              | 0.27 | .007              | .011 |
| c      | 0.09              | 0.20 | .0035             | .008 |
| D      | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| E      | 8.10 BASIC        |      | 0.319 BASIC       |      |
| E1     | 6.00              | 6.20 | .236              | .244 |
| e      | 0.50 BASIC        |      | 0.020 BASIC       |      |
| L      | 0.45              | 0.75 | .018              | .030 |
| N      | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| alpha  | 0°                | 8°   | 0°                | 8°   |
| aaa    | --                | 0.10 | --                | .004 |

## VARIATIONS

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 64 | 16.90 | 17.10 | .665     | .673 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

| Part / Order Number | Shipping Packaging | Package      | Temperature |
|---------------------|--------------------|--------------|-------------|
| 9DB1233AGLF         | Tubes              | 64-pin TSSOP | 0 to +70°C  |
| 9DB1233AGLFT        | Tape and Reel      | 64-pin TSSOP | 0 to +70°C  |

“LF” after the package code denotes the Pb-Free configuration, RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

## Revision History

| Rev. | Issue Date | Who | Description                                                                                                            | Page # |
|------|------------|-----|------------------------------------------------------------------------------------------------------------------------|--------|
| 0.1  | 7/7/2010   | RDW | Initial Release                                                                                                        | -      |
| A    | 7/12/2010  | RDW | 1. Changed 'PWD' to 'Default' in SMBus<br>2. Updated Electrical Tables<br>3. Move to Final                             | 12,13  |
| B    | 11/4/2010  | RDW | 1. Corrected Additive phase jitter calculation in PCIe phase jitter table<br>2. Added footnotes 5 and 6 to this table. |        |

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