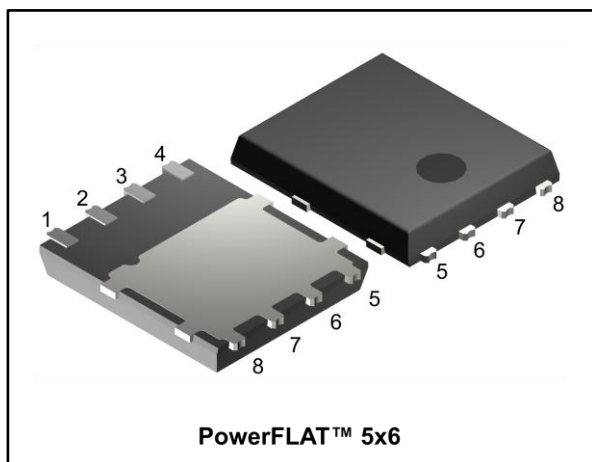


N-channel 100 V, 0.02 Ω typ., 10 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL40N10F7	100 V	0.024 Ω	10 A	5 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Figure 1: Internal schematic diagram

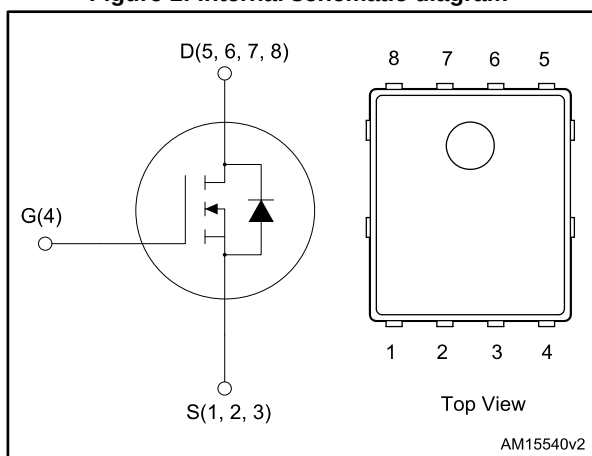


Table 1: Device summary

Order code	Marking	Package	Packing
STL40N10F7	40N10F7	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings.....	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package information	9
	4.1 PowerFLAT 5x6 type R package information	10
	4.2 Packing information.....	12
5	Revision history.....	14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	40	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	28	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	10	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	7	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	40	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	5	W
T_j	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:⁽¹⁾This value is rated according to R_{thj-c} ⁽²⁾This value is rated according to $R_{thj-pcb}$ ⁽³⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	2.08	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	30	$^\circ\text{C/W}$

Notes:⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 4: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\ \text{V}$ $V_{DS} = 100\ \text{V}$			10	μA
		$V_{GS} = 0\ \text{V}$, $V_{DS} = 100\ \text{V}$, $T_C = 125^\circ\text{C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\ \text{V}$, $V_{GS} = +20\ \text{V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	3		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$		0.02	0.024	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0\ \text{V}$	-	1270	-	pF
C_{oss}	Output capacitance		-	290	-	pF
C_{rss}	Reverse transfer capacitance		-	24	-	pF
Q_g	Total gate charge	$V_{DD} = 50\ \text{V}$, $I_D = 32\ \text{A}$, $V_{GS} = 10\ \text{V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	19	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	4.5	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ \text{V}$, $I_D = 16\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (see Figure 13: "Test circuit for resistive load switching times")	-	12	-	ns
t_r	Rise time		-	17.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
t_f	Fall time		-	5.6	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	$I_{SD} = 32\text{ A}$, $V_{GS} = 0\text{ V}$	-		32	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				128	A
$V_{SD}^{(2)}$	Forward on voltage				1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 32\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 80\text{ V}$, $T_J = 150^\circ\text{ C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	41		ns
Q_{rr}	Reverse recovery charge		-	47		nC
I_{RRM}	Reverse recovery current		-	2.3		A

Notes:

⁽¹⁾Pulse width limited by safe operating area

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

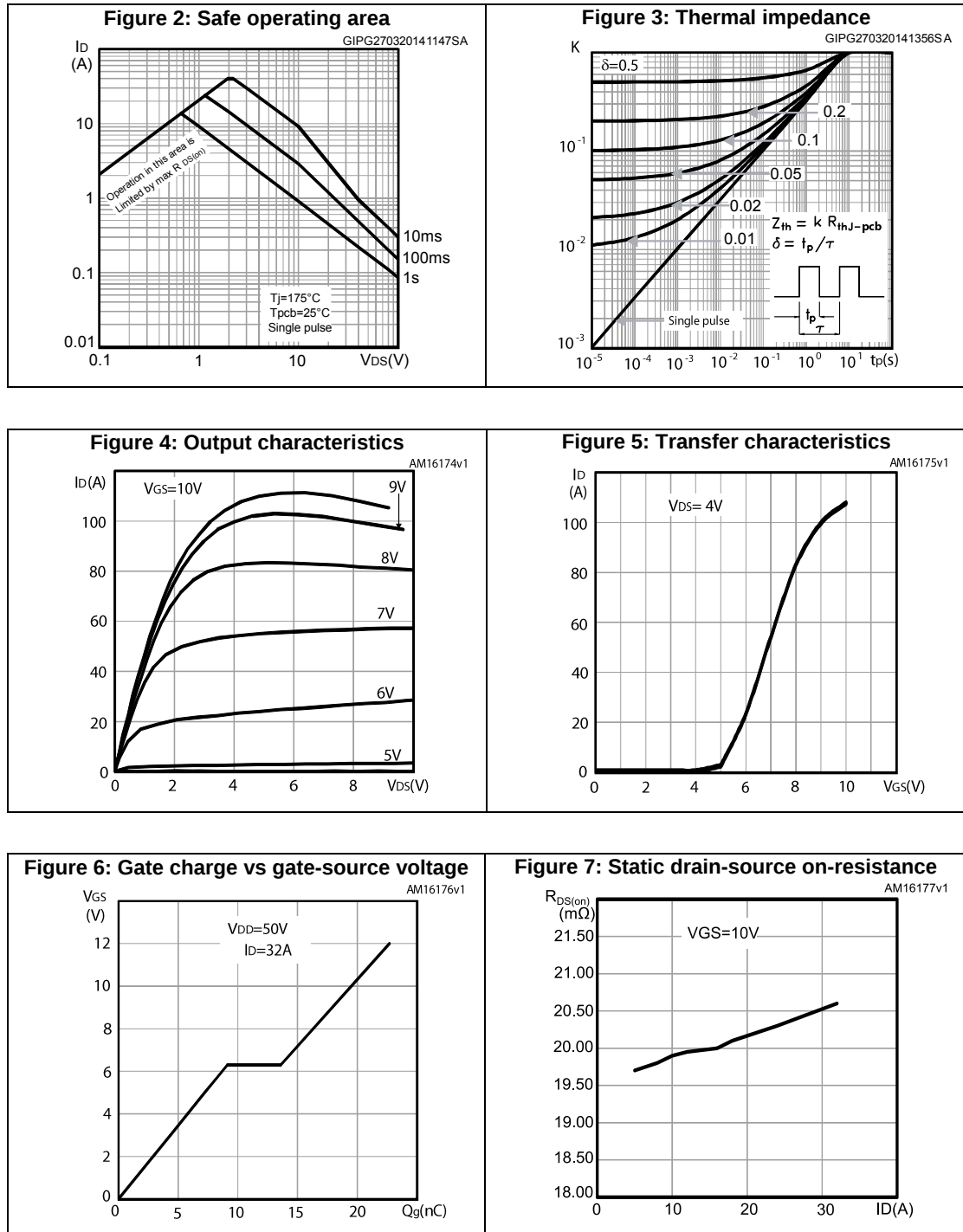


Figure 8: Capacitance variations

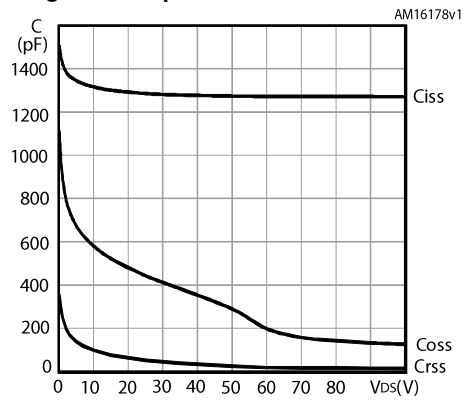


Figure 9: Normalized gate threshold voltage vs temperature

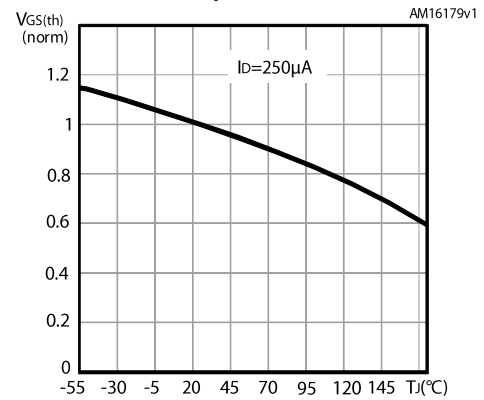


Figure 10: Normalized on-resistance vs temperature

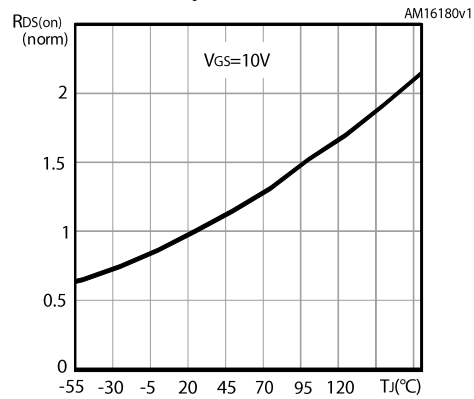


Figure 11: Normalized V(BR)DSS vs temperature

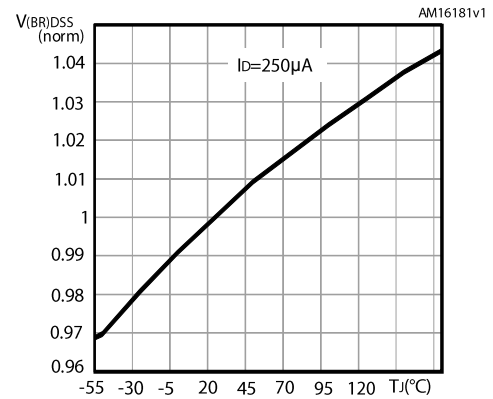
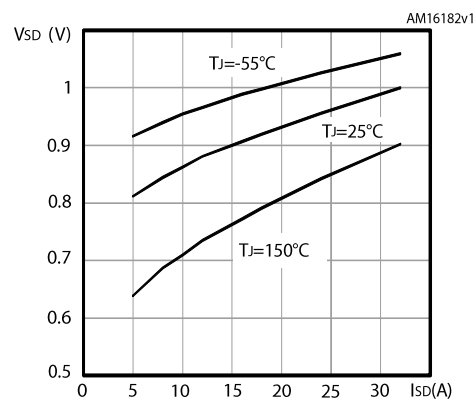
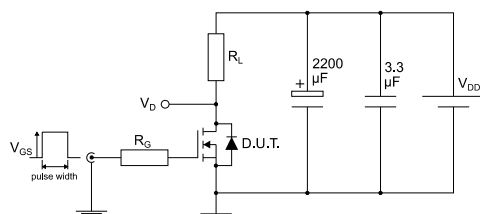


Figure 12: Source-drain diode forward characteristics



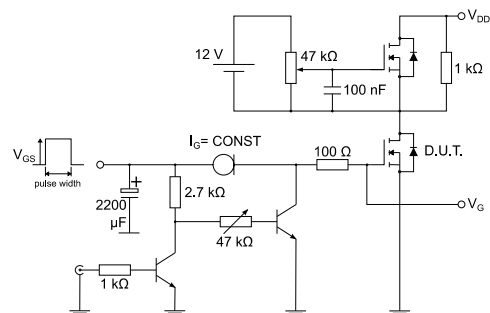
3 Test circuits

Figure 13: Test circuit for resistive load switching times



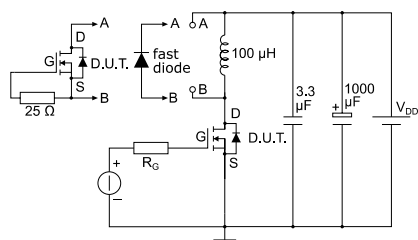
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Figure 14: Test circuit for gate charge behavior



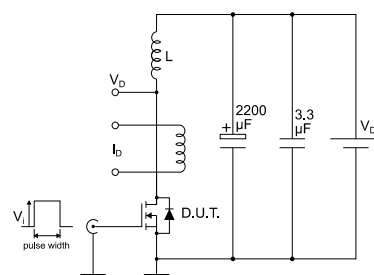
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Figure 15: Test circuit for inductive load switching and diode recovery times



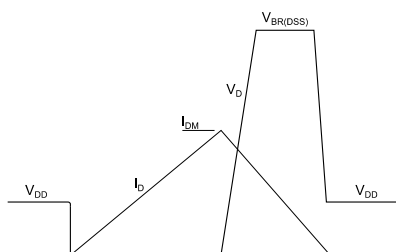
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Figure 16: Unclamped inductive load test circuit



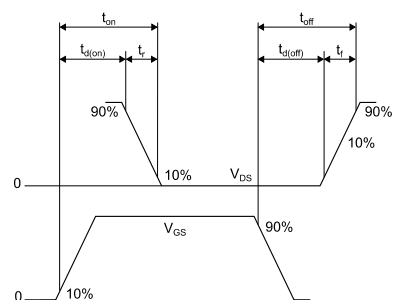
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT 5x6 type R package information

Figure 19: PowerFLAT™ 5x6 type R package outline

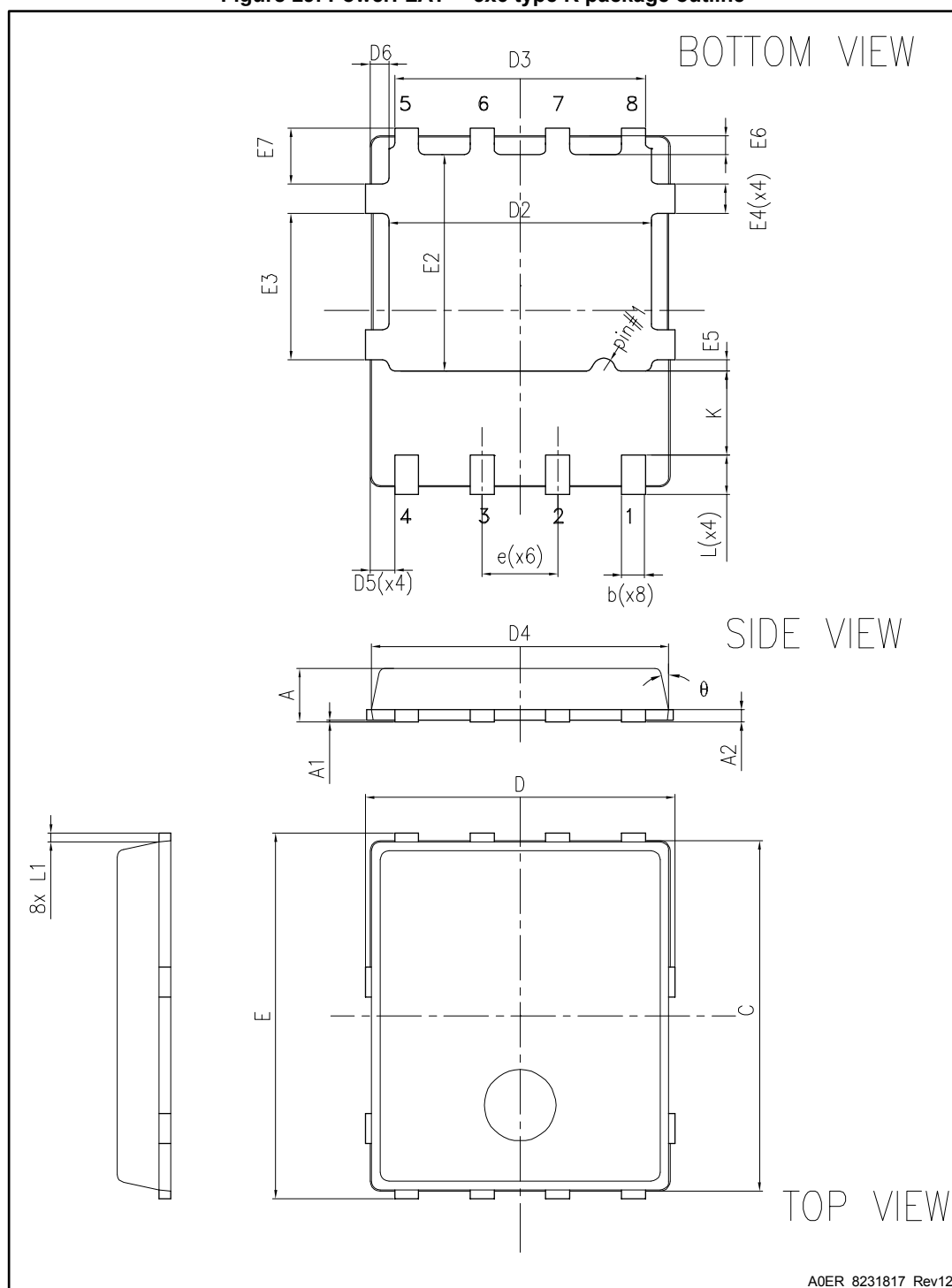
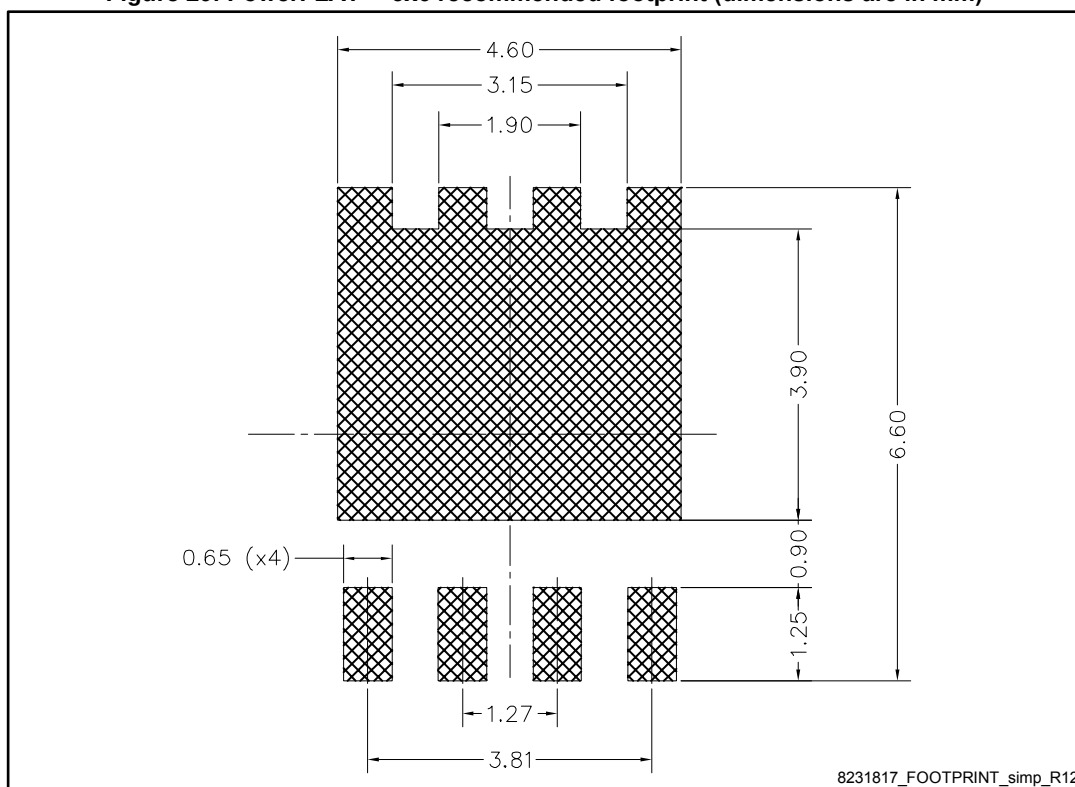


Table 8: PowerFLAT™ 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.2	0.325	0.450
E7	0.75	0.90	1.25
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

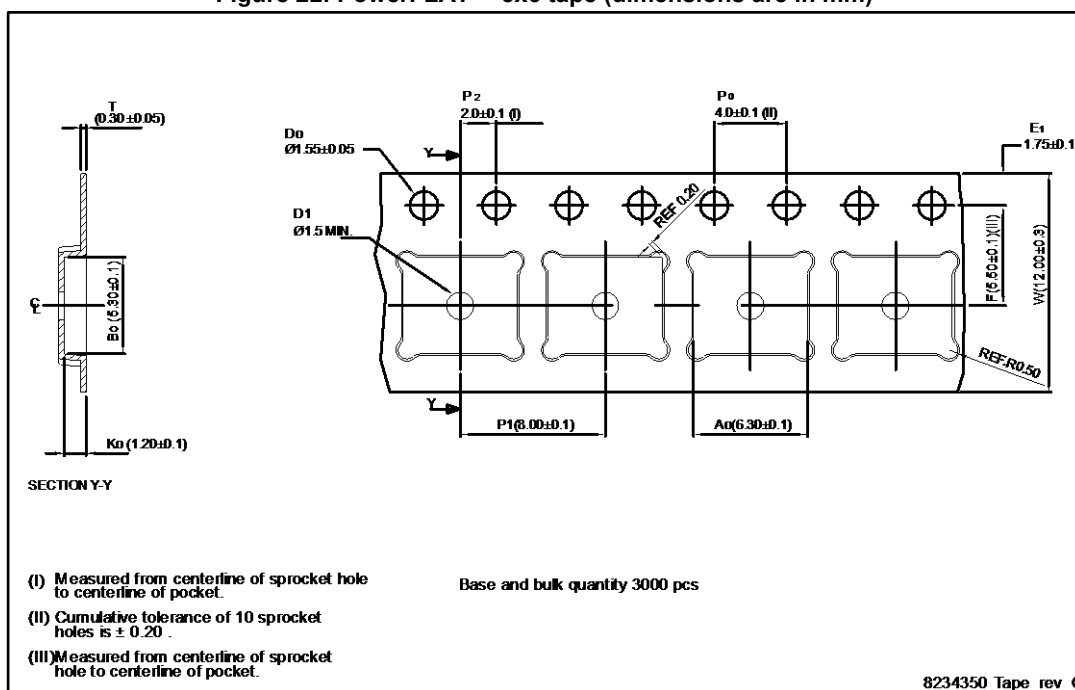


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

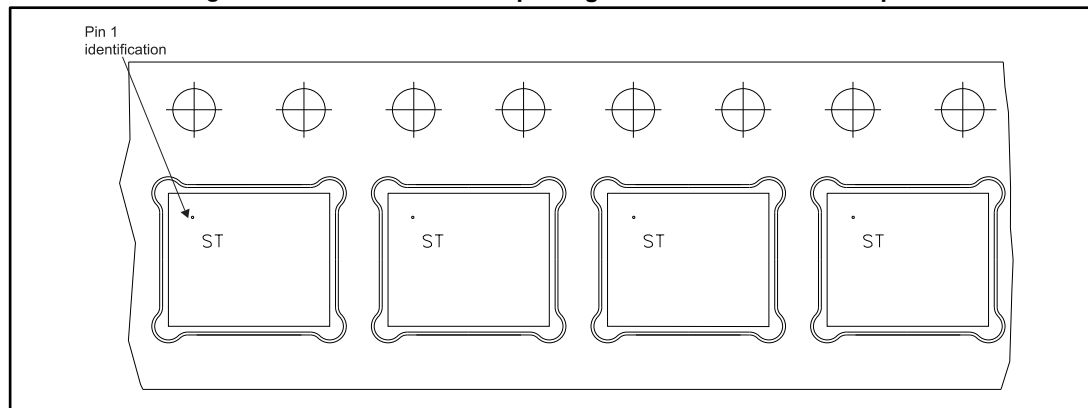
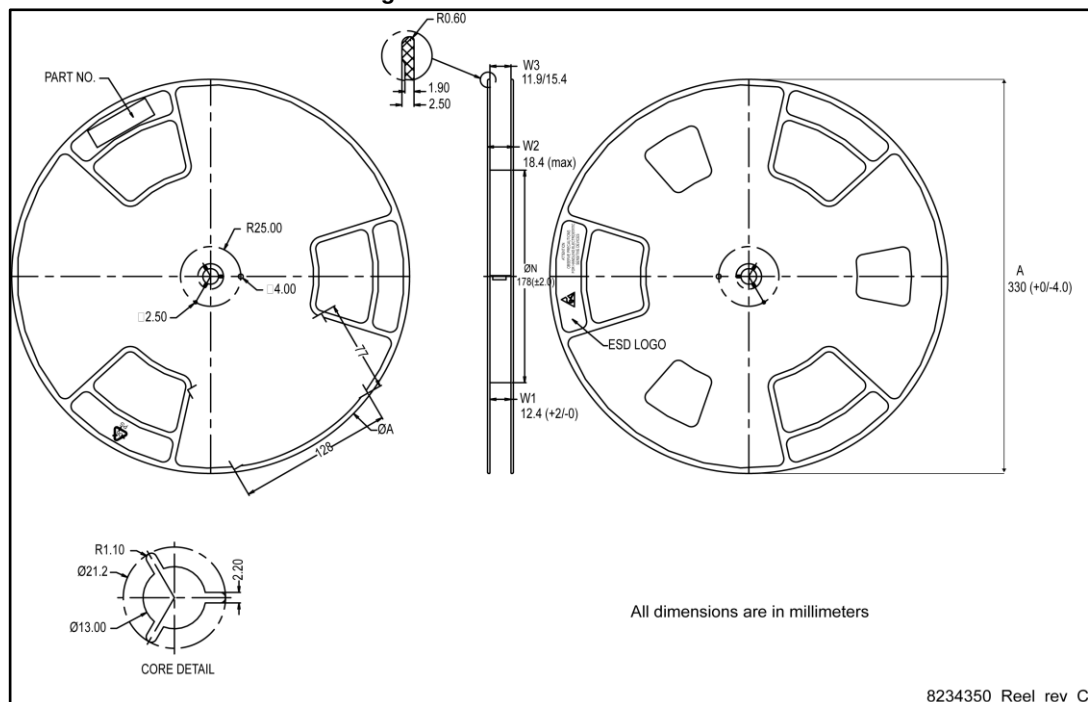


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
20-May-2015	1	First release.
02-Nov-2015	2	Document status promoted from preliminary to production data. Modified: $V_{GS(th)}$ values in tab 4. Updated the entire typical values in tab 5, tab 6 and tab 7 Added Electrical characteristics (curves) Updated Figure 13, 14, 15 and 16 Minor text changes.
18-Dec-2015	3	Updated title, features and description. Updated Table 2: "Absolute maximum ratings" and Table 4: "On/Off states" . Minor text changes.
01-Feb 2016	4	Updated Table 5: "Dynamic" Minor text changes.

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