# 74HC595; 74HCT595

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Rev. 9 — 28 February 2017

Product data sheet

### 1 General description

The 74HC595; 74HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset  $\overline{\text{MR}}$  input. A LOW on  $\overline{\text{MR}}$  will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ( $\overline{\text{OE}}$ ) is LOW. A HIGH on  $\overline{\text{OE}}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{\text{OE}}$  input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{\text{CC}}$ .

#### 2 Features and benefits

- · 8-bit serial input
- · 8-bit serial or parallel output
- · Storage register with 3-state outputs
- · Shift register with direct clear
- 100 MHz (typical) shift out frequency
- Complies with JEDEC standard no. 7A
- · Input levels:
  - For 74HC595: CMOS level
  - For 74HCT595: TTL level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3 Applications

- Serial-to-parallel data conversion
- · Remote control holding register

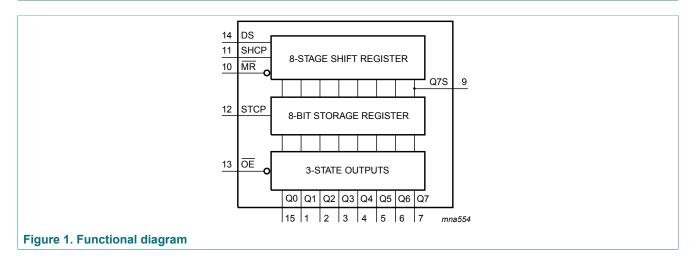


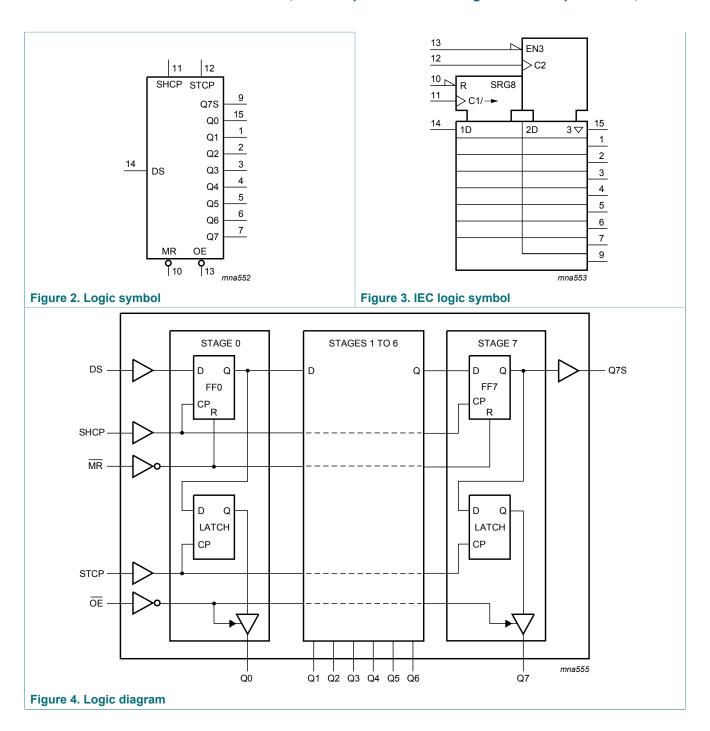
## 4 Ordering information

**Table 1. Ordering information** 

Type number	Package										
	Temperature range	Name	Description	Version							
74HC595D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1							
74HCT595D			body width 3.9 mm								
74HC595DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads;	SOT338-1							
74HCT595DB			body width 5.3 mm								
74HC595PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads;	SOT403-1							
74HCT595PW			body width 4.4 mm								
74HC595BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced	SOT763-1							
74HCT595BQ			very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm								

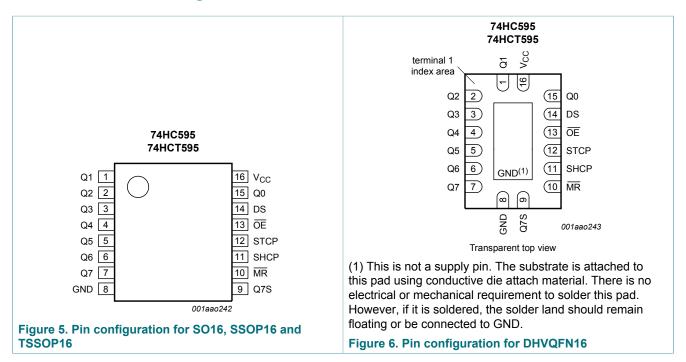
## 5 Functional diagram





## 6 Pinning information

#### 6.1 Pinning



#### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
ŌĒ	13	output enable input (active LOW)
DS	14	serial data input
Q0	15	parallel data output 0
V <sub>CC</sub>	16	supply voltage

## 7 Functional description

Table 3. Function table [1]

Contro	ol			Input	Outpu	ut	Function
SHCP	STCP	OE	MR	DS	Q7S	Qn	
X	X	L	L	Х	L	NC	a LOW-level on MR only affects the shift registers
X	1	L	L	Х	L	L	empty shift register loaded into storage register
X	X	Н	L	Х	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
1	X	L	Н	Н	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	1	L	Н	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
1	1	L	Н	Х	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

[1] H = HIGH voltage state;

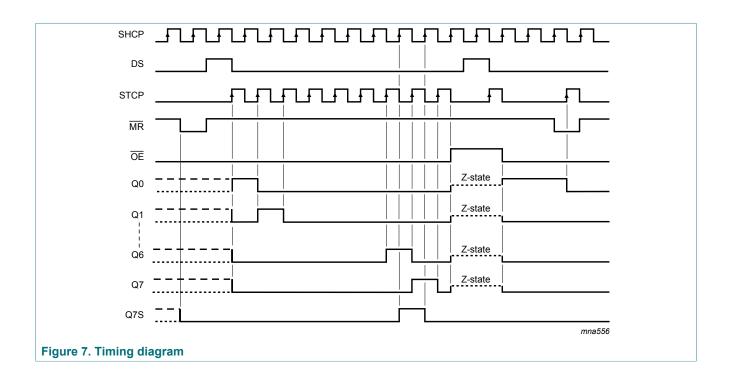
L = LOW voltage state;

↑ = LOW-to-HIGH transition;

X = don't care;

NC = no change;

Z = high-impedance OFF-state.



## **Limiting values**

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O}$ < -0.5 V or $V_{O}$ > $V_{CC}$ + 0.5 V	-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$			
		pin Q7S	-	±25	mA
		pins Qn	-	±35	mA
I <sub>CC</sub>	supply current		-	70	mA
I <sub>GND</sub>	ground current		-70	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	SO16 package [1]	-	500	mW
		SSOP16 package [2]	-	500	mW
		TSSOP16 package [2]	-	500	mW
		DHVQFN16 package [3]	-	500	mW

- For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C. For SSOP16 and TSSOP16 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C. For DHVQFN16 package:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## **Recommended operating conditions**

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	7	74HC595			74HCT595			
			Min	Тур	Max	Min	Тур	Max		
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V	
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V	
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V	
Δt/ΔV	input transition rise and	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V	
	fall rate	V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V	
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V	
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C	

#### 10 Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	o +125 °C	Uni
			Min	Тур	Max	Min	Max	
74HC595					1	1		
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$						
	output voltage	all outputs						
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	V
		Q7S output						
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V	3.84	4.32	-	3.7	-	V
		$I_{O}$ = -5.2 mA; $V_{CC}$ = 6.0 V	5.34	5.81	-	5.2	-	V
		Qn bus driver outputs						
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 4.5 V	3.84	4.32	-	3.7	-	V
		$I_{O}$ = -7.8 mA; $V_{CC}$ = 6.0 V	5.34	5.81	-	5.2	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$						
	output voltage	all outputs						
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	V
		Q7S output						
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.33	-	0.4	V
		Qn bus driver outputs						
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.33	-	0.4	V
		I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±1.0	-	±1.0	μA
l <sub>oz</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 6.0 \text{ V}$ ; $V_O = V_{CC}$ or GND	-	-	±5.0	-	±10	μA

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Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	80	-	160	μA
Cı	input capacitance		-	3.5	-	-	-	pF
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V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$						
	output voltage	all outputs						
		$I_O = -20 \mu A$ Q7S output	4.4	4.5	-	4.4	-	V
		I <sub>O</sub> = -4 mA	3.84	4.32	-	3.7	-	V
		Qn bus driver outputs						
		I <sub>O</sub> = -6 mA	3.7	4.32	-	3.7	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$						
	output voltage	all outputs						
		Ι <sub>Ο</sub> = 20 μΑ	-	0	0.1	-	0.1	V
		Q7S output						
		I <sub>O</sub> = 4.0 mA	-	0.15	0.33	-	0.4	V
		Qn bus driver outputs						
		I <sub>O</sub> = 6.0 mA	-	0.16	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	-	±1.0	μΑ
I <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	±5.0	-	±10	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0$ A; $V_I = V_{CC} - 2.1$ V; $V_{CC} = 4.5$ V to 5.5 V						
		pins MR, SHCP, STCP, OE	-	150	675	-	735	μΑ
		pin DS	-	25	113	-	123	μA
Cı	input capacitance		-	3.5	-	-	-	pF

## 11 Dynamic characteristics

#### **Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74HC595										
t <sub>pd</sub>	propagation	SHCP to Q7S; see Figure 8 [2]								
	delay	V <sub>CC</sub> = 2 V	-	52	160	-	200	-	240	ns
		V <sub>CC</sub> = 4.5 V	-	19	32	-	40	-	48	ns
		V <sub>CC</sub> = 6 V	-	15	27	-	34	_	41	ns
		STCP to Qn; see Figure 9 [2]								
		V <sub>CC</sub> = 2 V	-	55	175	-	220	-	265	ns
		V <sub>CC</sub> = 4.5 V	-	20	35	-	44	-	53	ns
		V <sub>CC</sub> = 6 V	-	16	30	-	37	-	45	ns
t <sub>PHL</sub>	HIGH	MR to Q7S; see Figure 11								
	to LOW propagation	V <sub>CC</sub> = 2 V	-	47	175	-	220	-	265	ns
	delay	V <sub>CC</sub> = 4.5 V	-	17	35	-	44	-	53	ns
		V <sub>CC</sub> = 6 V	-	14	30	-	37	-	45	ns
t <sub>en</sub>	enable time	OE to Qn; see Figure 12 [3]								
		V <sub>CC</sub> = 2 V	-	47	150	-	190	-	225	ns
		V <sub>CC</sub> = 4.5 V	-	17	30	-	38	-	45	ns
		V <sub>CC</sub> = 6 V	-	14	26	-	33	-	38	ns
t <sub>dis</sub>	disable time	OE to Qn; see Figure 12 [4]								
		V <sub>CC</sub> = 2 V	-	41	150	-	190	-	225	ns
		V <sub>CC</sub> = 4.5 V	-	15	30	-	38	-	45	ns
		V <sub>CC</sub> = 6 V	-	12	27	-	33	-	38	ns
t <sub>W</sub>	pulse width	SHCP HIGH or LOW; see Figure 8								
		V <sub>CC</sub> = 2 V	75	17	-	95	-	110	-	ns
		V <sub>CC</sub> = 4.5 V	15	6	-	19	-	22	-	ns
		V <sub>CC</sub> = 6 V	13	5	-	16	-	19	-	ns
		STCP HIGH or LOW; see Figure 9								
		V <sub>CC</sub> = 2 V	75	11	-	95	-	110	-	ns
		V <sub>CC</sub> = 4.5 V	15	4	-	19	-	22	-	ns
		V <sub>CC</sub> = 6 V	13	3	-	16	-	19	-	ns
		MR LOW; see Figure 11								

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Symbol	Parameter	Conditions			25 °C		-40 °C to +85 °C			°C to 5 °C	Unit
				Min	Typ [1]	Max	Min	Max	Min	Max	
		V <sub>CC</sub> = 2 V		75	17	-	95	-	110	-	ns
		V <sub>CC</sub> = 4.5 V		15	6	-	19	-	22	-	ns
		V <sub>CC</sub> = 6 V		13	5	-	16	-	19	-	ns
t <sub>su</sub>	set-up time	DS to SHCP; see Figure 10									
		V <sub>CC</sub> = 2 V		50	11	-	65	-	75	-	ns
		V <sub>CC</sub> = 4.5 V		10	4	-	13	-	15	-	ns
		V <sub>CC</sub> = 6 V		9	3	-	11	-	13	-	ns
		SHCP to STCP; see Figure 10									
		V <sub>CC</sub> = 2 V		75	22	-	95	-	110	-	ns
		V <sub>CC</sub> = 4.5 V		15	8	-	19	-	22	-	ns
		V <sub>CC</sub> = 6 V		13	7	-	16	-	19	-	ns
t <sub>h</sub>	hold time	DS to SHCP; see Figure 10									
		V <sub>CC</sub> = 2 V		3	-6	-	3	-	3	-	ns
		V <sub>CC</sub> = 4.5 V		3	-2	-	3	-	3	-	ns
		V <sub>CC</sub> = 6 V		3	-2	-	3	-	3	-	ns
t <sub>rec</sub>	recovery	MR to SHCP; see Figure 11									
	time	V <sub>CC</sub> = 2 V		50	-19	-	65	-	75	-	ns
		V <sub>CC</sub> = 4.5 V		10	-7	-	13	-	15	-	ns
		V <sub>CC</sub> = 6 V		9	-6	-	11	-	13	-	ns
f <sub>max</sub>	maximum frequency	SHCP or STCP; see Figure 8 and Figure 9									
		V <sub>CC</sub> = 2 V		9	30	-	4.8	-	4	-	MHz
		V <sub>CC</sub> = 4.5 V		30	91	-	24	-	20	-	MHz
		V <sub>CC</sub> = 6 V		35	108	-	28	-	24	-	MHz
C <sub>PD</sub>	power dissipation capacitance	$f_i = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$	5] [6]	-	115	-	-	-	-	-	pF
74HCT59	5; V <sub>CC</sub> = 4.5 \	/ to 5.5 V	,						·	<u> </u>	_
t <sub>pd</sub>	propagation	SHCP to Q7S; see Figure 8	[2]	-	25	42	-	53	-	63	ns
	delay	STCP to Qn; see Figure 9	[2]	-	24	40	-	50	-	60	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to Q7S; see Figure 11		-	23	40	-	50	-	60	ns
t <sub>en</sub>	enable time	OE to Qn; see Figure 12	[3]	-	21	35	-	44	-	53	ns
t <sub>dis</sub>	disable time	OE to Qn; see Figure 12	[4]	-	18	30	-	38	-	45	ns

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Symbol	Parameter Conditions			25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	Min	Max	
t <sub>W</sub>	pulse width	SHCP HIGH or LOW; see Figure 8		16	6	-	20	-	24	-	ns
		STCP HIGH or LOW; see Figure 9		16	5	-	20	-	24	-	ns
		MR LOW; see Figure 11		20	8	-	25	-	30	-	ns
t <sub>su</sub>	set-up time	DS to SHCP; see Figure 9		16	5	-	20	-	24	-	ns
		SHCP to STCP; see Figure 9		16	8	-	20	-	24	-	ns
t <sub>h</sub>	hold time	DS to SHCP; see Figure 10		3	-2	-	3	-	3	-	ns
t <sub>rec</sub>	recovery time	MR to SHCP; see Figure 11		10	-7	-	13	-	15	-	ns
f <sub>max</sub>	maximum frequency	SHCP and STCP; see Figure 8 and Figure 9		30	52	-	24	-	20	-	MHz
C <sub>PD</sub>	power dissipation capacitance	$f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ - 1.5 V	[5] [6]	-	130	-	-	-	-	-	pF

- Typical values are measured at nominal supply voltage.
- $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ . [2] [3]
- $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

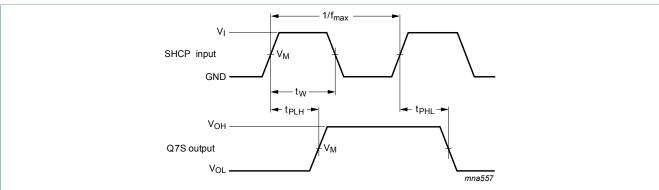
 $f_0$  = output frequency in MHz;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of outputs;

C<sub>1</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V. All 9 outputs switching.

#### 11.1 Waveforms and test circuit



Measurement points are given in Table 8.

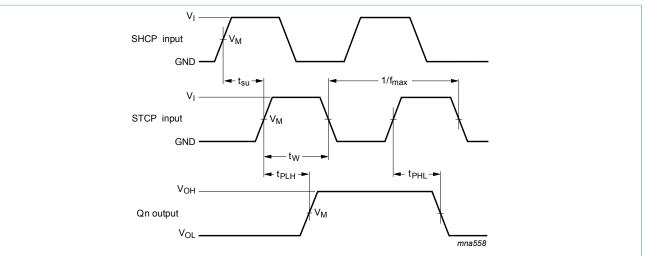
V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

Figure 8. Shift clock pulse, maximum frequency and input to output propagation delays

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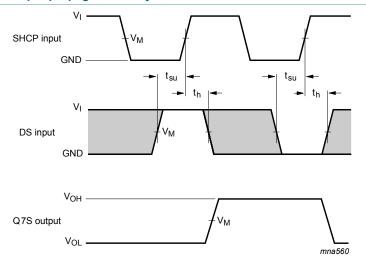
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Measurement points are given in Table 8.

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical output voltage levels that occur with the output load.

Figure 9. Storage clock to output propagation delays

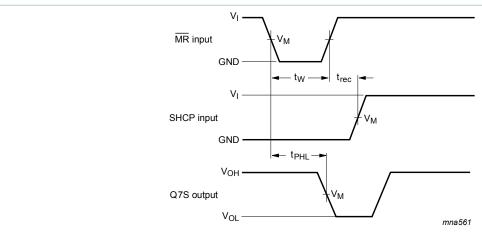


Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical output voltage levels that occur with the output load.

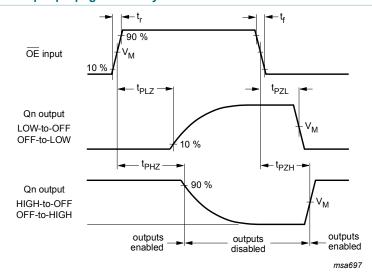
Figure 10. Data set-up and hold times



Measurement points are given in Table 8.

 $\ensuremath{V_{\text{OL}}}$  and  $\ensuremath{V_{\text{OH}}}$  are typical output voltage levels that occur with the output load.

Figure 11. Master reset to output propagation delays



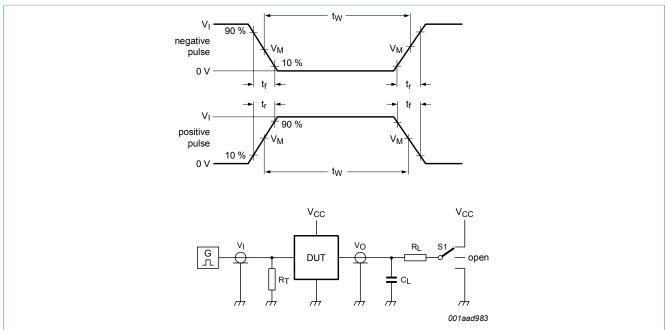
Measurement points are given in Table 8.

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical output voltage levels that occur with the output load.

Figure 12. Enable and disable times

**Table 8. Measurement points** 

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74HC595	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74HCT595	1.3 V	1.3 V



Test data is given in Table 9.

Definitions for test circuit:

C<sub>L</sub> = load capacitance including jig and probe capacitance.

R<sub>L</sub> = load resistance.

 $R_T$  = termination resistance should be equal to the output impedance  $Z_0$  of the pulse generator.

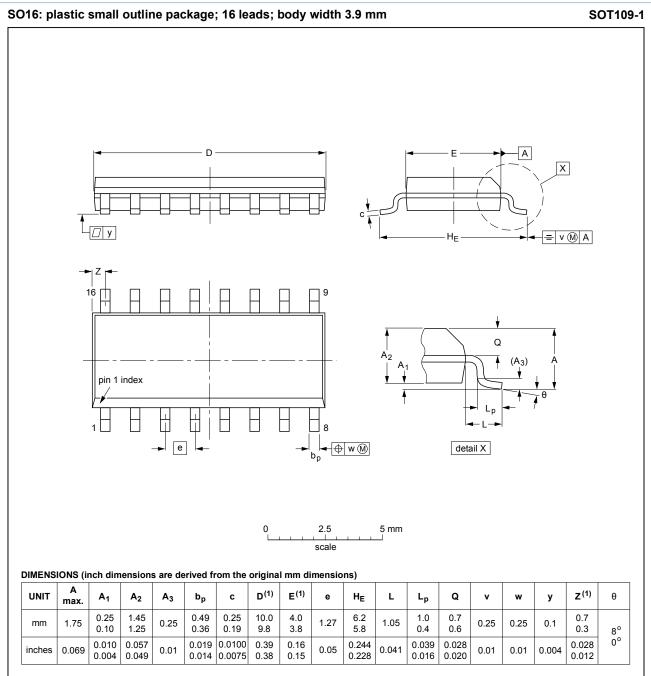
S1 = test selection switch.

Figure 13. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load		S1 position		
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
74HC595	V <sub>CC</sub>	6 ns	50 pF	1 kΩ	open	GND	V <sub>CC</sub>
74HCT595	3 V	6 ns	50 pF	1 kΩ	open	GND	V <sub>CC</sub>

## 12 Package outline



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	155UE DATE
SOT109-1	076E07	MS-012				<del>99-12-27</del> 03-02-19

Figure 14. Package outline SOT109-1 (SO16)

74HC\_HCT595

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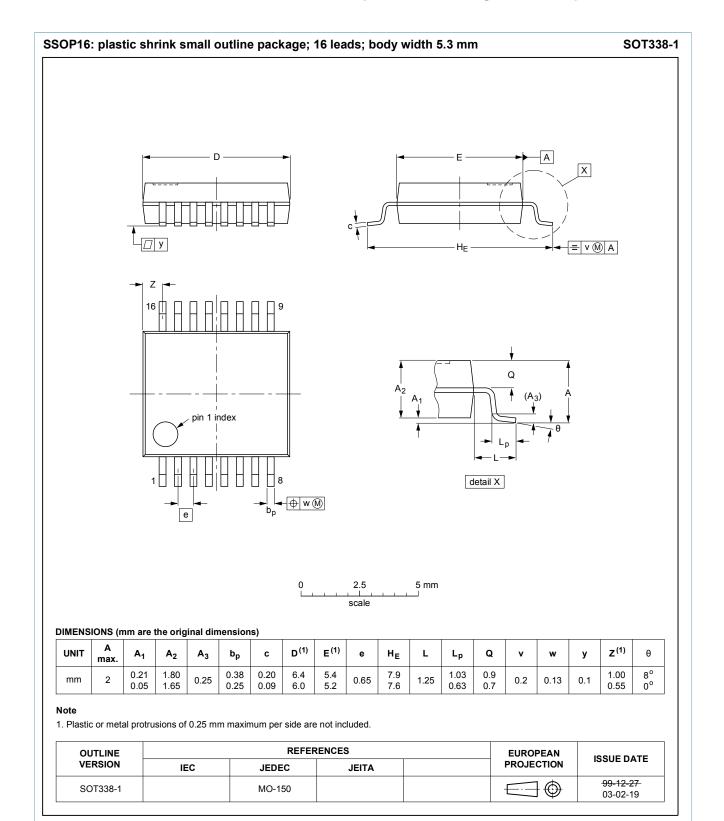
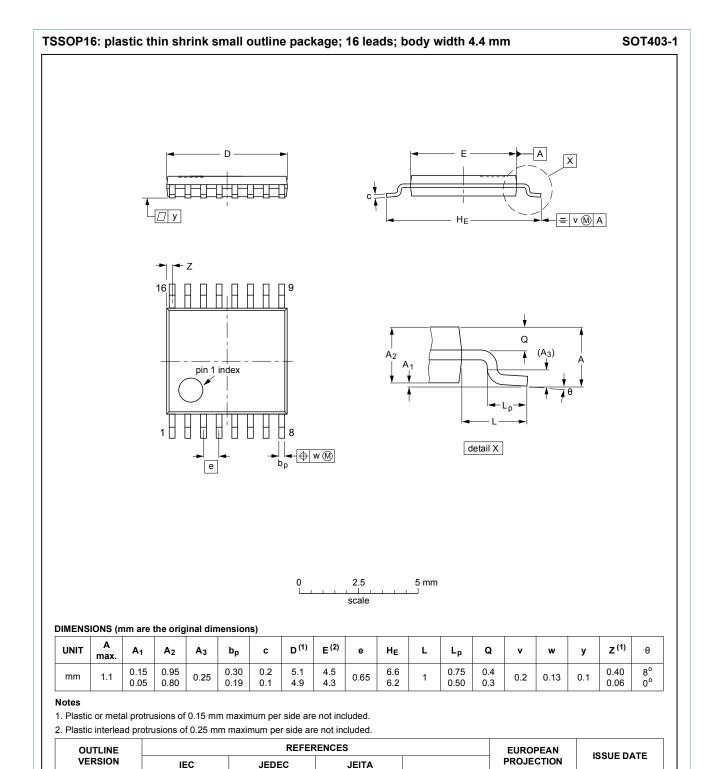


Figure 15. Package outline SOT338-1 (SSOP16)



#### Figure 16. Package outline SOT403-1 (TSSOP16)

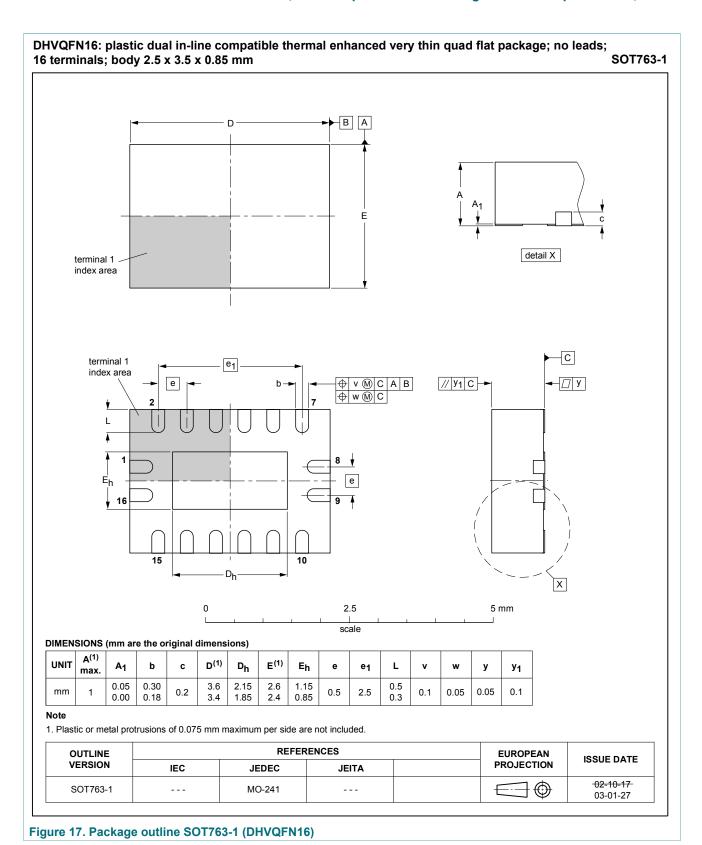
MO-153

99-12-27

03-02-18

 $\square$ 

SOT403-1



74HC\_HCT595

### 13 Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14 Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT595 v.9	20170228	Product data sheet	-	74HC_HCT595 v.8	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>				
74HC_HCT595 v.8	20160225	Product data sheet	-	74HC_HCT595 v.7	
Modifications:	Type numbers 74HC595N and 74HCT595N (SOT38-4) removed.				
74HC_HCT595 v.7	20150126	Product data sheet	-	74HC_HCT595 v.6	
Modifications:	Table 7: Power dissipation capacitance condition for 74HCT595 is corrected.				
74HC_HCT595 v.6	20111212	Product data sheet	-	74HC_HCT595 v.5	
Modifications:	Legal pages updated.				
74HC_HCT595 v.5	20110628	Product data sheet	-	74HC_HCT595 v.4	
74HC_HCT595 v.4	20030604	Product specification	-	74HC_HCT595_CNV v.3	
74HC_HCT595_CNV v.3	19980604	Product specification	-	-	

### 15 Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- The term 'short data sheet' is explained in section "Definitions". [2] [3]
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