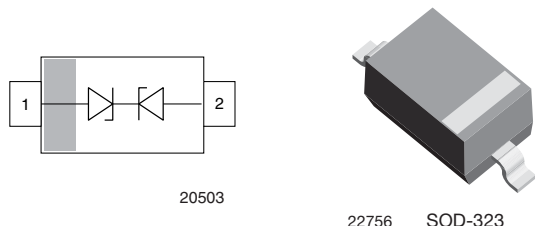


# Low Capacitance, Single-Line ESD-Protection Diode in SOD-323



## FEATURES

- For LIN-Bus applications
- Small SOD-323 package
- Working range: -16 V; +26.5 V
- Low leakage current  $I_R < 0.05 \mu A$
- Low load capacitance  $C_D < 18 \text{ pF}$
- ESD-protection acc. IEC 61000-4-2  
± 30 kV contact discharge  
± 30 kV air discharge
- ESD capability according to AEC-Q101:  
human body model: class H3B: > 8 kV
- e3 - pins plated with tin (Sn)
- 1-line ESD-protection
- AEC-Q101 qualified available
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

## MARKING (example only)



XYZ = type code (see table below)  
bar = pin 1

## ORDERING INFORMATION

PART NUMBER (EXAMPLE)	ENVIRONMENTAL AND QUALITY CODE				PACKAGING CODE		ORDERING CODE (EXAMPLE)
	AEC-Q101 QUALIFIED	RoHS-COMPLIANT + LEAD (Pb)-FREE TERMINATIONS		TIN PLATED	3K PER 7" REEL (8 mm TAPE) 15K/BOX = MOQ	10K PER 13" REEL (8 mm TAPE) 10K/BOX = MOQ	
		STANDARD	GREEN				
VLIN1626-02G	-	E	-	3	-08	-	VLIN1626-02G-E3-08
VLIN1626-02G	H	E	-	3	-08	-	VLIN1626-02GHE3-08
VLIN1626-02G	-	E	-	3	-	-18	VLIN1626-02G-E3-18
VLIN1626-02G	H	E	-	3	-	-18	VLIN1626-02GHE3-18

## PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VLIN1626-02G	SOD-323	6A1	4.30 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Pin 1 to pin 2; $T_A = 25^\circ C$ , acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single	$I_{PPM}$	6	A
	Pin 2 to pin 1; $T_A = 25^\circ C$ , acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single		4	
Peak pulse power	$T_A = 25^\circ C$ , acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	$P_{PP}$	200	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses, $T_A = 25^\circ C$	$V_{ESD}$	± 30	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses, $T_A = 25^\circ C$		± 30	
Operating temperature	Junction temperature	$T_J$	-55 to +150	°C
Storage temperature		$T_{STG}$	-55 to +150	

<b>ELECTRICAL CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	TEST CONDITIONS / REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Pin 1 to pin 2; max. reverse working voltage	$V_{RWM}$	-	-	16	V
	Pin 2 to pin 1; max. reverse working voltage		-	-	26.5	
Reverse voltage	Pin 1 to pin 2; at $I_R = 0.05\text{ }\mu\text{A}$	$V_R$	16	-	-	V
	Pin 2 to pin 1; at $I_R = 0.05\text{ }\mu\text{A}$		26.5	-	-	
Reverse current	Pin 1 to pin 2; at $V_{RWM} = 16\text{ V}$	$I_R$	-	-	0.05	$\mu\text{A}$
	Pin 2 to pin 1; at $V_{RWM} = 26.5\text{ V}$		-	-	0.05	
Reverse breakdown voltage	Pin 1 to pin 2; at $I_R = 1\text{ mA}$	$V_{BR}$	17.1	18.7	20.3	V
	Pin 2 to pin 1; at $I_R = 1\text{ mA}$		28	30	32	
Reverse clamping voltage	Pin 1 to pin 2; at $I_{PP} = 1\text{ A}$ ; $t_p = 8/20\text{ }\mu\text{s}$	$V_C$	-	22	25	V
	Pin 1 to pin 2; at $I_{PP} = 6\text{ A}$ ; $t_p = 8/20\text{ }\mu\text{s}$		-	29	33	
	Pin 2 to pin 1; at $I_{PP} = 1\text{ A}$ ; $t_p = 8/20\text{ }\mu\text{s}$		-	32	40	
	Pin 2 to pin 1; at $I_{PP} = 4\text{ A}$ ; $t_p = 8/20\text{ }\mu\text{s}$		-	39	50	
Capacitance	At $V_R = 0\text{ V}$ , $f = 1\text{ MHz}$	$C_D$	-	15.5	18	pF

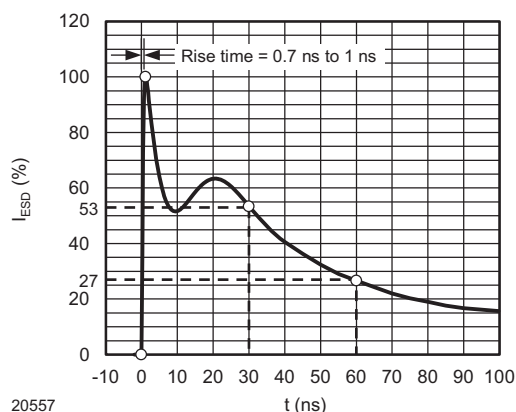
**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)


Fig. 1 - ESD Discharge Current Wave Form  
acc. IEC 61000-4-2 (330  $\Omega$  / 150 pF)

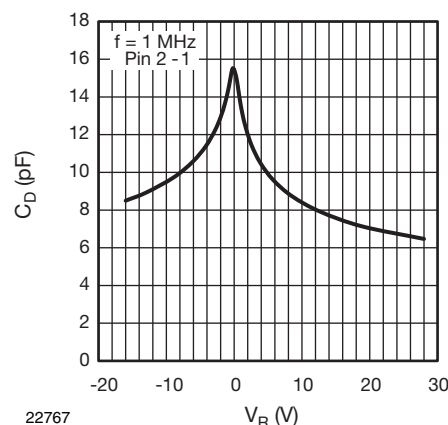


Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$

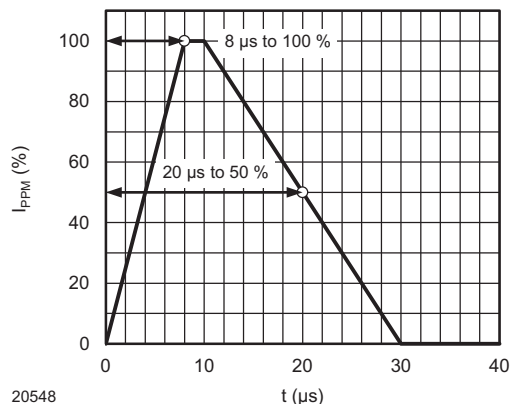


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form  
acc. IEC 61000-4-5

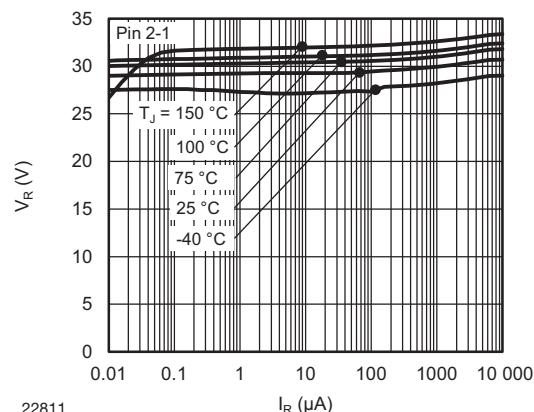


Fig. 4 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$

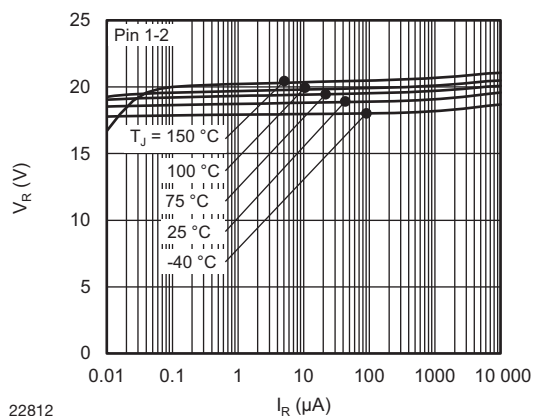


Fig. 5 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$

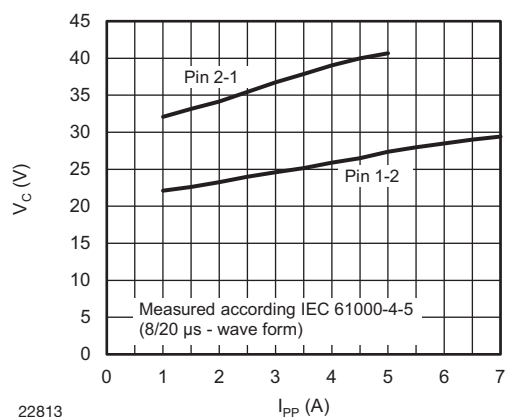


Fig. 6 - Typical Peak Clamping Voltage  $V_C$  vs. Peak Pulse Current  $I_{PP}$

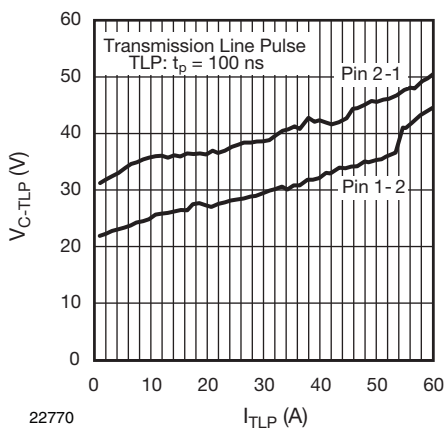
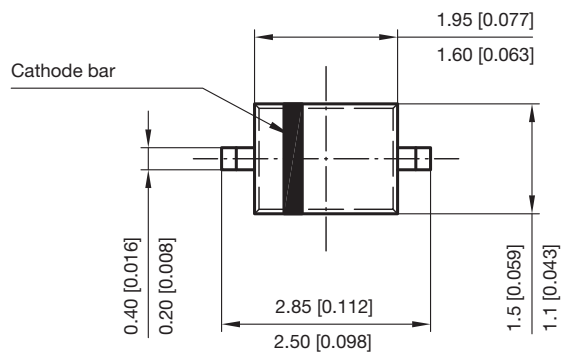
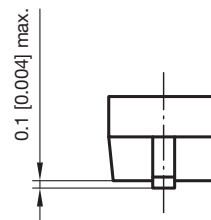
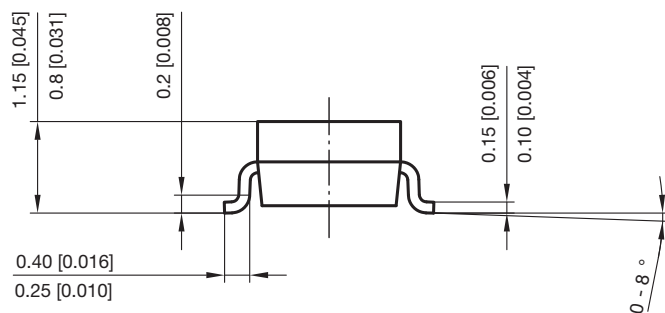


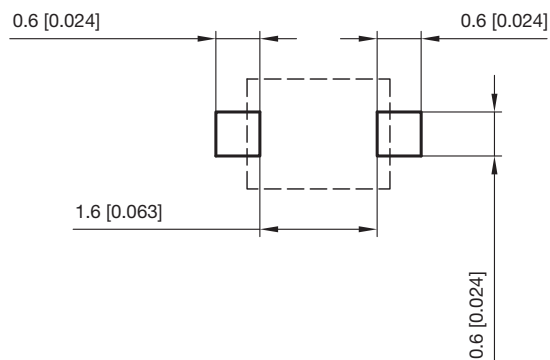
Fig. 7 - Typical Clamping Voltage  $V_{C-TLP}$  vs. Pulse Current  $I_{TLP}$



**PACKAGE DIMENSIONS** in millimeters (inches) **SOD-323**



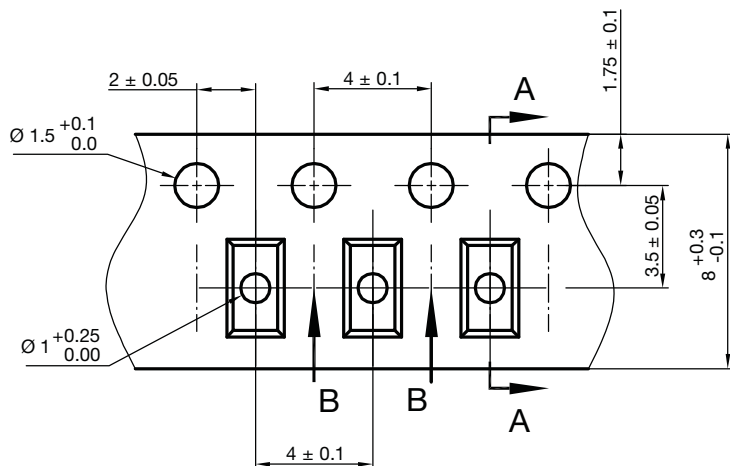
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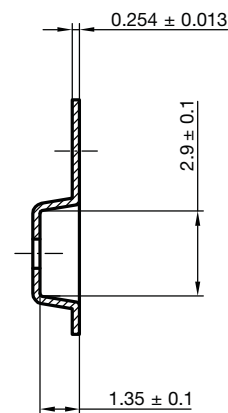
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Rev. 5 - Date: 23.Sept.2009  
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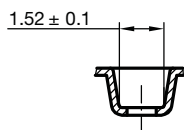
## CARRIER TAPE SOD-323



A-A Section

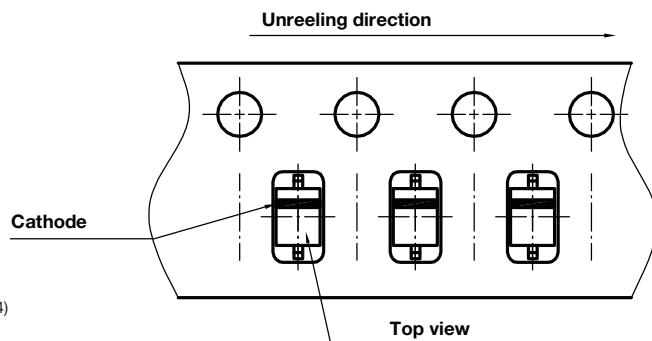


B-B Section



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Created - Date: 09. Feb. 2010  
22824

## ORIENTATION IN CARRIER TAPE SOD-323



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Created - Date: 09. Feb. 2010  
22772



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