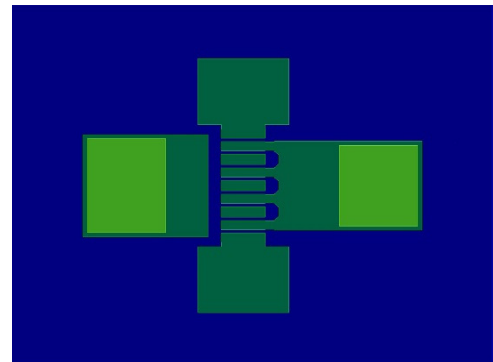


Product Overview

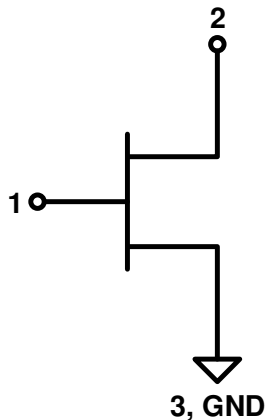
The Qorvo TGF2942 is a 2 W (P_{3dB}) discrete GaN on SiC HEMT which operates from DC to 25 GHz and 28 V supply. The device is constructed with Qorvo’s proven QGaN15 process. The device can support pulsed, CW, and linear operations.

Lead-free and ROHS compliant



0.411 x 0.551 x 0.100 mm

Functional Block Diagram



Key Features

- Frequency: DC to 25 GHz
 - Output Power (P_{3dB})¹: 2.4 W
 - Linear Gain¹: 18 dB
 - Typical PAE_{3dB}¹: 59%
 - Typical Noise Figure¹: 1.2 dB
 - Operating Voltage: 28 V
 - CW and Pulse capable
 - Non-linear & Noise Models available
- Note 1: @ 10 GHz

Applications

- Defense and Aerospace
- Broadband wireless
- Low noise amplifier

Ordering info

Part No.	ECCN	Description
TGF2942	EAR99	DC–25GHz, 28 V, 2 W GaN RF Transistor

Absolute Maximum Ratings¹

Parameter	Rating	Units
Breakdown Voltage, BV_{DG}	+60	V
Gate Voltage Range, V_G	-7 to +1.5	V
Drain Current, $I_{D_{MAX}}$	500	mA
Gate Current Range, I_G	See page 20.	mA
Power Dissipation, CW, P_{DISS}	3.2	W
RF Input Power, CW, 10 GHz, $T = 25\text{ }^\circ\text{C}$	+23	dBm
Channel Temperature, T_{CH}	275	$^\circ\text{C}$
Mounting Temperature (30 Seconds)	320	$^\circ\text{C}$
Storage Temperature	-65 to +150	$^\circ\text{C}$

Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions¹

Parameter	Min	Typ	Max	Units
Operating Temp. Range	-40	+25	+85	$^\circ\text{C}$
Drain Voltage Range, V_D	+12	+20	+29.5	V
Drain Bias Current, I_{DQ}	10	20	40	mA
Drain Current, I_D	-	170	-	mA
Gate Voltage, V_G^3	-	-2.8	-	V
Channel Temperature (T_{CH})	-	-	250	$^\circ\text{C}$
Power Dissipation, CW (P_D) ²	-	-	2.9	W

Notes:

1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85 $^\circ\text{C}$
3. To be adjusted to desired I_{DQ}

Model Load Pull Performance – Power Tuned¹

Parameter	Typical Values								Units
	3		6		10		18		
Frequency, F									GHz
Drain Voltage, V_D	20	28	20	28	20	28	20	28	V
Drain Bias Current, I_{DQ}	20	20	20	20	20	20	20	20	mA
Output Power at 3dB compression, P_{3dB}	32.5	33.8	32.5	33.7	32.6	33.8	32.8	33.8	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	58.7	61.3	60.5	58.6	57.2	56.6	54.3	54.2	%
Gain at 3dB compression, G_{3dB}	20.5	22.5	17.3	19.5	12.8	13.6	8.9	9.8	dB
Load Reflection Coefficient ⁽²⁾ , Γ_L	0.32 \angle 18°	0.54 \angle 22°	0.42 \angle 45°	0.57 \angle 45°	0.45 \angle 63°	0.58 \angle 59°	0.61 \angle 99°	0.70 \angle 90°	--

Notes:

1. CW, bondwires not included
2. Characteristic Impedance, $Z_0 = 50 \Omega$.

Model Load Pull Performance – Efficiency Tuned¹

Parameter	Typical Values								Units
	3		6		10		18		
Frequency, F									GHz
Drain Voltage, V_D	20	28	20	28	20	28	20	28	V
Drain Bias Current, I_{DQ}	20	20	20	20	20	20	20	20	mA
Output Power at 3dB compression, P_{3dB}	32.1	33.8	31.5	33.7	31.7	33.4	32.1	33.8	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	62.8	61.3	61.5	58.6	60.3	59.2	56.3	54.2	%
Gain at 3dB compression, G_{3dB}	22.6	22.5	17.9	19.5	14.9	15.3	9.4	9.8	dB
Load Reflection Coefficient ⁽²⁾ , Γ_L	0.45 \angle 27°	0.54 \angle 22°	0.57 \angle 45°	0.57 \angle 45°	0.63 \angle 72°	0.67 \angle 63°	0.71 \angle 98°	0.70 \angle 90°	--

Notes:

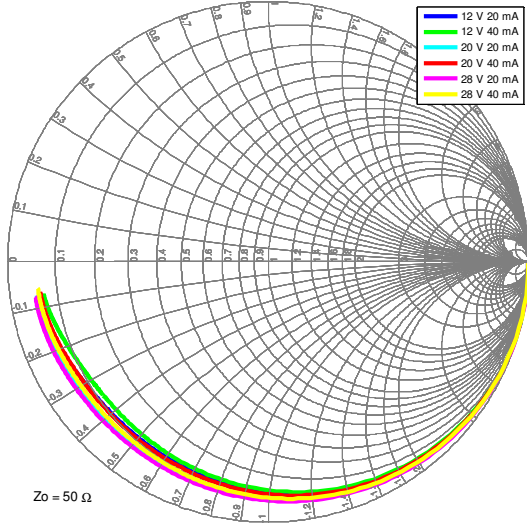
1. CW, bondwires not included
2. Characteristic Impedance, $Z_0 = 50 \Omega$.

Model S-parameters¹

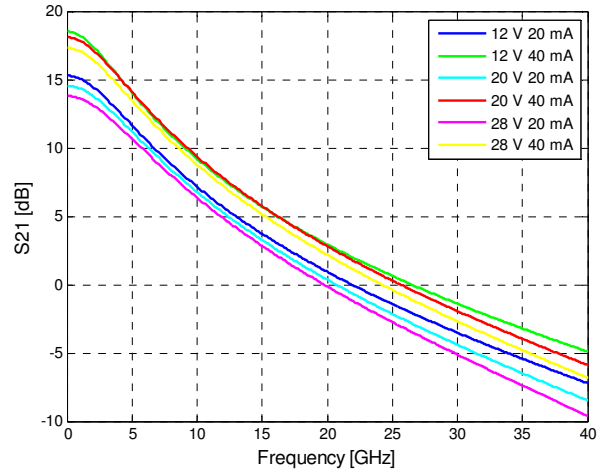
Notes:

- Bondwires are not included. T = 25 °C.

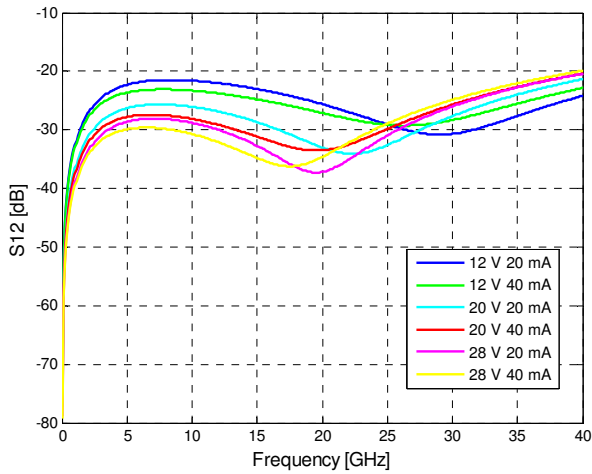
S11 from 0.01 GHz to 40 GHz



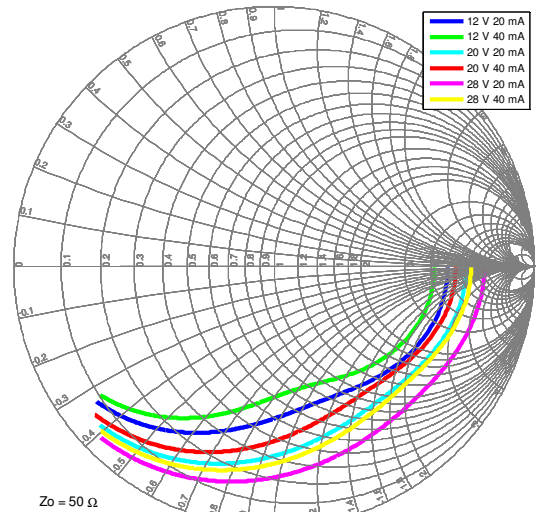
S21



S12



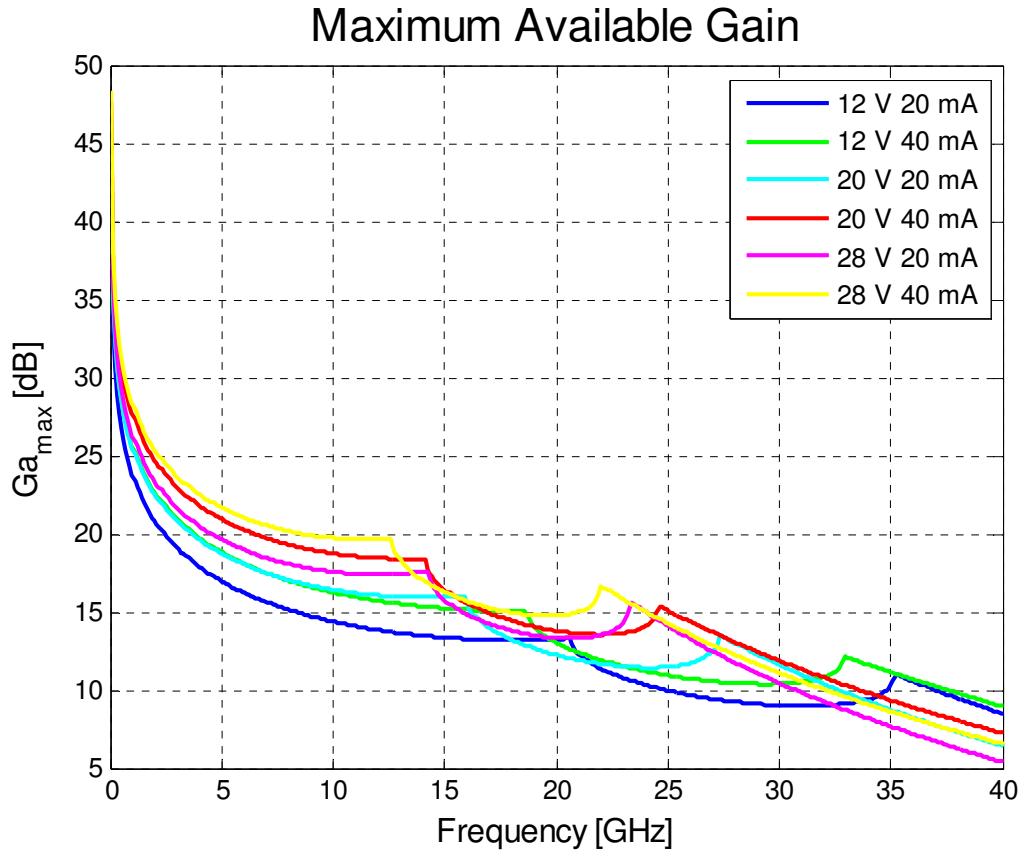
S22 from 0.01 GHz to 40 GHz



Model Maximum Available Gain¹

Notes:

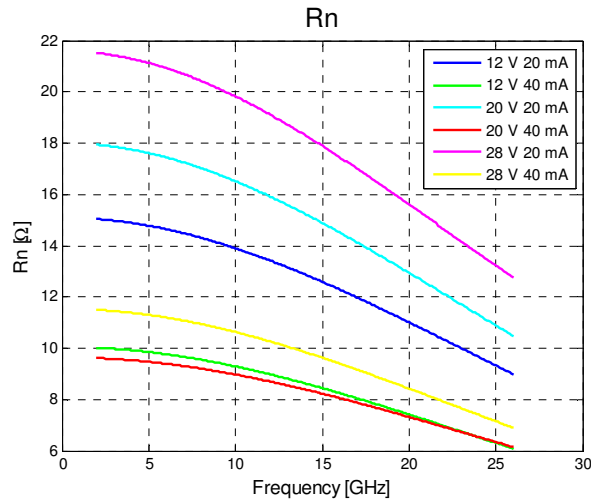
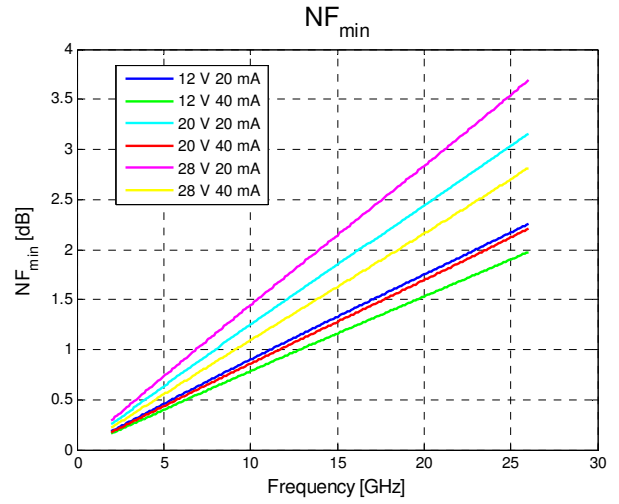
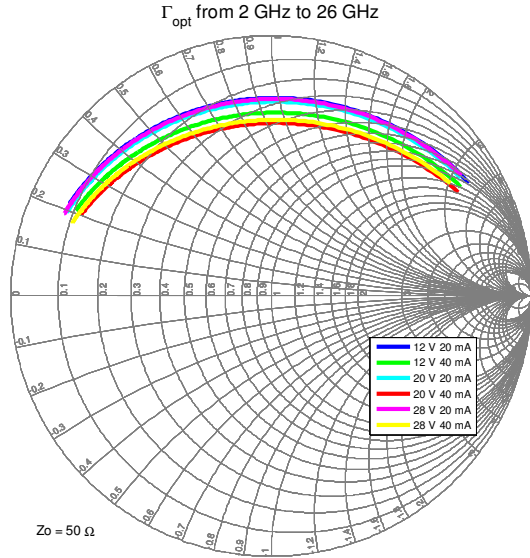
- 1. Bondwires are not included. T = 25 °C.



Model Noise¹

Notes:

- 1. Bondwires are not included. T = 25 °C.

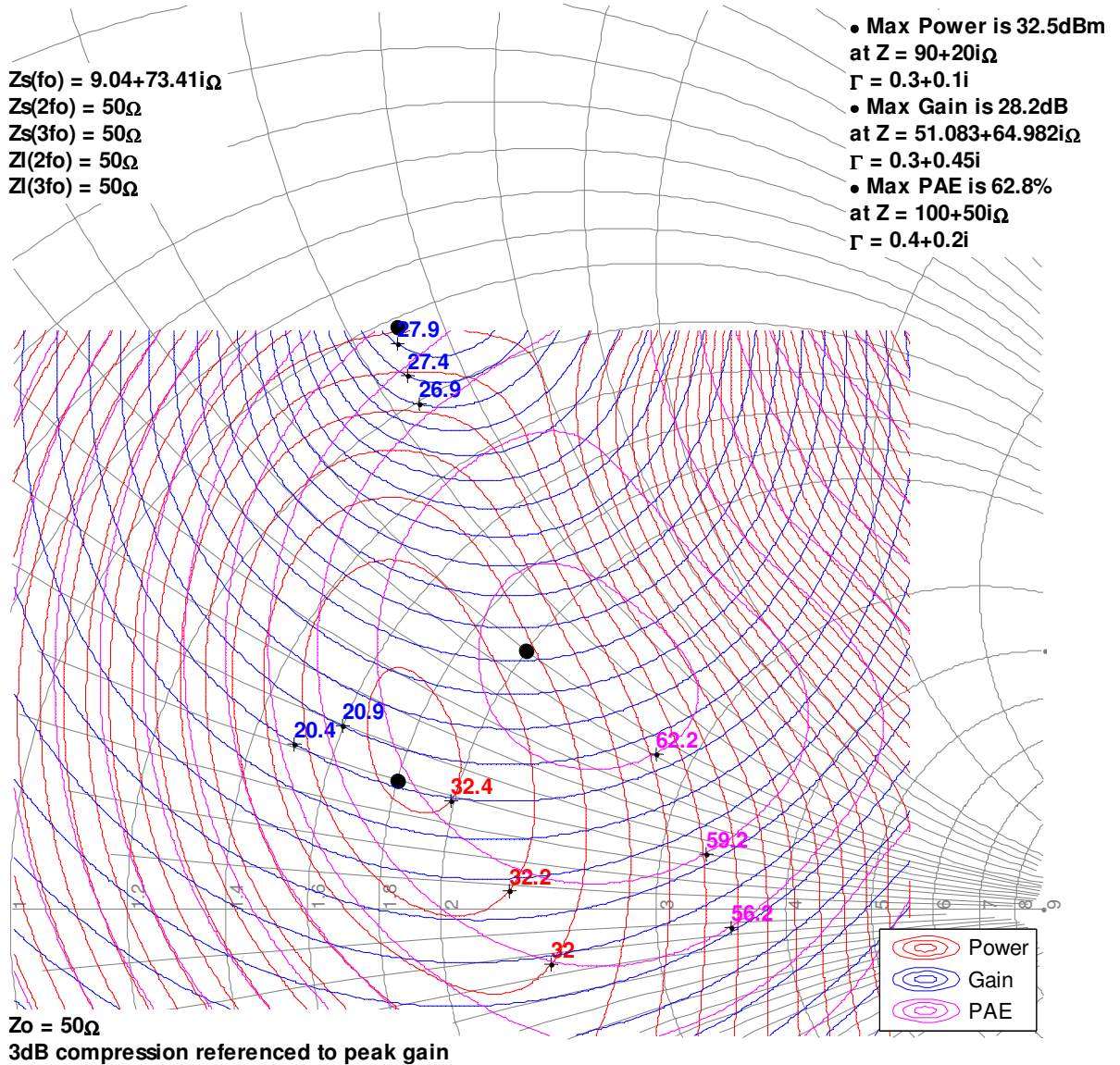


Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 20\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.

3GHz, Load-pull

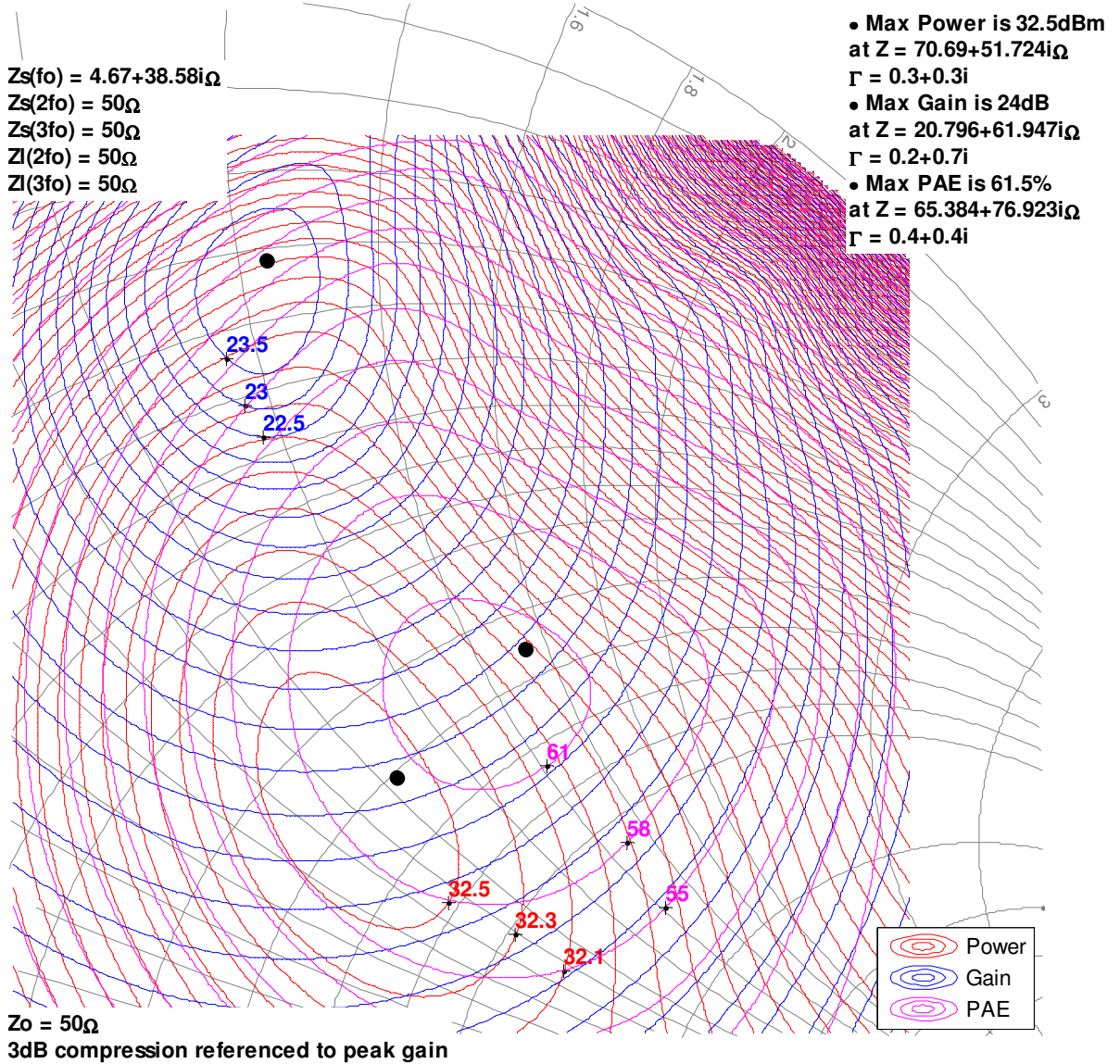


Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 20\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.

6GHz, Load-pull

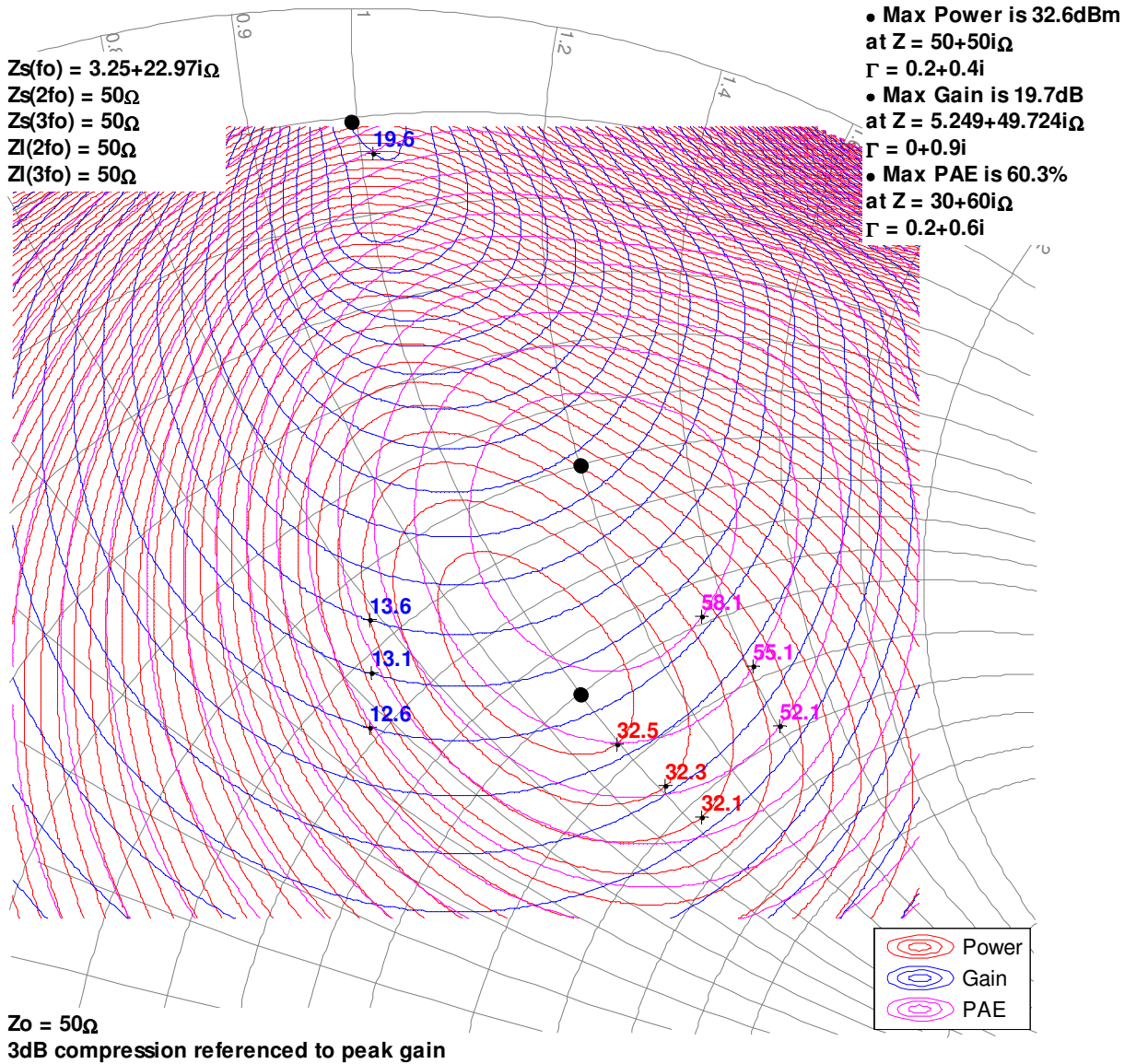


Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 20\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.

10GHz, Load-pull

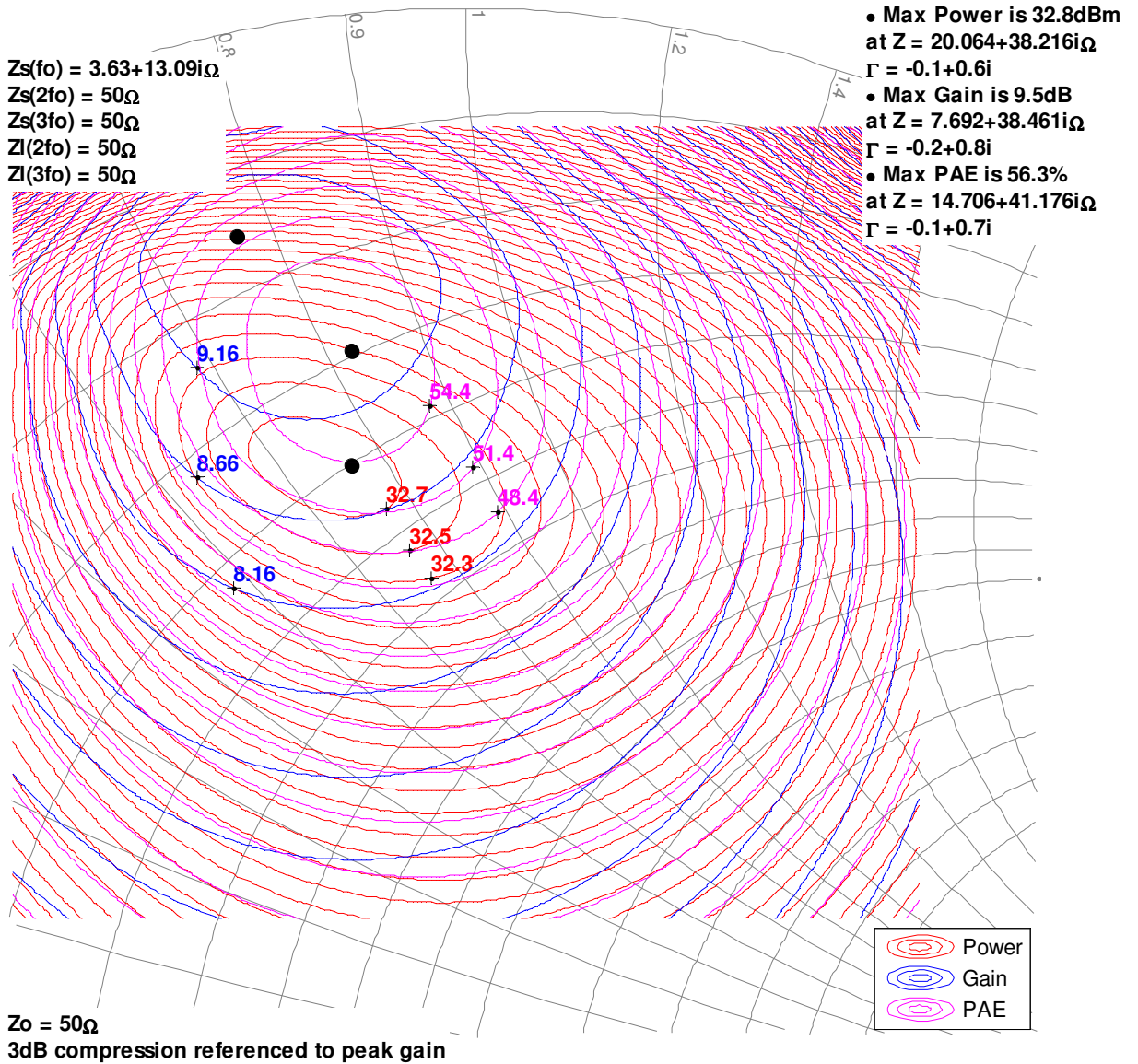


Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 20\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.

18GHz, Load-pull

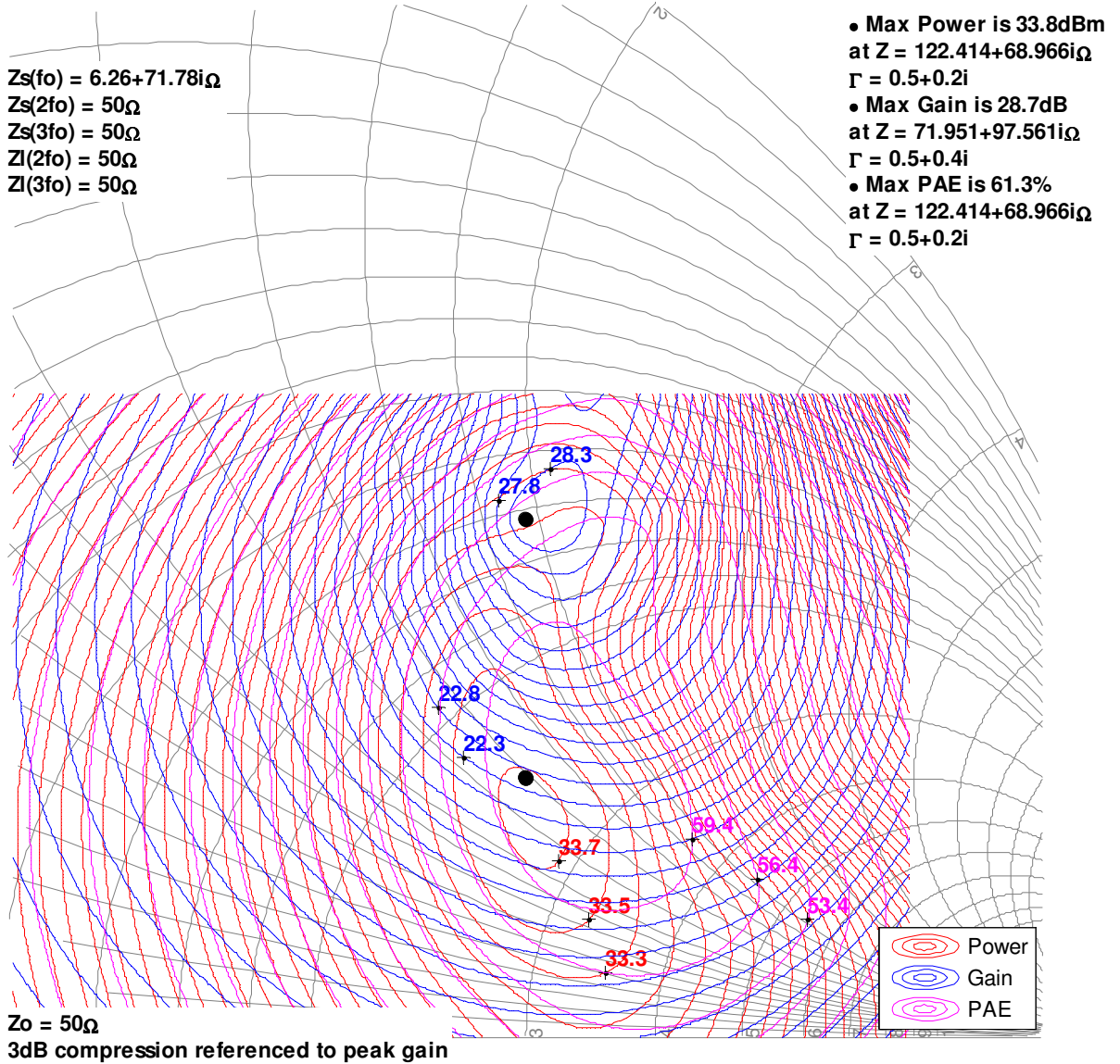


Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 28\text{ V}$, $I_{DQ} = 40\text{ mA}$, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.

3GHz, Load-pull

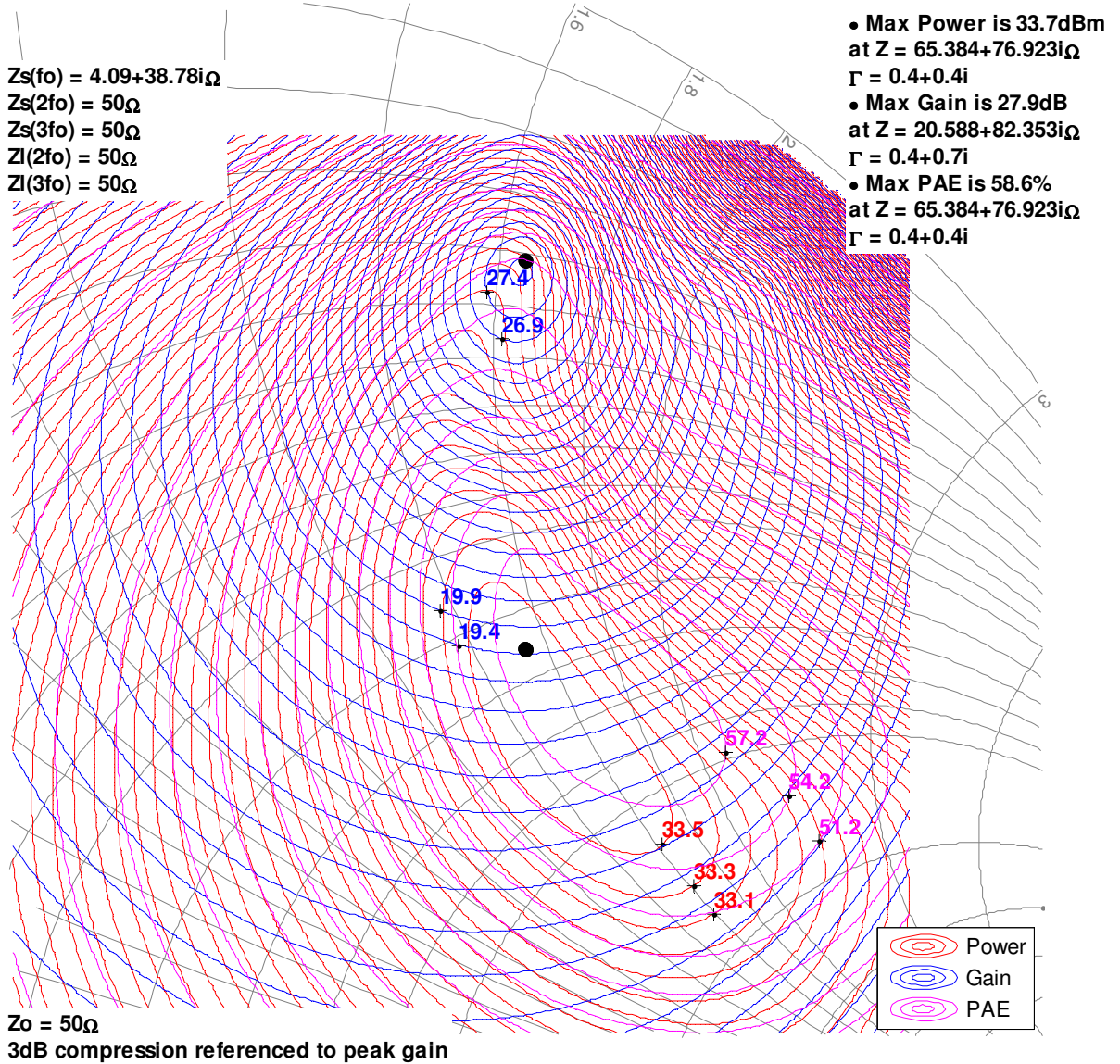


Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 28\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.

6GHz, Load-pull

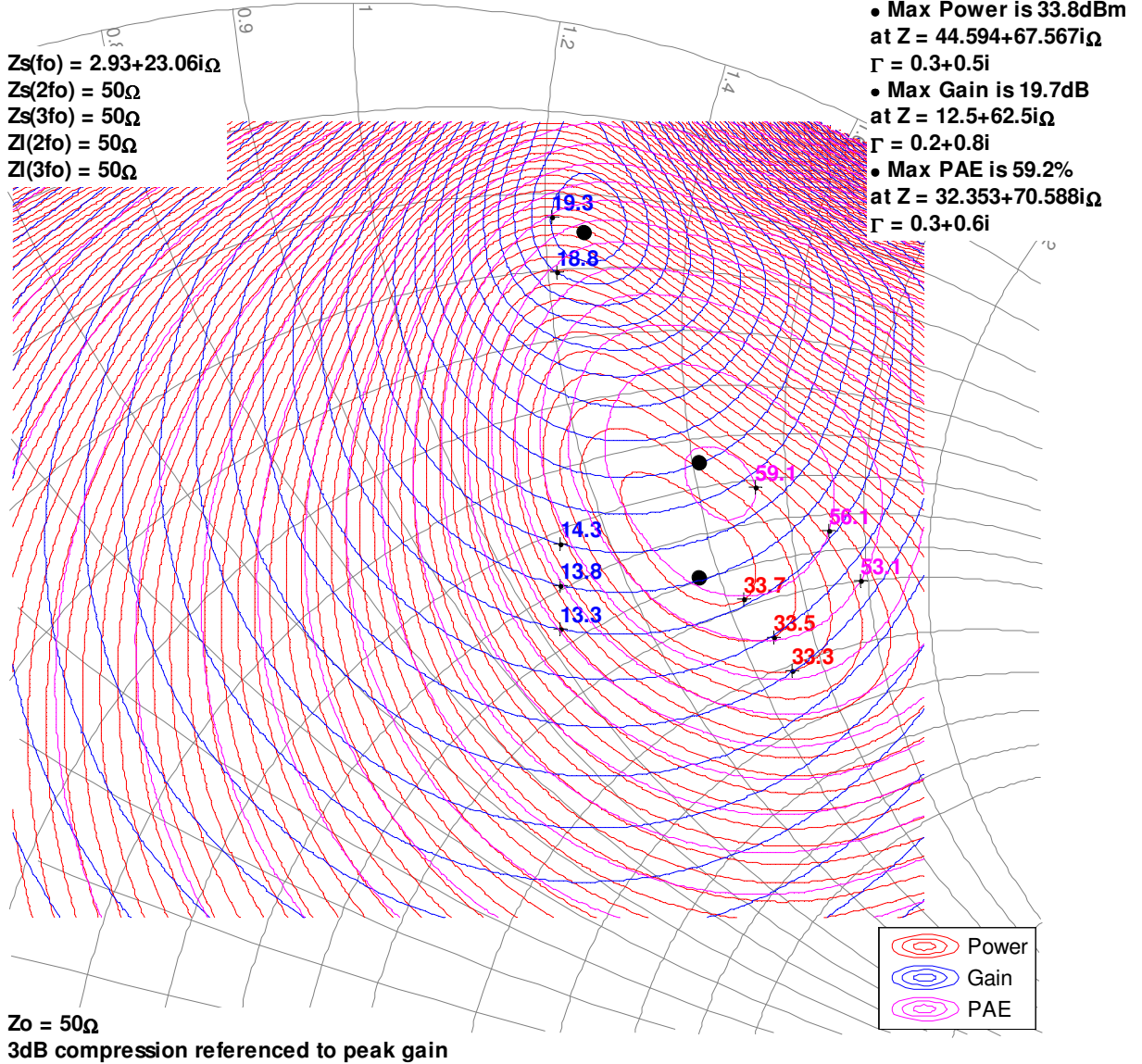


Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 28\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.

10GHz, Load-pull

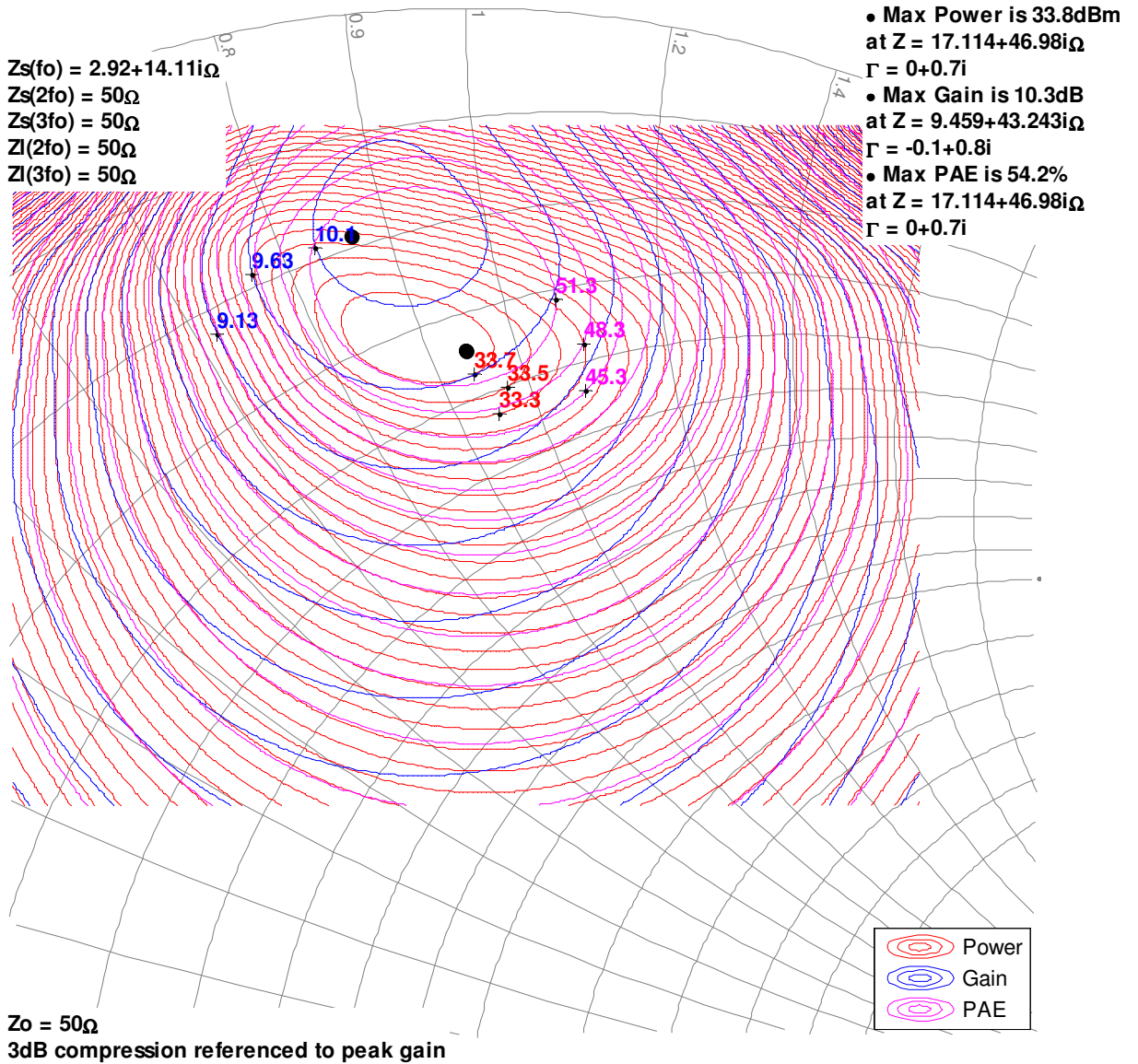


Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 28\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.

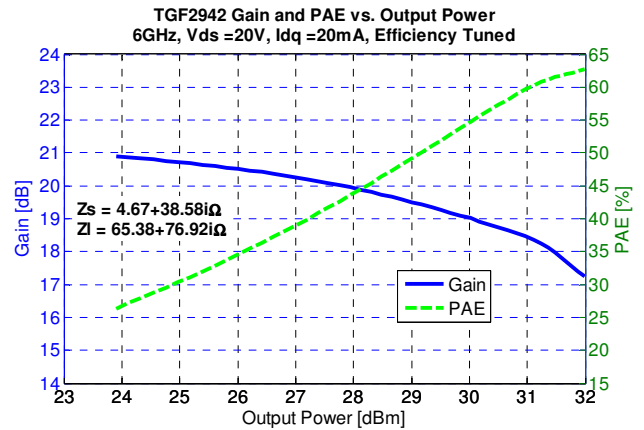
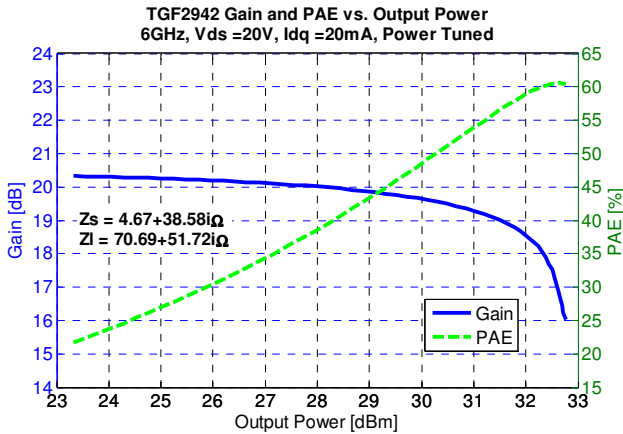
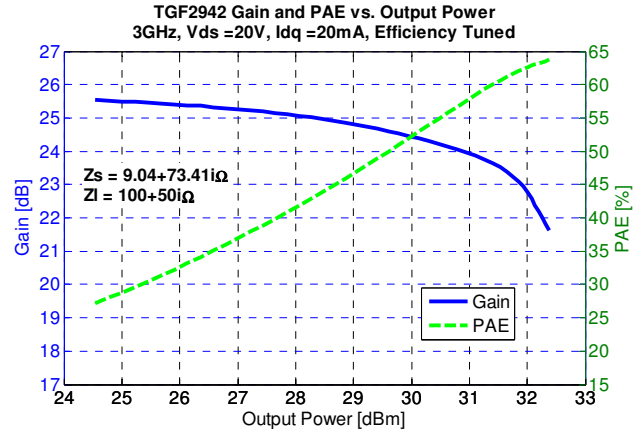
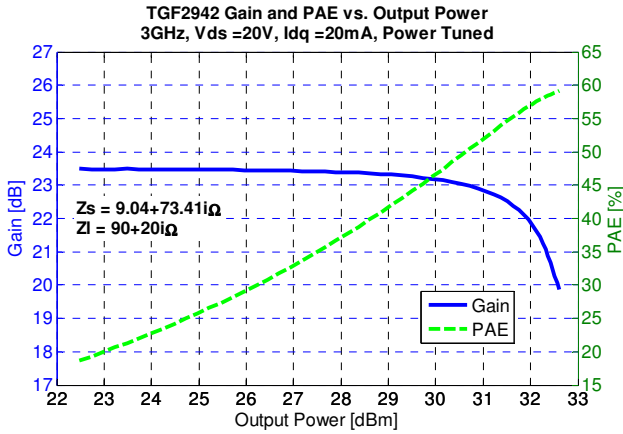
18GHz, Load-pull



Typical Model Performance – Load-Pull Drive-up^{1,2}

Notes:

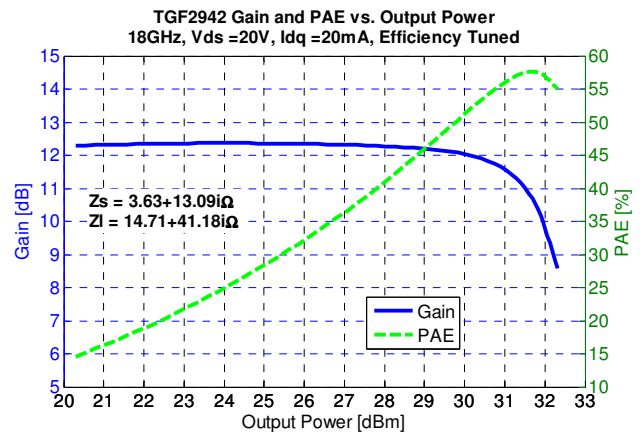
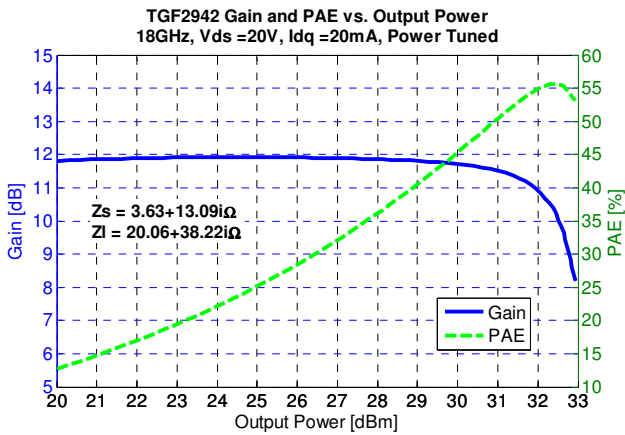
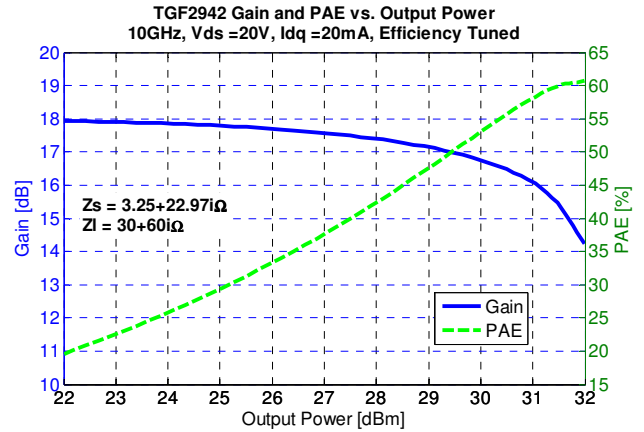
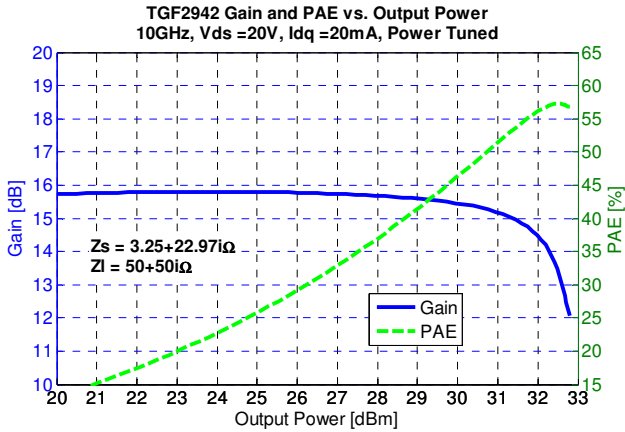
1. CW, Bondwires not included
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



Typical Model Performance – Load-Pull Drive-up^{1,2}

Notes:

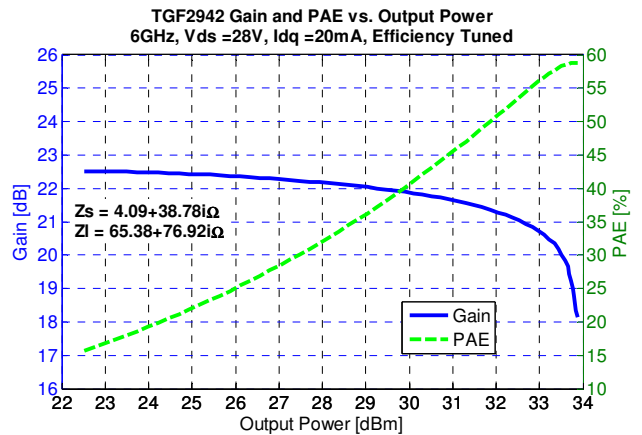
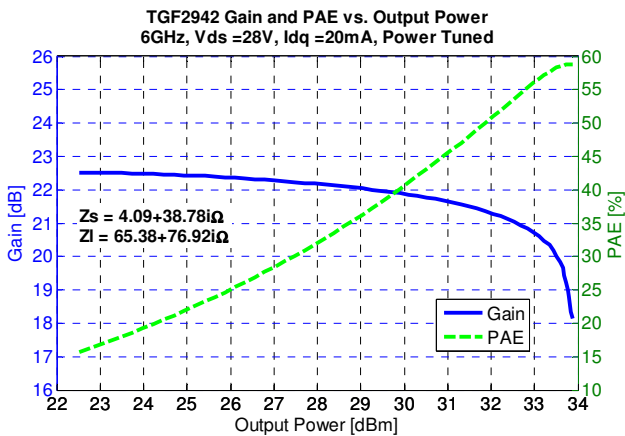
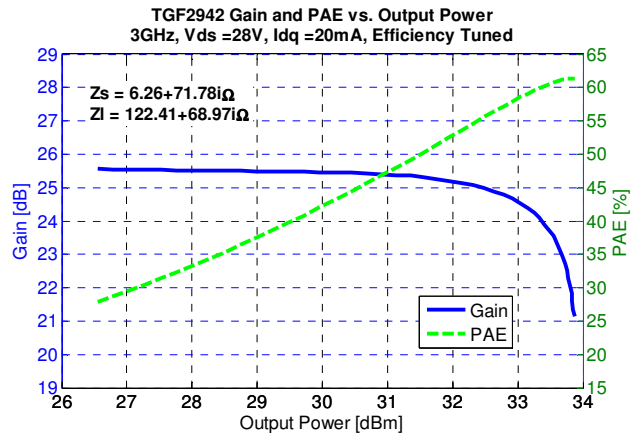
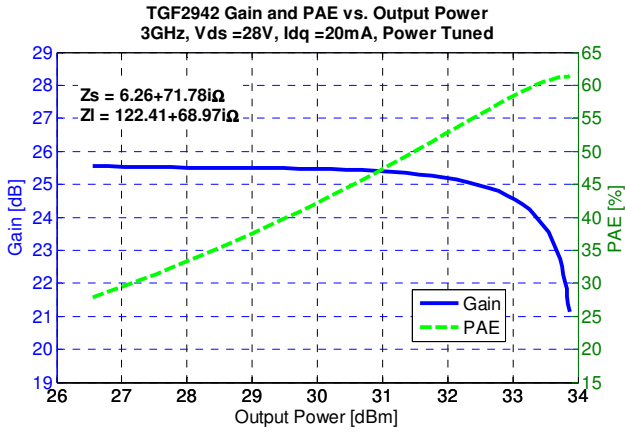
1. CW, Bondwires not included
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



Typical Model Performance – Load-Pull Drive-up^{1, 2}

Notes:

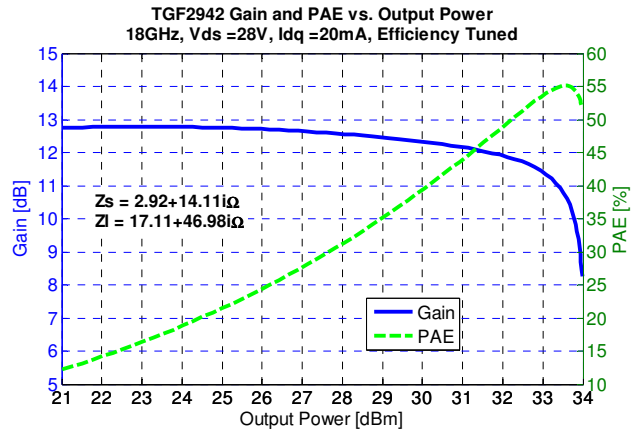
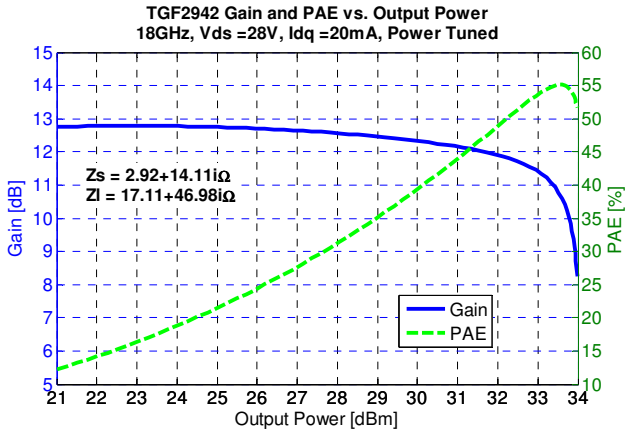
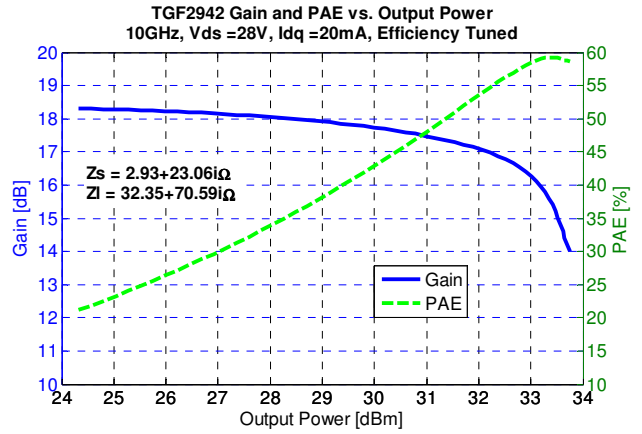
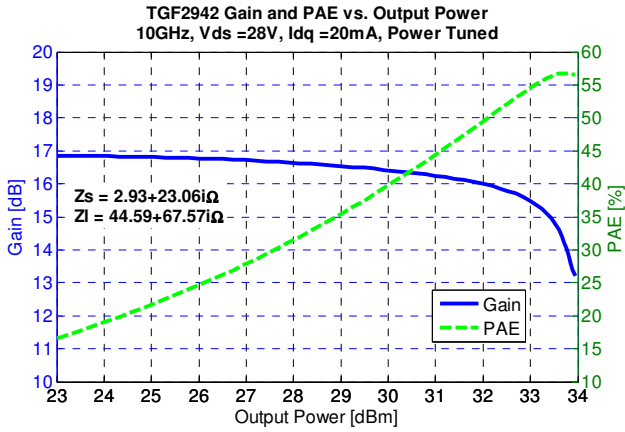
1. CW, Bondwires not included
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



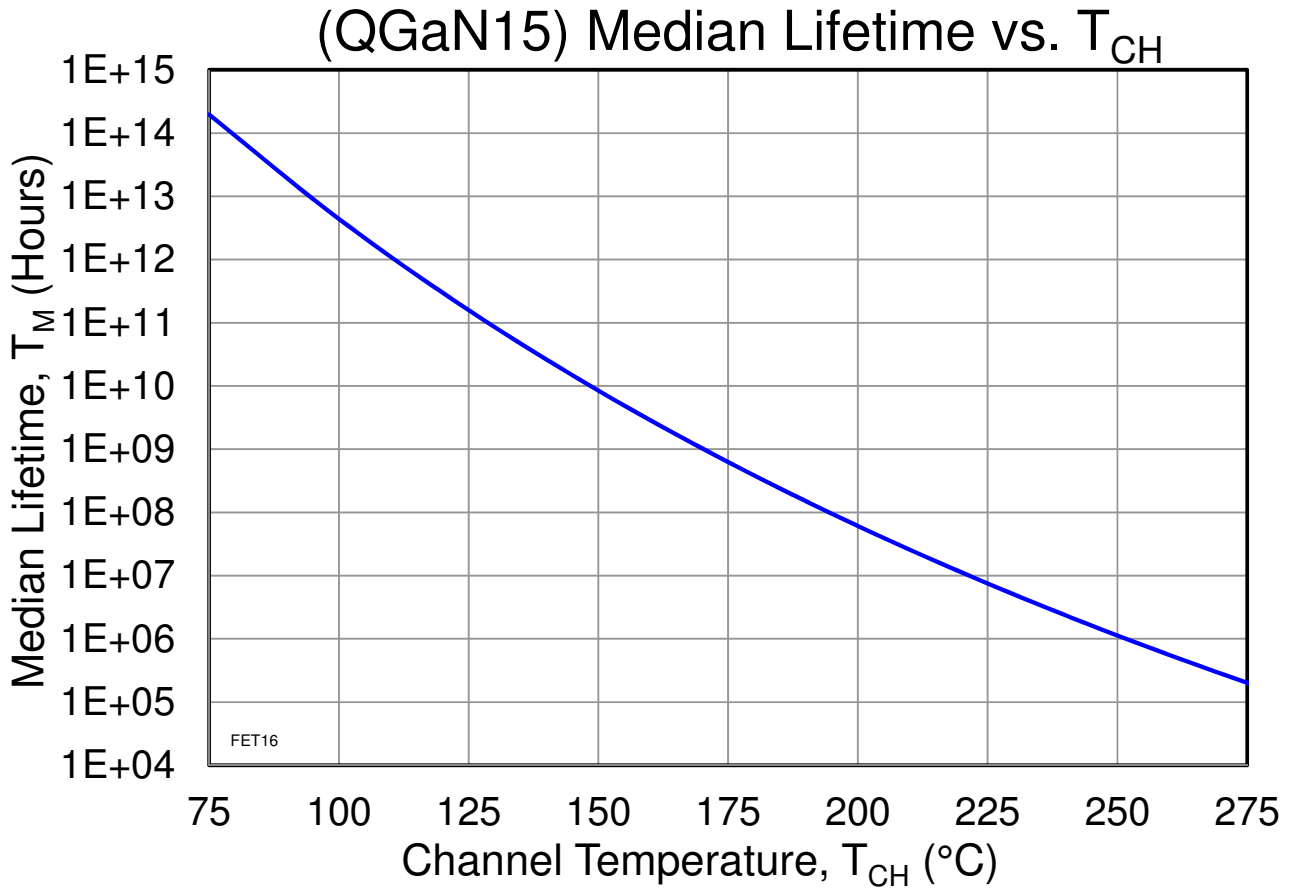
Typical Model Performance – Load-Pull Drive-up^{1,2}

Notes:

1. CW, Bondwires not included
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.

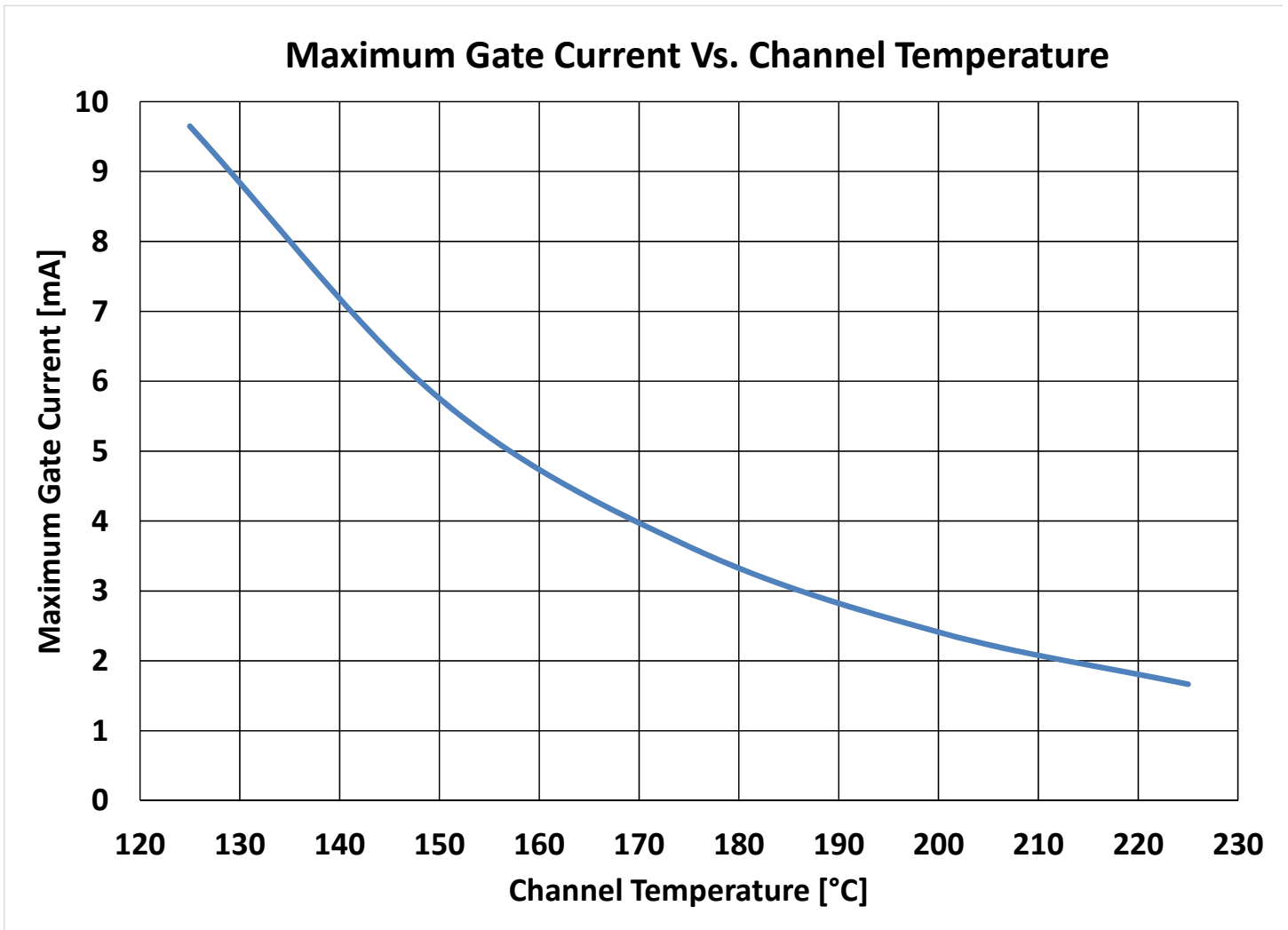


Median Lifetime¹



Notes:

1. Test Conditions: $V_D = +28\text{ V}$; Failure Criteria = 10% reduction in I_{D_MAX} during DC Life Testing

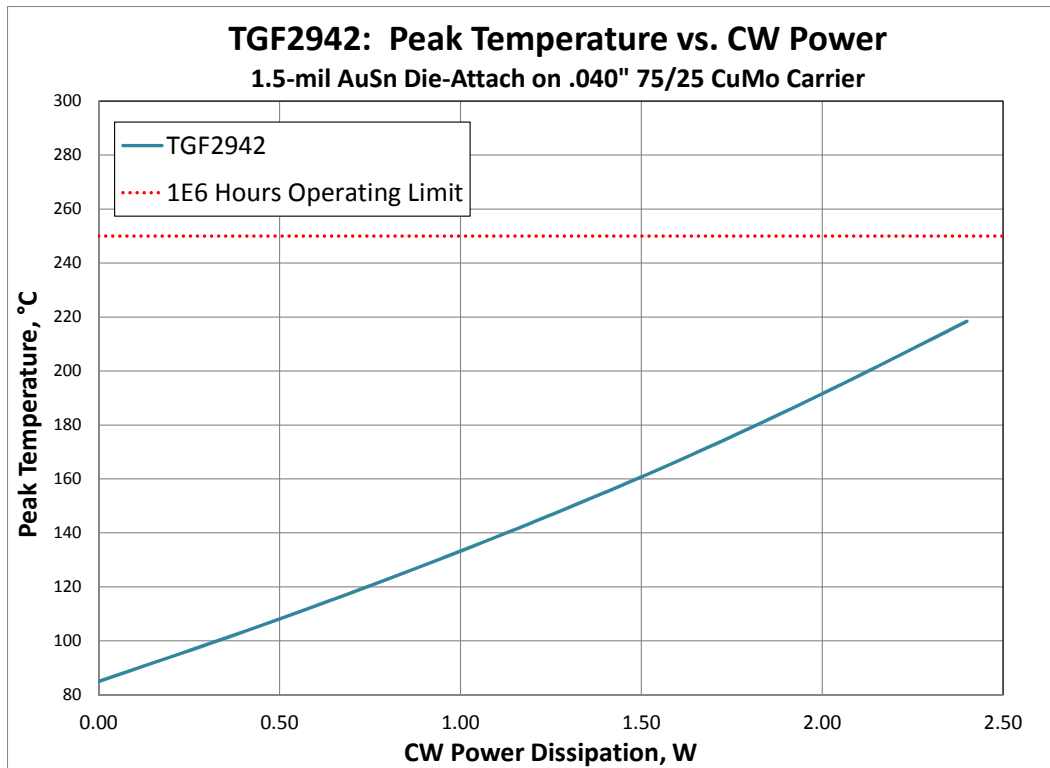
Maximum Gate Current

Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} ⁽¹⁾	CW	45.0	°C/W
Channel Temperature, T_{CH}	$T_{baseplate} = +85\text{ °C}$	103	°C
Median Lifetime, T_M	$P_{DISS} = 0.4\text{ W}$	2.9E12	Hrs
Thermal Resistance, θ_{JC} ⁽¹⁾	CW	47.5	°C/W
Channel Temperature, T_{CH}	$T_{baseplate} = +85\text{ °C}$	123	°C
Median Lifetime, T_M	$P_{DISS} = 0.8\text{ W}$	2.0E11	Hrs
Thermal Resistance, θ_{JC} ⁽¹⁾	CW	49.2	°C/W
Channel Temperature, T_{CH}	$T_{baseplate} = +85\text{ °C}$	144	°C
Median Lifetime, T_M	$P_{DISS} = 1.2\text{ W}$	1.7E10	Hrs
Thermal Resistance, θ_{JC} ⁽¹⁾	CW	51.3	°C/W
Channel Temperature, T_{CH}	$T_{baseplate} = +85\text{ °C}$	167	°C
Median Lifetime, T_M	$P_{DISS} = 1.6\text{ W}$	1.4E9	Hrs
Thermal Resistance, θ_{JC} ⁽¹⁾	CW	53.5	°C/W
Channel Temperature, T_{CH}	$T_{baseplate} = +85\text{ °C}$	192	°C
Median Lifetime, T_M	$P_{DISS} = 2.0\text{ W}$	1.2E8	Hrs
Thermal Resistance, θ_{JC} ⁽¹⁾	CW	55.4	°C/W
Channel Temperature, T_{CH}	$T_{baseplate} = +85\text{ °C}$	218	°C
Median Lifetime, T_M	$P_{DISS} = 2.4\text{ W}$	1.3E7	Hrs

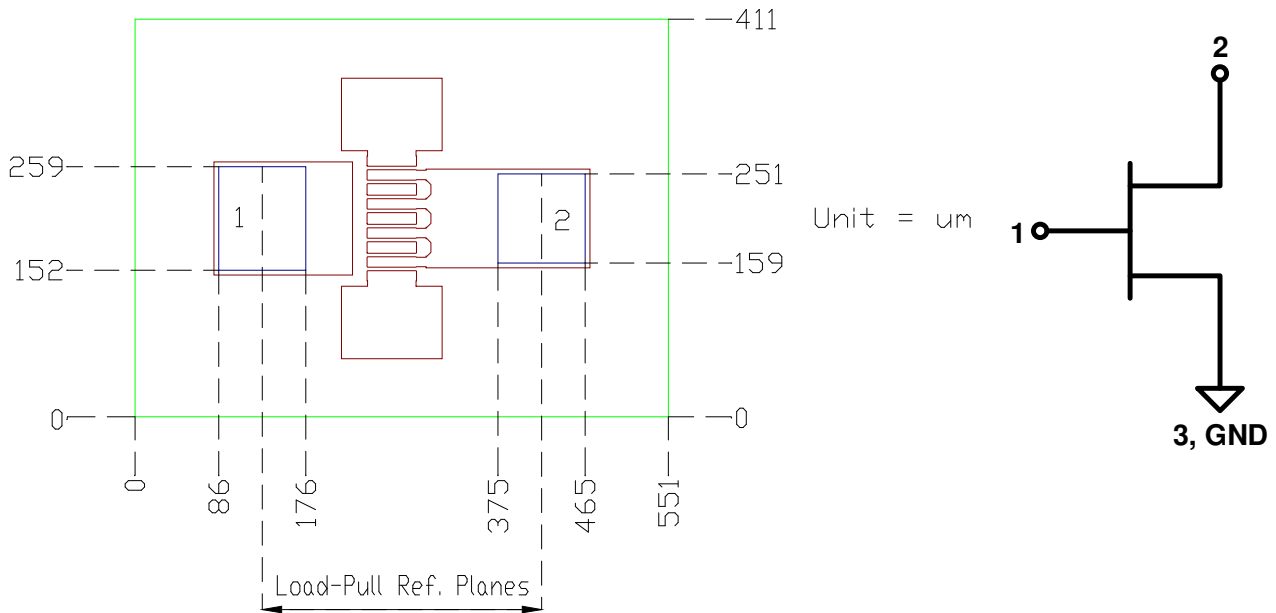
Notes:

1. Thermal resistance measured at back of package.



Pin Configuration and Description¹

Notes: 1. Die size tolerance is ± 0.015 mm.



Pin Description

Pin	Symbol	Description	Dimension
1	RF IN / V_G	Gate	0.107 x 0.090 mm
2	RF OUT / V_D	Drain	0.092 x 0.090 mm
3	Source	Source / Ground	0.411 x 0.551 mm

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) not recommended.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Ball bonding is the preferred interconnect technique, except where noted on the assembly diagram.
- Force, time, and ultrasonics are critical bonding parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Disclaimer

GaN/SiC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Bias-up Procedure

1. Set V_G to -4 V.
2. Set I_D limit to 25 mA.
3. Slowly adjust V_G until I_D reaches 20 mA.
4. Set I_D limit to 180 mA.
5. Apply RF signal.

Bias-down Procedure

1. Turn off RF signal.
2. Turn off V_D and wait 1 second to allow drain capacitor discharge.
3. Turn off V_G .

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	N/A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	N/A	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	N/A	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.

Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

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Tel: +1.972.994.8465

Fax: +1.972.994.8504

For technical questions and application information:

Email: info-products@qorvo.com

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