

TENTATIVE SPECIFICATIONS

DATE Aug.27 2013

PRODUCT NAME:

LC706200CM

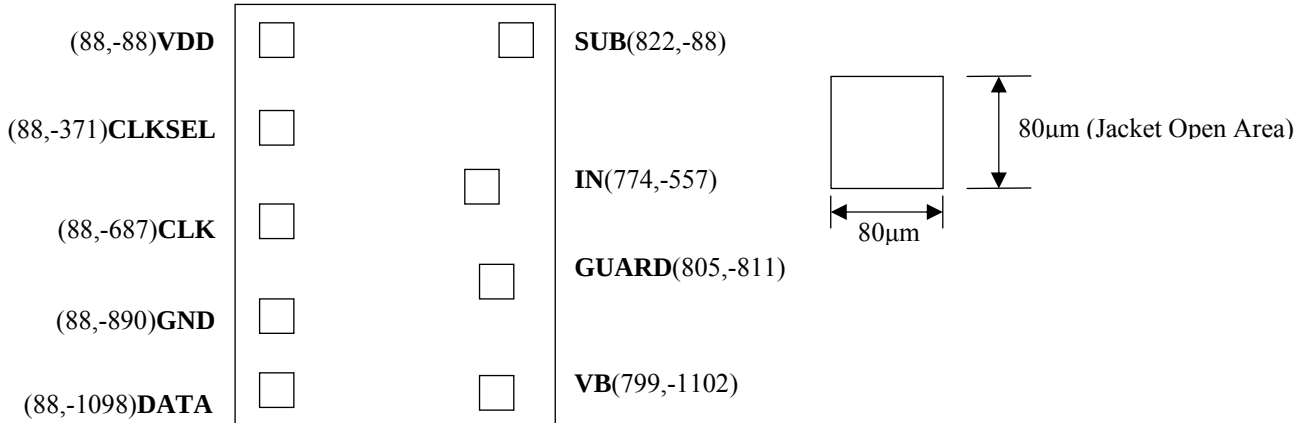
- Case Outline: Wafer Ring(8inch)
- Function: Semiconductor IC for Digital Silicon Microphone includes Pre-amplifier and Sigma Delta Modulator and Charge Pump.
- Application: Cellular phone and other
- Absolute Maximum Ratings at Ta=25°C, GND = 0V

Parameter	Symbol	Pin Name	Min	Max	Units
Maximum power supply voltage	V _{DD} max	VDD	-0.3	+4.0	V
Maximum input voltage	V _{CLK} max	CLK,CLKSEL	-0.3	VDD+0.3	V
	V _{IN} max	IN	-0.3	VDD+0.3	V
Maximum output voltage	V _{omax}	DATA	-0.3	VDD+0.3	V
Operating temperature range	Ta		-30	70	°C
Storage temperature range	Tstg		-40	85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Pad Coordinate (0,0)

PAD Size



5. Circuit Parameters

Parameter	Symbol	Pin Name	Test Condition	Min	Typ	Max	Units
Input capacitance of die	Cin	IN			0.4		pF

Note: IN-Pin has a limited protection against ESD. Value of IN-Pin is proven by design.

6. DC Electrical Characteristics Ratings at Ta=25°C,VDD=3.3V,GND=0V,Fclk=2.4MHz, Fduty =50%

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Units
Power supply voltage	VDD	VDD		1.64	3.3	3.6	V
Power consumption (IO Power consumption is not Included)	IDD	VDD	VDD=3.3V		800		uA
Standby Current	ISTBY	VDD	VDD=3.3V			200	nA
Input/Output LOW level	Viol	CLK, DATA CLKSEL	DATA : Iol=0.5mA			0.35×VDD	V
Input/Output HIGH level	Vioh	CLK, DATA CLKSEL	DATA : Ioh=-0.5mA	0.65×VDD			V

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Charge pump voltage	Vbias	VB/SUB	VDD=3.3V		10.5		V
Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Units
Charge Pump voltage tolerance	Tolerance	VB/SUB		-8		+8	%

7. AC Electrical Characteristics Ratings at Ta=+25°C, VDD=3.3V, GND=0V, Signal Frequency=1KHz, Measurement frequency=100Hz~20KHz, Fclk=2.4MHz, Fduty =50%, Bypass capacitor=0.1uF(VDD-GND)

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Units
Clock Frequency (Normal Operation)	Fclk	CLK		1	2.4	3.25	MHz
Clock Frequency (Sleep Mode)	Fclk_SL	CLK				1	KHz
Clock Duty	Fduty	CLK		40		60	%
Over Sampling Ratio	OSR				50		
Maximum Input Voltage (Input Full Scale Voltage)	Vin	IN	0dBFS (= 120dBSPL)		158.5		mVrms
THD / THD+N	THD_0	DATA	Vout=0dBFS (= 120dBSPL) (= 158.5mVrms)			10	% (THD)
	THD+N_1 ※1	DATA	Vout=-5dBFS (= 115dBSPL) (= 89.1mVrms) 1KHz Sin-Wave			5	% (THD+N)
	THD+N_2 ※1	DATA	Vout=-20dBFS (= 100dBSPL) (= 15.8mVrms) 50-4KHz Sin-Wave			1	% (THD+N)
Digital Noise Floor	DNF1	DATA	Bandwidth 20KHz A-weighted		-87		dBFS
PSRR ※1	PSRR	DATA	217Hz Square, 10MHz-Broadband Noise, 100mVpp		-70		dBFS
Transfer function ※2	TF1	DATA			18		dB
Wake Up Time ※1	WUT	CLK	Fclk=2.4MHz			10	ms
Fall Asleep Time ※1	FAT		Fclk=1KHz			10	ms

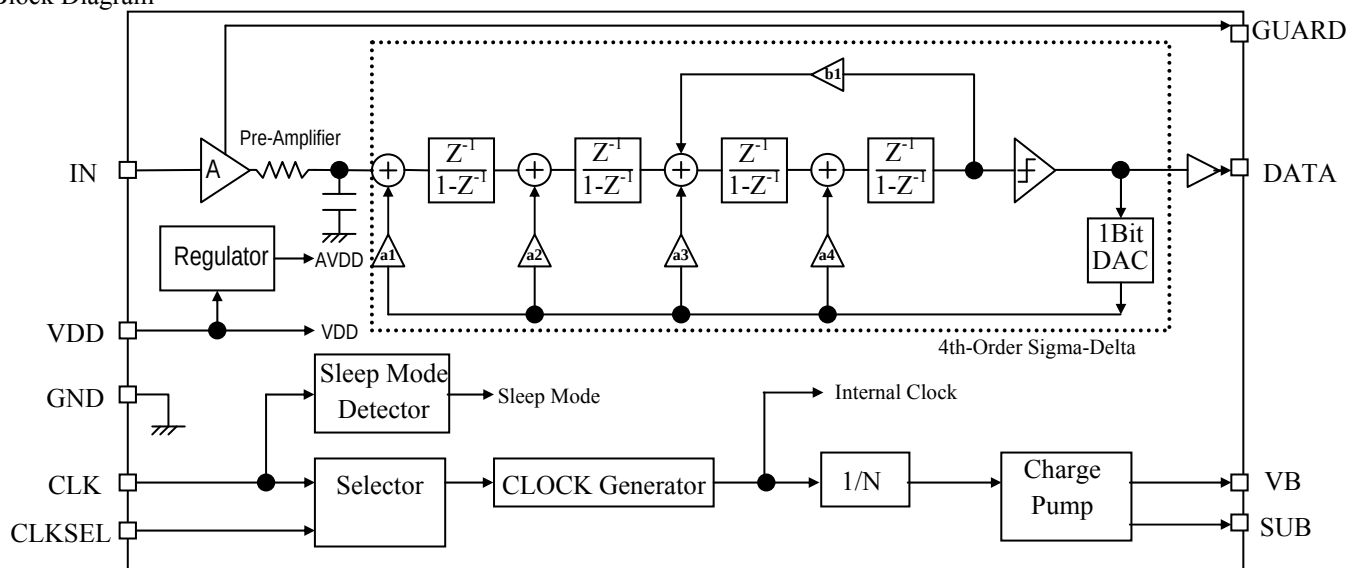
Note1 : ※1 are Reference data:No measurement.

Note2 : ※2 Each product has been designed with performance of +/-0.5dB tolerance for transfer function however it's not checked in outgoing inspection.

Note3: Input Full Scale Voltage 0dBFS is equivalent to 120dBSPL (= 158.5mVrms).

Note4: SNR Input Level Condition is -26dBFS (= 7.9mVrms, 94dBSPL, 1Pa).

Block Diagram



Pin Descriptions

No.	Pin Name	Function	I/O	Pin conditions
-	GND	Ground	—	—
-	VDD	Power Supply	—	—
-	GUARD	Connect to GUARD of MEMS	—	—
-	SUB	Connect to SUB of MEMS	—	—
-	DATA	PDM Data Output	output	
-	CLKSEL	CLK Select signal input Case1: When CLKSEL is LOW, PDM data is outputted in sync with negative edge of CLK. Case2: When CLKSEL is HIGH, PDM data is outputted in sync with positive edge of CLK.	Input	
-	CLK	Clock input	Input	
-	VB	Charge Pump Voltage Output	output	—
-	IN	Audio signal input	Input	

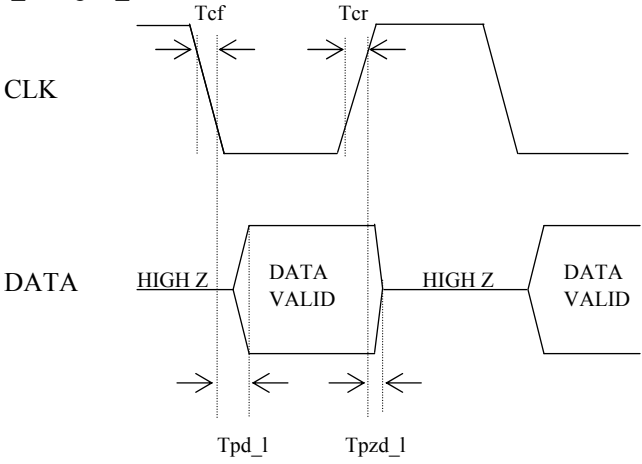
Switching Characteristics

(Ta=+25°C, VDD=1.8V,GND=0V,Fclk=2.4MHz ,Fduty=50%)

Case1 : CLKSEL=LOW

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Units
Clock Rise Time	Tcr	CLK				10	ns
Clock Fall Time	Tcf	CLK				10	ns
Output Data Delay	Tpd_l	DATA	CL=13pF,RL=1MΩ	20	31	40	ns
Output Hi-Z Delay	Tpzd_l	DATA	CL=13pF,RL=1MΩ	0	8	15	ns

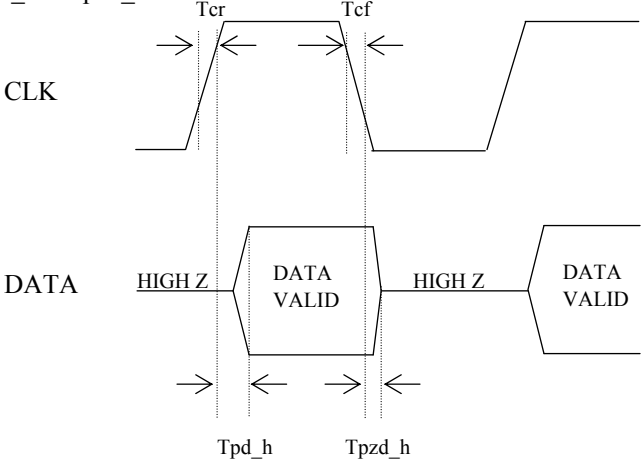
Note1: Tpd_l > Tpzd_l



Case2 : CLKSEL=HIGH

Parameter	Symbol	Pin Name	Condition	Min	Typ	Max	Units
Clock Rise Time	Tcr	CLK				10	ns
Clock Fall Time	Tcf	CLK				10	ns
Output Data Delay	Tpd_h	DATA	CL=13pF,RL=1MΩ	20	31	40	ns
Output Hi-Z Delay	Tpzd_h	DATA	CL=13pF,RL=1MΩ	0	8	15	ns

Note2: Tpd_h > Tpzd_h



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