

**ON Semiconductor®**



## **Schematic for the AR0135 Evaluation Board**

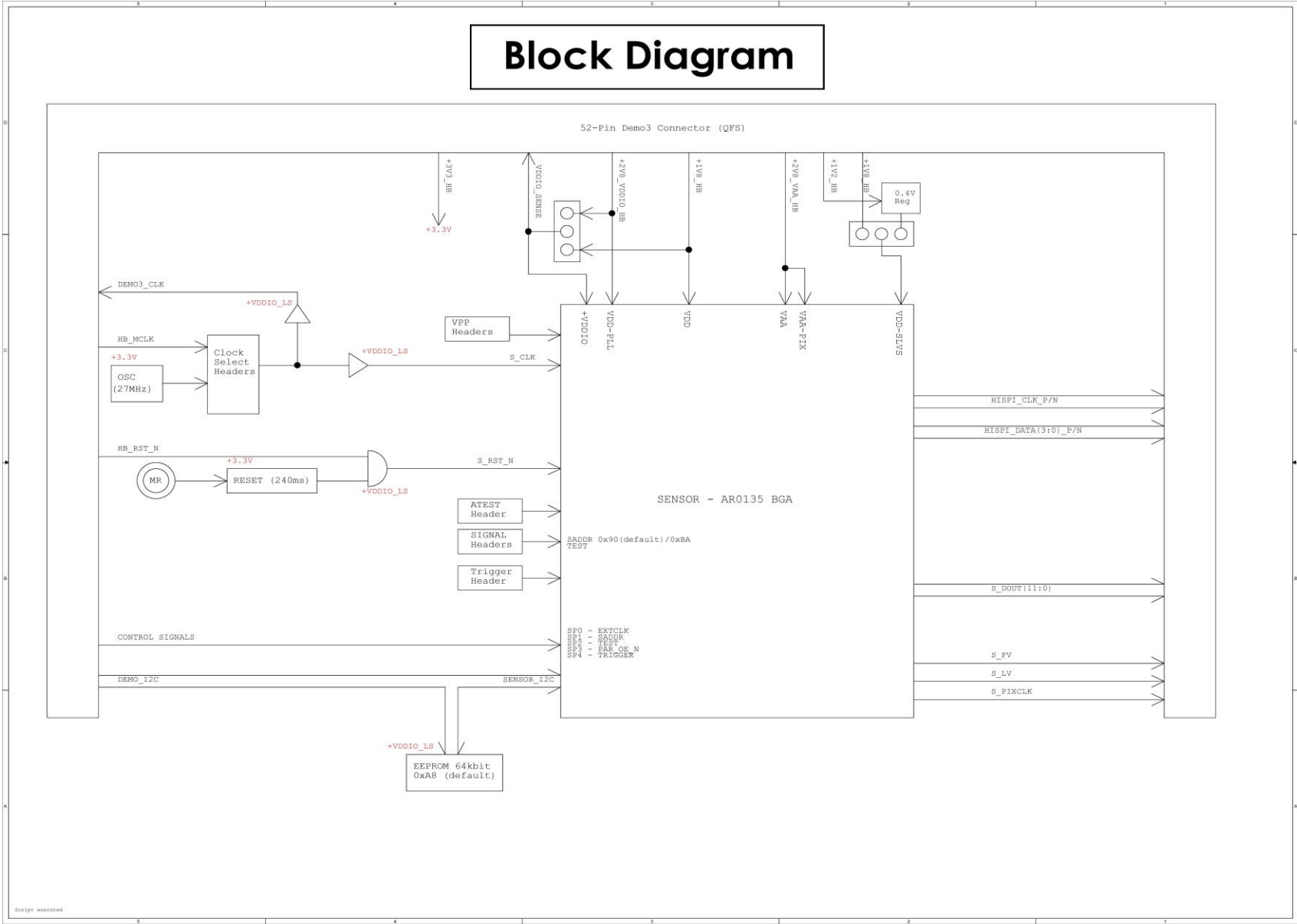


# AR0135\_BGA\_Demo3Head

Page	Description
1	Title Page
2	Block Diagram
3	Sensor
4	Power
5	Clock and Reset
6	External Interfaces

Rev	Who	Date	Description
Rev 0.0	aralex	05/07/14	Initial
Rev 0.0	aralex	05/08/14	Removed the 10nF Decaps on VDD and VDDIO for Sensor
		05/13/14	Updated the sensor with the new non socketed part, and added C-mount lens
		05/15/14	Updated the sensor with the new non socketed part, and added the socket for demo3 board
Rev 0.1	aralex	05/16/14	Removed text near R8 for TRIGGER signal Replaced R25 with a fixed resistor of 20K
	aralex	05/20/14	Removed Skip Block Fiducials FD4 and FD8.
Rev 1.0	aralex	04/23/15	Added a 2 pin header P28 for Trigger signal, deleted R8

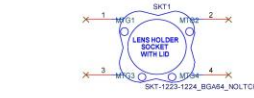
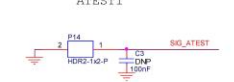
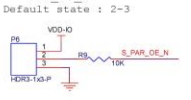
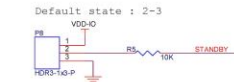
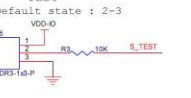
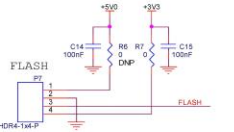
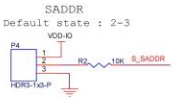
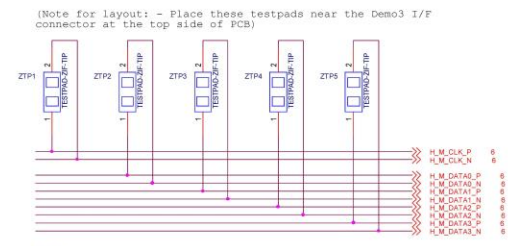
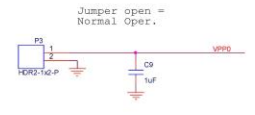
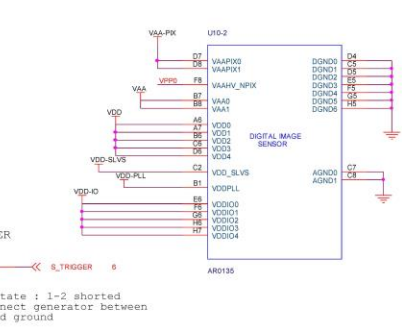
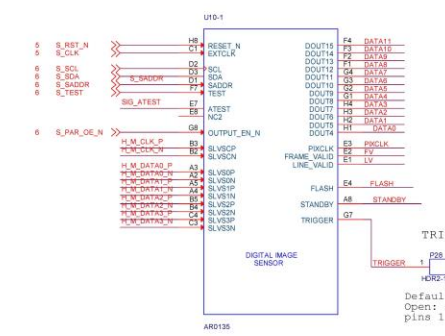
# Block Diagram





# Sensor

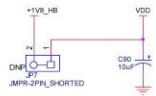
+SVD	4	+SVD	4
+VIO	4.5	+VIO	4.5
+VDDIO_LS	4.5.6	+VDDIO_LS	4.5.6
VDD	4	VDD	4
VDD-ID	4	VDD-ID	4
VDD-SLVS	4	VDD-SLVS	4
VDD-PLL	4	VDD-PLL	4
VAA	4	VAA	4
VAA-PK	4	VAA-PK	4



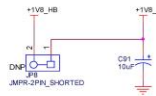
Debug Headers: Cut away the shorted trace and mount header for power debugging

# Power

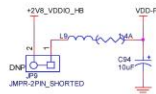
## VDD 1.8V SUPPLY



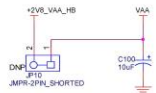
## VDD-SLVS 1.8V SUPPLY



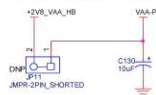
## VDD-PLL 2.8V SUPPLY



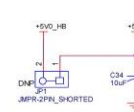
## VAA 2.8V SUPPLY



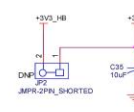
## VAA-PIX 2.8V SUPPLY



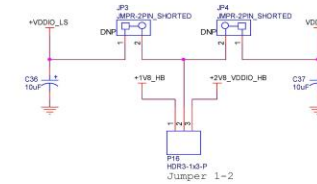
## PERIPHERAL 5V SUPPLY



## PERIPHERAL 3.3V SUPPLY

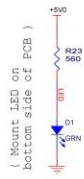


## VDDIO & VDDIO LS 1.8V/2.8V SUPPLY

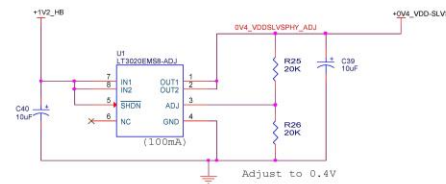


+5V0_HB	+5V0_HB	8
+3V3_HB	+3V3_HB	6
+2V8_VAA_HB	+2V8_VAA_HB	6
+2V8_VDDIO_HB	+2V8_VDDIO_HB	6
+1V8_HB	+1V8_HB	6
+1V2_HB	+1V2_HB	6
+5V0	+5V0	3
+3V3	+3V3	3,5
+VDDIO_LS	+VDDIO_LS	5,8
VDD	VDD	3
VDD-IO	VDD-IO	3
VDD-SLVS	VDD-SLVS	3
VDD-PLL	VDD-PLL	3
VAA	VAA	3
VAA-PIX	VAA-PIX	3

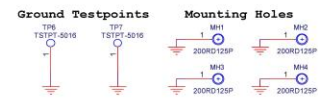
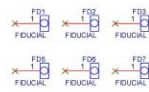
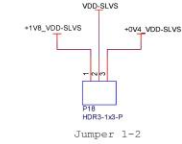
## 5V LED



## VDDSLVSPHY 0.4V SUPPLY



Selection of 0.4V or 1.2V/1V8 for VDDSLVSPHY supply

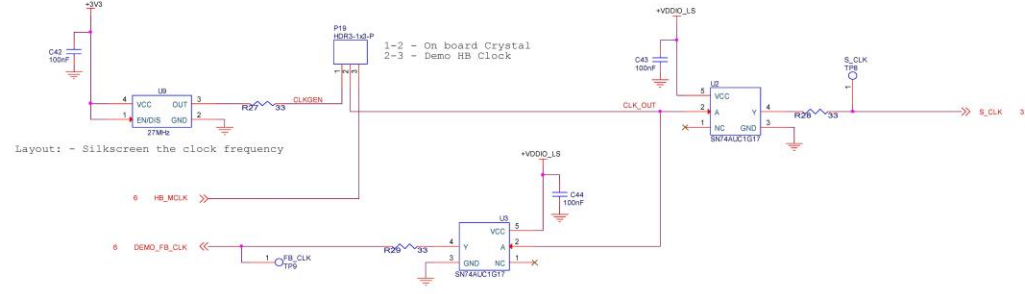




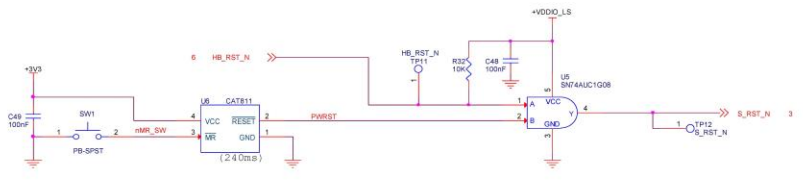
# Clock and Reset

+5V0	4	+5V0	3,4
+3V3	3,4	+3V3	3,4
+VDD0_L5	4,8	+VDD0_L5	4,8

## CLOCK CIRCUIT



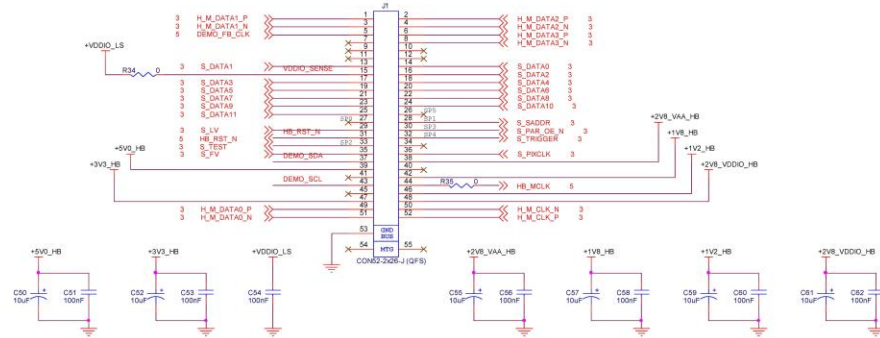
## RESET CIRCUIT



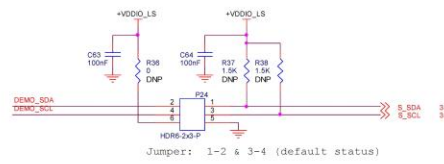
# External Interface

+5V0_HB	4	+5V0_HB	4
+5V0_HB	4	+2V8_HB	4
+2V8_VAA_HB	4	+3V0_VAA_HB	4
+2V8_VDDIO_HB	4	+2V8_VDDIO_HB	4
+1V2_HB	4	+1V2_HB	4
+1V2_HB	4	+1V2_HB	4
+3V3	3,4,5	+3V3	3,4,5
+VDDIO_LS	4,5	+VDDIO_LS	4,5

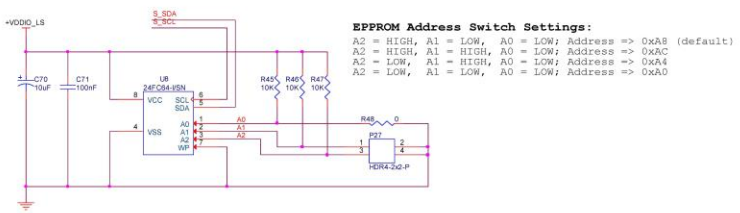
## DEMO3 BASEBOARD I/F



## I2C DEBUG



## LENS CORRECTION EEPROM



**EEPROM Address Switch Settings:**  
 A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)  
 A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xA9  
 A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4  
 A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0