CYW20733

Single-Chip Bluetooth Transceiver Wireless Input Devices

The Cypress CYW20733 is a Bluetooth 3.0 + EDR compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. The device is ideal for applications in wireless input devices including game controllers, keyboards, and joysticks. Built-in firmware adheres to the Bluetooth Human Interface Device (HID) profile and Bluetooth Device ID profile specifications. The CYW20733 radio has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification 3.0 + EDR. The single-chip Bluetooth transceiver is a monolithic component implemented in a standard digital CMOS process and requires minimal external components to make a fully compliant Bluetooth device. The CYW20733 is available in three package options: a 81-pin, 8 mm × 8 mm FBGA, a 121-pin, 9 mm × 9 mm FBGA, and a 56-pin, 7 mm x 7 mm QFN.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20733	CYW20733
BCM20733A3KFB1G	CYW20733A3KFB1G
BCM20733A3KFB2G	CYW20733A3KFB2G
BCM20733A3KML1G	CYW20733A3KML1G

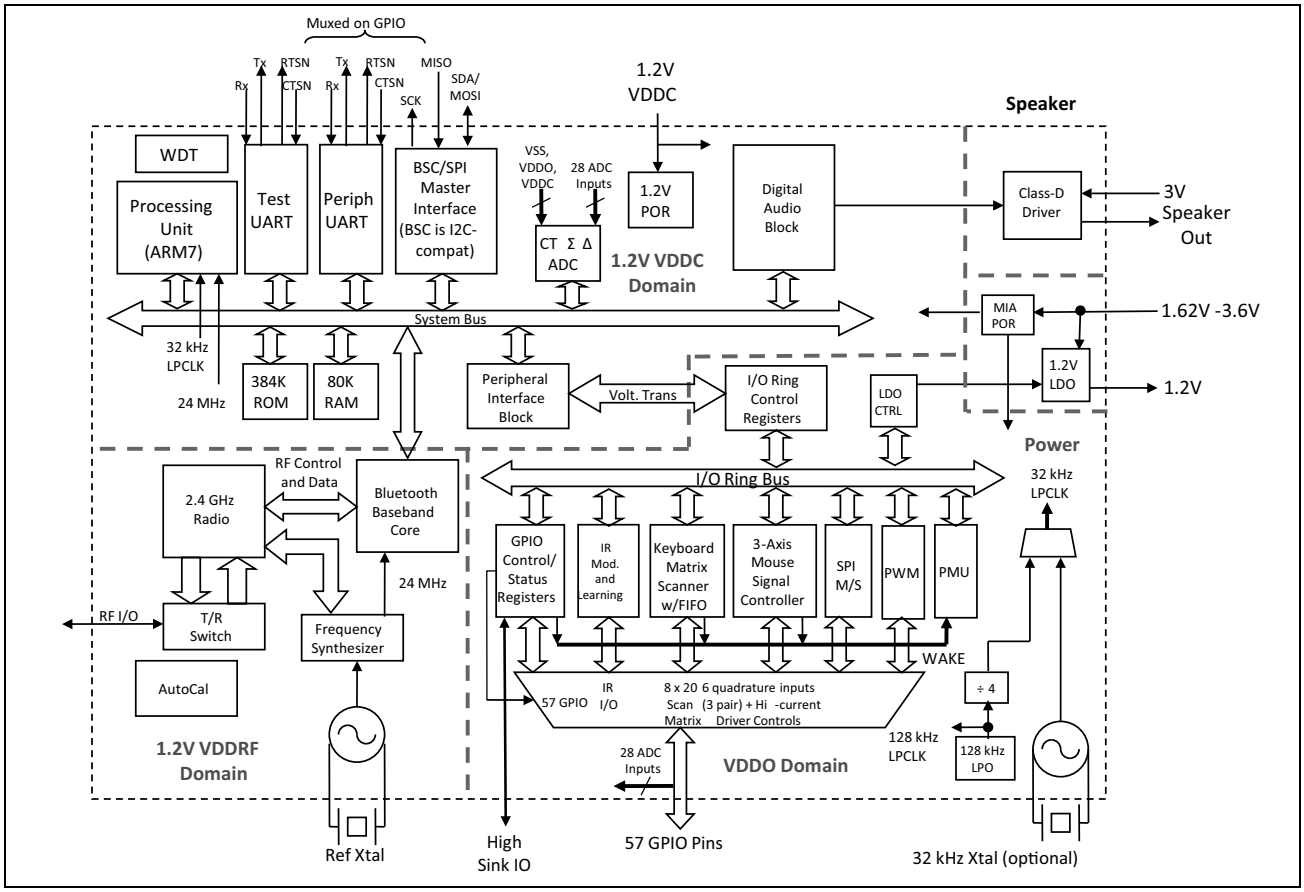
Features

- Integrated LDO to reduce BOM cost
- Bluetooth specification 3.0 + EDR compatible
- Bluetooth HID profile version 1.1 compliant
- Bluetooth Device ID profile version 1.3 compliant
- Supports AFH
- Excellent receiver sensitivity
- On-chip support for common keyboard and mouse interfaces eliminates external processor
- Infrared (IR) modulator
- IR learning
- Integrated 200 mW filterless Class-D audio amplifier
- Triac control
- Triggered Broadcom Fast Connect
- One I/O capable of sinking 100 mA for high- current drive applications
- Programmable key scan matrix interface, up to 8 × 20 key-scanning matrix
- Three-axis quadrature signal decoder
- On-chip support for serial peripheral interface (master and slave modes)
- Broadcom Serial Communications Interface (compatible with Philips® I2C slaves)
- Two independent half-duplex PCM/I2S interfaces
- Real-time clock supported with 32.768 kHz oscillator
- Programmable output power control meets Class 2 or Class 3 requirements
- On-chip PA with a maximum output power of +10dBm without external component
- Integrated ARM7TDMI-S™-based microprocessor core
- On-chip power on reset (POR)
- On-chip software control power management unit
- Three package types available:
  - 81-pin FBGA package (8 mm × 8 mm)
  - 121-pin FBGA package (9 mm × 9 mm)
  - 56-pin QFN package (7 mm x 7 mm)
- RoHS compliant

Applications

- Game controllers
- Wireless pointing devices: mice, trackballs
- Wireless keyboards
- Joysticks
- Point-of-sale (POS) input devices
- Remote controls
- Home automation
- 3D glasses

Figure 1. Functional Block Diagram



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1. Functional Description

1.1 Integrated Radio Transceiver

The CYW20733 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low power, low cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification 3.0 + EDR and meets or exceeds the requirements to provide the highest communication link quality of service.

1.1.1 Transmitter Path

The CYW20733 features a fully integrated zero IF transmitter. The baseband transmit data is GFSK modulated in the modem block and upconverted to the 2.4 GHz ISM band. The transmit path consists of signal filtering, I/Q upconversion, output power amplification, and RF filtering. It also incorporates the π/4-DQPSK and 8-DPSK modulation schemes, which support the 2 Mbps and 3 Mbps enhanced data rates, respectively.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signals. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Power Amplifier

The integrated power amplifier (PA) for the CYW20733 can transmit at a maximum power of +4 dBm for class 2 operation. The transmit power levels are for basic rate and EDR. Due to the linear nature of the PA, combined with some integrated filtering, no external filters are required for meeting Bluetooth and regulatory harmonic and spurious requirements.

The CYW20733 internal PA can deliver a maximum output power of +10 dBm for basic rate and +8 dBm for EDR with a flexible supply range of 2.5V to 3.0V.

1.1.2 Receiver Path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW20733 to be used in most applications without off-chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYW20733 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

1.1.3 Local Oscillator

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW20733 uses an internal RF and IF loop filter.

1.1.4 Calibration

The CYW20733 radio transceiver features an automated calibration scheme that is self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration will optimize the gain and phase performance of all the major blocks within the radio to within 2% of optimal conditions. Calibrated blocks include filters, the matching networks between key components, and key gain blocks. The calibration process corrects for both process and temperature variations. It occurs transparently during normal operation and the setting time of the hops and will calibrate for temperature variations as the device cools and heats during normal operation in its environment.

1.1.5 Internal LDO Regulator

To reduce the external BOM, the CYW20733 has an integrated 1.2V LDO regulator to provide power to the digital and RF circuits and system components. The 1.2V LDO regulator operates from a 1.62V to 3.63V input supply with a 60 mA maximum load current.

In noisy environments, a ferrite bead may be needed between the digital and RF supply pins to isolate noise coupling and suppress noise into the RF circuits.

Note: Always place the decoupling capacitors near the pins as close together as possible.

1.2 Microprocessor Unit

The CYW20733 microprocessor unit (µPU) runs software from the link control (LC) layer up to the Human Interface Device (HID). The microprocessor is based on an ARM7™ 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The µPU has 320 KB of ROM for program storage and boot-up, 80 KB of RAM for scratch-pad data, and patch RAM code.

The internal boot ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations, including UART, and with an external serial EEPROM or with an external flash memory. At power-up, the lower layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device can also support the integration of user applications.

1.2.1 EEPROM Interface

The CYW20733 provides the BSC (Broadcom Serial Control) master interface; the BSC is programmed by the CPU to generate four different types of BSC transfers on the bus: read-only, write-only, combined read/write, and combined write/read. BSC supports both low-speed and fast mode devices. The BSC is compatible with a Philips® I^2C slave device, except that master arbitration (multiple I^2C masters contending for the bus) is not supported. Native support for Microchip® 24LC128, Microchip 24AA128, and STMicroelectronics® M24128-BR is included.

The EEPROM can contain customer application configuration information, including: application code, configuration data, patches, pairing information, BD_ADDR, baud rate, SDP service record, and file system information used for code.

1.2.2 Serial Flash Interface

The CYW20733 includes an SPI master controller that can be used to access serial flash memory. The SPI master contains an AHB slave interface, transmit and receive FIFOs, and the SPI core PHY logic.

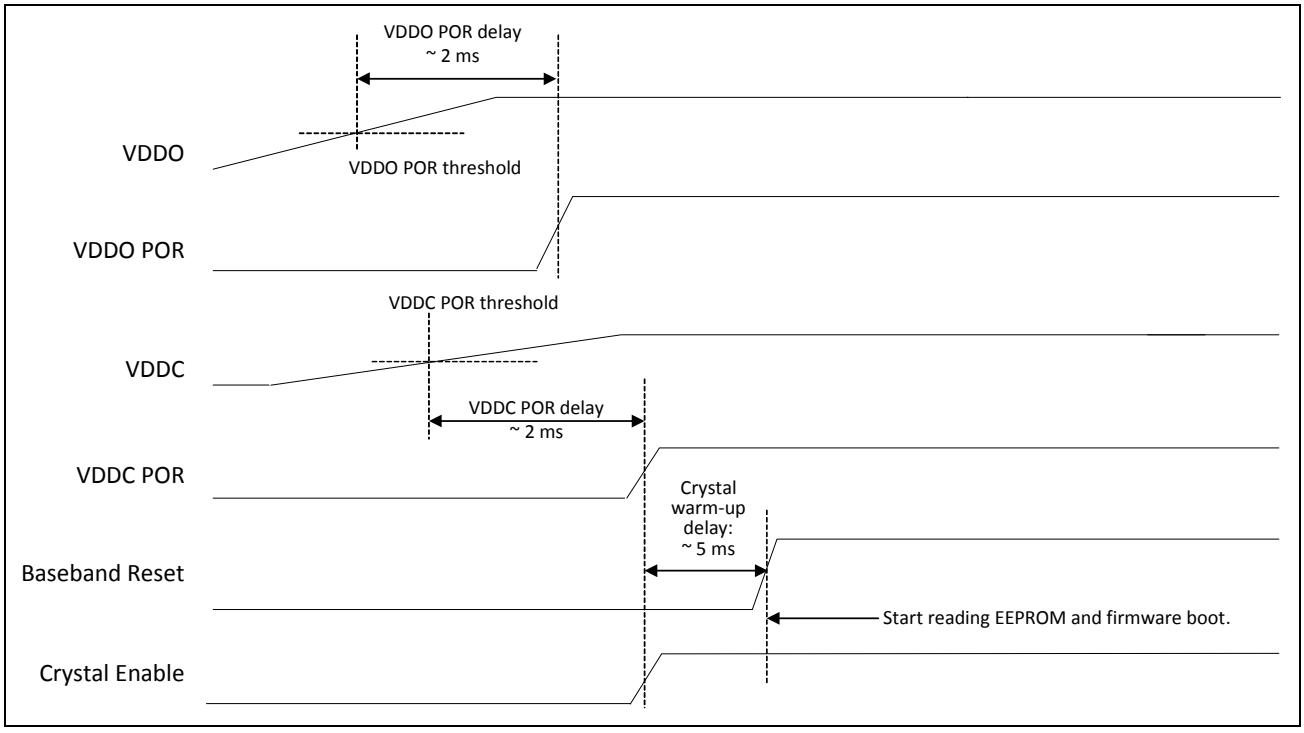
Devices natively supported include the following:

- Atmel® AT25BCM512B
- MXIC MX25V512ZUI-20G

1.2.3 Internal Reset

The CYW20733 has an integrated power-on reset circuit that resets all circuits to a known power-on state.

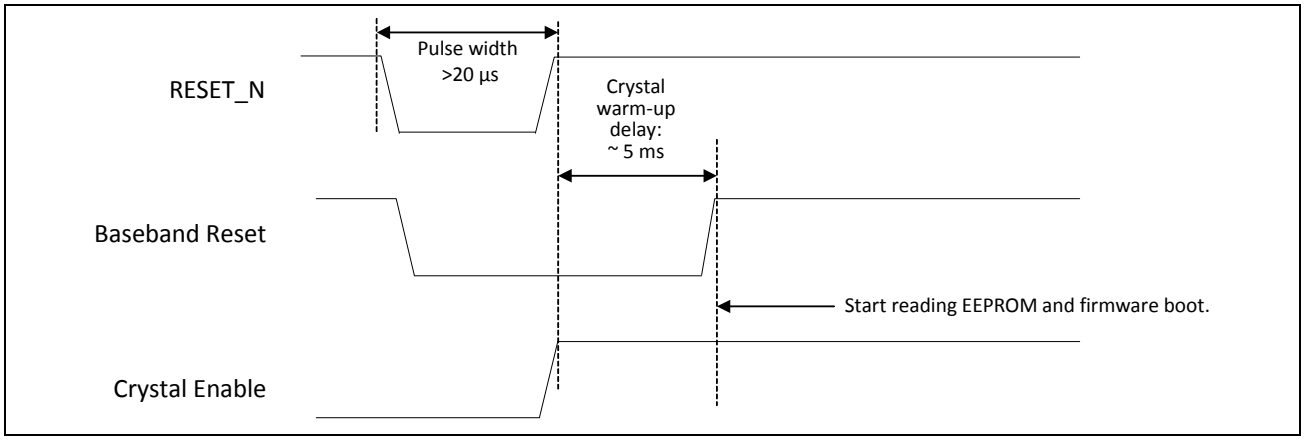
Figure 1. Internal Reset Timing



1.2.4 External Reset

An external active-low reset signal, RESET_N, can be used to put the CYW20733 in the reset state. The RESET_N pin has an internal pull-up resistor and, in most applications, it does not require that anything be connected to it. RESET_N should only be released after the VDDO supply voltage level has been stabilized.

Figure 2. External Reset Timing



1.3 Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Receive Functions: Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data de-whitening.
- Transmit Functions: Data framing, FEC generation, HEC generation, CRC generation, link key generation, data encryption, and data whitening.

1.3.1 Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number depending on the link controller state, Bluetooth clock, and the device address.

1.3.2 E0 Encryption

The encryption key and the encryption engine are implemented using dedicated hardware to reduce software complexity and provide minimal intervention.

1.3.3 Link Control Layer

The Link Control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the command controller, which takes commands from the software, and other controllers that are activated or configured by the command controller to perform the link control tasks. Each task performs in a different state in the Bluetooth link controller. STANDBY and CONNECTION are the two major states. In addition, there are five substates: page, page scan, inquiry, inquiry scan, and sniff.

1.3.4 Adaptive Frequency Hopping

The CYW20733 gathers link quality statistics on a channel-by-channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

1.3.5 Bluetooth Version 3.0 Features

The CYW20733 is fully compliant with the Bluetooth 3.0 standard, including the following options:

- Enhanced power control
- HCI read, encryption key size command

The CYW20733 supports all of the new Bluetooth version 2.1 features:

- Extended inquiry response
- Sniff subrating
- Encryption pause and resume
- Secure simple pairing
- Link supervision timeout changed event
- Erroneous data reporting
- Non-automatically flushable packet boundary flag
- Security Mode 4

1.3.6 Test Mode Support

The CYW20733 fully supports Bluetooth Test Mode, as described in Part 1 of the Bluetooth System Version 2.1 specification. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth test mode, the device supports enhanced testing features to simplify RF debugging and qualification and type approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
- Simplified type approval measurements (Japan)
- Aid in transmitter performance analysis
- Fixed frequency constant receiver mode
- Receiver output directed to I/O pin
- Direct BER measurements using standard RF test equipment
- Facilitated spurious emissions testing for receive mode
- Fixed frequency constant transmission
- 8-bit fixed pattern or PRBS-9
- Modulated signal measurements with standard RF test equipment
- Connectionless transmitter test
- Hopping or fixed frequency
- Multiple packet types
- Multiple data patterns
- Connectionless receiver test

1.4 Peripheral Transport Unit (PTU)

1.4.1 Broadcom Serial Control Interface

The CYW20733 provides a 2-pin master BSC interface that can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I^2C slave devices. The BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

Listed below are the transfer clock rates supported by the BSC:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I^2C-compatible speed.)

- 4 MHz maximum (Compatibility with high-speed I^2C-compatible devices is not guaranteed.)

The following transfer types are supported by the BSC:

- Read (up to 127 bytes can be read)
- Write (up to 127 bytes can be written)
- Read-then-Write (Up to 127 bytes can be read, and up to 127 bytes can be written.)
- Write-then-Read (Up to 127 bytes can be written, and up to 127 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYW20733 are required on both SCL and SDA for proper operation.

1.4.2 UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 1.5 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYW20733 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth 3.0 UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock is 24 MHz. The baud rate of the CYW20733 UART is controlled by two values. The first is a UART clock divisor (also called the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (also called the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

When setting the baud rate manually, the UART clock divisor is an 8-bit value that is stored as 256 minus the chosen divisor. For example, a divisor of 13 is stored as 256 – 13 = 243 = 0xF3.

The baud rate adjustment is also an 8-bit value, of which the four MSBs are the number of additional clock cycles to insert in the first half of each bit time, and the four LSBs are the number of clock cycles to insert in the second half of each bit time. If either of these two values is over eight, it is rounded to eight.

To compute the baud rate, the calculation is expressed as:

24 MHz ÷ ((16 × UART clock divisor) + total inserted 24-MHz clock cycles)

Table 2 contains example values to generate common baud rates.

Table 2. Common Baud Rate Examples

Desired Baud Rate (bps)	UART Clock Divisor	Baud Rate Adjustment		Actual Baud Rate (bps)	Error (%)
		High Nibble	Low Nibble		
1500000	0xFF	0x00	0x00	1500000	0.00
921600	0xFF	0x05	0x05	923077	0.16
460800	0xFD	0x02	0x02	461538	0.16
230400	0xFA	0x04	0x04	230769	0.16
115200	0xF3	0x00	0x00	115385	0.16
57600	0xE6	0x00	0x00	57692	0.16
38400	0xD9	0x01	0x00	38400	0.00
28800	0xCC	0x00	0x00	28846	0.16
19200	0xB2	0x01	0x01	19200	0.00
14400	0x98	0x00	0x00	14423	0.16
9600	0x64	0x02	0x02	9600	0.00

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYW20733 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

Peripheral UART Interface

The CYW20733 has a second UART that may be used to interface to other peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin as shown in Table 3.

Table 3. CYW20733 Peripheral UART

Pin Name	pUART_TX	pUART_RX	pUART_CTS_N	pUART_RTS_N
Configured pin name	P0	P2	P3	P1
	P5	P4	P7	P6
	P24	P25	P35	P30
	P31	P33	–	–
	P32	P34	–	–

1.5 PCM Interface

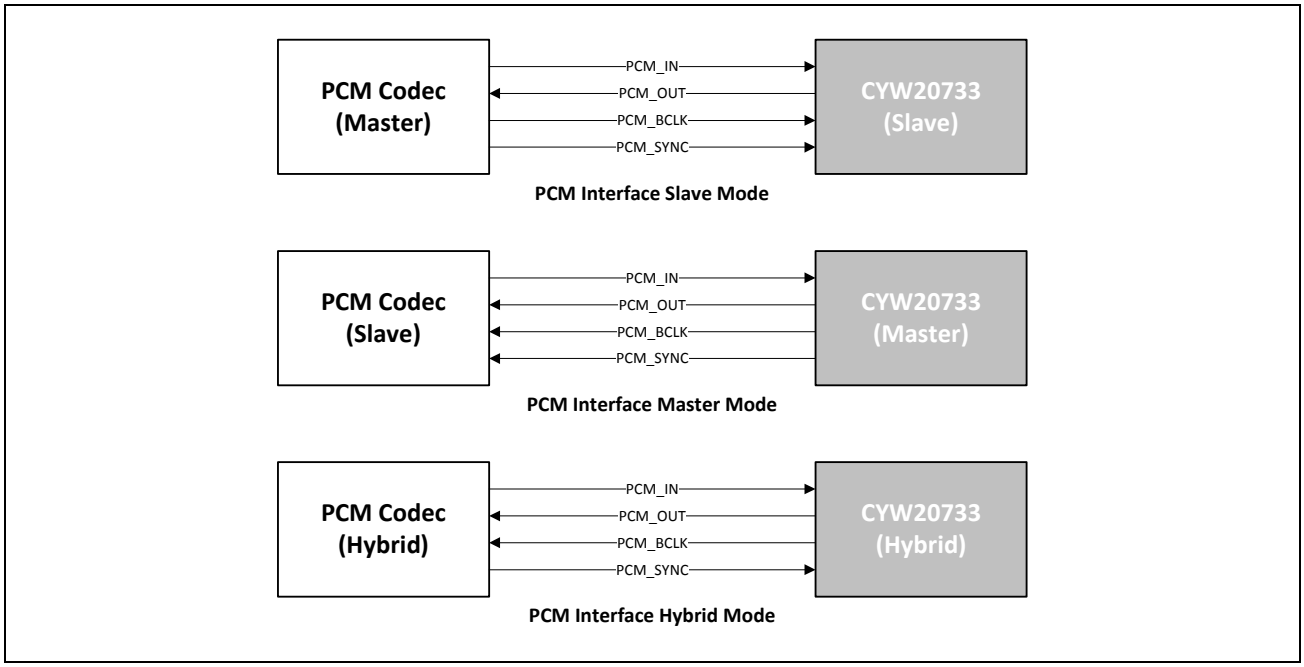
The CYW20733 PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, the device generates the PCM_BCLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface as inputs to the device.

The channels can be configured to either transmit or receive, but they must be assigned to different time slots. The two half-duplex channels cannot be combined to form a single full-duplex channel.

1.5.1 System Diagram

Figure 3 shows options for connecting the device to a PCM codec device as a master or a slave.

Figure 3. PCM Interface with Linear PCM Codec



1.5.2 Slot Mapping

Table 4. PCM Interface Time-Slotting Scheme

Audio Sample Rate	Time-Slotting Scheme
8 kHz	The number of slots depends on the selected interface rate, as follows: Interface rate Slot 1281 2562 5124 10248 204816
16 kHz	The number of slots depends on the selected interface rate, as follows: Interface rate Slot 2561 5122 10244 20488

The PCM data output driver tri-states its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

1.5.3 Frame Synchronization

The device supports both short and long frame synchronization types in both master and slave configurations. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate (which is a single bit period in width) and synchronized to the rising edge of the bit clock. The PCM slave expects PCM_SYNC to be high on the falling edge of the bit clock and the first bit of the first slot to start at the next rising edge of the clock. In the long frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate. However, the duration is 3-bit periods, and the pulse starts coincident with the first bit of the first slot.

1.5.4 Data Formatting

The device can be configured to generate and accept several different data formats. The device uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits is configurable to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with zeros, ones, a sign bit, or a programmed value on the output. The default format is 13-bit two's complement data, left justified, and clocked most significant bit first.

1.6 I²S Interface

The I²S interface supports up to two half-duplex channels. The channels can be configured to either transmit or receive, but they must be assigned to different time slots (left or right). The two half-duplex channels cannot be combined to form a single full-duplex channel. The I²S interface is capable of operating in either slave or master mode. The device supports a 16-bit data width with 8-kHz and 16-kHz frame rates.

1.7 Clock Frequencies

The CYW20733 is set with a crystal frequency of 24 MHz.

1.7.1 Crystal Oscillator

The crystal oscillator requires a crystal with an accuracy of ±20 ppm as defined by the Bluetooth specification. Two external load capacitors in the 5 pF to 30 pF range are required to work with the crystal oscillator. The selection of the load capacitors is crystal dependent. Table 5 shows the recommended crystal specification.

Figure 4. Recommended Oscillator Configuration—12 pF Load Crystal

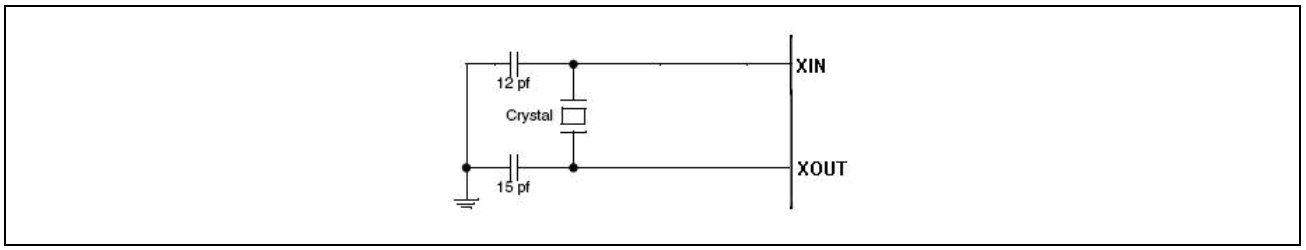


Table 5. Reference Crystal Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input signal amplitude	–	400	–	2000	mVp-p
Nominal frequency	–	–	24.000	–	MHz
Oscillation mode	–	Fundamental			–
Frequency tolerance	@25°C	–	±10	–	ppm
Tolerance stability over temp	@0°C to +70°C	–	±10	–	ppm
Equivalent series resistance	–	–	–	50	Ω
Load capacitance	–	–	12	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	µW
Aging	–	–	–	±10	ppm/year
Shunt capacitance	–	–	–	2	pF

HID Peripheral Block

The peripheral blocks of the CYW20733 all run from a single 128-kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If a peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case in that it may drop its clock request line even when enabled and then reassert the clock request line if a key-press is detected.

Real-Time Clock and 32 kHz Crystal Oscillator

The CYW20733 has a 48-bit counter that can be configured to be clocked directly from a 32.768 kHz or 32.000 kHz crystal oscillator. The real-time clock counter value is accessible via firmware.

Figure 5 shows the 32 kHz crystal (XTAL) oscillator with external components, and Table 6 lists the oscillator's characteristics. It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is ~100 mV. This circuit can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at a similar frequency. The default component values are: R1 = 10 MΩ, C1 = C2 = ~10 pF. The values of C1 and C2 are used to fine-tune the oscillator.

Figure 5. 32-kHz Oscillator Block Diagram

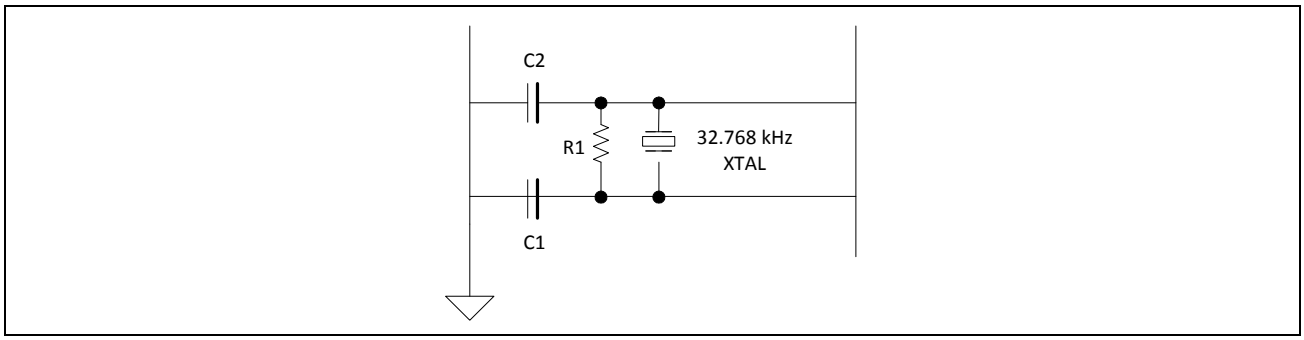


Table 6. XTAL Oscillator Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	–	500	ms
XTAL drive level	P_{drv}	For crystal selection	0.5	–	–	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	1.3	pF

1.8 GPIO Port

The CYW20733 has 40 general-purpose I/Os (GPIOs) in the 81-pin package and 58 GPIOs in the 121-pin package. All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3V or 4 mA at 1.8V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3V or 8 mA at 1.8V. GPIO P57 is capable of sinking 100 mA for VDDIO = 3.0V and 60 mA for VDDIO = 1.62V.

Port 0–Port 1, Port 8–Port 18, Port 20–Port 23, and Port 28–Port 38

All of these pins can be programmed as ADC inputs.

Port 26–Port 29

P[26:29] consist of four pins. All pins are capable of sinking up to 16 mA for LEDs. These pins also have the PWM function, which can be used for LED dimming.

1.9 Keyboard Scanner

The keyboard scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene. The scanner has the following features:

- Ability to turn off its clock if no keys are pressed.
- Sequential scanning of up to 160 keys in an 8 × 20 matrix.
- Programmable number of columns from 1 to 20.
- Programmable number of rows from 1 to 8.
- 16-byte key-code buffer (can be augmented by firmware).
- 128 kHz clock—allows scanning of full 160-key matrix in about 1.2 ms.
- N-key rollover with selective 2-key lockout if ghost is detected.
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs.

- Hardware debouncing and noise/glitch filtering.
- Low-power consumption. Single-digit µA-level sleep current.

1.9.1 Theory of Operation

The key scan block is controlled by a state machine with the following states:

Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128 kHz clock to be enabled (if it is not already enabled by another peripheral) and the state machine to enter the scan state. Also in this state, an 8-bit row-hit register and an 8-bit key-index counter is reset to 0.

Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. After the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row and column counters are both at their respective terminal count values. At that point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This counter is the value compared to the modifier key codes stored, or in the key-code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a lookup table of usage codes.

Also, as the *n*th row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains two or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in the status register is set to indicate this.

Scan End

This state determines whether any keys were detected while in the scan state. If yes, the state machine returns to the scan state. If no, the state machine returns to the idle state, and the 128 kHz clock request signal is made inactive.

The microcontroller can poll the key status register.

1.10 Mouse Quadrature Signal Decoder

The mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by an optomechanical mouse. The decoder has the following features:

- Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals. Each axis has two options:
  - For the X axis, choose P2 or P32 as X0 and P3 or P33 as X1.
  - For the Y axis, choose P4 or P34 as Y0 and P5 or P35 as Y1.
  - For the Z axis, choose P6 or P36 as Z0 and P7 or P37 as Z1.
- Control of up to four external high-current GPIOs to power external optoelectronics:
  - Turn-on and turn-off time can be staggered for each HC-GPIO to avoid simultaneous switching of high currents and having multiple high-current devices on at the same time.
  - Sample time can be staggered for each axis.
  - Sense of the control signal can be active high or active low.
  - Control signal can be tristated for off condition or driven high or low, as appropriate.

1.10.1 Theory of Operation

The mouse decoder block has four 10-bit PWMs for controlling external quadrature devices and sampling the quadrature inputs at its core.

The GPIO signals may be used to control such items as LEDs, external ICs that may emulate quadrature signals, photodiodes, and photodetectors.

1.11 ADC Port

The CYW20733 contains a 16-bit ADC.

Additionally:

- There are 28 analog input channels. All channels are multiplexed on various GPIOs.
- There is a built-in reference with bandgap-based reference modes.
- The maximum conversion rate is 187 kHz.
- There is a rail-to-rail input swing.

The ADC consists of an analog ADC core that performs the actual analog-to-digital conversion and digital hardware that processes the output of the ADC core into valid ADC output samples. Directed by the firmware, the digital hardware also controls the input multiplexers that select the ADC input signal (V_{inp}) and the ADC reference signals (V_{ref}).

Table 7. Sampling Rate and Effective Number of Bits

Mode	Effective Number of Bits (ENOB)		Sampling Rate (kHz)	Latency[a] (µs)
	Minimum	Typical		
0	10.4	13.0	5.859	171
1	10.2	12.6	11.7	85
2	9.7	12.0	46.875	21
3	9.3	11.5	93.75	11
4	7.9	10.0	187	5

a. Settling time of the ADC and filter after switching channels.

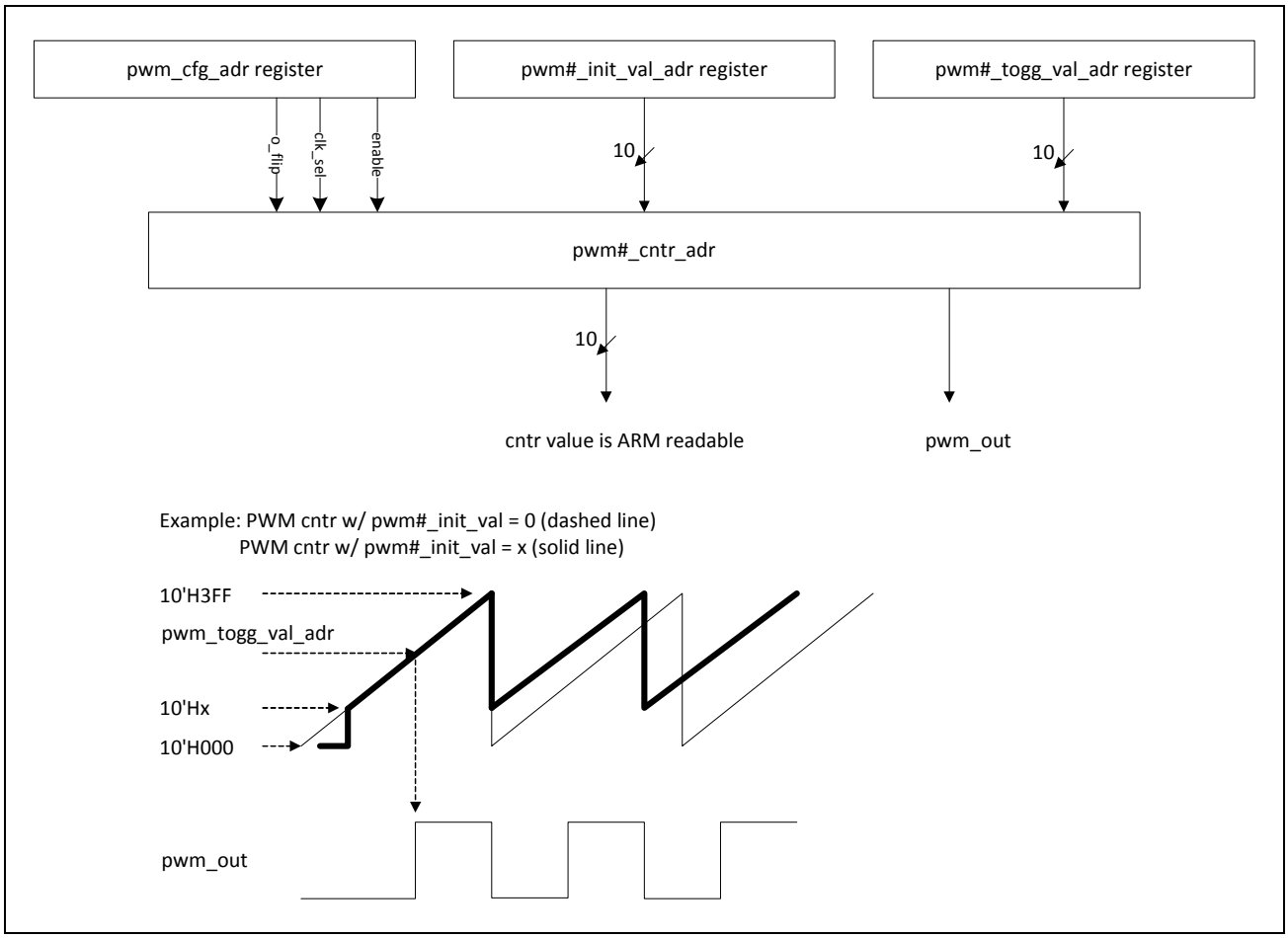
1.12 PWM

The CYW20733 has four internal PWMs. The PWM module consists of the following:

- PWM1–4
- Each of the four PWM channels, PWM1–4, contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- PWM configuration register shared among PWM1–4 (read/write). This 12-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 6 on page 15 shows the structure of one PWM.

Figure 6. PWM Block Diagram



1.13 Serial Peripheral Interface

The CYW20733 has two independent SPI interfaces. One is a master-only interface (SPI_1) and the other (SPI_2) can be either a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYW20733 has optional I/O ports that can be configured individually and separately for each functional pin, as shown in Table 8. The CYW20733 acts as an SPI master device that supports 1.8V or 3.3V SPI slaves. The CYW20733 can also act as an SPI slave device that supports a 1.8V or 3.3V SPI master.

Note: SPI voltage depends on VDDO/VDDM; therefore, it defines the type of devices that can be supported.

Table 8. CYW20733 First SPI Set (Master Mode)

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS[a]
Configured Pin Name	SCL	SDA	P24	–
	–	–	P26	–
	–	–	P32[b]	P33[b]
	–	–	P39	–

a. Any GPIO can be used as SPI_CS when SPI is in master mode.

b. Default for serial flash.

Table 9. CYW20733 Second SPI Set (Master Mode)

Configuration	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS[a]
1	p3	p0	p1	–
2	p3	p0	p5	–
3	p3	p4	p1	–
4	p3	p4	p5	–
5	p3	p27	p1	–
6	p3	p27	p5	–
7	p3	p38	p1	–
8	p3	p38	p5	–
9	p7	p0	p1	–
10	p7	p0	p5	–
11	p7	p4	p1	–
12	p7	p4	p5	–
13	p7	p27	p1	–
14	p7	p27	p5	–
15	p7	p38	p1	–
16	p7	p38	p5	–
17	p24	p0	p25	–
18	p24	p4	p25	–
19	p24	p27	p25	–
20	P24	P38	P25	–
21	p36	p0	p25	–
22	p36	p4	p25	–
23	p36	p27	p25	–
24	P36	P38	p25	–

a. Any GPIO can be used as SPI_CS when SPI is in master mode.

Table 10. CYW20733 Second SPI Set (Slave Mode)

Configuration	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS
1	p3	p0	p1	p6
2	p3	p0	p1	p2
3	p3	p0	p5	p6
4	p3	p0	p5	p2
5	p3	p0	p25	p6
6	p3	p0	p25	p2
7	p3	p4	p1	p6
8	p3	p4	p1	p2
9	p3	p4	p5	p6
10	p3	p4	p5	p2
11	p3	p4	p25	p6
12	p3	p4	p25	p2
13	p7	p0	p1	p2
14	p7	p0	p1	p6
15	p7	p0	p5	p6
16	p7	p0	p5	p2
17	p7	p0	p25	p2
18	p7	p0	p25	p6
19	p7	p4	p1	p6
20	p7	p4	p1	p2
21	p7	p4	p5	p6
22	p7	p4	p5	p2
23	p7	p4	p25	p2
24	p7	p4	p25	p6
25	p24	p27	p1	p26
26	p24	p27	p1	p32
27	p24	p27	p1	p39
28	p24	p27	p5	p26
29	p24	p27	p5	p32
30	p24	p27	p5	p39
31	P24	P27	P25	P26
32	p24	p27	p25	p32
33	P24	P27	P25	P39
34	p24	p33	p1	p26
35	p24	p33	p1	p32
36	p24	p33	p1	p39
37	p24	p33	p5	p26
38	p24	p33	p5	p32
39	p24	p33	p5	p39
40	P24	P33	P25	P26
41	p24	p33	p25	p32
42	P24	P33	P25	P39
43	p24	p38	p1	p26
44	p24	p38	p1	p32
45	p24	p38	p1	p39

Table 10. CYW20733 Second SPI Set (Slave Mode) (Cont.)

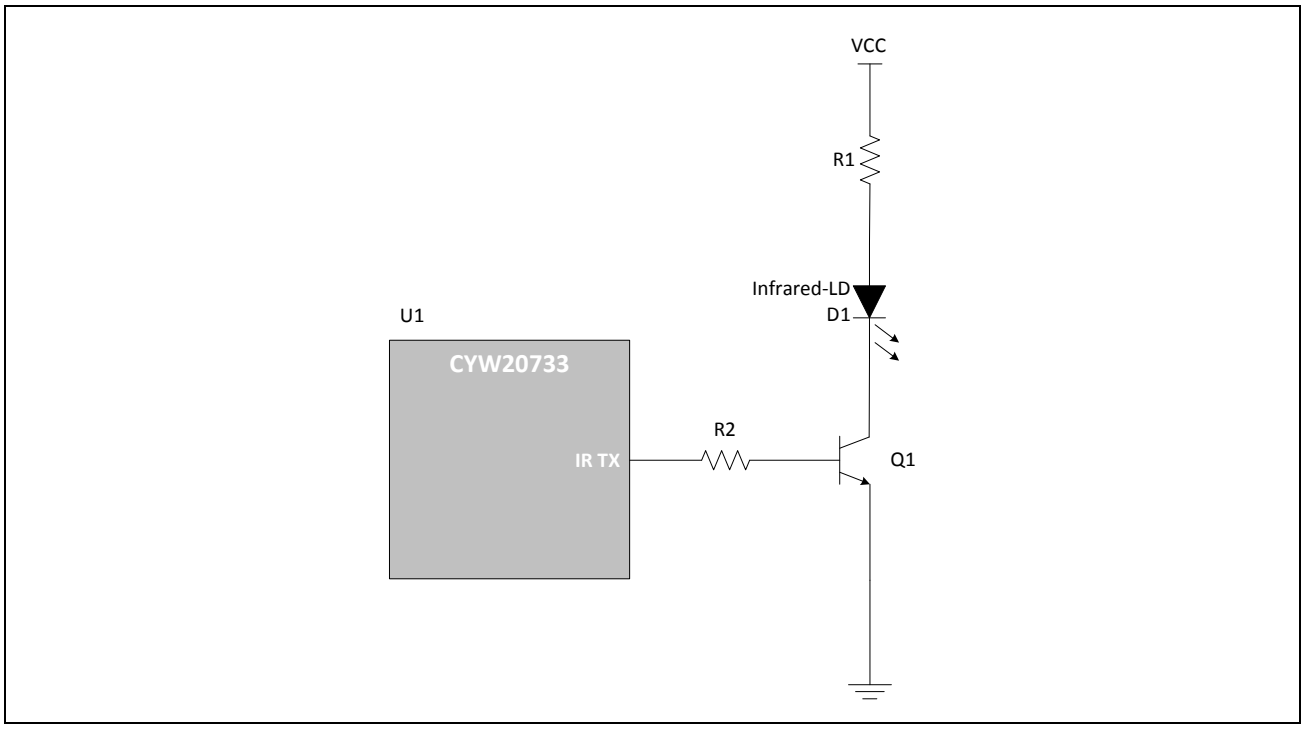
Configuration	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS
46	p24	p38	p5	p26
47	p24	p38	p5	p32
48	p24	p38	p5	p39
49	P24	P38	P25	P26
50	p24	p38	p25	p32
51	P24	P38	P25	P39
52	p36	p27	p1	p26
53	p36	p27	p1	p32
54	p36	p27	p1	p39
55	p36	p27	p5	p26
56	p36	p27	p5	p32
57	p36	p27	p5	p39
58	P36	P27	P25	P26
59	p36	p27	p25	p32
60	P36	P27	P25	P39
61	p36	p33	p1	p26
62	p36	p33	p1	p32
63	p36	p33	p1	p39
64	p36	p33	p5	p26
65	p36	p33	p5	p32
66	p36	p33	p5	p39
67	P36	P33	P25	P26
68	p36	p33	p25	p32
69	P36	P33	P25	P39
70	p36	p38	p1	p26
71	p36	p38	p1	p32
72	p36	p38	p1	p39
73	p36	p38	p5	p26
74	p36	p38	p5	p32
75	p36	p38	p5	p39
76	P36	P38	P25	P26
77	p36	p38	p25	p32
78	P36	P38	P25	P39

1.14 Infrared Modulator

The CYW20733 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767 µsec. The CYW20733 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without an underrun glitch. See Figure 7.

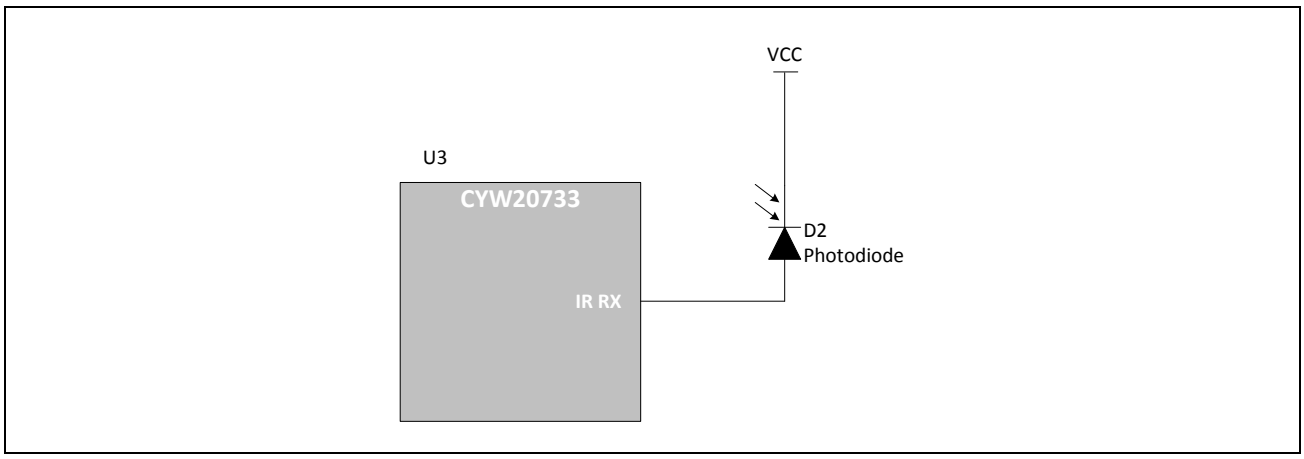
Figure 7. Infrared TX



1.15 Infrared Learning

The CYW20733 includes hardware support for infrared learning. The hardware can detect both modulated and unmodulated signals. For modulated signals, the CYW20733 can detect carrier frequencies between 10–500 kHz and the duration that the signal is present or absent. The CYW20733 firmware driver supports further analysis and compression of a learned signal. A learned signal can then be played back through the CYW20733 IR TX subsystem. See Figure 8.

Figure 8. Infrared RX



1.16 Shutter Control for 3D Glasses

The CYW20733, combined with the CYW20702, provides full system support for 3D glasses on televisions. The CYW20702 gets frame synchronization signals from the TV, converts them into proprietary timing control messages, then passes the messages to the CYW20733. The CYW20733 uses these messages to synchronize the shutter control for the 3D glasses with the television frames.

The CYW20733 can provide up to four synchronized control signals for left and right eye shutter control. These four lines can output pulses with microsecond resolution for on and off timing. The total cycle time can be set for any period up to 65535 msec. The pulses are synchronized to each other for left and right eye shutters.

The CYW20733 seamlessly adjusts the timing of the control signals based on control messages from the CYW20702, ensuring that the 3D glasses remain synchronized to the TV display frame.

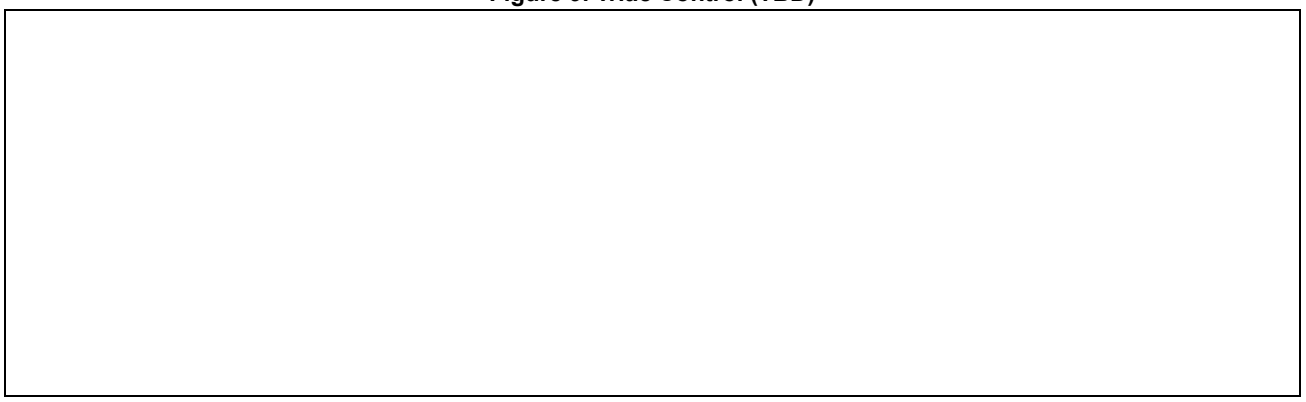
3D hardware control on the CYW20733 works independently of the rest of the system. The CYW20733 negotiates sniff with the CYW20702 and, except for sniff resynchronization periods, most of the CYW20733 circuitry remains in a low power state while the 3D glasses subsystem continues to provide shutter timing and control pulses. This significantly reduces total system power consumption.

1.17 Triac Control

The CYW20733 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYW20733 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the CYW20733 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches. See Figure .

Figure 9. Triac Control (TBD)



1.18 Cypress Proprietary Control Signalling and Triggered Broadcom Fast Connect

Cypress Proprietary Control Signaling (BPCS) and Triggered Broadcom Fast Connect (TBFC) are Cypress-proprietary baseband (ACL) suspension and low-latency reconnection mechanisms that reestablish the baseband connection with the peer controller that also supports BPCS/TBFC.

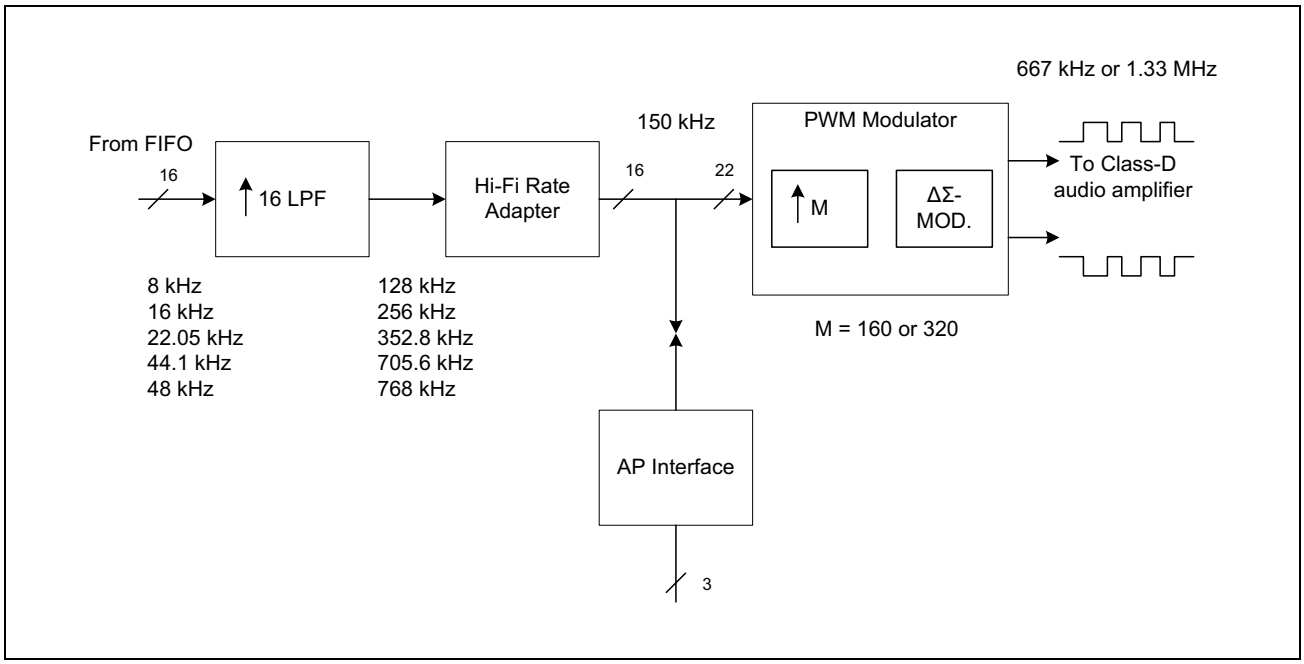
The CYW20733 uses BPCS primitives to allow a Human Interface Device (HID) to suspend all RF traffic after a configurable idle period with no reportable activity. To conserve power, it can then enter one of its low power states while still logically remaining connected at the L2CAP and HID layers with the peer device. When an event requires the HID to deliver a report to the peer device, the CYW20733 uses the TBFC and BPCS mechanisms to reestablish the baseband connection and immediately resume L2CAP traffic, greatly reducing latency between the event and delivery of the report to the peer device.

To achieve power savings and low latencies that cannot be achieved using long sniff intervals, certain applications may make use of the CYW20733 Broadcom Fast Connect (BFC) mechanism, which will eliminate the need to maintain an RF link, while still being able to establish ACL and L2CAP connections much faster than regular methods.

1.19 Integrated Filterless Class-D Audio Amplifier

The CYW20733 has an integrated speaker driver that includes both the digital path and an internal audio amplifier. The digital audio path includes a FIFO, LPF, rate adapter, and PWM modulator. The output of the PWM modulator drives an on-chip class-D high efficiency audio amplifier as shown in the figure below.

Figure 10. Class-D Block Diagram



The on-chip Class-D audio amplifier is designed to drive up to 200 mW into an 8Ω load and has a range of 20 Hz to 20 kHz, covering the entire audio spectrum. The amplifier is designed to deliver maximum dynamic range and power efficiency while minimizing quiescent current. The amplifier has two nonoverlapping switch drivers and a pair of MOSFET power switches for bridge-tie load. The digital Class-D modulator converts the audio input to a PWM signal that drives the switch driver. The modulator bitstream is retimed by a low-jitter 24/48 MHz clock at the input of the nonoverlapping switch drivers, used to prevent large crowbar currents during switching. A large W/L aspect ratio of the power transistor is used to minimize the on-resistance of the devices for improved efficiency.

The integrated audio amplifier requires a 3.0V regulated power supply. The required LDO characteristic is shown in Table 11.

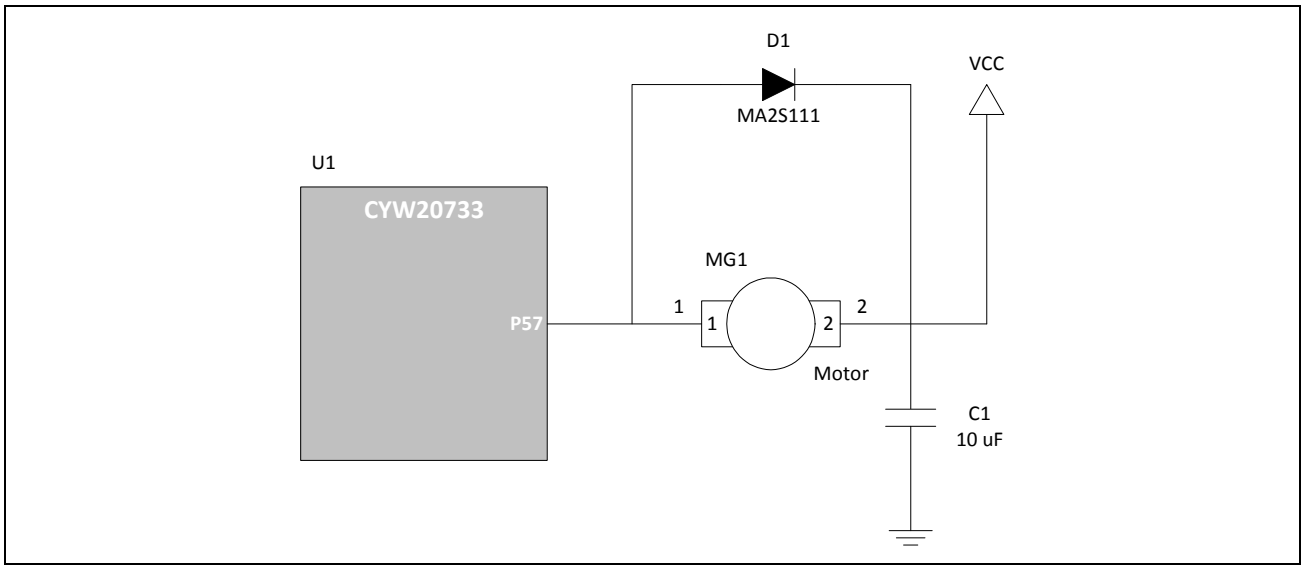
Table 11. LDO Requirement for the Integrated Audio Amplifier

Parameter	Condition	Minimum	Typical	Maximum	Unit
Output voltage	–	2.9	–	3.1	V
Output load current	–	–	–	200	mA rms
Load regulation	Vin = 2.9V and load current = 200 mA	–	–	40	mV
Power supply rejection ration (PSRR)	–	60	–	–	dB
Output impedance	–	–	–	20	mΩ
Output spot noise	At 1 kHz	–	–	1.5	µVrms/ sqrt (Hz)
Output noise	–	–	–	50	µVrms

1.20 High-Current I/O

The CYW20733 has one high-current I/O pin (GPIO P57) capable of sinking up to 100 mA with a maximum output voltage of 0.4V (VDDIO = 3.0V). For VDDIO = 1.62V, GPIO P57 is limited to sinking up to 60 mA. This pin can be used for LEDs, motors, or other high current devices. This pin can also be used as a GPIO if high current sink capability is not required. An example usage for driving a motor/vibrator is shown in Figure 11.

Figure 11. Motor/Vibrator Circuit



1.21 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet handling in the baseband core.

1.21.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver, which then processes the power-down functions accordingly.

1.21.2 Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in Deep-sleep mode.

1.21.3 BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection sniff mode. While in these low-power connection modes, the CYW20733 runs on the Low-Power Oscillator (LPO) and wakes up after a predefined time period.

The CYW20733 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Suspend mode
- Power-down mode
- HIDOFF mode

The CYW20733 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

HIDOFF mode is one of the power modes in which the core is powered down and only supervisory circuits running directly from the battery retain power.

2. Pin Assignments

Table 12. Pin Descriptions

Pin Number			Pin Name	I/O	Power Domain	Description
81-pin FBGA	121-pin FBGA	56-pin QFN				
Radio I/O						
D1	E1	9	RFP	I/O	VDDTF	RF antenna port
RF Power Supplies						
B1	C1	6	VDDIF	I	VDDIF	IFPLL power supply
E1	F1	11	VDDLNA	I	VDDLNA	RF front-end supply
F1	G1	12	VDDRF	I	VDDRF	VCO, LOGEN supply
G1	H1	13	VDDPX	I	VDDPX	RFPLL and crystal oscillator supply
C1	D1	7	VDDTF	I	VDDTF	PA supply
Power Supplies						
A3, J7	A2, L7	5	VDDC	I	VDDC	Baseband core supply
A7	B4, A8, E11	54	VDDO	I	VDDO	I/O pad and core supply
J6	L8	28	VDDM	I	VDDM	I/O pad supply
–	L3	–	VDD1P2	I	VDD1P2	Speaker differential clock conversion power supply
–	K10, L10	–	VDDSP	I	VDDSP	Speaker analog power supply
Ground						
C2, D2, E2, F2, G2, E3, F3, H3, J3, E4, E5, E6, E7	F8, H7, G7, F7, H6, G6, H5, G5, F5, H4, G4, J3, H3, G3, K2, J2, H2, G2, F2, E2, D2	Center paddle	VSS	I	VSS	Ground
–	K3	–	VSS1P2	I	–	Speaker differential clock conversion ground
–	J9, J10, J11	–	VSSSP	I	–	Speaker analog ground
Clock Generator and Crystal Interface						
J1	K1	16	XTALI	I	VDDRF	Crystal oscillator input. See “Crystal Oscillator” on page 10 for options.
J2	L1	15	XTALO	O	VDDPX	Crystal oscillator output.
–	C2	–	TP1	I	VDDPX	XTAL divide by 2. Connect to GND if main XTAL = 24 MHz.
H1	J1	14	RES	O	VDDPX	External calibration resistor, 15 kΩ at 1%
B4	A3	–	XTALI32K	I	VDDPX	Low-power oscillator (LPO) input. Alternate function: • P39 (FBGA-81 only)
D5	B3	–	XTALO32K	O	VDDPX	LPO output. Alternate function: • P38 (FBGA-81 only)
Core						
B2	C3	2	RESET_N	I/O PU	VDDO	Active-low system reset with open-drain output and internal pull-up resistor.
G3	B2	1	TMC	I	VDDO	Device test mode control. Connect to GND for all applications.
H2	L2	17	TMA	I	VDDM	ARM JTAG debug mode control. Connect to GND for all applications.
Speaker						
–	L11	–	AMPLP	O	VDDSP	Speaker driver positive output
–	K11	–	AMPLN	O	VDDSP	Speaker driver negative output

Table 12. Pin Descriptions (Cont.)

Pin Number			Pin Name	I/O	Power Domain	Description
81-pin FBGA	121-pin FBGA	56-pin QFN				
PCM2/I^{2}S						
G5	J8	24	PCM_SYNC	I/O, PD	VDDM	Frame synchronization for PCM interface. Alternate function: • I^{2}S word select
G4	J7	23	PCM_CLK	I/O, PD	VDDM	Clock for PCM interface. Alternate function: • I^{2}S clock
F4	K7	22	PCM_IN	I, PU	VDDM	Data input for PCM interface. Alternate function: • I^{2}S data input
F5	K8	25	PCM_OUT	O, PD	VDDM	Data output for PCM interface. Alternate function: • I^{2}S data output
UART						
J4	K6	20	UART_RXD	I	VDDM	UART serial input – Serial data input for the HCI UART interface.
J5	L6	21	UART_TXD	O, PU	VDDM	UART serial output – Serial data output for the HCI UART interface.
H4	L5	19	UART_RTS_N	O, PU	VDDM	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.
H5	K5	18	UART_CTS_N	I, PU	VDDM	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.
BSC						
H6	L9	26	SDA	I/O, PU	VDDM	Data signal for an external I^{2}C device. Alternate function: • SPI_1: MOSI (master only)
H7	K9	27	SCL	I/O, PU	VDDM	Clock signal for an external I^{2}C device. Alternate function: • SPI_1: SPI_CLK (master only)
LDO Regulator Power Supplies						
A2	A1	3	LDOIN	I	LDOIN	Battery input supply for the LDO
A1	B1	4	LDOOUT	O	LDOOUT	LDO output

Table 13. GPIO Pin Descriptions[a]

Pin Number			Pin Name	Default Direction	POR State	Power Domain	Alternate Function Description
81-pin FBGA	121-pin FBGA	56-pin QFN					
H8	H9	29	P0	Input	Floating	VDDO	• GPIO: P0 • Keyboard scan input (row): KSI0 • A/D converter input 29 • Peripheral UART: puart_tx • SPI_2: MOSI (master and slave) • IR_RX • 60Hz_main **Note:** Not available during TMC = 1.
J8	G9	31	P1	Input	Floating	VDDO	• GPIO: P1 • Keyboard scan input (row): KSI1 • A/D converter input 28 • Peripheral UART: puart_rts • SPI_2: MISO (master and slave) • IR_TX
J9	H10	30	P2	Input	Floating	VDDO	• GPIO: P2 • Keyboard scan input (row): KSI2 • Quadrature: QDX0 • Peripheral UART: puart_rx • SPI_2: SPI_CS (slave only)
H9	H11	32	P3	Input	Floating	VDDO	• GPIO: P3 • Keyboard scan input (row): KSI3 • Quadrature: QDX1 • Peripheral UART: puart_cts • SPI_2: SPI_CLK (master and slave)
G8	G10	34	P4	Input	Floating	VDDO	• GPIO: P4 • Keyboard scan input (row): KSI4 • Quadrature: QDY0 • Peripheral UART: puart_rx • SPI_2: MOSI (master and slave) • IR_TX
G9	F10	33	P5	Input	Floating	VDDO	• GPIO: P5 • Keyboard scan input (row): KSI5 • Quadrature: QDY1 • Peripheral UART: puart_tx • SPI_2: MISO (master and slave)
F8	F11	35	P6	Input	Floating	VDDO	• GPIO: P6 • Keyboard scan input (row): KSI6 • Quadrature: QDZ0 • Peripheral UART: puart_rts • SPI_2: SPI_CS (slave only) • 60Hz_main
F9	E10	36	P7	Input	Floating	VDDO	• GPIO: P7 • Keyboard scan input (row): KSI7 • Quadrature: QDZ1 • Peripheral UART: puart_cts • SPI_2: SPI_CLK (master and slave)
E8	D11	37	P8	Input	Floating	VDDO	• GPIO: P8 • Keyboard scan output (column): KSO0 • A/D converter input 27 • External T/R switch control: ~tx_pd

Table 13. GPIO Pin Descriptions[a] (Cont.)

Pin Number			Pin Name	Default Direction	POR State	Power Domain	Alternate Function Description
81-pin FBGA	121-pin FBGA	56-pin QFN					
E9	D10	38	P9	Input	Floating	VDDO	• GPIO: P9 • Keyboard scan output (column): KSO1 • A/D converter input 26 • External T/R switch control: tx_pd
D8	E9	39	P10	Input	Floating	VDDO	• GPIO: P10 • Keyboard scan output (column): KSO2 • A/D converter input 25 • External PA ramp control: ~PA_Ramp
D9	C11	41	P11	Input	Floating	VDDO	• GPIO: P11 • Keyboard scan output (column): KSO3 • A/D converter input 24
C9	C10	40	P12	Input	Floating	VDDO	• GPIO: P12 • Keyboard scan output (column): KSO4 • A/D converter input 23
C8	B11	43	P13	Input	Floating	VDDO	• GPIO: P13 • Keyboard scan output (column): KSO5 • A/D converter input 22 • External PA ramp control: ~PA_Ramp • Triac control 3
B9	B10	44	P14	Input	Floating	VDDO	• GPIO: P14 • Keyboard scan output (column): KSO6 • A/D converter input 21 • External T/R switch control: ~tx_pd • Triac control 4
A9	A11	42	P15	Input	Floating	VDDO	• GPIO: P15 • Keyboard scan output (column): KSO7 • A/D converter input 20 • IR_RX • 60Hz_main
B7	A9	–	P16	Input	Floating	VDDO	• GPIO: P16 • Keyboard scan output (column): KSO8 • A/D converter input 19
B8	A10	–	P17	Input	Floating	VDDO	• GPIO: P17 • Keyboard scan output (column): KSO9 • A/D converter input 18
C7	B9	–	P18	Input	Floating	VDDO	• GPIO: P18 • Keyboard scan output (column): KSO10 • A/D converter input 17
G7	C9	–	P19	Input	Floating	VDDO	• GPIO: P19 • Keyboard scan output (column): KSO11
F7	D9	–	P20	Input	Floating	VDDO	• GPIO: P20 • Keyboard scan output (column): KSO12 • A/D converter input 15
D7	E8	–	P21	Input	Floating	VDDO	• GPIO: P21 • Keyboard scan output (column): KSO13 • A/D converter input 14 • Triac control 3

Table 13. GPIO Pin Descriptions[a] (Cont.)

Pin Number			Pin Name	Default Direction	POR State	Power Domain	Alternate Function Description
81-pin FBGA	121-pin FBGA	56-pin QFN					
A8	G8	–	P22	Input	Floating	VDDO	• GPIO: P22 • Keyboard scan output (column): KSO14 • A/D converter input 13 • Triac control 4
D6	C6	–	P23	Input	Floating	VDDO	• GPIO: P23 • Keyboard scan output (column): KSO15 • A/D converter input 12
G6	F9	45	P24	Input	Floating	VDDO	• GPIO: P24 • Keyboard scan output (column): KSO16 • SPI_2: SPI_CLK (master and slave) • SPI_1: MISO (master only) • Peripheral UART: puart_tx
F6	D8	46	P25	Input	Floating	VDDO	• GPIO: P25 • Keyboard scan output (column): KSO17 • SPI_2: MISO (master and slave) • Peripheral UART: puart_rx
A4	A5	56	P26 PWM0	Input	Floating	VDDO	• GPIO: P26 • Keyboard scan output (column): KSO18 • SPI_2: SPI_CS (slave only) • SPI_1: MISO (master only) • Optical control output: QOC0 • Triac control 1 Current: 16 mA sink
B3	B5	55	P27 PWM1	Input	Floating	VDDO	• GPIO: P27 • Keyboard scan output (column): KSO19 • SPI_2: MOSI (master and slave) • Optical control output: QOC1 • Triac control 2 Current: 16 mA sink
C3	A4	–	P28 PWM2	Input	Floating	VDDO	• GPIO: P28 • Optical control output: QOC2 • A/D converter input 11 • LED1 Current: 16 mA sink
D3	C4	–	P29 PWM3	Input	Floating	VDDO	• GPIO: P29 • Optical control output: QOC3 • A/D converter input 10 • LED2 Current: 16 mA sink
C6	C8	47	P30	Input	Floating	VDDO	• GPIO: P30 • A/D converter input 9 • Pairing button pin in default FW • Peripheral UART: puart_rts
B6	B8	–	P31	Input	Floating	VDDO	• GPIO: P31 • A/D converter input 8 • EEPROM WP pin in default FW • Peripheral UART: puart_tx

Table 13. GPIO Pin Descriptions[a] (Cont.)

Pin Number			Pin Name	Default Direction	POR State	Power Domain	Alternate Function Description
81-pin FBGA	121-pin FBGA	56-pin QFN					
A6	B7	48	P32	Input	Floating	VDDO	• GPIO: P32 • A/D converter input 7 • Quadrature: QDX0 • SPI_2: SPI_CS (slave only) • SPI_1: MISO (master only) • Auxiliary clock output: ACLK0 • Peripheral UART: puart_tx
C4	B6	53	P33	Input	Floating	VDDO	• GPIO: P33 • A/D converter input 6 • Quadrature: QDX1 • SPI_2: MOSI (slave only) • Auxiliary clock output: ACLK1 • Peripheral UART: puart_rx
C5	C7	–	P34	Input	Floating	VDDO	• GPIO: P34 • A/D converter input 5 • Quadrature: QDY0 • Peripheral UART: puart_rx • External T/R switch control: tx_pd
B5	D7	49	P35	Input	Floating	VDDO	• GPIO: P35 • A/D converter input 4 • Quadrature: QDY1 • Peripheral UART: puart_cts
A5	A7	50	P36	Input	Floating	VDDO	• GPIO: P36 • A/D converter input 3 • Quadrature: QDZ0 • SPI_2: SPI_CLK (master and slave) • Auxiliary Clock Output: ACLK0 • Battery detect pin in default FW • External T/R switch control: ~tx_pd
D4	A6	–	P37	Input	Floating	VDDO	• GPIO: P37 • A/D converter input 2 • Quadrature: QDZ1 • SPI_2: MISO (slave only) • Auxiliary clock output: ACLK1
D5	C5	51	P38	Input	Floating	VDDO	• GPIO: P38 • A/D converter input 1 • SPI_2: MOSI (master and slave) • IR_TX • XTALO32K (FBGA-81 only)
B4	D4	52	P39	Input	Floating	VDDO	• GPIO: P39 • SPI_2: SPI_CS (slave only) • SPI_1: MISO (master only) • Infrared control: IR_RX • External PA ramp control: PA_Ramp • 60Hz_main • XTALI32K (FBGA-81 only)
–	H8	–	P40	Input	Floating	VDDO	• GPIO: P40 • pcm2_clk

Table 13. GPIO Pin Descriptions[a] (Cont.)

Pin Number			Pin Name	Default Direction	POR State	Power Domain	Alternate Function Description
81-pin FBGA	121-pin FBGA	56-pin QFN					
–	K4	–	P41	Input	Floating	VDDO	• GPIO: P41 • pcm2_sync
–	F6	–	P42	Input	Floating	VDDO	• GPIO: P42 • pcm2_di
–	J5	–	P43	Input	Floating	VDDO	• GPIO: P43 • pcm2_do
–	J4	–	P44	Input	Floating	VDDO	• GPIO: P44
–	J6	–	P45	Input	Floating	VDDO	• GPIO: P45
–	L4	–	P46	Input	Floating	VDDO	• GPIO: P46
–	E7	–	P47	Input	Floating	VDDO	• GPIO: P47
–	E6	–	P48	Input	Floating	VDDO	• GPIO: P48
–	D6	–	P49	Input	Floating	VDDO	• GPIO: P49
–	E5	–	P50	Input	Floating	VDDO	• GPIO: P50
–	D5	–	P51	Input	Floating	VDDO	• GPIO: P51
–	F4	–	P52	Input	Floating	VDDO	• GPIO: P52
–	F3	–	P53	Input	Floating	VDDO	• GPIO: P53
–	E4	–	P54	Input	Floating	VDDO	• GPIO: P54
–	E3	–	P55	Input	Floating	VDDO	• GPIO: P55
–	D3	–	P56	Input	Floating	VDDO	• GPIO: P56
–	G11	–	P57	Input	Floating	VDDO	• GPIO: P57 • PWM3

a. During power-on reset, all inputs are disabled.

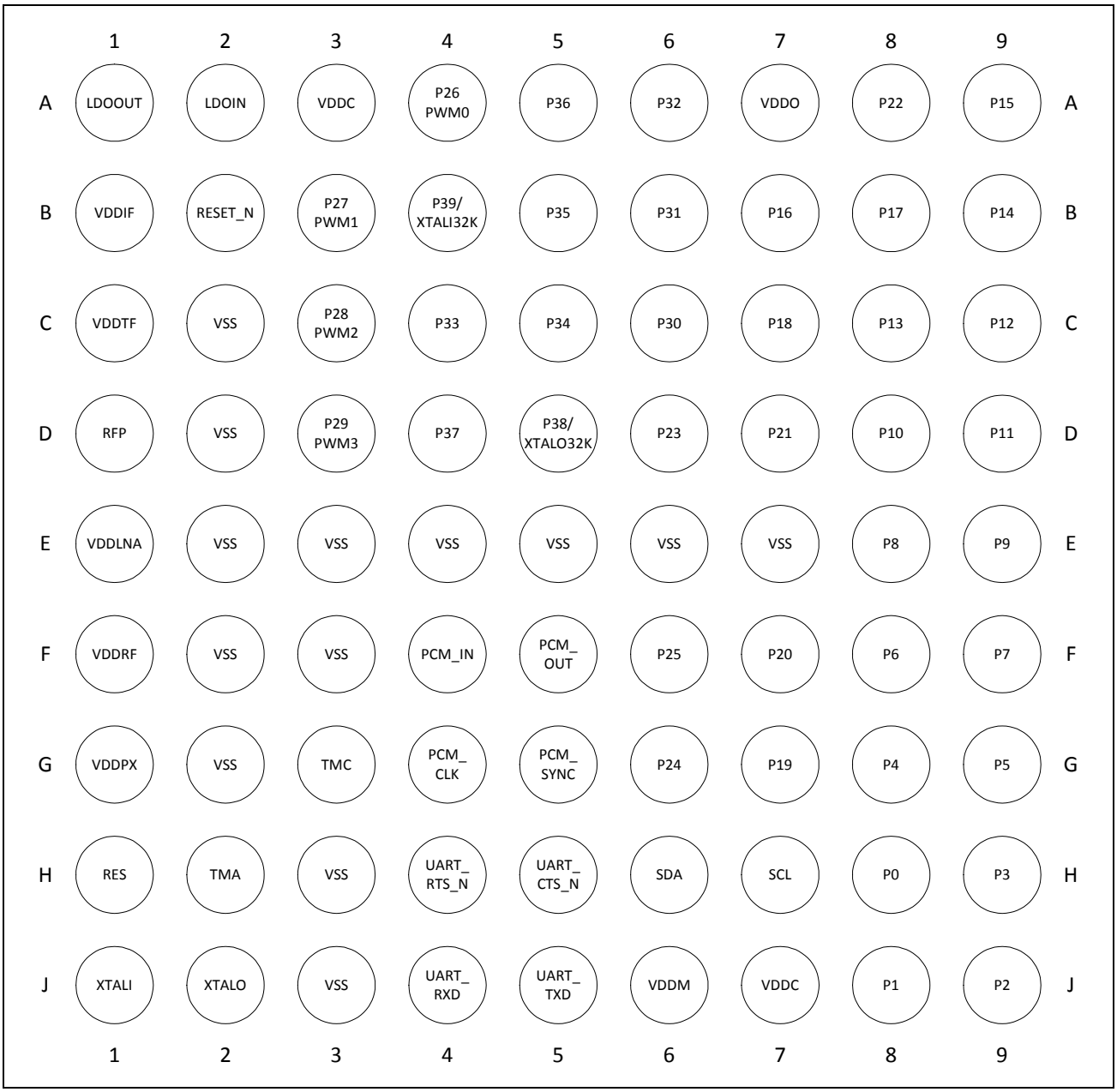
2.1 Ball Maps

This section presents the CYW20733 ball maps.

2.1.1 81-Pin FBGA Ball Map

Figure 12 shows the 81-pin FBGA package ball map.

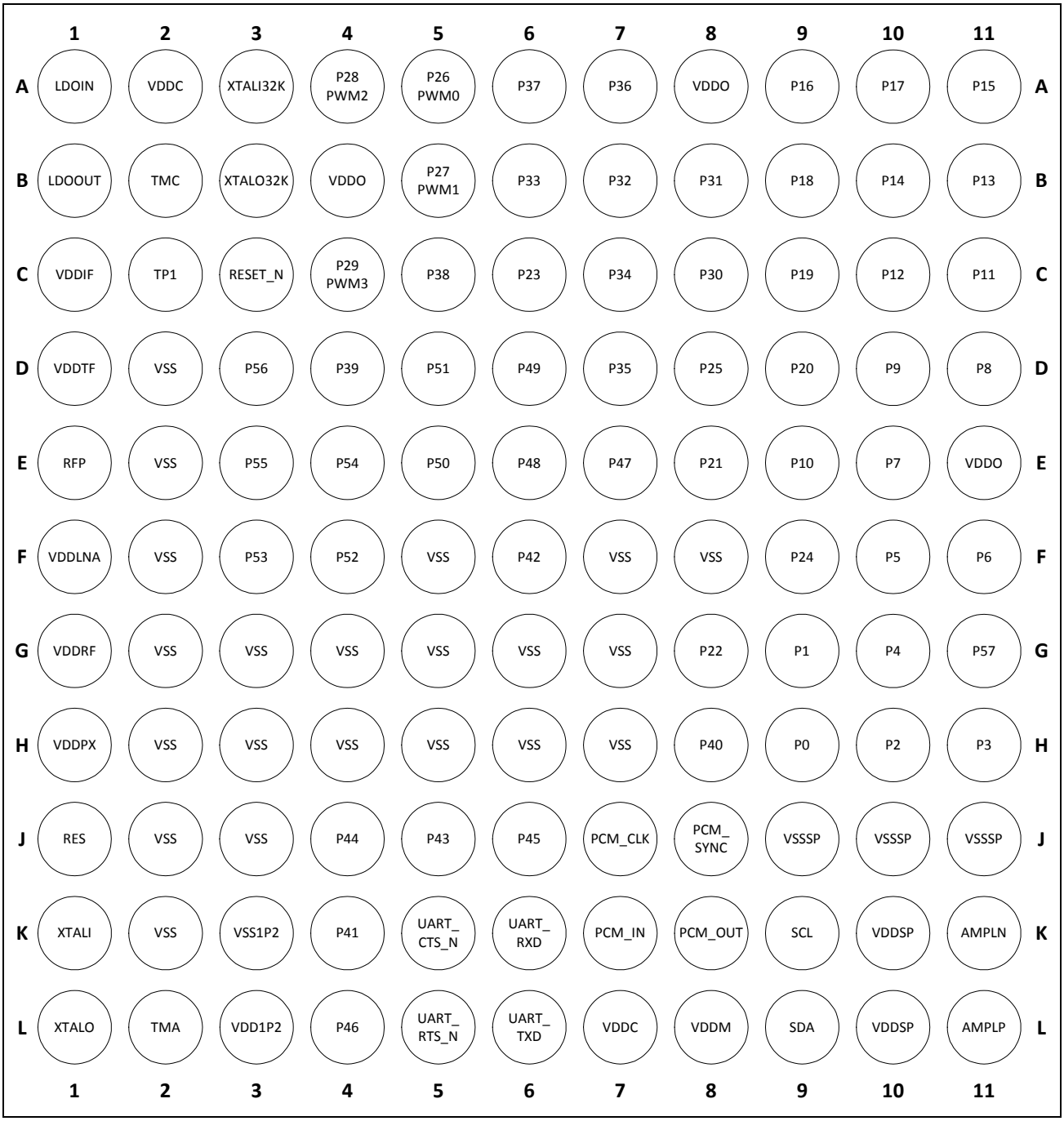
Figure 12. 81-Pin FBGA Ball Map



2.1.2 121-Pin FBGA Ball Map

Figure 13 shows the 121-pin FBGA package ball map.

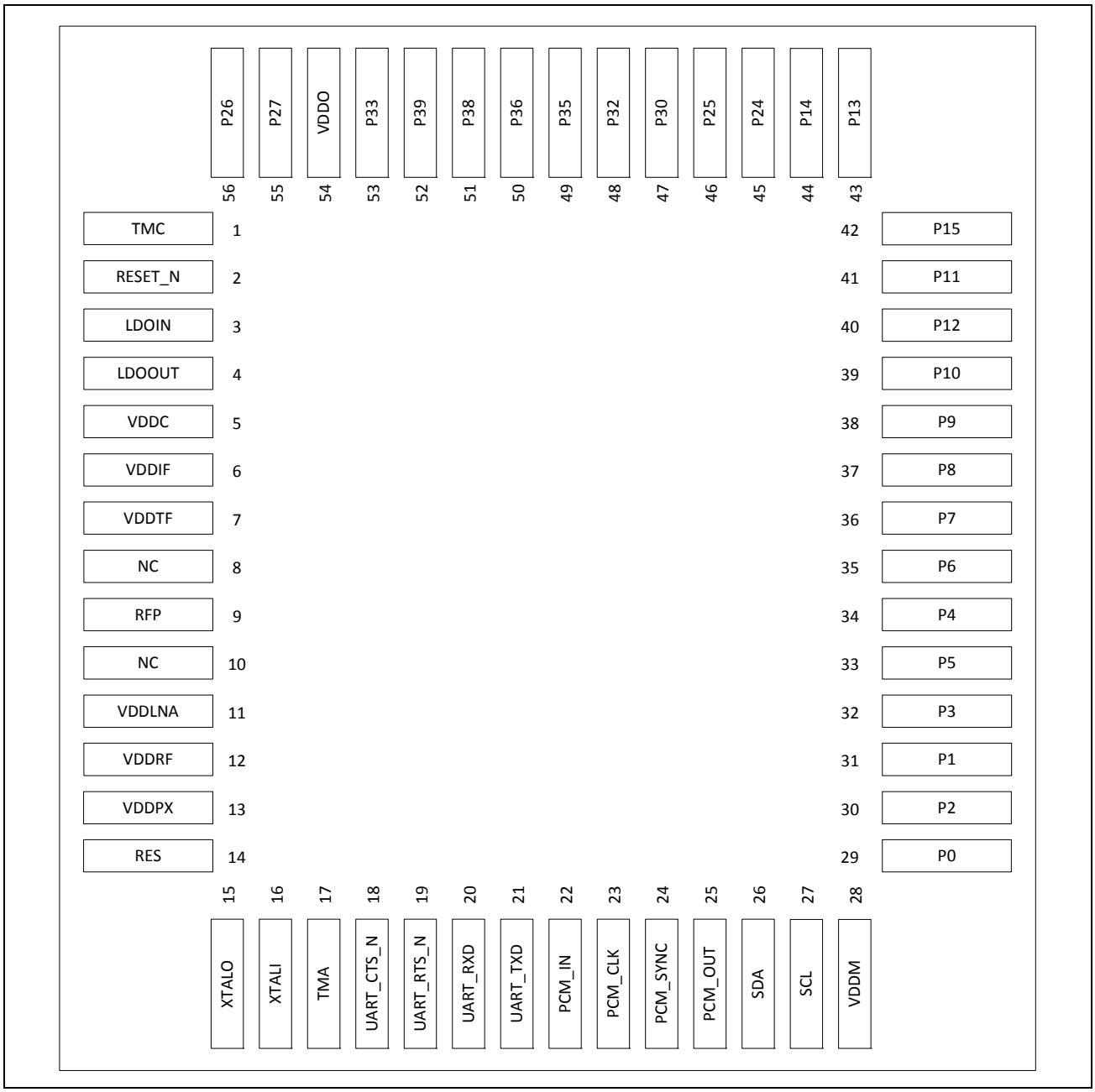
Figure 13. 121-Pin FBGA Ball Map



2.1.3 56-Pin QFN Diagram

Figure 14 shows the 56-pin QFN package.

Figure 14. 56-Pin QFN Diagram



3. Specifications

3.1 Electrical Characteristics

Table 14 shows the maximum electrical rating for voltages referenced to the VDD pin.

Table 14. Maximum Electrical Rating

Rating	Symbol	Value	Unit
DC supply voltage for RF domain	–	1.32	V
DC supply voltage for Core domain	–	1.4	V
DC supply voltage for VDDM domain (UART/I^{2}C)	–	3.8	V
DC supply voltage for VDDO domain	–	3.8	V
DC supply voltage for LDOIN	–	3.8	V
DC supply voltage for VDDLNA	–	1.4	V
DC supply voltage for VDDTF	–	3.3	V
Voltage on input or output pin	–	VSS – 0.3 to VDD + 0.3	V
Operating ambient temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–40 to +125	°C

Table 15 shows the power supply characteristics for the range T_J = 0 to 125°C.

Table 15. Power Supply

Parameter	Minimum[a]	Typical	Maximum[a]	Unit
DC supply voltage for RF	1.14	1.2	1.26	V
DC supply voltage for Core	1.14	1.2	1.26	V
DC supply voltage for VDDM (UART/I^{2}C)	1.62	–	3.63	V
DC supply voltage for VDDO	1.62	–	3.63	V
DC supply voltage for LDOIN	1.62	–	3.63	V
DC supply voltage for VDDLNA	1.14	1.2[b]	1.26	V
DC supply voltage for VDDTF	1.14	1.2[b]	3.3	V

a. Overall performance degrades beyond minimum and maximum supply voltages.

b. 1.2V for Class 2 output with internal VREG.

Table 16 shows the digital level characteristics for the LDO (VSS = 0V).

Table 16. LDO Regulator Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input voltage range	–	1.62	–	3.63	V
Default output voltage	–	–	1.2	–	V
Output voltage	Range	0.88	–	1.32	V
	Step size	–	40	80	mV
	Accuracy at any step	–5	–	+5	%
Load current	–	–	–	60	mA
Line regulation	Vin from 1.62 to 3.63V, I_{load} = 30 mA	–0.5	–	0.5	%V_O/V
Load regulation	I_{load} from 1 µA to 30 mA, Vin = 3.3V, Bonding R = 0.3Ω	–	0.1	0.15	%V_O/mA
Quiescent current	No load @Vin = 3.3V *Current limit enabled	–	6[a]	12[a]	µA
Power-down current	Vin = 3.3V, worst@70°C	–	–	200	nA

a. Includes the bandgap quiescent current.

Table 17. ADC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ADC Characteristics						
Number of Input channels	–	–	–	28	–	–
Channel switching rate	f_{ch}	–	–	–	187	kHz
Input signal range	V_{inp}	–	0	–	3.63	V
Reference settling time	–	–	7.5	–	–	µs
Input resistance	R_{inp}	Single-ended, input range of 0–1.2V	–	680	–	kΩ
		Single-ended, input range of 0–2.4V	–	1.84	–	MΩ
		Single-ended, input range of 0–3.6V	–	3	–	MΩ
Input capacitance	C_{inp}	–	–	–	5	pF
Conversion rate	f_C	–	5.859	–	187	kHz
Resolution	R	–	–	16	–	bits
Effective number of bits	–	In guaranteed performance range	–	See Table 7 on page 14	–	bits
Absolute voltage measurement error		Using on-chip ADC firmware driver	–	±2		%
Integral nonlinearity[1]	INL	In guaranteed performance range	–1	–	1	LSB[1]
Differential nonlinearity[1]	DNL	In guaranteed performance range	–1	–	1	LSB[1]

Notes:
1. LSBs are expressed at the 10-bit level.

Table 18. Integrated Audio Amplifier Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Analog supply voltage	–	2.9	3.0	3.1	V
Digital supply voltage	–	1.08	1.2	1.32	V
Quiescent current	Zero digital input	–	2	–	mA
Power down current	–	–	0.5	–	µA
Output power	R_L = 8Ω	200	240	–	mW
Maximum efficiency	At 200 mW output power	–	70	–	%
Dynamic range (DR)	At –60 dBFs input	65	68	–	dB
Signal-to-noise plus distortion ratio (SNDR)	At 200 mW output power	–	40	–	dB

Table 19. Digital Level[a]

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage	VIL	–	–	0.4	V
Input high voltage	VIH	0.75 × VDDO	–	–	V
Input low voltage (VDDO = 1.62V)	VIL	–	–	0.4	V
Input high voltage (VDDO = 1.62V)	VIH	1.2	–	–	V
Output low voltage[b]	VOL	–	–	0.4	V
Output high voltage[b]	VOH	VDDO – 0.4	–	–	V
Input capacitance (VDDMEM domain)	CIN	–	0.12	–	pF

a. This table is also applicable to VDDMEM domain.

b. At the specified drive current for the pad.

Table 20. Current Consumption, Class 1[a]

Operational Mode	Conditions	Typ	Unit
Receive (1 Mbps)	Peak current level during reception of a basic-rate packet.	28.2	mA
Transmit (1 Mbps)	Peak current level during the transmission of a basic-rate packet: GFSK output power = 10 dBm.	63.1	mA
Receive (EDR)	Peak current level during the reception of a 2 or 3 Mbps rate packet.	28.6	mA
Transmit (EDR)	Peak current level during the transmission of a 2 or 3 Mbps rate packet: EDR output power = 8 dBm.	63.7	mA
Average Current			
DM1/DH1 (RX)	Average current during basic rate maximum throughput connection, which includes only this packet type.	24.3	mA
DM5/DH5 (RX)	Average current during basic rate maximum throughput connection, which includes only this packet type.	26.3	mA
3DH1 (RX)	Average current during extended data rate maximum throughput connection which includes only this packet type.	24.9	mA
3DH5 (RX)	Average current during extended data rate maximum throughput connection, which includes only this packet type.	26.4	mA
DM1/DH1 (TX)	Average current during basic rate maximum throughput connection, which includes only this packet type.	29.6	mA
DM5/DH5 (TX)	Average current during basic rate maximum throughput connection, which includes only this packet type.	47.2	mA
3DH1 (TX)	Average current during extended data rate maximum throughput connection, which includes only this packet type.	29.7	mA
3DH5 (TX)	Average current during extended data rate maximum throughput connection, which includes only this packet type.	44.8	mA
Paging	–	23.7	mA
Sniff slave (495 ms)	Based on one attempt and no timeout parameter. Quality connection that rarely requires more than minimum packet exchange. Sniff master follows the optimal sniff protocol of the CYW20702 master.	290	µA
Sniff slave (22.5 ms)	–	2.57	mA
Sniff slave (11.25 ms)	–	4.93	mA

a. Current consumption measurements are taken at LDOIN. LDOIN = VDDIO = 2.6V, VDDPA = 3.0V.

Table 21. Current Consumption, Class 2 (0 dBm)[a]

Operational Mode	Conditions	Typ	Unit
Receive (1 Mbps)	Peak current level during the reception of a basic-rate packet.	29.0	mA
Transmit (1 Mbps)	Peak current level during the transmission of a basic-rate packet: GFSK output power = 0 dBm.	39.3	mA
Receive (EDR)	Peak current level during the reception of a 2 or 3 Mbps rate packet.	30.5	mA
Transmit (EDR)	Peak current level during the transmission of a 2 or 3 Mbps rate packet: EDR output power = 0 dBm.	39.3	mA
Average Current			
DM1/DH1 (RX)	Average current during basic rate maximum throughput connection, which includes only this packet type.	22.1	mA
DM5/DH5 (RX)	Average current during basic rate maximum throughput connection, which includes only this packet type.	25.8	mA
3DH1 (RX)	Average current during extended data rate maximum throughput connection, which includes only this packet type.	22.8	mA
3DH5 (RX)	Average current during extended data rate maximum throughput connection, which includes only this packet type.	24.7	mA
DM1/DH1 (TX)	Average current during basic rate maximum throughput connection, which includes only this packet type.	22.0	mA
DM5/DH5 (TX)	Average current during basic rate maximum throughput connection, which includes only this packet type.	30.9	mA
3DH1 (TX)	Average current during extended data rate maximum throughput connection, which includes only this packet type.	22.1	mA
3DH5 (TX)	Average current during extended data rate maximum throughput connection, which includes only this packet type.	31.6	mA
Paging	–	22.9	mA
Sniff slave (495 ms)	Based on one attempt and no timeout parameter. Quality connection that rarely requires more than minimum packet exchange. Sniff master follows optimal sniff protocol of CYW20702 master.	240	µA
Sniff slave (22.5 ms)	–	2.27	mA
Sniff slave (11.25 ms)	–	4.46	mA

a. Current consumption measurements are taken at LDOIN. LDOIN = VDDIO = 2.6V, VDDPA = 1.2V.

Table 22. Current Consumption

Operational Mode	Conditions	Typ	Unit
Sleep	Internal LPO is in use.	46.5	µA
HIDOFF	–	1.1	µA
Inquiry scan (1.28 sec.)	Periodic scan rate is R1 (1.28 seconds).	540	µA
Page Scan (R1)	Periodic scan rate is R1 (1.28 seconds).	490	µA
Inquiry Scan + Page Scan (R1)	Both inquiry and page scans are interlaced together at a periodic scan rate of 1.28 seconds.	940	µA

3.2 RF Specifications

Table 23. Receiver RF Specifications[a,b]

Parameter	Conditions	Minimum	Typical [c]	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity [d]	GFSK, 0.1% BER, 1 Mbps	–	–89	–85	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–91	–85	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–86	–81	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	π/4-DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
Interference Performance					
C/I cochannel	GFSK, 0.1% BER	–	–	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20.0	dB
C/I cochannel	π/4-DQPSK, 0.1% BER	–	–	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	–	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33.0	dB
C/I image channel	8-DPSK, 0.1% BER	–	–	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13.0	dB
Out-of-Band Blocking Performance (CW) [e]					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Intermodulation Performance [f]					
BT, Δf = 5 MHz	–	–39.0	–	–	dBm

Table 23. Receiver RF Specifications[a,b] (Cont.)

Parameter	Conditions	Minimum	Typical [c]	Maximum	Unit
Spurious Emissions [g]					
30 MHz to 1 GHz	–	–	–	–57	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm

a. All specifications are single ended. Unused inputs are left open.
b. All specifications, except typical, are for commercial temperatures.
c. Typical operating conditions are 1.22V operating voltage and 25°C ambient temperature.
d. The receiver sensitivity is measured at a BER of 0.1% on the device interface.
e. Meets this specification using front-end band-pass filter.
f. f0 = –64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n × 1 MHz, where n is 3, 4, or 5. For the typical case, n = 5.
g. Includes baseband radiated emissions.

Table 24. Transmitter RF Specifications [a,b]

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class1: GFSK Tx power[cd]	–	6.5	10	–	dBm
Class1: EDR Tx power[de]	–	4.5	8	–	dBm
Class 2: GFSK Tx power[d]	–	–0.5	3	–	dBm
Power control step	–	2	4	6	dB
Modulation Accuracy					
π/4-DQPSK frequency stability	–	–10	–	10	kHz
π/4-DQPSK RMS DEVM	–	–	–	20	%
π/4-QPSK peak DEVM	–	–	–	35	%
π/4-DQPSK 99% DEVM	–	–	–	30	%
8-DPSK frequency stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
In-Band Spurious Emissions					
+500 kHz	–	–	–	–20	dBc
1.0 MHz < |M – N| < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz	–	–	–	–20	dBm
|M – N| ≥ 2.5 MHz	–	–	–	–40	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [f]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [f, g]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

a. All specifications are for commercial temperatures.

b. All specifications are single-ended. Unused inputs are left open.

c. +10 dBm output for GFSK measured with VDDTF = 2.9 V.

d. Power output is measured at the device without a front-end band-pass filter.

e. +8 dBm output for EDR measured with VDDTF = 2.9 V.

f. Maximum value is the value required for Bluetooth qualification.

g. Meets this specification using a front-end band-pass filter.

3.3 Timing and AC Characteristics

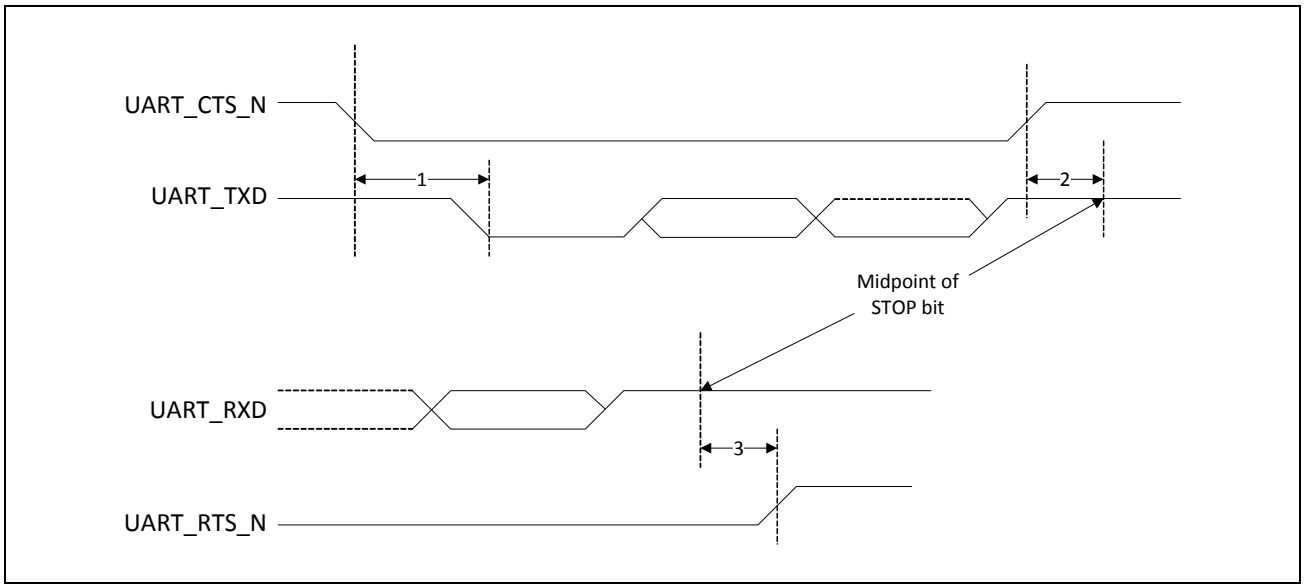
In this section, use the numbers listed in the Reference column of each table to interpret the following timing diagrams.

3.3.1 UART Timing

Table 25. UART Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

Figure 15. UART Timing



3.3.2 SPI Timing

Figure 16. SPI Timing Diagram

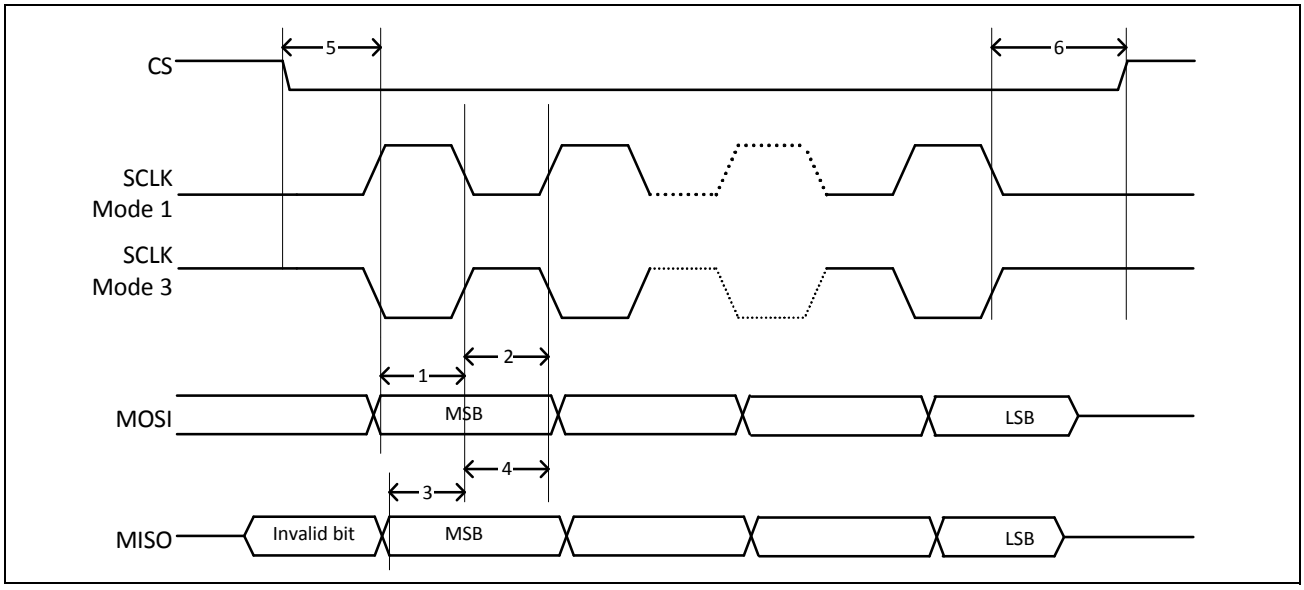


Table 26. SPI1 Timing Values—SCLK = 12 MHz and VDDM = 1.8V[a]

Reference	Characteristics	Symbol	Min	Typical[b]	Max	Unit
1	Output setup time, from MOSI data valid to sample edge of SCLK	Tds_mo	–	23	–	ns
2	Output hold time, from sample edge of SCLK to MOSI data update	Tdh_mo	–	60	–	ns
3	Input setup time, from MISO data valid to sample edge of SCLK	Tds_mi	–	TBD	–	ns
4	Input hold time, from sample edge of SCLK to MISO data update	Tdh_mi	–	TBD	–	ns
5[c]	Time from CS assert to first SCLK edge	Tsu_cs	½ SCLK period – 1	–	–	ns
6[c]	Time from first SCLK edge to CS deassert	Thd_cs	½ SCLK period	–	–	ns

a. The SCLK period is based on the limitation of Tds_mi. SCLK is designed for a maximum speed of 12 MHz. The speed can be adjusted to as low as 400 Hz by configuring the firmware.

b. Typical timing based on 20 pF//1 MΩ load and SCLK = 12 MHz.

c. CS timing is firmware controlled.

Table 27. SPI1 Timing Values—SCLK = 12 MHz and VDDM = 3.3V[a]

Reference	Characteristics	Symbol	Min	Typical[b]	Max	Unit
1	Output setup time, from MOSI data valid to sample edge of SCLK	Tds_mo	–	34	–	ns
2	Output hold time, from sample edge of SCLK to MOSI data update	Tdh_mo	–	49	–	ns
3	Input setup time, from MISO data valid to sample edge of SCLK	Tds_mi	–	TBD	–	ns
4	Input hold time, from sample edge of SCLK to MISO data update	Tdh_mi	–	TBD	–	ns
5[c]	Time from CS assert to first SCLK edge	Tsu_cs	½ SCLK period – 1	–	–	ns
6[c]	Time from first SCLK edge to CS deassert	Thd_cs	½ SCLK period	–	–	ns

a. The SCLK period is based on the limitation of Tds_mi. SCLK is designed for a maximum speed of 12 MHz. The speed can be adjusted to as low as 400 Hz by configuring the firmware.

b. Typical timing based on 20 pF//1 MΩ load and SCLK = 12 MHz.

c. CS timing is firmware controlled.

Table 28. SPI2 Timing Values—SCLK = 6 MHz and VDDM = 3.3V[a]

Reference	Characteristics	Symbol	Min	Typical[b]	Max	Unit
1	Output setup time, from MOSI data valid to sample edge of SCLK	Tds_mo	–	67	–	ns
2	Output hold time, from sample edge of SCLK to MOSI data update	Tdh_mo	–	99	–	ns
3	Input setup time, from MISO data valid to sample edge of SCLK	Tds_mi	–	TBD	–	ns
4	Input hold time, from sample edge of SCLK to MISO data update	Tdh_mi	–	TBD	–	ns
5[c]	Time from CS assert to first SCLK edge	Tsu_cs	½ SCLK period – 1	–	–	ns
6[c]	Time from first SCLK edge to CS deassert	Thd_cs	½ SCLK period	–	–	ns

a. The SCLK period is based on the limitation of Tds_mi. SCLK is designed for a maximum speed of 6 MHz. The speed can be adjusted to as low as 400 Hz by configuring the firmware.

b. Typical timing based on 20 pF//1 MΩ load and SCLK = 6 MHz.

c. CS timing is firmware controlled in master mode and can be adjusted as required in slave mode.

3.3.3 BSC Interface Timing

The specifications in Table 29 and Table 30 on page 43 reference Figure 17 on page 43.

Table 29. BSC Interface Timing Specifications (up to 1 MHz)

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[a]	0	–	ns
7	Data input setup time	100	–	ns

Table 29. BSC Interface Timing Specifications (up to 1 MHz)

Reference	Characteristics	Min	Max	Unit
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[b]	650	–	ns

a. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

b. Time that the CBUS must be free before a new transaction can start.

Table 30. BSC Interface Timing Specification (1 MHz through 4 MHz)

Reference	Characteristics	Min	Max	Unit
1	Clock frequency[a]	1.000	4.000	MHz
2	START condition setup time	233	–	ns
3	START condition hold time	66	–	ns
4	Clock low time[b]	½ SCL period	–	ns
5	Clock high time[b]	½ SCL period	–	ns
6	Data input hold time[c]	0	–	ns
7	Data input setup time[d]	33.4	–	ns
8	STOP condition setup time	233	–	ns
9	Output valid from clock	–	150	ns
10	Bus free time[e]	650	–	ns

a. Maximum speed is achieved without clock stretching. Strict timing parameter adherence for modes beyond I^2C fast mode may require that the total capacitance of the SDA and SCL traces be very similar so that signal transition times are very similar.

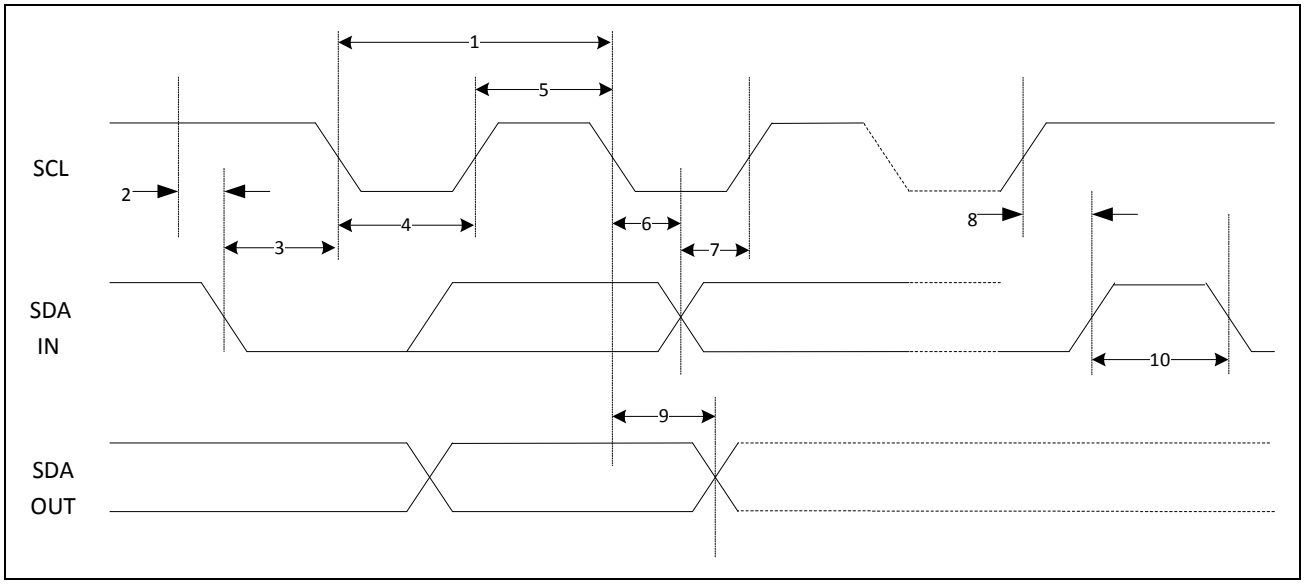
b. Programmable by firmware. Use 50% of period for overclocking frequencies greater than 2.400 MHz. Can be asymmetric (65/35 duty) for modest overclocking—up to 2.400 MHz.

c. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

d. Depends on the degree of overclocking. Application-specific programmability of the hardware block can affect this parameter.

e. Time that CBUS must be free before a new transaction can start.

Figure 17. BSC Interface Timing Diagram



3.3.4 PCM Interface Timing

The following is a list of the PCM interface timing diagrams.

- PCM Electrical Timing Slave — Short Frame Sync
- PCM Electrical Timing Master—Short Frame Sync
- PCM Electrical Timing Burst (Slave Rx Only)—Short Frame Sync

- PCM Electrical Timing Slave—Long Frame Sync
- PCM Electrical Timing Master—Long Frame Sync
- PCM Electrical Timing Burst (Slave Rx Only)—Long Frame Sync

Note: The TX and RX timings are combined on the same diagram. The CYW20733 can only either transmit or receive in a given slot.

PCM Electrical Timing Slave — Short Frame Sync

Figure 18. PCM Electrical Timing Slave—Short Frame Sync Diagram

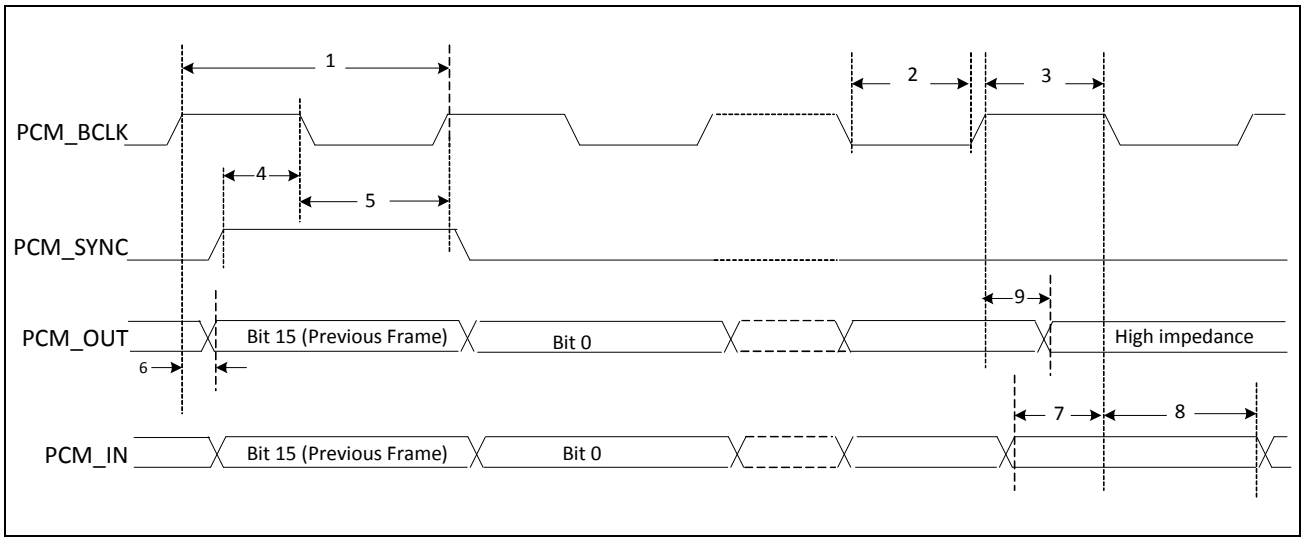


Table 31. PCM Electrical Timing Slave—Short Frame Sync Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low time	41	–	–	ns
3	PCM bit clock high time	41	–	–	ns
4	PCM_SYNC setup time	8	–	–	ns
5	PCM_SYNC hold time	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

PCM Electrical Timing Master—Short Frame Sync

Figure 19. PCM Electrical Timing Master—Short Frame Sync Diagram

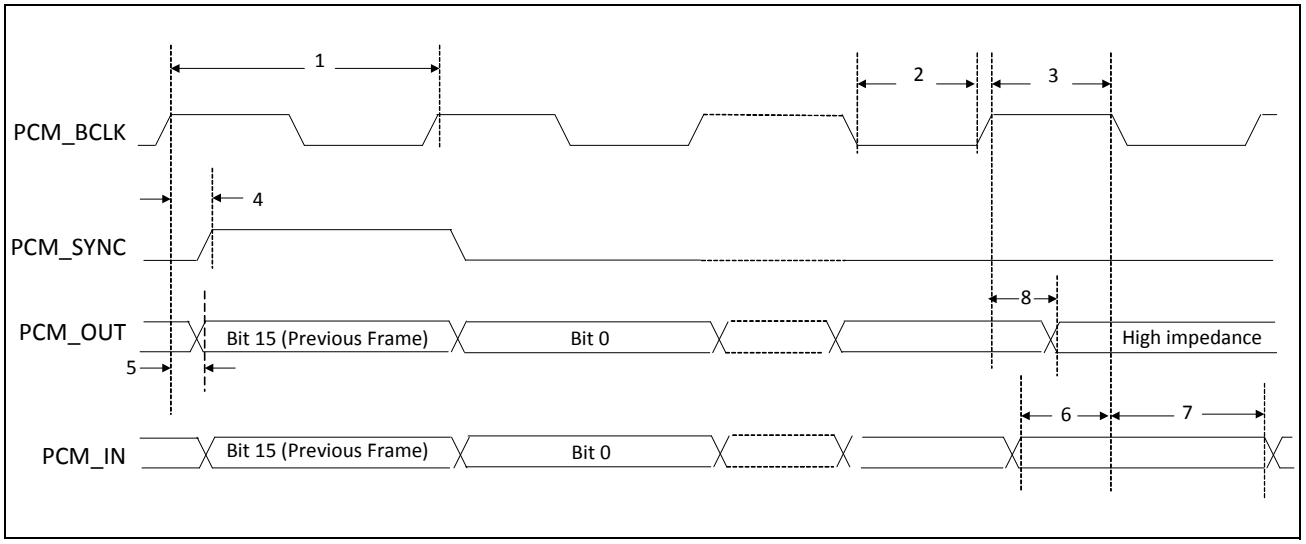


Table 32. Values of PCM Electrical Timing Master—Short Frame Sync Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low time	41	–	–	ns
3	PCM bit clock high time	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

PCM Electrical Timing Burst (Slave Rx Only)—Short Frame Sync

Figure 20. PCM Electrical Timing Burst (Slave Rx-Only)—Short Frame Sync Diagram

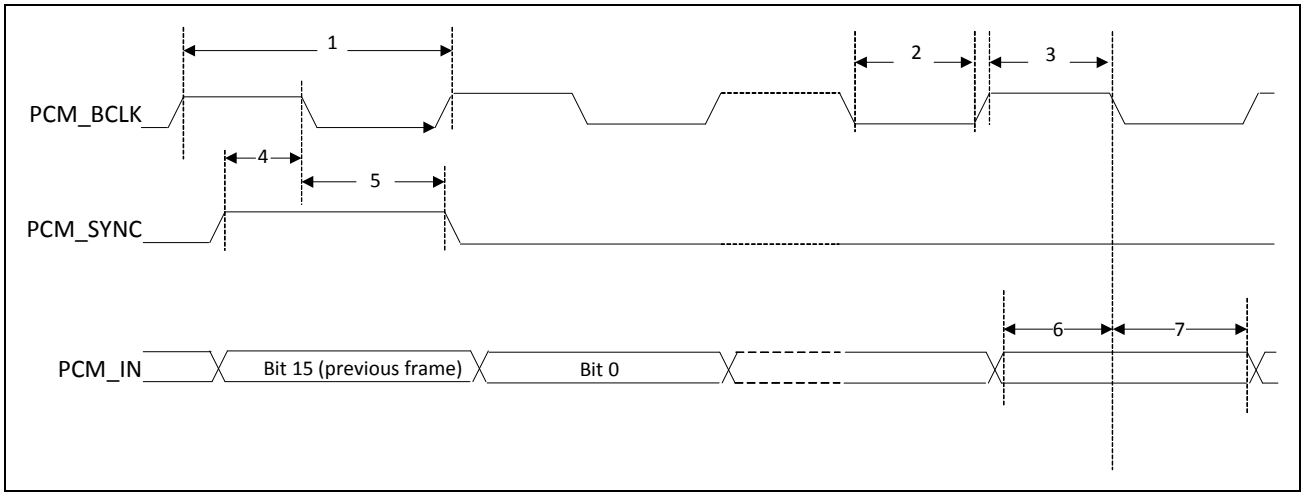


Table 33. Values of PCM Electrical Timing Burst (Slave Rx-Only)—Short Frame Sync Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low time	20.8	–	–	ns
3	PCM bit clock high time	20.8	–	–	ns
4	PCM_SYNC setup time	8	–	–	ns
5	PCM_SYNC hold time	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

PCM Electrical Timing Slave—Long Frame Sync

Figure 21. PCM Electrical Timing Slave—Long Frame Sync Diagram

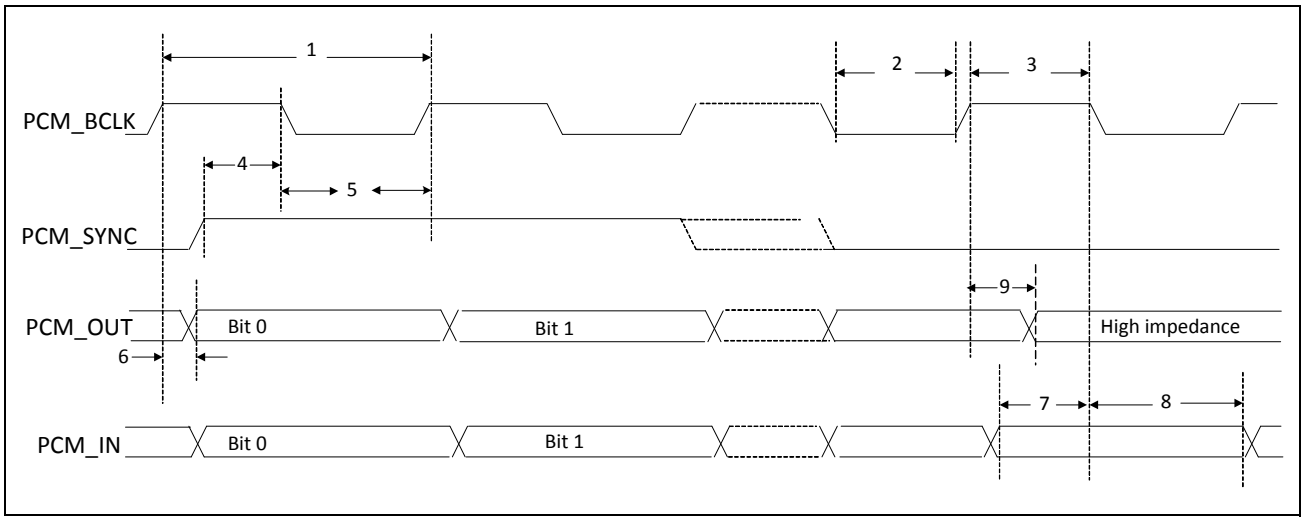


Table 34. Values of PCM Electrical Timing Slave—Long Frame Sync Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low time	41	–	–	ns
3	PCM bit clock high time	41	–	–	ns
4	PCM_SYNC setup time	8	–	–	ns
5	PCM_SYNC hold time	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

PCM Electrical Timing Master—Long Frame Sync

Figure 22. PCM Electrical Timing Master—Long Frame Sync Diagram

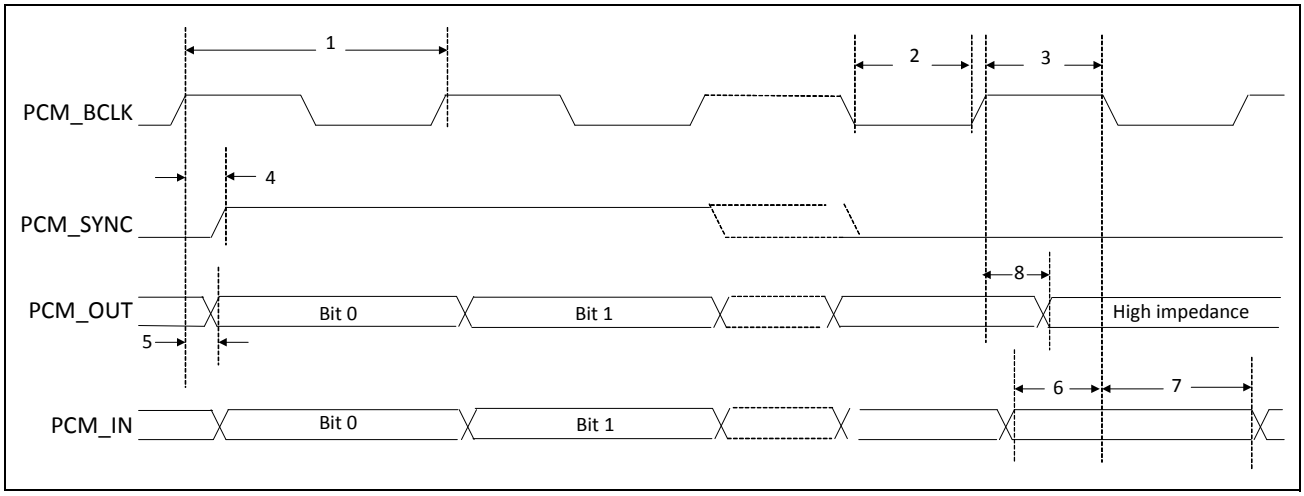


Table 35. Values of PCM Electrical Timing Master—Long Frame Sync Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low time	41	–	–	ns
3	PCM bit clock high time	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

PCM Electrical Timing Burst (Slave Rx Only)—Long Frame Sync

Figure 23. PCM Electrical Timing Burst (Slave Rx-Only)—Long Frame Sync Diagram

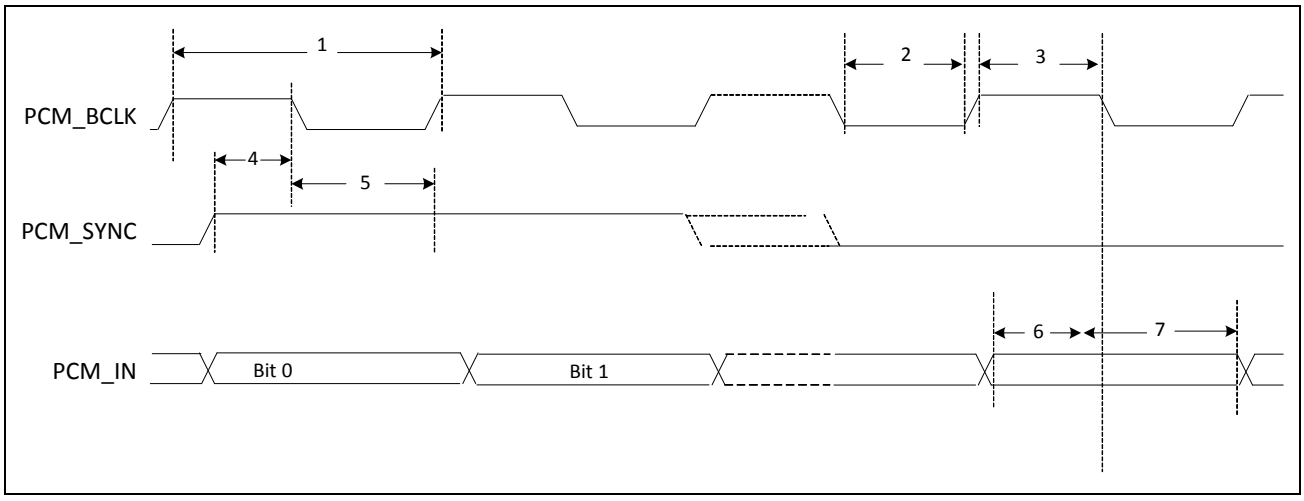


Table 36. Values of PCM Electrical Timing Burst (Slave Rx Only)—Long Frame Sync Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low time	20.8	–	–	ns
3	PCM bit clock high time	20.8	–	–	ns
4	PCM_SYNC setup time	8	–	–	ns
5	PCM_SYNC hold time	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

3.3.5 I²S Timing

The following is a list of the I²S timing diagrams.

- I²S Electrical Timing Slave—Short Frame WS
- I²S Electrical Timing Master—Short Frame WS
- I²S Electrical Timing Burst (Slave Rx Only)—Short Frame WS
- I²S Electrical Timing Slave—Long Frame WS
- I²S Electrical Timing Master—Long Frame WS
- I²S Electrical Timing Burst (Slave Rx Only)—Long Frame WS

Note: The TX and RX timings are combined on the same diagram. The CYW20733 can only either transmit or receive in a given slot.

I²S Electrical Timing Slave—Short Frame WS

Figure 24. I²S Electrical Timing Slave — Short Frame WS Diagram

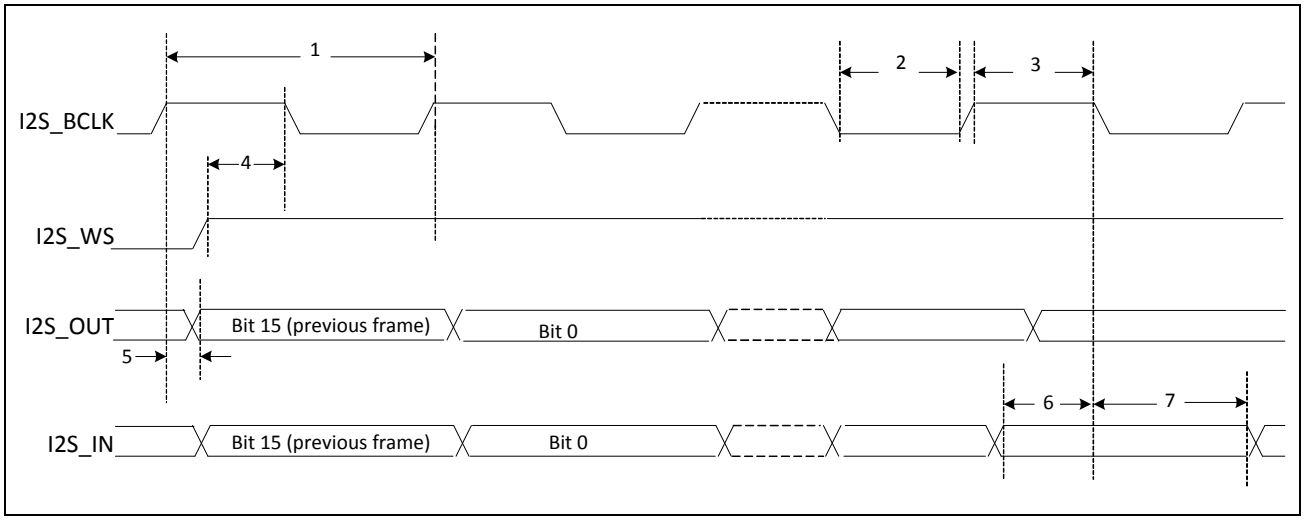


Table 37. Values of I²S Electrical Timing Slave—Short Frame WS Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	I²S bit clock frequency	–	–	12	MHz
2	I²S bit clock low time	41	–	–	ns
3	I²S bit clock high time	41	–	–	ns
4	I2S_WS setup time	8	–	–	ns
5	I2S_OUT delay	0	–	25	ns

Table 37. Values of I²S Electrical Timing Slave—Short Frame WS Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
6	I2S_IN setup	8	–	–	ns
7	I2S_IN hold	8	–	–	ns

I²S Electrical Timing Master—Short Frame WS

Figure 25. I²S Electrical Timing Master—Short Frame WS Diagram

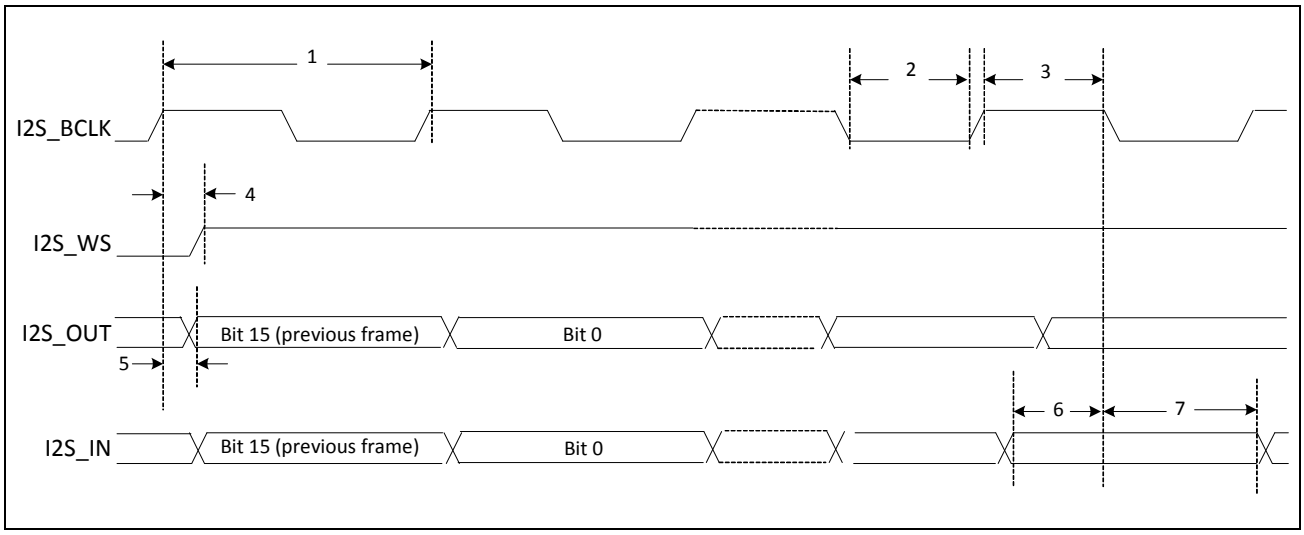


Table 38. Values of I²S Electrical Timing Master—Short Frame WS Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	I²S bit clock frequency	–	–	12	MHz
2	I²S bit clock low time	41	–	–	ns
3	I²S bit clock high time	41	–	–	ns
4	I2S_WS delay	0	–	25	ns
5	I2S_OUT delay	0	–	25	ns
6	I2S_IN setup	8	–	–	ns
7	I2S_IN hold	8	–	–	ns

I²S Electrical Timing Burst (Slave Rx Only)—Short Frame WS

Figure 26. I²S Electrical Timing Burst (Slave Rx Only) — Short Frame WS Diagram

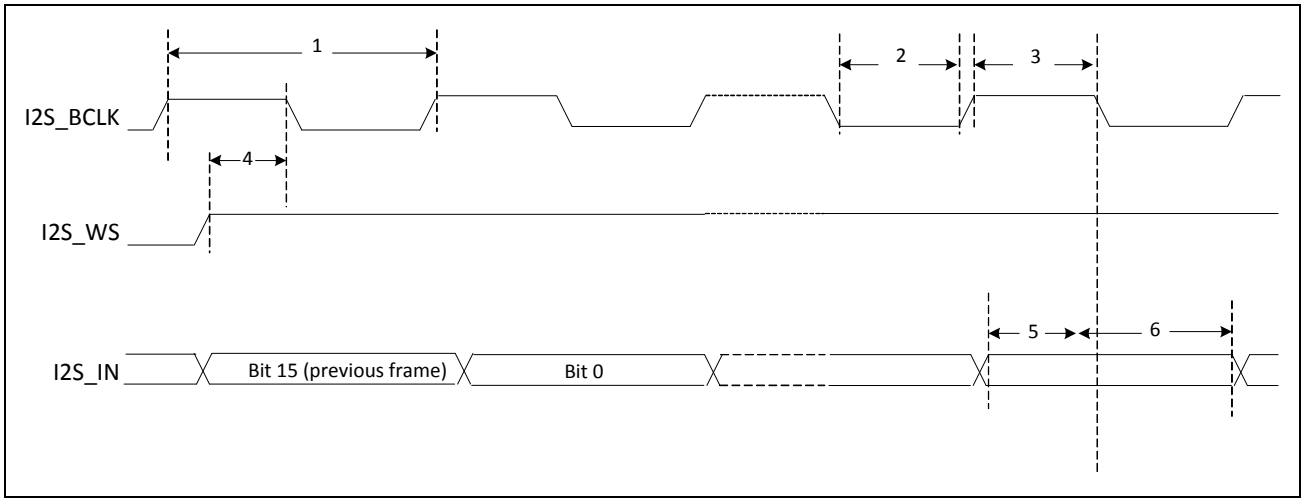


Table 39. Values of I²S Electrical Timing Burst (Slave Rx-Only)—Short Frame WS Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	I²S bit clock frequency	–	–	24	MHz
2	I2S bit clock low time	20.8	–	–	ns
3	I²S bit clock high time	20.8	–	–	ns
4	I2S_WS setup time	8	–	–	ns
5	I2S_IN setup	8	–	–	ns
6	I2S_IN hold	8	–	–	ns

I²S Electrical Timing Slave—Long Frame WS

Figure 27. I²S Electrical Timing Slave — Long Frame WS Diagram

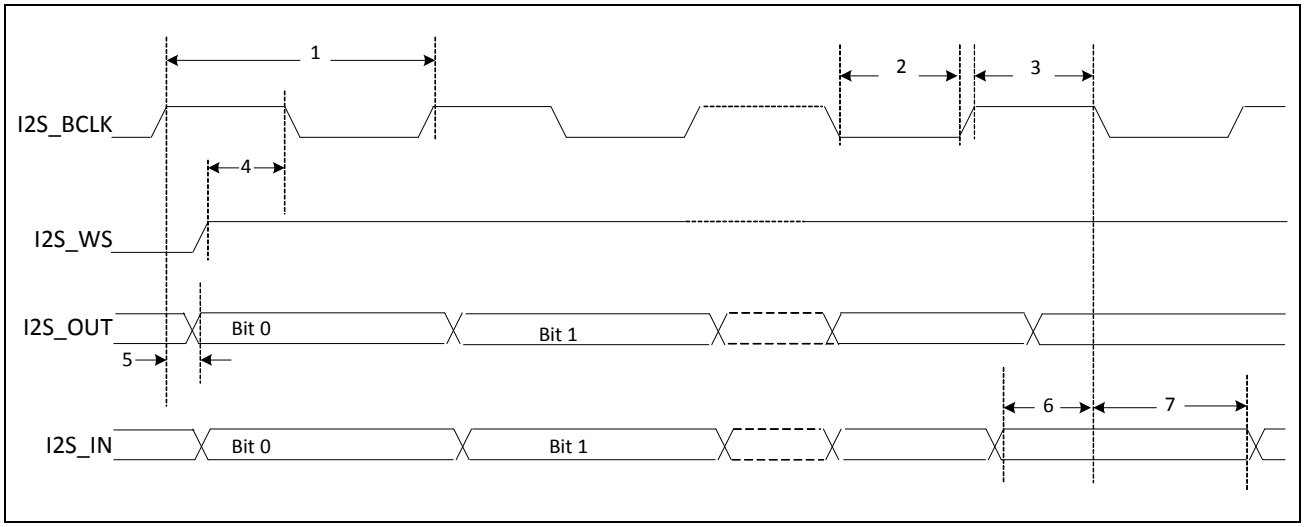


Table 40. Values of I²S Electrical Timing Slave—Long Frame WS Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	I²S bit clock frequency	–	–	12	MHz
2	I²S bit clock low time	41	–	–	ns
3	I²S bit clock high time	41	–	–	ns
4	I2S_WS setup time	8	–	–	ns
5	I2S_OUT delay	0	–	25	ns
6	I2S_IN setup	8	–	–	ns
7	I2S_IN hold	8	–	–	ns

I²S Electrical Timing Master—Long Frame WS

Figure 28. I²S Electrical Timing Master—Long Frame WS Diagram

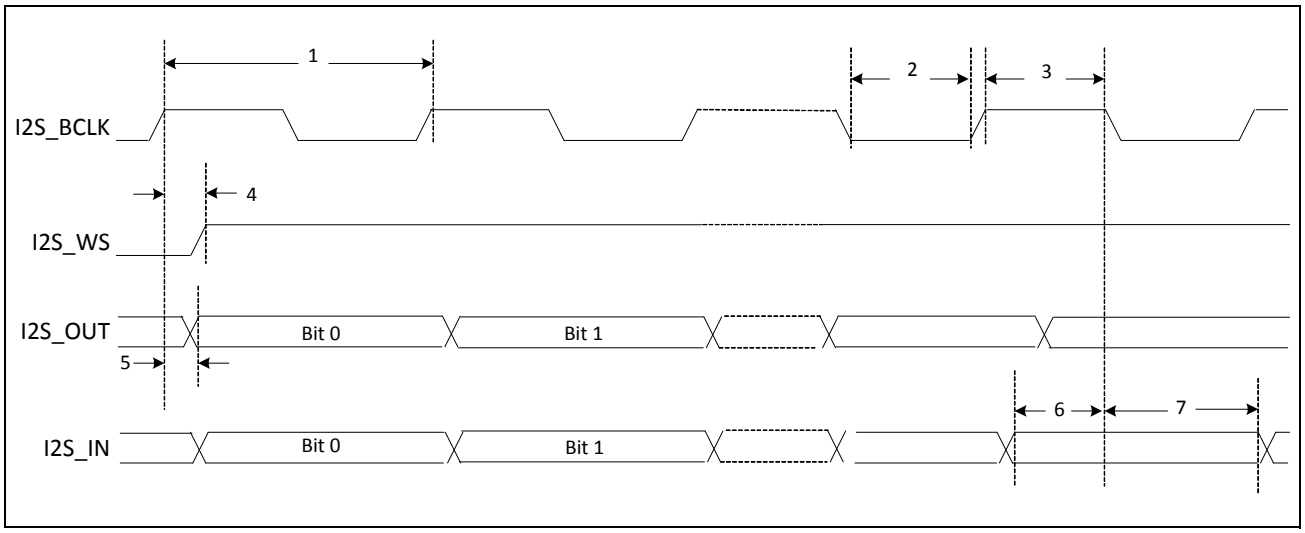


Table 41. Values of I²S Electrical Timing Master—Long Frame WS Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	I²S bit clock frequency	–	–	12	MHz
2	I²S bit clock low time	41	–	–	ns
3	I²S bit clock high time	41	–	–	ns
4	I2S_WS delay	0	–	25	ns
5	I2S_OUT delay	0	–	25	ns
6	I2S_IN setup	8	–	–	ns
7	I2S_IN hold	8	–	–	ns

I²S Electrical Timing Burst (Slave Rx Only)—Long Frame WS

Figure 29. I²S Electrical Timing Burst (Slave Rx Only) — Long Frame WS Diagram

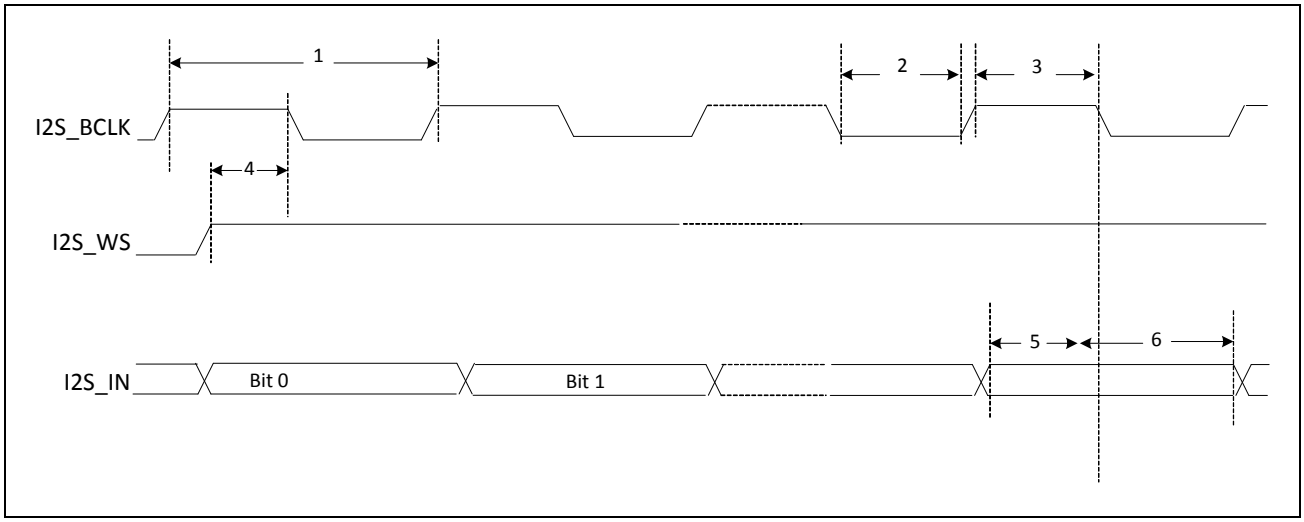
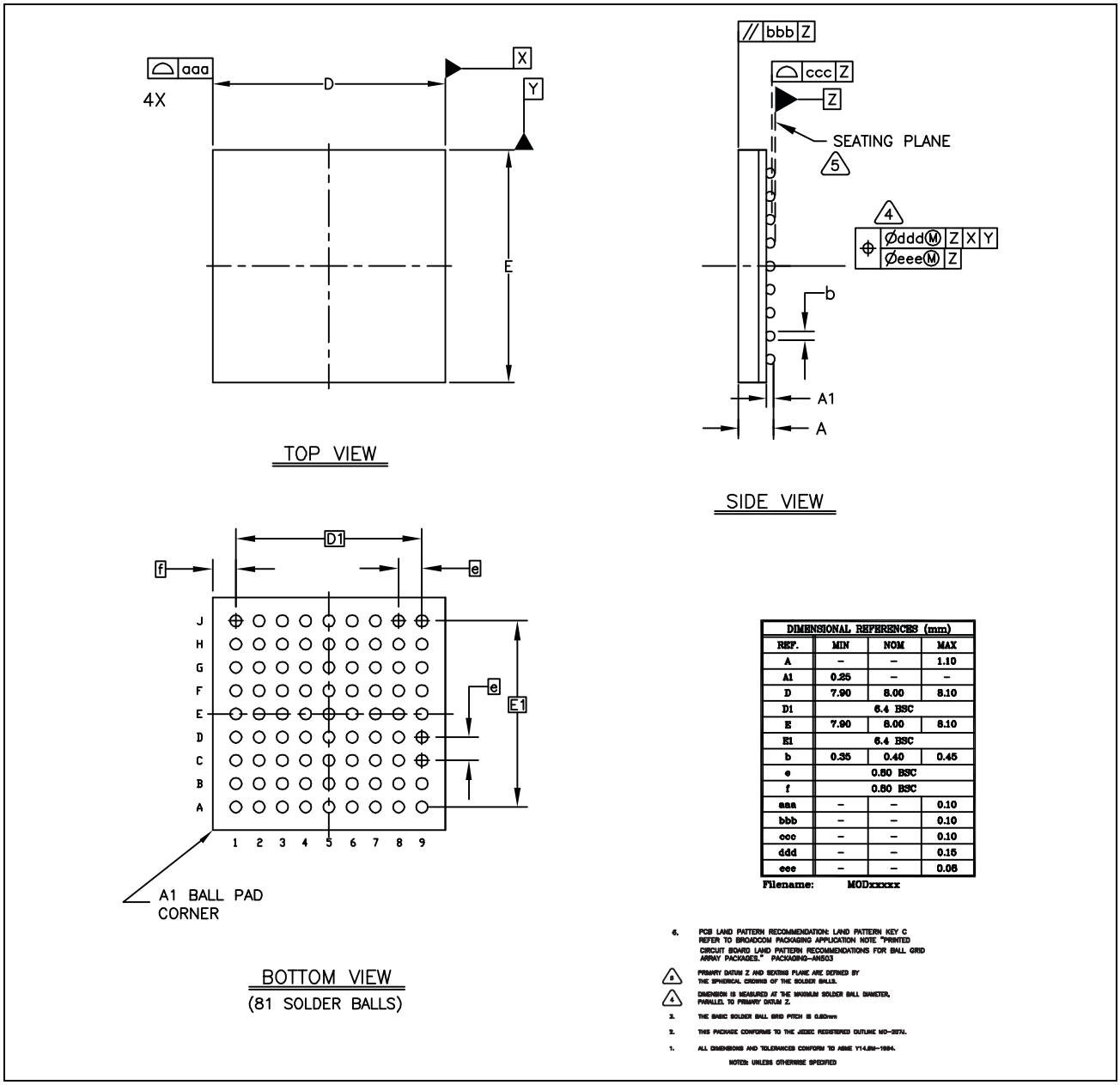


Table 42. Values of I²S Electrical Timing Burst (Slave Rx Only)—Long Frame WS Characteristics

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	I²S bit clock frequency	–	–	24	MHz
2	I²S bit clock low time	20.8	–	–	ns
3	I²S bit clock high time	20.8	–	–	ns
4	I2S_WS setup time	8	–	–	ns
5	I2S_IN setup	8	–	–	ns
6	I2S_IN hold	8	–	–	ns

4. Mechanical Information

Figure 30. 81-Pin FBGA



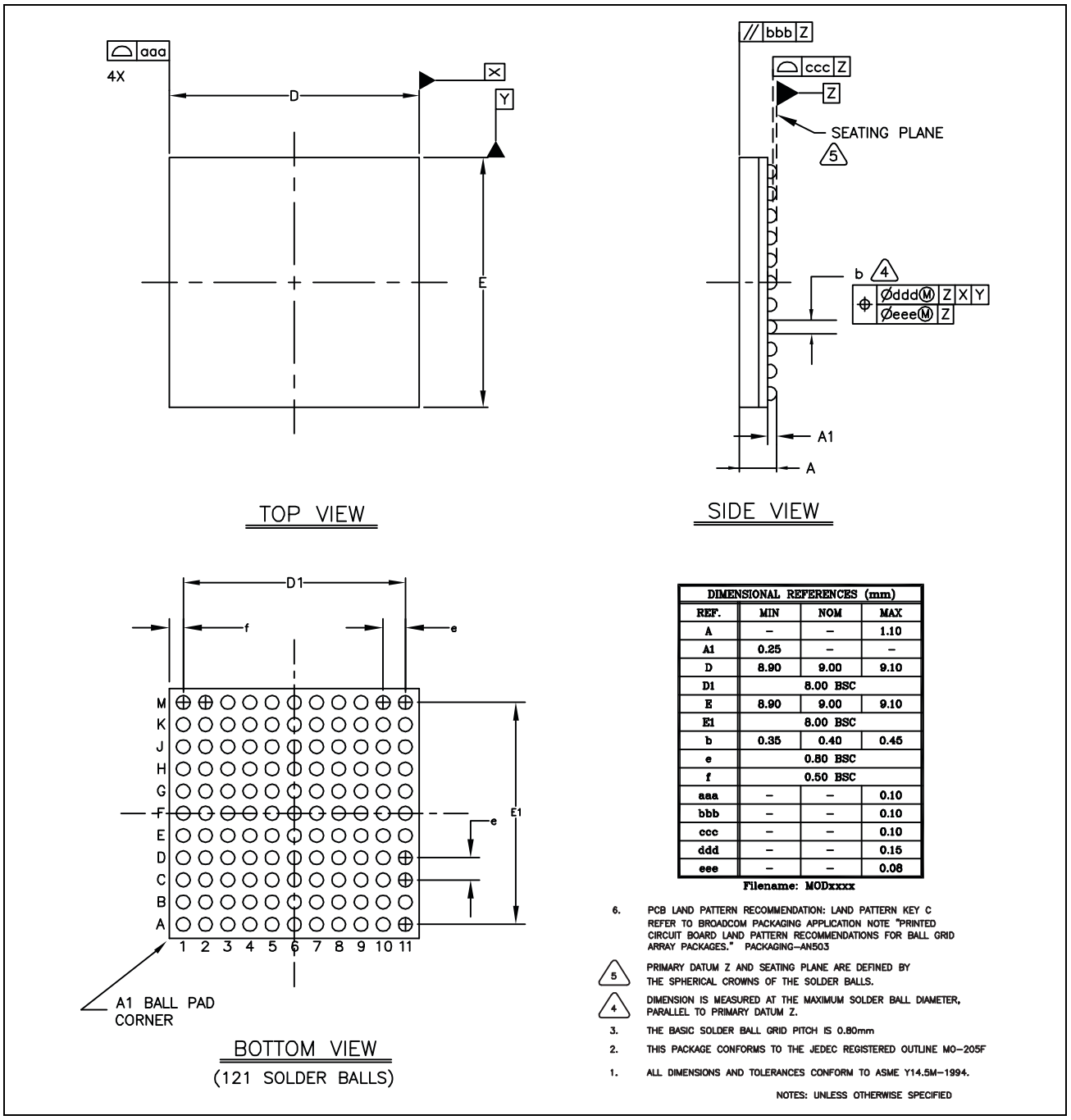
DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.10
A1	0.25	–	–
D	7.90	8.00	8.10
D1		6.4 BSC	
E	7.90	8.00	8.10
E1		6.4 BSC	
b	0.35	0.40	0.45
e		0.80 BSC	
f		0.80 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.10
ddd	–	–	0.15
eee	–	–	0.08

Filename: MODxxxxx

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY C REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES." PACKAGING-AN503
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
3. THE BASIC SOLDER BALL GRID PITCH IS 0.80mm
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-207A.
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 31. 121-Pin FBGA



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.10
A1	0.25	–	–
D	8.90	9.00	9.10
D1		8.00 BSC	
E	8.90	9.00	9.10
E1		8.00 BSC	
b	0.35	0.40	0.45
e		0.80 BSC	
f		0.50 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.10
ddd	–	–	0.15
eee	–	–	0.08

Filename: MODxxxx

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY C REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES." PACKAGING–AN503

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

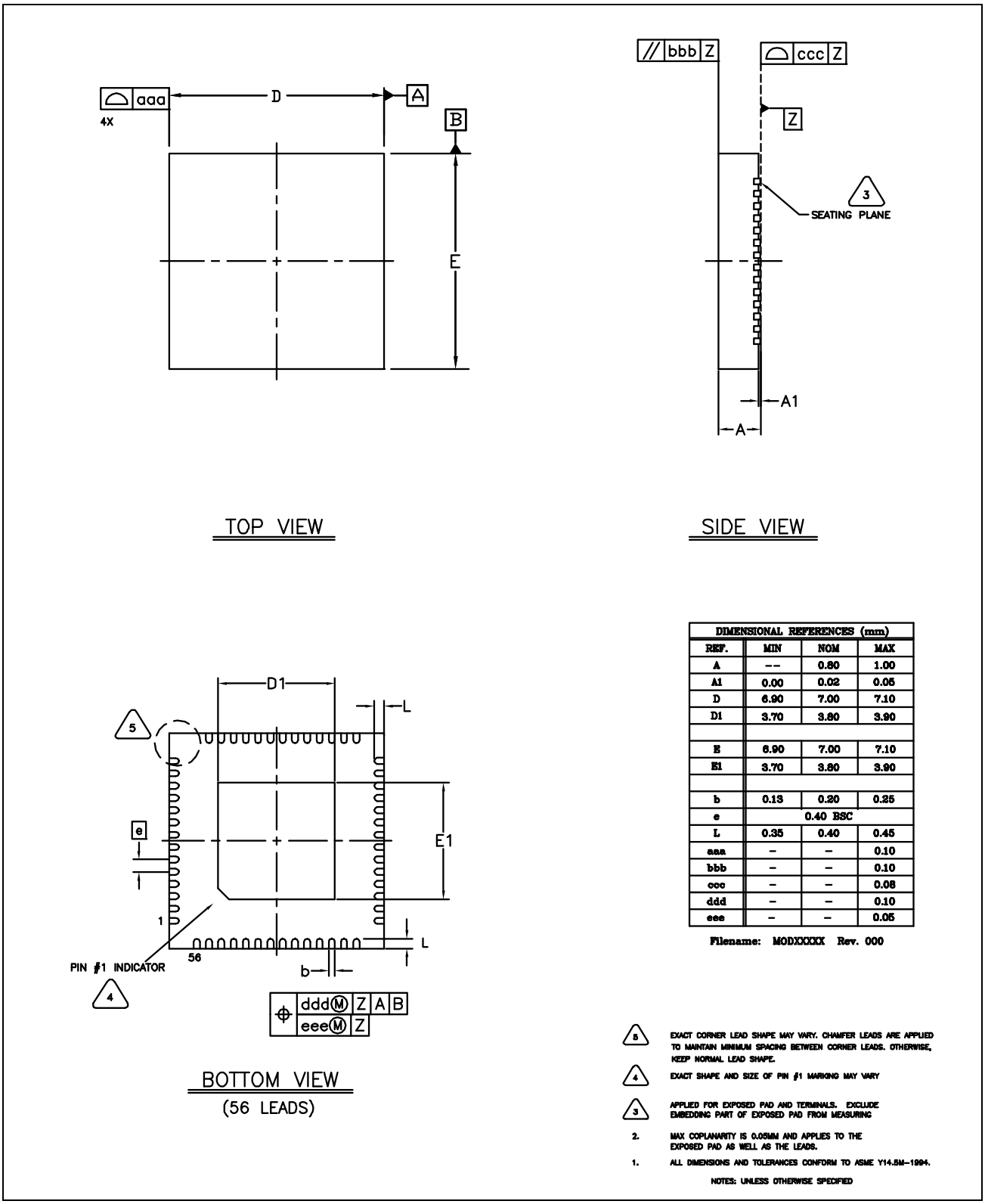
3. THE BASIC SOLDER BALL GRID PITCH IS 0.80mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–205F

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 32. 56-Pin QFN



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	--	0.80	1.00
A1	0.00	0.02	0.05
D	6.90	7.00	7.10
D1	3.70	3.80	3.90
E	6.90	7.00	7.10
E1	3.70	3.80	3.90
b	0.13	0.20	0.25
e		0.40 BSC	
L	0.35	0.40	0.45
aaa	-	-	0.10
bbb	-	-	0.10
ccc	-	-	0.08
ddd	-	-	0.10
eee	-	-	0.05

Filename: MODXXXXX Rev. 000

5. EXACT CORNER LEAD SHAPE MAY VARY. CHAMFER LEADS ARE APPLIED TO MAINTAIN MINIMUM SPACING BETWEEN CORNER LEADS. OTHERWISE, KEEP NORMAL LEAD SHAPE.
4. EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY
3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING
2. MAX COPLANARITY IS 0.05MM AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

4.0.1 Tape Reel and Packaging Specifications

Table 43. CYW20733 8 × 8 × 1.0 mm FBGA 81-Pin Tape Reel Specifications

Quantity per reel	2500 pieces
Reel diameter	13 inches
Hub diameter	7 inches
Tape width	16 mm
Tape pitch	12 mm

Table 44. CYW20733 9 x 9 x 1.0 mm FBGA 121-Pin Tape Reel Specifications

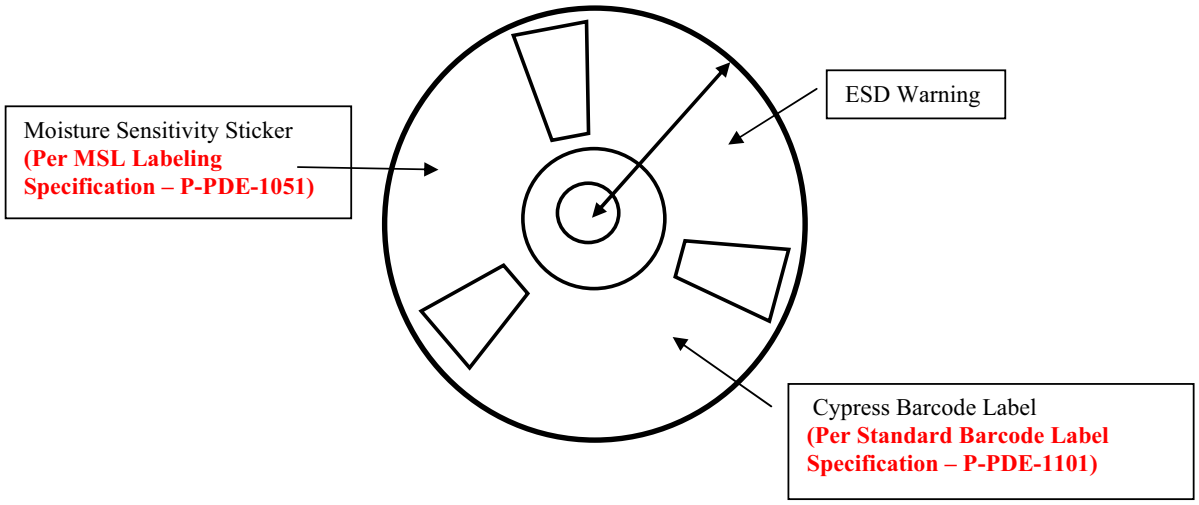
Quantity per reel	1500 pieces
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	16 mm
Tape pitch	12 mm

Table 45. CYW20733 7 x 7 x 1.0 mm QFN 56-Pin Tape Reel Specifications

Quantity per reel	2500 pieces
Reel diameter	13 inches
Hub diameter	7 inches
Tape width	16 mm
Tape pitch	12 mm

Figure 33. CYW20733 Reel/Labeling/Packaging Specification

Reel Specifications:



Device Orientation/Mix Lot Number:

Each Reel may contain up to three individual lot numbers within 13 work weeks. These individual lots must be labeled on the box, moisture barrier bag and reel.

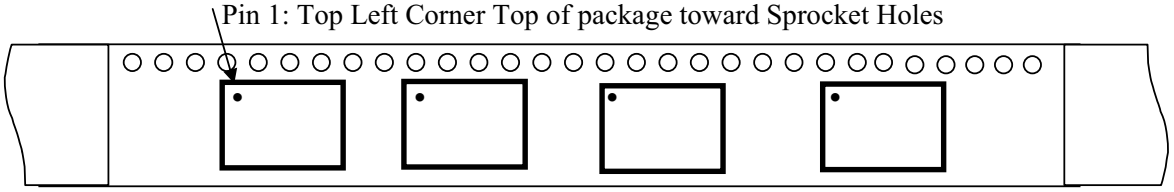


Figure 34. CYW20733 9 × 9 FBGA Package Tray (1 of 2)

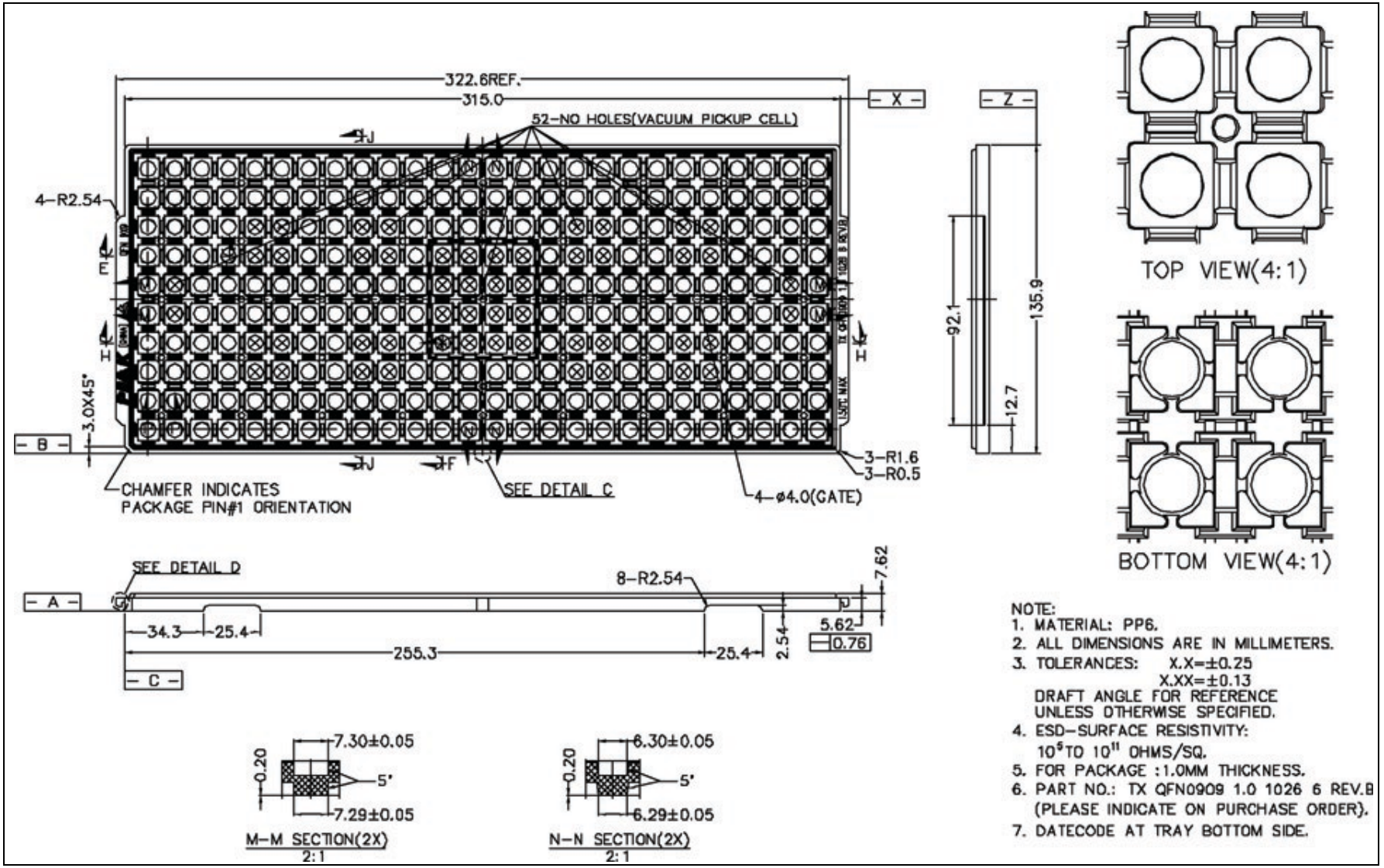


Figure 35. CYW20733 9 × 9 FBGA Package Tray (2 of 2)

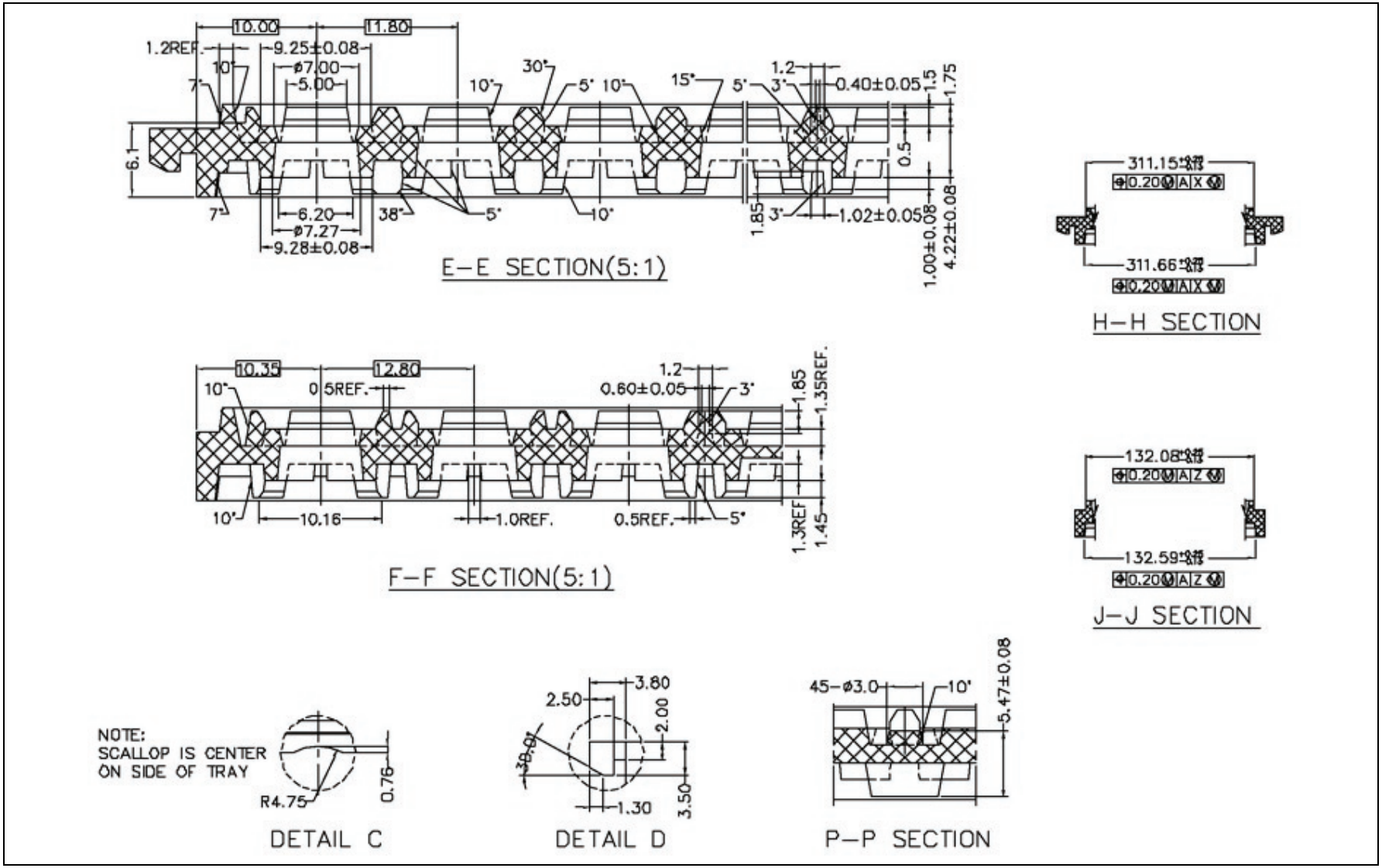


Figure 36. CYW20733 8 × 8 FBGA Package Tray (1 of 2)

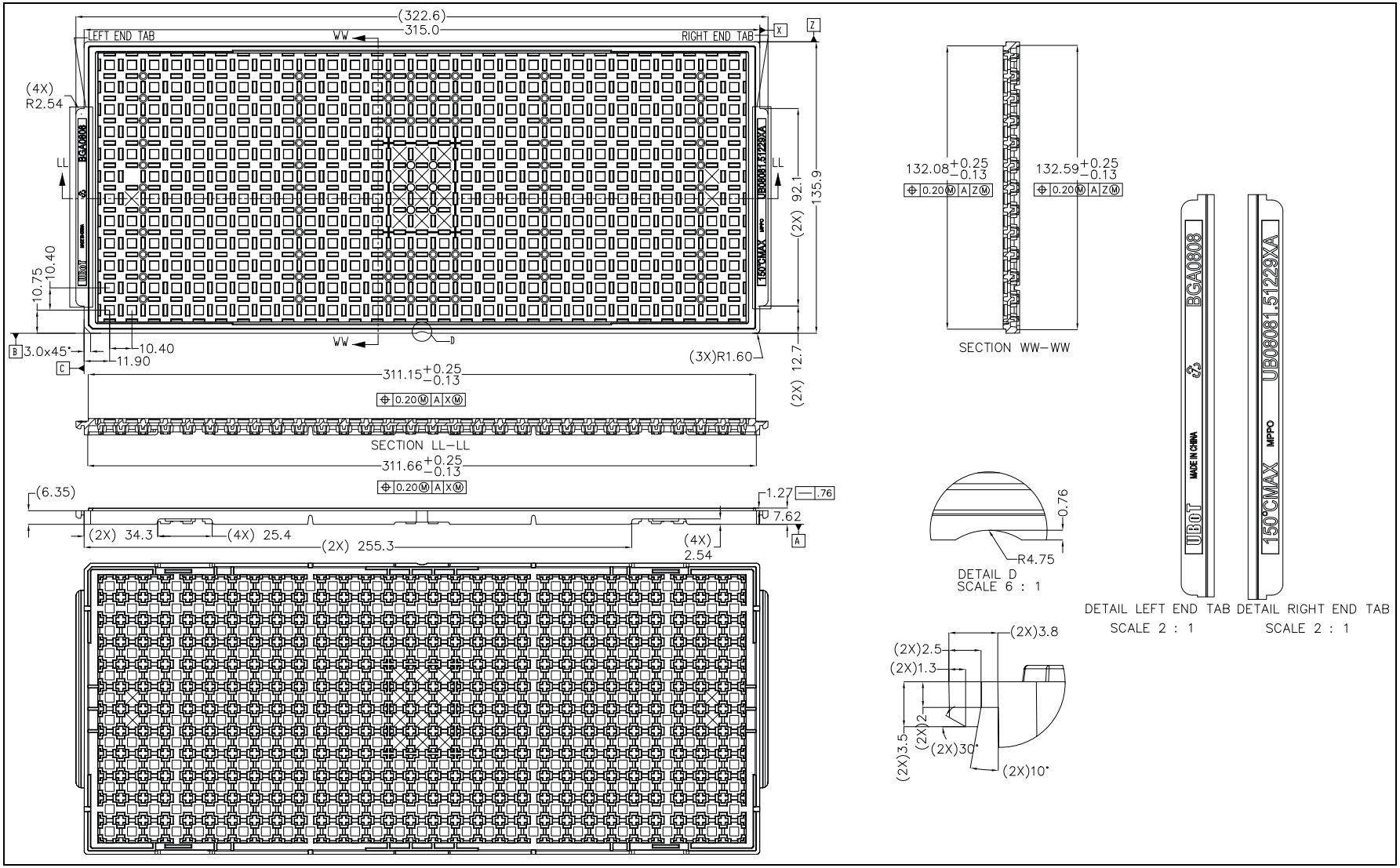
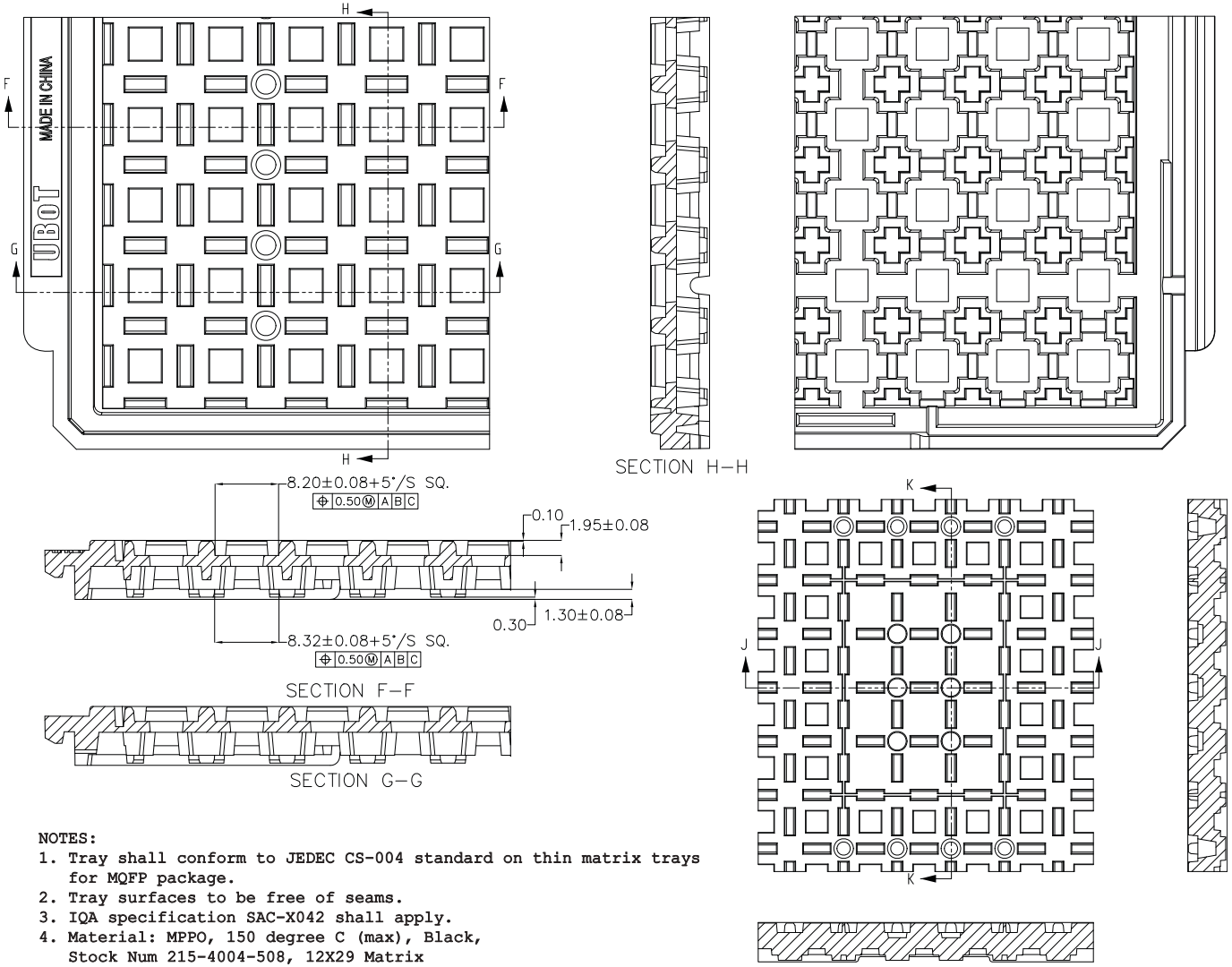


Figure 37. CYW20733 8 × 8 FBGA Package Tray (2 of 2)



NOTES:
1. Tray shall conform to JEDEC CS-004 standard on thin matrix trays for MQFP package.
2. Tray surfaces to be free of seams.
3. IQA specification SAC-X042 shall apply.
4. Material: MPPO, 150 degree C (max), Black, Stock Num 215-4004-508, 12X29 Matrix

5. Ordering Information

Table 46. Ordering Information

Part Number	Package	Ambient Operating Temperature
CYW20733A3KFB1G	Commercial 81-pin FBGA	0°C to 70°C
CYW20733A3KFB2G	Commercial 121-pin FBGA	0°C to 70°C
CYW20733A3KML1G	Commercial 56-pin QFN	0°C to 70°C

6. IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

A. Acronyms and Abbreviations

The following list of acronyms and abbreviations may appear in this document.

For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary

Acronym	Description
ADC	analog-to-digital converter
AFH	adaptive frequency hopping
AHB	advanced high-performance bus
APB	advanced peripheral bus
APU	audio processing unit
ARM7TDMI-S™	Acorn RISC Machine 7 Thumb instruction, Debugger, Multiplier, Ice, Synthesizable
BSC	Broadcom Serial Control
BTC	Bluetooth® controller
COEX	coexistence
DFU	device firmware update
DMA	direct memory access
EBI	external bus interface
HCI	Host Control Interface
HV	high voltage
IDC	initial digital calibration
IF	intermediate frequency
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low drop-out
LHL	lean high land
LPO	low power oscillator
LV	LogicVision™
MIA	multiple interface agent
PCM	pulse code modulation
PLL	phase locked loop
PMU	power management unit

Acronym	Description
POR	power-on reset
PWM	pulse width modulation
QD	quadrature decoder
RAM	random access memory
RF	radio frequency
ROM	read-only memory
RX/TX	receive, transmit
SPI	serial peripheral interface
SW	software
UART	universal asynchronous receiver/transmitter
UPI	µ-processor interface
USB	universal serial bus
WD	watchdog

Document History

Document Title: CYW20733 Single-Chip Bluetooth Transceiver Wireless Input Devices Document Number: 002-14859				
Revision	**ECN**	**Orig. of Change**	**Submis-sion Date**	**Description of Change**
**	–	–	07/23/2010	20733-DS00-R Initial release
*A	–	–	07/20/2010	Updated: Table 10: “Pin Descriptions,” on page 35 and Table 11: “GPIO Pin Descriptions,” on page 38. Figure 13: “81-Pin FBGA Ball Map,” on page 44. Table 16: “Integrated Audio Amplifier Electrical Specifications,” on page 48. Table 25: “PCM Electrical Timing Slave—Short Frame Sync Characteristics,” on page 57. Table 26: “Values of PCM Electrical Timing Master—Short Frame Sync Characteristics,” on page 58. “PCM Interface Timing” on page 57. “I2S Timing” on page 63.
*B	–	–	08/30/2010	20733-DS02-R Updated: “Microprocessor Unit” on page 13: ROM memory capacity. “Link Control Layer” on page 15: Bluetooth Link Controller tasks. “UART Interface” on page 17: normal baud rate mode. “GPIO Port” on page 23. “Theory of Operation” on page 25: mouse decoder PWMs. “ADC Port” on page 26: analog input channels. Table 7: “CYW20733 First SPI Set (Master Mode),” on page 28. Table 11: “Pin Descriptions,” on page 35 and Table 12: “GPIO Pin Descriptions,” on page 37. Figure 13: “81-Pin FBGA Ball Map,” on page 44. Added: “Peripheral UART Interface” on page 19.
*C	–	–	10/25/2010	20733-DS03-R Updated: “General Description” and “Features” on page 1 TBD for second package changed to 121-pin, 9 mm x 9 mm FBGA, throughout the document. Table 11: “Pin Descriptions,” on page 39 (added 121-pin info) Table 12: “GPIO Pin Descriptions,” on page 41 (added 121-pin info) Figure 14: “121-Pin FBGA Ball Map,” on page 49 (added) Figure 30: “81-Pin FBGA,” on page 73 Figure 31: “121-Pin FBGA,” on page 74 (121-pin outline drawing, added) Table 38: “CYW20733 8 × 8 × 1.0 mm FBGA TBD Tape Reel Specifications,” on page 75 Table 39: “CYW20733M 9 x 9 x 1.0 mm FBGA TBD Tape Reel Specifications,” on page 75 Figure 33: “CYW20733 9×9 FBGA Package Tray (1 of 2),” on page 77 Figure 35: “CYW20733 8×8 FBGA Package Tray (1 of 2),” on page 79 Table 40: “Ordering Information,” on page 81
*D	–	–	04/04/2011	20733-DS04-R Updated: Figure 1: “Functional Block Diagram,” on page 2 “UART Interface” on page 19 Table 1: “Common Baud Rate Examples,” on page 20 Table 5: “XTAL Oscillator Characteristics,” on page 25 “Port 0–Port 1, Port 8 – Port 18, Port 20 – Port 23, and Port 28 – Port 38” on page 26 Table 6: “Sampling Rate and Effective Number of Bits,” on page 29 Table 12: “GPIO Pin Descriptions,” on page 40 Table 16: “ADC Specifications,” on page 50 Table 19: “Current Consumption, Class 1,” on page 52 Table 20: “Current Consumption, Class 2 (0 dBm),” on page 53 (added) Table 21: “Receiver RF Specifications” on page 54 Table 22: “Transmitter RF Specifications,” on page 55 Section 5: “Ordering Information,” on page 81

Document Title: CYW20733 Single-Chip Bluetooth Transceiver Wireless Input Devices Document Number: 002-14859				
*E	–	–	06/29/2011	20733-DS05-R Updated: Figure 1: “Functional Block Diagram,” on page 2 “GPIO Port” on page 25 “High Current I/O” on page 34 Table 10: “Pin Descriptions,” on page 36 Figure 13: “121-Pin FBGA Ball Map,” on page 46 Table 15: “ADC Specifications,” on page 48 Table 17: “Current Consumption, Class 1,” on page 49 Table 18: “Current Consumption, Class 2 (0 dBm),” on page 51 Added: Table 19: “Current Consumption,” on page 52Removed: “Integrated Filterless Class-D Audio Amplifier,” on page 35 Table 16: “Integrated Audio Amplifier Electrical Specifications,” on p. 49.
*F	–	–	03/01/2012	20733-DS06-R Updated: Table 7: “CYW20733 First SPI Set (Master Mode),” on page 32 Table 10: “Pin Descriptions,” on page 38 Table 11: “GPIO Pin Descriptions,” on page 41 Table 15: “ADC Specifications,” on page 52 Table 17: “Current Consumption, Class 1,” on page 53 Table 18: “Current Consumption, Class 2 (0 dBm),” on page 55 Notes in Table 20 on page 57 and Table 21 on page 59 Table 23: “Values of SPI1 Timing Characteristics,” on page 61 Table 39: “CYW20733 8 × 8 × 1.0 mm FBGA 81-Pin Tape Reel Specifications,” on page 80 Table 40: “CYW20733 9 x 9 x 1.0 mm FBGA 121-Pin Tape Reel Specifications,” on page 80 Added: Information related to the 56-pin QFN package on page 1 “56-Pin QFN Diagram” on page 50 Table 24: “Values of SPI2 Timing Characteristics,” on page 62 Figure 32: “56-Pin QFN,” on page 79 Table 41: “CYW20733 7 x 7 x 1.0 mm QFN 56-Pin Tape Reel Specifications,” on page 80 Figure 33: “CYW20733 Reel/Labeling/Packaging Specification,” on page 81
*G	–	–	03/19/2012	20733-DS07-R Updated: Notes in Table 23: “Values of SPI1 Timing Characteristics,” on page 65 and Table 24: “Values of SPI2 Timing Characteristics,” on page 66
*H	–	–	05/18/2012	20733-DS08-R Updated: Table 8: “CYW20733 Second SPI Set (Master Mode),” on page 33. Table 9: “CYW20733 Second SPI Set (Slave Mode),” on page 34.
*I	–	–	06/08/2012	20733-DS09-R Updated: Bluetooth HID profile version 1.0 to 1.1 on the cover page. “Calibration” on page 15. “Triac Control” on page 38. “Cypress Proprietary Control Signalling and Triggered Broadcom Fast Connect” on page 38. Table 15: “ADC Specifications,” on page 56 by fixing the Conditions for the Reference settling time and Input resistance parameters. Table 20: “Receiver RF Specifications” on page 59 by updating Df to uf in the inter-modulation performance row. “SPI Timing” on page 63.
*J	–	–	08/30/2012	20733-DS10-R Updated: Table 43: “Ordering Information,” on page 89.
*K	–	–	10/01/2012	20733-DS11-R Updated: Cover page features to include Class-D audio amplifier. Figure 1: “Functional Block Diagram,” on page 2 by adding Class-D audio driver. Table 11: “Pin Descriptions,” on page 43. Figure 14: “56-Pin QFN Diagram,” on page 55. Added: “Integrated Filterless Class-D Audio Amplifier” on page 40. Table 17: “Integrated Audio Amplifier Electrical Specifications,” on page 58

Document Title: CYW20733 Single-Chip Bluetooth Transceiver Wireless Input Devices Document Number: 002-14859				
*L	–	–	11/26/2012	20733-DS12-R Updated: Table 17: “Integrated Audio Amplifier Electrical Specifications,” on page 58. Table 21: “Current Consumption,” on page 61.
*M	–	–	01/21/2013	20733-DS13-R Updated: Table 12: “GPIO Pin Descriptions,” on page 46.
*N	–	–	05/31/2013	20733-DS14-R Updated: Table 45: “Ordering Information,” on page 91.
*O	–	–	08/12/2013	20733-DS15-R Updated: Table 21: “Current Consumption,” on page 62.
*P	–	–	09/25/2013	20733-DS16-R Updated: Table 4: “Reference Crystal Electrical Specifications,” on page 26.
*Q	–	–	07/10/2015	20733-DS17-R **Updated** document status.
*R	5487130	UTSV	10/21/2016	Updated to Cypress Template Added Cypress part numbering scheme
*S	5962319	AESATMP9	11/09/2017	Updated logo and copyright.

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